Chapter 1

Introduction

1-1 Overview of polysilicon thin-film transistor technology

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have much attention because of their widely applications in active matrix (AM) liquid crystal displays (LCDs),[1-1] and organic light-emitting displays (OLEDs).[1-2] Besides large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs),[1-3] static random access memories (SRAMs),[1-4] electrical programming read only memories (EPROM),[1-5] electrical erasable programming read only memories (EEPROMs),[1-6] linear image sensors,[1-7] thermal printer heads,[1-8] photo-detector amplifiers,[1-9] scanners, and neutral networks.[1-10] Comparing with amorphous silicon (a-Si:H) TFTs, although the main advantages of the a-Si:H TFT are the low temperature process that can avoid damaging the glass substrate and the low leakage current that can avoid gray level shift as the TFT is turned off. However, the low electron field effect mobility as these devices adopted on glass limits the capability of advanced and integrated circuit. Poly-Si TFTs can provide carrier mobility much improved in poly-Si film and the capability to integrate panel array and peripheral driving circuit on the same substrates, resulting in higher aperture ratio and lower parasitic gate-line capacitance for better display performance. This provides the opportunity of using poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Among the poly-Si technologies, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are primarily applied on glass substrate since higher process temperature may cause the substrate bent and twisted. Up to now, dozens of researches have been made to

develop various technologies for improving the performance and reliability of LTPS TFTs. Since the electron field-effect mobility of LTPS TFTs is larger than a-Si:H TFTs, that is enough to used as peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate, namely, system-on-glass (SOG) technology.

	a-Si:H TFTs	Polysilicon TFTs
Advantage:	Cheap and reliable technology for very large area IC.	Higher speed , Inherent stability, brighter and higher resolution.
Application:	Flat panel displays, imagers, printers, copiers, consumer products.	High-resolution projection displays.
Market:	Probably the second most important technology (after CMOS and MOS technology).	Challenge a-Si:H in future.
Disadvantage:	Very slow technology and sensitive to heat and light, reduced brightness.	Expensive due to the higher processing temperatures, larger OFF state current leakage.

Table.1-1 Comparison of amorphous Si and polysilicon TFTs

1-2 System on Glass (SOG)

Panel-sized drivers possess a length approximate to that of LCD width or height,

have identical outputs for scan and column lines, and do not require tape-carrier packages (TCPs) or printed circuit boards (PCBs) in assembly. As the display resolution increases, assembly becomes more complicated because the place around the panel is needed for many large scale integrated (LSI) circuits and printed board, while the space available in AMLCDs is usually limited. The use of peripheral circuits and the assembly processes are usually so much that the reduction of manufacturing cost is inhibited. As a result, "System-on-Glass," which mounts a screen and its peripheral circuits on the same glass. The successful implementation of this technology will lead to a substantial savings in costs by shortening the display manufacturing (integration of peripheral circuits can also decrease the module weight) and inspection processes while maintaining a level of high reliability.

Since LTPS TFTs can provide the higher carrier field effect mobility, some peripheral circuits used in AMLCD can adopt these TFTs as the transistors and be integrated on glass. In many works, poly-Si TFTs have demonstrated a great advantage over those built-in a-Si ones even in large size active matrix displays with the peripheral circuit integrated on the same substrate. With advanced poly-si technology and higher carrier mobility in poly-Si TFTs in the future, it can be estimated that the peripheral circuit may be fully integrated on glass.

1-3 Defects in poly-Si film

Some problems still exist in applying poly-Si TFTs on SOG displays. In comparison with single-crystalline silicon, in Fig 1-3-1, poly-Si is much in grain boundary defects as well as intra-grain defects,[1-12] and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain

boundary regions to degrade the ON current seriously. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, the typical characteristics such as threshold voltage, subthreshold swing, ON current, mobility and transconductance of TFTs are inferior to those of devices fabricated on single crystal silicon film. To overcome this inherent disadvantage of poly-Si film, many researches have been focused on modifying or eliminating these grain boundary traps. Traps are associated with dangling bonds arising from lattice discontinuities between different oriented grains or at the Si/SiO_2 interface. The most useful method so far to remove traps is to passivate these dangling bonds with hydrogen atoms. The influences of the grain boundary traps on poly-Si TFT device characteristics were evaluated in detail. It can help us to analyze about LTPS TFT variation.

1-4 Motivation

LTPS TFTs are found to suffer serious behavior variation result from the presence of a large number of traps localized in the energy gap. Compare with MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), the variation behaviors of TFTs are much worse than MOSFETs. Variations are introduced by statistical fluctuations in manufacturing process. Since the variation of device behavior would directly affect the circuit performance, it would be very essential to have a clear understanding of how the variation may come and the behaviors the variation could be. Some variations can be reduced by tighter control of process. The normally controllable gross variables presently may include, for example, random dopant fluctuations, local oxide thickness variation, and oxide fixed charge and interface trapped charge etc. However, some variations are inherently uncontrollable such as

grain boundary trap. In the scope of this thesis, the temperature effects in a specific device which has the same defects are taken into consideration. The device variation and temperature dependence are cross examined to analyze the scattering mechanism of turn-on characteristics. They better understanding of temperature dependence is helpful to develop the device model.

1-5. Thesis Organization

Chapter 1 Introduction

1-1 Overview of polysilicon thin-film transistor technology

1-2 System on Glass(SOG)

1-3 Defects in poly-Si film

1-4 Motivation

1-5 Thesis Organization

Chapter 2 Temperature effects of LTPS TFT

2-1 Parameter extraction and analysis method

2-1-1 Typical device parameters

2-1-2 Statistical analysis method

2-2 N-type TFT

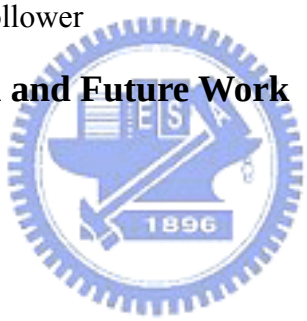
2-2-1 Device Fabrication

2-2-2 Temperature effect

2-2-3 Statistical Conventional Parameter Distribution

2-3 P-type TFT

2-3-1 Device Fabrication

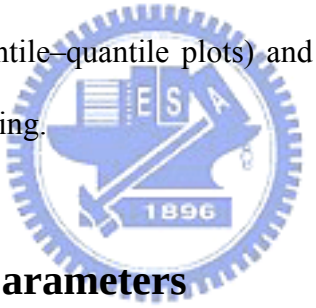


Chapter 2.

Temperature Effects for LTPS TFT

2-1 Parameter extraction and analysis method

In this section, we introduce the extraction methods for typical parameters of the TFTs and the statistical approaches to analyze the distribution of these parameters in this thesis. Threshold voltage Vth, electron mobility Mu and subthreshold swing S.S. are chosen to be analyzed since these three important indices are the typical and important parameters to describe the turn-on behavior of devices. To examine the distribution and the deviation from normal distribution, we adopt the histogram, the Q-Q plot (quantile–quantile plots) and the detrend Q-Q plots, which will be explained in the following.



2-1-1 Typical device parameters

Determination of the threshold voltage

Plenty ways are used to determinate the threshold voltage which is the most important parameter of semiconductor devices. The method to determinate the threshold voltage in my thesis is the constant drain current method that the voltage at a specific drain current I_N is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified at 10nA for $V_D = 0.1$ V.

Determination of the subthreshold swing

Subthreshold swing *S.S* (V/dec) is a typical parameter to describe the control ability of gate toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The subthreshold swing is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, S.S is extracted at the I_d-V_g curve for V_d=0.1V. We defined the sub-threshold swing (S.S) is the minimum value as

$$S.S = \left[\frac{\partial(\log I_{ds})}{\partial V_{gs}}\right]^{-1} \tag{2-1}$$

Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance g_m at low drain voltage. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{TH})V_D - \frac{1}{2}V_D{}^2] \tag{2-2}$$

where

C_{ox} is the gate oxide capacitance per unit area, W is channel width, L is channel length,V_{TH} is the threshold voltage. If V_D is much smaller than V_G-V_{TH} (i.e. V_D << V_G-V_{TH}) and $V_G > V_{TH}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \tag{2-3}$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \qquad (2\text{-}4)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_D}\mathrm{g_m} \qquad (2\text{-}5)$$

2-1-2 Statistical analysis method

In statistics, the standard deviation value, σ, is usually used to investigate the distribution of the observed value. The standard deviation value is given as

$$\sigma \equiv \sqrt{\frac{1}{n}\sum_n (\chi - \bar{\chi})^2} \quad \text{where } \chi \text{ is the observe value} \qquad (2\text{-}6)$$

This parameter represents the difference between the observed values and the corresponding mean value. In a normal distribution, 99.7% of the total observed samples will fall in the region three times of σ from the average value. In other words, three times of the deviation value will provide the information how broad this distribution may be. If σ is large, it means that the value of the observed samples will fall in a large range and result in the broad distribution in the histogram. By simply adding the average value and three times of the deviation value, we can realize the range that most of the observed values actually fall in, even the distribution is not a Gaussian distribution.

In order to examine the distribution of measured data and the deviation from the normal distribution, we adopt the histogram, the Q-Q plot (quantile–quantile plots) and the detrend Q-Q plot. The histogram is the most common graph to examine the distribution of an observed value. A histogram is a rectangular graph of a frequency distribution. To test the normality of the distribution, the graphical methods include the use of probability plots are developed. These can be either P-P plots

(probability–probability plots), in which the empirical probabilities are plotted against the theoretical probabilities for the distribution, or Q-Q plots (quantile–quantile plots), in which the sample points are plotted against the theoretical quantiles. The Q-Q plots are more common because they are invariant to differences in scale and location. If the assumed population is correct, then the observed value and the expected value for each case would be very close to each other. If the observations come from a specific distribution, then the plotted points should roughly lie on a straight line. On the other hand, if the assumed population is not correct, then the observed and expected value would not be approximately the same and the points in this plot would not follow the 45° straight line. Thus, if the points in this plot are close to the line of identity, this plot supports the reasonableness of the assumed population distribution. For the same reason, if the plotted points deviate markedly from the line of identity, then the plots also provide evidence that the assumed distribution is not the appropriate model to describe the observed value. Especially for the normal distribution, the Q-Q plots are known as the normal probability plots, which are adopted in this thesis.

A residual is the difference between an observed value and the corresponding anticipated value. A graphic presentation of residuals, called a residual plot, is useful for highlighting major departures between the observed and the anticipated patterns or relationships in a data set. The detrend Q-Q plot is one of the residual analysis. The residual analysis refers to a set of diagnostic methods for investigating the appropriateness of a regression model utilizing the residuals. If a regression model is appropriate, the residuals should reflect the properties ascribed to the mode error terms ε_i. For instance, since regression model assumes that the ε_i are normal random variables with constant variance, the residuals should show a pattern consistent with these properties. If the model is appropriate, the residuals should reflect the properties ascribed to the model error terms. Using the normal probability plots of the residuals,

where the ranked residuals are plotted against their expected values under normality, we may further investigate the difference between the distribution of the measured data and the normal distribution.

2-2 N-type TFT

2-2-1 Device Fabrication

The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on a glass substrate, then excimer laser XeCl was used to crystallize the a-Si:H film, followed by poly-Si active area definition. Subsequently, a gate insulator was deposited before the metal gate formation, and source/drain doping was performed next to make the n-type devices in a self-align configuration. A Lightly doped drain (LDD) structure was used on the devices. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. I-V characteristics of many TFTs with channel width W = 20 μm and length L = 6 μm were measured using an HP 4156 semiconductor parameter analyzer at different temperatures. The Fig. 2-2-1 shows the Schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

2-2-2 Temperature effect

Fig. 2-2-2, 2-2-3 and 2-2-4 are the average and deviation of the threshold voltage, electron mobility and subthreshold swing at different temperature. Table 2-1 is the values for these parameters. The Fig 2-2-2 shows the average value AVG of the Mu from 54 to 62 cm^2/VS, the standard deviation STD are 2.69, 2.98, 2.94 cm^2/VS with temperature. From Fig 2-2-3, it can be seen that the average value AVG of the Vth

from 3.02 to 2.24 V, while the standard deviation STD range from 0.14 to 0.08 V with temperature. Refer to the Fig 2-2-4, the average value AVG of the S.S from 0.27 to 0.35 V/dec, the standard deviation STD range from 0.024 to 0.083 V/dec with temperature.

The increase of electron mobility at higher temperature indicates the increased Coulomb scattering by grain boundary traps and ionized impurity scattering.[2-1] Furthermore, the scattering mechanisms can be reconfirmed by investigating the variant ranges at the different temperatures. For the n-type TFTs, the variant range of the mobility is almost the same over the temperatures. Extrinsic effect, parasitic series resistance, were dominant the temperature dependence characteristics. Then, the trap charges in the grain boundaries unchanged in a single device are diverse from device to device. The thermal energy is less influenced the charged defects. Most of n-type TFTs are influenced by such as ionized impurity scattering. The characteristics of device variance are unchanged.

The value of threshold voltage for n-type TFTs significantly increased with decreasing temperature with decreasing temperature, because the Fermi potential is increased as a result of the Fermi level approaching the energy band edge and the influence of the grain boundary traps become more pronounced at lower temperature. The variation suggests that there are different trap densities. Because the influence of threshold voltage is deep state trap density which origin from device dangling bond. Owing to deep state trap density is Gaussian-like distribution. The Fermi level approaches the peak point of Gaussian distribution at higher temperature. The variation is relative small at this region by the view point of statistics. Then, the variation is also comparative small at higher temperature. Fig. 2-2-5 shows temperature dependence for mobility mechanism. [2-2]

The subthreshold swing of TFT is increased as the temperature is increased. The

increase in the subthreshold swing for n-type TFTs is due to the increased influence of the grain boundary traps. The thermionic emission is happened easily at higher temperature. The leakage current is also increased seriously. The leakage component of the reverse biased drain junction is included. At the room temperature, this component is negligible, but it can become significant at higher temperature. The reasons cause the TFT on/off ratio decrease and make the subthreshold swing increase. The trap charges which located at grain boundary suffer much more thermal perturbation as temperature rise. The carriers which have thermionic emission[2-3] considerably depend on the numbers of defect.

Average		Vth (V)	Swing(V/dec)	Mobility(cm^2/Vs)
	30℃	3.0228	0.27149	54
	100℃	2.5118	0.29022	60
	150℃	2.2401	0.34832	62
		Vth (V)	Swing(V/dec)	Mobility(cm^2/Vs)
Standard deviation	30℃	0.139	0.02403	2.69
	100℃	0.094	0.05438	2.98
	150℃	0.077	0.08316	2.94

Table 2-1 The temperature dependence of average values and the standard deviation values for n-type TFT devices.

2-2-3 Statistical Conventional Parameter Distribution

Fig 2-2-5 to 2-2-31 are the Vth, mobility and subthreshold swing of n-type TFTs and the corresponding Q-Q plot and the detrend Q-Q plot at various temperature. It can be seen that Vth, S.S and mobility comprise similar distribution of normal distribution. Refer to the Q-Q plot and the detrend Q-Q plot, the observed values and

the fitting normal distribution values are both very close. LTPS TFTs which have LDD structure are dominant the characteristics distribution. As the temperature increases, the distribution of Vth moves positively away.

2-3 P-type TFT

2-3-1 Device Fabrication

The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on a glass substrate, then excimer laser XeCl was used to crystallize the a-Si:H film, followed by poly-Si active area definition. Subsequently, a gate insulator was deposited before the metal gate formation, and source/drain doping was performed next to make the p-type devices in a self-align configuration. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. I-V characteristics of many TFTs with channel width W = 20 μm and length L = 6 μm were measured using an HP 4156 semiconductor parameter analyzer at different temperatures. The Fig. 2-3-1 shows the Schematic cross-section structure of the p-type poly-Si TFT.

2-3-2 Temperature effect

Fig. 2-3-2, 2-3-3 and 2-3-4 are the average and deviation of the threshold voltage, electron mobility and subthreshold swing at different temperature. Table 2-2 is the values for these parameters. The Fig 2-3-2 shows the average value AVG of the Mu from 96 to 76 cm^2/VS, the standard deviation STD range from 4.05 to 2.45 cm^2/VS with temperature. From Fig 2-3-3, it can be seen that the average value AVG of the Vth from -1.02 to -0.01 V, while the standard deviation STD range from 0.17 to 0.14

V with temperature. Refer to the Fig 2-3-4, the average value AVG of the S.S from -0.19 to -0.95 V/dec, the standard deviation STD range from 0.075 to 0.273 V/dec with temperature.

Fig. 2-3-2 shows the temperature dependences of maximum field effect mobility μ_{max}. The relative standard deviation of mobility μ_{max} is also plotted. For all the devices, negative temperature dependence is observed. Furthermore, the variation of diverse devices decreases with the rise of temperature. By the thermionic emission, most of the carriers can jump over the defect induced potential barriers. In the mean time, the thermal energy can help the holes to run over the scattering of charged traps. Therefore, less Coulomb influence of the traps and the similar lattice structures in the grains lead to the dominance of the phonon scattering, [2-4] and thus the variation range decreases. Even though the lattice scattering thermally prevails, the temperature dependences for the distinct devices are not exactly the same, which reveals the existence of other mechanisms such as Coulomb one. The carriers which pass through the trap center with proportion. Fig. 2-2-5 shows temperature dependence for mobility mechanism.

Similar behavior of the threshold voltage is also obtained in p-type TFT. The absolute value of threshold voltage for p-type TFTs significantly increased with decreasing temperature with decreasing temperature, because the Fermi potential is increased as a result of the Fermi level approaching the energy band edge and the influence of the grain boundary traps become more pronounced at lower temperature. The influence of threshold voltage is deep state trap density which origin from device dangling bond. Owing to deep state trap density is Gaussian-like distribution. The Fermi level approaches the peak point of Gaussian distribution at higher temperature. The variation is relative small at this region by the view point of statistics. Then, the variation is also comparative small at higher temperature. The donor-like trap, which

is located in the lower half of the band gap, plays an important role in the p-type TFT. Accordingly, these results also indicate that the grain boundary trap has an asymmetrical energy distribution in the energy gap.

The subthreshold swing of TFT is increased as the temperature is increased. The increase in the subthreshold swing for p-type TFTs is due to the increased influence of the grain boundary traps. The thermionic emission is happened easily at higher temperature. The leakage current is also increased seriously. The leakage component of the reverse biased drain junction is included. At the room temperature, this component is negligible, but it can become significant at higher temperature. The reasons cause the TFT on/off ratio decrease and make the subthreshold swing increase. The trap charges which located at grain boundary suffer much more thermal perturbation as temperature rise. The carriers which have thermionic emission considerably depend on the numbers of defect.

Average	AVG		Vth (V)	Swing(V/dec)	Mobility(cm^2/VS)
		30℃	-1.0175	-0.18659	96
		100℃	-0.4551	-0.30797	84
		150℃	-0.0053	-0.94814	76
			Vth (V)	Swing(V/dec)	Mobility(cm^2/VS)
Standard deviation	STD	30℃	0.173	0.0075	4.05
		100℃	0.162	0.0149	3.01
		150℃	0.145	0.2728	2.45

Table 2-2 The temperature dependence of average values and the standard deviation values for p-type TFT devices.

2-3-3 Statistical Conventional Parameter Distribution

Fig 2-2-7 to 2-2-21 are the Vth, mobility and subthreshold swing of p-type TFTs and the corresponding Q-Q plot and the detrend Q-Q plot at various temperature. It can be seen that S.S comprise similar distribution of normal distribution. Refer to the Q-Q plot and the detrend Q-Q plot, the observed values and the fitting normal distribution values are both very close. As the temperature increases, the distribution of Vth moves positively away. We should be further detail causes the two peak distribution of conventional device parameters .

2-4 Summaries

In this chapter, the LTPS TFTs temperature effect is investigated with respect to device defects. We first extracted typical device parameter and use statistical method to analyze the thermal characteristics from different devices. It is found as the device temperature increases, the both type TFTs threshold voltage indeed decrease, and subthreshold swing are increased. However, the mobility show the different tendency with temperature. It can be suggested that the dominant turn-on characteristics mechanism of n-type TFT is LDD structure extrinsic parasitic series resistance. Furthermore, we also find the device parameter distributions. Owning to LDD effect, n-type TFT, we notice that the conventional device parameters distribution is normal distribution. However, for p-type TFT, we can see at least two peaks in the chart. The temperature dependences for the devices are not exactly the same. It reveals the existence of other minor mechanisms.

Chapter 3

Operative Mechanism and LTPS TFT Model

3-1 Introduction

Polysilicon Thin Film Transistors (poly-Si TFTs) are widely used in active matrix liquid crystal display (LCDs) to drive the pixel. The characteristics of the TFTs are severely affected by a large number of defect states within the band gap of disordered material. Moreover, the TFTs operate with a floating substrate. As a result, the characteristics of a TFT cannot be modeled accurately by the common bulk MOSFET model. RPI model is a complete model which is based on the universal charge control concept which guarantees stability and conversion. This model provides physical based parameters can be extracted from experimental data. This model includes the following effects for drain current. The conduction in poly-Si is more complex than in crystalline MOSFETs. In the crystalline grains, as in crystalline MOSFETs, drift and diffusion are the main mechanisms of the current in the normal voltage range of operation. Diffusion dominates in the subthreshold regime and drift in the above threshold regime. On the other hand, the carriers have to cross the grain boundary barrier by thermionic field and thermionic emission.

3-2 Operation for TFT DC model

In this section, we will review the conventional unified DC model of TFT.

Voltage	(V_{off})	(V_t)	(V_{on})	(V_{kink})	
Operative regime	Cut-off (leakage)	Sub-threshold	Pseudo-Sub threshold	Above threshold	Kink

Table 3-1 Five operative regimes of LTPS TFTs

The poly-Si TFT models could be divided into three categories: the models that try to incorporate the physics related to individual grain boundaries, [3-1] the models that use close form analytical expressions for current-voltage characteristics, [3-2] and the models based on effective medium. In recent years, several models for poly-Si TFTs have been proposed. Lin et al. obtained an expression for grain barrier height as a function of gate bias and the lateral electric field from a quasi-two-dimensional formulation of Poisson's equation. This solution was incorporated in an expression for the drain current in poly-Si TFTs. Further insight relating the characteristics to the poly-Si material parameters was provided by Fortunato and Magliorato.[3-3] Other solutions use Poisson's equation with the inclusion of space charge due to traps. Still others seek formulations with a minimum of empirical approximations. Although useful for the insight they provide, these expressions tend to be too complication for implementation in circuit simulators. The effective medium approach permits the development of comparatively simple models with only a few easily extractable parameters. Although these parameters cannot always be directly related to material properties, such models are attractive for use in SPICE type circuit simulators.

The above models are mainly developed for long-channel poly-Si TFTs although later versions by Jacunski et al.[3-4] have included physics based formulations of important mechanisms such as the kink effect, the field effect mobility in moderate inversion, and the subthreshold current. Finally, the most recent models based on these semi-empirical effective medium approach also include short-channel effects, drain induced barrier lowering (DIBL), velocity saturation, temperature effects, and mobility degradation at high gate bias.[3-5] The poly-Si TFT models developed by Jacunski et al. are essentially unified models for long-channel devices.

Cut-off regime: Leakage current (thermionic emission)

The current which is due to reverse-bias drain junction leakage in poly-Si TFTs is higher than in crystalline MOSFETs. Because of the presence of grain boundaries and intra grain trap states. The trap-assisted mechanisms include electrical field near drain and temperature and independent of channel length. Thermionic emission is the main mechanism at low drain bias. At moderate drain bias, trap assisted thermionc emission is the dominant leakage mechanism. At high drain bias, the main contribution to the drain current is tunneling from and between the traps. It is given by

$$I_{leak} = I_0 W\left[\exp\left(\frac{\pm B_{lk} V_{ds}}{V_{th}}\right) - 1\right]\left[X_{TFE}(F_p) + X_{TE}\right] + I_{diode} \quad (3\text{-}1)$$

Where F_p is the maximum electric field near the drain and I_0 , B_{lk} are extracted parameter. $X_{TFE}(F_p)$ and X_{TE} are analytical formulation of the theory developed by Bhattacharya et al.

Subthreshold regime (diffusion like model)

In the subthreshold regime, most of the induced charge is trapped in deep acceptor states (for n-channel devices), and the current is dominated by diffusion. This current is limited by source junction potential barrier.

$$\mathrm{I}_{sub} = \mu_s \mathrm{C}_{ox} \frac{\mathrm{W}}{\mathrm{L}} (\eta \mathrm{V}_{th})^2 \exp\left(\frac{\mathrm{V}_{gs} - \mathrm{V}_t}{\eta \mathrm{V}_{th}}\right)\left[1 - \exp\left(\frac{-\mathrm{V}_{ds}}{\eta \mathrm{V}_{th}}\right)\right] \quad (3\text{-}2)$$

Here μ_s is subthreshold mobility, η is the subthreshold ideality factor, and the parameter V_{th} is the thermal voltage and is given by $\mathrm{kT/q}$. Where temperature is device temperature which experimental data shows that the subthreshold swing is a function of temperature. The large subthreshold ideality factor is a result of the polysilicon grain-boundary trap states.

Pseudo-subthreshold regime (c-Si like with MOSFET)

The current is due to carrier drift. The field effect mobility becomes a function of gate bias and accounts for trap states, which increase with gate voltage exponentially. This region based on the crystalline MOSFET model, inversion-charge density increases with VG-Vt linearly. Drain current increases exponentially with gate voltage.

Above Threshold regime

The current is also due to carrier drift. The field effect mobility saturates at a certain value. The inversion-charge density increases with VG-Vt linearly. Drain current increases linearly with gate voltage.

$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gt} - \frac{V_{dse}}{2\alpha_{sat}} \right) V_{dse} \qquad (3\text{-}3)$$

In the above expression, μ_{FET} is the gate voltage-dependent field effect mobility. V_{gt} is defined as $V_{gs} - V_t$, α_{sat} is the body constant and V_{dse} is the effective drain-source voltage:

$$V_{dse} = \frac{V_{ds}}{\left(1 + \left(V_{ds} / V_{sat}\right)^{m_s}\right)^{m_s}} \qquad (3\text{-}4)$$

where

$$V_{sat} = 2^{1/m_s} \alpha_{sat} V_{gt} \qquad (3\text{-}5)$$

α_{sat} accounts for the variation of depletion charge a across the channel, otherwise , also partially accounts for velocity saturation cross the channel.

Kink regime (impact ionization with feedback)

For very large drain biases in saturation, the kink effect is observed. It is modeled as impact ionization generating electron-hole pairs in a narrow region near the drain. The electrons will be swept to the drain contact while the holes are injected into the silicon film and propagate towards the source. Especially in fully depleted (floating body) poly-Si TFTs, this hole current will forward bias the junction between the film and the

source, leading to a reduction of the threshold voltage and a sudden increase of the drain current. The expression can be written as:

$$I_{kink} = \left[\frac{L_{kink}}{L}\right]^{m_{kink}} \left[\frac{V_{ds} - V_{dse}}{V_{kink}}\right] \exp\left[\frac{-V_{kink}}{V_{de} - V_{dse}}\right] I_d \qquad (3\text{-}6)$$

3-3 Variation in Temperature Dependence Effect

Low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted much attention for the higher mobility and better reliability compared to amorphous silicon thin film transistors. However, even the devices fabricated under the identical process, LTPS TFTs still have different electrical characteristics due to the influence from different numbers of the inter-grain and intra-grain defects. The trapping states at the grain boundaries in polysilicon are the key states which limit severely the device performance and make difficult to design the circuit with the state variation. Since the variations are intrinsically introduced by statistical fluctuations in manufacturing processes. The temperature effects in a specific device which has the same defects are taken into consideration. The temperature dependence of the transfer characteristics has three parts; thermal generation region, subthreshold region and ON region. In the thermal generation region, the drain current increases with temperature due to thermal generation of the carriers. For this region of a device operation, the channel activation energy is equal to the conductivity activation energy of the intrinsic poly-Si film. In the subthreshold region, the drain current increases with temperature because the quasi-Fermi level exists between the intrinsic Fermi level and the bottom of band tail states. In the ON state, temperature does not affect the drain current significantly because of low tail state density which is typical for good polycrystalline silicon. The channel activation energy of drain current in the ON state are equal to the

width of the band tail states.

The turn-on characteristics of one p-type LTPS TFT at different temperatures are shown in Fig 3-3-1 A common cross point of the Id-Vg curves at the cross voltage Vx is firstly noticed. At the gate voltage (Vgs) below Vx, the drain current increases with the temperature, while the opposite temperature dependence is observed at higher Vgs. The temperature dependence of the transconductance also changes from positive to negative at even lower gate voltage. It indicates that the superior conducting mechanisms at high and low Vgs are different. At low voltages, the carrier number increase with temperature since more holes can overcome the defect induced potential barriers. In addition, when the temperature gets up, the carriers pass through the area near the trap centers more frequency because the holes move faster. On the contrary, at high Vgs, the decrease of the holes mobility at risen temperature is attributed to the more significant lattice scattering.[3-6] This phonon scattering is so important that the increase owing to the less Coulomb scattering for higher carrier velocity and more carriers induced is overwhelmed.

The cross voltage Vx is a good indication about the thermal balance of invariant phonon scattering and defect-related conducting mechanism. Since both Vx and Vt of the TFTs vary with devices, the relative gate voltage is used instead of the real Vgs value to analyze the behavior of the field effect mobility. Fig 3-3-2 illustrates the average mobility μ_{ave} and the relative mobility deviation σ_{μ}/μ_{ave} in the region between the cross voltage Vx and the threshold voltage Vt in accordance with the relative Vgs. As can be seen, the trend of average mobility is the same as that of a single device, which reflects the common behaviors of the TFTs. Moreover, the relative mobility deviation is large at the voltage close to Vt and at lower temperature where the characteristics of TFTs are profoundly affected by the defects.

The Fig 3-3-3 shows the relationship of |Vx-Vt| verse mobility extracted from

where the transconductance gives maximum for the poly-Si TFTs. It is clear that for the device having less absolute value of Vx-Vt, its mobility is relative large, which indicates that |Vx-Vt| can be declared whether the LTPS TFT conductance characteristics is better or not. This range can describe the number of traps in the TFT device, too. For the device with the crossing voltage at more negative gate bias, the phonon scattering effect prevails later because of the larger number of defects, which results in the lower mobility.

The balance of scattering mechanism is reviewed by changing the drain voltage. When the drain voltage increases, owing to drain induced grain barrier lower (DIGBL), [3-7] the influence of the defects is reduced, thus the decrease of |Vx-Vt| is observed. At the quite high drain voltage, e.g. 10V, where the effect of defects becomes minor, the Vx swerves to shift negatively. It is because the carriers, which originally are retarded by the phonon vibration centers, gain energy from higher electrical field to accelerate and meanwhile the reduction of change ratio for the drain current with different temperatures is also observed.

3-4 Proposed Above-Threshold Model

Corresponding to this phenomenon, a proper temperature model for the mobility should be developed to well describe the device in simulation tools. Fig. 5 shows the transconductance dependences of the gate bias at different temperature for the analytical models and experiment data. The transconductance firstly increases with the gate voltage, and then decreases gradually. The increase is due to the lowering of the potential barrier with increasing gate voltage. When the potential barrier decreases to a value smaller than thermal voltage, the current is limited by surface roughness scattering and thus the transconductance decrease.

A new mobility model modified from RPI's [3-8] is shown as below

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_1\left[\frac{2(V_{GS}-V_t)^m}{\eta_i V_{th}}\right]} + \frac{1}{\mu_0\left(\frac{T}{T_0}\right)^{-\gamma}} \qquad (3\text{-}7)$$

where m, μ_0 and μ_1 are the mobility parameters, η_i is the subthreshold ideality, V_{th} is the thermal voltage. The new feature of the modified temperature model is adding a degradation term of $(T/T_0)^{\gamma}$, where T and T_0 are the temperature and the referenced

temperature respectively, and γ is a new parameter to describe bulk mobility scattering effect. The extracted values of γ are about 0.8, which also vary with devices. This modification will gives better description of the TFT about the cross in the Id-Vg curves.

3-5 Poly-Si TFT Application

3-5-1 Inverter

A Poly-Si TFT inverter consists of two transistors, one n-channel and p-channel. This configuration is widely-used in dc/ac transfer and its application is directly related to the definition of threshold voltage of the TFT. The simplest source configuration in this work is shown in Fig.

3-5-2 Source-Follower

Source follower is defined as an output circuit whose output load is connected in the source circuit of a field-effect transistor and whose input is applied between the gate and the remote end of the source load, which may be at ground potential. This configuration is widely-used in analog circuits and its application is directly related to the definition of threshold voltage of the TFT. The simplest source configuration in this work is shown in Fig. A typical way to specify a source follower is by the voltage drop between the gate Vg and source electrode Vs of the transistor as the source follower stops charging. It is expected that in the initail stage, the voltage difference between gate and source, Vgs, and between drain and source, Vds, are large and the charging behavior of the capacitor is very fast. As time increases, the voltage difference is both decreased and charging behavior becomes slow. Conventionally, when the source follower stops charging, the voltage difference between gate and source will reach the Vth of the transistor.

Chapter 4

Conclusion and Future Work

4-1 Conclusion

LTPS TFTs suffer from serious device characteristic variation due to the number and behavior of defects of the polysilicon film. This thesis has reported the temperature dependence and the cross voltage concerning the conduction mechanisms of poly-Si TFTs. We establish measurement database from identical device process and extracted typical device parameter to analyze the thermal characteristics from many different devices. Furthermore, we also find the device parameter tendencies and distributions with temperature. The difference between the cross voltage and threshold voltage may also be an index for the turn-on characteristics of the LTPS TFTs. This investigation for thermal behaviors statistically is helpful us to develop the accurate LTPS TFT model with temperature effects. A new model is proposed to fit the device transfer characteristics well at different temperatures. This modification will gives better description of the TFT about the cross in the Id-Vg curves.

4-2 Suggestions for Future Work

According to the model of poly-Si TFT based on the concept of physical model studied in this thesis. We want to find the thermal voltage which can define n-type LDD structure model. We should be further investigate bias temperature effect for reliability model and detail causes the two peak distribution of conventional device parameters .

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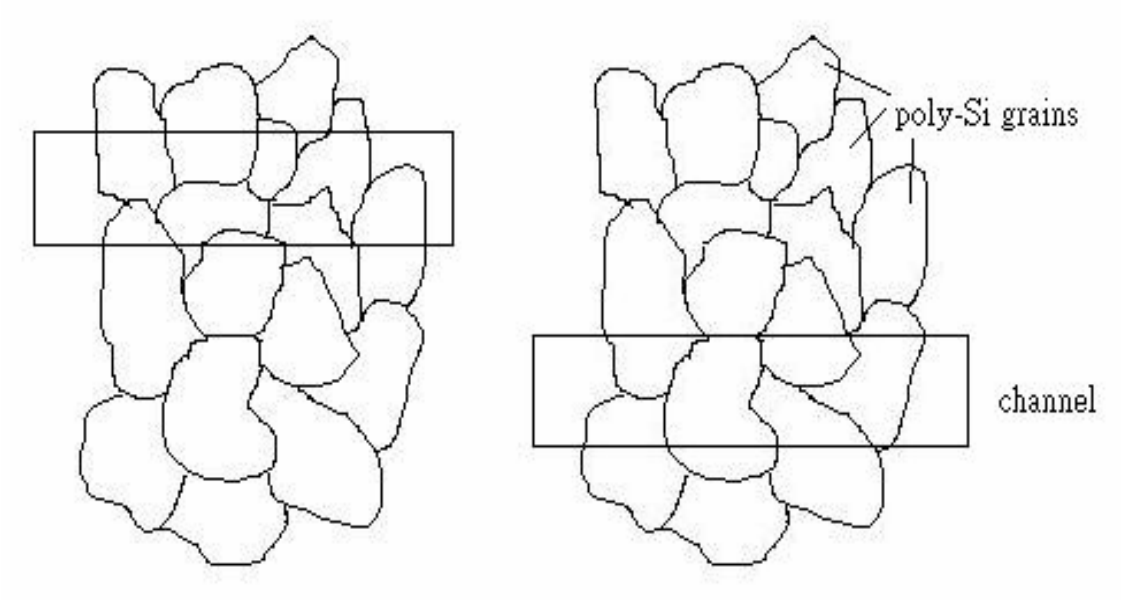

Fig 1-3-1 The diagram of different TFTs with various amount of grain boundaries existing in the channel.

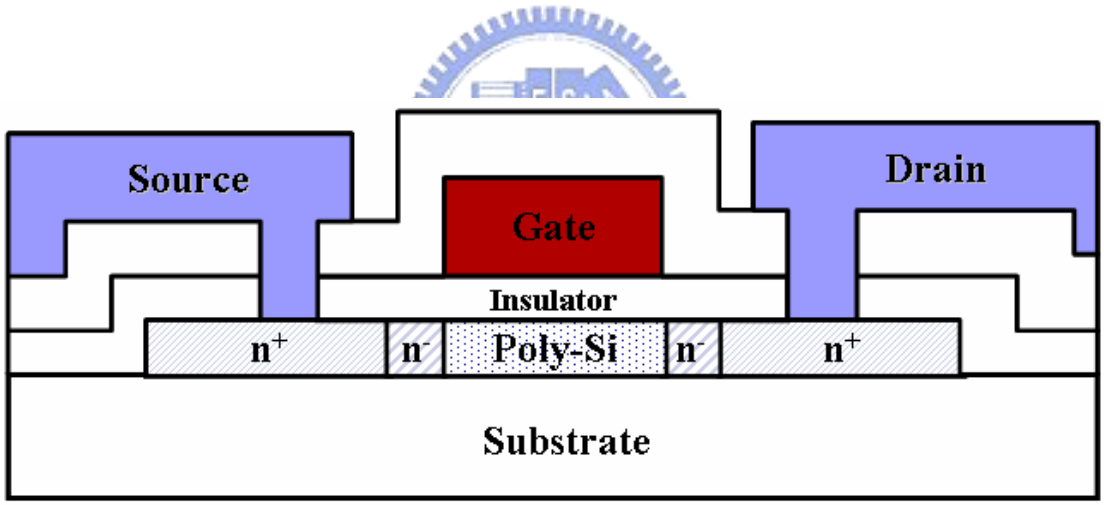

Fig 2-2-1 Schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

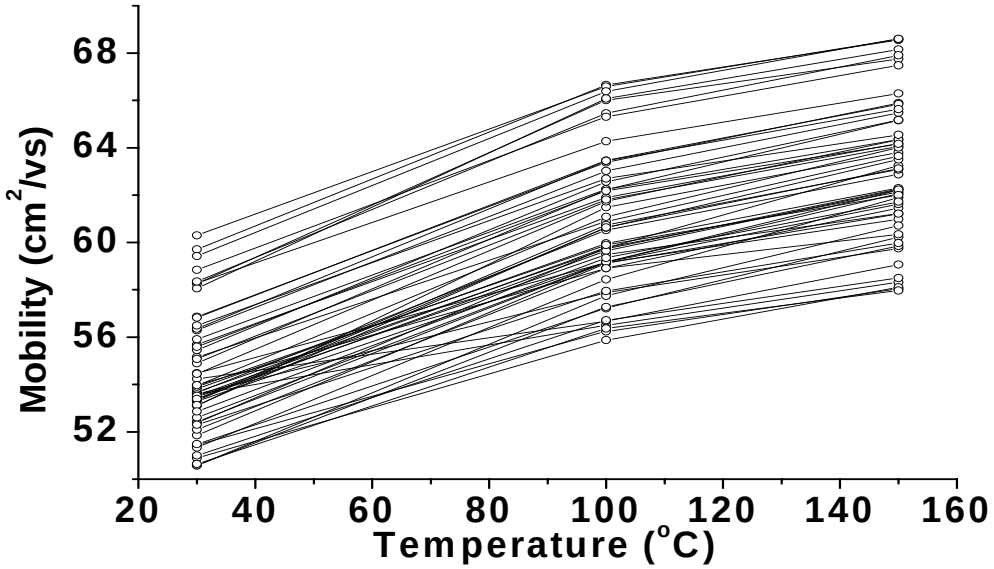

Fig 2-2-2 Many temperature dependences of the effective mobility for n-type TFTs.

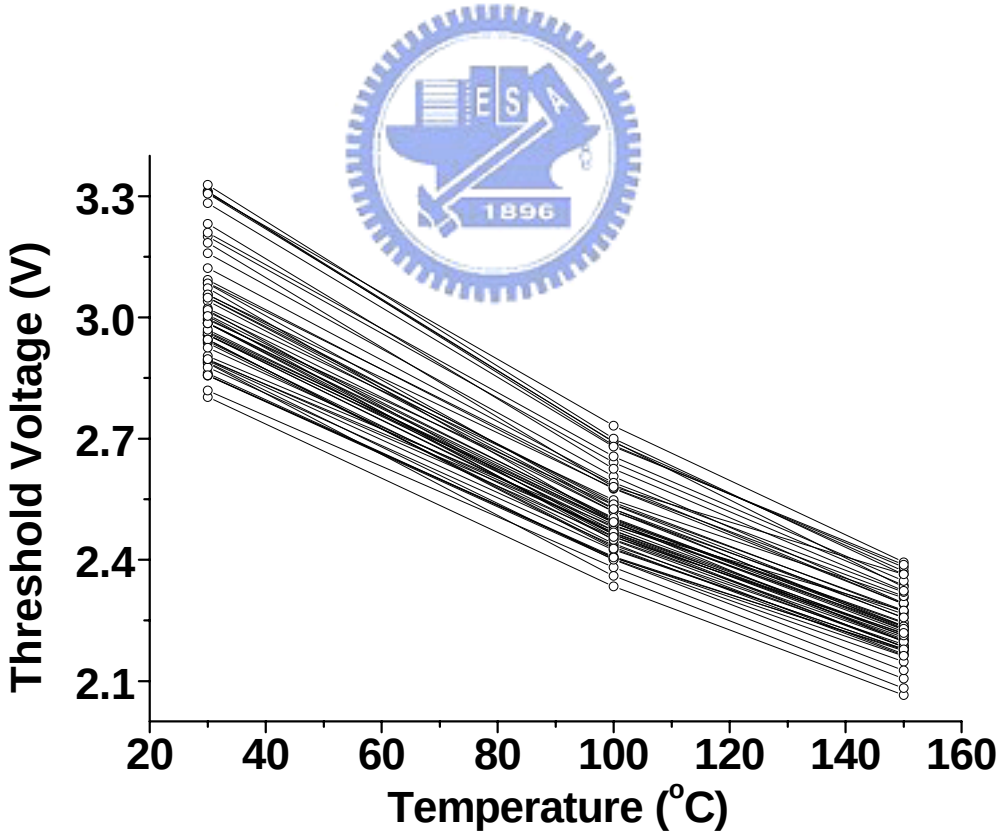

Fig 2-2-3 Many temperature dependences of the threshold voltage for n-type TFTs.

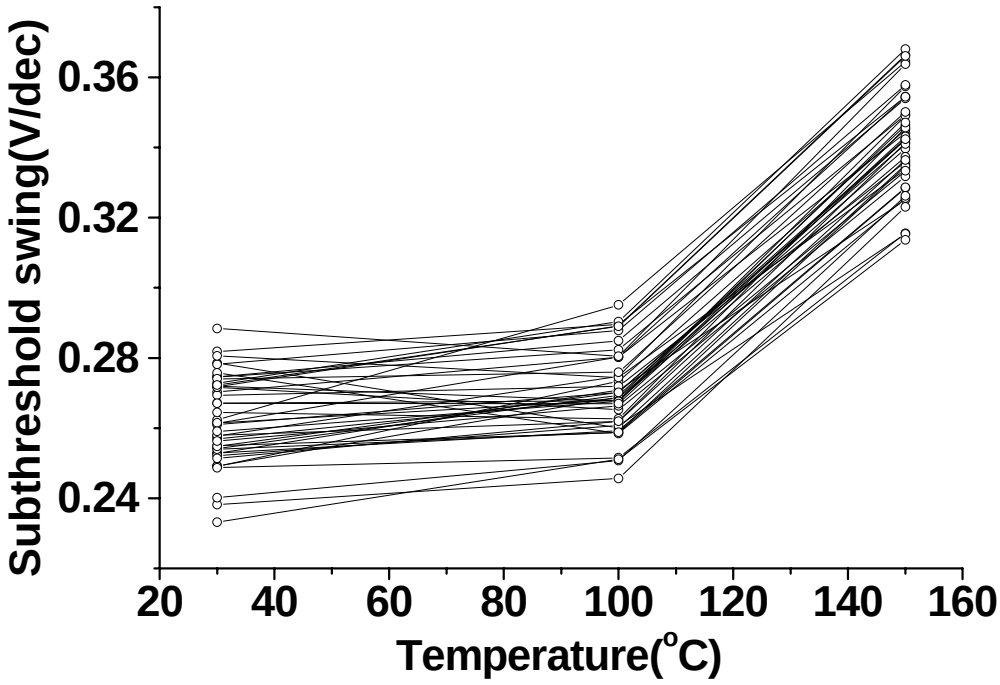

Fig 2-2-4 Many temperature dependences of the S.S for n-type TFTs.

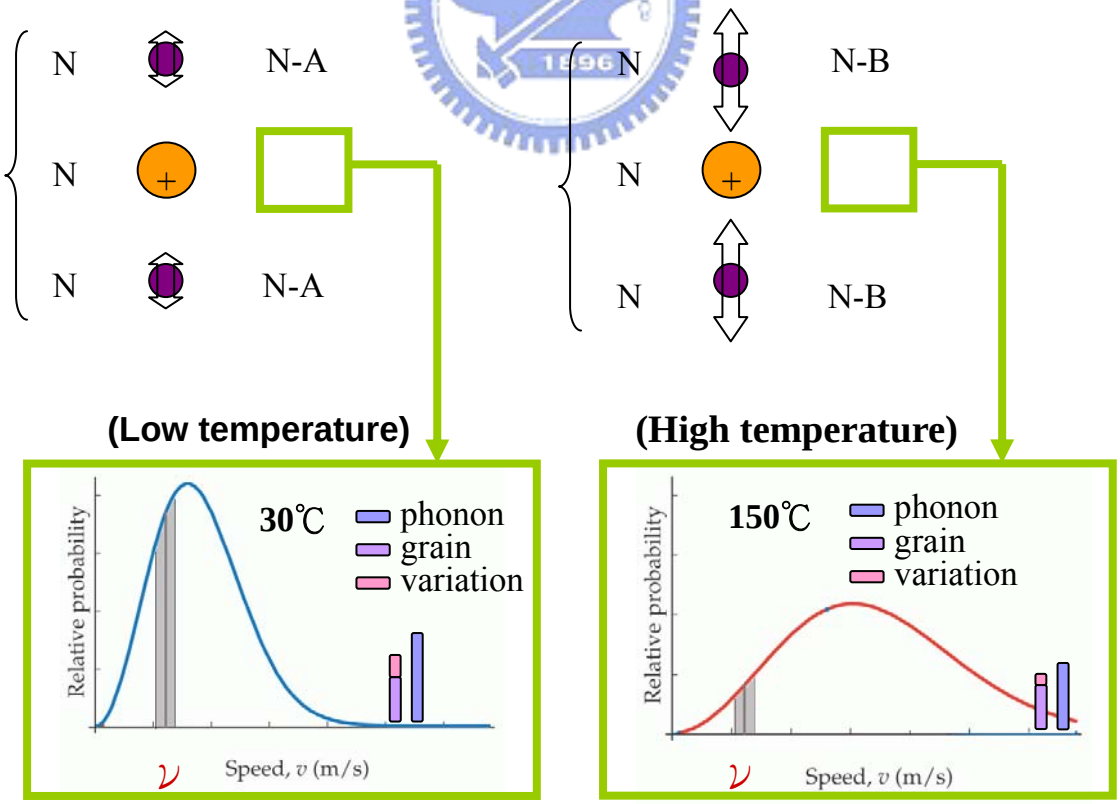

Fig 2-3-5 Temperature dependence for mobility mechanism.

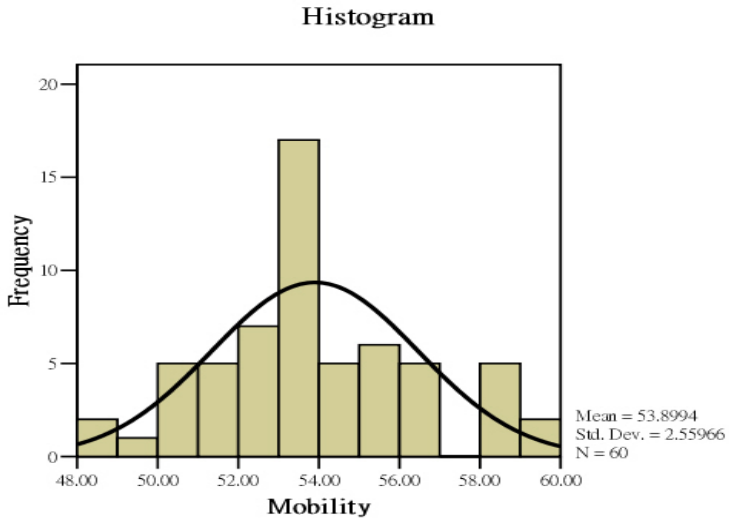

Fig 2-2-5 The histogram of n-type TFTs distribution verse mobility at 30℃.

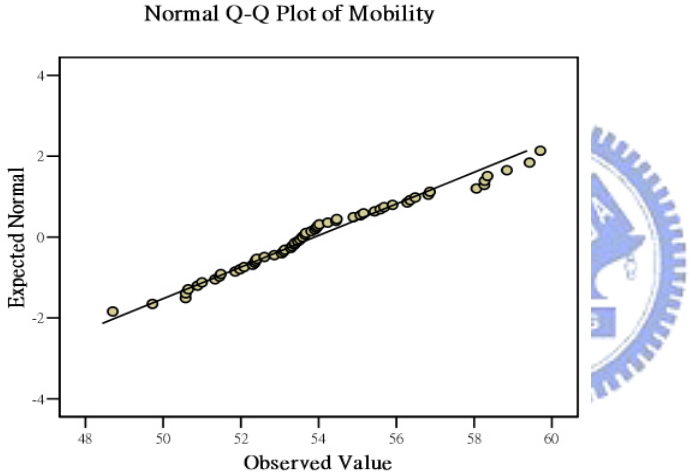

Fig 2-2-6 The Q-Q plot of n-type TFTs mobility at 30℃.

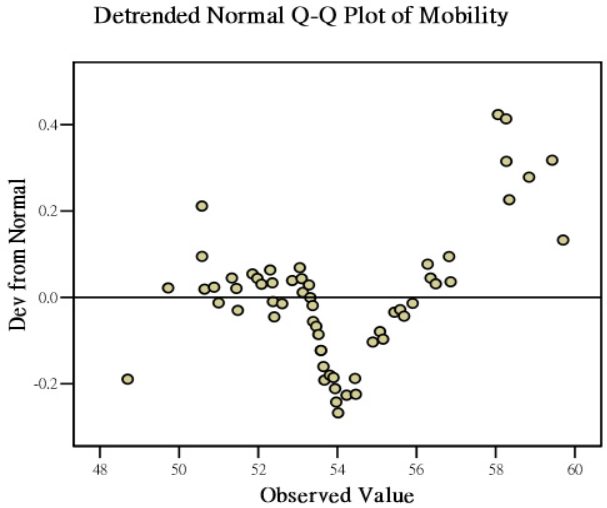

Fig 2-2-7 The detrended Q-Q plot of n-type TFTs mobility at 30℃.

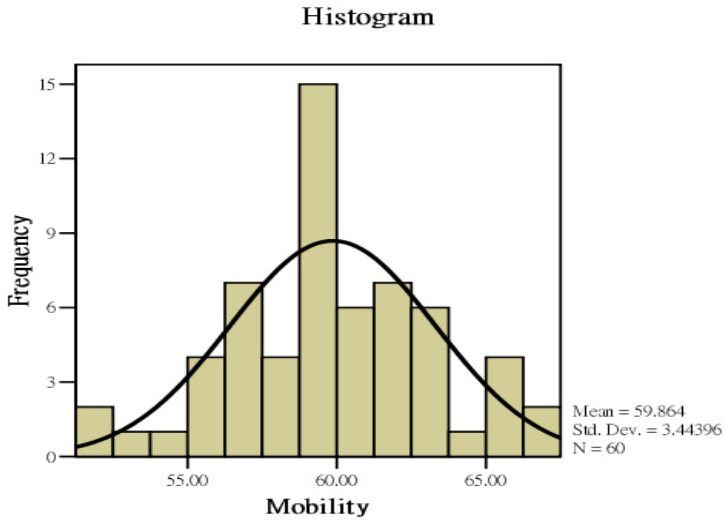

Fig 2-2-8 The histogram of n-type TFTs distribution verse mobility at 100℃.

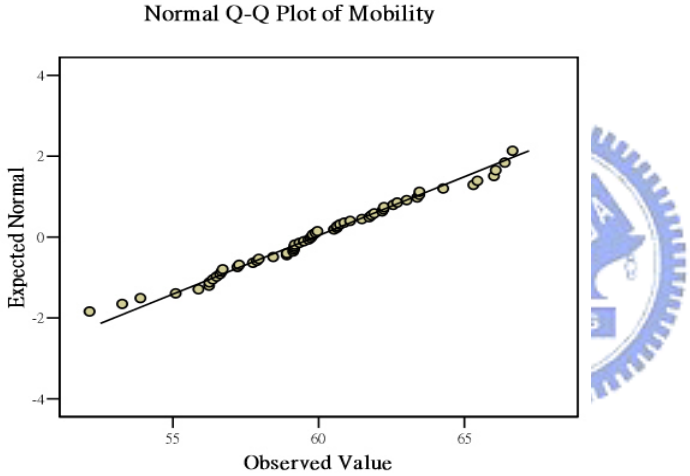

Fig 2-2-9 The Q-Q plot of n-type TFTs mobility at 100℃.

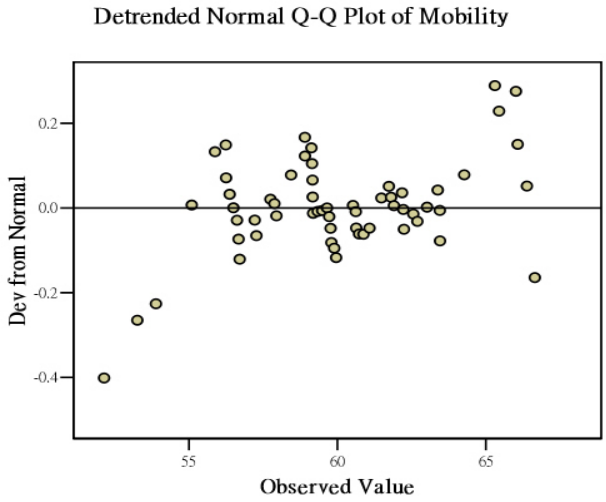

Fig 2-2-10 The detrended Q-Q plot of n-type TFTs mobility at 100℃.

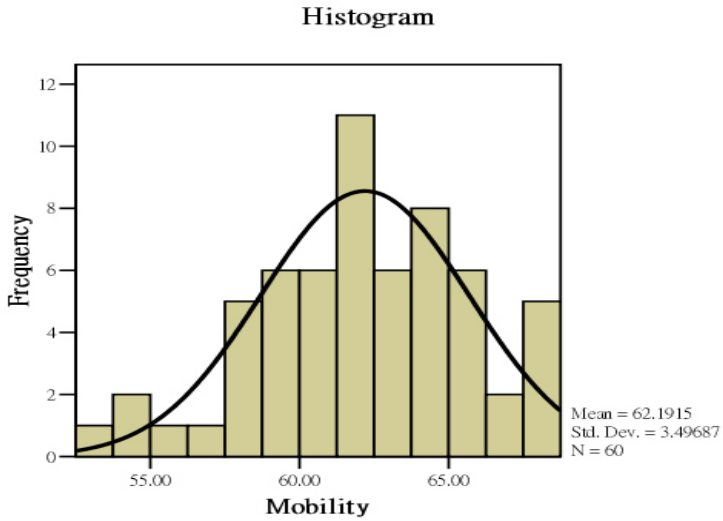

Fig 2-2-11 The histogram of n-type TFTs distribution verse mobility at 150℃.

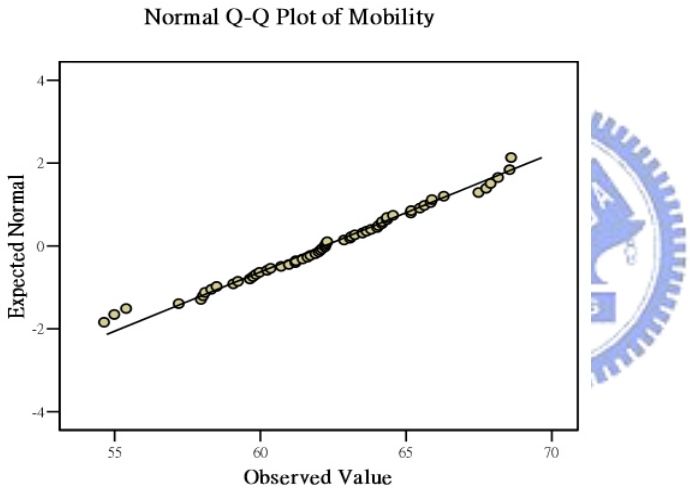

Fig 2-2-12 The Q-Q plot of n-type TFTs mobility at 150℃.

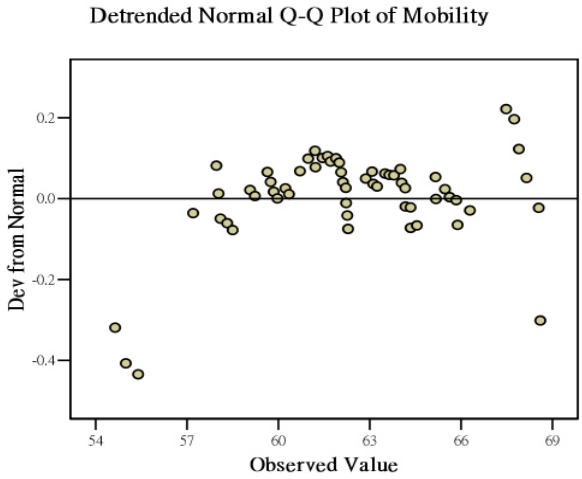

Fig 2-2-13 The detrended Q-Q plot of n-type TFTs mobility at 150℃.

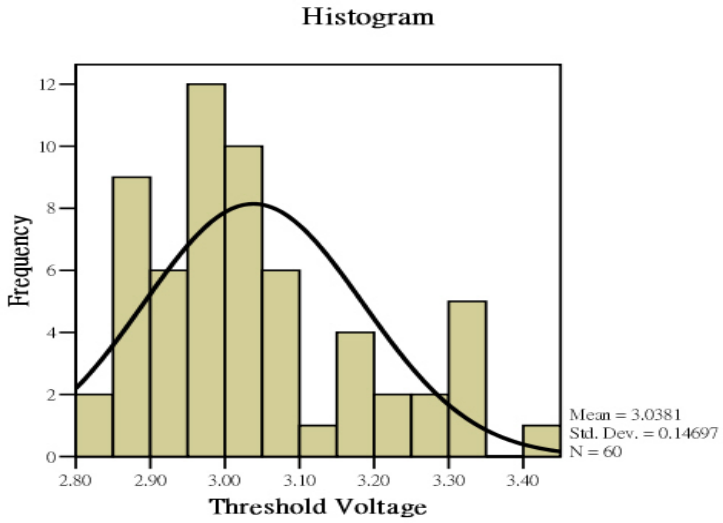

Fig 2-2-14 The histogram of n-type TFTs distribution verse Vth at 30℃.

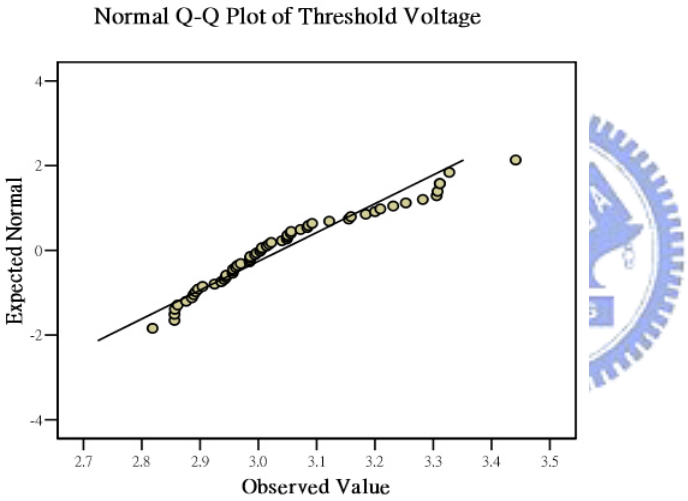

Fig 2-2-15 The Q-Q plot of n-type TFTs Vth at 30℃.

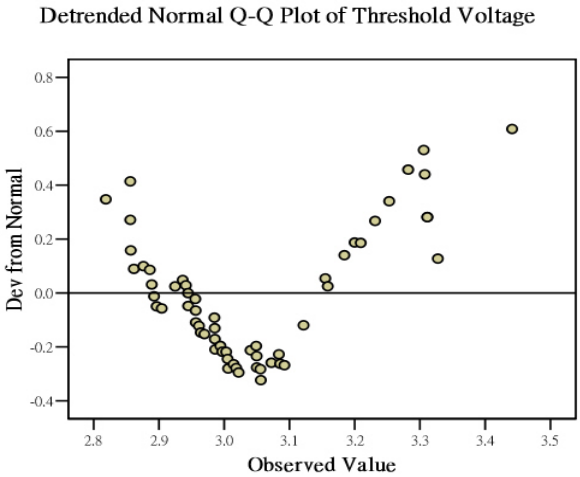

Fig 2-2-16 The detrended Q-Q plot of n-type TFTs Vth at 30℃.

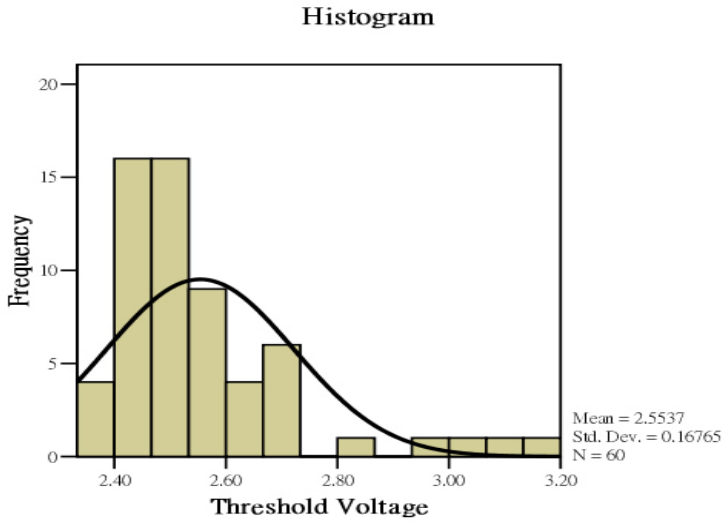

Fig 2-2-17 The histogram of n-type TFTs distribution verse Vth at 100℃.

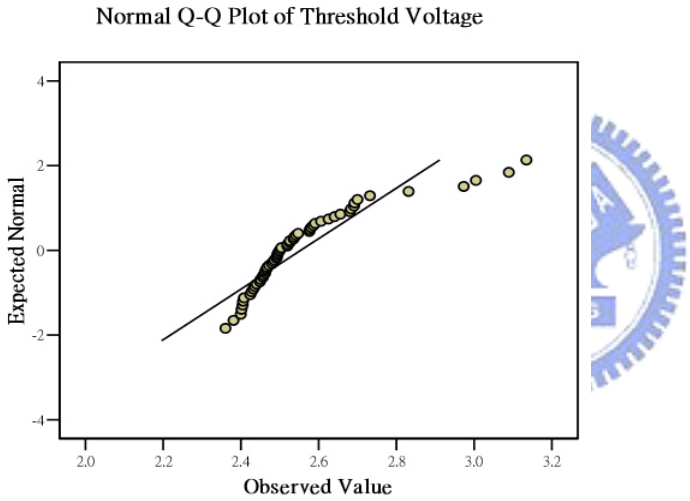

Fig 2-2-18 The Q-Q plot of n-type TFTs Vth at 100℃.

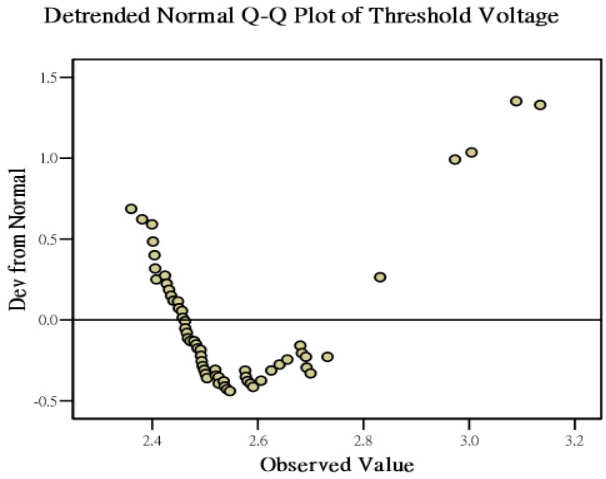

Fig 2-2-19 The detrended Q-Q plot of n-type TFTs Vth at 150℃.

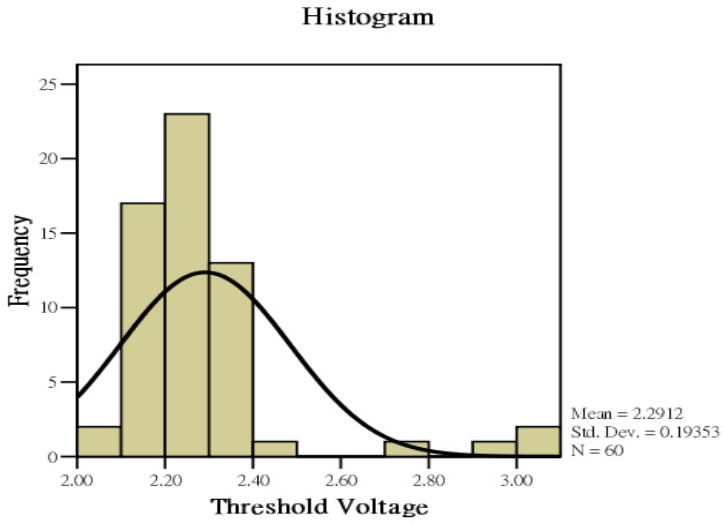

Fig 2-2-20 The histogram of n-type TFTs distribution verse Vth at 150℃.

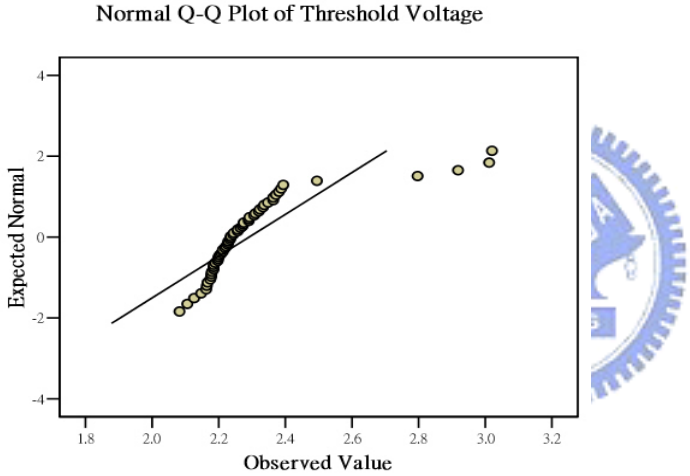

Fig 2-2-21 The Q-Q plot of n-type TFTs Vth at 150℃.

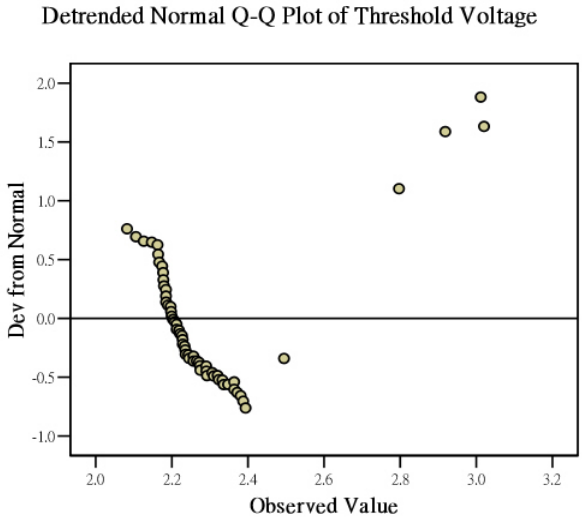

Fig 2-2-22 The detrended Q-Q plot of n-type TFTs Vth at 150℃.

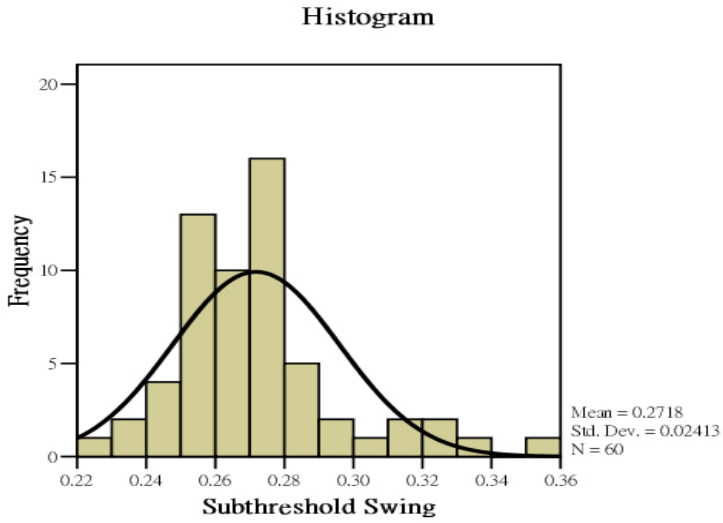

Fig 2-2-23 The histogram of n-type TFTs distribution verse S.S at 30℃.

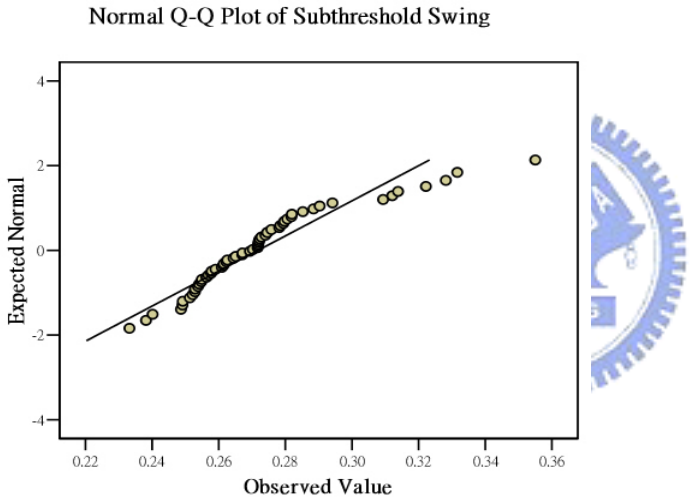

Fig 2-2-24 The Q-Q plot of n-type TFTs S.S at 30℃.

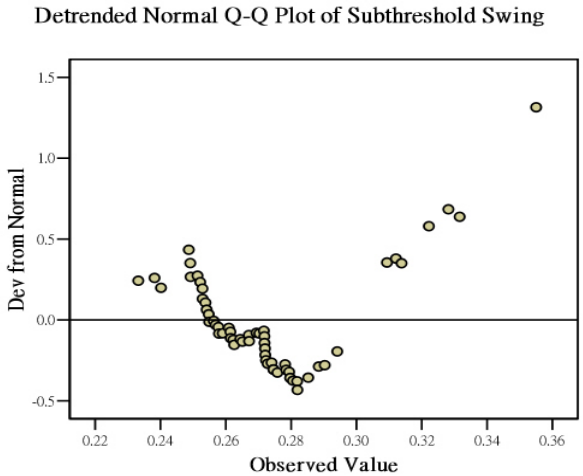

Fig 2-2-25 The detrended Q-Q plot of n-type TFTs S.S at 30℃.

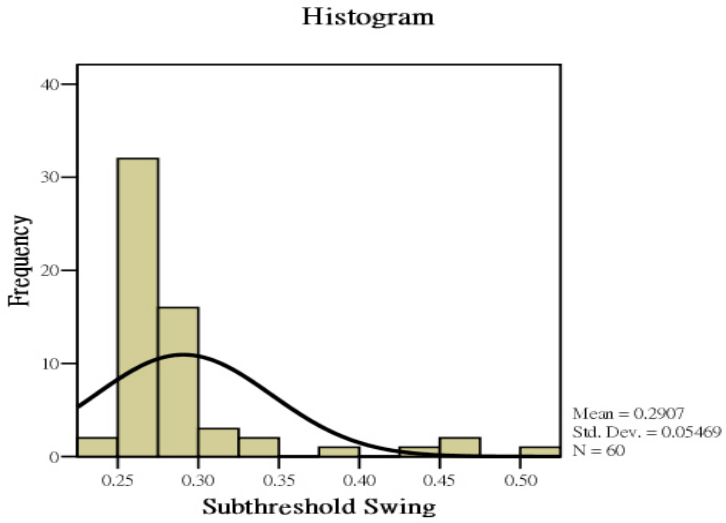

Fig 2-2-26 The histogram of n-type TFTs distribution verse S.S at 100℃.

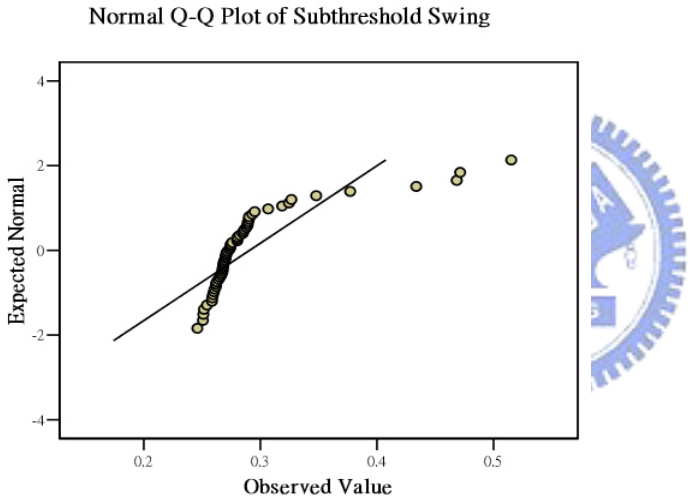

Fig 2-2-27 The Q-Q plot of n-type TFTs S.S at 100℃.

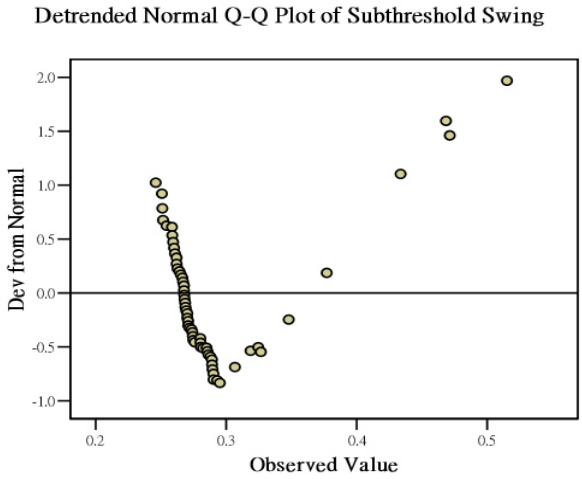

Fig 2-2-28 The detrended Q-Q plot of n-type TFTs S.S at 100℃.

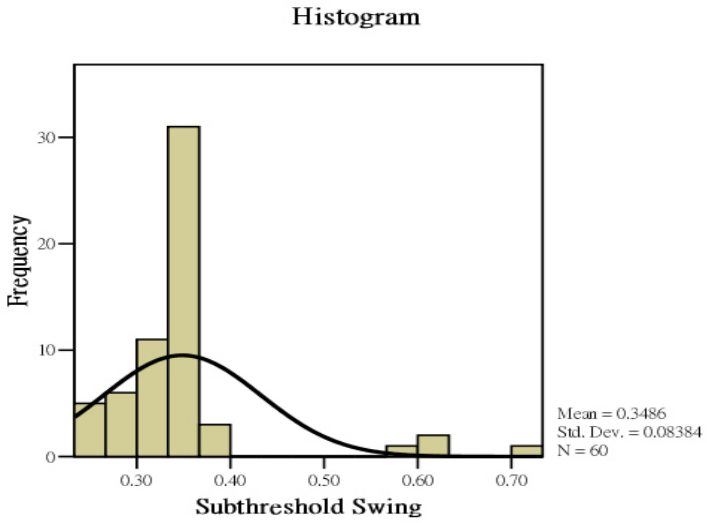

Fig 2-2-29 The histogram of n-type TFTs distribution verse S.S at 150℃.

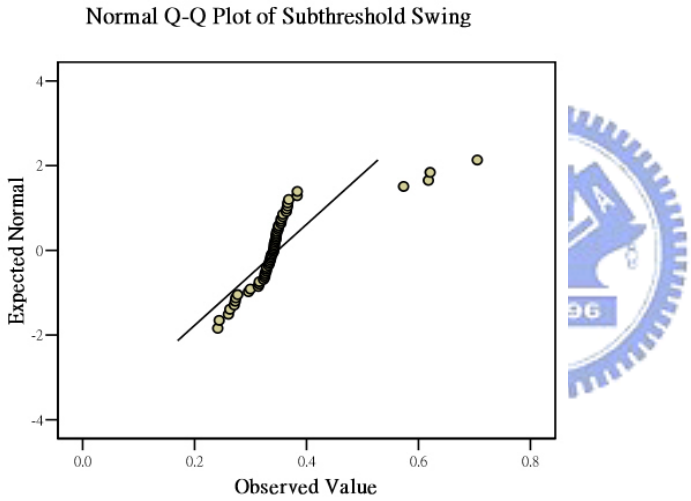

Fig 2-2-30 The Q-Q plot of n-type TFTs S.S at 150℃.

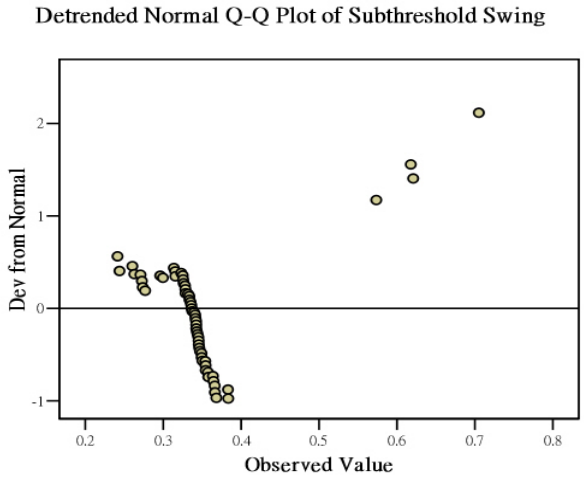

Fig 2-2-31 The detrended Q-Q plot of n-type TFTs S.S at 150℃.

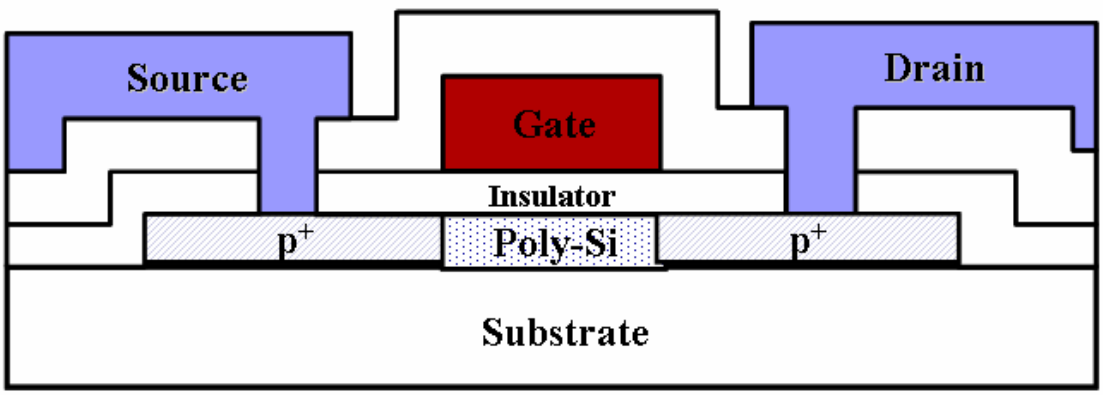

Fig 2-3-1 Schematic cross-section structure of the p-type poly-Si TFT.

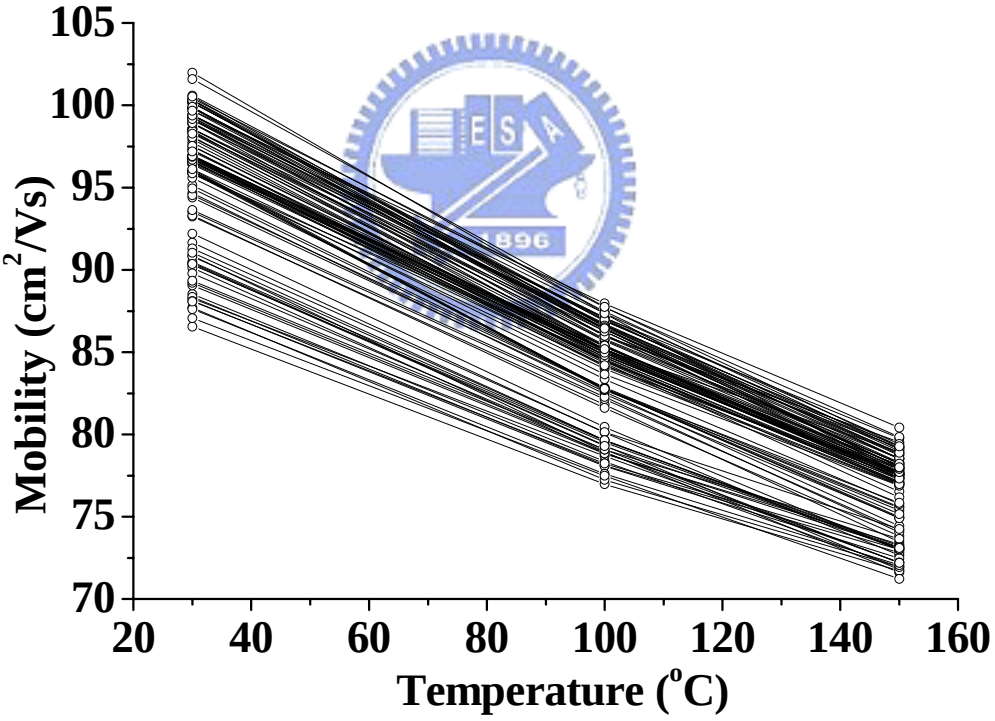

Fig 2-3-2 Many temperature dependences of the effective mobility for p-type TFTs.

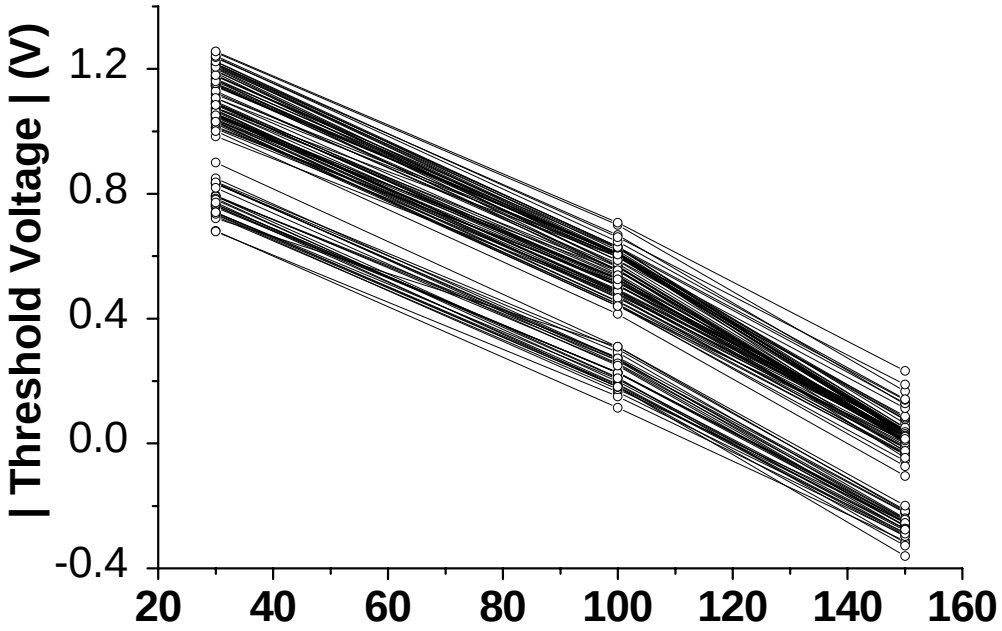

Fig 2-3-3 Many temperature dependences of the threshold voltage for p-type TFTs.

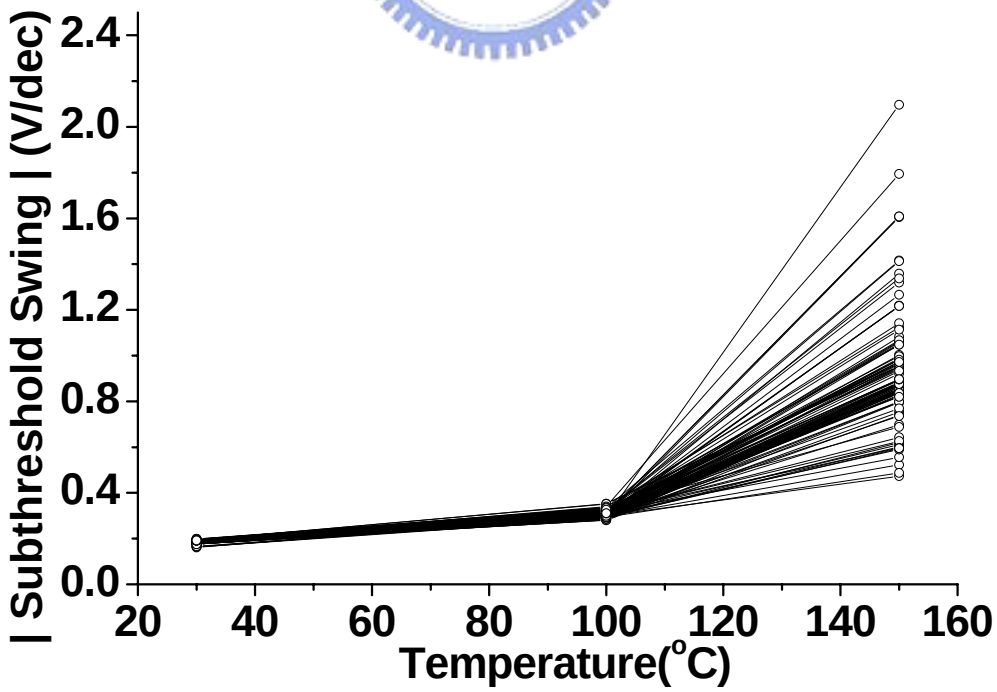

Fig 2-3-4 Many temperature dependences of the S.S for p-type TFTs.

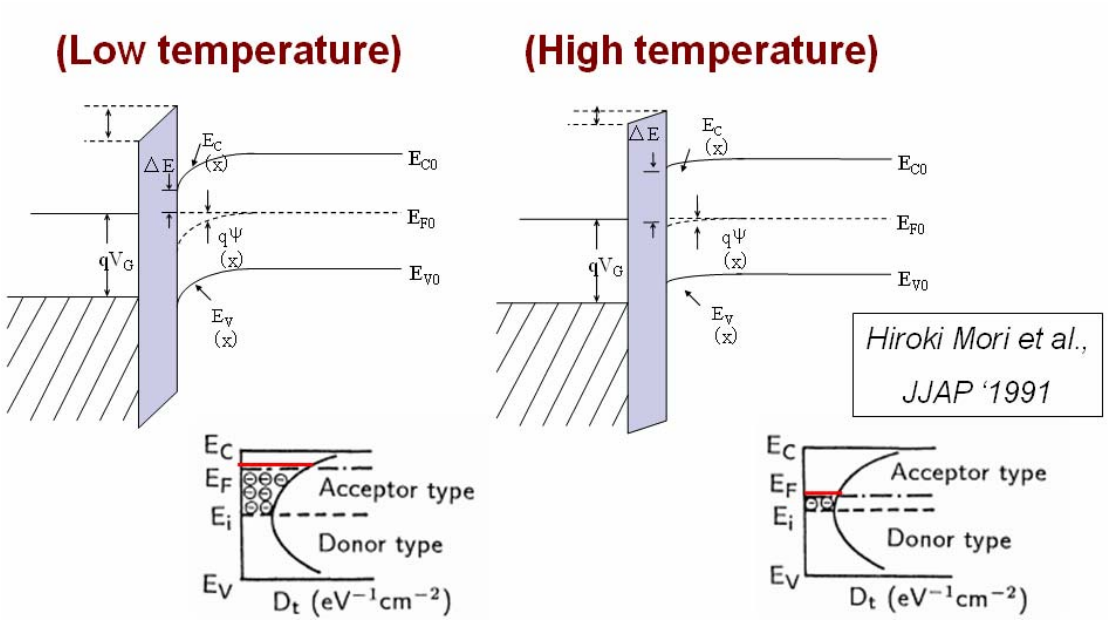

Fig 2-3-6 Temperature dependence for threshold voltage mechanism

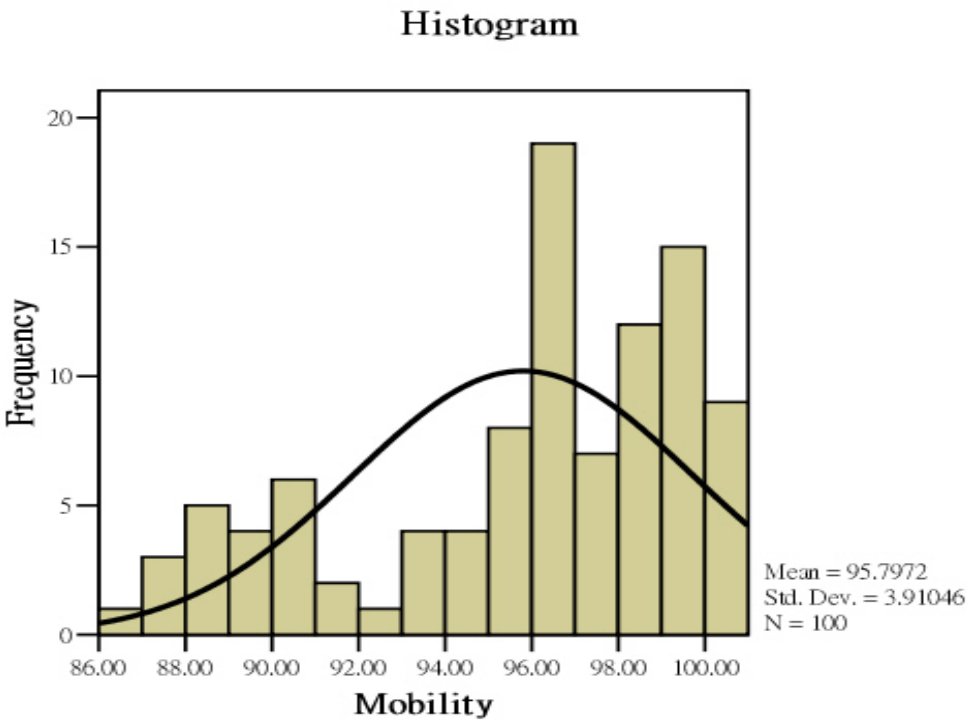

Fig 2-3-7 The histogram of p-type TFTs distribution verse mobility at 30℃.

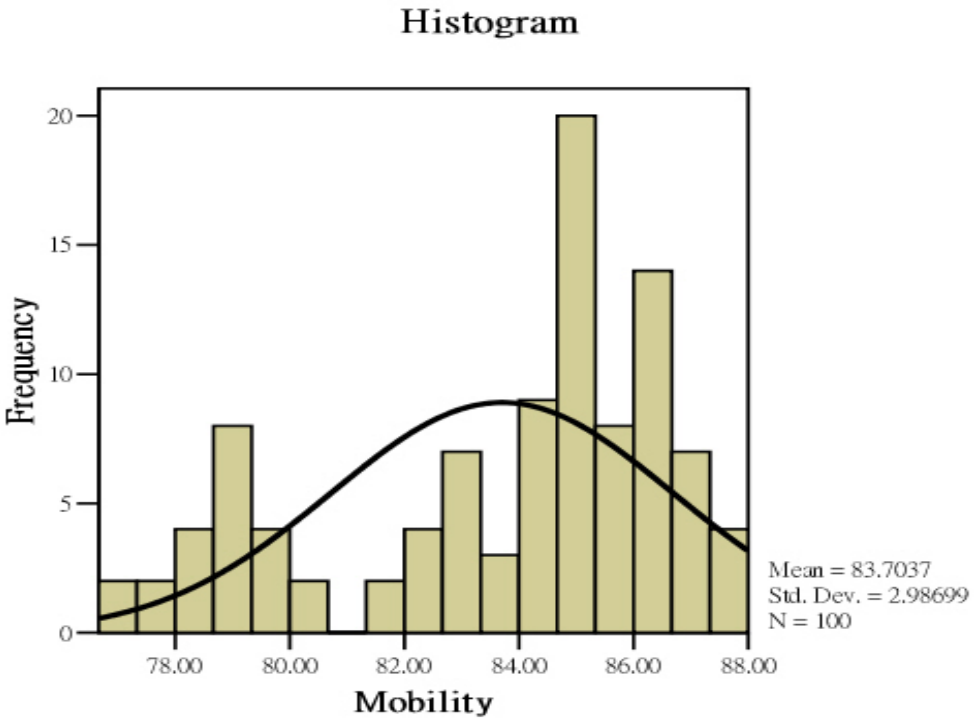

Fig 2-3-8 The histogram of p-type TFTs distribution verse mobility at 100℃.

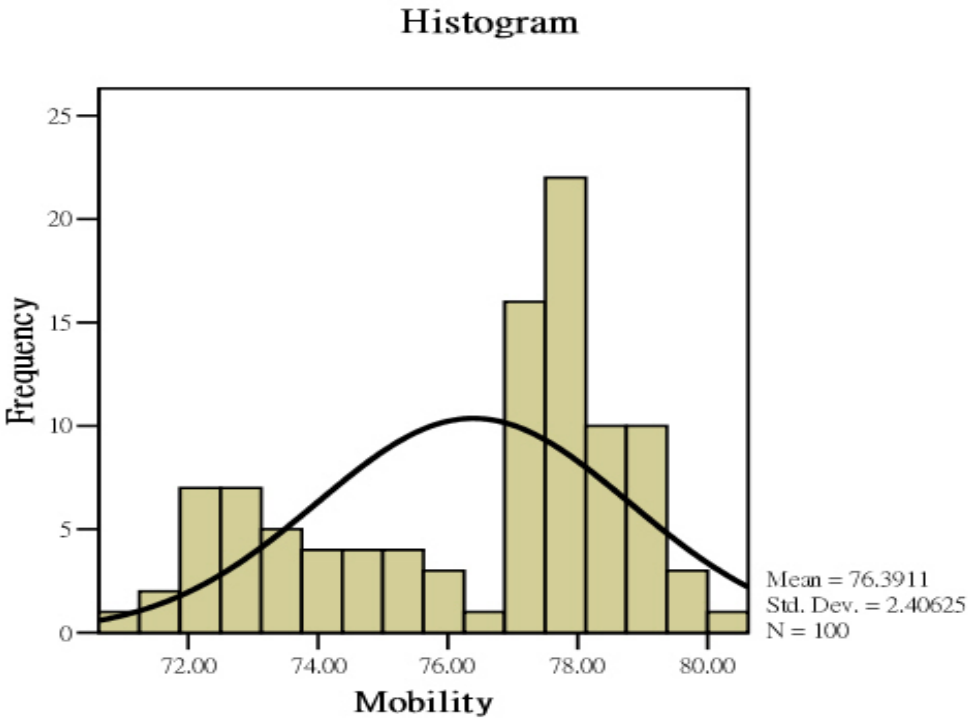

Fig 2-3-9 The histogram of p-type TFTs distribution verse mobility at 150℃.

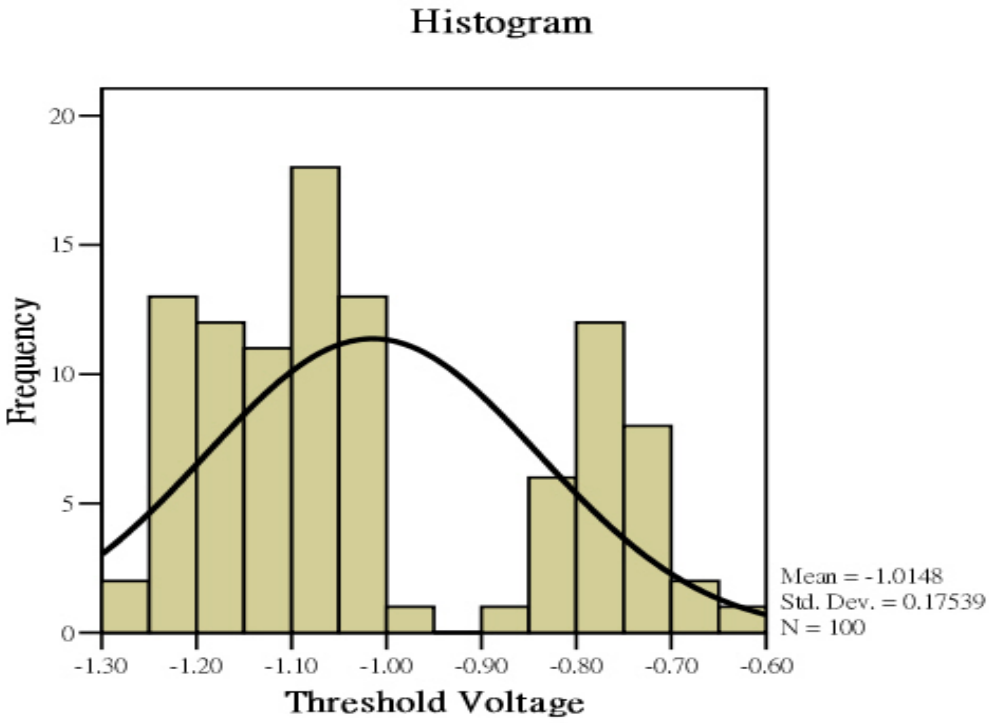

Fig 2-3-10 The histogram of p-type TFTs distribution verse Vth at 30℃.

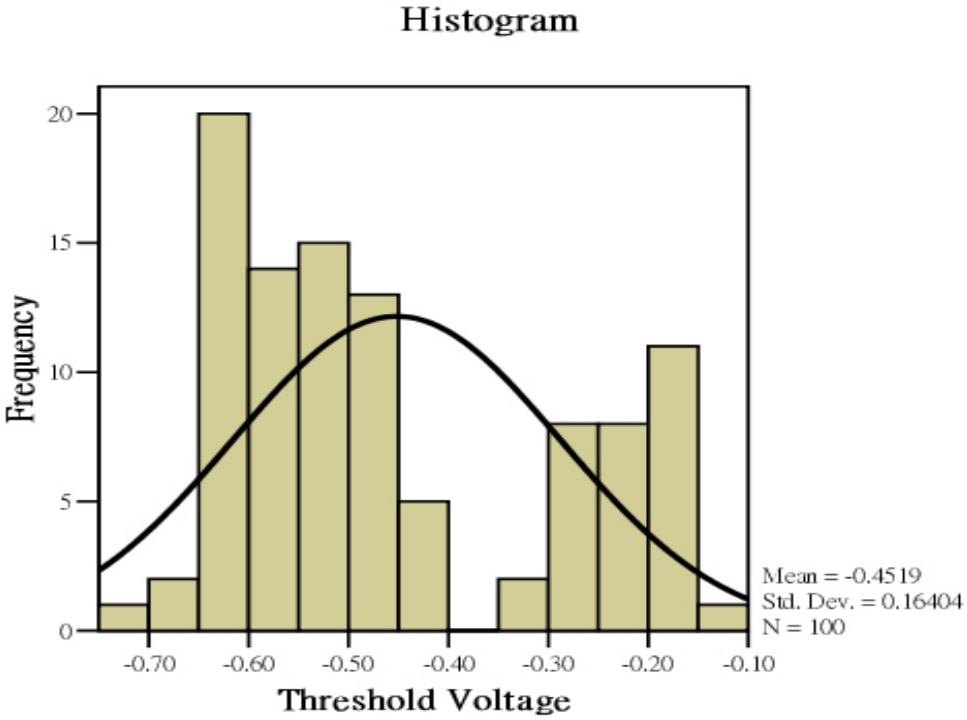

Fig 2-3-11 The histogram of p-type TFTs distribution verse Vth at 100℃.

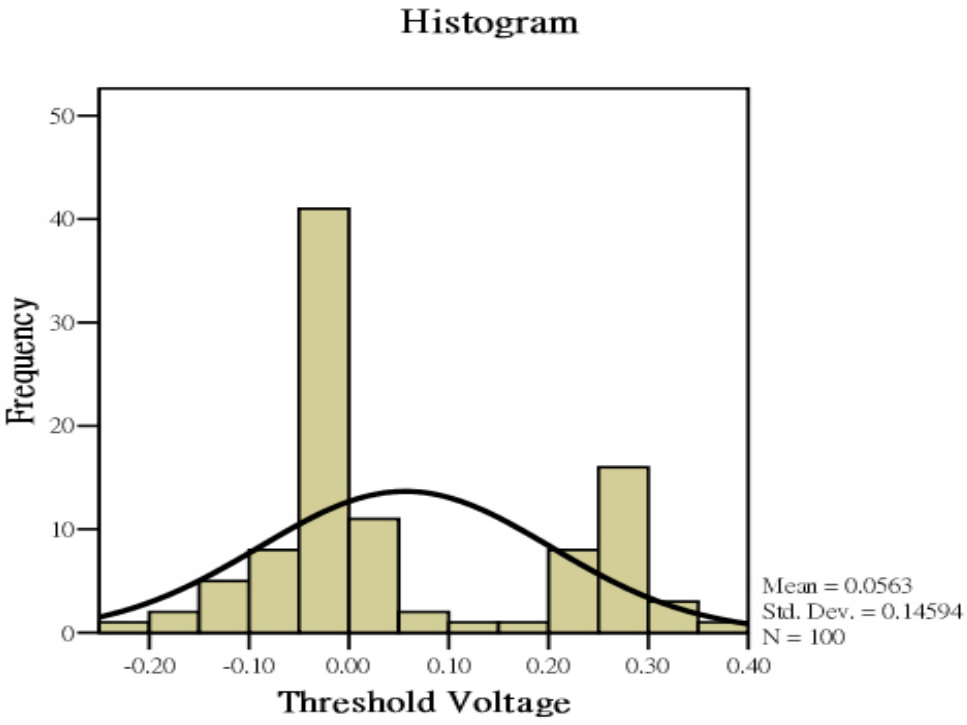

Fig 2-3-12 The histogram of p p-type TFTs distribution verse Vth at 150℃.

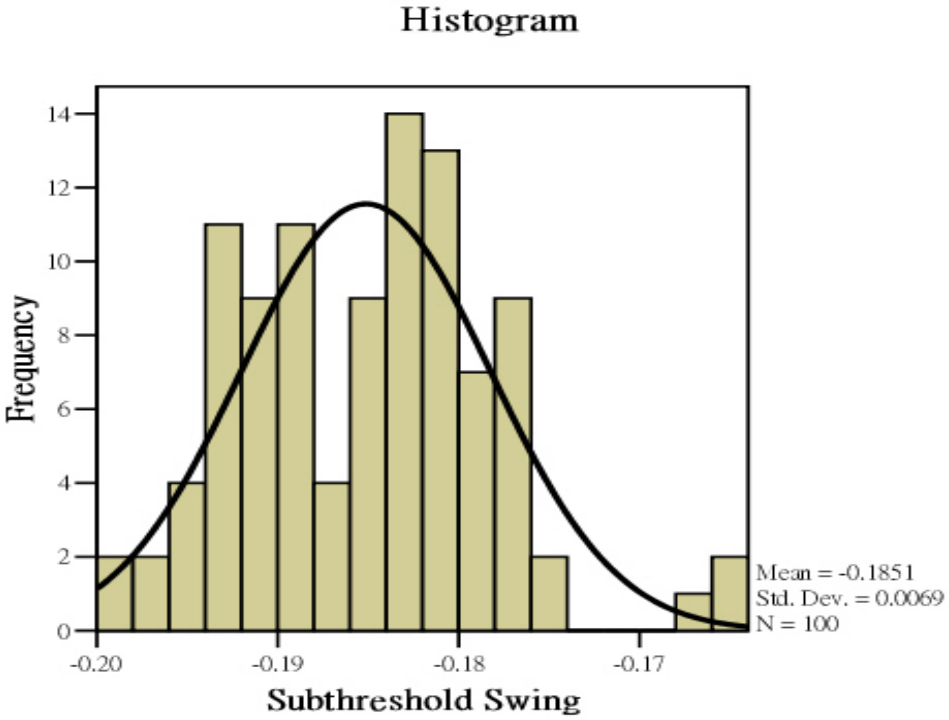

Fig 2-3-13 The histogram of p-type TFTs distribution verse S.S at 30℃.

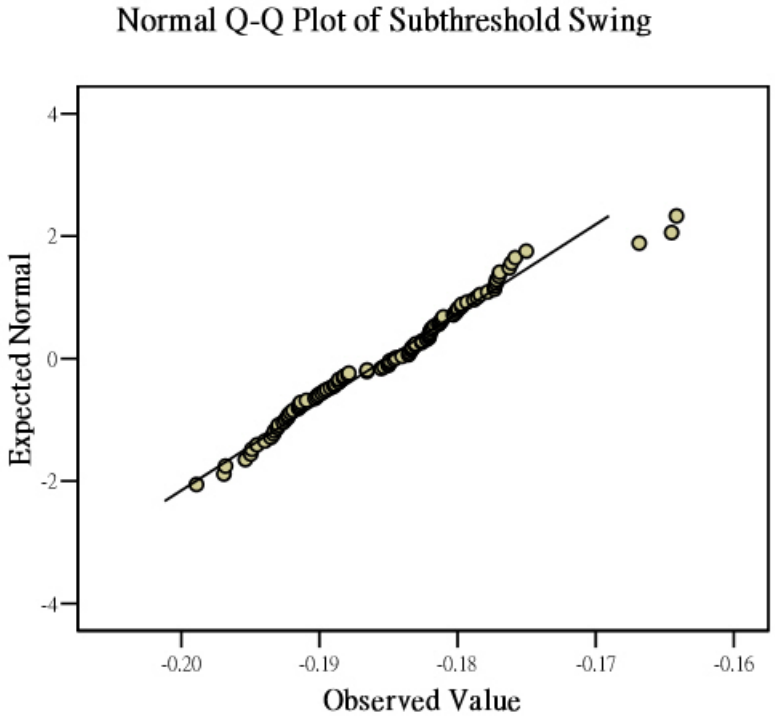

Fig 2-3-14 The Q-Q plot of p-type TFTs S.S at 30℃.

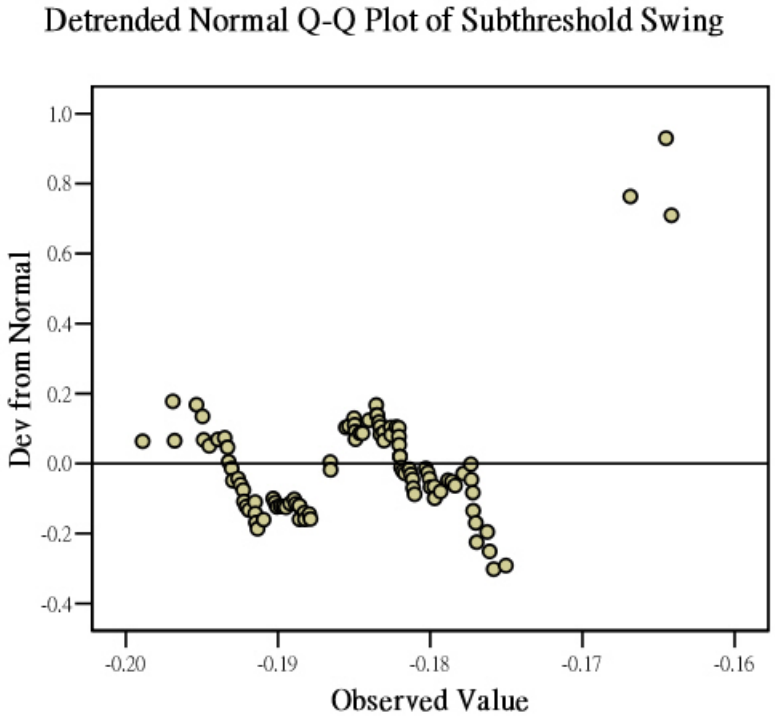

Fig 2-3-15 The detrended Q-Q plot of p-type TFTs S.S at 30℃.

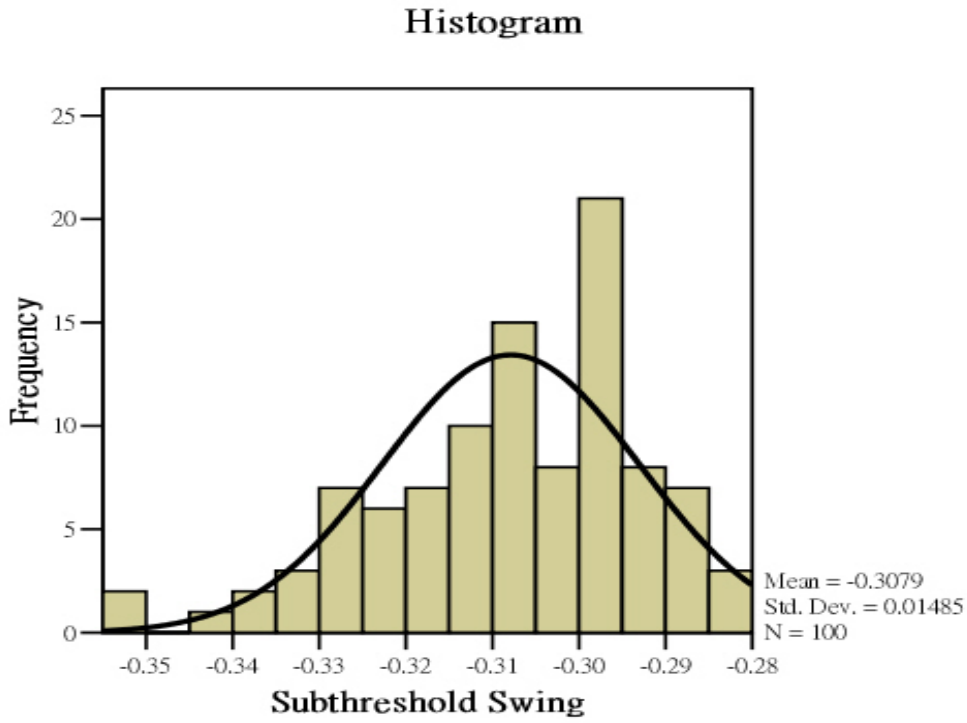

Fig 2-3-16 The histogram of p-type TFTs distribution verse S.S at 100℃.

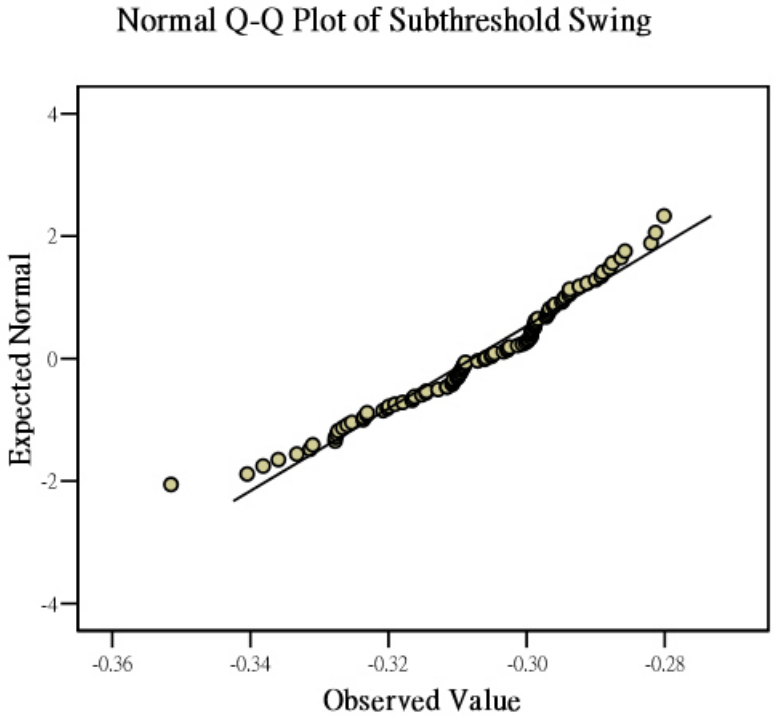

Fig 2-3-17 The Q-Q plot of p-type TFTs S.S at 100℃.

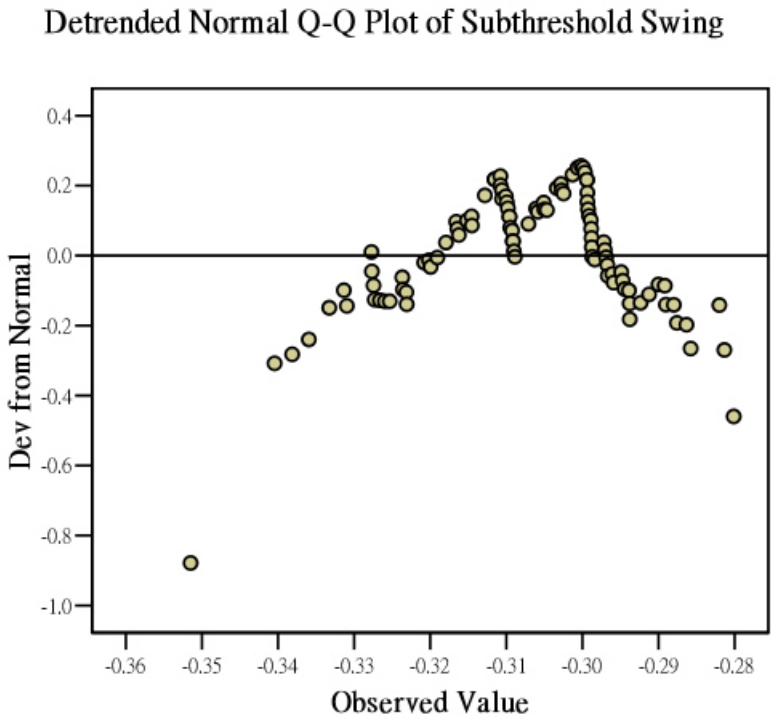

Fig 2-3-18 The detrended Q-Q plot of p-type TFTs S.S at 100℃.

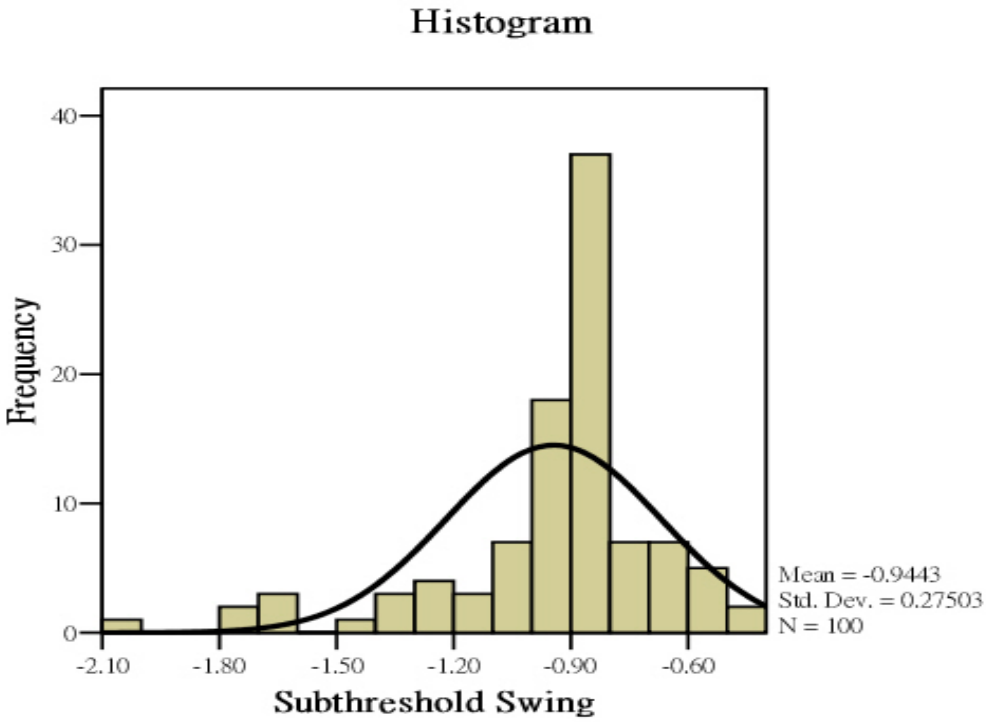

Fig 2-3-19 The histogram of p-type TFTs distribution verse S.S at 150℃.

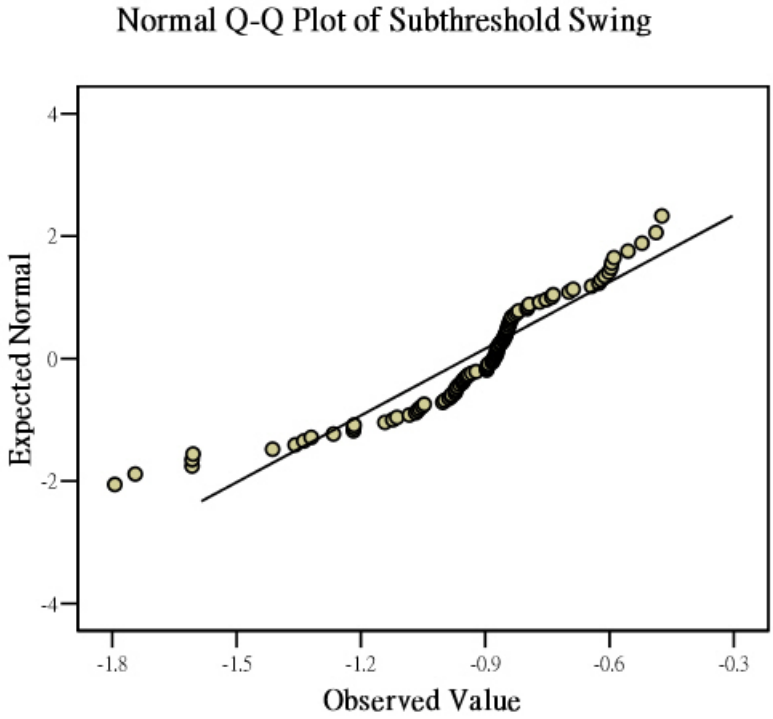

Fig 2-3-20 The Q-Q plot of p-type TFTs S.S at 150℃.

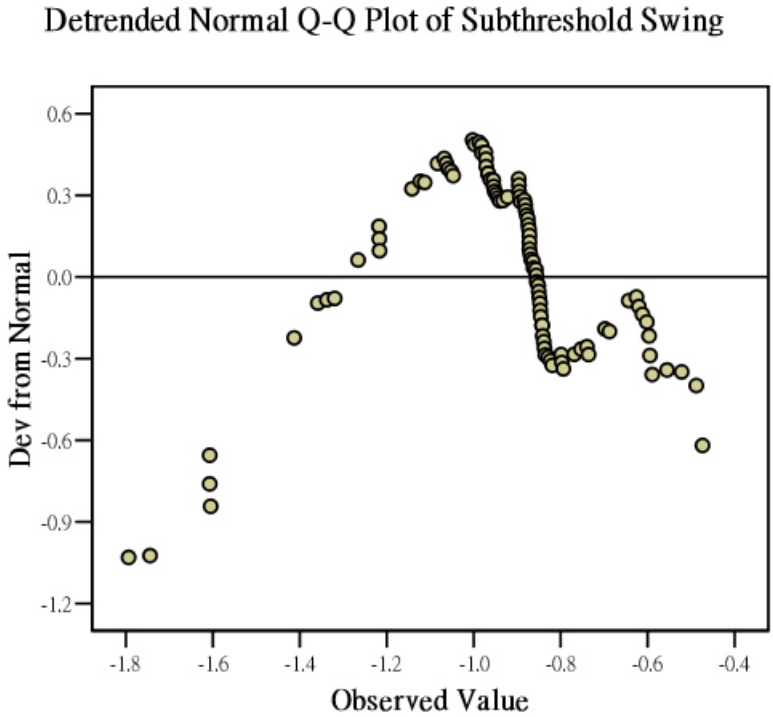

Fig 2-3-21 The detrended Q-Q plot of p-type TFTs S.S at 150℃.

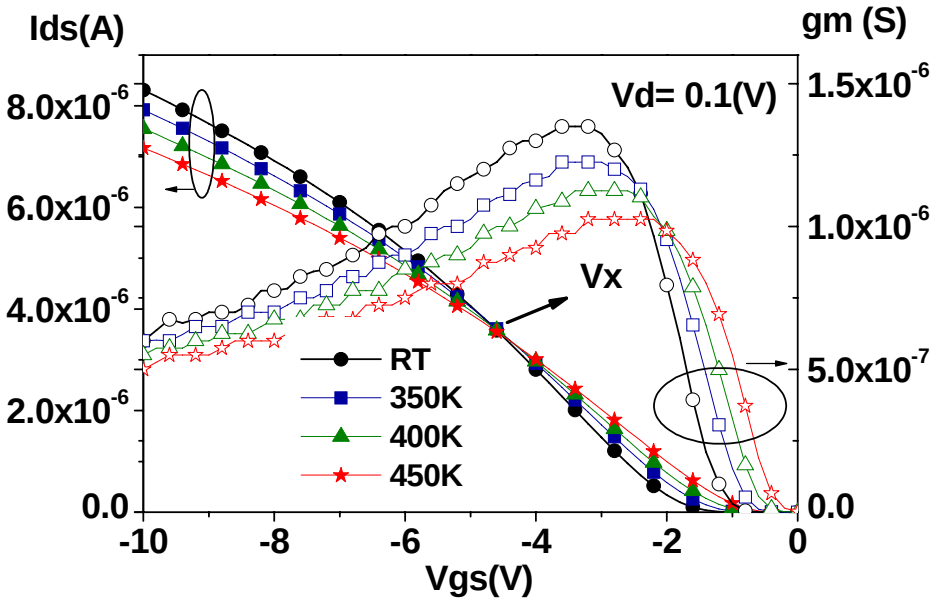

Fig 3-3-1 The gate voltage dependences of drain current and transconductance for a p-type LTPS TFT at different temperatures.

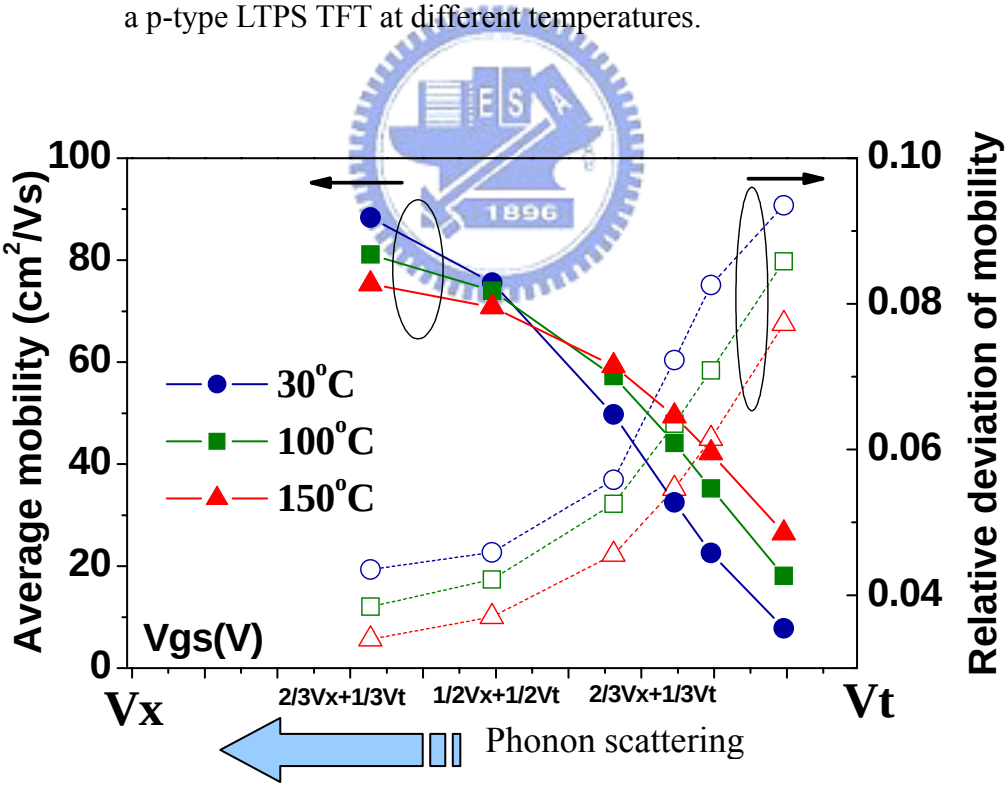

Fig 3-3-2 The average mobility μ_{ave} and the relative mobility deviation σ_{μ}/μ_{ave} in accordance with the relative Vgs in the region between Vx and Vt.

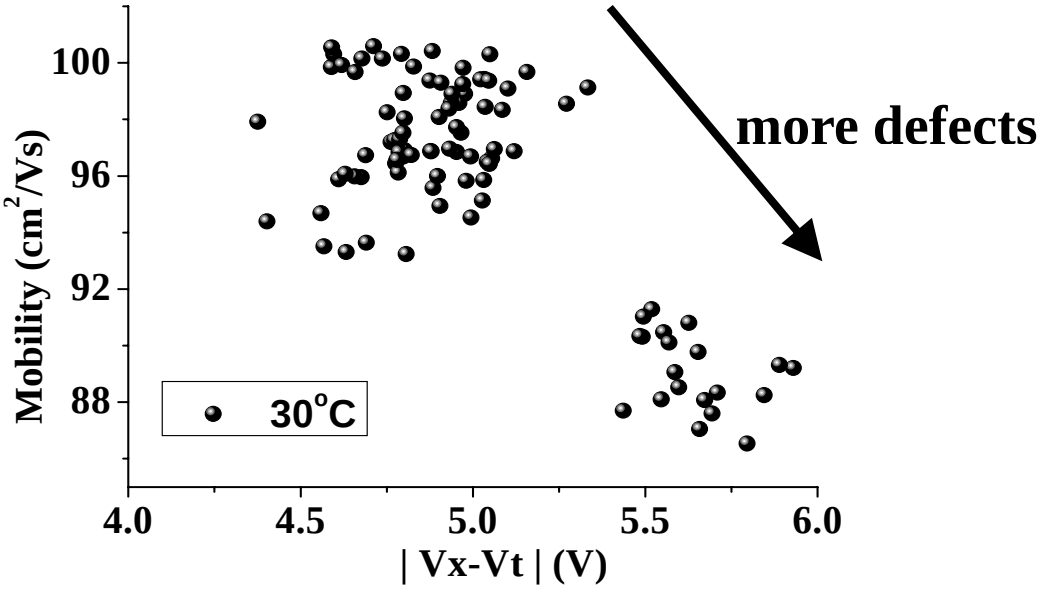

Fig 3-3-3 The comparisons of |Vx-Vt| verse mobility for much p-type poly-Si TFTs at room temperature.

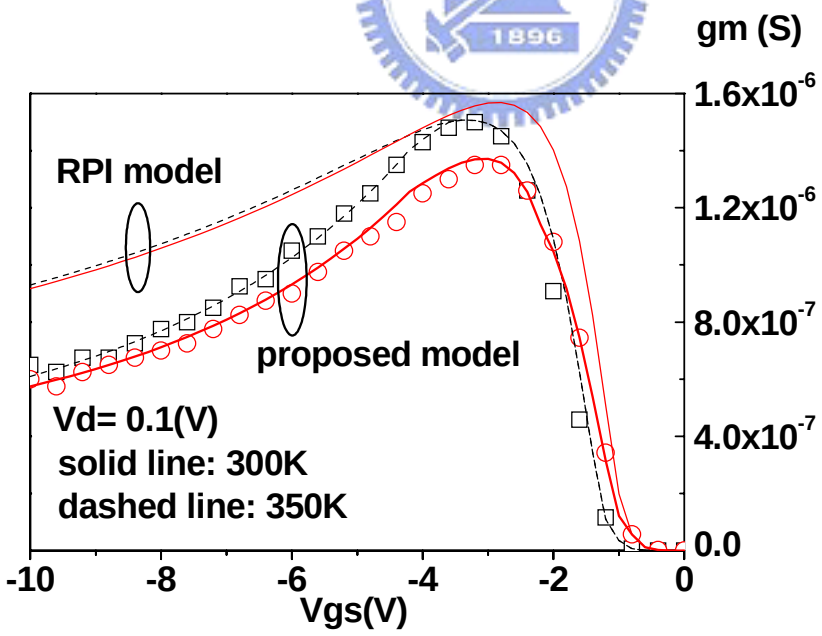

Fig 3-4-1 Comparison of analytically modeled field effect mobility at different t temperature with measured data.