新型閘極覆蓋輕摻雜汲極複晶矽薄膜電晶體之製作與研究

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中文摘要

本論文中，我們成功製作了一個具有閘極覆蓋輕摻雜汲極的複晶矽薄膜電晶體。我們提出了新穎的簡易製作方式，不需要額外的光罩、也不需要任何活性離子非等向性蝕刻技術，同時輕摻雜汲極的長度可以利用控制濕式蝕刻的時間輕易從 100nm 變化到 600nm。比起傳統的閘極覆蓋輕摻雜汲極結構，我們的方法可以避免間隙壁製作過程中的電漿損害、可以製作較長的輕摻雜汲極長度以有效降低元件的漏電，同時是一個低成本的製作流程，可以被簡單的應用。

和對照組的標準元件相比較，我們的結構確實降低了漏電，也有效抑制了元件的短通道效應，這表示我們的結構確實可以有效降低汲極電場。另外我們也發現，我們所提出的結構也可以有效提升導通電流，我們認為這可能是因為元件的閘極覆蓋輕摻雜汲極區域的載子濃度提升、寄生電阻下降，所以和傳統元件相較，可以有效提升導通電流。為了驗證，我們也量測不同通道長度的標準元件和新穎元件的線性區導通電阻，做圖萃取他們的寄生電阻，結果發現確實標準元件的寄生電阻是新穎元件的五倍以上。

最後，我們也比較了新穎元件和標準元件的可靠度，利用典型的熱載子劣化分析，發現確實如預期的，所提出的新穎元件在可靠度測試後的劣化程度較標準元件的輕微很多，這也驗證了所提出的元件確實具有可以實際應用的價值。

The Fabrication and Investigation of A Novel Gate-Overlapped Lightly Doped Drain (GOLDD) Polycrystalline Silicon TFTs

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Abstract

In this thesis, we had demonstrated a novel gate-overlapped lightly doped drain (GOLD) poly-Si TFT. Without any spacer fabrication, additional mask definition or RIE etch back processing, an effective GOLD TFT can be fabricated successfully and easily. The LDD length ranging from 100nm to 600nm can be controlled by simply arranging different wet etching time. Compared to control standard samples, the proposed devices have larger turn-on current, smaller leakage current and better short channel effect immunity such as suppressed threshold voltage roll-off effect. These improved performances prove that the proposed structure had effectively reduced the drain side electric field. The enhanced turn-on current of proposed devices is found to be caused by reduced parasitic resistance. A plausible reason is that the gate-overlapped lightly doped region enhances the carrier density and therefore increases the driving current.

To obviously compare the parasitic resistance effect, we extract the parasitic resistance of standard devices and proposed devices by analyzing the linear region turn-on resistance for devices with various channel length. It is found that the parasitic resistance of standard devices is indeed 5 times larger than that of the proposed GOLD devices.

Finally, we also examine the reliability of the proposed devices. With typical hot carrier stress for 3000 sec. The standard devices exhibit serious degradation such as increased leakage current, larger subthreshold swing and lower turn-on current. The proposed devices, comparing with the standard device under the same stress condition, have much superior immunity for this hot carrier degradation. As a conclusion, the proposed GOLD devices have not only simply fabrication process but also good output performance for channel length ranging from 10 um to 3um.

致謝

發現口試過的那一瞬間，2 年來的辛苦都的到了回報，雖然還有些不踏實，想說這樣就畢業了嗎，還有什麼事我還不夠，還沒學到的地方，或許這些都有待我以後需要繼續努力的地方。

回首求學生涯的這些年，一路上許多人的幫助跟鼓舞，使我的求學路能一直走的很順利。我的父母王同利先生和王林雪華女士，很注意我的學習，從小就陪著我做功課 ，一路陪著我走過來，給予我最大的支持，讓我無論處在任何情況，都有最堅強的後盾、最安全的避風港。感謝我的指導教授，冉曉雯老師這 2 年多的教導，讓我從一片迷霧中看到一道曙光，讓我對 TFT 有了深刻的瞭解。也感謝陳世青學長這 2 年多的照顧，教會我實驗的方法和技巧以及煮咖啡、喝咖啡的藝術。以及交大的顏國錫學長、吳興華學長、士欽、兆仟、凱傑、政偉、士強、贊文、宏光、士哲、承和、彥甫，清大的銘龍、德章，等多位學長同學 2 年來的互相勉勵，彼此支持，不論是實驗上或是生活上的協助。最後是小我一屆的學弟妹，貞儀、章佑、奕德….等學弟妹，這一年多的相處，辛苦你們啦。

Contents

Chinese Abstract I
English Abstract II
致謝 III
Contents V
Table Captions VI
Figure Captions VII
Chapter 1. Introduction 1
1-1. Overview of Polysilicon Thin-Film Transistor Technology 1
1-2. Defects in ploy-Si film 2
1-2-1. The defect-influenced electrical properties 2
1-2-2. The carrier transport in poly-silicon films 3
1-2-3. Leakage current mechanism 4
1-2-4. Kink effect 5
1-3. Motivation 5
1-4. Thesis outline 6
Chapter 2 .Drain Engineering 7
2-1. Multiple gate 7
2-2. Offfset gate 8
2-3. Lightly doped gate (LDD) 9
2-4. Gate-overlapped LDD (GOLDD) 11
Chapter 3. Fabrication and Characterization 13
3-1. Fabrication Process the GOLDD TFTs 13
3-2. Method of Device Parameter Extraction 15
3-2-1. Determination of the threshold voltage 15
3-2-2. Determination of On/Off Current Ratio 16
3-2-3. Determination of the channel resistance and the parasitic resistance 16
3-2-4. Determination of the trap density 17
Chapter 4. Electrical Characteristics of GOLDD TFTs 19
4-1. Typical characteristics comparison 19

4-2. Short channel effect 20
4-3. Reliability 23
Chapter 5. Conclusions 24
References 26
Figures 33
Table 72

Table captions

Table I. Extracted Parasitic Resistance of Standard Devices and Proposed GOLDD Devices with Channel Width = 3um.

Table II. Extracted Parasitic Resistance of Standard Devices and Proposed GOLDD Devices with Channel Width = 10 um.

Table III. Extracted trap density of Proposed GOLDD Devices with Channel Width = 3um.

Figure captions

Chapter 1

Fig. 1-1-1 The electron mobility for a-Si and poly-Si TFT.
Fig. 1-1-2 The aperture ratio for a-Si and poly-Si TFT.
Fig. 1-2-1 All kinds defect well. (a) is the Dirac well. (b) is the repulsive Columbic well. (c) is the Columbic well.
Fig. 1-2-2 Schematic illustration of the leakage current mechanisms. (a) thermionic emission. (TE) (b) thermionic field emission. (TFE) (c) pure field emission. (FE)
Fig. 1-2-3 The devices operate in the saturation.

Chapter 2

Fig. 2-1-1 Cross section of the multiple-gated TFT.
Fig. 2-1-2 I-V transfer characteristics as V_{DS} = 10 V for TFT's with one, two, three, five, and six gates.
Fig. 2-2-1 Cross section of the offset-gate TFT.
Fig. 2-2-2 I_D versus V_G characteristics of a offset structure TFT and conventional TFT (L / W = 50 μm / 10 μm) for various value of V_D.
Fig. 2-2-3 Schematic cross-section of the offset gated poly-Si TFT without as additional offset mask.
Fig. 2-2-4 Schematic cross-section of the self-aligned offset gated poly-Si TFT.
Fig. 2-2-5 The offset lengths of symmetrical device are 1.1 μm and those the asymmetric poly-Si TFT are 1.5 μm and 0.3 μm. Under forward bias the asymmetric poly-Si TFT's offset length at the drain region is 1.5 μm and that at the source region is 0.3 μm.
Fig. 2-3-1 Schematic cross-section of top gate, coplanar poly-Si TFT with lightly doped drain region.
Fig. 2-3-2 The channel area is defined in (a) and is not affected by subsequent processes. The LDD regions are well defined in (b) by the spacers, and are self-aligned to the channel and the source/drain regions.
Fig. 2-4-1 Schematic cross-section of GOLDD TFT.

Chapter 3

Fig. 3-1-1 The top view of the T-gate poly-Si TFTs.

Fig. 3-1-2 Schematic cross sectional view of devices with conventional top-gate structure.

Fig. 3-1-3 The fabrication process (a) deposited to the second TEOS layer. (b) used gate mask to define this TEOS layer. (c) side etch the TEOS. (d) formed the raised structure (e) remove oxide about the source and drain. (f) implant to form the n^+ source and drain regions and n^- regions.

Fig. 3-1-4 In-line SEM picture (a) short LDD length, (b) long LDD length.

Fig. 3-2-1 The I_D-V_D characteristics of the ploy-Si TFTs.

Fig. 3-2-2 An example of ON resistance measurement in the linear regions of the ploy-Si TFT output characteristics.

Fig. 3-2-3 Width -normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data .The channel width of these devices is fixed at 3μm.

Chapter 4

Fig. 4-1-1 I_D versus V_G characteristic of non-LDD TFT and GOLDD TFT.

Fig. 4-1-2 Width -normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data.: (a) conventional TFT, (b) LDD length is 0.158 μm, (c) LDD length is 0.594 μm.

Fig. 4-1-3 The dopant redistribution for (a) conventional TFTs, (b) GOLDD TFTs.

Fig. 4-1-4 The current path for (a) conventional TFTs, (b) GOLDD TFTs.

Fig. 4-1-5 I_G versus V_D characteristic of non-LDD TFT and GOLDD TFT.

Fig. 4-2-1 I_D versus V_D characteristic of conventional TFT and GOLDD TFT.

Fig. 4-2-2 The electron current path.

Fig. 4-2-3 The V_{th}-L characteristics for conventional and GOLDD TFTs : (a) V_D = 0.1 V, (b) V_D =5 V.

Fig. 4-2-4 The charge share characteristics for (a) conventional TFTs, (b) GOLDD TFTs.
Fig. 4-2-5 The ΔV_{th}-L^{-1} characteristics for conventional TFTs.
Fig. 4-2-6 The I_D-V_G characteristics for different LDD length in the GOLDD TFTs.
Fig. 4-2-7 Plotting of ln〔I_D / (V_G - V_{FB})V_D〕versus (V_G - V_{FB})$^{-2}$.
Fig. 4-2-8 The I_D-V_G characteristics for different LDD length in the GOLDD TFTs.
Fig. 4-2-9 The energy band for channel and LDD region at V_D = 0.1 V and V_G = -10 V.
Fig. 4-2-10 The average I_D-V_G characteristics for different LDD length in the GOLDD TFTs.
Fig. 4-2-11 The average I_D-V_G characteristics for different LDD length in the GOLDD TFTs.
Fig. 4-3-1 The typical characteristics for conventional TFTs : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-2 The typical characteristics for conventional TFTs stressed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-3 The typical characteristics for conventional TFTs stressed and reversed Drain/Source contact : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-4 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-5 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm and stressed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-6 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm, stressed and Drain/source reversed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-7 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-8 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm and streed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.
Fig. 4-3-9 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm, streed and Drain/source reversed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.