Chapter 1

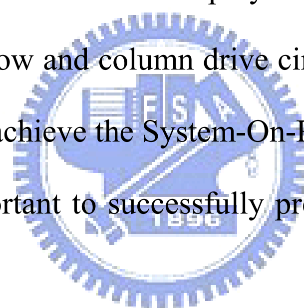
Introduction

1-1. Overview of Polysilicon Thin-Film Transistor Technology

In 1966, the first polycrystalline silicon thin-film transistors (poly-Si TFT's) were fabricated by Fa et al.[1.1]. Since then, many research reports have been proposed to study their conduction mechanisms, fabrication processes and device structures to improve the performance. Today, poly-Si TFTs have received much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs)[1.2], and active matrix organic light-emitting displays (AM-OLEDs) [1.3]. Except large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs) [1.4], static random access memories (SRAMs)[1.5], electrical programming read only memories (EPROM) [1.6], electrical erasable programming read only memories (EEPROMs) [1.7], linear image sensors[1.8], thermal printer heads[1.9], photo-detector amplifier[1.10], scanner[1.11], neutral networks[1.11]. Lately, some superior performances of poly-Si TFTs also have been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality[1.12][1.13]. This provides the opportunity of using poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary trend, leading to rapid developing of poly-Si TFT technology.

Over the past twenty years, the most interesting application of poly-Si TFTs is AMLCDs, although the present first generation of AMLCDs relies predominantly upon hydrogenated amorphous silicon (a-Si:H) TFTs for the pixel switching devices.

A-Si:H film exhibits high OFF-state resistivity which can reduce the leakage current of TFTs. Unfortunately, the extremely low field-effect mobility (typically around 1 $cm^2/V.sec$) in a-Si:H TFTs limits the technology from being developed to form integrated drive circuits on the active matrix plate. On the contrary, there are many advantages for using poly-Si TFTs to replace a-Si:H TFTs, such as the superior carrier mobility in Fig. 1-1-1, CMOS capability, lower photocurrent, and better device reliability[1.14], [1.15]. Higher field-effect mobility implies higher driving current. The higher drive current allows small-geometry TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio in Fig. 1-1-2 and lower parasitic gate-line capacitance for improved display performance. Therefore, the superior field-effect mobility achievable with poly-Si TFTs is seen to be essential for the successful integration of row and column drive circuits on the active panel [1.16]. At the same time, in order to achieve the System-On-Panel (SOP) and computer-aided circuit design, it is very important to successfully predict the electrical properties of poly-Si TFTs.



1-2. Defects in Poly-Si Film

However, some problems still exist in applying poly-Si TFTs on large-area displays. The poly-Si material is a heterogeneous material made of varies small crystals of silicon atoms in contact with each other constituting a solid phase material. These crystals are called crystallites. The borders of these crystallites are called grain boundaries[1.17]. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects. These grain boundaries act as energy barriers that the carriers have to overcome so that the conduction is strongly affects by the grain boundaries.

1-2-1. The defect-influenced electrical properties

Usually, we consider defects as accepter-like defects and donor-like defects. The formers are neutral when empty and are negative-charged when occupied by electrons; and the latter are positive-charged when empty and are neutral when occupied by holes. Therefore when electrons or holes meet the defects, the defects will present different properties. Giving the acceptor -like defect as an example. When an electron faces a "neutral" acceptor-like defect, there is no interaction between the defect and electron, the defect is similar as a Dirac well, as Fig. 1-2-1 (a) shows. However an electron faces a "negative" acceptor-like defect, there is a repulsive Columbic force which exists between the defect and electron, as Fig. 1-2-1 (b) shows. This type of well can't capture more carrier than Dirac well, because the repulsive Columbic force. Relatively, when a hole faces a "neutral" acceptor-like defect, the defect is similar the Dirac well, and the Columbic well for the "negative" acceptor-like defect as. Fig. 1-2-1 (c) shows. Then this type of well - Columbic well - can capture more carrier than the Dirac well and the repulsive Columbic well. For the same reason, an electron faces the "neutral" donor-like defect, the defect will form a Dirac well, and the Columbic well for the "positive" donor-like defect. When a hole faces the "neutral" donor-like defect, the defect will form a Dirac well, and the repulsive Columbic well for the "positive" donor-like defect.

1-2-2. The carrier transport in the poly-silicon films

The grain boundary regions are full of disordered crystallite structures and the dangling bonds. They will affect device characteristics seriously because they act as trapping centers to trap carriers. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, the typical characteristics such as threshold voltage (V_{TH}), subthreshold swing (S.S.), ON current,

mobility and transconductance of TFTs are inferior to those of devices fabricated on single crystal silicon film. It is also found that poly-Si TFTs exhibit large leakage current. The leakage current increases with increasing the drain voltage and the off-state gate voltage. Dominant mechanism of the leakage current had been proposed to be the field emission via grain boundary traps due to the high electric field near the drain junction [1.18]. To overcome this inherent disadvantage of poly-Si film with grain boundary defects, many researches have focused on modifying or eliminating these grain boundary traps. Traps are associated with dangling bonds arising from lattice discontinuities between different oriented grains or at the Si/SiO_2 interface. One of the useful methods to remove traps is to passivate these dangling bonds with hydrogen atoms or nitrogen atoms[1.19][1.20]. As the number of trapped carrier decreases, the potential barriers in grain boundaries will be decreased and the leakage current is also reduced

1-2-3. Leakage current mechanisms

In the channel region near the drain junction, the reveres bias may induce a high electric field that mainly occurs at grain boundaries. Three main mechanisms are observed in the reverse mode[1.17] [1.18] Fig. 1-2-2

(a) thermionic emission (TE) [1.21]

(b) thermionic field emission (TFE) [1.22]

(c) pure field emission (FE)

When Poly-Si TFT's operate in the OFF region, a depletion region will exist near the drain side. Carriers can generate from the depletion region via the traps which are in the grain boundary.

(a) It is linked to the density of defects in the forbidden band in the crystallite as well as in the disturbed zone of the grain boundary, which act as traps for carriers

following the Schockley-Read-Hall model[1.23]. Carriers can generates and recombination via the traps in the grain boundary due to the thermal excited trapped carriers. (b) The mechanism is relative to the electrical field effect on the thermal emission of trap in the semiconductor junctions. This effect can separate from two parts. One is the thermionic effect and another is tunneling effect. As an electron recombine with phonons, electron could jump to a virtual state from a defect level. The electron in the virtual state might tunnel from the state to the conduction band under the aid of the electrical field. (c) If there is a large enough electrical field in the depletion region that carrier could tunneling via trap in the grain boundary, it is trap to band tunneling.

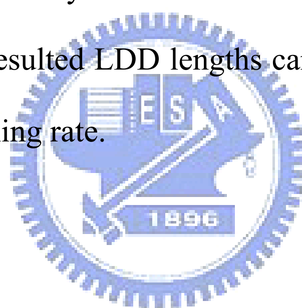
1-2-4. Kink effect

When devices are operated in the saturation, impact ionization will take place in the high-field region near the drain to generate electron-hole pairs from the Fig. 1-2-3. Electrons are collect at drain electrode and holes are injected into the film. Then the holes flow toward the source and finally lower the source junction potential. The added drain current is called kink effect. The kink effect is enhanced by the action of a parasitic bipolar transistor due to the floating body effect which is similar to SOI devices[1.24] [1.25]. As kink effect increases in the digital circuits, the power dissipation increases and the switching characteristics is degraded. In analogue circuit applications, it reduces the maximum attainable gain as well as the common mode rejection ratio[1.26].

1-3. Motivation

To reduce the drain side electric field that cause serious leakage current and the kink effect, the lightly-doped drain (LDD) structures had been widely adopted to solve these problems. When using the LDD structure to suppress the drain electric

field, the parasitic resistance in these lightly-doped areas can also lower the turn-on current. As a result, gate-overlapped LDD (GOLDD) structure had been proposed to maintain high ON current in the turn-on region and exhibit reduced drain electric field and lower leakage current in the turn-off region [1.27]. However, most GOLDD structures are very complicated fabrication that need either large-angle tilt implantation or poly-Si spacer process. Most seriously, the LDD length in the proposed methods are usually less than 300nm due to the process limit, this is not long enough to suppress the leakage current for poly-Si TFTs. In this thesis, we proposed a very simple way to fabricate GOLDD TFTs. Only by adding a capping oxide layer above the gate layer and using wet etching to define the LDD length, the GOLDD devices can be successfully fabricated. Nor additional mask neither RIE etch back process is needed. The resulted LDD lengths can be varied from 100 nm to 600 nm by controlling the wet etching rate.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1-4. Thesis Outline

In chapter 1, we introduce the thin film transistors technologies and several undesirable effects in the electric characteristics, including large off-current, kink-effect due to defects in the grain boundaries.

In chapter 2., we make a brief introduction for different structures which proposed to reduce lateral high field near the drain region

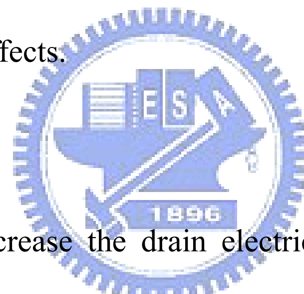
In chapter 3 and 4, we describe the detail of fabrication process and parameter extraction that we use. We would also show our experiment results. The typical characteristics comparison for conventional and GOLDD TFTs and short channel effect are proposed. The reliability issues will be also discussed by hot carrier stress. The related results will be shown in chapter 4.

Finally, the conclusion will be given in chapter 5.

Chapter 2

Drain Engineering

Electrical characteristics of the poly-Si TFTs have specific concerns: high leakage current, kink effects and hot carrier effects. The leakage current mechanism is explained to be field emission via grain boundary traps in the depletion region. Kink effect is the saturation current increase due to generation of electron-hole pairs induced by the high electric field at the channel/drain contact region. Then, traps can enhance the phenomenon. The traps can be decreased by hydrogenation. But, the hydrogenation method does not completely remove the traps. On the other hand, decrease in the electric field in the drain depletion region is very effective in suppressing the undesirable effects.



2-1. Multiple Gate

The first approach to decrease the drain electric field was the introduction of multiple gates in the TFTs[2.1][2.2][2.3][2.4][2.5], as show in Fig. 2-1-1. By dividing the channel into several heavily doped regions connected in series, the voltage and field between the source and drain will simply be divided, thereby the drain field each TFT becomes moderate. The leakage current can be suppressed and on-current also is reduced in Fig. 2-1-2. This is because linear partition of the total potential gives an experimental decrease in the leakage current, which exponentially increases with the drain field and minority carriers generated in the drain high field region would recombine the (or one of the) heavily doped channel region(s) without reaching the source. A drawback of the multiple gates is that the channel width must be increased in order to compensate by the limit on the minimum feature size. This increases the TFT’s area, and thus, decreases the aperture ratio of the LCDs. The trade-off between

the leakage current and TFT area often results in selecting of the gate number of two.

2-2. Offset Gate

A offset structure TFT is proposed in which n^- regions are introduced between the channel and the n^+ source-drain electrodes in order to decrease the electric field in the drain depletion region as shown in Fig. 2-2-1[2.6]. The structure has low leakage current but also has low on-current due to the high parasitic resistance in Fig. 2-2-2. The on-current , off-current and on/off current ratio decreased as offset length increases. This device has three major drawbacks, One is the increased process complexity. Other is the large parasitic resistance which reduces driving ability and the other is the variation in the channel length due to the difficulty in precise control of the offset length.

A TFT without an additional offset mask was proposed in 1995[2.7]. The structure is show in Fig. 2-2-3. The silicon islands except a channel region are formed with an action mask. Another upload a-Si (the upper a-Si layer) are deposited. Then a gate oxide layer and poly-Si layer are deposited. The five layers (gate poly-Si, gate oxide, upper poly-Si, buffer oxide and lower poly-Si) are formed. The upload regions near the source and drain are isolated from the gate electrode by a buffer oxide layer and acts as an offset gated region. The length of the offset region is established to the extent that the gate electrode is overlapped with the poly-Si action layer. The structure has two advantages. One is that the fabrication process saves a mask to define the offset region. Another advantage over the conventional devices is that the over-etch problems of a contact hole may be solved because the source/drain region (the lower poly-Si) can be made thick maintaining the very thin channel layer (the upper poly-Si) and a very thin film TFT may be fabricated easily. But the devices still have problems. The fabrication process is more complicated and ON current is lower than

conventional TFT.

The offset length can be controlled by photo-resist reflow[2.8]. The structure uses a sub-gate to extend the offset range of conventionally used offset length. Photoresist form on the top of the gate can be reflowed to extend beyond the gate pattern boundary in Fig. 2-2-4 (a). During the gate oxide etching, the oxide between the main-gate and the sub-gate was not etched because the space between the main-gate and sub-gate was filled with the reflowed photoresist. The dopants of the implantation for source and drain will not be injected to poly-Si under the extended oxide region, thereby creating the offset region in Fig. 2-2-4 (b). The structure can improve the mis-alignment problem in the conventional offset gated poly-Si TFT's due to the additional photolithography step to form an offset region. The forward and reverse transfer characteristics of the asymmetric device exhibit significant different device characteristics, while those of the symmetric device are not changed in Fig. 2-2-5. In the asymmetric poly-Si TFT's, the reverse I_D-V_G curve, when the offset length of source is larger than that of drain side, shows that the maximum current is decreased from 1.6×10^{-5} A to 4.1×10^{-6} A and the threshold voltage is increased from 6.8 to 9.9 V, compared with the forward I_D-V_G curve. The self-aligned offset gated poly-Si TFT's not only save a mask step but also is a symmetric device. Unfortunately, the devices still have a large series parasitic resistance in the turn-on and turn-off regions.

2-3. Lightly Doped Drain (LDD)

The current pinching phenomenon in the offset gate structure can improved by employing an n^--region between the channel and drain, i.e., lightly doping the offset region as shown in Fig. 2-3-1[2.9]. The LDD region can be formed by, for example, an additional implantation or ion-doping[2.10] of impurity atoms with a low dosage. Alternatively, the LDD region can be formed by doping through a thick insulating

layer, such as SiO_2 or TaOx[2.11] extending from the gate edge. LDD region can be formed together with doping for the source and drain, since the insulating layer lowers the acceleration voltage and hence the doping concentration,

Since the parasitic resistance effect is inversely proportional to the LDD doping concentration N_{LDD} while the drain field decreases for decreasing requirement of the TFT. The LDD structure also lowers the lateral field in the saturation region, and consequently, decreases the impact ionization rate[2.12].

One of the difficulties in preparing the LDD structure is that the lightly doped implant, in addition to being expensive, is difficult to reproduce. This is because the background doping and the doping efficiency, both closely related to the grain size and defects in the grain boundary and within the grains, vary from run to run and are difficult to control. The other difficulty is variations in the channel length L_{ch} and the offset length L_{off} (the distance from the gate edge to the heavily doped drain region). Because the offset area is lithographically defined with respect to the channel area, L_{ch} and consequently L_{off} vary between devices. This in turn introduces variations in the I-V characteristics, and implies questions for the device reliability and limitation on the integration of sub-micrometer circuits. As result, the performance nonuniformity has been the major issue for the yield of integrated circuits which incorporate TFT's.

A simple lightly doped drain (LDD) structure is utilized to control the channel electric field at the drain junction and to improve the performance of the TFT's. The LDD region is self-aligned to the channel and the source/drain regions[2.13]. A thick oxide layer is first deposited and patterned to define the channel region. It serves as a mask which covers the channel region in the LDD implant in Fig. 2-3-2 (a). The device is created by a spacer around an oxide mask which exclusively defines the channel length L_{ch} in Fig. 2-3-2 (b). The process of the spacer does not affect L_{ch} and

requires no further lithography steps. Consequently, the LDD length L_{LDD} and channel length L_{ch} can be well controlled in the deep-submicrometer regime, thereby improving the device stability and the submicrometer integration. In addition, by removing one lithography step, the process complexity is also reduced. Therefore, systematic experimental data show that the saturation current, leakage current, ON/OFF current ratio, and ***SS*** of the inverted TFT's are closely related to V_D, L_{ch}, V_G, L_{LDD}, and the LDD dose. Variations of the saturation current are caused by the resistance in the lightly doped source region, which reduces the effective V_G and V_D. With an LDD dose of ≥ $10^{14}/cm^2$, the resistance is small enough not to affect the saturation current of the device. The leakage current is minimized with a structure which balances the channel electric field at the drain junction. It depends strongly on L_{LDD} and the LDD implant dose. For example, an LDD implant with 1 x $10^{14}/cm^2$ boron ions at 20 keV optimizes the ON/ OFF current ratio for an L_{LDD} = 0.3 μm device. The parasitic resistance is more improved than that in the offset-gate TFTs. But, the parasitic resistance is still larger than it in the conventional TFTs.

2-4. Gate-Overlapped LDD (GOLDD)

In the GOLDD structure[2.14][2.15][2.16][2.17], the gate overlaps with the LDD region is proposed. The key process sequence of the GOLDD TFTs is the buffer oxide etching after the photolithographic step for n^+ implant in Fig. 2-5-1 (a). The buffer oxide is employed in order to remove an additional implantation for LDD and create a thin LDD region so that the series resistance of the LDD can be more easily controlled by the overlapped gate electric field.

The ON currents of GOLDD TFT's are almost identical with the conventional TFT without offset due to the significant decrease of series resistance in the LDD region regardless of buffer oxide thickness. This is because, under identical overlap

gate bias, the amount of electron carriers accumulated in the LDD region is almost constant regardless of initial doping concentration. At the OFF state, the location of peak electric field is almost fixed at the n-/n+ junction due to the decrease of electron concentration in LDD region under the negative gate bias; this results in a relatively uniform ON/OFF current ratio regardless of LDD doping level. We have also found that the ON current of new devices is much more immune to the change of LDD length, which is known as an advantage of the FID poly-Si TFT's over the conventional offset-gate poly-Si TFT's. Owing to the gate modulation of the LDD region, the series resistance problems of LDD are substantially suppressed. In addition, kink-effect and hot-carrier induced degradation are improved. This is because, the electron current, flowing at the insulator/semiconductor interface along the channel, is redirected towards the back channel at the channel/n^- region junction and flows at the back of the n^- region, where the electron concentration is still sufficiently high to support the current flow. When the device is operated at pinch off condition, the LDD region is depleted and current path diverted two passes at the top and bottom[2.18]. As a result, the impact ionization and hot-carrier injection is concentrated in the back channel region.

But, GOLDD TFT fabrication require the use of a high temperature process, such as poly-Si sidewall gates[2.19] or additional photolithographic processes [2.20]. In the GOLDD structure, the parasitic capacitance increases due to the overlap between the gate and the LDD region, thus the high-speed operation of the TFTs will be compromised.

Chapter 3

Fabrication and Characterization

3-1. Fabrication Process of GOLDD Poly-Si TFTs

In this experiment, we fabricate the poly-Si TFTs with typical T-gate structure and self aligned GOLDD successfully. The top view of the devices is shown in Fig. .3-1-1 and the schematic cross sectional view of devices with the structure is shown in Fig. 3-1-2. The fabrication procedure is described as follow in Fig. 3-1-3.

Step1. Substrate

100 mm p-type single crystal silicon wafers with (100) orientation were used as the starting materials. After a STD initial cleaning procedure. Si wafers were deposited with 550-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000 ℃.

Step2. Poly-Si thin film formation

Undoped poly-Si layers and undoped amorphous-Si with thickness with thickness of 100 nm were deposited by low pressure chemical vapor deposition (LPCVD) on oxide by pyrolysis of silane (SiH_4) at 620°C and 550°C respectively. The amorphous-Si films were recrystallized by solid phase crystalliztion (SPC) method at 600 ℃ for 24 hrs in an N_2 ambient. These as-deposite poly-Si and recrystallized poly-Si films were then patterned into islands by transformer couple plasma (TCP) etching using the mixture of Cl_2 and HBr.

Step3. Gate oxide formation

In order to decrease the roughness of interface between gate-oxide and poly-Si

island, thermal oxidation of silicon is excluded. After defining the active region, the wafers were boiled in RCA initial cleaning procedure to ensure cleanliness of the wafers before deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Soon, the gate insulator was deposited in a horizontal furnace using TEOS and O_2 gases at 700°C. The thickness of the TEOS oxide thin film is 50nm.

Step4. Raised Gate electrode formation

After deposition of gate insulators, another 250nm doped poly-Si films were deposited immediately on the gate insulators by vertical furnace. The second TEOS film was deposited above the gate layer in Fig. 3-1-3 (a). The TEOS film was defined by gate mask. The TEOS film was etched by using TEL5000 oxide etcher in Fig. 3-1-3 (b). The gate-overlapped LDD structure was self-aligned by using selective side etching of the TEOS film in Fig. 3-1-3 (c). The raised structure was then patterned by transformer couple plasma (TCP) etching to define the gate regions and to be the mask for self-aligned implantation in Fig. 3-1-3 (d). Then, we use BOE to etch the TEOS layer above the gate, drain and source in Fig. 3-1-3 (e). The In-line SEM figure is shown in Fig. 3-1-4. We employ the side etching time to control the LDD length from 0.158 μm to 0.594 μm without an additional mask or a spacer etching process.

Step5. Source/drain formation

After shielding the body contact region by lithography process, phosphorus ions at a dose of 3×10^{15} ions/cm^2 were implanted to form the n^+ source and drain regions. Then, phosphorus ions at a dose of 1×10^{13} ions/cm^2 were implanted to form the n^- LDD regions in Fig. 2-1-3 (f).

Step6. Body formation.

When the body contact was exposed with shielding the remaining gate and

source/drain areas, boron ions at a dose of 3×10^{15} ions/cm^2 were implanted to form a p^+ contact region. Dopants were activated by rapid thermal annealing (RTA) at 800 ºC for 20 sec.

Step7. Metallization

The aluminum layers were deposited by thermal coater for 0.5 μm and then patterned at the gate, source/drain and body contact regions as the metal pads. Finally, the finished devices were sintered at 400 °C for 30 minutes in an N_2 ambient.

Step8. Passivation

It is known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. Therefore, to reduce trap density and improve interface quality, wafers were also immured in an NH3 plasma generated by plasma enhanced CVD (PECVD) at 300 ºC for 2 hr.

3-2. Method of Device Parameter Extraction

In this section, we will introduce the methods of typical parameter extraction such as threshold voltage, On/Off current ratio, channel resistance and the parasitic resistance from device characteristics.

3-2-1. Determination of the threshold voltage

Plenty ways are used to determinate the threshold voltage (V_{th}) which is the most important parameter of semiconductor devices. The method to determinate the threshold voltage in my thesis is the *constant drain current method* that the voltage at a specific drain current I_N is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified at 10nA for $V_D = 0.1$ V and 100 nA for $V_D = 5$ V in most papers to

extract the threshold voltage of TFTs.

3-2-2. Determination of On/Off Current Ratio

On/Off ratio is another important factor of TFTs. High On/Off ratio represents not only large turn-on current but also small off current (leakage current). It affects the bright and dark states of TFT screens directly. The leakage mechanism in poly-Si TFTs is much different from conventional MOSFETs since the channel layer of poly-Si TFTs is composed of polycrystalline. A large amount of trap densities in grain structure serve as lots of defect states in energy band gap to enhance tunneling effect. Therefore, the leakage current due to trap-assisted tunneling effect is much larger in poly-Si TFTs than in the single crystal MOSFETs.

There are many methods to specify the on and off current. The easiest one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage equal to 5V.

3-2-3. Determination of the channel resistance and the parasitic resistance

It is well known that the channel resistance and the parasitic resistance can be extracted from the output characteristics of devices with various channel length. For example, the output characteristics of the fabricated devices are depicted in Fig. 3-2-1. When devices are operated under small drain voltage and high gate voltage, their ON resistance (R_{on}) can be expressed as

$$R_{on} = \frac{\partial V_D}{\partial I_D} = R_{ch} + R_p \qquad (3\text{-}1)$$

where R_{ch} and R_p represent channel resistance and parasitic resistance. Therefore, when fitting the linear region in Fig. 3-2-1 by least square regression as in Fig. 3-2-2, the R_{on} can be obtained from the slope of those straight lines. Since the channel

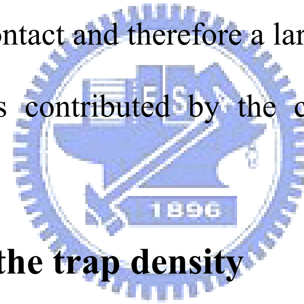
resistance in the linear region can be given approximately by

$$R_{ch} = \frac{L}{W\mu C_{ox}(V_G - V_{TH})} \tag{3-2}$$

$L = L_{eff} = L_{MASK} - l_0$

V_{TH} is defined by constant current

where C_{ox} is the gate dielectric capacitance per unit area and W is device channel width, respectively. The parasitic resistance R_p can be extracted by plotting width-normalized R_{on} versus L as in Fig. 3-2-3[3.1]. It is found that all the width-normalized R_{on} vs L curves merge at l_0 = 0 μm and has a residual value of a gate-voltage independent R_p of 5 kΩ. l_0 can be viewed as a characteristics length for the accumulation channel under the S/D region. A larger l_0 represents a smaller current spreading under the contact and therefore a larger parasitic resistance. Usually, the parasitic resistance R_p is contributed by the contact resistance and also the source/drain resistance.



3-2-4. Determination of the trap density

The grain boundary potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs.As proposed by Levinson *et al*, the *I-V* characteristics including the trap density can be obtained:

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \exp(-\frac{q^3 N_t^{\,2} t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}) \tag{3-3}$$

This equation had been further corrected by Proano *et al*. by considering the mobility under low gate bias. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in

an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$tch = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \tag{3-4}$$

The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp\left(-\frac{q^2 N_t^{\,2} \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^{\,2}(V_G - V_{FB})^2}\right) \tag{3-5}$$

The effective trap state density then can be obtained from the slope of the curve $ln[I_D/(V_G\text{-}V_{FB})V_D]$ versus $(V_G\text{-}V_{FB})^{-2}$.

Chapter 4

Electrical Characteristics of GOLDD TFTs

4-1. Typical characteristics comparison

Fig. 4-1-1 presents the I_D-V_G characteristic for non-LDD and GOLDD TFTs. The circle lines represent the I_D-V_G characteristic of standard TFTs and square lines represent this of GOLDD TFTs which LDD length is 0.158 μm and LDD doping is 1×10^{18} ions/cm^3. All devices are n-type TFTs. In this figure, the off current of the GOLDD TFTs is lower than that of the standard TFTs. The dominant mechanism of off current is known to be the field emission via grain boundary traps due to a high electric field in the drain depletion. In the GOLDD TFTs, the LDD area can decrease the electric field near the drain region to suppress the leakage current. But, the on current of the GOLDD TFTs is slightly larger than that of the conventional TFT. This is because the GOLDD TFTs have the smaller series resistance. So, the on/off current ratio in the GOLDD was higher by two orders of magnitude.

From the Fig. 4-1-2 (a) (b) (c), we can find the effective length and parasitic resistance. The related extracted data is listed in Table I and Table II for devices with different channel widths. The effective length in the GOLDD TFTs and also the conventional TFTs is smaller than the designed (mask) length, which is associated to dopant redistribution. Fig. 4-1-3 shows the dopant redistribution condition in the conventional and GOLDD TFTs. The parasitic resistance in the GOLDD TFTs is much smaller than the in the conventional TFTs. A plausible reason is that the gate-overlapped lightly doped region enhances the carrier density and therefore increases the driving current. The other possible reason is that the GOLDD TFTs have

two RTA processes but conventional TFTs have only one RTA process. Besides, the different current paths for GOLDD and conventional TFTs in Fig. 4-1-4 are also another reason. The conclusion is that the effective length and parasitic resistance are affected by dopant redistribution, the enhancement of the carrier density, different RTA order and current path.

As increasing the LDD length, decreasing the effective length and increasing the parasitic resistance. The reason is that GOLDD TFTs of long LDD length have much defect due to ion impanting.

Fig. 4-1-5 shows the I_G-V_D characteristic for conventional and GOLDD TFTs. The circle line represents the I_G-V_D characteristic of conventional TFTs and square line represents that of GOLDD TFTs which LDD length is 0.158 μm and LDD doping is 1×10^{18} ions/cm^3. In the figure, it is obviously observed that our fabrication process does not damage gate oxide in order to two lines almost match together.

4-2. Short channel effect

The I_D-V_D characteristics for conventional and GOLDD TFTs show in the Fig. 4-2-1. The circle line represents the I_D-V_D characteristic of conventional TFTs and triangular line represents this of GOLDD TFTs which LDD length is 0.594 μm and LDD doping is 1×10^{18} ions/cm^3. From this figure, we find that the GOLDD TFTs slightly suppress the kink effect. In our experiments, LDD length is must enough long otherwise kink effect does not decrease. Because the device is operated at pinch off condition, the LDD region which is depleted and current path diverted two passes at the top and bottom.

Then, we find the second saturation of the drain current in the GOLDD TFTs. Because biasing the device in the kink regime causes electron depletion in the n^- region, due to the negative gate-to-n^--region potential induced by the increasing drain

voltage. From the Fig. 4-2-2, the electron current, flowing at the insulator/ semiconductor interface along the channel, is redirected towards the back channel at the channel/n^--region junction and flows at the back of the n^- region, where the electron concentration is still sufficiently high to support the current flow. As drain voltage increasing, the depletion removes toward channel region. When the whole n^- region depleted, the second saturation of the drain current is observed.

From the Fig. 4-2-3, it shows the threshold voltage (V_{th}) versus different channel length (L) characteristics for conventional and GOLDD TFTs. The circle line represents the characteristic of conventional TFTs, square line represents this of GOLDD TFTs which LDD length is 0.158 μm and LDD doping is 1×10^{18} ions/cm^3 and triangular line represents this of GOLDD TFTs which LDD length is 0.594 μm and LDD doping is 1×10^{18} ions/cm^3. We find that drain current which V_D is 0.1 V in the conventional TFTs has reverse short channel effect. The reason is dopant redistribution. Then, V_{th} in the conventional TFTs is observed a phenomenon of threshold voltage roll-off due to charge sharing cause. Fig. 4-2-4 shows the different depletion region for conventional and GOLDD TFTs. Fig. 4-2-5 plots the conventional TFTs' threshold voltage shift (ΔV_{TH}) versus different reverse channel length (L^{-1}). We see that the plot is almost linear. So, it can verify that the threshold voltage roll-off is caused by charge sharing.

Fig. 4-2-3 also shows that the threshold voltage increases as the LDD length increases. This is because the device which is long LDD length has the more defect in active layer due to doping implantation.

Fig. 4-2-6 shows the I_D-V_G characteristics for different LDD length in the GOLDD TFTs when devices operate at V_D = 5 V. The circle line represents the characteristic of GOLDD TFTs which LDD length is 0.158 μm and LDD doping is 1

× 10^{18} ions/cm^3 and triangular line represents this of GOLDD TFTs which LDD length is 0.594 μm and LDD doping is 1 × 10^{18} ions/cm^3. As LDD length increases, the on-current is almost the same. The leakage current which V_G = -9 V in the long LDD length is lower than that in the short LDD length due to the high electric field reduce. However, the off current which V_G = -1.5 V in the long LDD length is higher than that in the short LDD length. Because the off current mechanism is not high field effect, the off current comes from the natural resistance. The total length for the LDD length and channel length is the same. So, LDD length is longer, the channel length is shorter. The resistance for LDD region is lower than that for undoped channel region. The subthreshold swing (S.S.) for long LDD length is smaller than it for short LDD length. The reason is that the trap density in the device which has long LDD length are more than that which has short LDD length. Fig. 4-2-7 shows the relative trap extracted. The related extracted data is listed in Table Ш for devices with different LDD length.

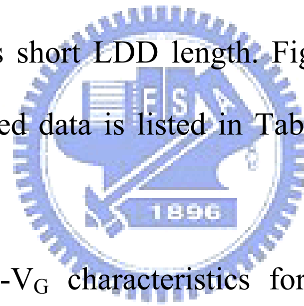


Fig. 4-2-8 shows the I_D-V_G characteristics for different LDD length in the GOLDD TFTs when devices operate at V_D = 0.1 V. The circle line represents the characteristic of GOLDD TFTs which LDD length is 0.158 μm and LDD doping is 1 × 10^{18} ions/cm^3 and triangular line represents this of GOLDD TFTs which LDD length is 0.594 μm and LDD doping is 1 × 10^{18} ions/cm^3. The leakage current which V_G = -10 V in the long LDD length is higher than that in the short LDD length due to gate induced barrier lowering (GIBL). Fig. 4-2-9 shows the energy band for the channel and LDD region at V_D = 0.1 V and V_G = -10 V. The energy band bending for the LDD region is more serious than that for the channel region. So, leakage current for the devices which have long LDD length is higher than that which have short LDD length.

Fig. 4-2-10 and Fig. 4-2-11 show the average drain current versus gate voltage for different LDD length. In our experiment, we measure ten devices to average the drain current. From the pictures, the above-mentioned conclusions are proved repeatedly.

4-3. Reliability

From the Fig. 4-3-1, Fig.4-3-2 Fig.4-3-3, Fig.4-3-4, Fig.4-3-5, Fig.4-3-6, Fig.4-3-7, Fig.4-3-8 and Fig.4-3-9 show that increasing LDD GOLDD TFT have high ability to resist the hot-carrier stress. The reason for hot-carrier stress is that the high drain voltage applied in the drain region results the high electric field in the depletion near the drain to accelerate the carriers. So, the accelerated carriers would bombard and damage the drain region to result parasitic resistance. However, the GOLDD TFTs can decrease the damage due to lower the electric field near the drain. Besides, increasing LDD length, the device has the higher resistibility for hot-carrier stress. This is because the devices which have long LDD length can more reduce the electric field near the drain region. After stressed, we find that the current which reversed the drain and source is lower than it which did not reverse. But, the degeneracy for the measurements reversed is more slightly than that which did not reverse. The devices which reversed drain and source take damage region as source. So, the current flow for electrons suffers many defects as first to lower the total current. But, drain current in the high electric field does not suffer the defect by hot-carrier stress and the degeneracy is dropped. The drain voltage which happens current saturation is lower.

Chapter 5

Conclusion

In this thesis, a novel self-aligned gate-overlapped LDD poly-Si TFT was fabricated by using a TEOS layer as a mask. We used this layer to form raised gate and defined LDD regions. Therefore, this self-aligned process is very simple that no additional lithography mask is needed. Also, since the structure can be accomplished by only using wet etching process, the plasma damage associated with the RIE etch back process for typical spacer structure can be avoided. We can control various LDD lengths by simply changing the oxide wet etching time. The experiment shows that self-aligned GOLDD poly-Si TFT can decreases the OFF current and suppress the kink effect.

To self-aligned define the LDD region, the raised gate electrode had to be formed. Then the S/D region and the LDD region can be defined by only adjusting the energy and the dopant density during implantation. The LDD region implantation needs higher energy since the dopant has to penetrate the thin gate region and also the gate oxide. We had carefully measured the oxide leakage current, and found that no degradation was caused by this implantation step. As a result, the on/ off current ratio can be improved to two orders of magnitude than the conventional TFTs.

The parasitic resistance is also decreased to be only 1/5 of that of standard devices. This is maybe due to the enhanced carrier density in the gate-overlapped lightly doped region. When analyzing the threshold voltage roll-off phenomenon, it is found that our devices exhibit much superior short channel effect immunity than conventional ones. Finally, by using hot-carrier stress to examine the reliability of the proposed

devices, it is also verified that the GOLDD devices have better reliability than standard devices. Suppressed hot-carrier degradation are found such as smaller leakage current variation or the little subthrehsold swing degradation.

It can be concluded that a novel and simple GOLDD TFTs had been proposed and demonstrated successfully. Without any complicated process or any high-cost mask or lithography process, this structure is appliable to the current AMLCD technology.

Reference

Chapter 1.

[1.1] C. H. Fa and T. T. Jew, “The polysilicon insulated-gate field-effect transistors,” *IEEE Trans. Electron Devices*, vol. 13, no. 2, pp. 290, 1966.

[1.2] H. Oshima and S. Morozumi, “Future trends for TFT integrated circuits on glass substrates,” *IEDM Tech. Dig*., pp. 157, 1989.

[1.3] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, “Polysilicon TFT technology for active matrix OLED displays ,” *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001.

[1.4] H. Kuriyama et al., “An asymmetric memory cell using a C-TFT for ULSI SRAM,” *Symp. On VLSI Tech*., pp. 38, 1992.

[1.5] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanala, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K. Sasaki, T. Nishida, T. Mine, E. Takeda, and T. Nagano, “Advanced TFT SRAM cell technology using a phase-shift lithography,” *IEEE Trans. Electron Devices*, Vol. 42, pp. 1305-1313,1995.

[1.6] K. Yoshizaki, H. Takaashi, Y. Kamigaki, T.asui, K. Komori, and H. Katto, *ISSCC Digest of Tech*., pp. 166, 1985.

[1.7] N. D.Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French , “The fabrication and characterization of EEPROM arrays on glass using a low-temperature poly-Si TFT process,” *IEEE Trans. Electron Devices*, Vol. 43, pp. 1930-1936, 1996.

[1.8] T. Kaneko, U. Hosokawa, N. Tadauchi, Y. Kita, and H. Andoh, “400 dpi

integrated contact type linear image sensors with poly-Si TFT's analog readout circuits and dynamic shift registers," *IEEE Trans. Electron Devices*, Vol. 38, pp. 1086-1093, 1991.

[1.9] U. Hayashi, H. Hayashi, M. Negishi, T. Matsushita, *Proc. of IEEE Solid-State Circuits Conference (ISSCC),* pp. 266 , 1998.

[1.1]N.Yamauchi, U. Inava, and M. Okamura, "An integrated photodetector-amplifier using a-Si p-i-n photodiodes and poly-Si thin-film transistors," *IEEE Photonic Tech. Lett,* Vol. 5, pp. 319-321, 1993.

[1.11] M. G. Clark, *IEE Proc. Circuits Devices Syst*, Vol. 141, 133 (1994)

[1.12] Noriyoshi Yamauchi, Jean-Jacques J. Hajjar and Rafael Reif, "Polysilicon thin-film transistors with channel length and width comparable to or smaller than the grain zize of the thin film," *IEEE Trans. Electron Devices*, Vol. 38, pp 55-60, 1991.

[1.13] Singh Jagar, Mansun Chan, M. C. Poon, Hongmei Wang, Ming Qin, Ping K. Ko, Yangyuan Wang, "Single grain thin-film-transistor (TFT) with SOI CMOS performance formed by metal-induced-lateral-crystallization," *IEDM Tech. Dig*., pp. 293-296, 1999.

[1.14] J. R. Ayres and N. D. Young, "Hot carrier effects in devices and circuits formed from poly-Si," *IEEE proc. Circuits Decices Syst.*, vol. 141, no. 1, pp. 38, 1994.

[1.15] M. J. Powell , C. van Derkel, and J. R. Hughes, " Time and temperature dependence of instability mechanisms in amorphous silicon TFTs," *Appl. Phys. Lett*., vol. 54, no. 14, pp. 1323, 1989.

[1.16] J. S. Im, M. A. Crowder, R. S. Sposili, J. P. Leonard, H. J. Kim, J. H. Yoon, V.

V. Gupta, H. Jin Song, and H. S. Cho "Controlled Super-Lateral Growth of Si Films for Microstructural Manipulation and Optimization" *phys. stat. sol.* (a) 166, 603 1998.

[1.17] Yue Huo, ”Thin Film Transistors Materials and Process Volume 2: polycrystalline Silicon Thin Film Transistors."

[1.18] K. R. Olasupo and M. K. Hatalis, ”Leakage current Mechanism in Sub-Micron Polysilicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1218, 1996.

[1.19] Wei Wu, Tiao-Yuan Huang, Warren B. Jackson, Alan G. Lewis, and Anne Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma Hydrogenation," *IEEE Electron Device Lett.*, vol. 12, pp. 181-183, 1991.

[1.20] Wei Wu, Alan G. Lewis, Tiao-Yuan Huang, and Anne Chiang, "Effects of trap-state density reduction by plasma hydrogenation in low-temperature polysilicon TFT," *IEEE Electron Device Lett.*, vol. 10, pp. 123-125, 1989.

[1.21] S. M. Sze, "Physics of Semiconductor Devices, 2nd ed" New York: Wiley-Interscience,1982.

[1.22] G. Vincent, A. Chantre, and D. Bois, "Electric field effect on the thermal emission of traps in semiconductor junctions" *J. Appl. Phys.* Vol.50, No.8, August, 1979.

[1.23] W. Schockley, W. T. Read, "Statistics of recombination of holes and electrons," *Phys. Rev.*, 87 (5), pp. 835, 1952.

[1.24] M. Hack and Alan G. Lewus, "Avalanche-Induced effects in polysilicon Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 12, no. 5, pp.

203-205, 1991.

[1.25] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, "Floating Body Effects in Polysilicon Thin-Film Transistors," *IEEE Trans. on electron Devices*, vol. 44, no. 12, pp. 2234-2241, 1997.

[1.26] L. Mariucci, G. Fortunato, A. Bonfiglietti, M. Cuscuna, A. Pecora, and A. Valletta, "Polysilicon TFT Structures for Kink-Effect Suppression," *IEEE Trans. on Electron Device*s, vol. 51, no. 7, July, pp. 1135, 2004.

[1.27] Yasuyoshi Mishima and Yoshili Ebiko, "Improved Lifetime of Poly-Si TFTs with a Self-Aligned Gate-overlapped LDD structure," *IEEE Trans. on Electron Devices*, vol. 49, no. 6, June, pp. 981, 2002.

Chapter 2.

[2.1] S. Morozumi, K. Oguchi, S.Yazawa, T. Kodaria, H. Ohshima and T. Mano, "B/W and color LC video displays addressed by poly-Si TFT's," *1983 Soc. Information Display Dig. Tech. Pap.*, pp. 156, 1983.

[2.2] S. Morozumi, K. Oguchi, R. Araki, T. Sonehara, and S. Aruga, "Full-color TFT-LCD with phase-change guest-host mode," in *SID 85 Dig.*, pp. 278, 1985.

[2.3] R. E. Proano, R. S. Misage and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Electron Device Lett.,* vol. 36, no. 9, pp. 1915-1922, 1989.

[2.4] M. Hack, I-Wei Wu, "Analysis of leakage currents in multiple gate poly-si thin film transistors for active matrix liquid crystal displays," *IEEE Device Research Conference*, pp. 51 - 52, 1994

[2.5] L Mathew, Yang Du, A. V-Y Thean, M. Sadd, A.Vandooren, C. Parker, T. Stephens, R. Mora, Raghav Rai, M. Zavala, D. Sing, S. Kalpai, J. Hughes, R. Shimer, S. Jallepalli, G. Workman, B. E. White, B.-Y. Nguyen, J. Mogab, "Multi gated device architectures advances, advantages and challenges,' *IEEE Integrated Circuit Design and Technology, 2004. ICICDT '04. International Conference*, pp. 97–98, 2004.

[2.6] K. Tanaka, H. Arai and S. Kohda, "Characteristics of Offset-structure Polycrtstalline-Silicon Thin-Film Transistors," *IEEE Electron Device Lett.,* vol. 9, no. 1, January, pp. 23, 1988.

[2.7] B. H. Min, C. M. Park, amd M. K. Han, "A Novel Offset Gated Polysilicon Thin Film Transistor Without an Additional Offset Mask," *IEEE Electron Device Lett.,* vol. 16, no. 5, pp. 161, 1995.

[2.8] C. M. Park, B. H. Min, J. H. Jun, J. S. Yoo and M. K. Han, "Self-Aligned Offset Gated Poly-Si TFT's with a Floating Sub-Gate," *IEEE Electron Device Lett.,* vol. 18, no. 1, 16, 1997.

[2.9] K. Nakazawa, K. Tanaka, S. Suyama, K. Kato, and S. Kohda, "Lightly Doped Drain TFT Structure for Poly-Si LCDs," 1*990 Soc. Information Display Dig. Tech. Pap*., pp. 311, 1990.

[2.10] S. Yuda, K. Kitai, Y. Segawa and Y. Okita, "Improved poly-Si TFTs with all lightly doped drain structure using an ion doping process," *Dig. Of Techn. Pap. 1994 Int. Workshop on Active-Matrix Liquid-Crystal Display-TFT technologies and Related Materials*, Tokyo, pp. 136, 1994.

[2.11] M. Furuta, S. Moaegawa, H. Sano, T. Yoshida, Y. Uraoka, H. Tsutsu, I. Kobayashi, T. Kawamura and Y. Miyata, "A 2.8-in. Diagonal Low-Temperature-Processed Poly-Si TFT-Lces with New LDD Structure,"

Proc. Of the 16th Int. Display Research Conference, Birmingham, pp. 547, 1996.

[2.12] Chun Ting Liu and K. H. Lee, "An experimental study on the short-channel effects in undergated polysilicon thin-film transistors with and without lightly doped drain structures," *IEEE Electron Device Lett.*, vol. 14, no. 3, pp. 149-151, 1993.

[2.13] Chun-Ting Liu, Chen-Hua Douglas Yu, Avi Kornblit, amd Kuo-Hua Lee, "Inverted thin-film transistors with a simple self-aligned lightly doped drain structure," *IEEE Trans. on Electron Devices*, vol. 39, no. 12, pp. 2803-2809, 1992.

[2.14] J. G. Fossum, A. Oritz-Conde, H. Shichijo and S. K. Banerjee, "Anomalous leakage current in LPCVD polysilicon MOSTFT's," *IEEE Trans. Electron Devices*, ED-32, pp. 1878, 1985.

[2.15] Kwon-Young Choi and Min-Koo Han, "A Novel Gate-overlapped LDD Poly-Si Thin Film Transistors," *IEEE Electron Device Lett.*, vol. 17, no. 12, pp. 566-568, 1996

[2.16] K. Y. Choi, K. C. Park, C. H. Kim, J. S. Yoo and M. K. Han, "Fabrication of Gate Overlapped-LDD poly-Si TFT for Large Area AMLCD," E*xtended Abstract of the 1997 Int. Conf. Solid State Devices and Materials (SSDM),* pp. 358, 1997.

[2.17] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres and M. J. Yrainor, "Influence of melt depth in laser crystallized poly-Si thin film transistors," *J. Appl. Phys.*, 82, 4086 ,1997.

[2.18] Pecora, F. Massussi, L. Mariucci, G. Fortunato, J. R. Ayres and S. D. Brotherton, "Numerical analysis of the electrical characterization of gate

overlapped lightly doped drain polysilicon thin film transistors." *Jpn. J. Appl. Phys.*, 38, 3475, 1999.

[2.19] M. Hatano, H. Akimoto, and T. Sasaki, "A novel self-aligned gate- overlapped LDD poly-Si TFT with high reliability and performance," in *IEDM Tech. Dig.*, pp. 523–526, 1997.

[2.20] N. D. Young, I. D. French, M. J. Trainor, D. T. Murley, D. J. McCulloch, and R.W.Wilks, "LTPS for AMLCD on glass and polymer substrates," in *Int. Display Workshop 99, Sendai, Japan*, pp. 219–222, 1999.

Chapter 3

[3.1] Shengwen Luan and Gerold W. Neudeck, "An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors ." , *J. Appl. Phys.* Vol. 72, No. 2,pp.766-772, 15 July 1992.