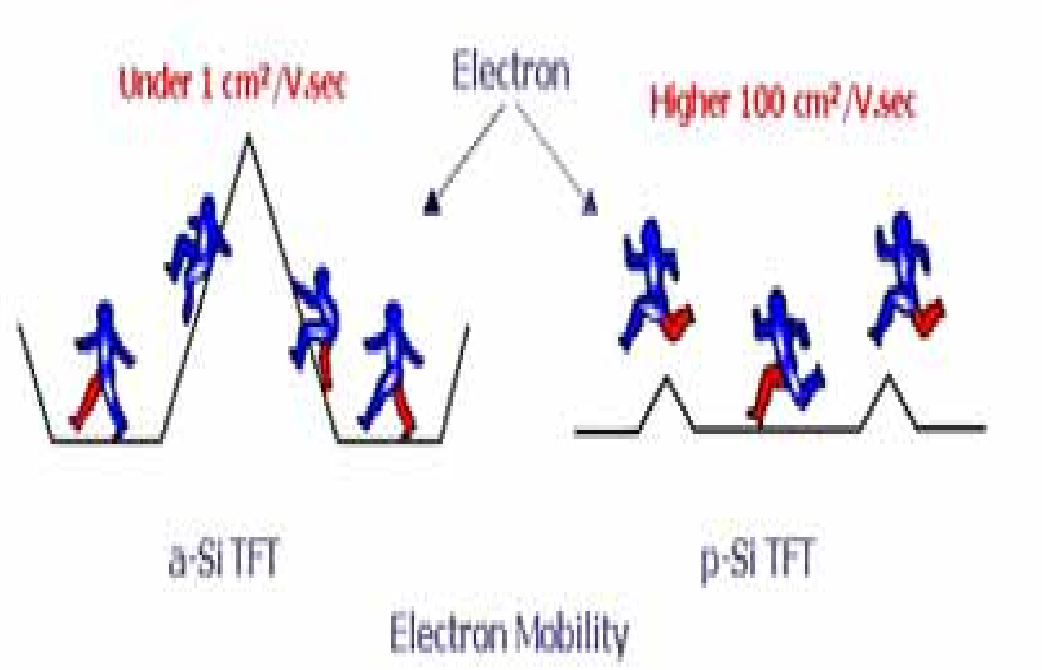


Fig. 1-1-1 The electron mobility for a-Si and poly-Si TFT.

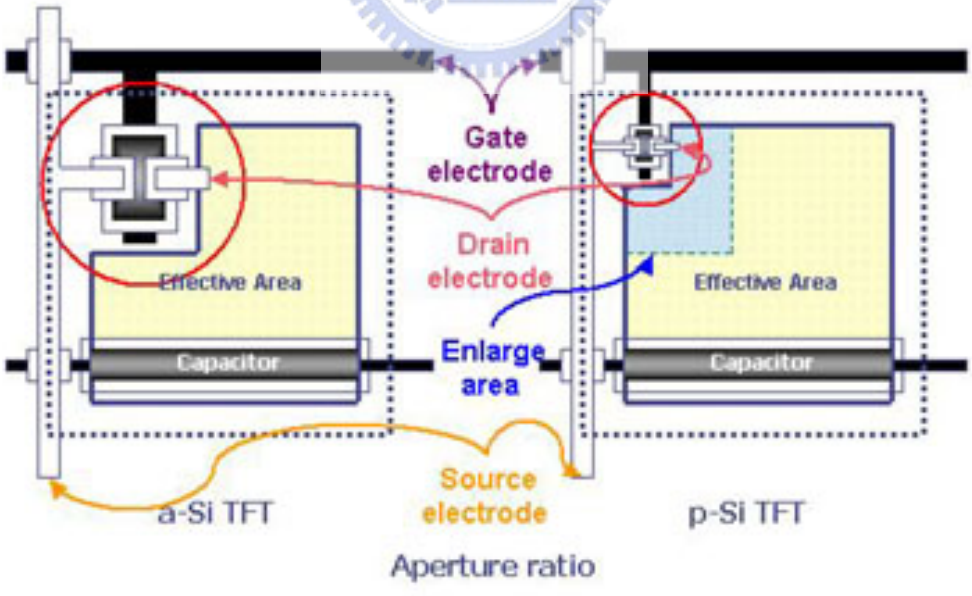


Fig. 1-1-2 The aperture ratio for a-Si and poly-Si TFT.

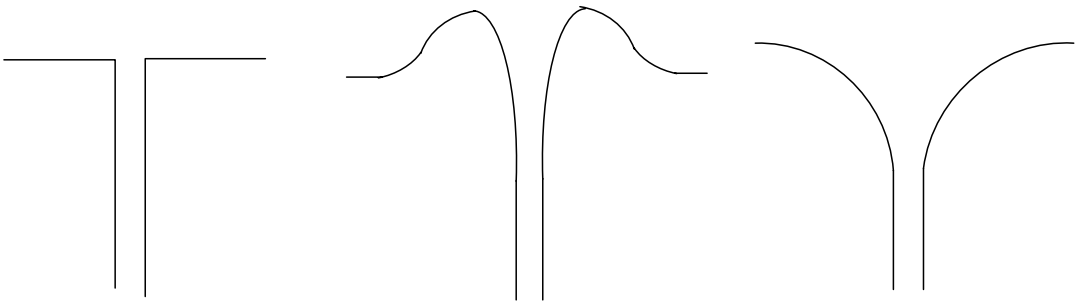


Fig. 1-2-1 All kinds defect well.
(a) is the Dirac well.
(b) is the repulsive Columbic well.
(c) is the Columbic well.

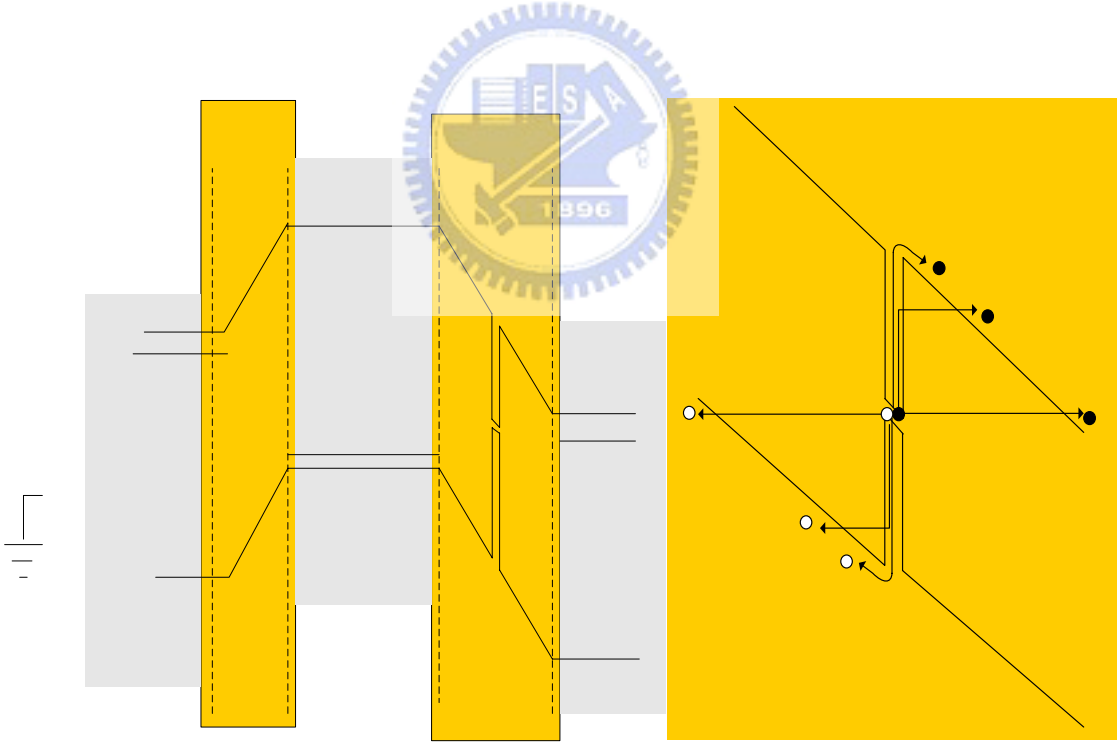


Fig. 1-2-2 Schematic illustration of the leakage current mechanisms.
(a) thermionic emission. (TE)
(b) thermionic field emission. (TFE)
(c) pure field emission. (FE)

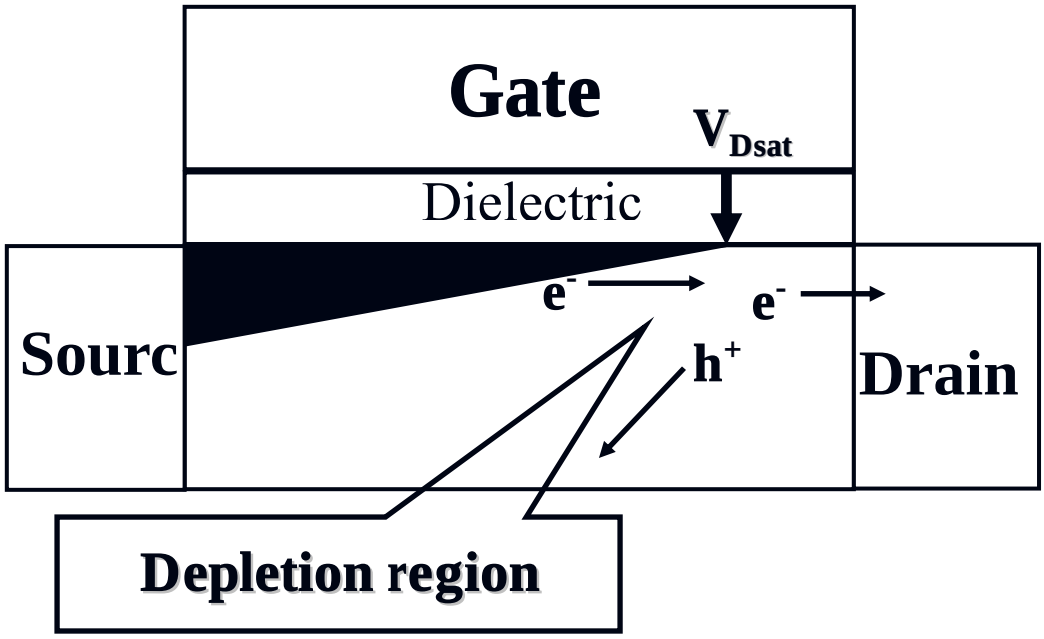


Fig. 1-2-3 The devices operate in the saturation.

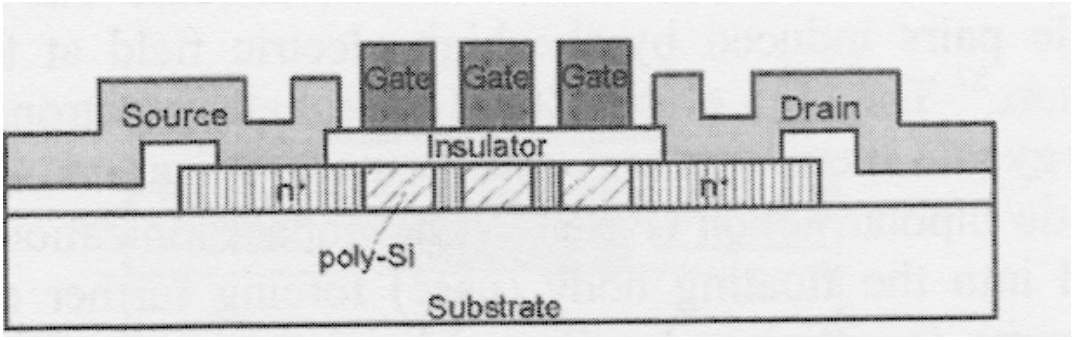


Fig. 2-1-1. Cross section of the multiple-gated TFT

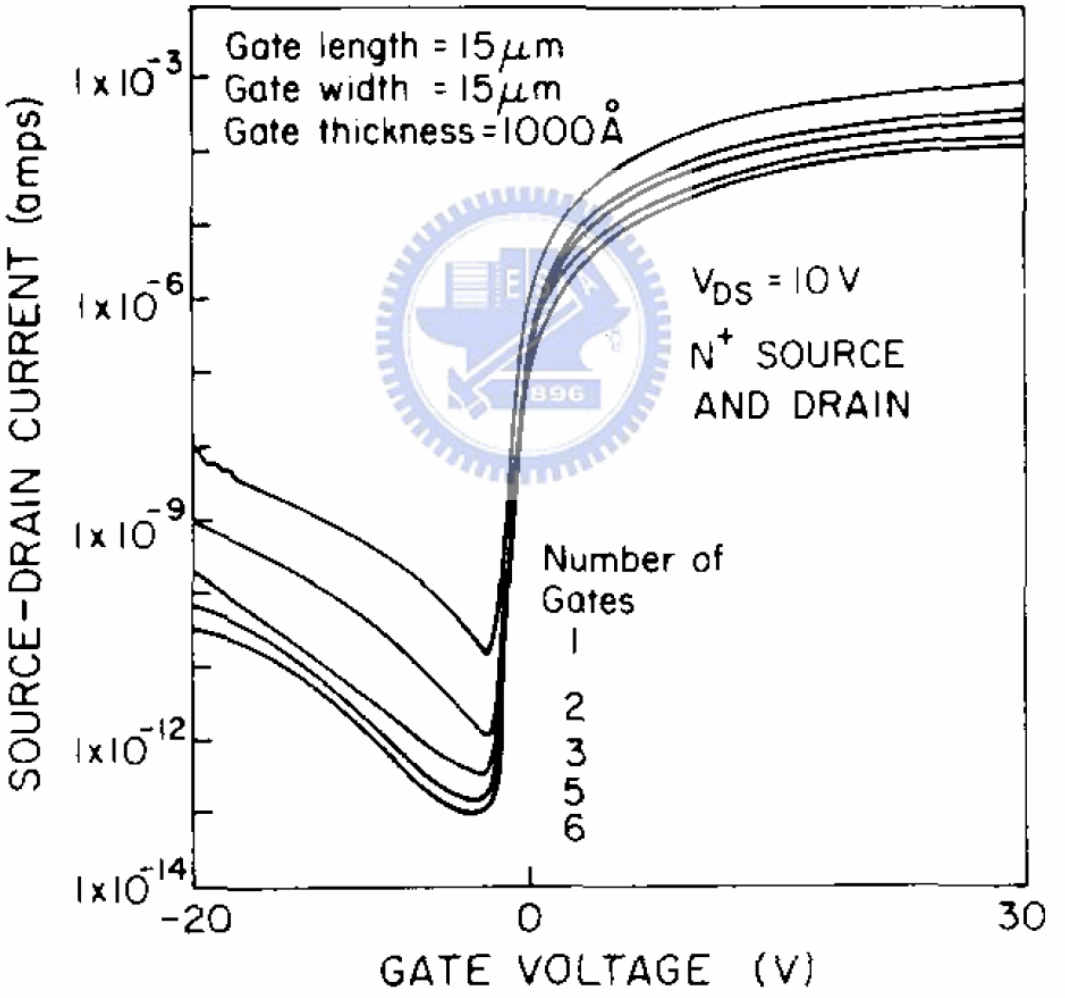


Fig. 2-1-2. I_D-V_G transfer characteristics as V_{DS} = 10 V for TFT's with one, two, three, five, and six gates.

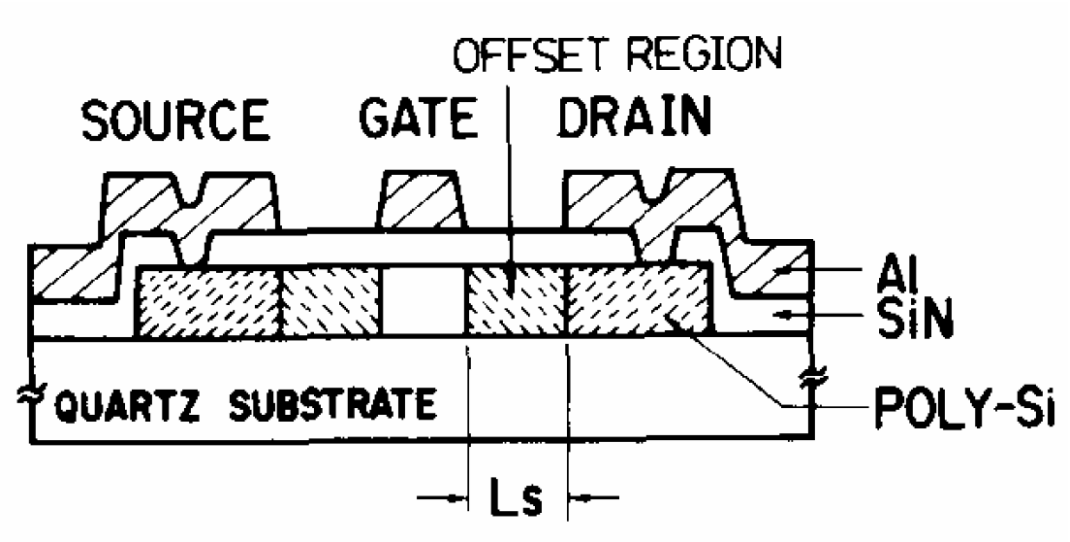


Fig. 2-2-1 Cross section of the offset-gate TFT

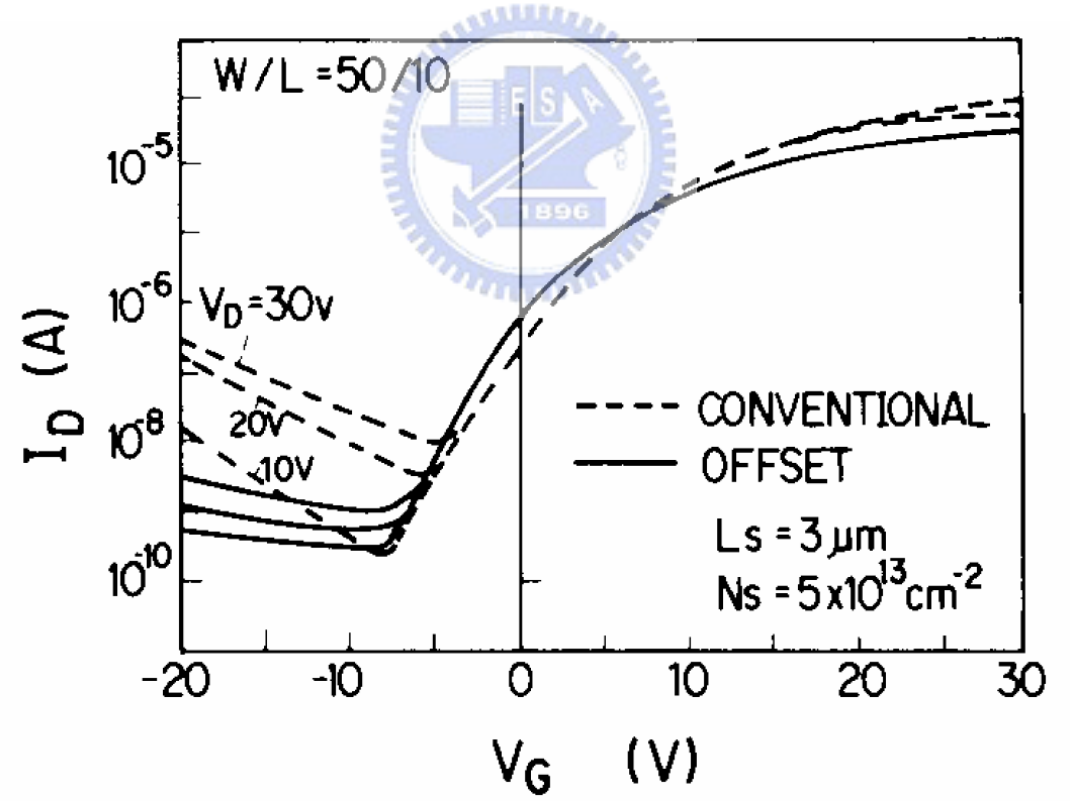


Fig. 2-2-2 I_D versus V_G characteristics of a offset structure TFT and conventional TFT (L / W = 50 μm / 10 μm) for various value of V_D.

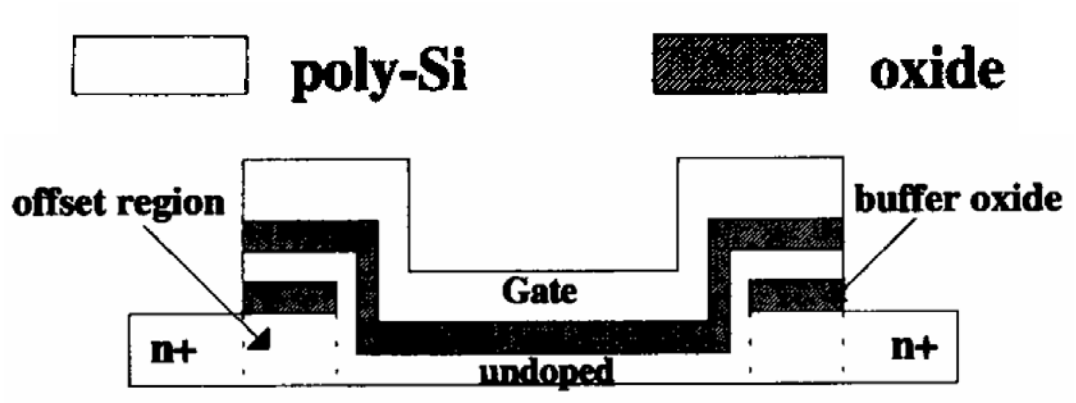


Fig. 2-2-3 Schematic cross-section of the offset gated poly-Si TFT without as additional offset mask

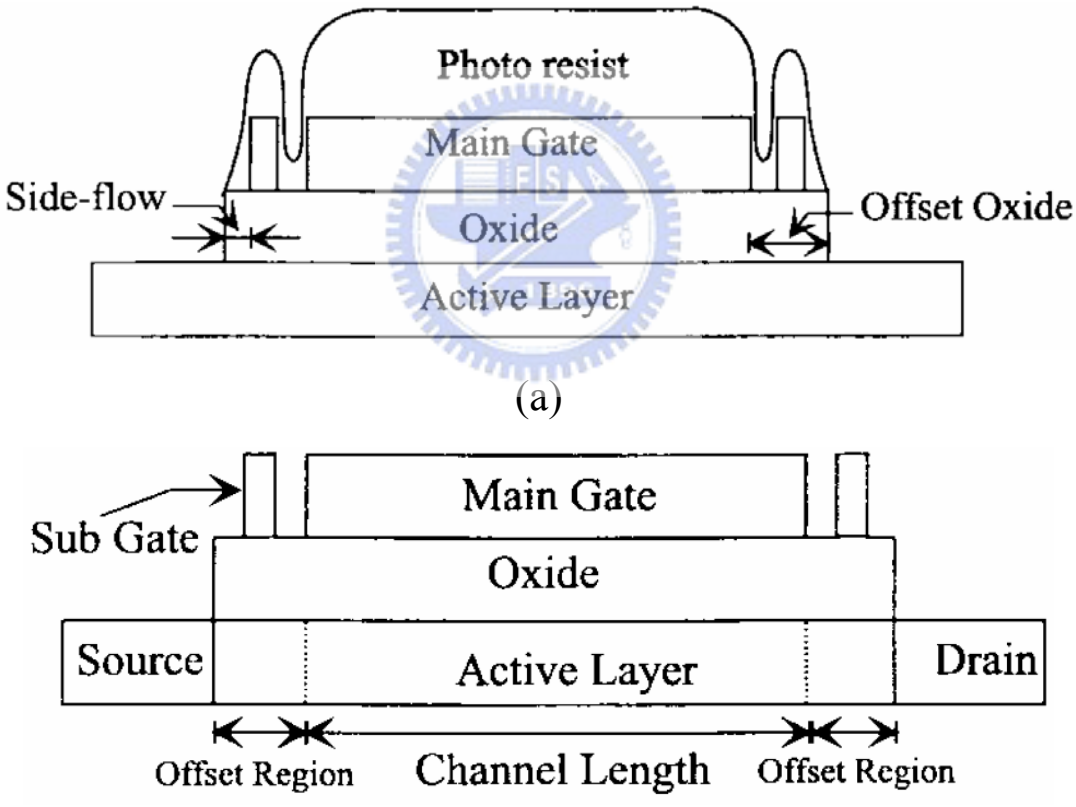


Fig. 2-2-4 Schematic cross-section of the self-aligned offset gated poly-Si TFT.

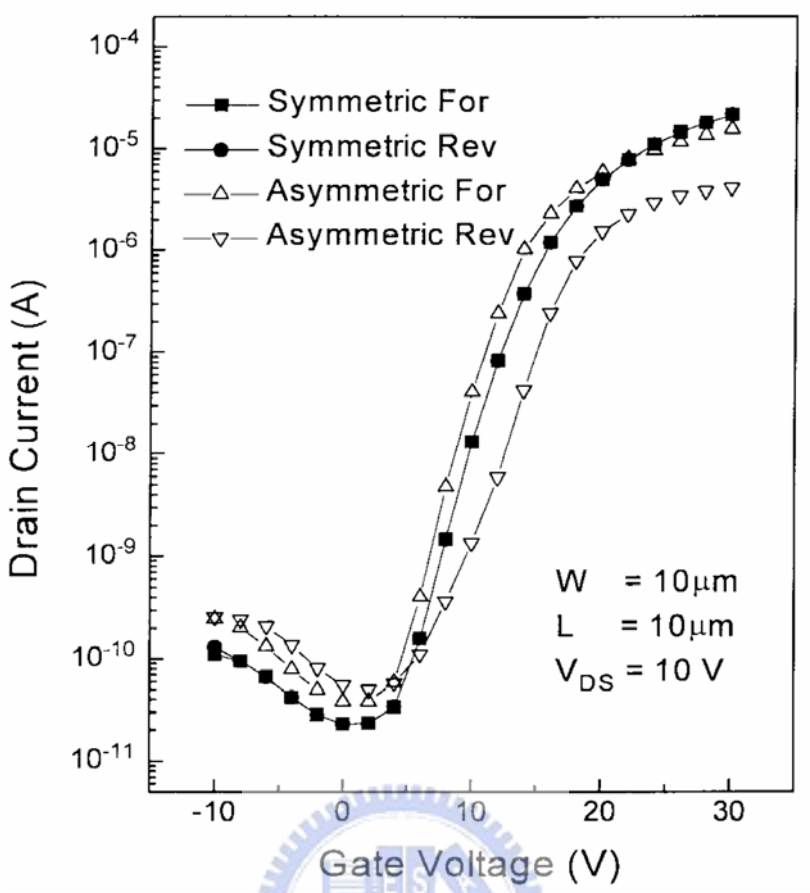


Fig. 2-2-5 The offset lengths of symmetrical device are 1.1 μm and those the asymmetric poly-Si TFT are 1.5 μm and 0.3 μm. Under forward bias the asymmetric poly-Si TFT's offset length at the drain region is 1.5 μm and that at the source region is 0.3 μm.

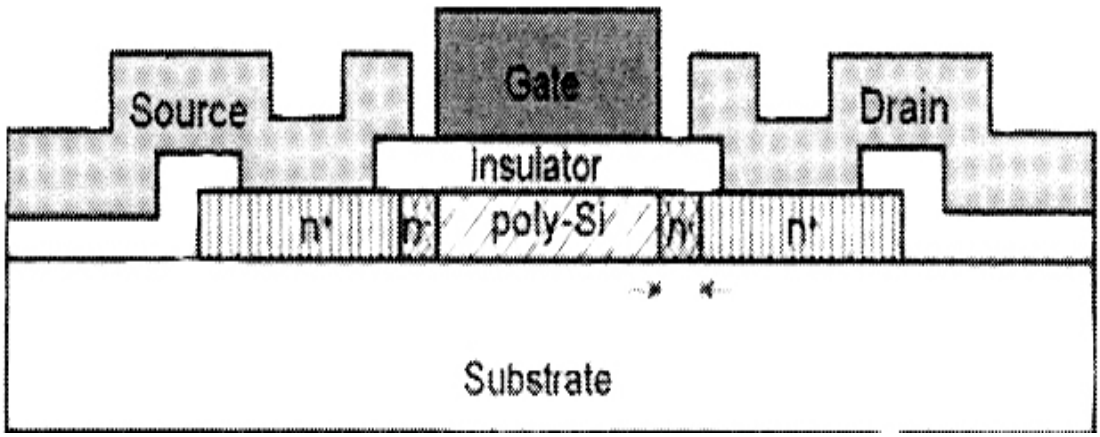
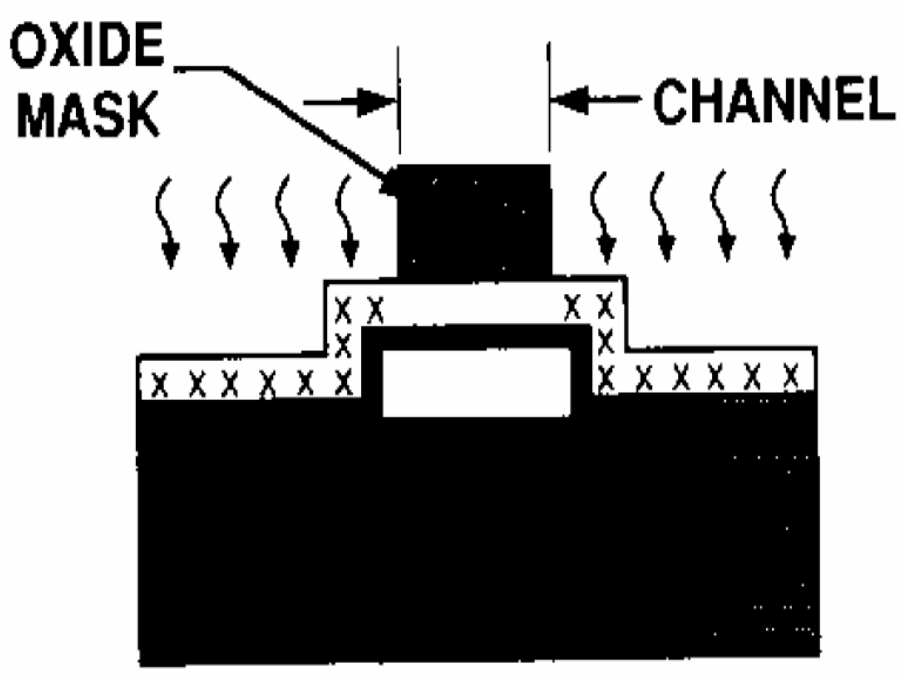
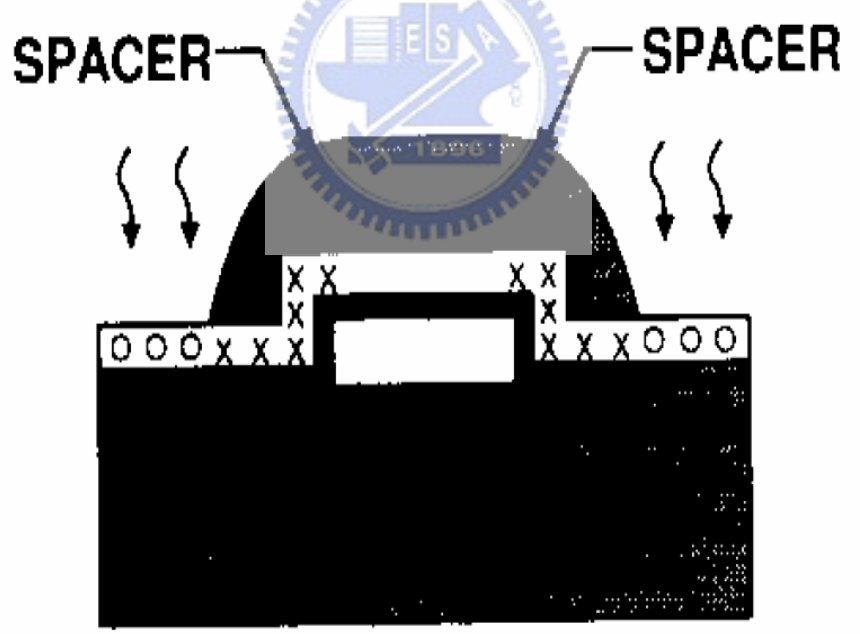


Fig. 2-3-1 Schematic cross-section of top gate, coplanar poly-Si TFT with lightly doped drain region



(a)



(b)

Fig. 2-3-2 The channel area is defined in (a) and is not affected by subsequent processes. The LDD regions are well defined in (b) by the spacers, and are self-aligned to the channel and the source/drain regions.

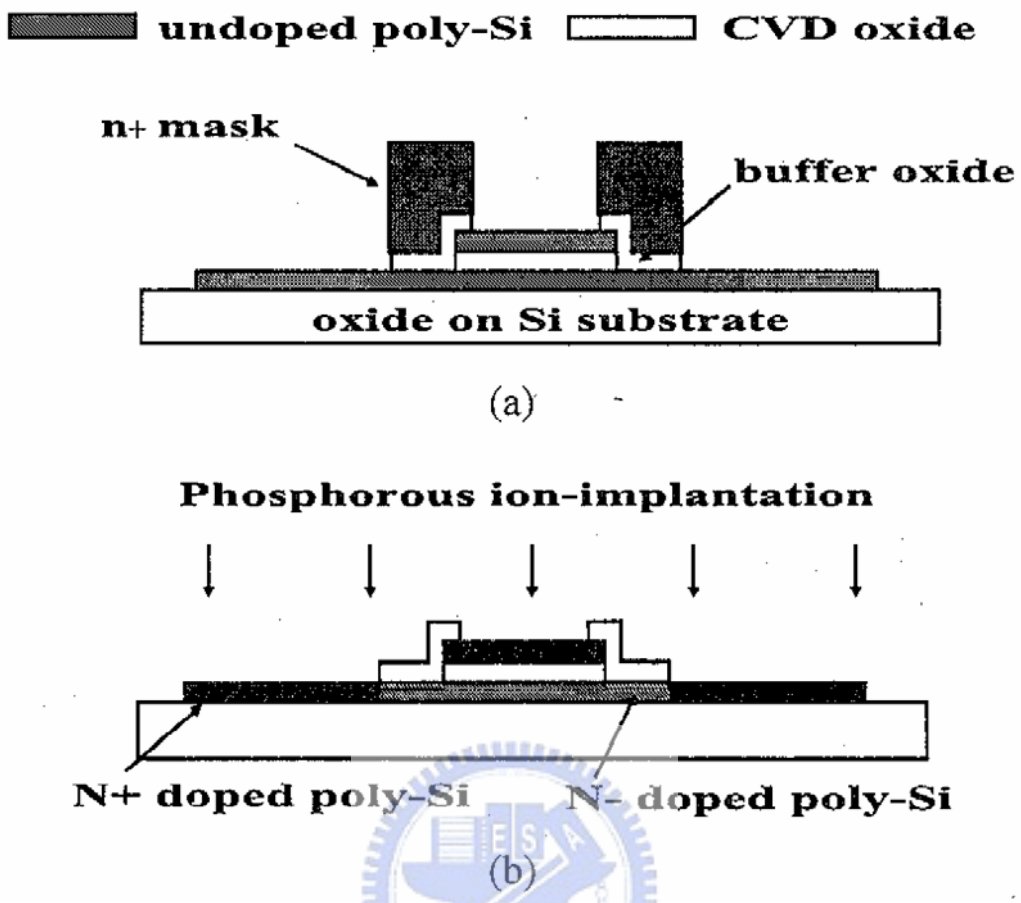


Fig. 2-4-1 Schematic cross-section of GOLDD TFT

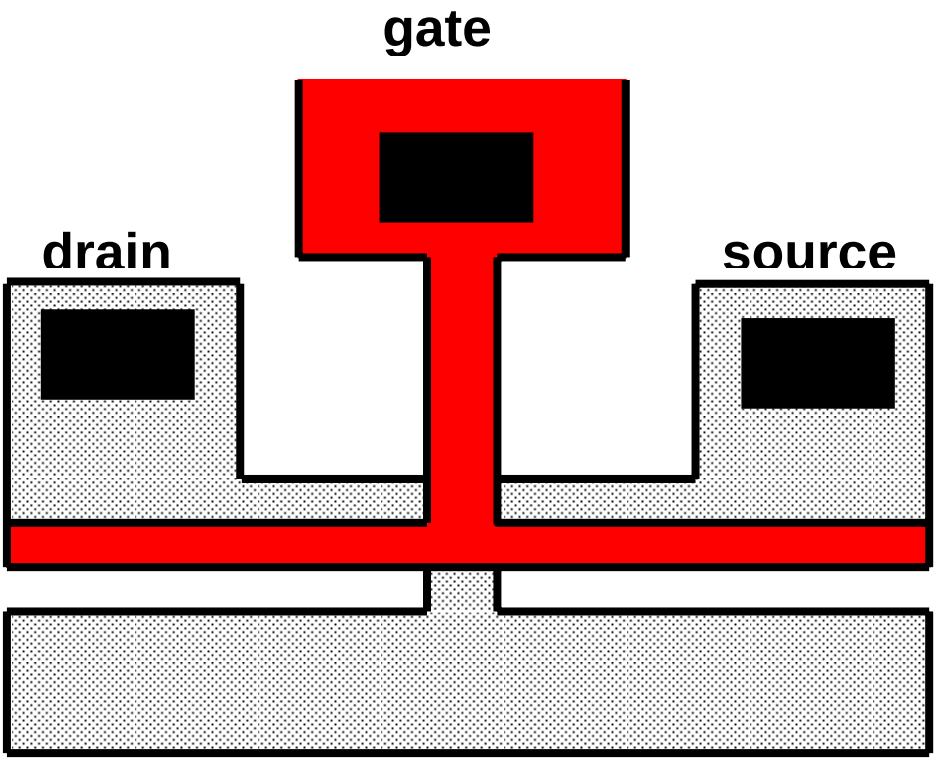


Fig. 3-1-1 The top view of the T-gate poly-Si TFTs.

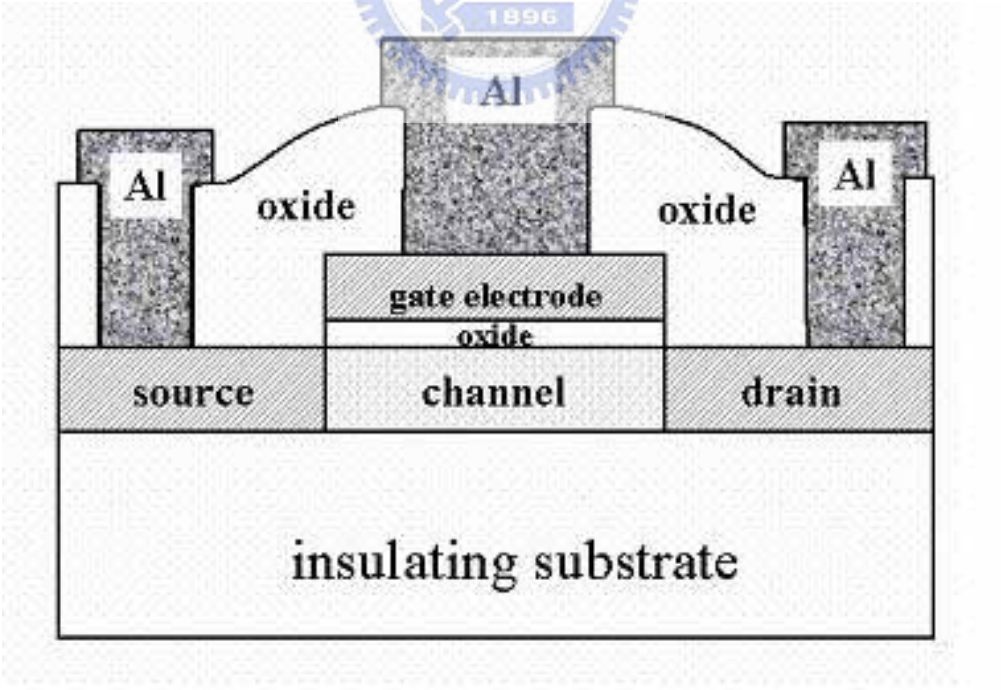


Fig. 3-1-2 Schematic cross sectional view of devices with conventional top-gate structure.

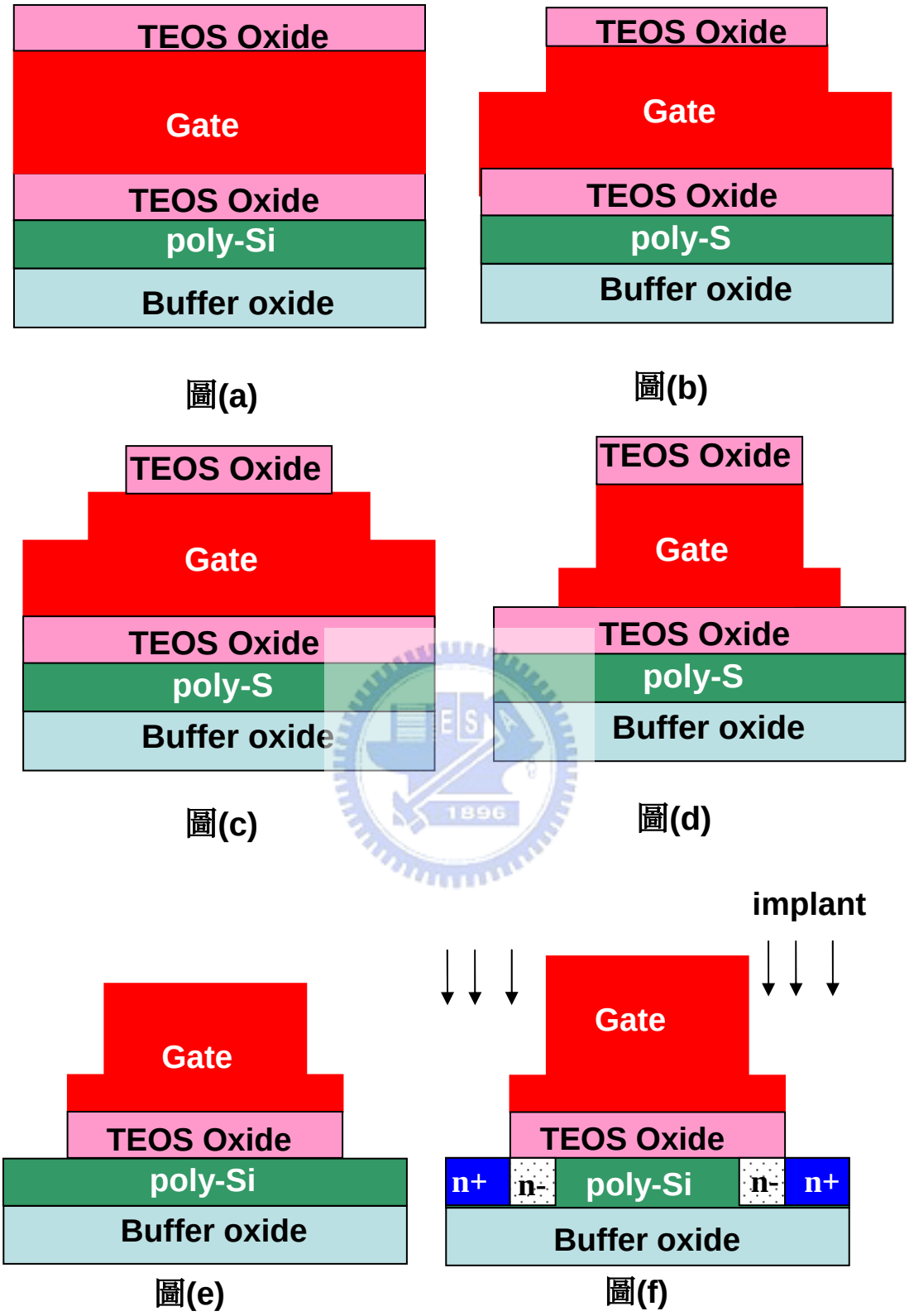
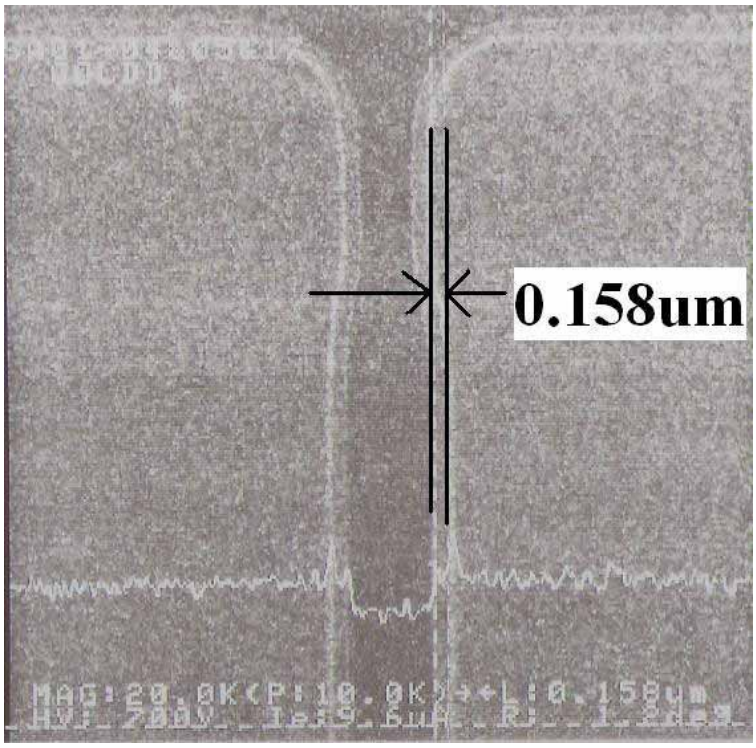
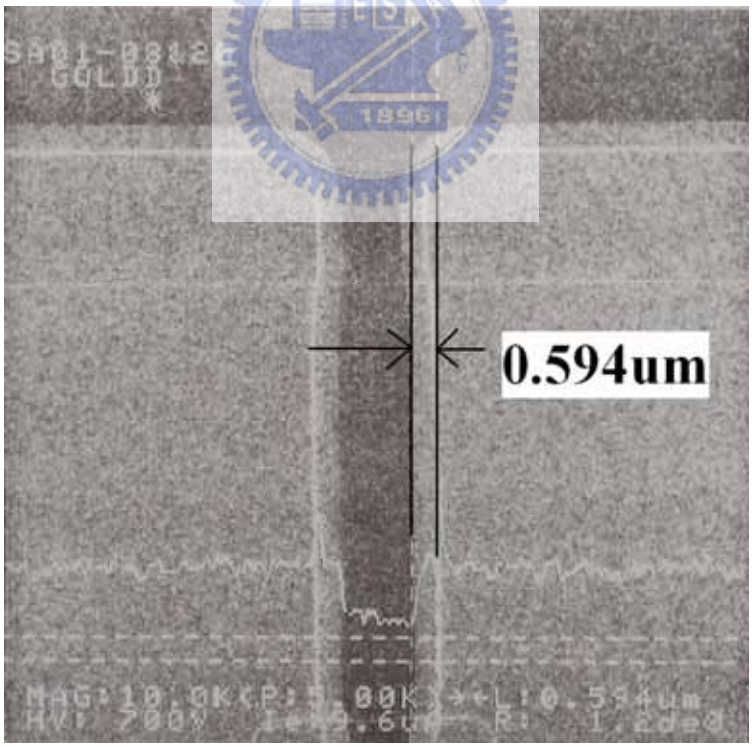


Fig. 3-1-3 The fabrication process (a) deposited to the second TEOS layer. (b) used gate mask to define this TEOS layer. (c) side etch the TEOS. (d) formed the raised structure (e) remove oxide about the source and drain. (f) implant to form the n^+ source and drain regions and n^- regions.



(a)



(b)

Fig. 3-1-4 In-line SEM picture (a) short LDD length, (b) long LDD length.

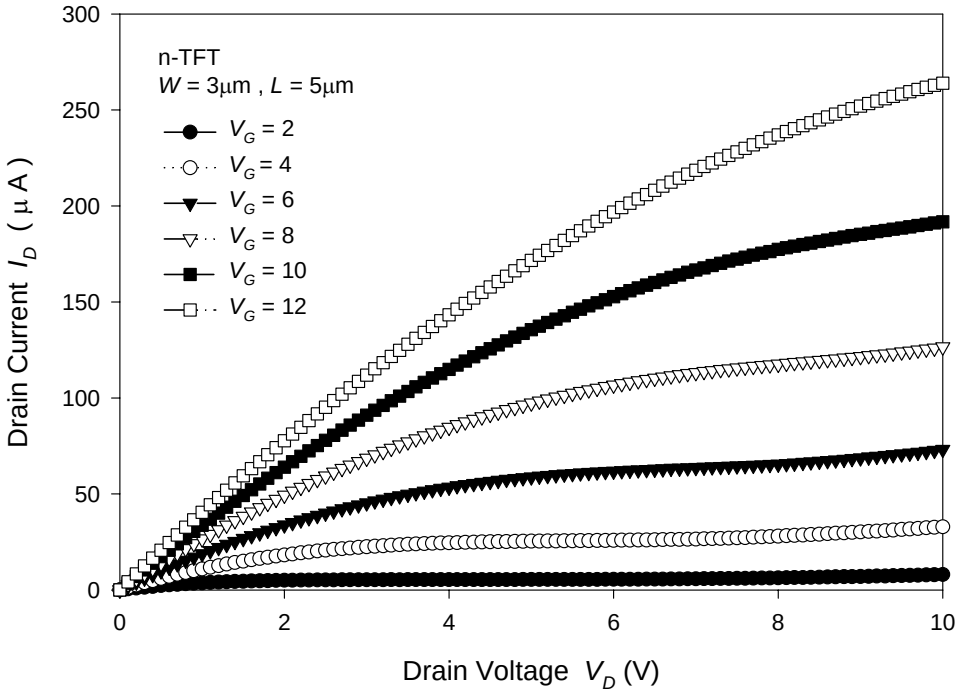


Fig. 3-2-1. The I_D-V_D characteristics of the ploy-Si TFTs.

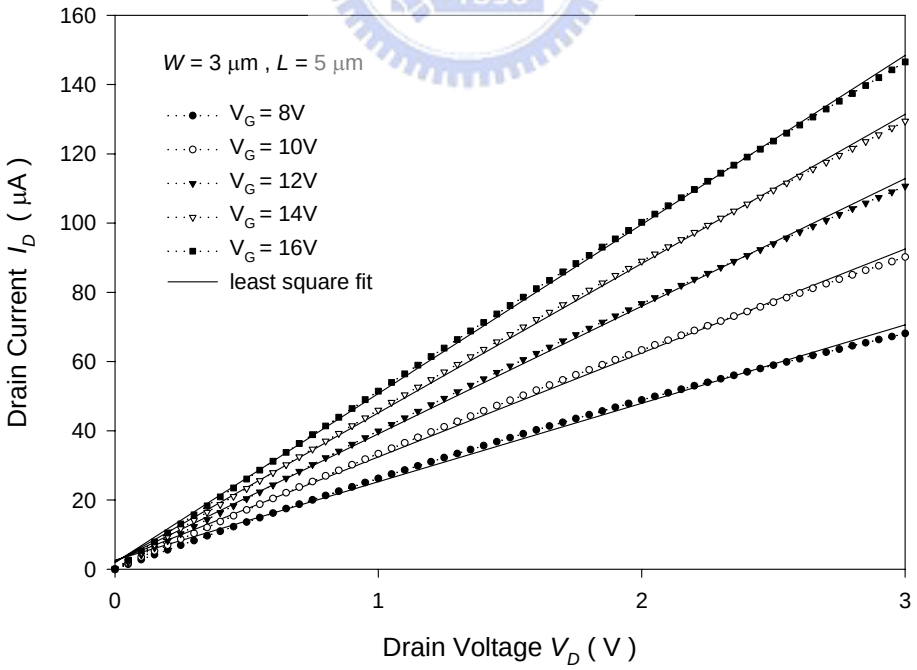


Fig. 3-2-2. An example of ON resistance measurement in the linear regions of the ploy-Si TFT output characteristics.

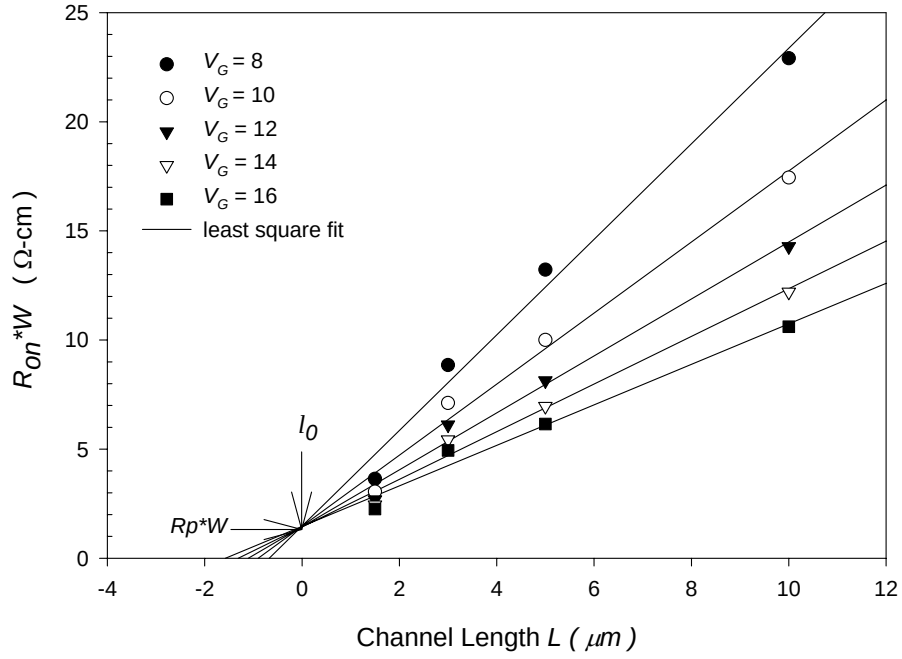


Fig. 3-2-3. Width -normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data .The channel width of these devices is fixed at 3 μ m.

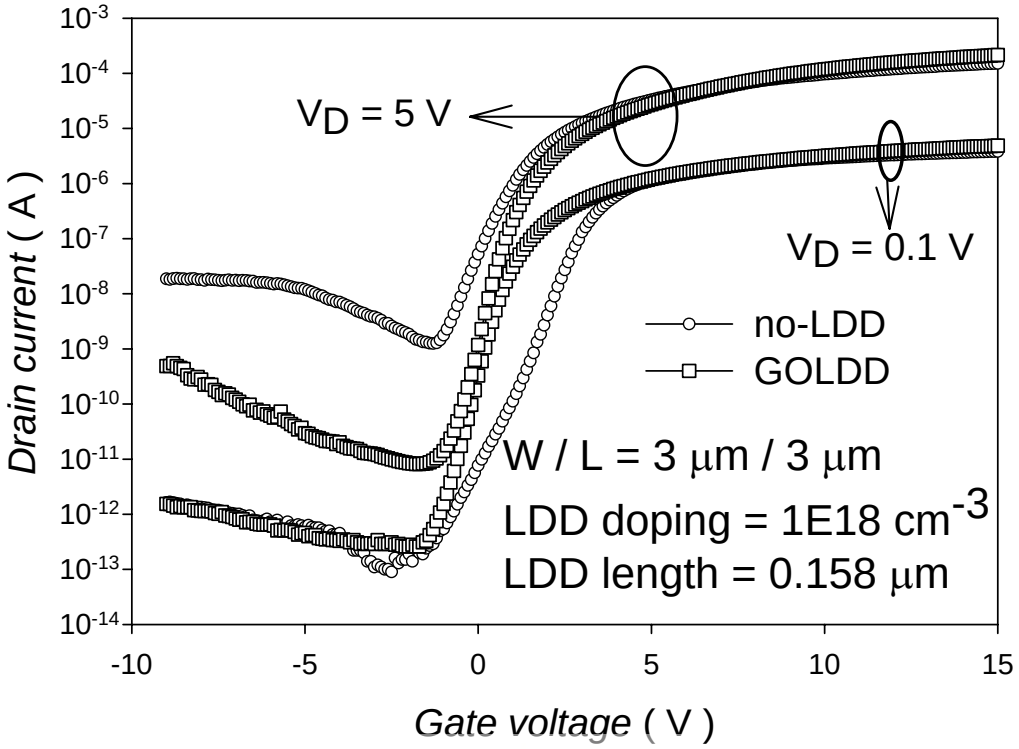
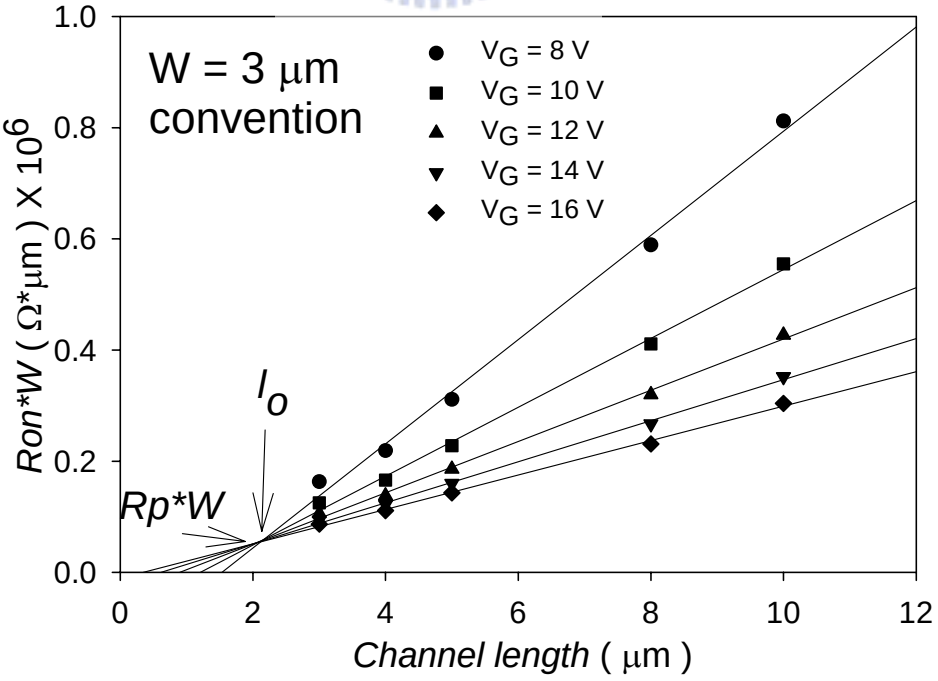
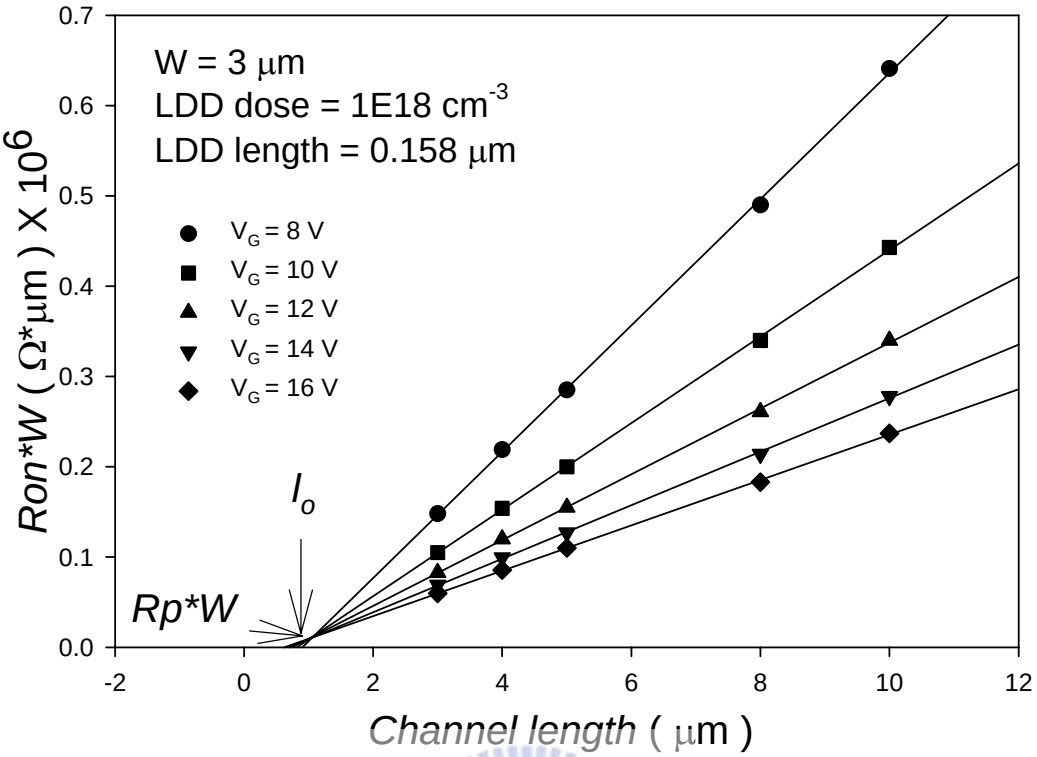


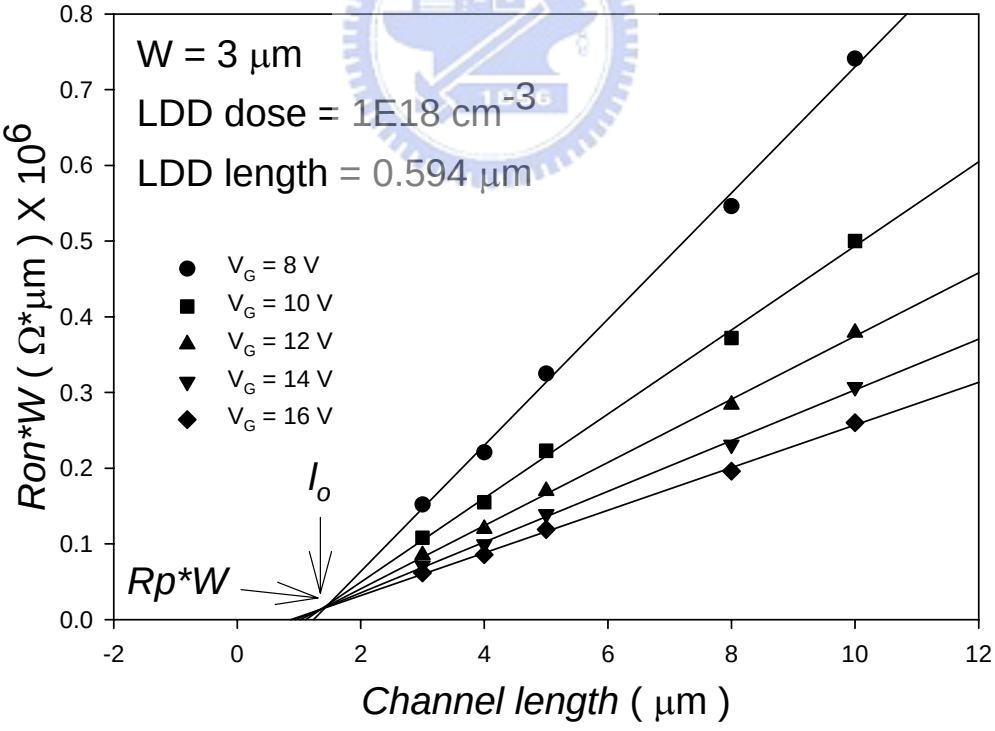
Fig. 4-1-1 I_D versus V_G characteristic of non-LDD TFT and GOLDD TFT.



(a)



(b)



(c)

Fig. 4-1-2 Width -normalized ON resistance as a function of channel length at different gate voltages. The solid lines represent the linear least square fit of the data.：(a) conventional TFT, (b) LDD length is 0.158 μm, (c) LDD length is 0.594 μm.

$l_o > 0$

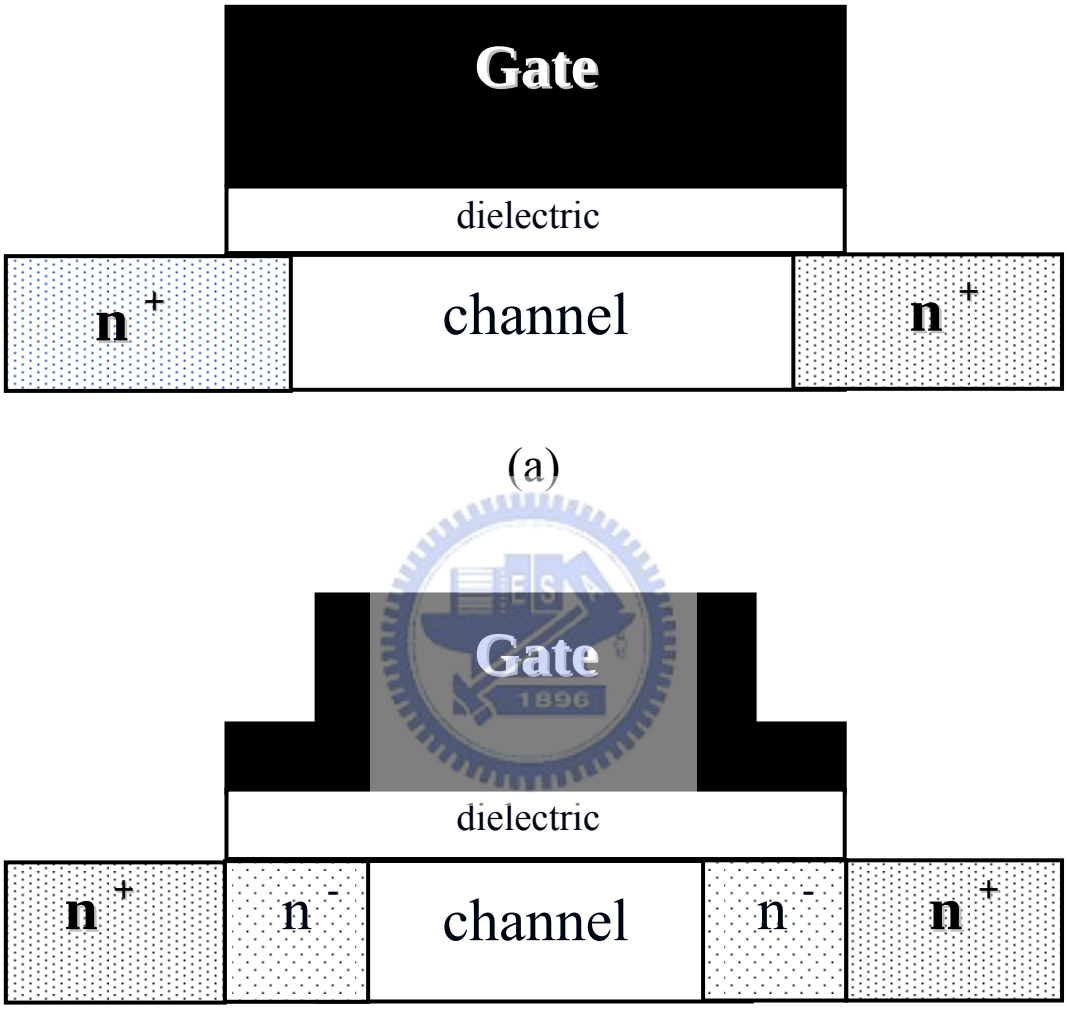
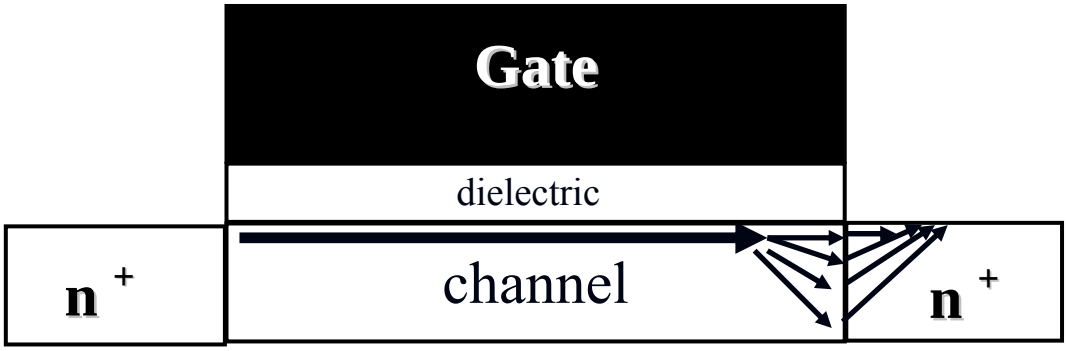
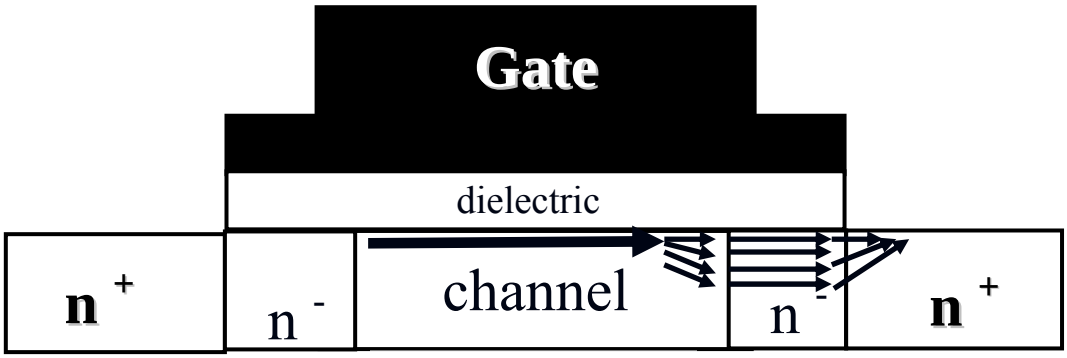


Fig. 4-1-3 The dopant redistribution for (a) conventional TFTs, (b) GOLDD TFTs.



(a)



(b)

Fig. 4-1-4 The current path for (a) conventional TFTs, (b) GOLDD TFTs.

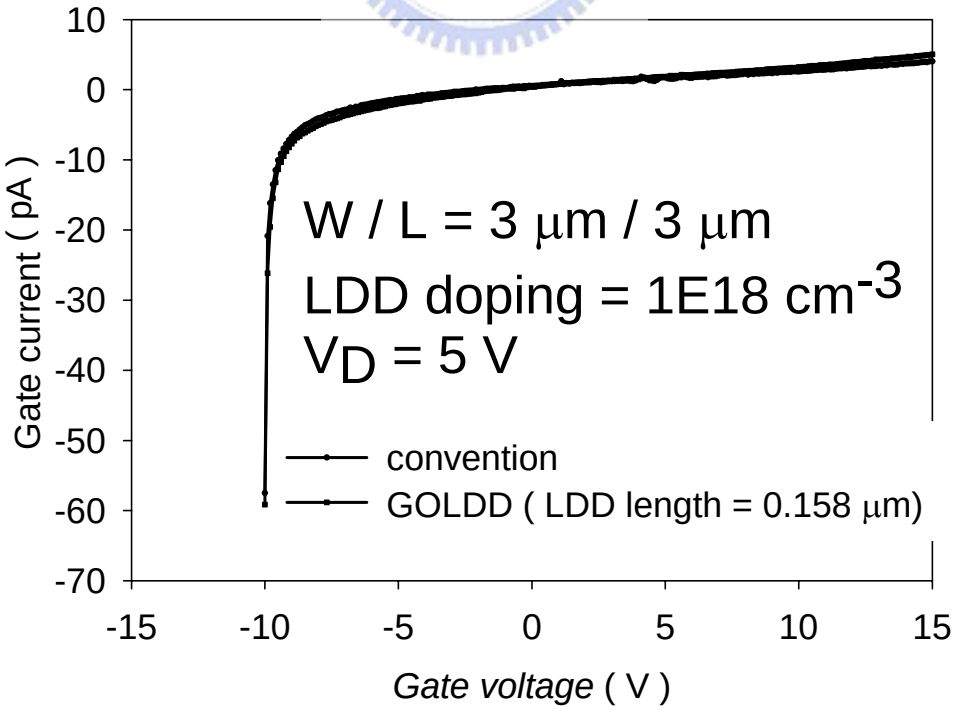


Fig. 4-1-5 I_G versus V_D characteristic of non-LDD TFT and GOLDD TFT.

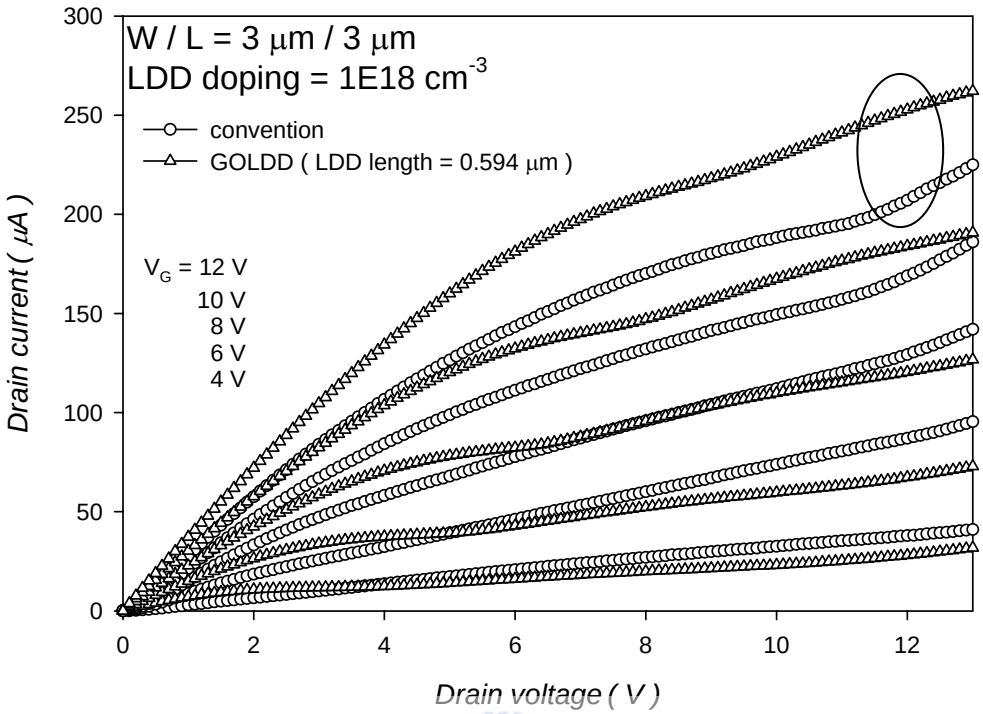


Fig. 4-2-1 I_D versus V_D characteristic of conventional TFT and GOLDD TFT.

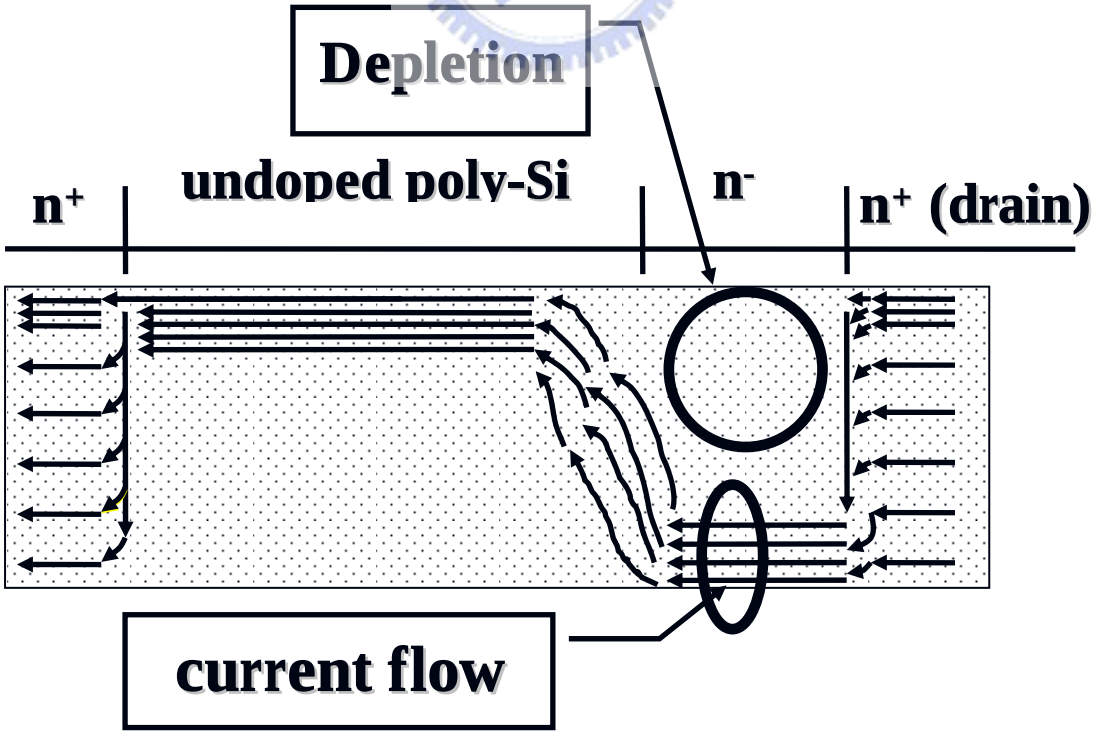
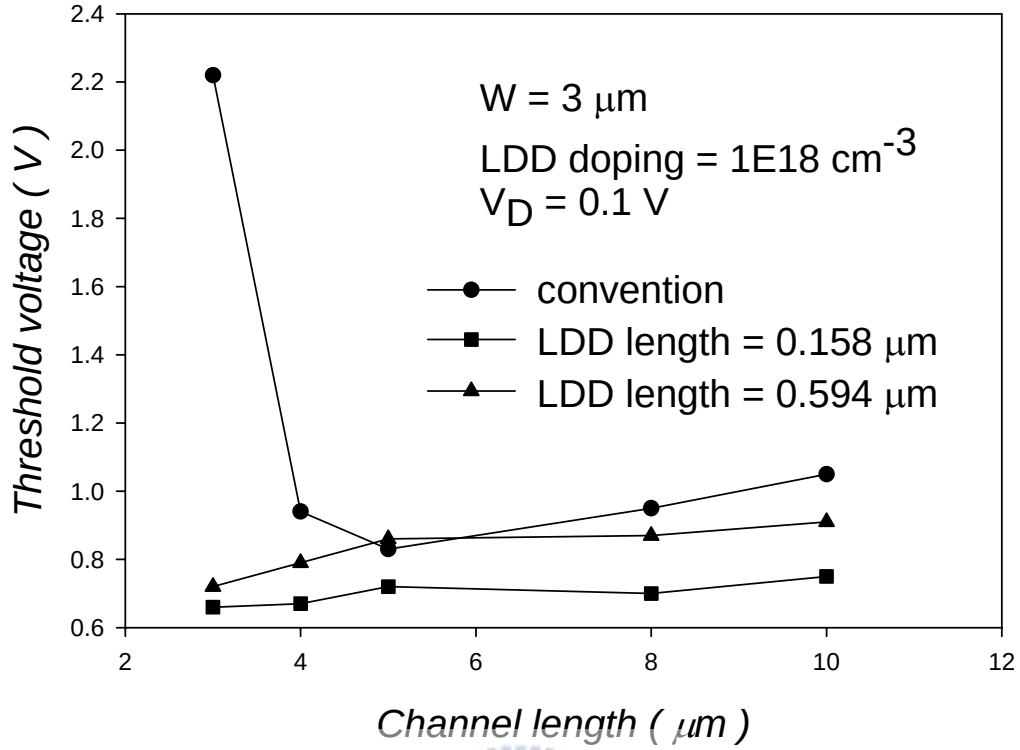
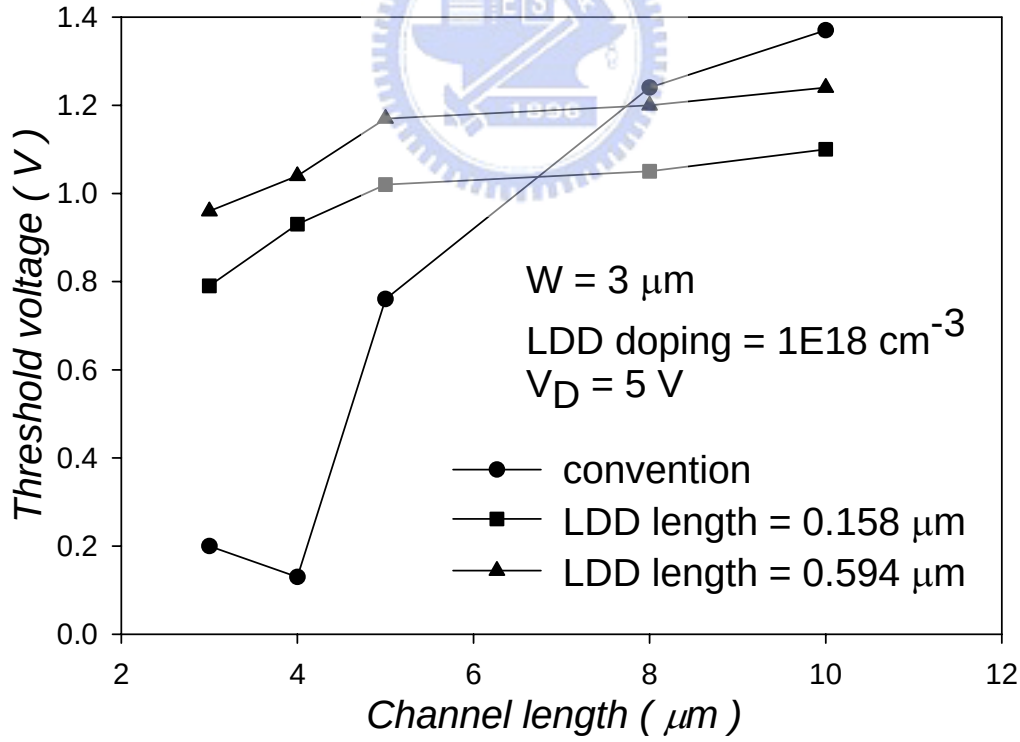


Fig. 4-2-2 The electron current path.

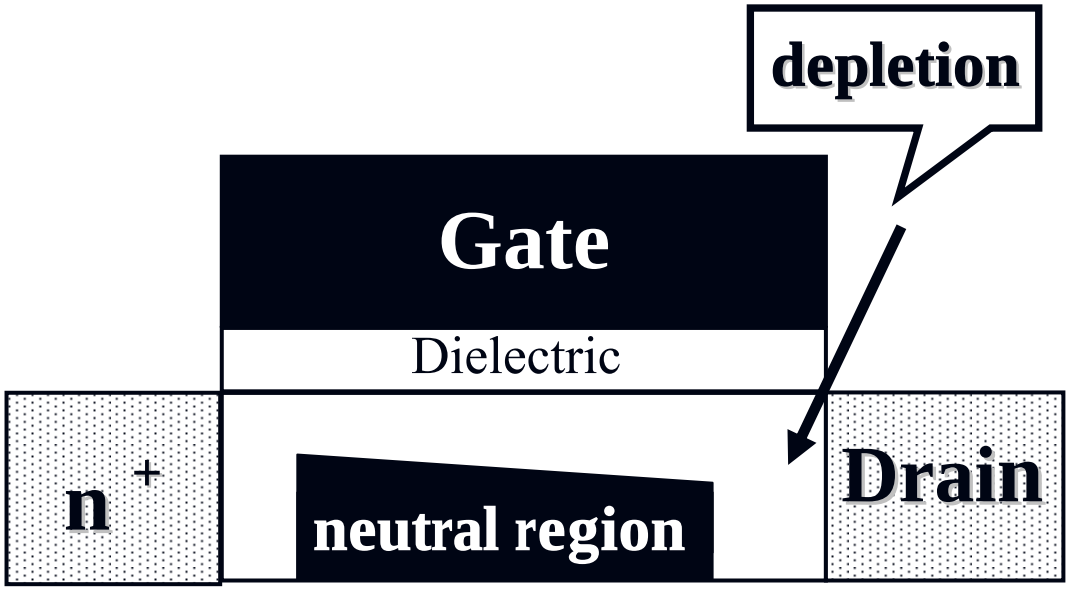


(a)

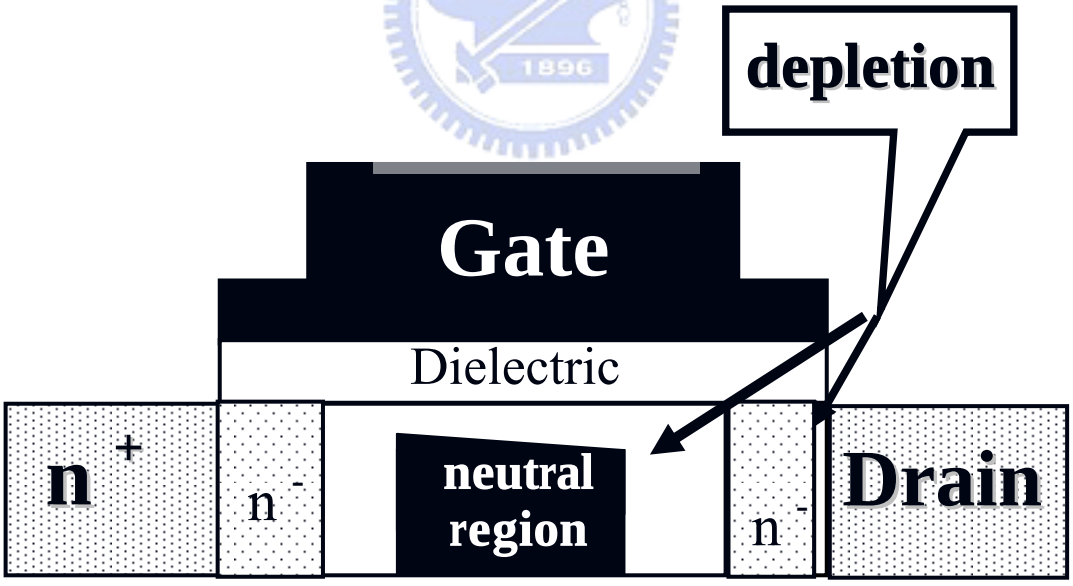


(b)

Fig. 4-2-3 The V_{th}-L characteristics for conventional and GOLDD TFTs：(a) V_D = 0.1 V, (b) V_D =5 V.



(a)



(b)

Fig. 4-2-4 The charge share characteristics for (a) conventional TFTs, (b) GOLDD TFTs.

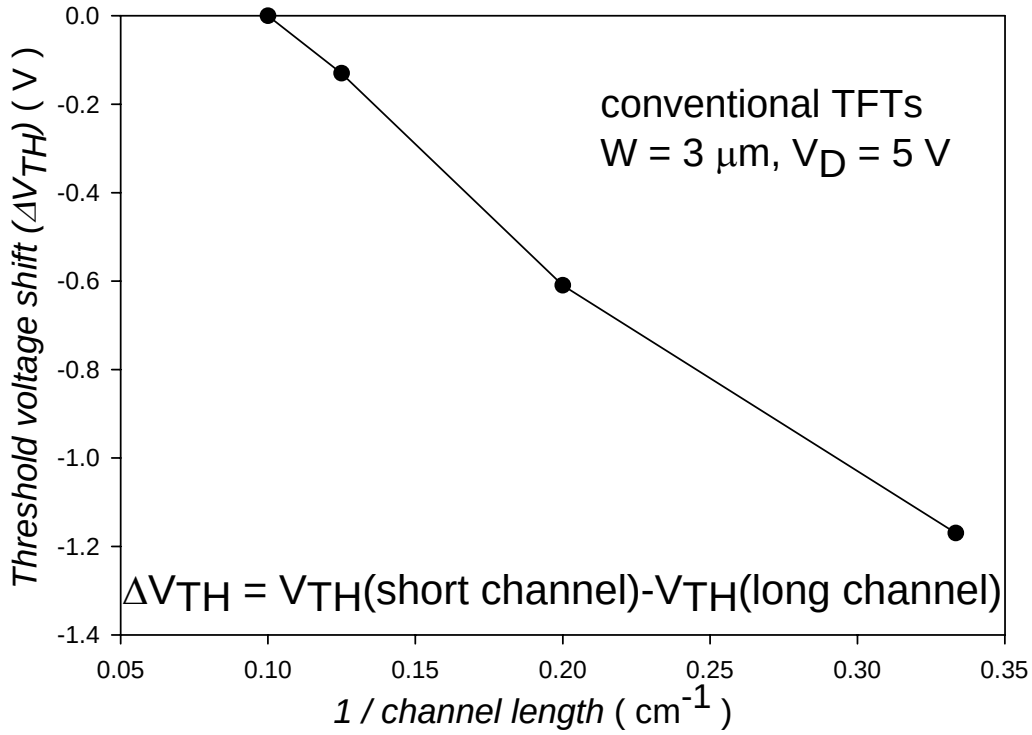


Fig. 4-2-5 The $\triangle V_{th}$-L^{-1} characteristics for conventional TFTs.

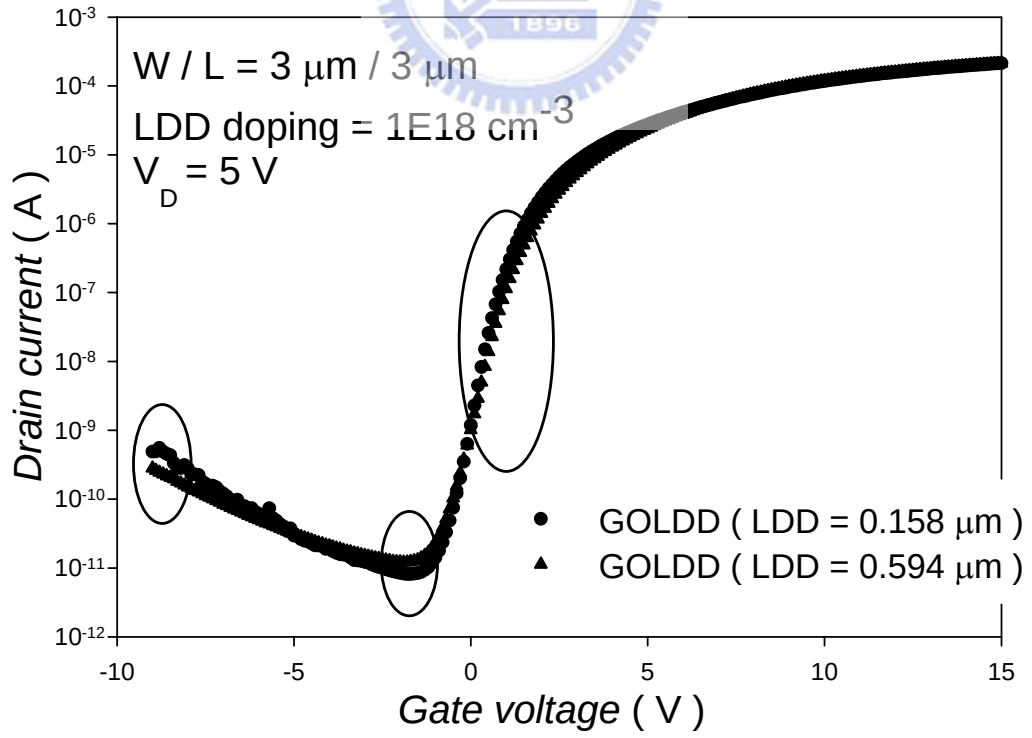
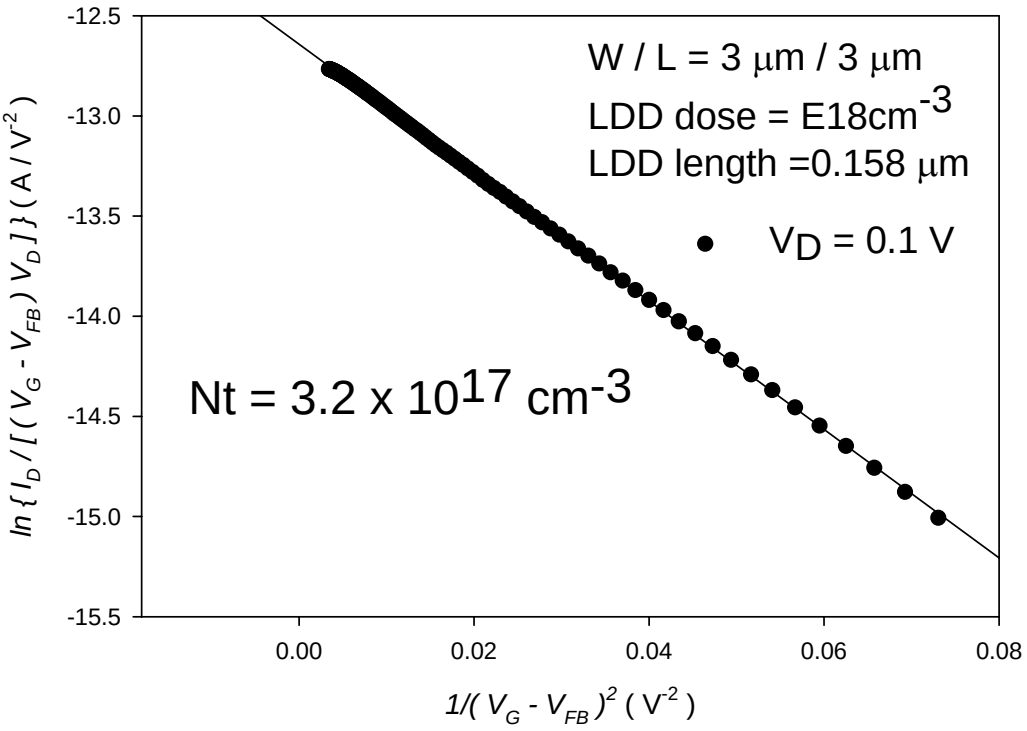
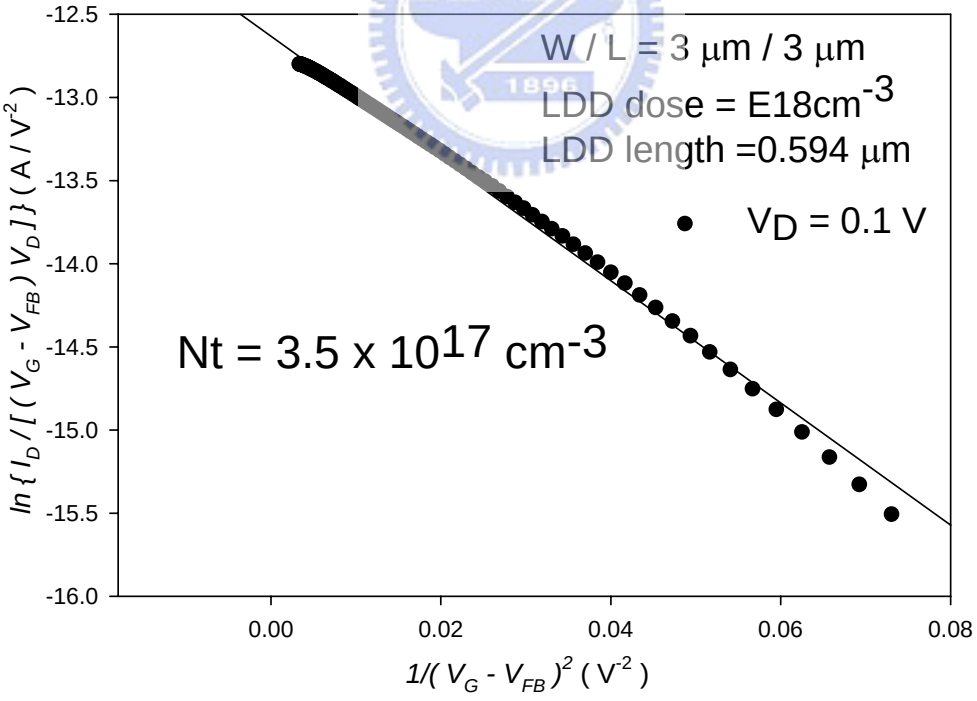


Fig. 4-2-6 The I_D-V_G characteristics for different LDD length in the GOLDD TFTs.



(a)



(b)

Fig. 4-2-7 Plotting of ln〔 $I_D / (V_G - V_{FB}) V_D$ 〕versus $(V_G - V_{FB})^{-2}$.

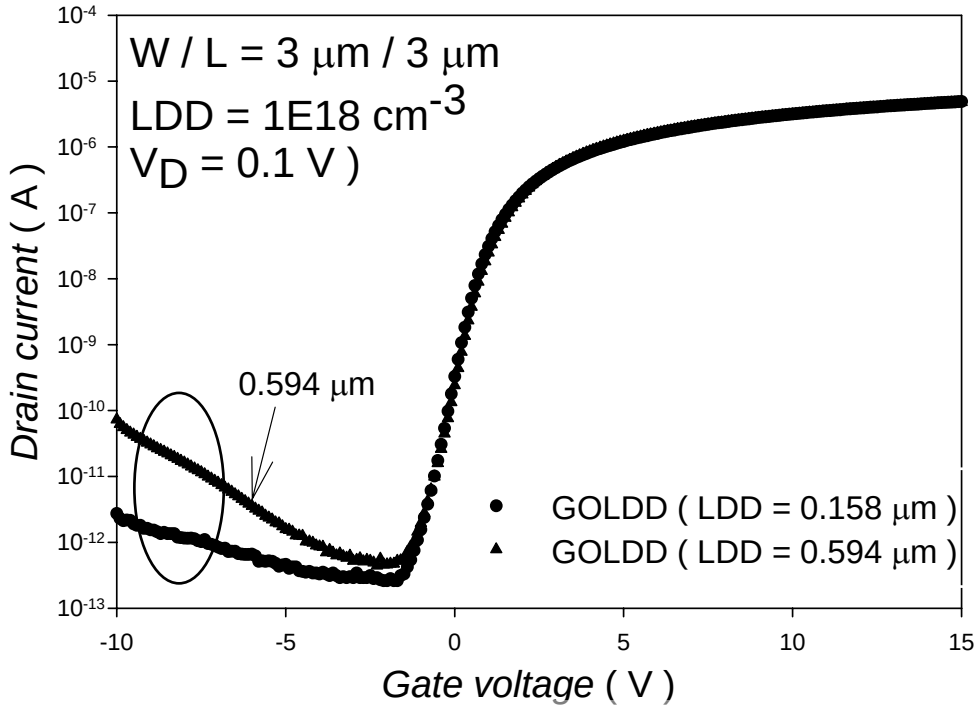


Fig. 4-2-8 The I_D-V_G characteristics for different LDD length in the GOLDD TFTs.

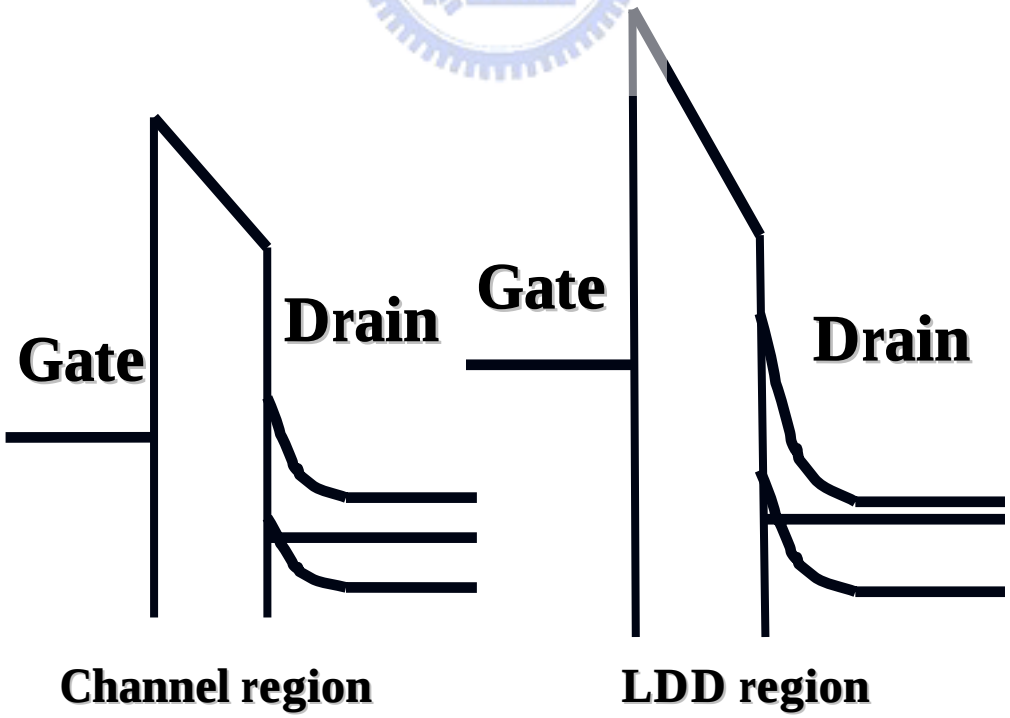


Fig. 4-2-9 The energy band for channel and LDD region at V_D = 0.1 V and V_G = -10 V.

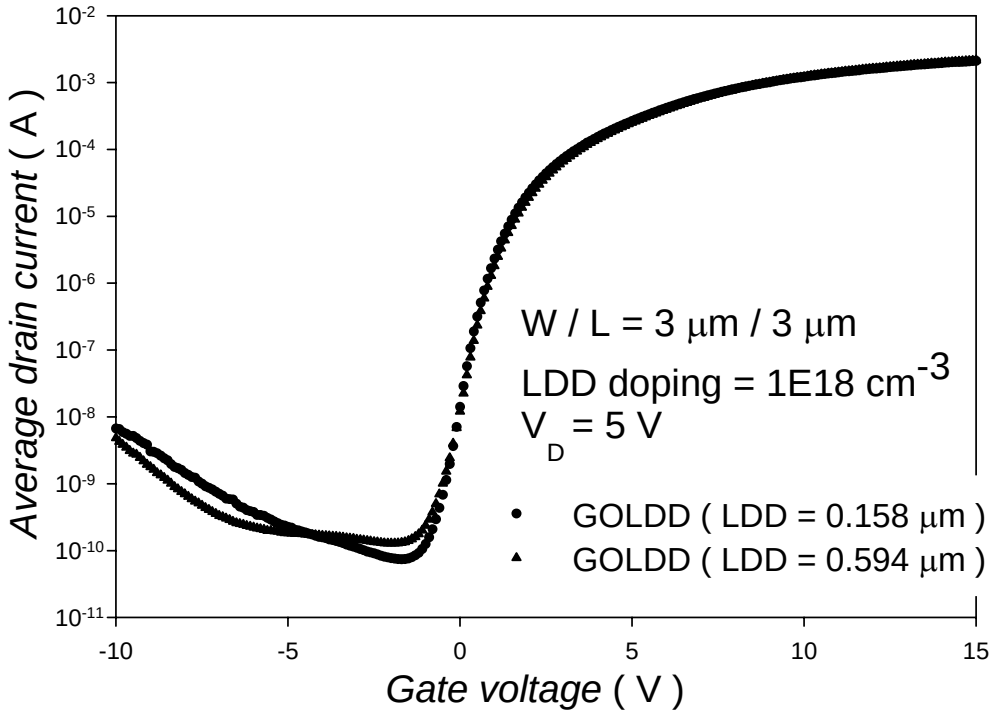


Fig. 4-2-10 The average I_D-V_G characteristics for different LDD length in the GOLDD TFTs.

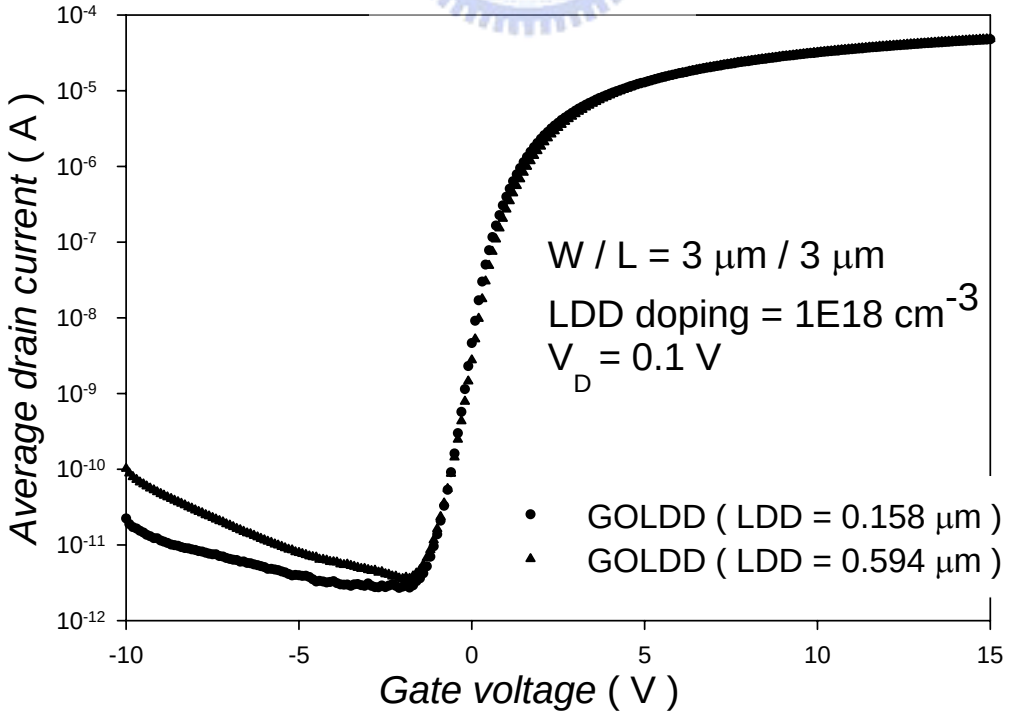
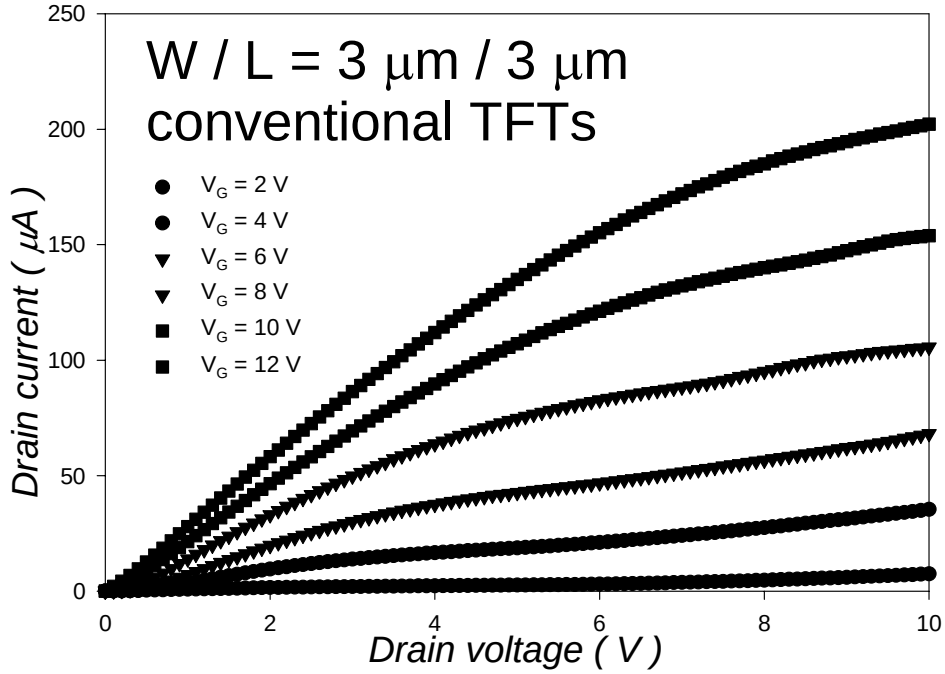
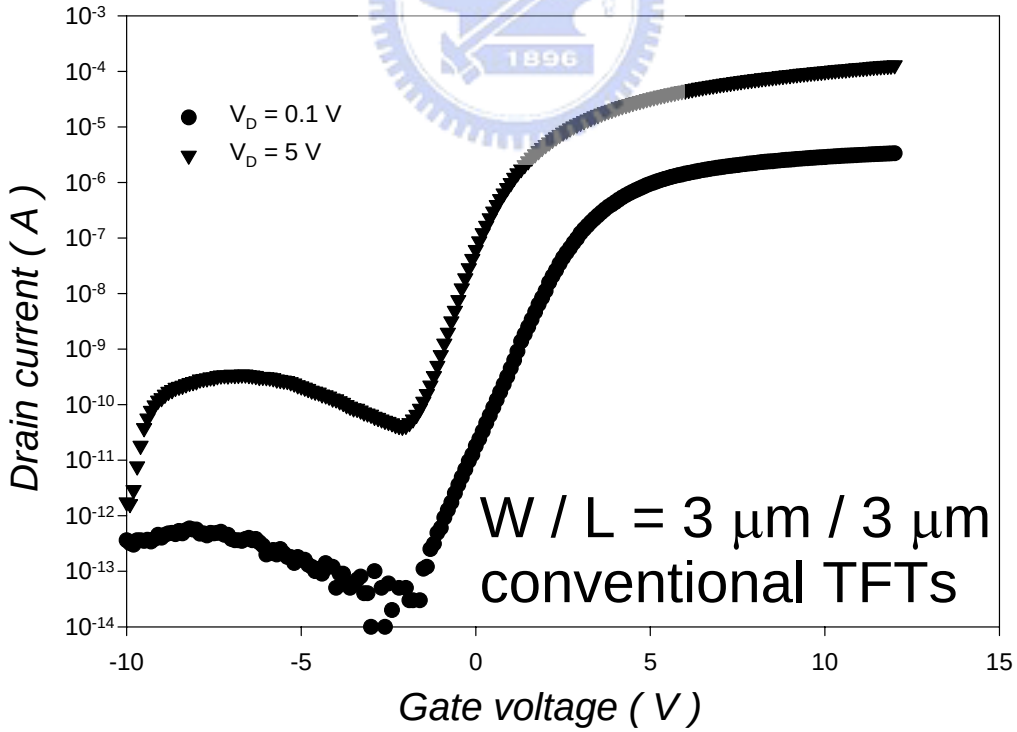


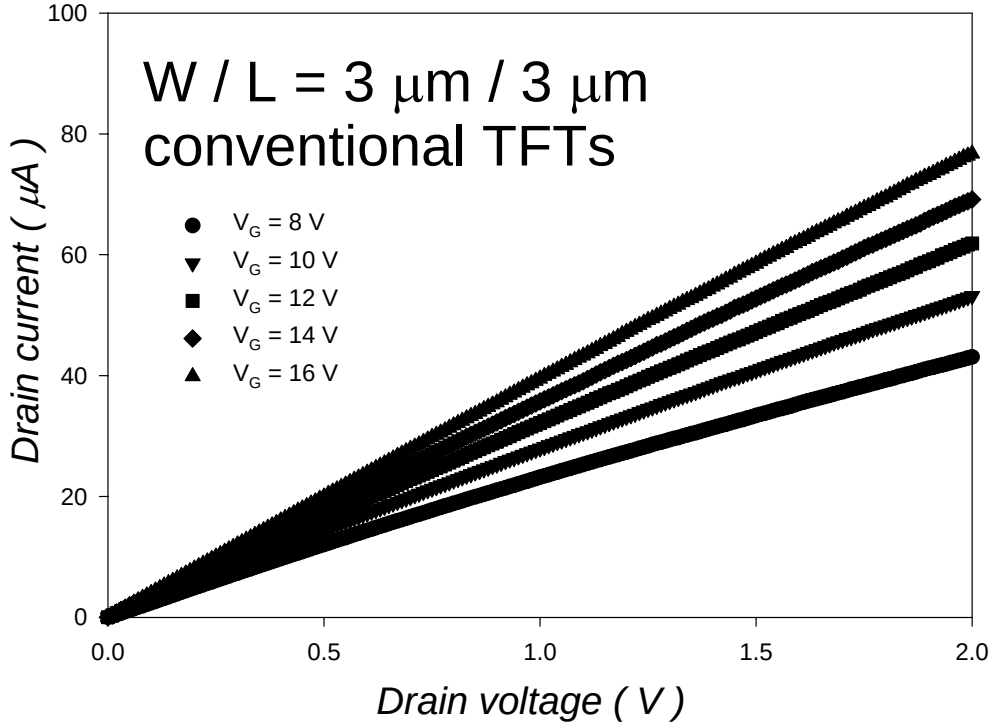
Fig. 4-2-11 The average I_D-V_G characteristics for different LDD length in the GOLDD TFTs.


W / L = 3 μm / 3 μm
conventional TFTs
V_G = 2 V
V_G = 4 V
V_G = 6 V
V_G = 8 V
V_G = 10 V
V_G = 12 V
Drain current (μA)
Drain voltage (V)
0
50
100
150
200
250
0
2
4
6
8
10

(a)

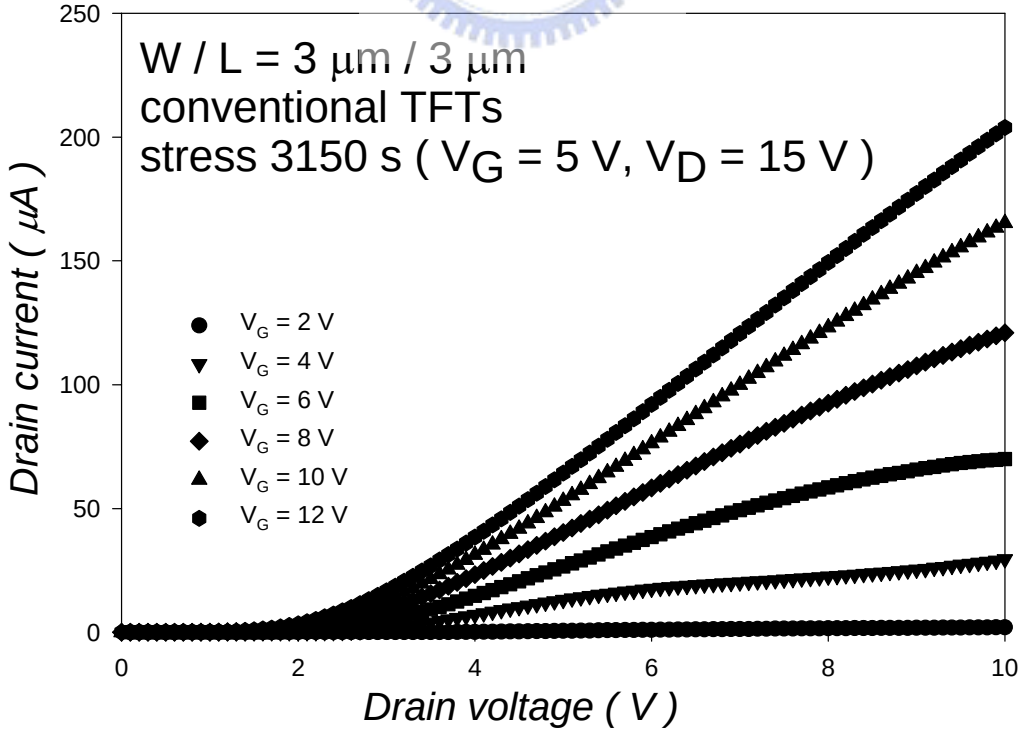

V_D = 0.1 V
V_D = 5 V
W / L = 3 μm / 3 μm
conventional TFTs
Drain current (A)
Gate voltage (V)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
-10
-5
0
5
10
15

(b)

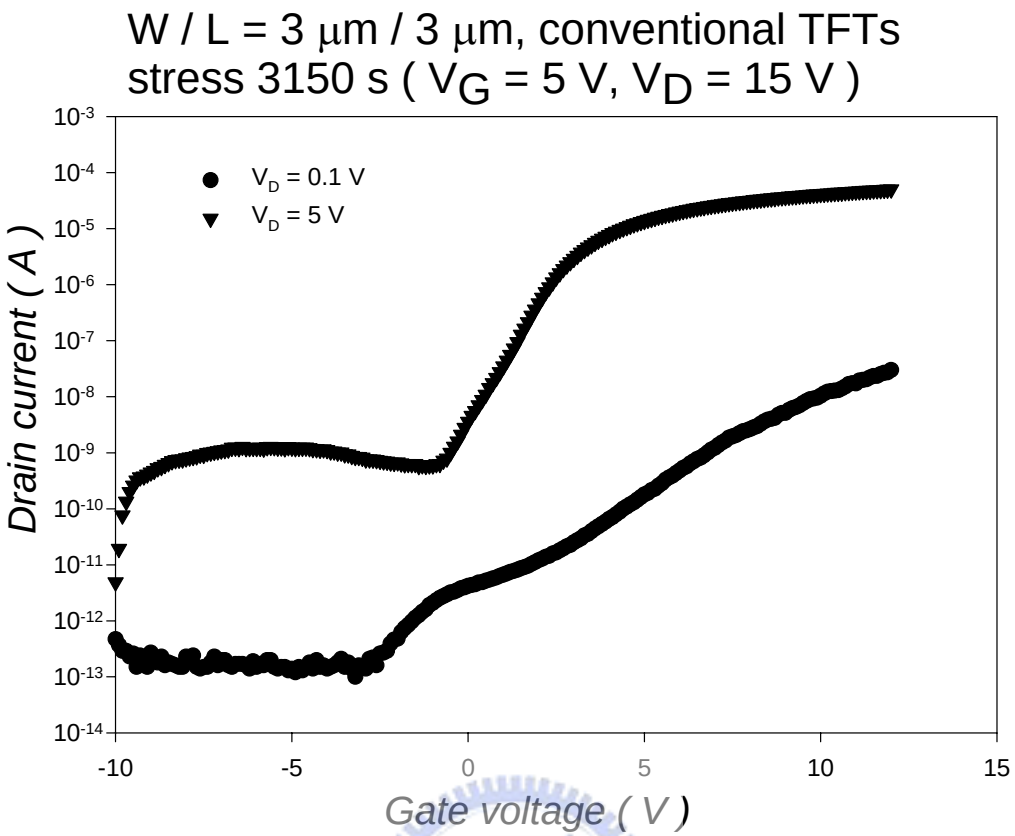


(c)

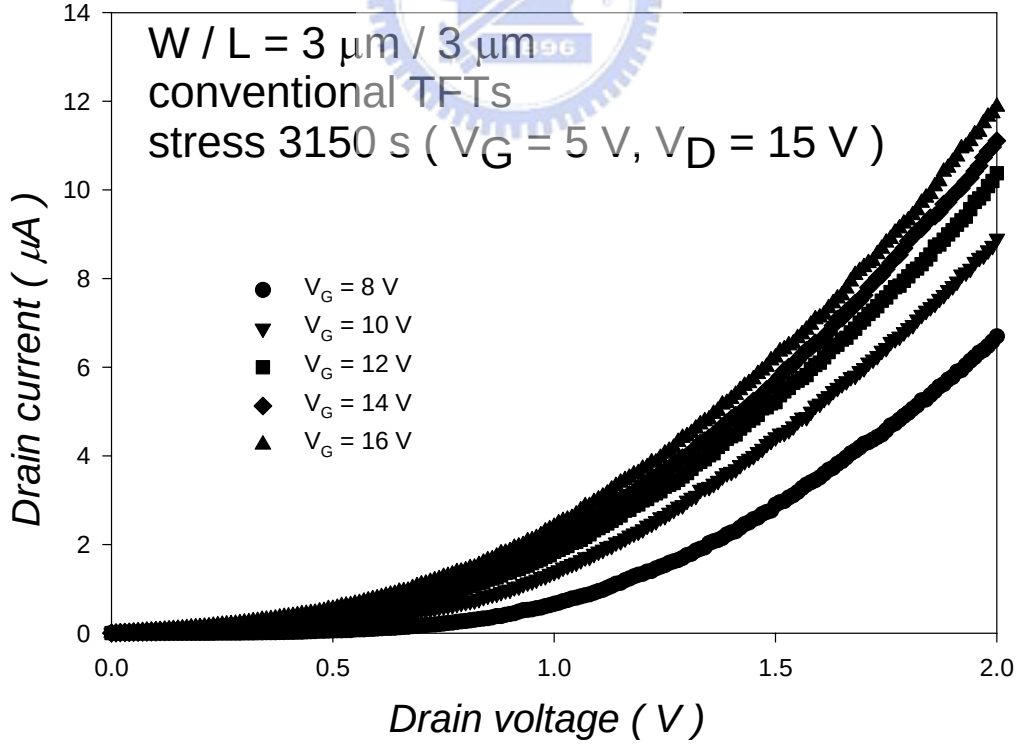
Fig. 4-3-1 The typical characteristics for conventional TFTs : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.



(a)

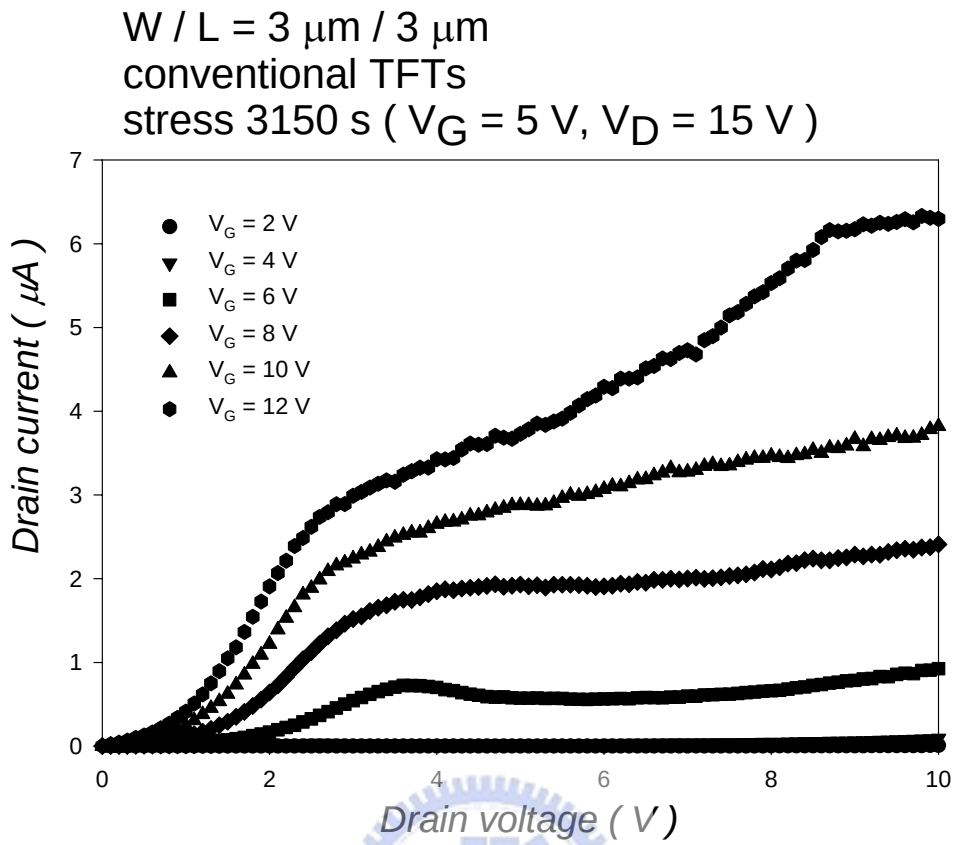


(b)

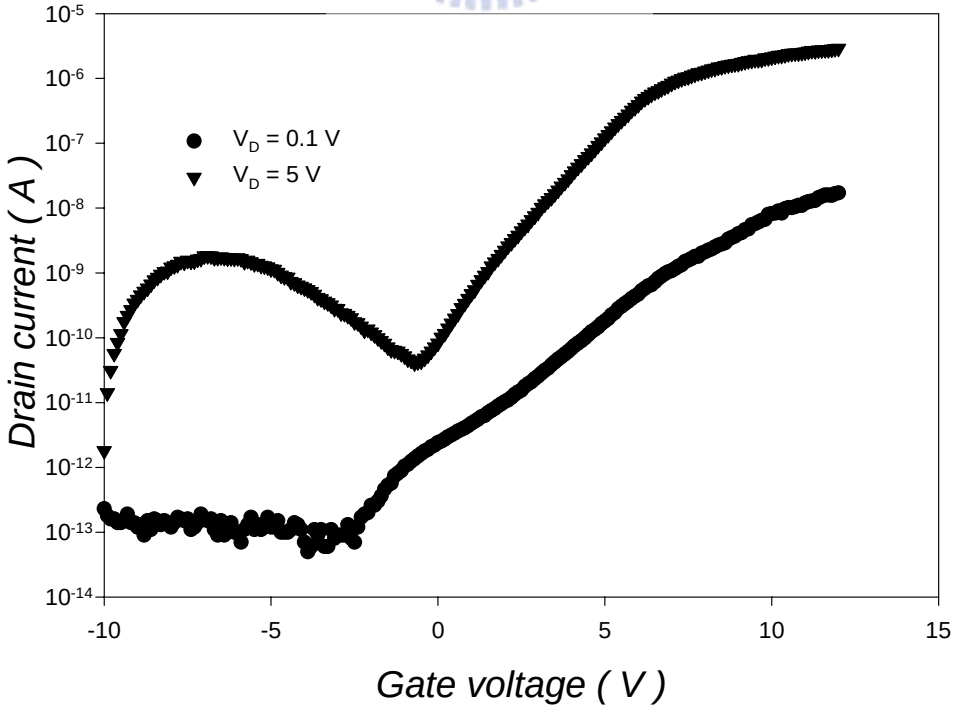


(c)

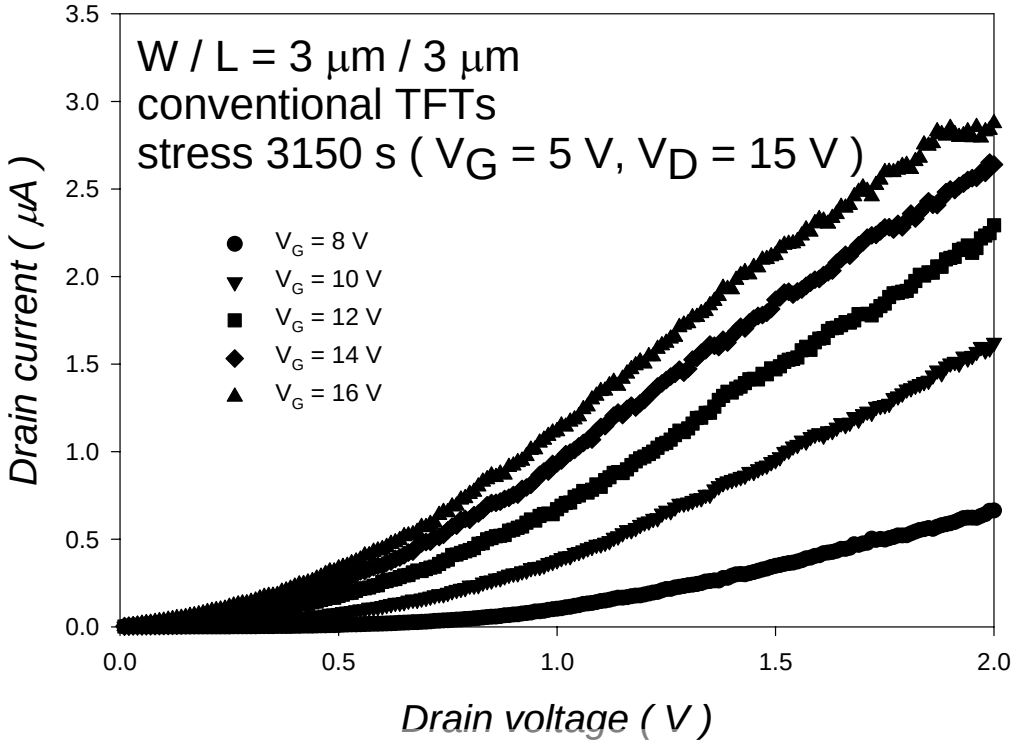
Fig. 4-3-2 The typical characteristics for conventional TFTs stressed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.


W / L = 3 μm / 3 μm
conventional TFTs
stress 3150 s (V_G = 5 V, V_D = 15 V)
Drain current (μA)
V_G = 2 V
V_G = 4 V
V_G = 6 V
V_G = 8 V
V_G = 10 V
V_G = 12 V
0
1
2
3
4
5
6
7
0
2
4
6
8
10
Drain voltage (V)

(a)

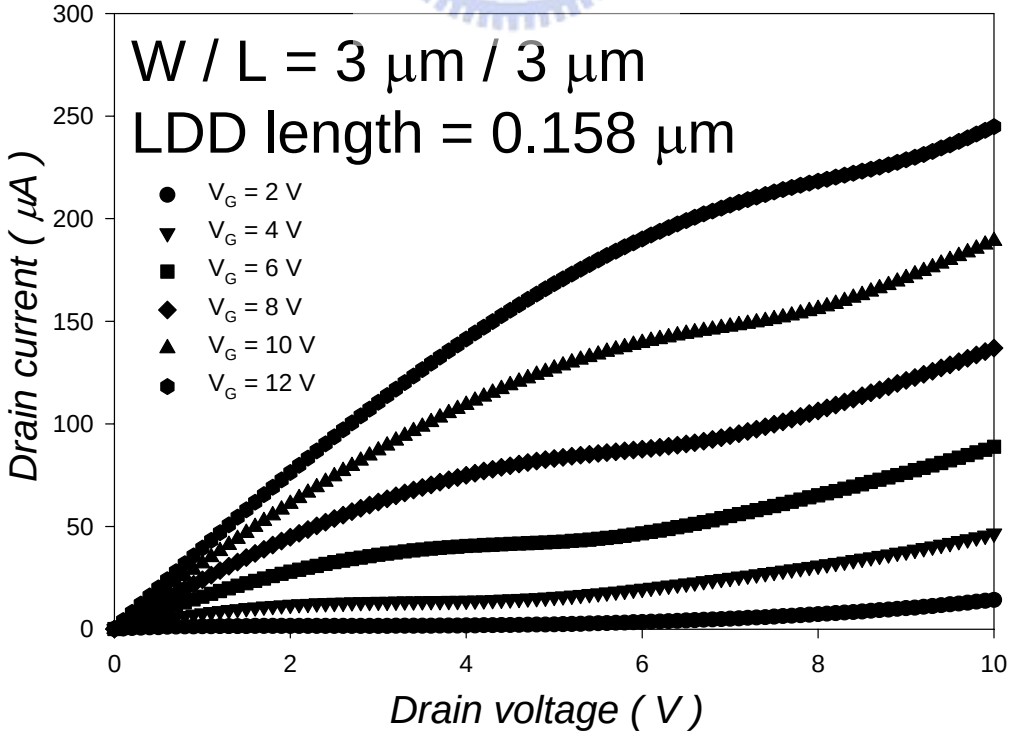

W / L = 3 μm / 3 μm
conventional TFTs
stress 3150 s (V_G = 5 V, V_D = 15 V)
Drain current (A)
V_D = 0.1 V
V_D = 5 V
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
-10
-5
0
5
10
15
Gate voltage (V)

(b)

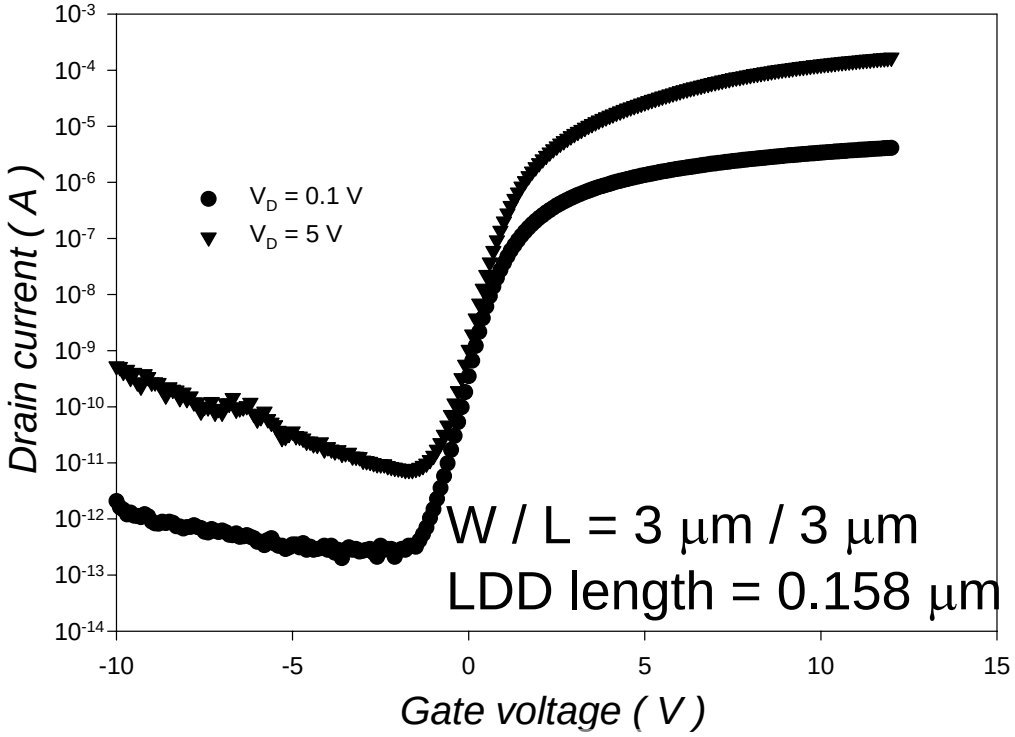


(c)

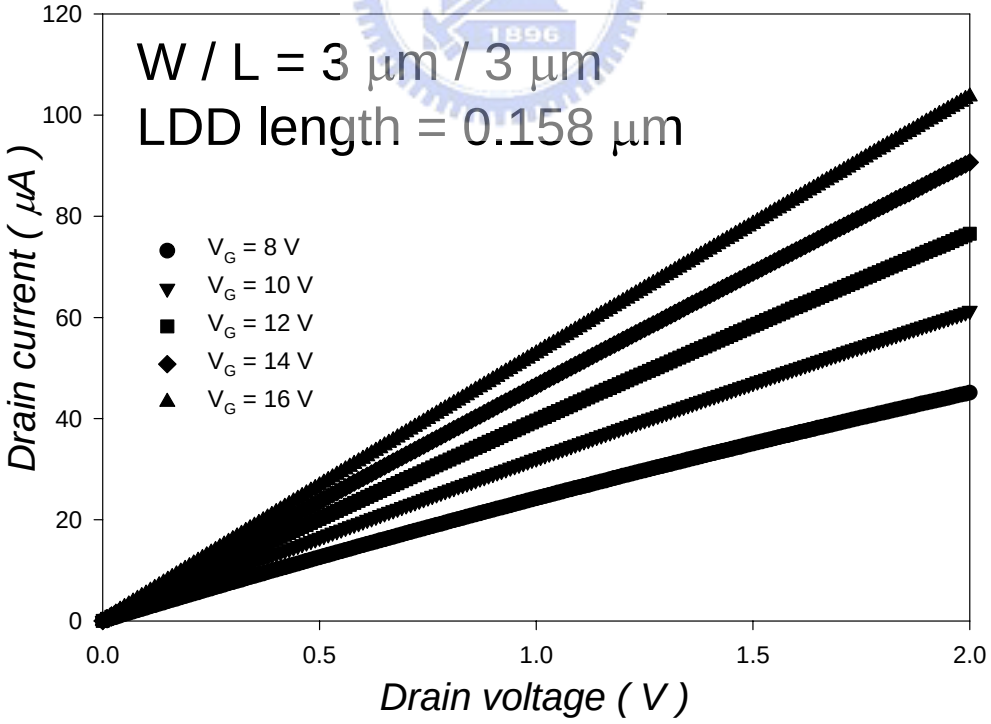
Fig. 4-3-3 The typical characteristics for conventional TFTs stressed and reversed Drain/Source contact : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.



(a)

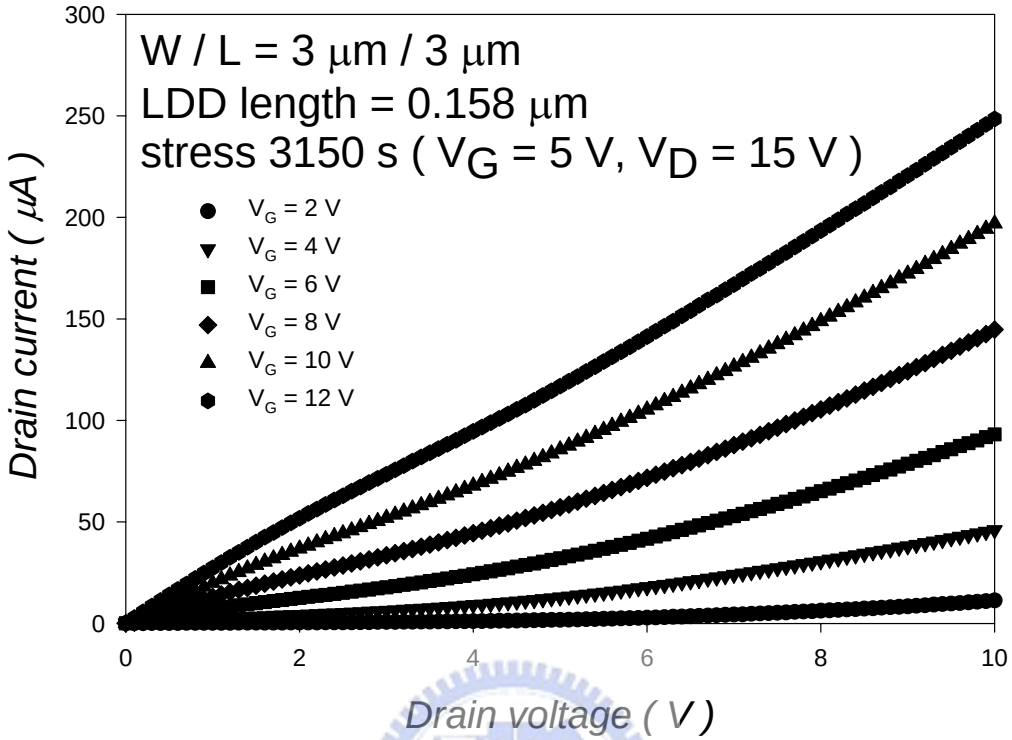


(b)

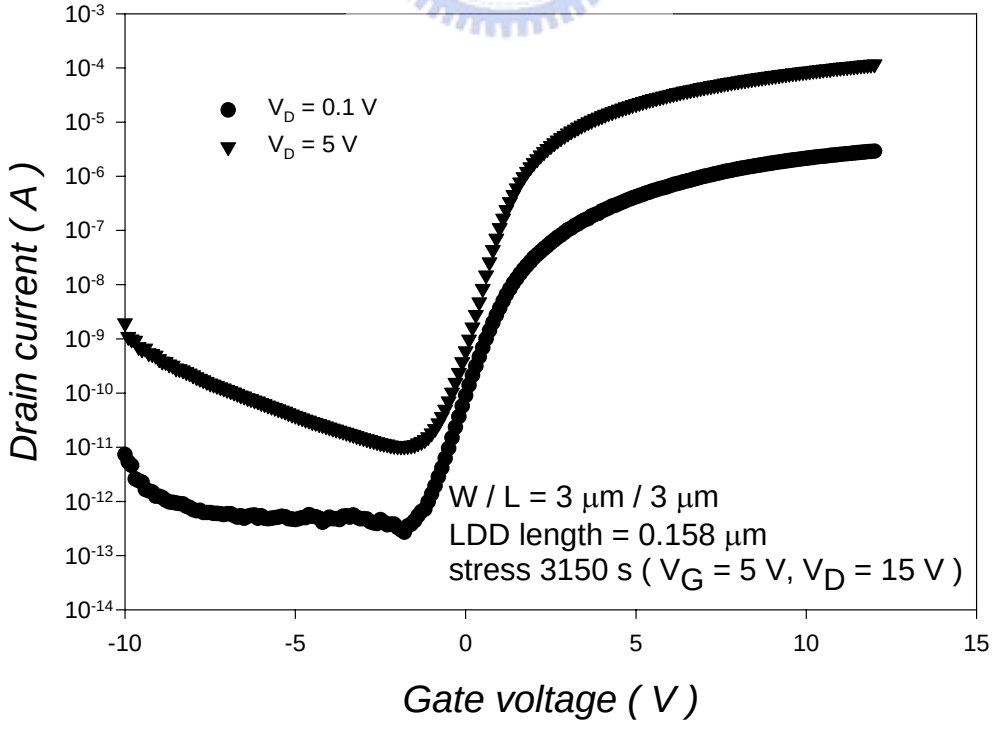


(c)

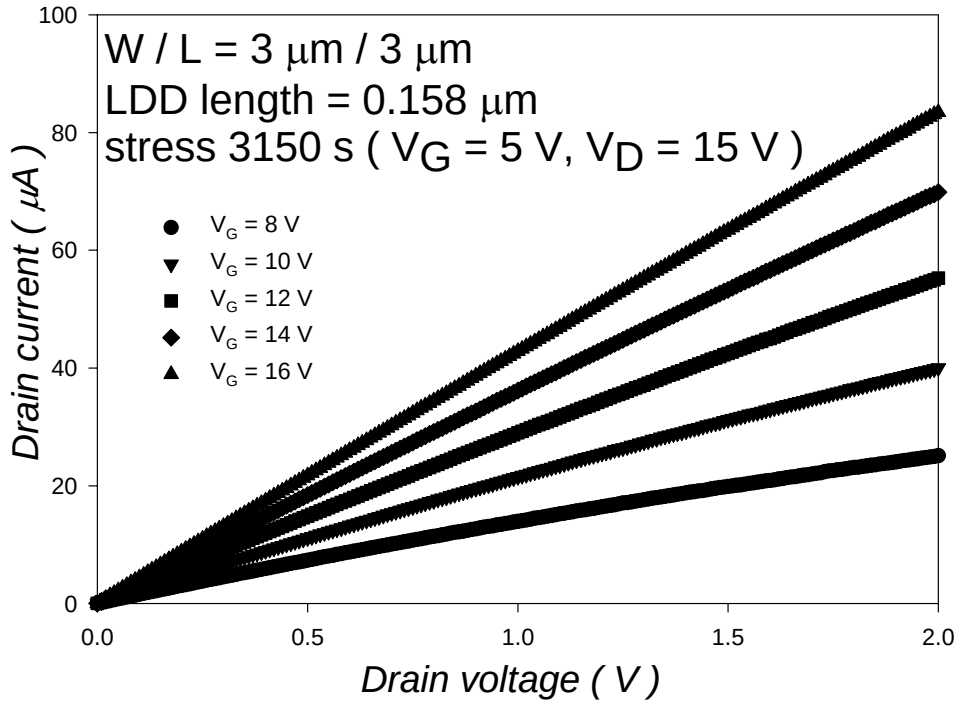
Fig. 4-3-4 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.


W / L = 3 μm / 3 μm
LDD length = 0.158 μm
stress 3150 s (V_G = 5 V, V_D = 15 V)
V_G = 2 V
V_G = 4 V
V_G = 6 V
V_G = 8 V
V_G = 10 V
V_G = 12 V
Drain current (μA)
Drain voltage (V)
300
250
200
150
100
50
0
0
2
4
6
8
10

(a)

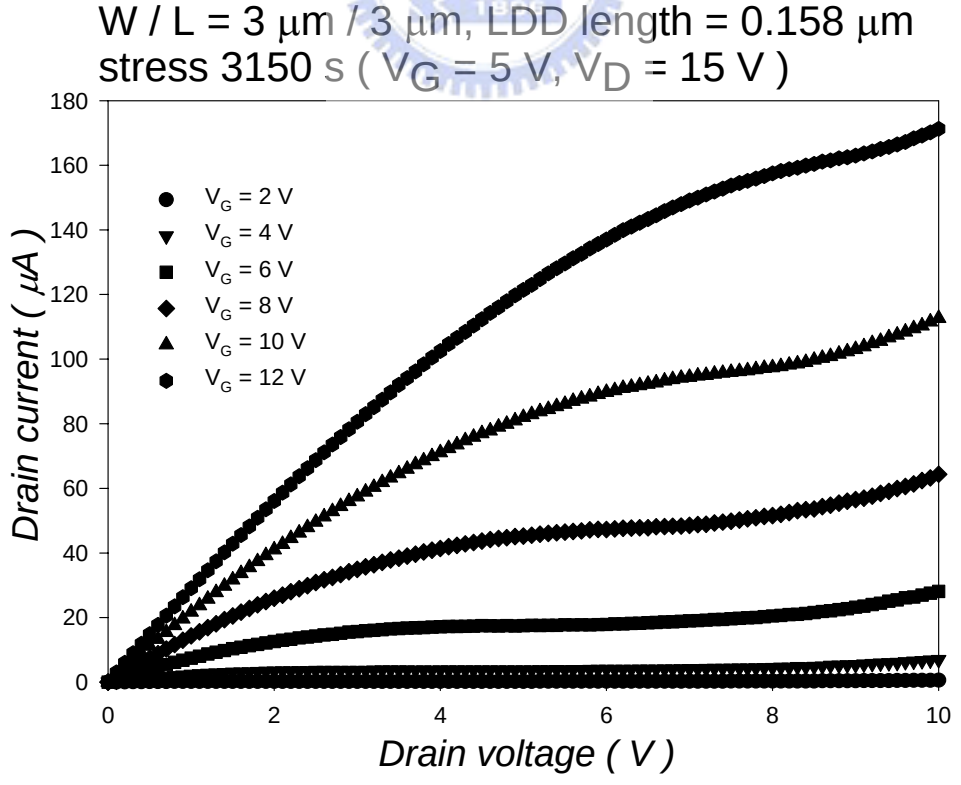

V_D = 0.1 V
V_D = 5 V
W / L = 3 μm / 3 μm
LDD length = 0.158 μm
stress 3150 s (V_G = 5 V, V_D = 15 V)
Drain current (A)
Gate voltage (V)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
-10
-5
0
5
10
15

(b)

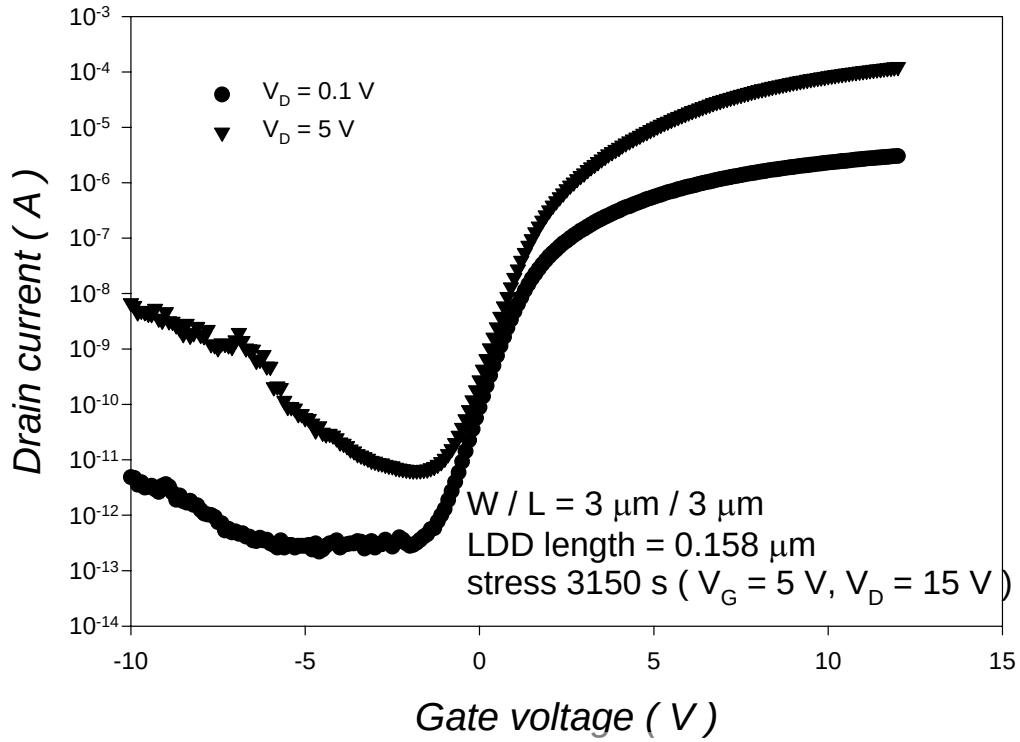


(c)

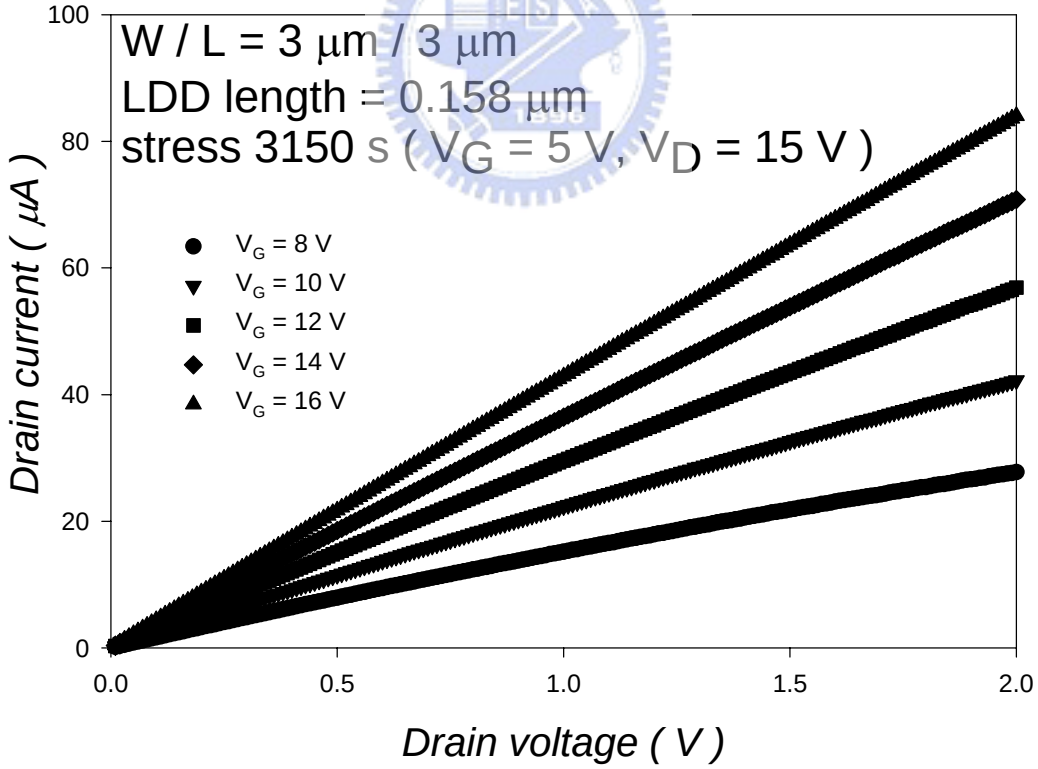
Fig. 4-3-5 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm and stressed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.



(a)

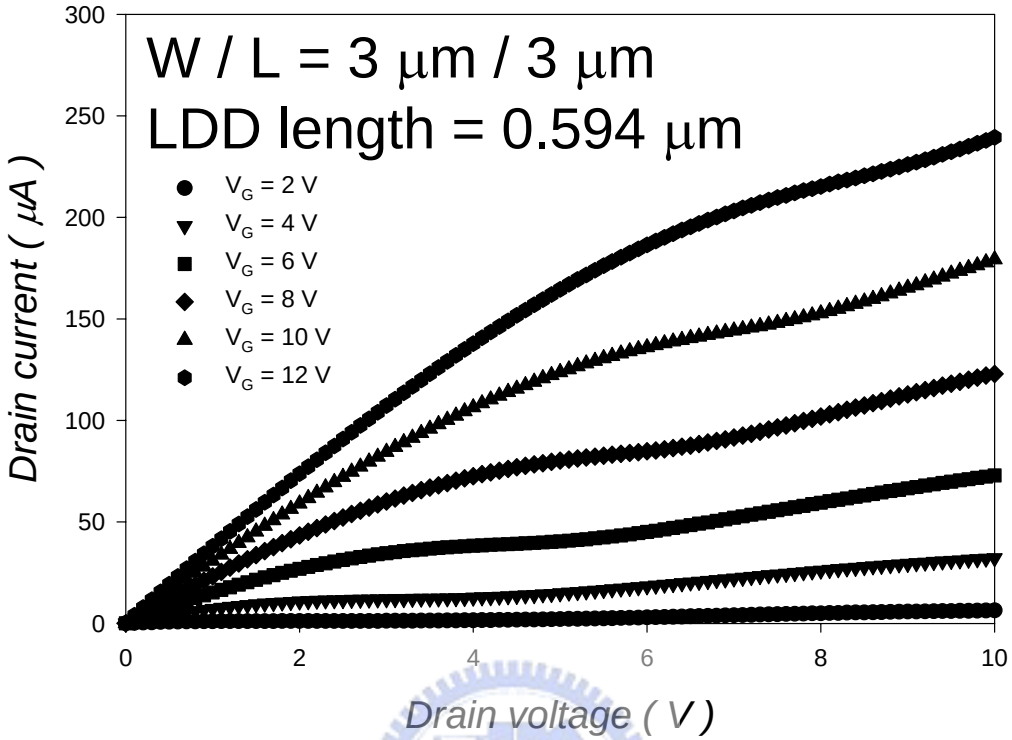


(b)

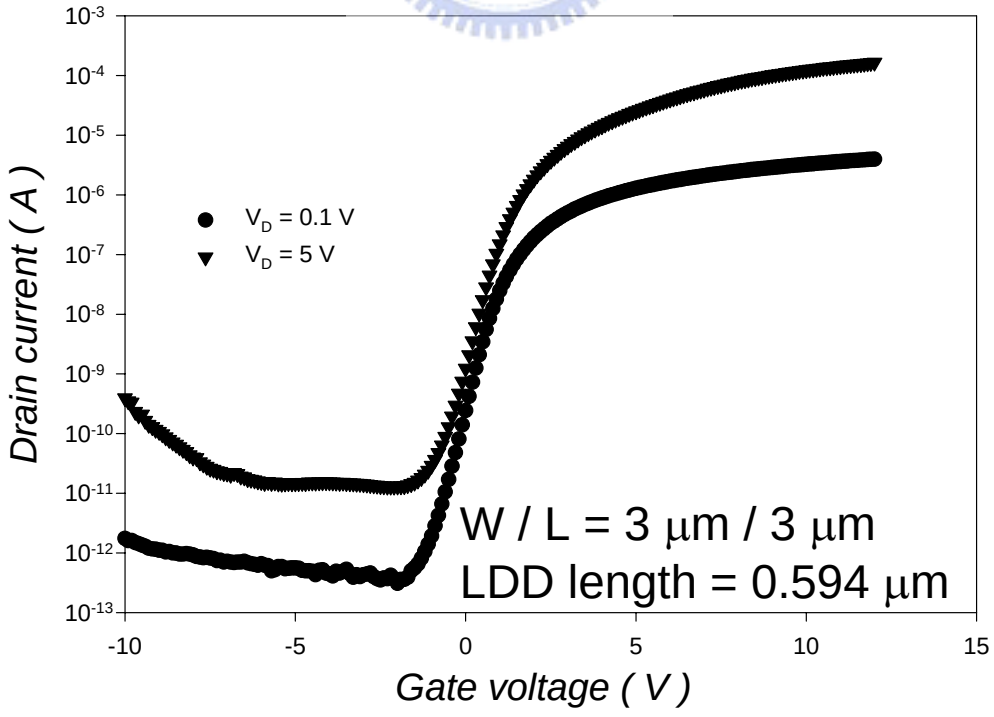


(c)

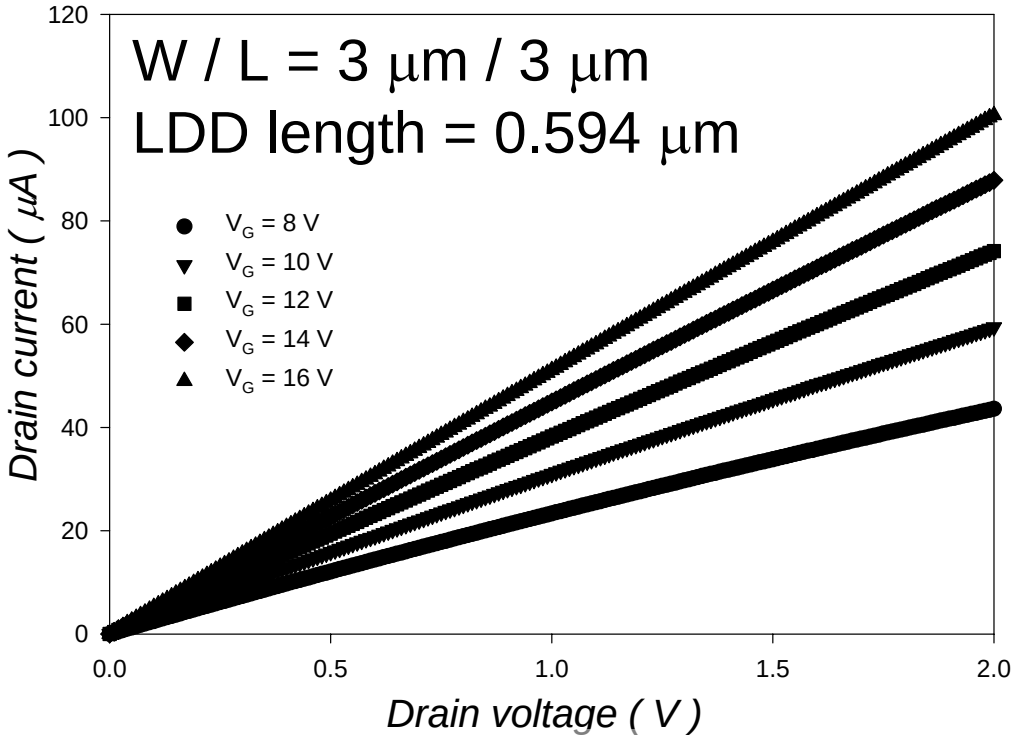
Fig. 4-3-6 The typical characteristics for GOLDD TFTs which LDD length =0.158 μm, stressed and Drain/source reversed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.


W / L = 3 μm / 3 μm
LDD length = 0.594 μm
V_G = 2 V
V_G = 4 V
V_G = 6 V
V_G = 8 V
V_G = 10 V
V_G = 12 V
Drain current (μA)
Drain voltage (V)
0
50
100
150
200
250
300
0
2
4
6
8
10

(a)

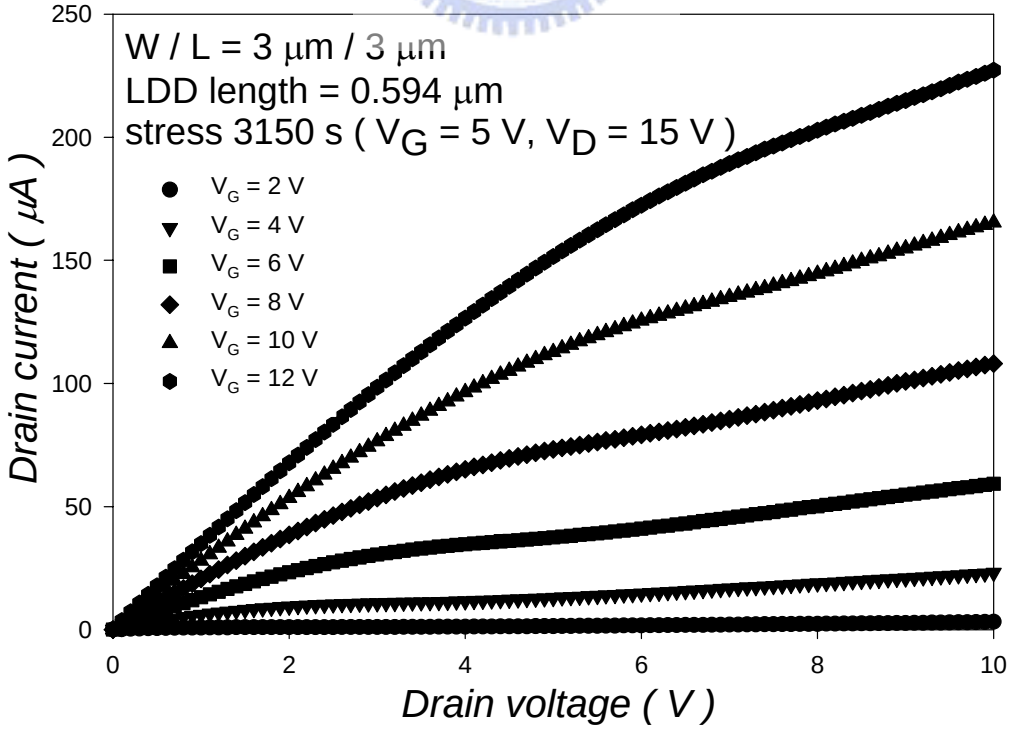

V_D = 0.1 V
V_D = 5 V
W / L = 3 μm / 3 μm
LDD length = 0.594 μm
Drain current (A)
Gate voltage (V)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
-10
-5
0
5
10
15

(b)

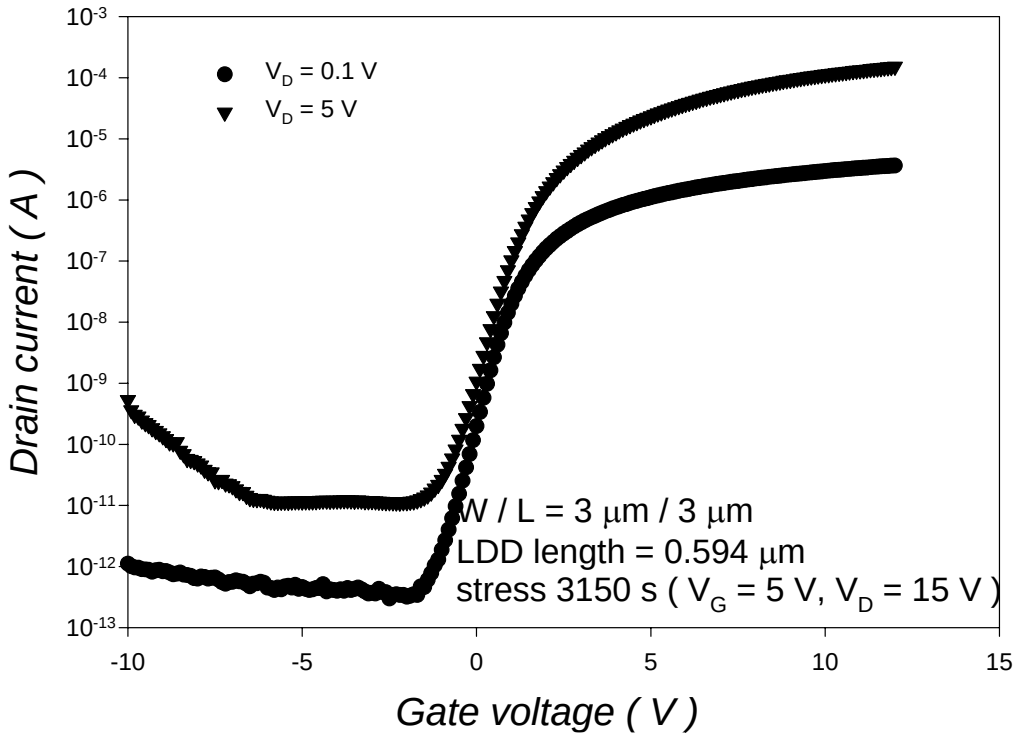


(c)

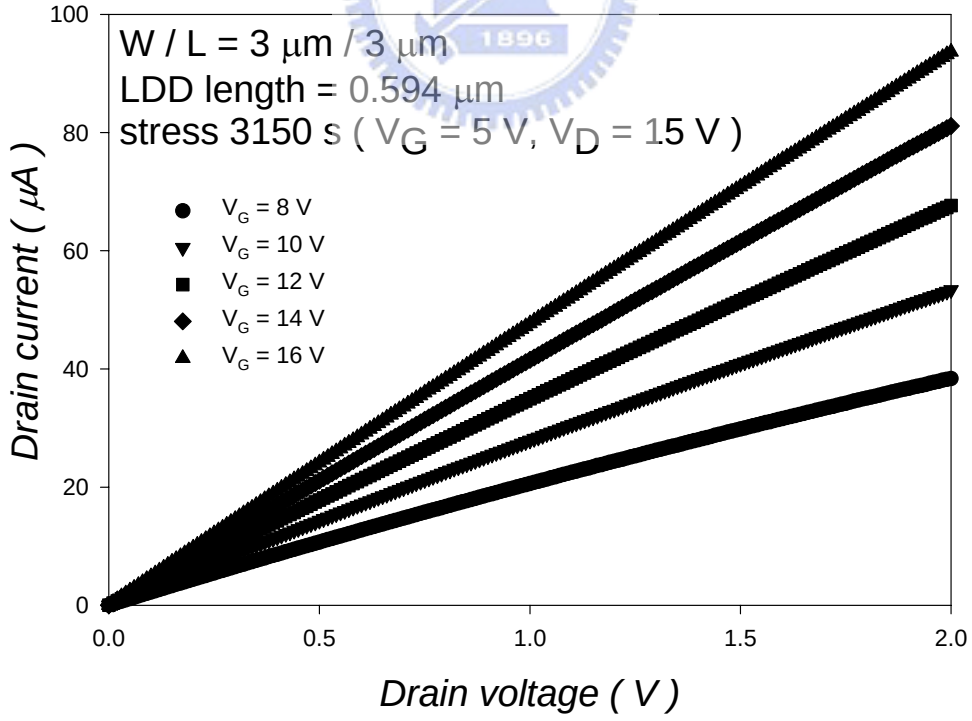
Fig. 4-3-7 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.



(a)

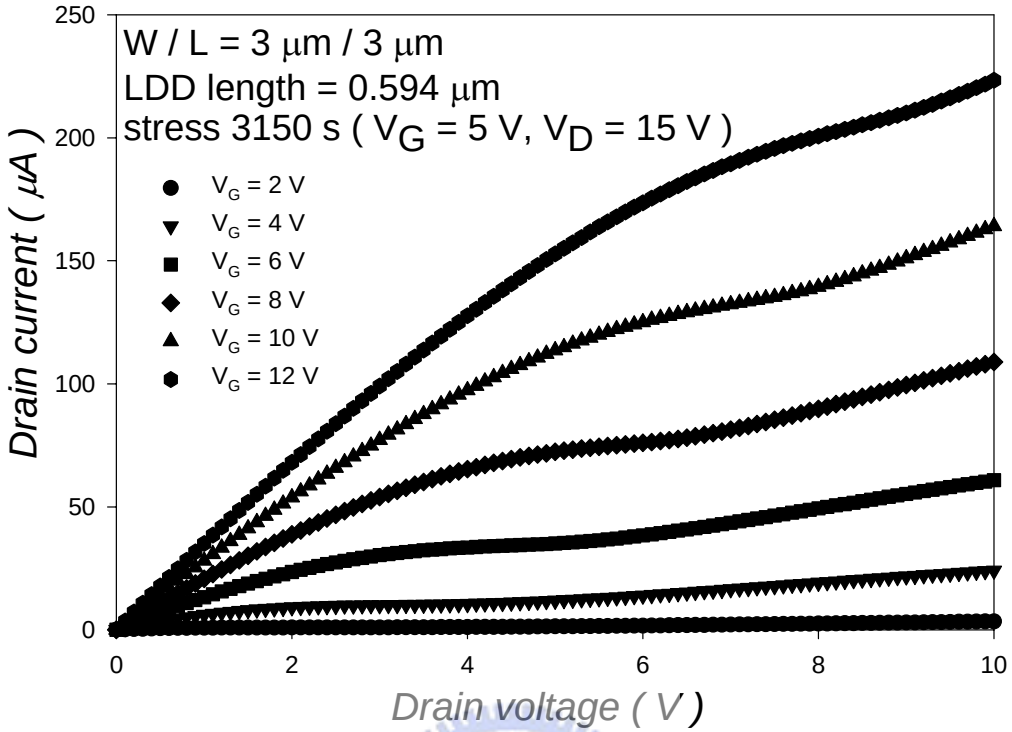


(b)

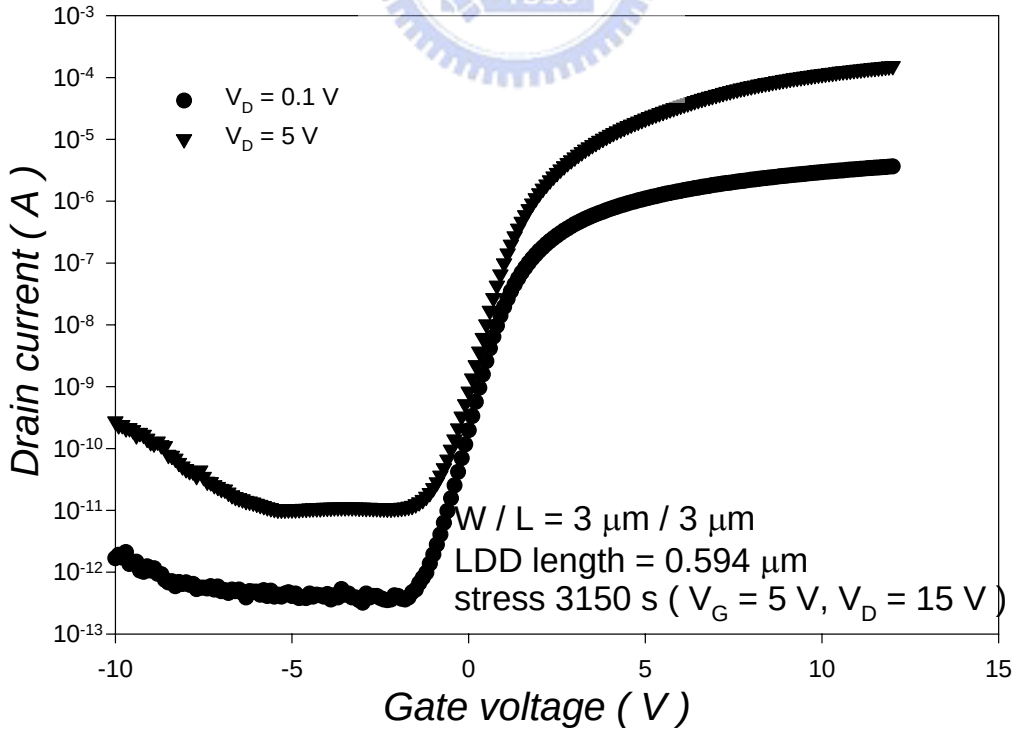


(c)

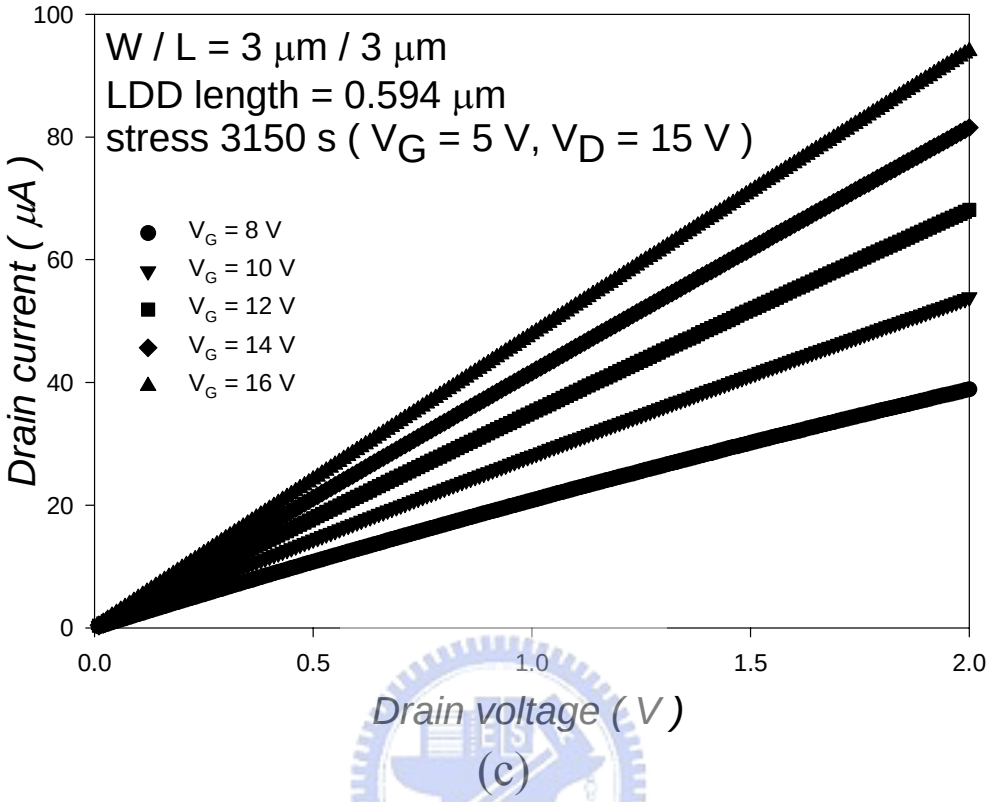
Fig. 4-3-8 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm and streed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.


W / L = 3 μm / 3 μm
LDD length = 0.594 μm
stress 3150 s (V_G = 5 V, V_D = 15 V)
V_G = 2 V
V_G = 4 V
V_G = 6 V
V_G = 8 V
V_G = 10 V
V_G = 12 V
Drain current (μA)
Drain voltage (V)
0
50
100
150
200
250
0
2
4
6
8
10

(a)


V_D = 0.1 V
V_D = 5 V
W / L = 3 μm / 3 μm
LDD length = 0.594 μm
stress 3150 s (V_G = 5 V, V_D = 15 V)
Drain current (A)
Gate voltage (V)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
-10
-5
0
5
10
15

(b)



(c)

Fig. 4-3-9 The typical characteristics for GOLDD TFTs which LDD length =0.594 μm, streed and Drain/source reversed : (a) I_D-V_D, (b) I_D-V_G (c) I_D-V_D.

Table I Extracted Parasitic Resistance of Standard Devices and Proposed GOLDD Devices with Channel Width = 3um.

W = 3 um

	LDD density	LDD length	Rp
standard	0	0	17600Ω
	1E13	0.158 um	3300Ω
	1E13	0.594 um	4500Ω
	5E13	0.158 um	3000Ω
	5E13	0.685 um	3600Ω

Table II Extracted Parasitic Resistance of Standard Devices and Proposed GOLDD Devices with Channel Width = 10 um.

W = 10 um

	LDD density	LDD length	Rp
standard	0	0	6400Ω
	1E13	0.158 um	1300Ω
	1E13	0.594 um	2350Ω
	5E13	0.158 um	1200Ω
	5E13	0.685 um	1600Ω

Table III Extracted trap density of Proposed GOLDD Devices with Channel Width = 3um.

LDD density	LDD length	Nt(10^17cm-3)
1E13	0.158 um	3.2
1E13	0.594 um	3.5