國 立 交 通 大 學

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博 士 論 文

複晶矽薄膜電晶體中漏電流及可靠度課題之研究

A Study of Leakage Current and Reliability Issues in Poly-Si Thin-Film Transistors

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摘要

本論文提出並實作一種具有自我對準能力之複晶矽奈米線薄膜電晶體，以及一種應用於解析熱載子衰退的新穎測試結構。首先，我們描述奈米線薄膜電晶體之製程，及如何製作此複晶矽奈米線的製程參數。我們也審視了影響奈米線尺寸及形狀之因子。這個製程非常簡單，不牽涉到複雜且昂貴的電子束微影或是深紫外光微影設備。

我們研究並討論了奈米線薄膜電晶體的開狀態特性，包括剛製成的元件及經過電漿處理的元件，然後討論了電漿處理及尺寸對於電特性的影響。與傳統平面結構的元件比較，此奈米線通道的優點包括有：絕佳的開電流密度及對短通道效應有較佳的控制能力等等。此外，由於奈米線的寬度很窄，在進行氫化的時候能夠更夠效率地使元件的特性改善。

我們也研究了奈米線薄膜電晶體其獨特的關狀態漏電流機制。產生於閘極與汲極間重疊區域的閘極引發汲極漏電流(gate-induced drain leakage, GIDL)，被發現是造成此一異常漏電流的元兇。我們仔細檢驗了此一異常漏電流的產生原因，以及電漿處理對於此漏電流的影響。我們發現此一電流起因於在閘極與汲極介面的低摻雜區域，此區域引發了一條額外的漏電流路徑。在檢驗了漏電流的起因之後，我們提出並實際驗證了數種減

少此一漏電流的方案。這些方案包括了快速熱退火(Rapid thermal annealing, RTA)、在閘極與汲極間插入一層氮化矽、以及改使用複晶矽鍺材料作為奈米線通道等。這數種方案的特色被逐一比較並加以討論。

我們也提出並實作了一種新穎的測試結構，可以解析薄膜電晶體中熱載子衰退所發生的位置及時間演變。此一新穎測試結構的製作方式與傳統的薄膜電晶體一樣容易，與現在的超大規模積體電路製程完全相容，並且不需要額外的光罩。我們檢視了此一測試元件所帶來之靈敏度的提昇以及在決定施壓條件時的優點，也探討了金屬後電漿處理對於熱載子衰退效應的影響。特別的是，我們在研究過程中，利用此一結構發現了兩種會造成臨界電壓漂移的機制。

由於此測試結構的高靈敏度及解析能力，使得在研究可靠度相關議題時，能夠直接利用此一測試結構直接觀察元件的衰退現象，不必再利用高電壓施壓條件下的結果，去推測元件在正常操作或是低電壓施壓條件之下的衰退現象，並可以比較元件在高低電壓施壓下的不同現象和機制。

我們也利用此一測試結構，研究了當元件操作於交流模式時，所產生的熱載子衰退現象。關於操作頻率、上升及下降時間都有詳細的探討。利用此一測試結構的特性，輸入訊號中各個準位階段其所對應到的損傷位置可以被定位出來。實驗結果顯示，損傷主要是當閘極訊號切換時，瞬間所產生的熱載子所導致。伴隨著偵測熱載子衰退時的高靈敏度，此一元件也可以應用於一般交流操作時的可靠度研究之用。

在此論文的最後一個部份，我們進行了關於缺陷能態密度的分析。在說明原理及方式之後，我們可以利用前述的測試元件萃取出當元件受到熱載子損傷之後，其能態密度分佈的變化。由於傳統元件在受到熱載子損傷後，通道中各部位的能態密度分佈將會變

得不均勻，且局部的缺陷密度增加量將會在萃取能態密度分佈時被整體所稀釋，造成實務上萃取的困難。利用此一測試元件，我們可以萃取出各部位其能態密度分佈的變化，並重組成元件衰退後的真實分佈狀態，並利用元件模擬技術重現元件的次臨界特性曲線。

關鍵字：薄膜電晶體；複晶矽；奈米線；自我對準；閘極引發汲極漏電流；電漿處理；矽鍺；快速熱退火；熱載子；熱載子衰退；熱載子效應；測試結構；交流施壓；能態密度；元件模擬；可靠度。


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A Study of Leakage Current and Reliability Issues in Poly-Si Thin-Film Transistors

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Abstract

In this thesis, we proposed and demonstrated a poly-Si thin-film transistor with self-aligned nanowire channels, as well as a novel test structure suitable for resolving hot-carrier degradation. Firstly, the fabrication of proposed NWTFT was described, followed by the detail in poly-Si nanowire formation and investigation of the factors affecting size and shape of the nanowire. The fabrication is simple and does not involve costly lithography tools.

On-state characteristics of NWTFT were then examined and discussed, including as-fabircated and plasma-treated samples. The effects of post-metal treatment and geometric parameters on NWTFT were then discussed. The advantages of NWTFT were demonstrated by comparing with traditional planar structures. Such nanowire structure has been shown to be excellent in terms of on-current per unit width and controllability over short-channel effects. Owing to the fine nano-scale of NW width, hydrogenation would be very efficient for further performance improvement.

The unique off-state leakage mechanism of NWTFT was also investigated. A gate-induced drain leakage (GIDL), which is generated in the overlapped region between the gate and the drain, was uncovered as the major culprit for the anomalous leakage. The origin

of the anomalous leakage was then examined, as well as the effect of post-metal treatment. This current was found to originate from the lightly-doped region at gate/drain interface, which induced an additional current path. After that, several modifications were proposed and demonstrated in order to alleviate the unique leakage. Rapid thermal annealing (RTA), inserted nitride mask, and poly $Si_{1-X}Ge_X$ were investigated and compared.

A tester, which can spatially and temporally resolve hot-carrier degradations, was proposed and demonstrated. The fabrication of the novel test structure is simple and compatible with standard ULSI processings without extra masking. Advantages in sensitivity and stress-condition determination were discussed, accompanying with the effects of post-metal plasma treatment on hot-carrier degradations. Specifically, we found that at least two mechanisms are responsible for the negative threshold voltage shift detected by monitor transistors. The high sensitivity and resolving capability of the novel test structure can also help researchers observe directly degradation phenomena occurring when devices are stressed under moderate or minor conditions.

We also studied the phenomena of hot-carrier degradation during AC operations using the proposed test structure. Effects of frequency, rising and falling times, were investigated and discussed. The phenomena of the hot-carrier degradation can be spatially resolved using the proposed tester. By applying such a tester to AC hot-carrier stressing, the relationship between different stages of input signal and resultant damage location can be established. The tester also showed a high sensitivity in detecting even mild AC degradation. The experiment provides unambiguous evidence that the damage occurs during the transient stages, with the aid of the test structure.

At the last part of the thesis, the analyses related to effective density-of-states distributions were performed. After the description of experimential procedures, effective

density-of-states distributions of localized damaged regions were extracted using the aforementioned tester. The information revealed by the analyses was then discussed. The extracted density-of-states distributions for both unstressed and stressed films were used to conduct simulations for subthreshold characteristics of TFTs and compared with the experimental data. The combination of the proposed novel test structure and density-of-states extraction technique provides a powerful tool for resolving the non-uniform density-of-states distribution of TFTs after HC stressing, which is impossible using traditional testers.

Keyword: Thin-film transistor; Polycrystalline silicon; Poly-Si; Nanowire; NWTFT; Self-aligned; Gate-induced drain leakage (GIDL); Plasma treatment; Silicon germanium; Rapid-thermal annealing (RTA); Hot-carrier; Hot-carrier degradation; Hot-carrier effect; Test structure; HCTFT; AC stress; Density of states; Device simulation; Reliability.


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從碩士班加入當時的記憶體元件實驗室，到博士班從改名後的先進元件技術實驗室畢業，這七年裡的日子，現在回想起來，點點滴滴，印象深刻。那些在 NDL 度過的日日夜夜，不管是早上五點起來搖酸、換酸、簽 run、E-gun 的生活，還是下午進去出來時正好看到隔日的日出，現在回想起來，那些曾經的苦澀，已經轉化成「啊! 我也有過這種日子」的小小驕傲。

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李明賢

誌於風城交大

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Chapter 1

Introduction

Polycrystalline silicon (Poly-Si) thin-film transistors (TFTs) have been extensively used in many applications, including active-matrix liquid-crystal displays (AMLCDs) [1.1]-[1.4], memory devices [1.5]-[1.9], image sensors [1.10], and thermal printer heads [1.11]. Because of their better grain crystallinity, compared with the amorphous counterparts, better device performance such as carrier mobility and drive current can be realized in poly-Si TFTs.

1.1 An overview of poly-Si thin-film transistors: trends in the development

Thin-film transistors have been put into commercial use in the past decades. Since it is impossible to deposite single crystalline silicon (c-Si) film on glass substrate by low-pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD), amorphous silicon or polycrystalline silicon are used as the channel materials in TFTs.

By replacing quartz substrate with low-cost glass, and migrating the channel material from amorphous to polycrystalline, TFTs can now meet the requirement in fabrication cost, process temperature, and device performance. Because of the lack in short range order, the electron field effect mobility (μ_n) of amorphous silicon material is usually lower than 1 cm^2/V-s. On the contrary, the mobility of poly-Si material varies from tens to hundreds cm^2/V-s, depending on the process condition and the treatment in material preparation.

Nonetheless, both are much lower than that of c-Si (~600 cm^2/V-s). Therefore, how to increase the mobility of poly-Si is one of the most important challenges.

1.1.1 Efforts in mobility enhancement

Since mobility of poly-Si is mainly determined by the crystallinity, many studies focus on the grain size and the grain quality in poly-Si material. Although poly-Si can be directly deposited by LPCVD over 540-620˚C, its mobility is limited to about 10 cm^2/V-s due to grain size of 100~500nm [1.12]. Solid phase crystallization (SPC) technique, where amorphous films was first deposited and then crystallized into poly-Si, has been shown to improve mobility and enhance grain size [1.13]. Usually, the crystallization process is performed in furnaces at 600˚C for 20-24 hours. The resultant grain size can exceed 1 μm, and the mobility can reach several tens of cm^2/V-s. One of the practical limitations of the SPC technique is the temperature of 600˚C, which is still higher for most glass substrates. Processes where poly-Si preparation is carried out in lower temperatures hence were developed. Excimer laser anneal (ELA) [1.14]-[1.16] represents one of the promising candidates for low-temperature poly-Si (LTPS) technologies. By radiating pulsed excimer lasers on amorphous Si films, localized region can be melted and transformed into poly-Si. Since only the localized region was heated, the substrate temperature can be kept to lower than 400˚C. After adjusting energy density and duration of the laser pulse, along with scanning patterns [1.17] and substrate temperature, a high mobility of 280cm^2/V-s can be achieved [1.18]. Another candidate for LTPS is the metal-induced lateral crystallization (MILC). It uses metals like Ni [1.19] or Pd [1.20] as the catalyst to promote the transition of a-Si to poly-Si in a lower temperature.

1.1.2 Efforts in off-state leakage reduction

In addition to mobility, another prime concern for TFT applications is their high off-state

leakage current. Off-state leakage is a critical factor since it increases standby power dissipation. Most of the leakage is originated from the electrical field between gate and drain [1.21], combined with the impact of the defects inside channel material. Since the gate/drain bias is required for circuit operation, all efforts in off-state leakage reduction are focused on the reduction of trap state density or the uses of structural modification to reduce the localize electric field between gate and drain.

The role of the trap states is to determine carrier generation rate and lifetime of generated electron-hole pairs. To reduce the trap density, employment of hydrogen passivation is a common technique [1.22]. Another approach is to enlarge grain size and reduce the number of the grain boundary in poly-Si material, because most of defects are located inside the grain boundaries. Equipped with the knowledge that the off-state leakage is originated near drain, by controlling the location of grain boundaries and keeping them away from the drain junction, the off-state leakage can also be effectively reduced [1.23].

Lightly-doped drain (LDD) is the most popular approach of structural modifications for leakage reduction [1.24][1.25]. It can effectively reduce the high electric field when devices are operated at off-state [1.26]. One of its impacts to TFTs is the attenuation of on-state current due to the addition of series resistance. There are other approaches which are based on the concept of LDD, but trying not to attenuate the on-state current [1.27]. In addition to LDD, other approaches such as field-induced drain [1.28] or multi-fingered gate [1.29] were also proposed to reduce the off-state leakage.

1.2 An introduction of silicon nanowires

Minimization is always the most critical issue in silicon technology. To enhance the output current and increase the density of devices per unit area on a chip, the geometry of device have been continually scaled down for past decades [1.30]. Nowadays with the

technology node at 65nm, the semiconductor industry has entered into nanoscale era. As the device is shrunk to the nanoscale regime, where the geometry of devices is smaller than 100nm, mechanical and electrical properties of the material may be different from those in the bulk material. As a result, the realization of some new structures and materials is likely. In addition to conventional planar structure which has been broadly employed in MOSFETs, some other structures such as FinFET [1.31], single-electron transistors [1.32], and nanowire [1.33][1.34], were proposed.

Nanowires can be used as a conduction wire [1.35], a resistor [1.36], or a field-effect transistor (FET) [1.37]. Owing to its unique feature of high-surface-to-volume ratio, nanowire exhibits great potential for some specific applications such as bio-sensors [1.38][1.39], memory devices [1.40], and switches [1.41]. There are two major approaches for nanowire preparation. One is the top-down approach, which requires advanced lithographic tools like deep UV steppers [1.48][1.49]. Another is the bottom-up approach, such as growth of the nanowire by catalyst-assisted growth or epitaxy [1.50]. The former approach is very straight-forward, but costly. In contrast, the latter approach is very flexible for experimental studies, but has concerns of metal contaminations. Although many methodologies and materials have been proposed and demonstrated for nanowire preparation, the top-down approach, which is compatible with current MOSFET technology and without issues of contamination, is still the first choice for commercial manufacturing. More detail about the methodologies will be introduced in Section 2.1.

1.3 Reliability issues in poly-Si TFTs

As poly-Si TFTs were employed in the commercial applications, long term stability in device characteristics during circuit operations becomes another important issue. To keep circuits function properly, performance and electrical characteristics of TFTs must be within

the design specification, even after long-term operations. As a result, reliability issues need to be taken into considerations.

Most of the reliability issues come from the low-temperature process needed for poly-Si TFTs and the nature of materials used in poly-Si TFTs. For instance, the deposited gate oxide, unlike the high-quality thermal oxide in MOSFET, may induce high gate leakage current or gate oxide failure after long-term operations [1.42][1.43]. Another example is hot-carrier degradation and self-heating in poly-Si TFTs. The former may result in shift of device characteristics owing to the localized damage induced in some portions of channel [1.44][1.45]. The latter may be ascribed to poor thermal-conducting of glass substrate and large amount of heat generated from on-current [1.46][1.47].

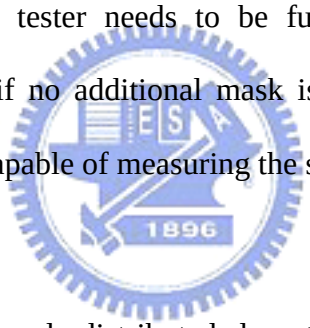
1.4 Motivation of this study

As mentioned in the above sections, the top-down approach is the best choice when integrating such a new device into current MOSFET technology. Since the cost is a critical concern for the top-down method, it is desirable to develop a new method that can not only be compatible with ULSI processes, but also reduces cost of fabrication. To achieve these goals, expensive advanced lithography must be avoided and an alternative approach needs to be adopted. It is required that the nanowire can not only be produced, but also be positioned at specific locations (i.e., the channel region). It is also desirable that this approach must be integrated with MOSFETs in a seamless manner. In lines with this, a novel method to fabricate nanowire thin film transistors (NWTFTs) was proposed and demonstrated in this dissertation.

While characterizing the proposed NWTFT, we found that the off-state leakage current of device is much larger than we originally expected. After further investigation of the leakage current, we found that the current is proportional to the gate-to-drain overlap region. To

uncover the mechanism, more experiments were performed and some approaches were proposed in order to reduce the effect of such anomalous leakage. Eventually, we successfully demonstrated some process and device modifications, and new material for leakage reduction. The results are in a good agreement with our understanding.

Similar to the device minimization which led us to the study of NWTFTs, the need in hot-carrier analysis also led us to the development of new test structures. Owing to the nature of non-uniform distributions of damages across the channel, the call for a test structure which is capable of spatially resolving the damages along the channel of stressed transistor is urgent. Information gathered from such test structures will be very valuable since it will enable us to easily locate the damage sites, analyze the mechanisms, and find cures to alleviate impacts of hot-carrier degradation. Again, this tester needs to be fully compatible with the ULSI processes. It would be even better if no additional mask is needed for such a tester. The outcome is a test structure which is capable of measuring the spatial and temporal evolution of hot-carrier degradation.



Because the damage is non-uniformly distributed along the channel, it is very difficult to extract and analyze the difference in effective density-of-states (DOS) distributions before and after hot-carrier degradation. Since the proposed tester is capable of observing a localized degradation, density-of-states extraction technique can be adopted to investigate the impact of hot-carrier degradation on defect density in certain part of the channel. We have extracted the effective density-of-states distributions in damaged regions and validated the result by conducting the subthreshold characteristics using the extracted DOS and the device simulator.

1.5 Organization of the thesis

In this thesis, seven chapters are organized to present the detail of the aforementioned works. An overview of poly-Si TFTs is described in Chapter 1, together with the introduction

of silicon nanowires and the reliability issue in TFTs. Motivation of this study and organization of this work (i.e., the current section) are also included in this chapter.

In Chapter 2, the nanowire thin-film transistors (NWTFTs) are demonstrated. Several methodologies are introduced and compared, providing the backgrounds of nanowire formation. The fabrication of proposed NWTFT is then described, followed by the detail in poly-Si nanowire formation and the investigation of factors that affect size and shape of the nanowire. Afterwards, on-state characteristics of NWTFTs are examined and discussed in Section 2.3. The characteristics of both as-fabricated and plasma-treated samples are demonstrated. The effects of post-metal treatment and geometric parameters on NWTFTs are then discussed. Last in this chapter, the advantages of nanowire channel are demonstrated by comparing with the traditional planar structure.

In Chapter 3, the unique off-state leakage mechanism of proposed NWTFT is investigated. In the beginning of this chapter, some background knowledge such as off-state leakages in TFT, proposed mechanisms, analysis methodologies, and proposed leakage reduction methods, are introduced. Afterwards, the leakage mechanism of proposed NWTFT is investigated in Section 3.2. The origin of anomalous leakage is examined, as well as the effect of post-metal treatment. In Section 3.3, several modifications are proposed and demonstrated in order to alleviate the unique leakage. Rapid thermal annealing (RTA), inserted nitride mask, and poly $Si_{1-X}Ge_X$ are investigated and compared. An indicator called OSCR is also proposed to evaluate the effect of these modifications on off-state leakage reduction.

In Chapter 4, the aforementioned novel tester for hot-carrier investigation is introduced, by describing design specifications and operating principles of the tester. The tester, which is called HCTFT, is then evaluated under various hot-carrier stressing experiments. The

capability of the tester in spatially resolving hot-carrier degradation is demonstrated, followed by the discussion on sensitivity and stress conditions. We also demonstrate the application in observing temporal evolution during hot-carrier degradation in this chapter. At the end of this chapter, effects of post-metal plasma treatment on hot-carrier degradation are investigated.

In Chapter 5, the HCTFTs are adopted in analyses of hot-carrier degradation under AC operations. The effects of several parameters, such as frequency, rising and falling times, are investigated and discussed. At last, a complicated case where two different types of degradation simultaneously occur at different part of the channel, along with the analysis using temporal evolution, are demonstrated.

The analyses related to effective density-of-states distributions are performed and discussed in Chapter 6. Procedures of extracting effective density-of-states distributions and setup of simulation are described in detail. Afterwards, effective density-of-states distributions of the localized damaged regions are extracted. The information revealed by the analysis is then discussed. The extracted density-of-states distributions for both unstressed and stressed film are used to conduct simulations for subthreshold characteristics of TFTs and compared with the experimental data.

Finally, the summaries and conclusions as well as some suggestions for future study are given in Chapter 7. References for each chapter are organized and listed at the end of this dissertation.

Chapter 2

Nanowire TFTs with Self-Aligned Poly-Si Channels

2.1 Background

Minimization of silicon devices is being actively pursued. In this regard, Si nanowires (NWs) possess great potential for testing and understanding the fundamental role of dimensionality and size in device electrical properties. Owing to its inherent high surface-to-volume ratio, NWs can effectively suppress the short-channel effects normally encountered in nano-scale MOSFETs [2.1] and provide high surface sensitivity for sensing devices. Many potential applications of Si NWs have been investigated, including nano CMOS [2.1], novel logic devices [2.2], memory devices [2.3], NW TFTs [2.4], biosensors [2.5][2.6] , and nano-electromechanical switch devices [2.7].

Si NWs could be prepared by either top-down or bottom-up methods. The former approach uses advanced lithographic tools like deep UV steppers [2.1][2.3] and e-beam writers [2.6], to define the pattern of NWs. Silicon-on-insulator (SOI) wafers are usually required as the substrate to fabricate single-crystalline silicon (c-Si) NWs. Although well developed and mature for mass production purpose, top-down approach is very costly as it requires expensive equipments and cutting-edge technologies. The size of NWs is also restricted by the resolution limit of lithography and etching. To further shrink the width of the line into nano-scale regime, several techniques have been proposed to replace direct pattern-and-etching. One of the techniques is to use the spacer as the hard mask for etching

[2.8]. This is because the formation of sidewall spacer is well developed, and the size of spacer can be carefully controlled to within several hundreds angstrom. By applying spacers as the hard mask, the Si layer under the spacer can be etched to form the NWs. Another technique is by shrinking the width of patterned oxide layer via over-time wet etching [2.9]. After the chemical shrink is complete and the width of under-cutted oxide is within the nano-scale, photo resist is then removed and shrunk oxide is used as the hard mask for etching of the underlying Si layer.

Unlike the top-down approach, the bottom-up approach is very flexible for experimental studies. Instead of an existing Si layer on the wafer, NWs are prepared by catalyst-assisted growth or epitaxy. Several techniques are developed for this approach, such as vapor-liquid-solid (VLS) [2.10], solid-liquid-solid (SLS) [2.11], solid phase diffusion [2.12], molecular beam epitaxy (MBE) [2.13], oxide-assisted nucleation [2.14], and metal-organic chemical vapor deposition (MOCVD) [2.15]. Since the catalyst is usually metallic, contamination is a great concern. In addition, the positioning of NWs [2.16], and the control of structural parameters such as NW's diameter, length, and orientation [2.17], could eventually hinder its use in practical manufacturing.

A novel method for preparing nanowire TFTs (NWTFTs) is introduced and demonstrated in this chapter. The proposed method is simple and compatible with modern semiconductor processings. Moreover, it does not require costly lithographic tools. Solid-phase crystallized (SPC) poly-Si and as-deposited poly-$Si_{1-x}Ge_x$ by low-temperature chemical vapor deposition (LPCVD) are used as the channel material. Performance comparisons with conventional planar devices, effects of plasma treatment, and geometric parameters are explored and addressed in this chapter. The conduction mechanism of the off-state leakage current and the methods for its reduction will be investigated and demonstrated in the next chapter.

2.2 Fabrication of nanowire TFTs

2.2.1 Device Structure

Figure 2-1 shows schematic structure of the proposed NWTFT. It adopts a side-gated scheme where two NW channels are formed on the sidewall of the gate. Source and drain (S/D) regions lying across the gate are defined simultaneously with the formation of NW channels in a self-aligned manner that will be described later. Another unique feature of the new structure is that a large portion of the NWs is inherently exposed to the environment which serves seamlessly as the sensing site when the device is used as a sensor. For example, for biologic sensor applications, the exposing NW surface serves as the sensing site and, after certain immobilization treatment, specific receptor agents are formed on the surface which could selectively detect the target species contained in the test solution [2.5], [2.6].

The top and cross-sectional views of the NWTFT are shown in Fig. 2-2(a) and Fig. 2-2(b), respectively. The definitions of dimensional parameters are also labeled in Fig. 2-2. It should be noted that “Gate Width” is different from “NW width”.

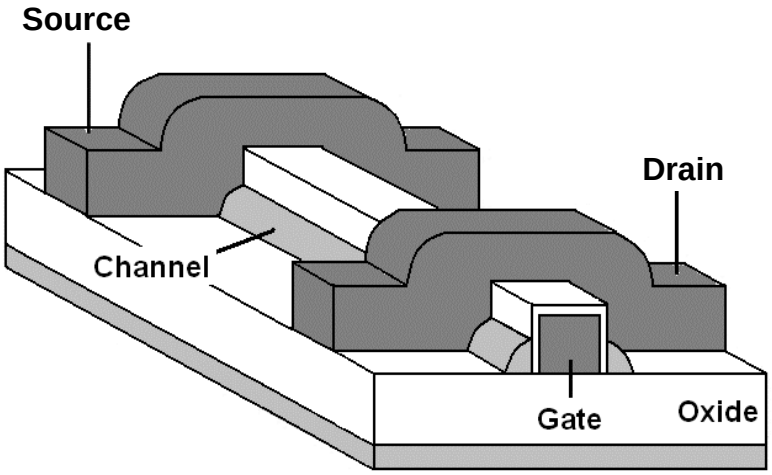


Fig. 2-1 Schematic structure of NWTFTs.

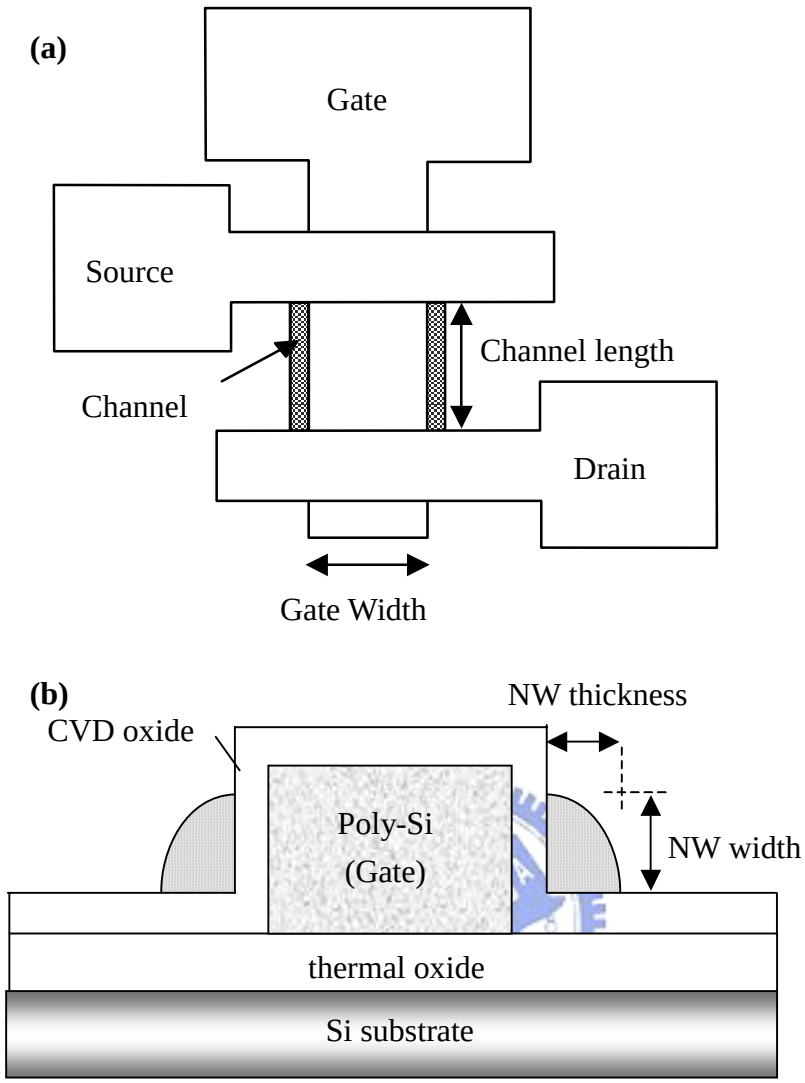


Fig. 2-2 (a) Top view and (b) cross-sectional view of the NWTFT.

2.2.2 Process of fabrication

The key process for fabricating NWTFTs is briefly illustrated in Fig. 2-3. An n^+ poly-Si gate of 100nm thick was first formed on a Si substrate capped with an oxide layer (Fig. 2-3(a)), followed by the deposition of oxide layer using low-temperature chemical vapor deposition (LPCVD). The oxide layer is 30nm thick, and serves as the gate dielectric. An amorphous Si layer of 100nm thick was then deposited by CVD, followed by an annealing step at 600 ^oC in N_2 ambient for 24 hours to transform the amorphous Si into poly-Si (Fig. 2-3(b)). Subsequently, source/drain (S/D) implant was performed (Fig. 2-3(c)). It should be

noted that the implant energy was kept low so that most implanted dopants were located near the top surface of the Si layer. S/D photoresist patterns were then formed on the substrate by a standard lithography step. A reactive plasma etch step was subsequently used to etch the poly-Si layer. The sidewall Si channels were formed after this step in a self-aligned manner (Fig. 2-3(d)). Since the implanted energy is low, dopants in places other than S/D regions were removed during the etch step owing to the shallow project range. The S/D dopants were then activated by an annealing treatment. The fabrication was completed after the formation of test pads using standard metallization steps. To investigate the effectiveness of plasma passivation, some samples were treated in NH_3 plasma at 300 ^oC after the metallization steps.

To illustrate the impacts of using the NW channels on device performance, control devices with conventional top-gate and self-aligned S/D structure were also fabricated. These control devices have a 50 nm-thick SPC channel treated with the same SPC conditions as the NW split, and also received a plasma treatment in NH_3 plasma at 300 ^oC for 1 hour.

2.2.3 Formation of poly-Si nanowires

The pictures taken by transmission electron microscopy (TEM) after channel formation are shown in Fig. 2-4. In Fig. 2-4(a), it can be clearly seen that the location of the NW channel is on the sidewall of the gate. The width and thickness of the NW can be characterized in Fig. 2-4(b), which are 21 and 23nm, respectively. Since the device adopts side-gate scheme, the width of the NW represents the width of the conduction channel.

The size and shape of the spacer-like NW are determined by the following process parameters: thickness of the poly-Si gate, thickness of the deposited channel layer, time of etch, and recipe of the etcher (RIE). All four must be adjusted properly to obtain the desirable size of NW. The cross-sectional TEM view of the NW consisted of 200nm thick gate and 100nm thick channel layer is shown in Fig. 2-5. The etching recipe in this case is mainly

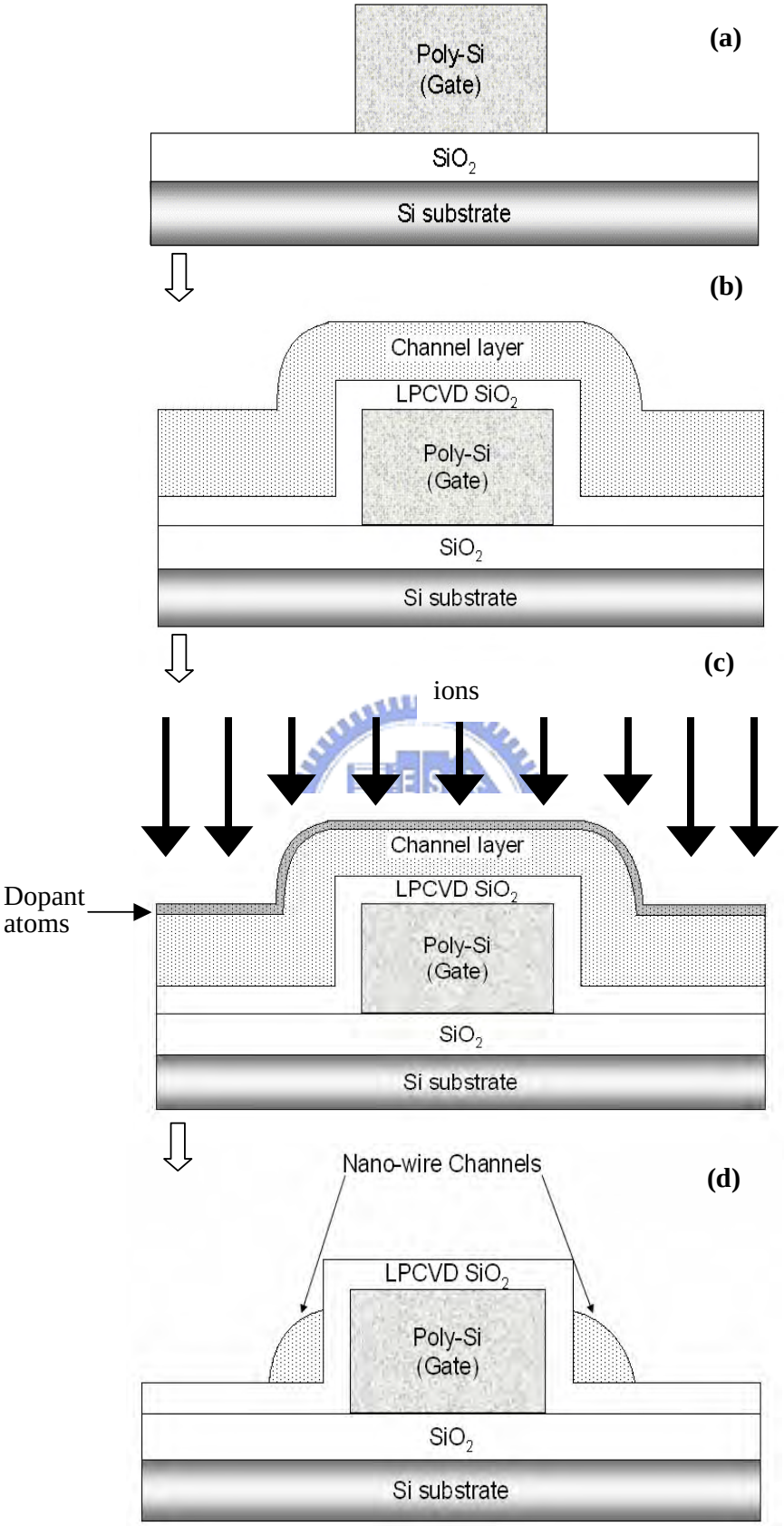


Fig. 2-3 Key processing steps for fabricating NWTFTs.

constructed by a break-through etch, a main etch (ME) with end-point detection, and an over etch (OE) of 60 seconds.The detail of the recipe is listed in Table 2-I. The resultant width and thickness of the NW are 174nm and 107nm, respectively. Although the shape in this case is rounded, the size of nanowire is still too large to meet the requirement (width < 100nm).

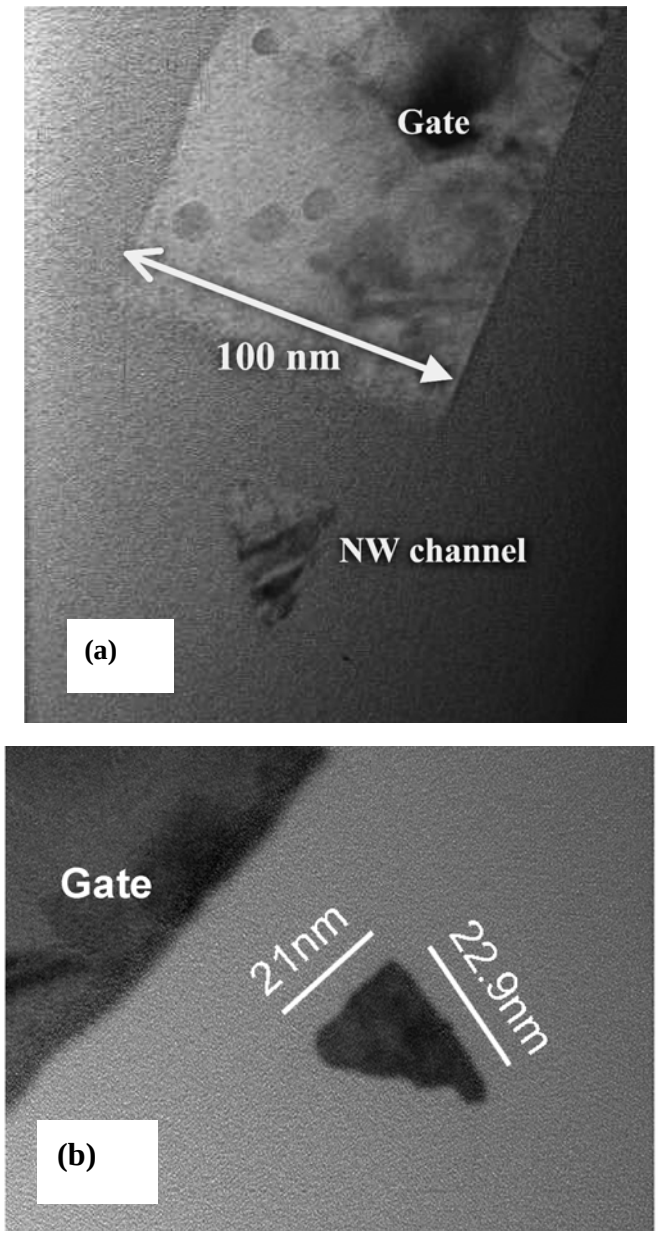


Fig. 2-4 The cross-sectional view of NWTFTs taken by transmission electron microscopy (TEM). The deposited gate and the channel layer thicknesses are 100nm and 100nm, respectively.

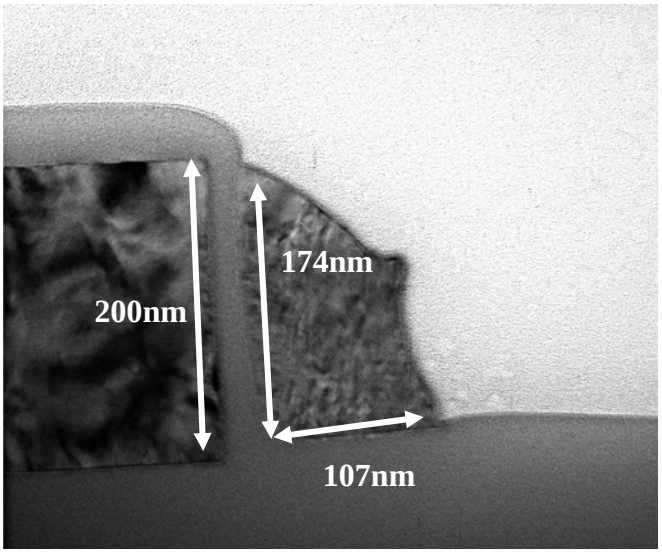


Fig. 2-5 Cross-sectional view of NW consisted of 200nm thick gate and 100nm channel layer.

Etching step	Pressure (mTorr)	RF Top power (W)	RF Bottom power (W)	Gas flow (sccm)	Time (sec)
Break-through	5	250	200	Cl_2: 80	4
Main etch (ME)	17	160	33	Cl_2: 22 O_2: 1.5 HBr: 165	End-point detection
Over etch (OE)	25	250	33	O_2: 2 HBr: 150	

Table 2-I Details of the etching recipe during NW formation.

Samples with 100nm thick gate and 50nm thick channel layer are also fabricated. Owing to etching rate, the etching recipe is mainly constructed by a break-through etch and an over etch of 25 seconds. The resultant NW is shown in Fig. 2-6. The width and thickness of the NW in this case are 35nm and 34nm, respectively.

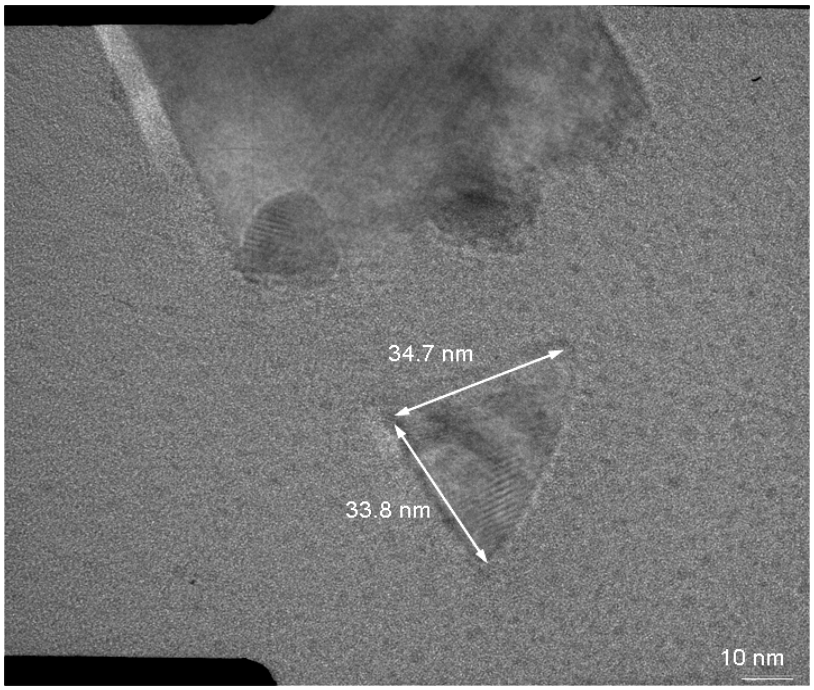


Fig. 2-6 Cross-sectional view of NW with 100nm thick gate and 50nm channel layer.

Since the time of main etch is controlled by end-point detection, over-etch time is used for NW size control. Several over-etch time are tested to determine the relationship between the over-etch time and the NW size. Samples with 100nm thick gate and 100nm thick channel layer are used in this experiment. The measured width and thickness of NW as a function of the OE time is illustrated in Fig. 2-7. Both NW thickness and width decrease with OE time. The results indicate that structural parameters of NW devices could be controlled reasonably. In other words, by carefully controlling the thickness of deposited film and the over-etch time, the structure can be easily shrunk into nano-scale regime.

2.3 On-state Characteristics of nanowire TFTs

Electrical characteristics of the fabricated nanowire TFTs are mainly characterized by the automated measurement setup constructed by an Aglient^{TM} 4156A semiconductor parameter analyzer and Interactive Characterization Software (ICS) software.

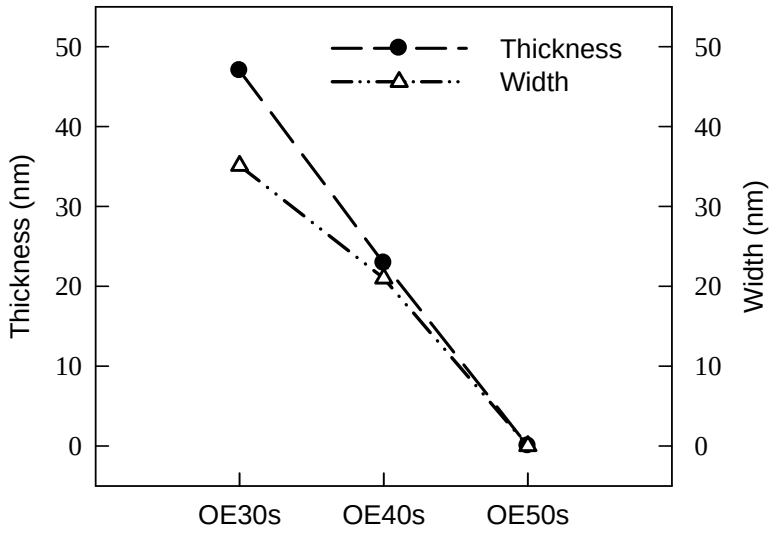


Fig. 2-7 Measured width and thickness of the NW as a function of the OE time.

2.3.1 Characteristics of as-fabricated nanowire TFTs

"As-fabricated" devices mean that the devices received no post-metal treatment such as NH_3-plasma or H_2/N_2 mixed anneal. Subthreshold and output characteristics of a typical poly-Si NW TFT device are shown in Fig. 2-8 and Fig. 2-9, respectively. In this example, the height of n^+ poly-Si electrode is 100 nm, while the thickness of deposited Si layer and gate oxide are 100 and 30 nm, respectively. As can be seen in Fig. 2-8 and Fig. 2-9, good device performance with high on/off current ratio (around 10^5) and reasonable subthreshold swing (around 400 mV/decade) are achieved, even though the channel material quality and device structure are not optimized. The leakage current is rather high, presumably related to the process-induced damage during plasma etching and the gate-induced-drain-leakage (GIDL) occurred at the gate-to-drain overlap region. The mechanism and reduction of the leakage current will be discussed in Chapter 3.

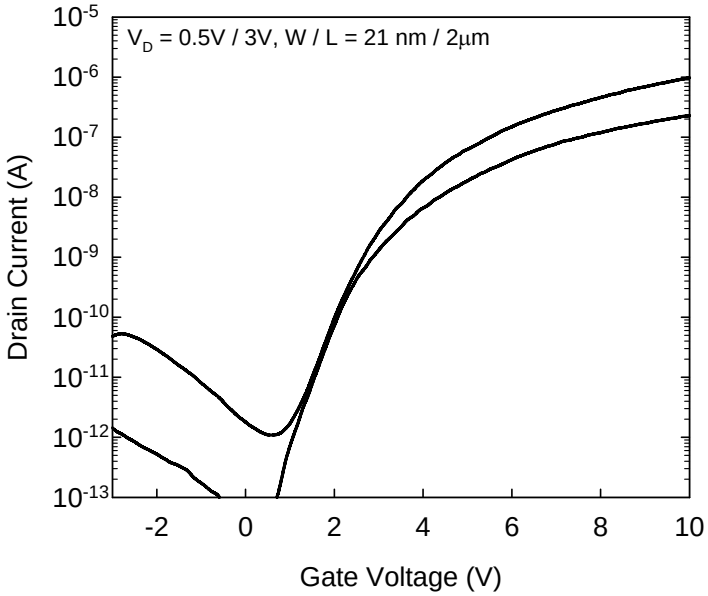


Fig. 2-8 Subthreshold characteristics of an as-fabricated NWTFT.

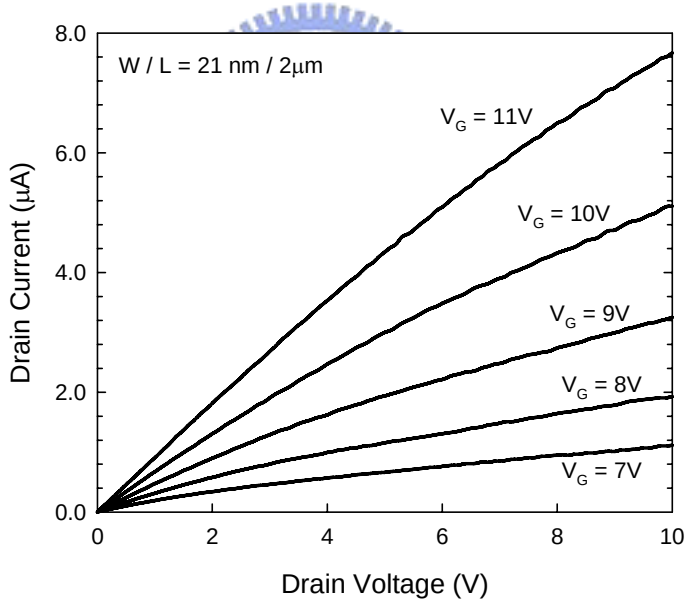


Fig. 2-9 Output characteristics of an as-fabricated NWTFT.

2.3.2 Effects of post-metal treatment

Post-metal hydrogenation has been reported to effectively reduce both the deep and tail states [2.18], and consequently enhance the performance of TFTs. Owing to the abundant grain boundaries and defects in TFTs, the effect of post-metal treatment in TFTs is more

important than that in MOSFETs. In recent years, plasma treatments in hydrogen ambient and other ambient such as deuterium [2.19], N_2/H_2 [2.20], or NH_3 [2.21] have been investigated. The diffused hydrogen and nitrogen species have been reported to effectively passivate the dangling bonds, traps, and defects at grain boundaries and oxide/channel interface [2.22]. As a result, the device performance of TFTs improves, including better subthreshold characteristics, higher on/off current ratio, and lower barrier potential in the grain boundaries.

To investigate the effect of post-metal treatment, the aforementioned "as-fabricated" devices were put under different ambients. In this work, both forming gas annealing (denoted as FG) in furnace and NH_3 plasma treatment in PECVD were employed. For those which were annealed in forming gas, the devices were exposed in N_2/H_2 ambient at 400ºC for 30 minutes. For those which received plasma treatments, the devices were put in NH_3 ambient at 300ºC, and exposed under a RF plasma of 200 watt for either 1 or 2 hours.

Transfer characteristics of the samples which received different post-metal treatment are shown in Fig. 2-10. The width of NWs characterized in this experiment is 35nm. It can be clearly seen that the samples which received forming gas annealing exhibit only slightly better subthreshold swing, larger on-state current, and lower off-state leakage. Compared with FG annealing, dramatic improvement in device performance in terms of drastically reduced threshold voltage, steeper subthreshold slope, higher on-state current, and reduced leakage, is achieved with the plasma treatment. This is because the plasma can generate more excited hydrogen species, and provide more energy needed in diffusion and passivation. More defects will therefore be passivated, resulting in device performance improvement.

The major performance parameters for the aforementioned NWTFTs are listed in Table 2-II . On and off current used to calculate on/off current ratio are defined as the current at V_G=10V, V_D=0.5V and V_G= -3V, V_D=0.5V, respectively.

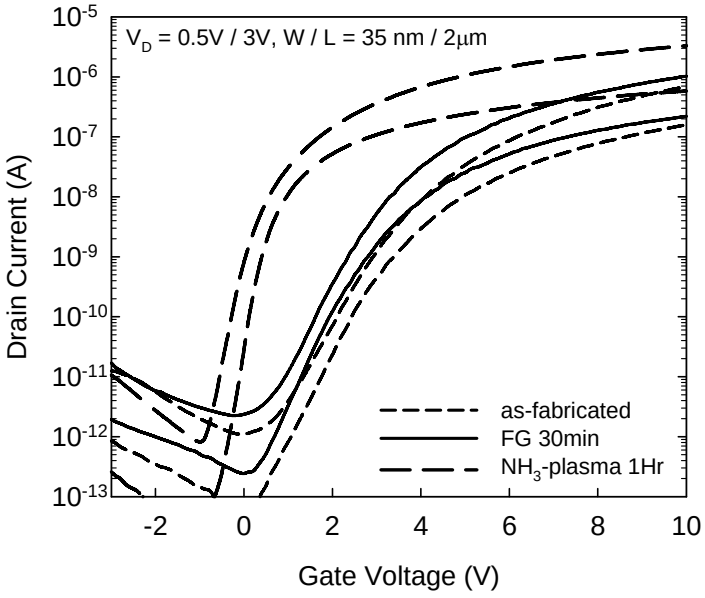


Fig. 2-10 Subthreshold characteristics of NWTFTs which received different post-metal treatment.

	Vth (V)	SS (mV/dec)	Mobility (cm2V-1s-1)	On/off current ratio
As-fabricated	7.19	637	24	$1.85x10^5$
Forming gas 30min	5.97	611	28	$1.12x10^5$
NH_3-plasma 1Hr	3.27	259	40	$2.24x10^6$
W / L = 2x35nm / 2μm, Tox = 30nm, Ioff : I_D @ V_G = -3V				

Table 2-II Major performance parameters for NWTFTs which received different post-metal treatments.

Samples which received longer NH_3 plasma treatments were also investigated. Transfer characteristics of NWTFTs which received different duration of NH_3 plasma treatment are shown in Fig. 2-11. It can be seen that samples which received longer (e.g., 2-hours) treatment exhibit larger improvement on off-state leakage. The major performance parameters for the aforementioned NWTFTs are listed in Table 2-III.

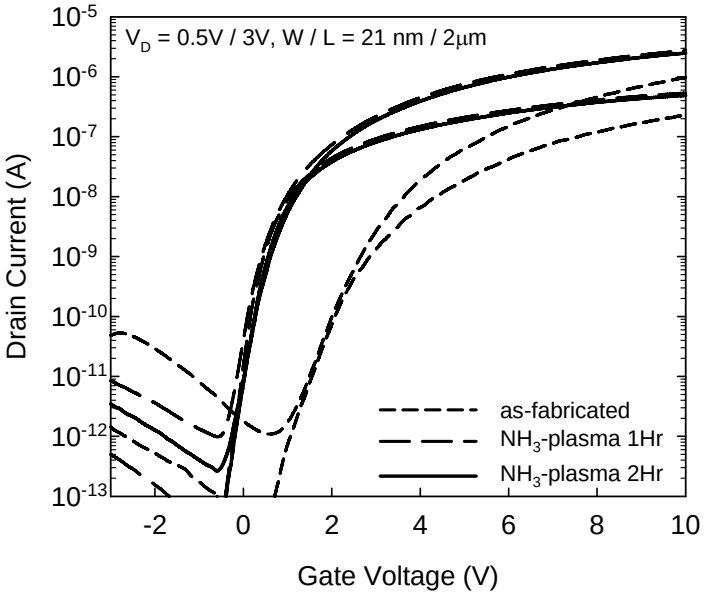


Fig. 2-11 Subthreshold characteristics of NWTFTs which received longer treatment.

	Vth (V)	SS (mV/dec)	Mobility (cm2V-1s-1)	On/off current ratio
As-fabricated	7.27	431	55	$4.02x10^5$
NH_3-plasma 1Hr	2.29	203	63	$1.07x10^6$
NH_3-plasma 2Hr	2.09	180	62	$5.56x10^6$
W / L = 2x21nm / 2μm, Tox = 30nm, Ioff : I_D @ V_G = -3V				

Table 2-III Major performance parameters for NWTFTs which received different duration of plasma treatment.

2.3.3 Effects of geometric parameters of the nanowire channel

As mentioned before, the size of nanowire channel can be controlled by over-etch time.

Unlike the conventional planar self-aligned counterpart where channel width only affects on-current, the size of the nanowire will influence electric characteristics in many aspects. This is owing to the edge effect of nanowire channel. In this section, impacts of geometric parameters of nanowire channel on electrical characteristics will be investigated.

The transfer (subthreshold) and output characteristics of the NWTFTs with different channel width are shown in Fig. 2-12 and Fig. 2-13, respectively. In Fig. 2-12, it can be clearly seen that the NWTFT with W=21nm shows better electrical characteristics, including steeper subthreshold slope, higher on-state current, and lower off-state leakage current, compared with NWTFT with W=35nm. This could be ascribed to the better gate controllability and the fringing electrical field contributed by the edge of nanowire channel. The detailed explanation of the edge effect and the comparison between nanowire and conventional planar structure will be discussed in the next section.

As shown in Fig. 2-13, it is interesting to note that the NWTFT with W=21nm possesses higher output current than the NWTFT with W=35nm. The threshold voltage difference owing to the steeper subthreshold slope may be the major cause. Since the NWTFT with W=21nm possesses lower threshold voltage, its output current will be larger from the well-known fundamental equation, in which the drain current can be expressed as:

$$I_D = \mu_n C_{OX} \frac{W}{L} (V_G - V_{TH})^2 \qquad \text{Eq. 2-1}$$

The extracted data in Table 2-II and Table 2-III also indicate that the mobility of the sample with W=21nm is higher than the sample with of W=35nm. This also contributes to the output-current enhancement.

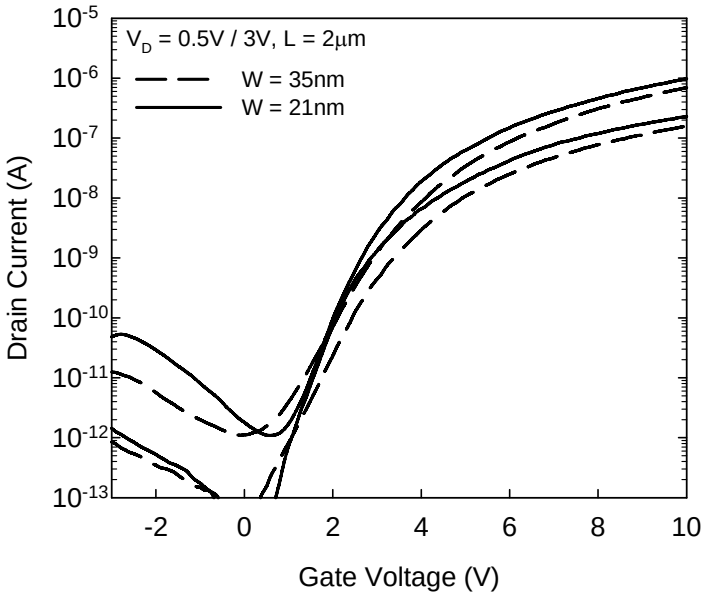


Fig. 2-12 Subthreshold characteristics of NWTFTs with different channel width.

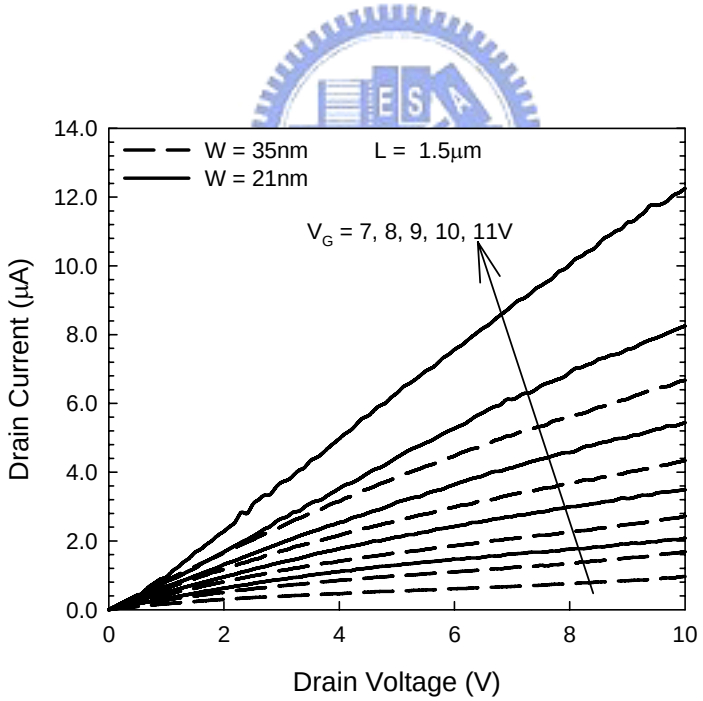


Fig. 2-13 Output characteristics of NWTFTs with different channel width.

The effect of channel length is also investigated. In our experiments, NWTFTs with channel length ranging from 0.8μm to 5μm are used to study long and short channel effects, respectively. Figure 2-14 depicts subthreshold characteristics of NWTFTs with two extremes

of the channel: L=0.8μm and L=5.0μm. It is seen that NWTFTs with the shortest channel suffer from short channel effects. Drain-induced-barrier-lowing (DIBL) and threshold-voltage-roll-off are both observed. Because the gate controllability is attenuated by the electric field of drain, the short channel devices are more difficult to turn off when the gate is biased near zero volt, resulting in a larger minima drain current (Imin) compared with the long channel counterparts.

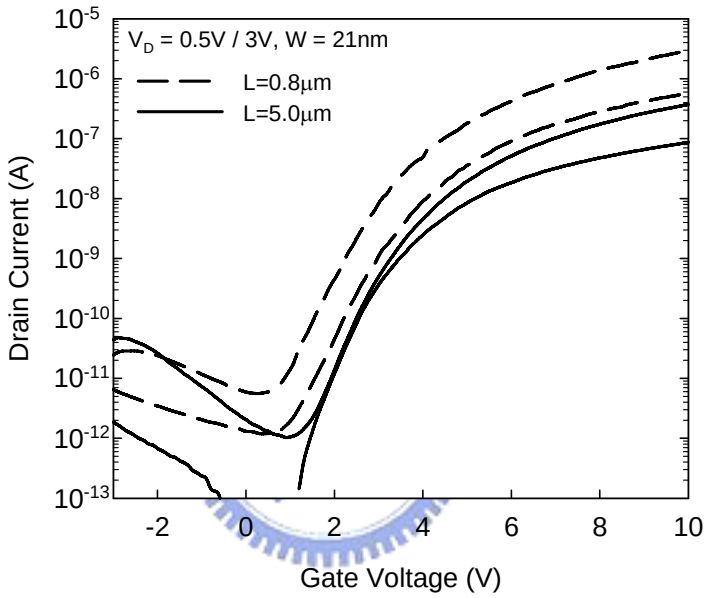


Fig. 2-14 Subthreshold characteristics of NWTFTs with different channel length.

The lost of the gate controllability in short channel devices can be easily observed when operating in ($V_D > V_G - V_{TH}$) in output characteristics. As shown in Fig. 2-15, the drain current in the devices with L=0.8μm does not saturate.

Threshold voltage (Vth) and drain current (Id) of the fabricated devices as a function of channel length (L) are shown in Fig. 2-16 and Fig. 2-17, respectively. The number of devices characterized under each condition is 50. The on-state current in Fig. 2-17 were measured at V_G=10V and V_D=3V. As can be seen in Fig. 2-16, plasma treatment results in

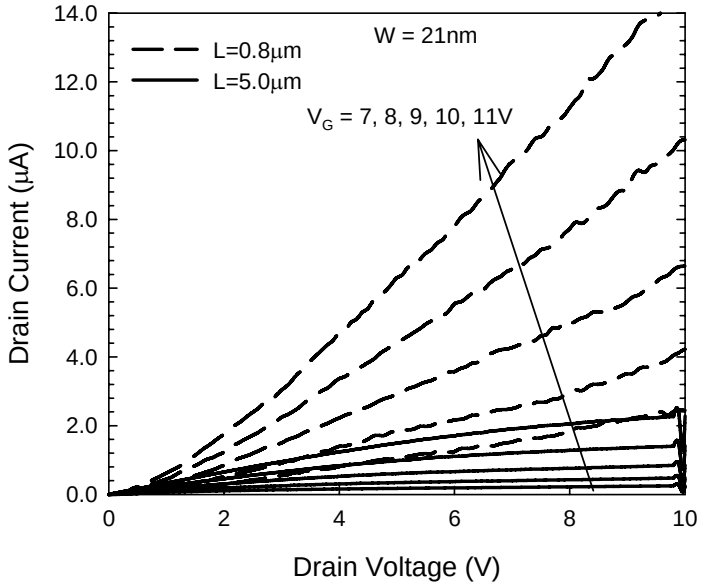


Fig. 2-15 Output characteristics of NWTFTs with different channel length.

a significant reduction in threshold voltage, indicating an effective passivation of the traps contained in the channel after treatment. Fluctuation in these parameters becomes more obvious as the channel becomes shorter. This is reasonable and is related to the inherent grain structure contained in the channels [2.23]. As the channel dimensions approach the grain size, the variation in the number of grain boundaries would greatly affect the device performance, resulting in larger fluctuation of device characteristics.

On the other hand, on-state current increases reasonably with decreasing channel length, as shown in Fig. 2-17. After plasma treatment, on-state current is dramatically improved. This is due to the reduction of threshold voltage as well as improved mobility after passivation, which is consistent with the transfer characteristics shown in Fig. 2-10 and Fig. 2-11.

2.3.4 Features of TFTs in nano-scale regime

In spite of the physics in nano-scale regime, electrical characteristics of NWTFTs are also different than those of conventional planar structures.

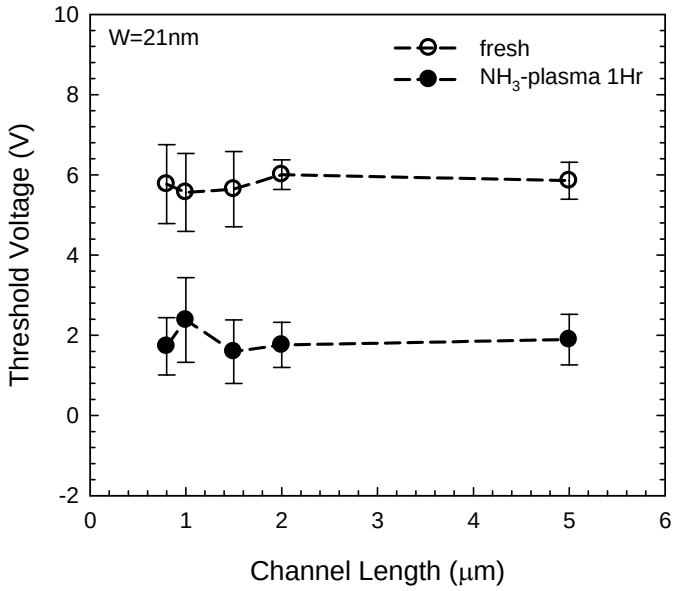


Fig. 2-16 Threshold voltage (Vth) as a function of channel length for NWTFTs with and without plasma treatment.

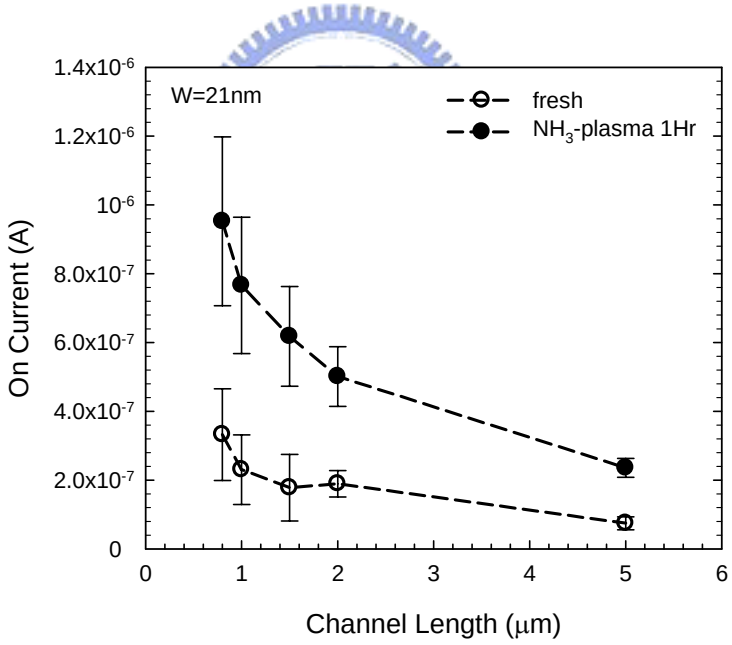


Fig. 2-17 On-state current as a function of channel length for NWTFTs with and without plasma treatment.

Figure 2-18 compares the threshold voltage of NWTFTs with that of conventional planar self-aligned structure, as a function of channel length. Channel thickness of reference devices (i.e., conventional planar self-aligned structure) is 50 nm. The channel width is 20 μm for reference devices and 21 nm for the NW TFTs. These devices received a treatment in NH_3

plasma for 1 hour. The number of devices characterized for each condition is 20. As can be seen in the figure, threshold voltage roll-off is evident for the control split as channel length is shorter than 2 μm, while the NWTFTs exhibit only weak dependence on channel length. This comparison reflects the high surface-to-volume-ratio feature of nanowires mentioned above which tends to enhance gate controllability. As the source-to-drain leakage current via the body of the channel is effectively suppressed in NW devices by thinning NW thickness, good control over short-channel effect could also be achieved.

To more clearly illustrate the impact of using NWs as channel, Fig. 2-19 depicts the subthreshold characteristics of devices with various channel width. Note that the drive current has been normalized to channel width. The results indicate that the shrinkage of channel

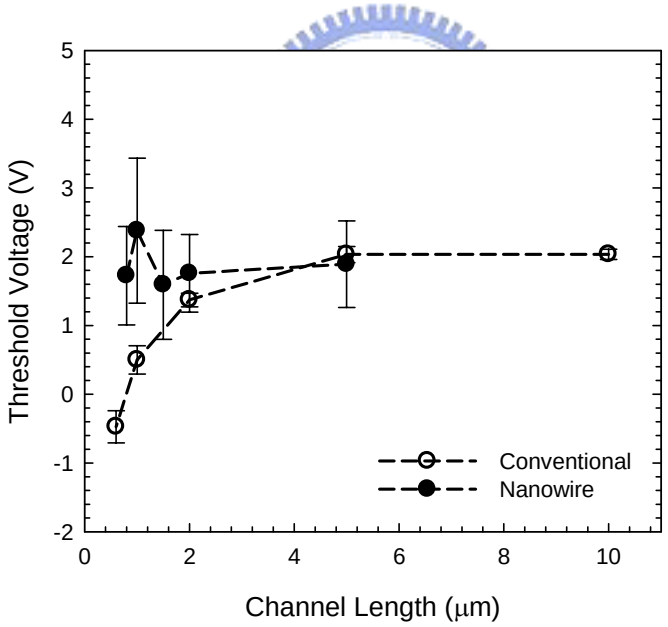


Fig. 2-18 Threshold voltage as a function of channel length for reference and NW devices.

dimensions could help improve device performances in terms of higher on-current and steeper subthreshold slope. To help understand this impact, we use the illustrations shown in Fig. 2-20 to analyze the geometry difference of the proposed NW with that of conventional planar structure. Here the cross-section of the NW is assumed to have a triangular shape with an area

of 1/2(W_{NW} • T_{NW}), as shown in Fig. 2-20(a), where W_{NW} and T_{NW} are the NW width and thickness, respectively. The nominal channel area under the gate control (denoted as gate area for short) is L • W_{NW}, thus the gate area-to-NW volume ratio is $2/T_{NW}$. On the other hand, the gate area-to-channel volume ratio is 1/T for the planar structure, where T is the channel thickness, as shown in Fig. 2-20(b). The NW structures characterized in Fig. 2-18 and Fig. 2-19 are with T_{NW} of 23 nm, much thinner than the channel thickness of the planar devices (50 nm). This well explains the trends shown in the figures. Besides, the fringing field originating from the gate voltage could increase the effective channel conduction width, further enhancing the gate controllability of the NW devices.

Figure 2-21 depicts the drive current of planar SA and NW devices as a function of channel width. Channel length of the devices characterized in this figure is 2 μm. The dependences of channel width on field-effect mobility and subthreshold slope (SS) are illustrated in Fig. 2-22. It is seen that these characteristics are significantly improved as the width is reduced to below 2 μm for planar SA devices. This could be explained by the following two facts: (1) Better passivation effect as channel width is shortened. It has been pointed out previously [2.24] that the passivation species (e.g., hydrogen) diffuse mainly through gate oxide into channel from channel edge. The passivation therefore becomes more effective as channel width is reduced. As a result, the on-state current and mobility could be effectively improved as well. (2) The electric field generating from the gate would induce additional charges at channel edge which in turn could effectively increase the on-current [2.25]. Contribution of the edge component increases with decreasing channel width and becomes significant as the device dimension is scaled into nano-scale regime.

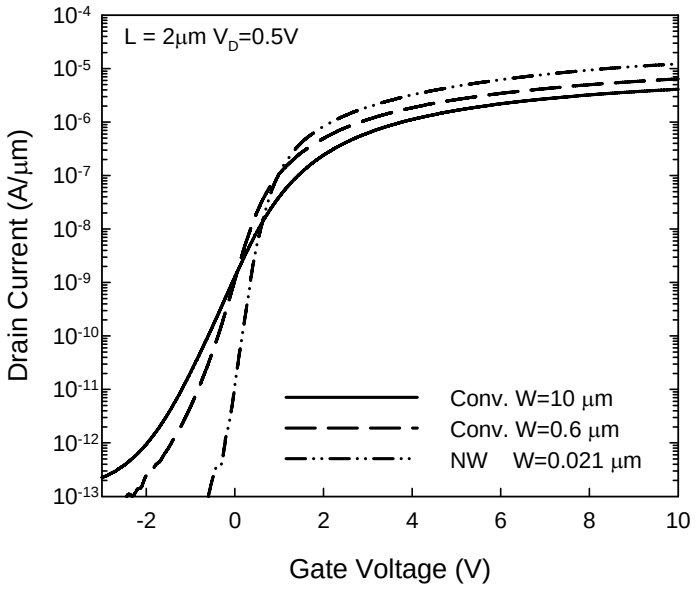


Fig. 2-19 Drain current per unit width as a function of channel width for control and NW TFTs.

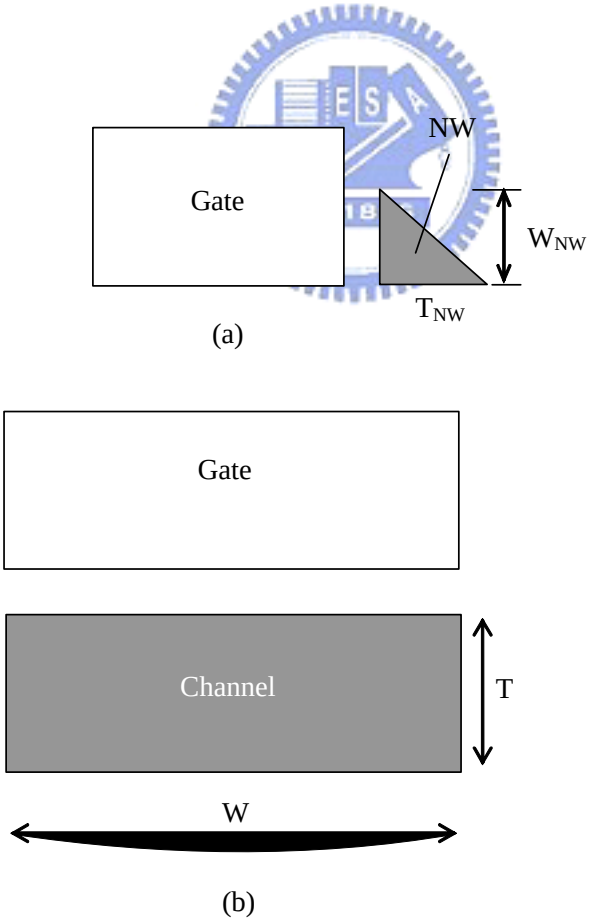


Fig. 2-20 Schematic drawings of the cross-section of (a) the triangle NW and (b) conventional planar structure along the width direction.

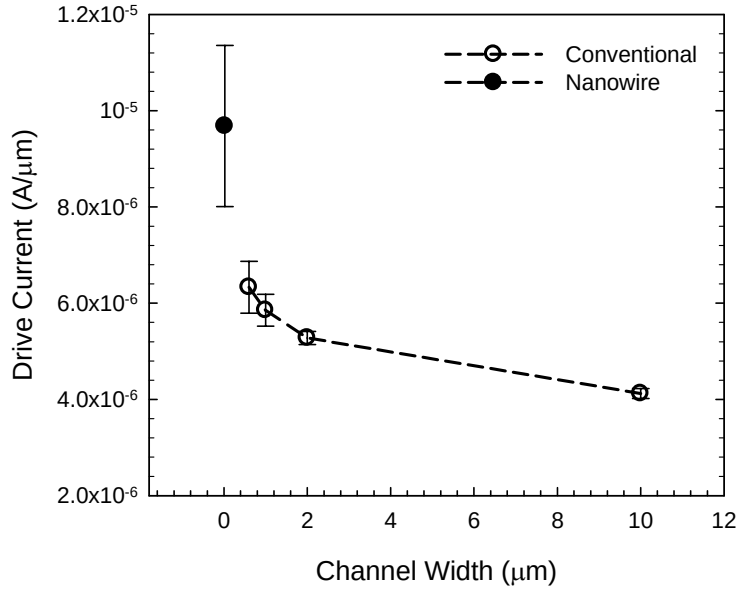


Fig. 2-21 Drive current (normalized to the channel width) as a function of channel width for control and NW devices.

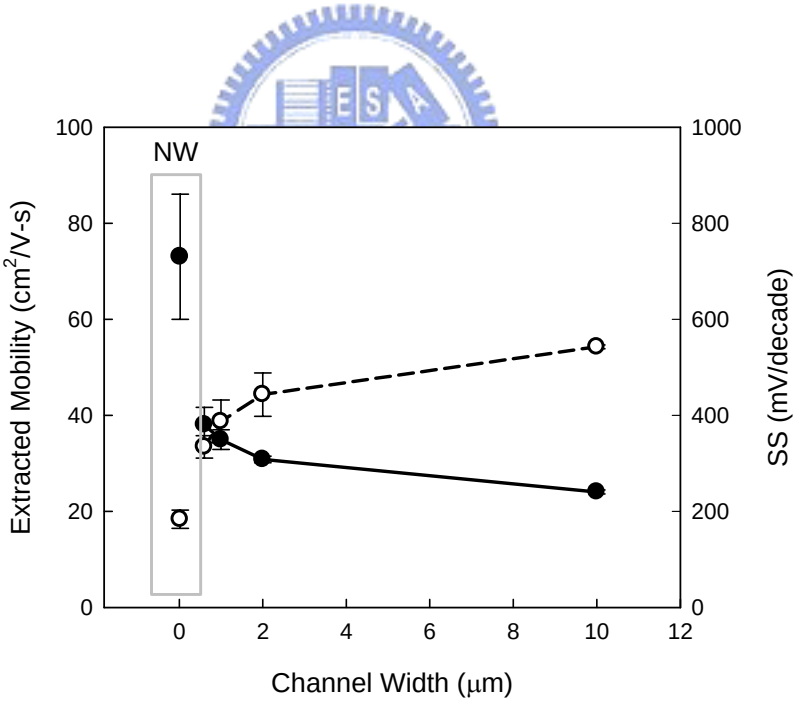


Fig. 2-22 Mobility and subthreshold slope as a function of channel width for control and NW devices.

2.4 Summary

In this chapter, we have investigated the performance of TFTs configured with the novel

poly-Si NW channels formed with SPC method. The fabrication is simple and does not involve costly lithography tools. Such NW structure has been shown to be excellent in terms of on-current per unit width and controllability over short-channel effects. Owing to the fine nano-scale of NW width, the hydrogenation would be very efficient for further performance improvement.

The above results clearly indicate that, despite its simplicity, the proposed method is genuinely robust and suitable to produce devices with excellent performance. As mentioned in Section 2.2.1, the exposure of a significant portion of poly-Si NW channel to the environment leads itself nicely to chemical and biologic sensor applications, since the exposed channel region could serve as the sensing site. For practical applications, an appropriate bias could be applied to the side-gate so that the channel potential could be tuned to a level that is most sensitive to the concentration variation of the target species. This also implies that the complicated channel doping step necessary in conventional NW device fabrications [2.26] could be skipped in our approach. Probably the major concern for our device is the channel crystallinity. This issue could be addressed if advanced Si crystallization techniques, such as metal-induced lateral crystallization (MILC) or excimer laser annealing, are employed. More applications will be addressed in Chapter 7 dealing with suggested future work.

Off-state leakage current is one of the most critical issues for TFTs owing to the abundant defects in grain boundaries. The off-state current of the proposed NWTFT is larger than what we have expected. The major mechanism responsible for the unexpected high off-state leakage of the fabricated devices will be identified and discussed in the next chapter. By proposing several modifications of device structure and process steps, the leakage could be effectively suppressed.

Chapter 3

Off-state Characteristics of Nanowire TFTs

In the preceding chapter, a new nanowire TFT (NWTFT) structure was proposed and demonstrated. Several factors in fabrication process and post-metal treatment have been investigated. The subthreshold and on-state characteristics of NWTFTs were also discussed. Owing to its unique features, the mechanism of off-state leakage current in the proposed NWTFT differs from that in conventional TFTs. The off-state characteristics will be discussed and investigated in this chapter. First, general background about the leakage in TFTs will be introduced in Section 3.1, followed by the explanation and discussion of the leakage mechanism for NWTFTs in Section 3.2. Several process and material modifications for leakage current reduction will be introduced and demonstrated in Section 3.3. The impact of each method will be evaluated in detail. Finally, a short summary is given in Section 3.4.

3.1 Introduction to off-state leakage in TFTs

3.1.1 General background

Like the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) counterparts, the off-state leakage current is a very important issue in the technology development of TFTs. As compared in Fig. 3-1(a) and Fig. 3-1(b), the off-state characteristics of TFTs exhibit much higher drain current than that of MOSFETs. The off-state leakage reduces on/off current ratio, and consumes additional power when devices are turned off. The origin of off-state leakage in TFTs is mainly ascribed to the imperfect channel material, e.g., amorphous or polycrystalline silicon, which is not as perfect as single crystalline silicon. The defects and traps inside the

channel material are responsible for electron-hole pair generation or trap-assisted tunneling, which generate leakage current. Localized electric field and roughness at grain boundaries (GBs) also enhance the generation of leakage current. Many studies have been devoted for identifying mechanisms, establishing methods to measure or analyze the leakage, and proposing methods to reduce the impact of leakage to device performance. Most of them will be introduced in this section.

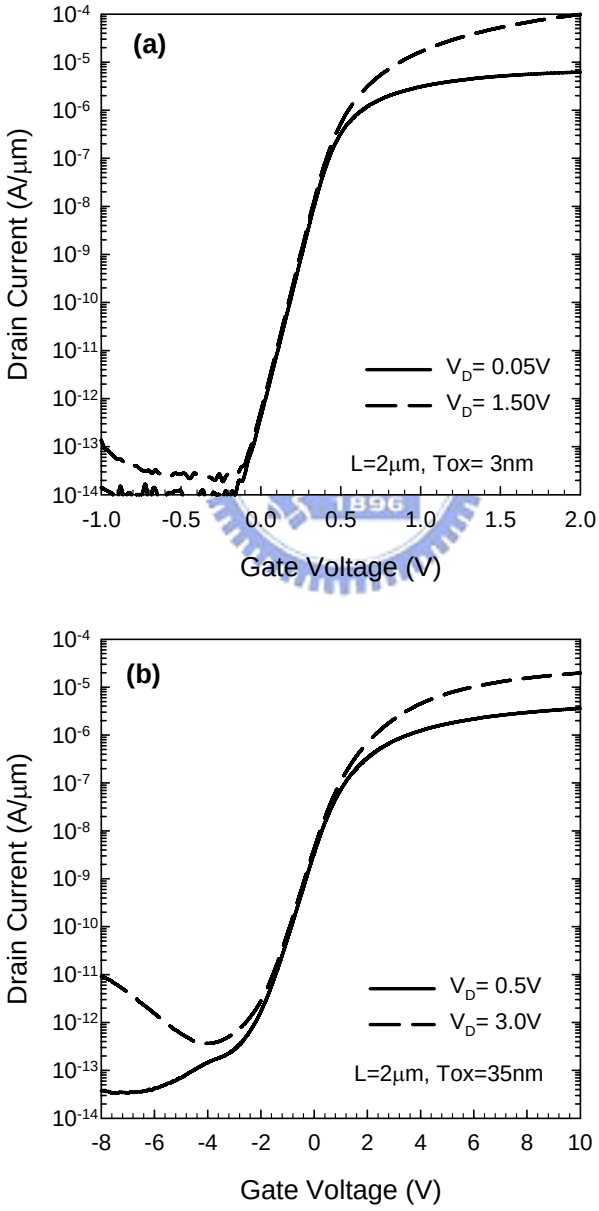


Fig. 3-1 Typical transfer characteristics (I_D-V_G) of (a) MOSFET and (b) TFT device.

3.1.2 Proposed mechanisms for off-state leakage current

Several works have been published in an effort to identify the mechanisms and construct models for off-state characteristics of TFTs. Most of them were based on the leakage mechanisms mutually developed for MOSFET or SOI MOSFET by adding the impact of the traps existing in poly-Si channel material. Resistive current [3.1][3.2], reverse-biased PN junction leakage [3.3], parasitic bipolar effects [3.4], impact ionization in the drain depletion region [3.5][3.6], thermal emission / thermal generation [3.7][3.8], pure field emission/ tunneling [3.2][3.9], and thermionic field emission [3.10][3.11] or Frenkel-Poole emission [3.1], were proposed to explain the behavior of TFTs operating in the off-state.

It should be noted that, under different bias conditions, different mechanisms may dominate. The dominating phenomenon is mainly determined by two factors: The electric field between gate and drain, and the grain boundary trap density near drain. Since the maximum electric field exists at the drain junction when devices are biased at the off-state, the leakage mechanism could hence be qualitatively grouped and explained as a function of gate and drain biases as shown below [3.10]:

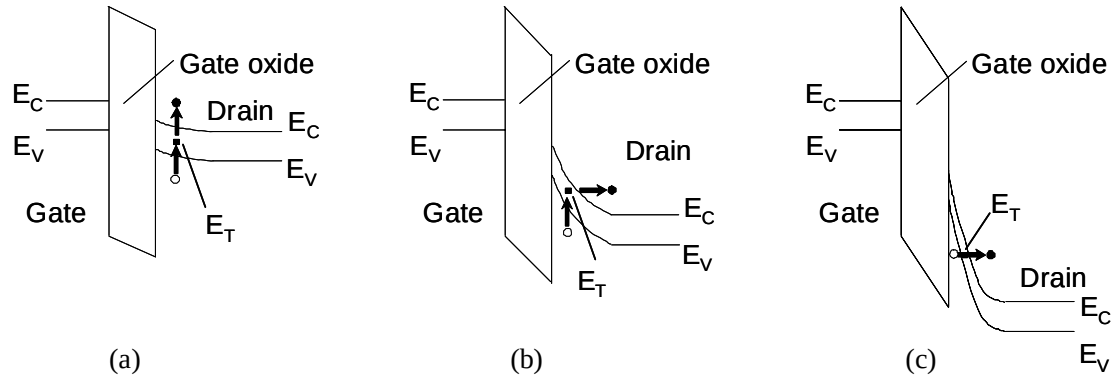


Fig. 3-2 Schematic band diagrams of TFTs under various gate biases.

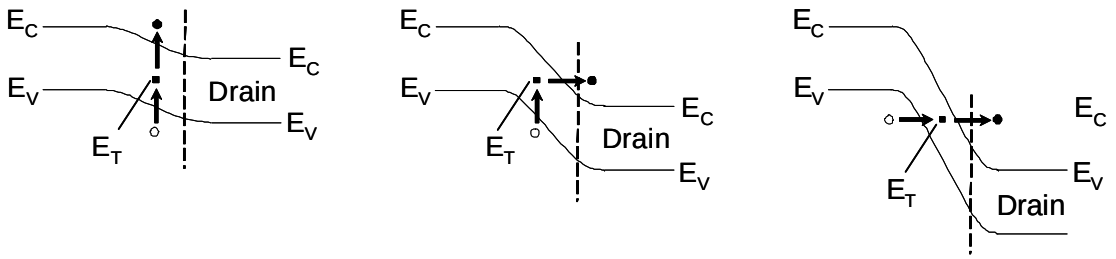


Fig. 3-3 Schematic band diagrams of TFTs under various drain biases.

Under low electric-field regime (Fig. 3-2(a) and Fig. 3-3(a)): The off-state current is mainly dominated by thermal emission via the mid-gap traps located at the grain boundaries. As a consequence the activation energy is about half of the band gap.

Under medium electric-field regime (Fig. 3-2(b) and Fig. 3-3(b)): Electrons in the valence band are thermally activated to the trap states, and then tunnel to the conduction band. This is known as the thermionic field emission.

Under high electric-field regime (Fig. 3-2(c) and Fig. 3-3(c)): Under this situation, quasi Fermi level at the channel/oxide interface shifts toward the conduction-band edge, and band-to-band tunneling takes place easily with the aid of trap states, which may lead to high leakage current in the off-state region and reduced activation energy.

3.1.3 Methods for analyzing off-state leakage current

Since most off-state characteristics of TFTs are determined by the aforementioned factors (traps, temperature, and electric field), when analyzing off-state leakage current, both operating temperature and voltage bias of gate and drain can be used effectively to identify the mechanism responsible for the leakage current. The effect of voltage bias can be directly resolved by current-voltage characteristics, while the effect of temperature can be isolated by characterizing devices under different temperatures.

Activation energy is a crucial method for analyzing the off-state characteristicsof TFTs. It reveals the energy needed to activate the leakage conduction under specific bias conditions. It is based on the assumption that the magnitude of the leakage current is as an exponential function of activation energy and temperature, which can be expressed by the following equation:

$$I_{OFF} = I_0 \exp(-\frac{E_A}{kT}) \qquad \text{Eq. 3-1}$$

Here I_{OFF}, I_0, E_A, k, and T represent the off-state leakage current, intrinsic leakage current which is independent of temperature, activation energy, Boltzmann constant, and temperature, respectively.

To apply this method, device characteristics under different temperatures need to be measured. The activation energies under each bias condition are then extracted by fitting the slope of Arrhenious plot [3.12]. Major steps in extracting activation energy are demonstrated in Fig. 3-4.

3.1.4 Methods for off-state leakage current reduction

Because the off-state leakage current is mainly due to the defects and traps inside poly-Si channel material, the most intuitive method to reduce the leakage is to reduce the defects in poly-Si. This can be achieved by either enhancing the crystallinity during/after poly-Si deposition or passivating the defects/traps via hydrogenation or plasma treatment.

The pursuit of crystallinity enhancement of the poly-Si materials never ceases because mobility is strongly correlated to grain size and quality of poly-Si materials. A lot of techniques have been thoroughly investigated in order to increase grain size and improve grain crystallinity. Poly-Si prepared by recrystallization of amorphous silicon, including solid

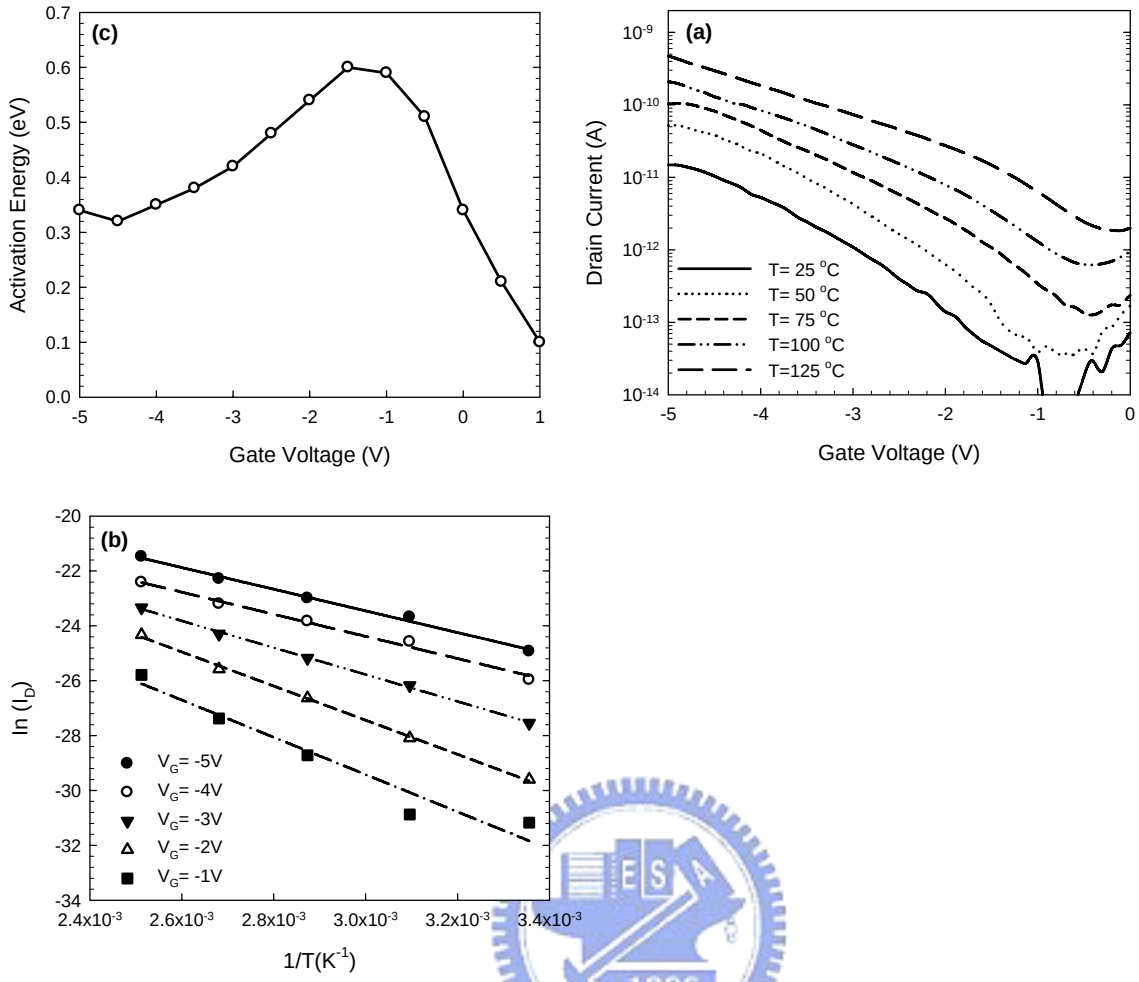


Fig. 3-4 Demonstration of activation energy extraction: (a) measuring off-state drain current under various temperatures, (b) performing Arrhenious plot, and (c) calculating activation energy from the fitted slope in (b).

phase crystallization (SPC), excimer laser annealing (ELA), and metal induced lateral crystallization (MILC), are considered as the main stream in crystallinity enhancement. Among these techniques, the first two are beneficial to the leakage reduction, while MILC does not because of the metal contaminations [3.13]. Another useful method is to anneal the poly-Si material under high temperature (~ 900 ˚C) [3.3]. Although it is impractical for the TFTs used in liquid crystal display (LCD) panels, it can be applied to the TFTs used in SRAM and other applications where high temperature processing (HTP) is tolerable.

Trap states can be effectively reduced by hydrogenation, which passivates the dangling

bonds in poly-Si by diffused hydrogen atoms. The hydrogen atoms and the energy for diffusion and bonding can be provided by several means, such as forming gas annealing [3.14], hydrogen diffusion from a hydrogen-rich capping layer [3.15][3.16] , H^+ implantation plus annealing [3.17][3.18], or plasma treatment [3.19][3.20]. These techniques usually not only reduce the off-state leakage current, but also enhance device performance such as subthreshold swing, on-state current, and field effect mobility. Instead of hydrogen-only ambient [3.8][3.20], many other hydrogen-related gas or combinations have been investigated. In recent years, plasma treatments in other ambient such as N_2/H_2 [3.21], or NH_3 [3.22] are reported to be able to effectively reduce the trap density in poly-Si channel, and consequently reduce the off-state leakage.

In addition to the enhancement in quality of poly-Si/oxide materials, adjustments in device structure were also proposed to reduce the off-state leakage. Lightly doped drain (LDD) structure was introduced to not only MOSFETs but also TFTs [3.23]-[3.25] for suppressing the electric field near the drain junction. It is shown that LDD structure can effectively reduce the off-state leakage current up to four orders of magnitude [3.10], especially when drain voltage is large. More modifications such as gate overlapped lightly doped drain (GOLDD) [3.26], field-induced drain (FID) [3.27], n-p-n gate structure [3.28], amorphous Si buffer structure [3.29], high-k spacer offset-gate [3.30], and air cavity structure [3.31], were also proposed and evaluated.

3.2 Leakage current mechanism in NWTFTs

Special attention is paid to the off-state leakage of NW devices. Since current is proportional to the width of current path (i.e., the cross-sectional area of NW channel), the leakage is originally expected to be low owing to the small cross-sectional area of NW channel. Figure 3-5 shows the comparison of the drain current per unit width between

NWTFTs and conventional TFTs. The off-state current density shown in Fig. 3-5 clearly indicates that the off-state current of NWTFTs is higher than that of conventional devices. Specifically, when the devices are biased under high drain voltage (e.g., V_D=3V), three orders higher off-state current density is observed in NWTFTs. Careful examination has been performed to track down the origin of such high off-state current. The leakage path through gate oxide, which is initially suspected, is ruled out because the measured gate current (I_G) is within the reasonable range of two pico-ampere.

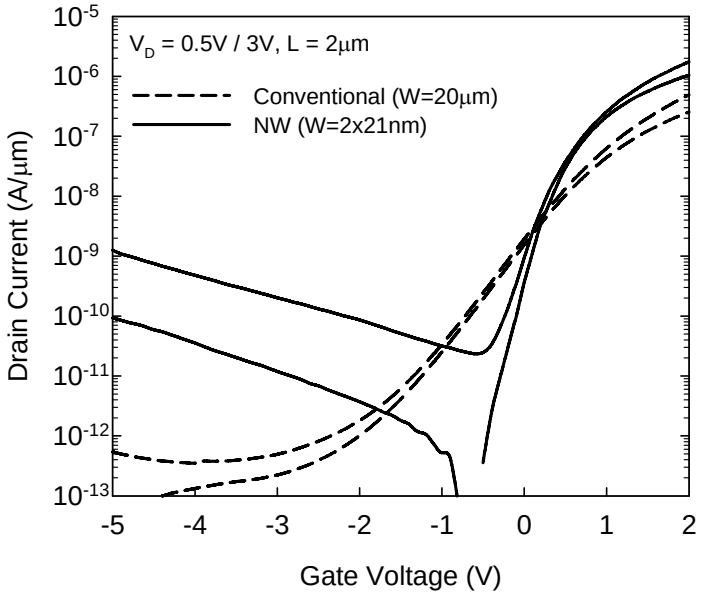


Fig. 3-5 Drain current per unit width of NWTFTs and conventional TFTs.

3.2.1 Origins of off-state leakage current in NWTFTs

After carefully examining and analyzing the device characteristics of different structural parameters, we found that samples with different gate width exhibit drastic difference in off-state characteristics. The gate width (GW) is defined in Fig. 2-2(a), and represents the width of gate electrode. Since the gate width is not related to the conduction path of current, the size of gate electrode should be irrelevant. The dependence of off-state leakage current of

NWTFTs with various GW is shown in Fig. 3-6. The off-state characteristics of NWTFTs, originally expected to be the same, are actually quite different for NWTFTs with different GW. In fact, by extracting the off-state current at V_D = 5V and V_G = -5V, we found that the off-state leakage is actually proportional to gate width (Fig. 3-7).

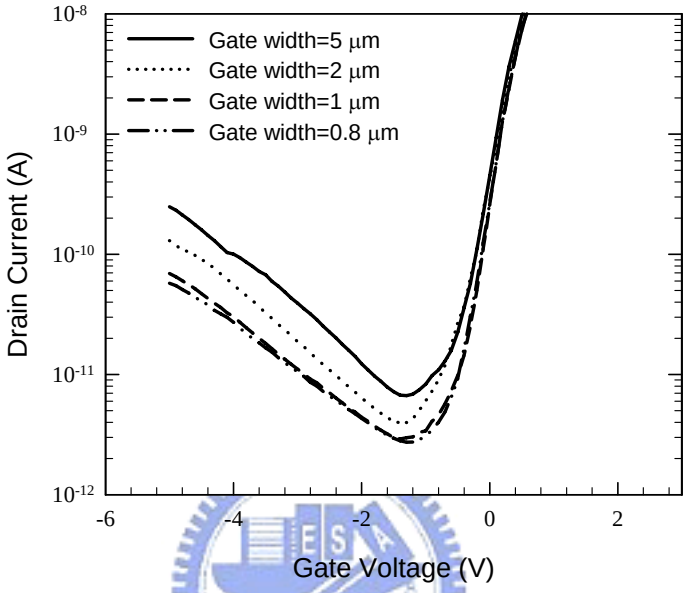


Fig. 3-6 Dependence of off-state leakage current for NWTFTs with different gate width.

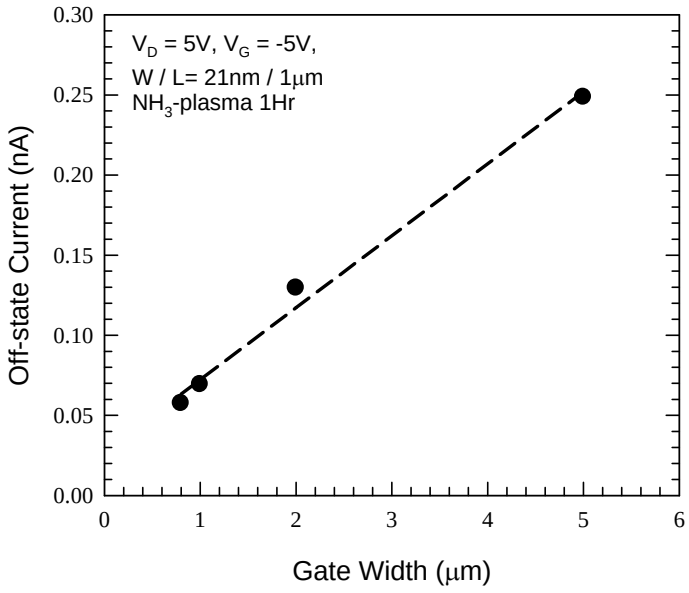


Fig. 3-7 Off-state leakage current of NWTFTs versus gate width.

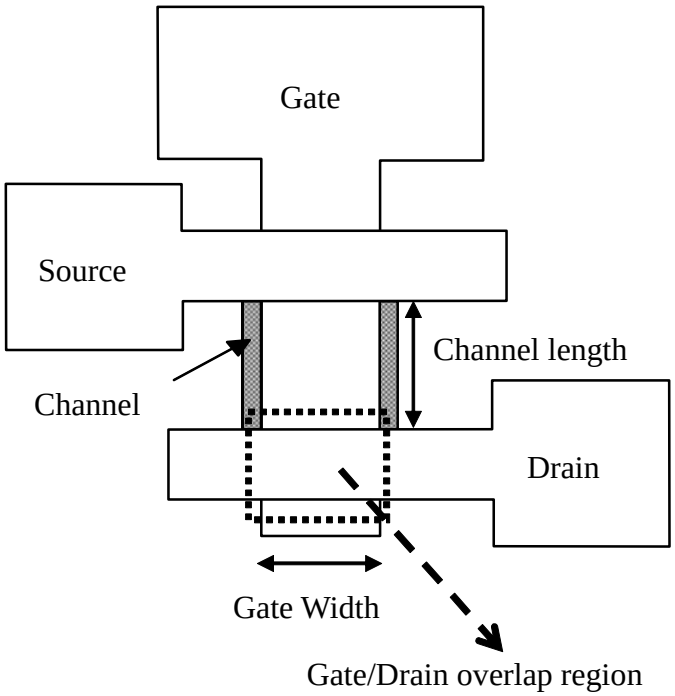


Fig. 3-8 Top view of the gate-to-drain overlap region in the device structure where major leakage current conducts.

From these observations we conclude that the difference of off-state current among the devices shown in Fig. 3-7 is mainly dependent on the area of the top gate-to-drain overlap region shown in Fig. 3-8. Gate-induced drain leakage (GIDL) [3.32] is the most likely cause for the anomalously high off-state current. GIDL current is ascribed to the high field presenting at oxide/drain region due to high V_{GD}. As described in Section 3.1.2, when devices are biased under high electric field, the electric field tends to deplete the drain and eventually leads to (trap-assisted) band-to-band tunneling, which in turn causes high leakage current in the off-state region.

By further looking into the origin of the GIDL current, we found that the origin of the leakage in our NW devices is related to the unique doping profile in drain. As mentioned in Section 2.2.2 (Process of fabrication), the S/D implantation was deliberately performed at a low energy (e.g., 15 keV) to avoid excess dopants being incorporated in NW channels. This results in a gradient dopant distribution in drain region where the dopant concentration

decreases toward oxide/Si interface. This aggravates GIDL current since it is more vulnerable to depletion by the gate bias in off-state.

The activation energy for devices with gate width of 5 and 1 μm were extracted by measuring the I-V characteristics at temperatures ranging from 35 to 125 ºC. The detail about the extraction of activation energy from I-V characteristics has been mentioned in Section 3.1.3. The extracted activation energies are shown in Fig. 3-9. It can be seen that the activation energies are essentially independent of gate width at both V_D=0.5V and V_D=5V, indicating that the same leakage mechanism occurs in the devices.

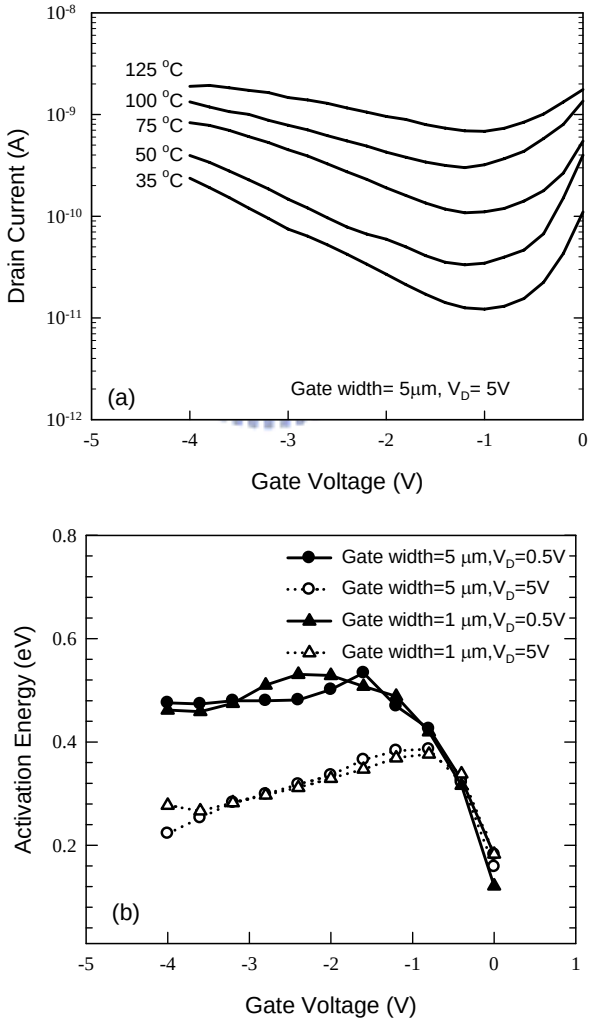


Fig. 3-9 (a) Off-state I-V characteristics of a NWTFT measured at different temperatures. (b) Activation energy of NWTFTs measured at V_D = 0.5 or 5 V as a function of gate voltage.

Also indicated in Fig. 3-9(b), the activation energy is strongly dependent on both gate voltage (x-axis) and drain voltage (V_D=0.5V and V_D=5V), which implies that the off-state leakage current is related to the voltage difference between gate and drain (V_{GD}), or the strength of electric field in the drain near oxide/Si interface. The peak value of the activation energy is about 0.55 eV, which is half of silicon band gap (~1.1eV). The value is consistent with the aforementioned "low electric-field regime" described in Section 3.1.2, which implies that defect states located near the mid-gap (deep states) play as an important role on the off-state leakage.

3.2.2 Effects of post-metal plasma treatment

The off-state characteristics of NWTFTs with and without post-metal plasma treatment in NH_3 ambient are shown in Fig. 3-10. It can be easily seen that after NH_3-plasma treatment, the devices exhibit lower off-state leakage current. This is because some defects are passivated after plasma treatment, thus trap-assisted band-to-band tunneling is suppressed.

The off-state leakage mechanism for sample treated by NH_3 plasma can be also examined by aforementioned technique, by plotting the relationship between off-state current and gate width. As shown in Fig. 3-11, although off-state leakage current is lower after treatment, it is still proportional to gate width. The result indicates that the GIDL current occurring in the drain-and-gate overlap region still plays the primary role.

Figure 3-12 describes the activation energies of NWTFTs with and without post-metal plasma treatment. Similar trend for all curves again confirms that the off-state leakage mechanism is not changed after treatment. The value of the extracted activation energy for plasma-treated samples is however higher than that for as-fabricated devices, which implies that the leakage current is more difficult to generate for plasma-treated samples. The result is also consistent with the off-state characteristics shown in Fig. 3-10 and Fig. 3-11.

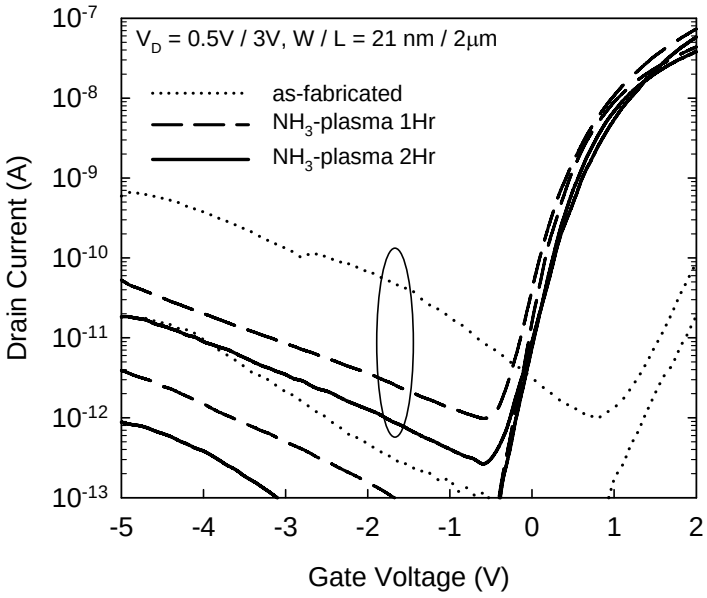


Fig. 3-10 Off-state characteristics of NWTFTs with and without NH_3 plasma treatment.

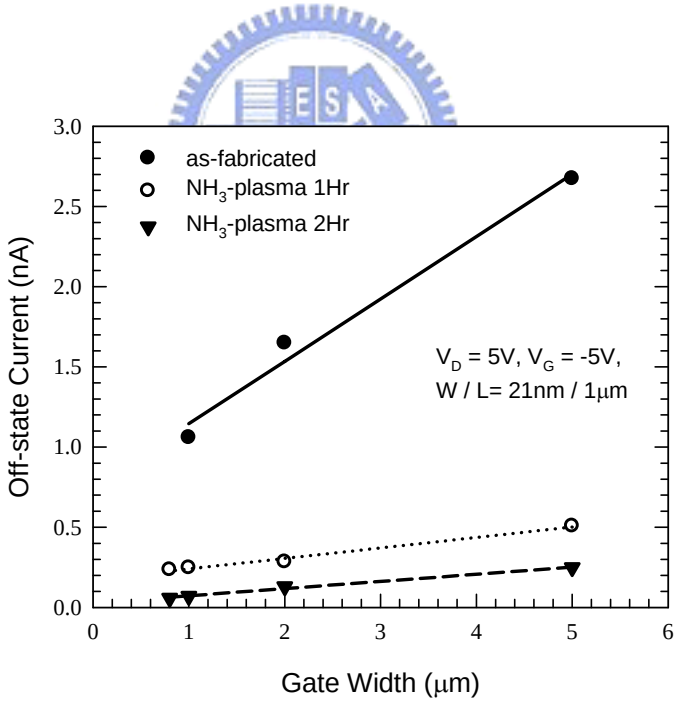


Fig. 3-11 Off-state leakage current of NWTFTs with and without NH_3 plasma treatment as a function of gate width.

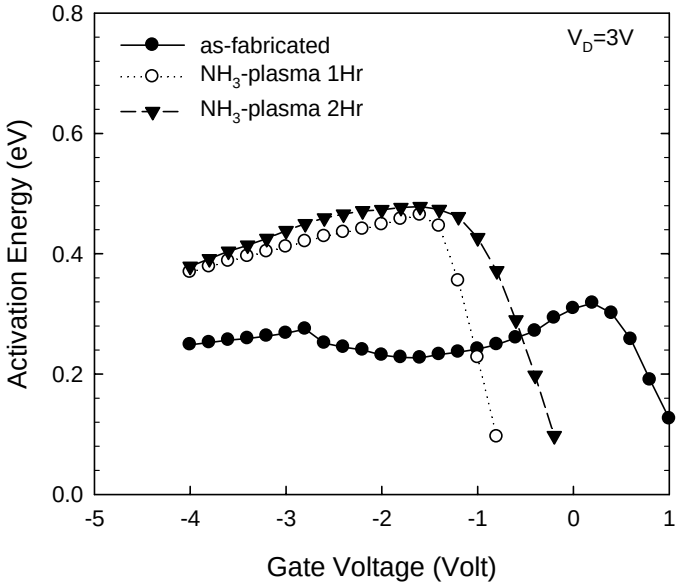


Fig. 3-12 Activation energy of NWTFTs with and without NH_3 plasma treatment as a function of gate voltage.

3.3 Reduction of off-state leakage current in NWTFTs

The off-state leakage current of the fabricated devices has been identified to be due to the GIDL mechanism occurring at the gate-to-drain overlap region. Major factors are the strength of electric field and the dopant concentration at drain/oxide interface, as well as the trap density in channel film.

Several strategies could be used to reduce the off-state leakage: (1) Reduce the area of gate-to-drain overlap region. This is very straightforward and have been demonstrated in sample with narrower gate (GW=0.8μm). This can also be done by redesigning the layout and avoiding the gate-to-drain overlapping. (2) Use of plasma treatment to passivate the traps in the channel. This is evidenced previously by the results shown in Fig. 3-10. (3) Reduce the trap density in poly-Si films through crystallinity enhancement techniques, like excimer-laser-anneal (ELA), metal-induced-lateral-crystallization (MILC), and rapid-thermal-anneal (RTA) methods. (4) Increase the thickness of dielectrics between the

drain and gate at the overlap region. This is a simple way to reduce the field strength and could be easily implemented in device fabrication by simply adding a dielectric hard-mask over the top of the gate. (5) Increase the dopant concentration in drain region near oxide interface by additional anneal treatments or ion-implantation. Note that such anneal should be done after the NW formation to avoid excess incorporation of the dopants into the channel.

3.3.1 Proposed methods for leakage current reduction in NWTFTs

Several process treatments or modified structures were investigated to improve the off-state characteristics of NWTFTs, and are described in the following sections. First, to discuss the effect of film crystallinity, rapid thermal annealing (RTA) technique was employed after channel formation. Devices with an inserted dielectric hard-mask at the gate-to-drain overlap region were also fabricated. Silicon nitride (SiN_X) layer was used in this case as the hard-mask to reduce the electric field between gate and drain. We also fabricated the NWTFTs with silicon germanium ($Si_{1-X}Ge_X$) as channel material. Because of the higher resistance for the current path where GIDL is originated, primary leakage path will shift from the overlap region back to the drain junction. This will change the off-state leakage behavior. The comparison of each method will be performed and discussed in Section 3.3.5. An indicator will also be proposed to evaluate the improvement of each method, by excluding the effect of size difference of NW channel.

3.3.2 Effects of rapid thermal annealing (RTA)

Rapid thermal annealing has been reported to enhance the crystallinity of poly-Si materials [3.33]. Under such high temperature, silicon atoms can rearrange their position, repair broken bonds, and improve grain quality. In our experiment, an additional RTA anneal step was performed at 900ºC for 30 seconds after NW formation. The off-state characteristics

of NWTFTs with an RTA step are shown in Fig. 3-13. Compared with the control samples, the samples with an RTA step exhibit better off-state characteristics by an order of magnitude.

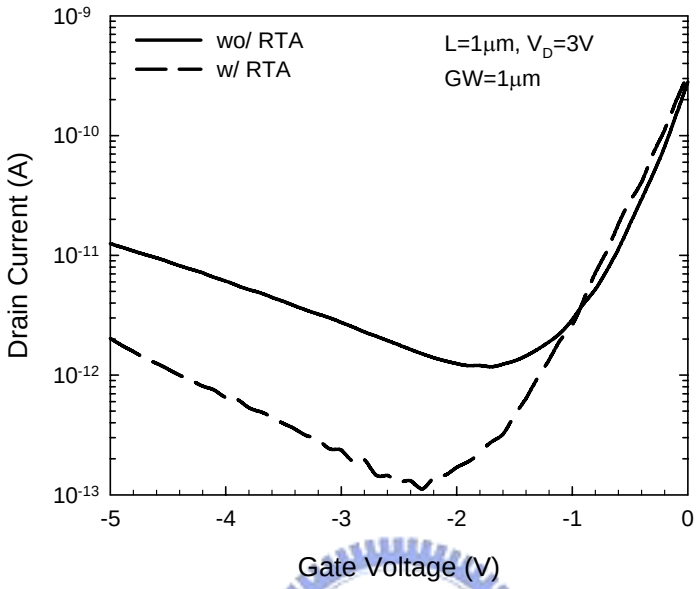


Fig. 3-13 Off-state characteristics of the devices with and without RTA treatment.

To investigate whether the off-state leakage mechanism is changed for the devices with RTA treatment, the off-state leakage current as a function of gate width is plotted in Fig. 3-14. The off-state leakage current for the devices with RTA treatment, albeit lower than that without RTA, still remains proportional to gate width. This implies that the primary leakage mechanism is identical for the devices without RTA treatment. Although RTA lowers the trap density in gate-to-drain overlap region, off-state leakage still originates from the same region.

3.3.3 Effects of additional nitride hard mask in gate/drain overlap region

Since the electric field at the gate-to-drain overlap region dominates the off-state leakage, reducing the electric field by inserting a nitride layer in the overlap region is also proposed.

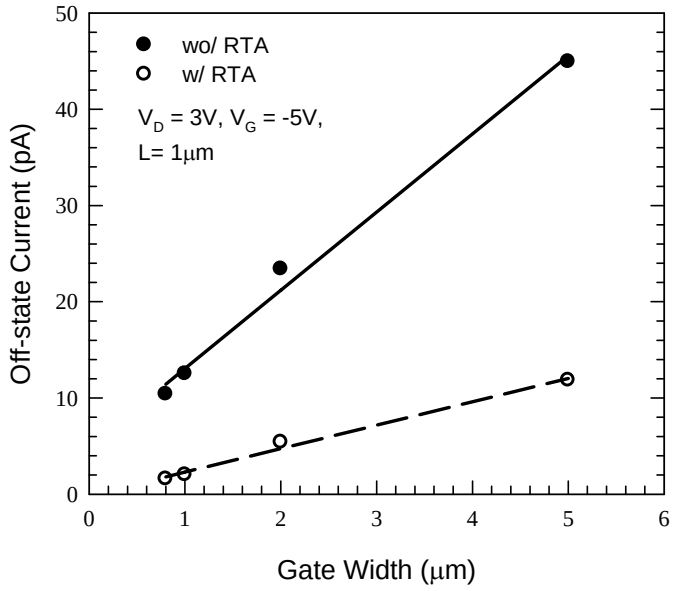


Fig. 3-14 Off-state leakage current of NWTFTs with RTA treatment as a function of gate width.

The schematic view of the modified structure is shown in Fig. 3-15. It can be seen that a layer called “nitride hard mask (HM)” is inserted between the gate and the drain, and hence reduces the electric field. To employ such modifications, the processing steps in the gate formation module must be altered. For the devices embedded with nitride hard mask, an additional LPCVD nitride layer of 100nm thick was deposited right after the deposition of the poly-Si gate layer. The photo-resist used to define the gate is then spun-on and patterned. Afterwards, the nitride layer is etched, followed by the etching of the poly-Si material using the nitride layer as the hard mask. The gate electrode will be carried out after removing the photo-resist. A cross-sectional TEM picture of the NWTFT embedded with nitride hard mask is shown in Fig. 3-16. The existence of nitride can be clearly seen in this figure. It must be noted that the insertion of the nitride HM layer will change the height of side-wall where the NW is located, thus alter the geometric profile of the NW. As can be seen in Fig. 3-16, the width and the thickness of the NW are 125 nm and 72 nm, respectively. More work needs to be done to optimize the profile of the NW. In this thesis, because our attention is focused on

whether the off-state characteristics are improved, the resultant samples are adequate for the analysis.

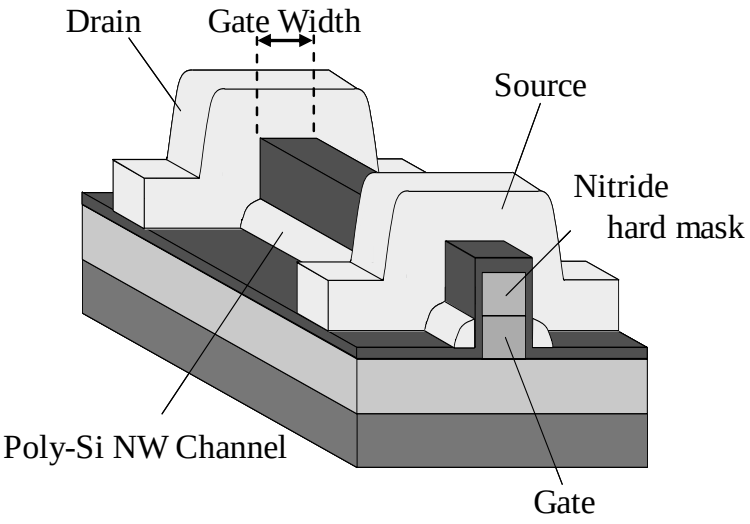


Fig. 3-15 Schematics of the NWTFT with hard mask modification.

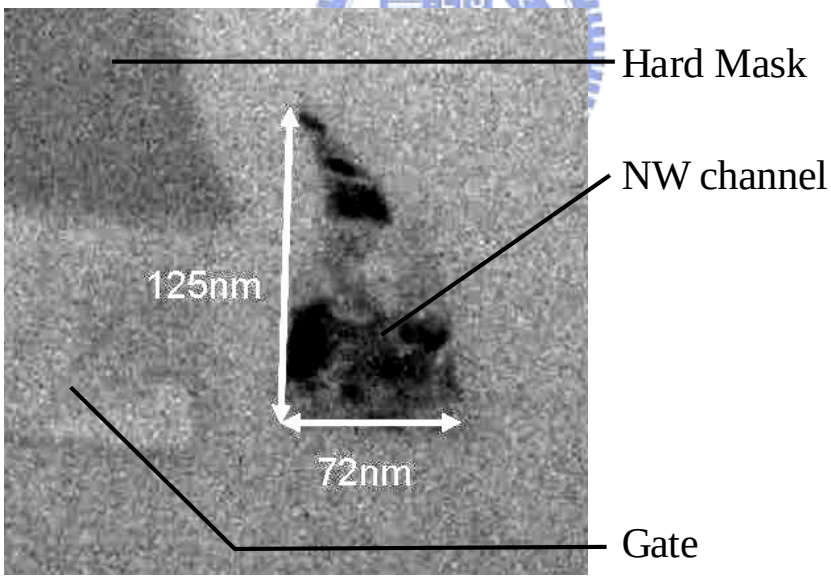


Fig. 3-16 Cross-sectional TEM of the NW-TFT embedded with nitride hard mask.

The off-state characteristics of the devices embedded with hard mask are shown in Fig. 3-17. It appears that the off-state characteristics show very weak dependence on gate width. In other words, the off-state characteristics now are not originated in the gate-to-drain overlap

region. This means that the incorporated nitride layer could significantly reduce the electric field strength in the gate-to-drain overlap region, and thus eliminates the GIDL.

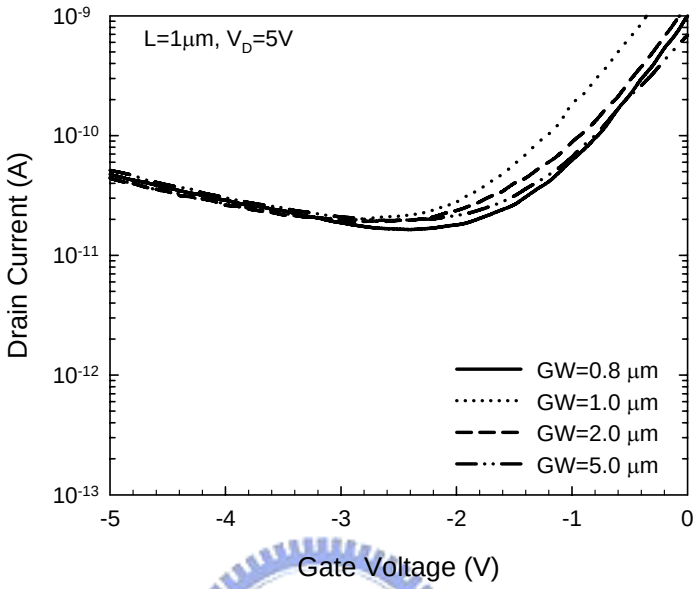


Fig. 3-17 Off-state characteristics of the devices embedded with hard mask.

3.3.4 Effects of $Si_{1-X}Ge_X$ channel material

Samples with $Si_{1-X}Ge_X$ as channel material were also prepared and characterized. Similar results (see Fig. 3-18) to those embedded with nitride hard mask are observed: The off-state characteristics exhibit weak dependence on gate-width. This phenomenon can be ascribed to the higher density of states (DOS) in the $Si_{1-X}Ge_X$ material [3.34]. The higher defect density increases the series resistance of the lightly doped region, and restricts the current spreading in that area.

With the help of the schematics shown in Fig. 3-19, the phenomenon can be further explained. Figure 3-19 depicts the leakage current flows near the drain side. The electron current tends to spread out into the drain region while flowing out from the nanowire channel. In the control device, GIDL current, flows mainly by path A, dominates the off-state leakage.

In the SG device, the high DOS in $Si_{1-X}Ge_X$ material not only significantly increases the resistance of path A, but also decreases the band-bending needed for band-to-band tunneling. This is because in order to enforce band-bending, or shift the Fermi-level inside band gap, the defect states below the Fermi-level must be filled. If the DOS is high, the Fermi-level is hard to shift, thus band-bending is decreased. In the mean time, the higher DOS will generate more electron-hole pairs near the drain junction, which is the dominant leakage current generation in conventional TFTs. Both reasons prohibit path A, so the leakage mainly flows through path B, thus exhibits a weak dependence on GW.

3.3.5 Comparisons and discussion among proposed methods

In this section, we will try to compare the dependence of GIDL on the off-state leakage for all samples employing different modifications. As mentioned before, test devices can be split into four groups, namely, control (denoted as CON), RTA treated (denoted as RTA), hard-masked (denoted as HM), and $Si_{1-X}Ge_X$ channel devices (denoted as SG).

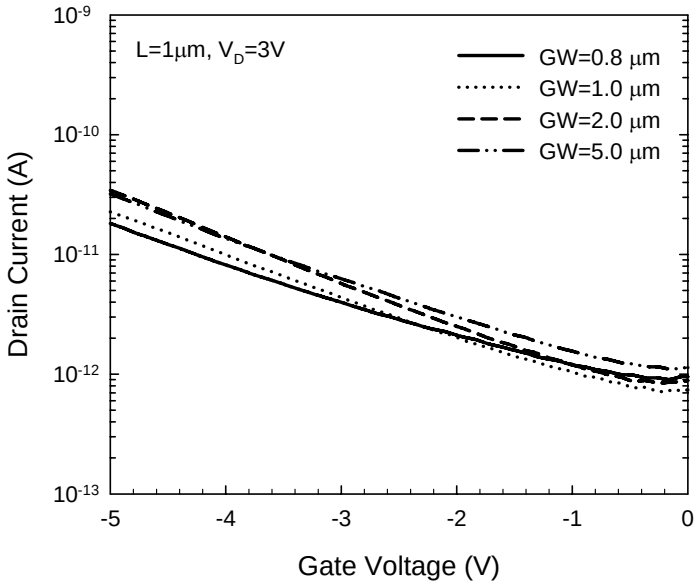


Fig. 3-18 Off-state characteristics of devices with $Si_{1-X}Ge_X$ channels.

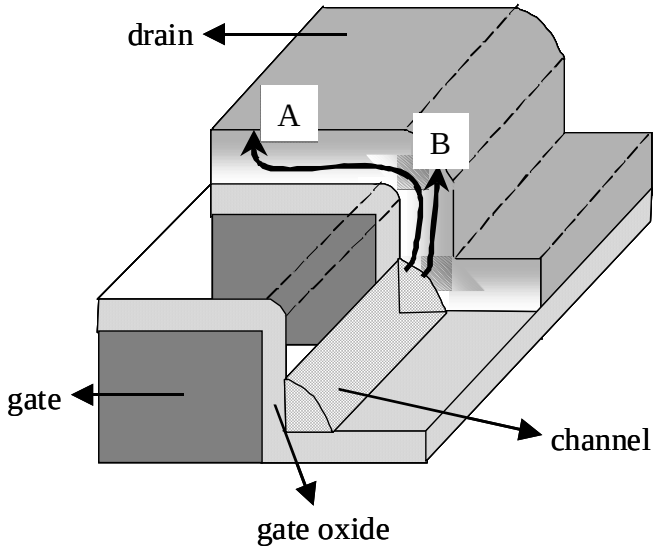


Fig. 3-19 Leakage current flows near the drain side of NW-TFT.

To discuss the dependency between the GIDL current and the total off-state leakage, the off-state current at specific bias condition (e.g., V_G = -5V, V_D = 3V) can not be directly compared for each groups because of the difference in structural profile. For example, the resultant channel width in HM group is different from those in CON and RTA group owing to the inserted nitride layer. The channel width of SG group is also different because the etching rate is different between Si and $Si_{1-X}Ge_X$ material. Another method is to first plot the off-state current as a function of gate width (which is demonstrated in Fig. 3-14), then compare the slope of the line from each group. But this method is still unable to show the dependency owing to the aforementioned effect of channel profile and material. Considering the demonstrated result in Fig. 3-14, although the slope of RTA is smaller than that of CON group, it is hard to distinguish whether the result comes from weaker dependence on gate width, or from the smaller off-state leakage contributed by better crystallinity.

To resolve the dependency between the GIDL current and the total off-state leakage, an indicator called Off-State Current Ratio (OSCR) is proposed. It is defined as:

$$OSCR = \frac{I_D}{I_D(GW = 0.8um)} \qquad \text{Eq. 3-2}$$

Here I_D indicates the off-state leakage current at specific bias condition. By dividing the off-state current of each sample by that of GW = 0.8μm, the effect of gate width (i.e., GIDL) can be extracted from the effect contributed by other factors. The comparison of the slope among all samples can now be used as an indicator for examining the dependency.

The OSCR for each sample is plotted in Fig. 3-20. It appears that although the leakage current of RTA split is lower than that of CON (as shown in Fig. 3-14), the leakage current of RTA split is strongly proportional to GW. In contrast to the less band-bending induced by higher defect density discussed in SG split, the better crystallinity will increase the band-bending and reduce the resistance for path A schematized in Fig. 3-19, and enhance the dependency. The result implies that OSCR successfully rules out other factors and provide a simple and clear method for investigating the dependency.

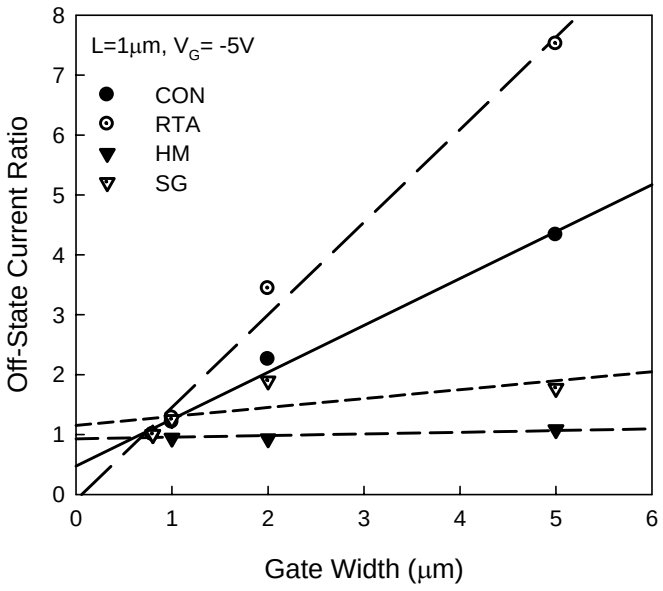


Fig. 3-20 OSCR of devices with different modification schemes.

Unlike CON and RTA groups, HM and SG groups exhibit distinctly different off-state leakage characteristics. As shown in Fig. 3-20, the off-state leakage current of HM and SG group shows very weak dependence on GW. The result is consistent with the data shown in previous sections, which can be ascribed to different reasons.

3.4 Summary

In this chapter, the mechanism of off-state characteristics in the newly-developed NWTFT is proposed and discussed. According to its unique structure, several process and material modifications were employed for reducing the off-state leakage current of the proposed NWTFTs. The detailed mechanisms of off-state leakage current in each modification scheme are also discussed.

As pointed out previously, the low-energy S/D implantation forms a lightly-doped region at the gate/drain interface, which may induce an additional GIDL current path (path A in Fig. 3-19). This path dominates the leakage current in CON and RTA samples, and results in the GW-dependent leakage. In HM device, path A is eliminated because of the relaxation of GIDL effect owing to the reduction of gate-induced electric field. In SG device, the high DOS in the $Si_{1-X}Ge_X$ material not only significant increases the resistance of path A, but also prohibits the band-bending needed for the GIDL. Both reasons prohibit path A. In the last two cases, leakage mainly flows through path B in Fig. 3-19, thus exhibiting a weak dependence on GW.

The proposed GIDL current is mainly affected by several major factors: electric field between the gate and the drain, doping distribution at gate-to-drain overlap region, and trap density in poly-Si material. All of them determine how much band-bending occur near the oxide-Si interface: larger field and lower doping concentration induce more bending. It has been demonstrated by the devices embedded with a nitride hard mask. The amount of trap density in poly-Si material can also affect GIDL, which is evidenced by RTA and SG splits.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