Chapter 4

Investigation of Hot-carrier Degradation Using a Novel Test Structure

Hot-carrier effect (HCE) plays a very important role in reliability issue for metal-oxide-semiconductor field-effect transistors (MOSFETs). There are many studies and reports about the impact of HCE. Along with the improvement of performance, especially in mobility, poly-Si TFTs are now also suffer from the degradation and shift in characteristics induced by HCE. In this chapter, HCE in both MOSFETs and TFTs will be introduced, followed by the demonstration of a novel structure which can spatially and temporally resolving the locations and effects induced by HCE. The new test structure consists of several source/drain electrode pairs arranged in the direction perpendicular to the normal (i.e., lateral) channel of test transistor. This unique feature allows the study of spatial resolution of hot-carrier degradations along the channel of test transistor after stressing. The extent of degradation as well as the major degradation mechanisms along the channel of test transistor can be clearly identified. Our experimental results also clearly show that the initial damage during the early stage of hot-carrier stressing, which is still undetectable by conventional test structures, can be easily observed by the structure. In addition, the proposed test structure is also capable of resolving the evolution of the degradation along the channel, thus providing a powerful tool to study the location-dependent damage mechanisms.

4.1 Introduction of hot-carrier effect (HCE)

When under the influence of high electric field during device operation, the majority

carriers (electrons for NMOS, or holes for PMOS) inside the inversion layer can gain sufficient energy and become “hot carriers”. These carriers may release their energy at other portions of channel, and cause several damages or reliability problems. Since the channel electric field is not uniformly distributed, HC damage is location-dependent in the channel. There are two major types of hot carriers in MOSFETs, one is called channel hot-electron injection (CHEI), and the other is called drain avalanche hot-carrier (DAHC). CHEI is generated when electrons are accelerated by lateral electric field across the channel, and gain energy to form hot electrons [4.1]. The voltage biases of V_G=V_D has been reported to be the optimum condition for CHEI [4.2]. Unlike CHEI, DAHC is mainly induced by impact ionization which originates from the high electric field near the drain [4.3][4.4]. The generated energetic electrons will then cause avalanche multiplication and substantially increase the amount of energetic carriers. Experiments show the optimum condition to observe DAHC is near V_G= 0.5 V_D. Schematics of CHEI and DAHC are illustrated in Fig. 4-1(a) and Fig. 4-1(b), respectively.

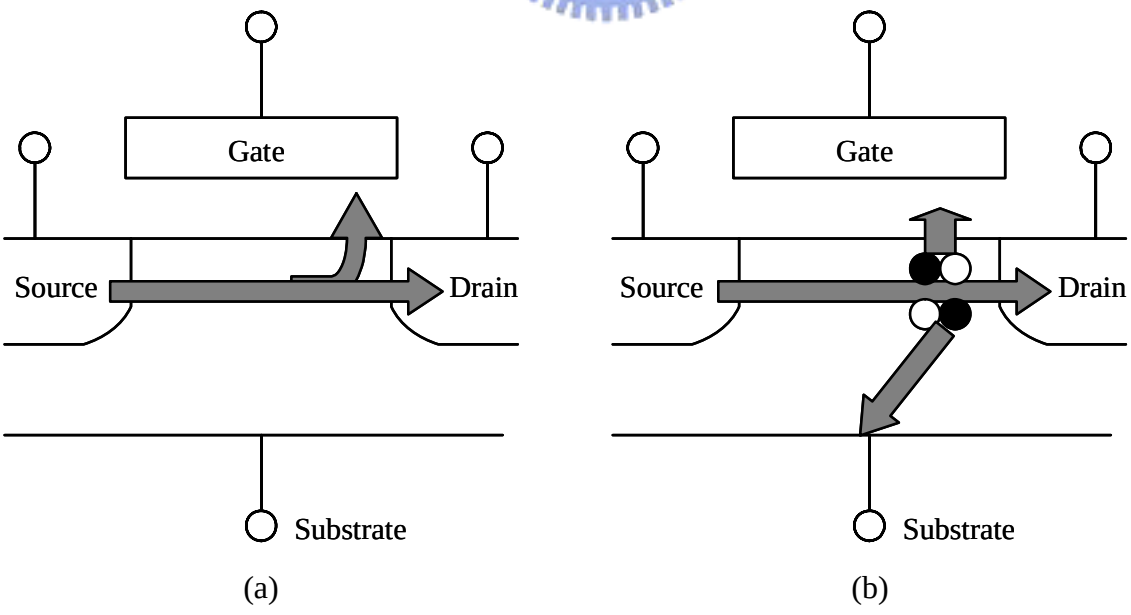

Fig. 4-1 Schematic illustration of (a) CHEI and (b) DAHC in hot-carrier generation.

4.1.1 Hot-carrier degradation in MOSFETs

The impacts of HCE in MOSFET can be roughly categorized into the following phenomena:

- Hot carriers may be injected into gate insulator, and form fixed charges or oxide traps.
- Hot carriers may surmount the barrier at Si/SiO_2 interface, reach gate and become excess gate leakage.
- Hot carriers may lose their energy at Si/SiO_2 interface, degrade the property of interface and increase interface states (N_{it}). This will cause the performance degradation in field-effect mobility and subthreshold swing.

Many methods have been developed to analyze the HCE. Several useful tools are widely employed as the indicator of hot-carrier degradation:

- The subthreshold and output characteristics of the device: This is the most intuitive and easiest method to observe HCE by the changes in drain current, gate current, threshold voltage, transconductance, mobility, and subthreshold swing.
- Substrate current (I_{SUB}): It is a very common indicator because the generated holes in DAHC prefer to flow out from the substrate contact. By measuring the substrate current, the severity of hot-carrier generation can be evaluated.
- Charge pumping method: when interface state density increases after hot-carrier stressing, the difference can be observed by this method.

4.1.2 Challenges in hot-carrier analysis of TFTs

Polycrystalline silicon (Poly-Si) thin-film transistors (TFTs) are used in many applications, including flat-panel displays and large-area microelectronics [4.5]-[4.8]. Because of their better film crystallinity, significant improvement in carrier mobility and drive current can be realized in poly-Si TFTs, compared with amorphous silicon TFTs. Nevertheless, hot-carrier degradation remains as one of the most critical reliability concerns for practical applications of poly-Si TFTs [4.9][4.10].

Due to the lack of substrate contacts, together with the presence of numerous inter-/intra-grain defects [4.11], the whole picture is much more complicated for poly-Si TFTs, compared with bulk MOSFETs. As a result, numerical simulation techniques are normally required to acquire the location dependence of HC effects under specific stress conditions [4.12]. Resolving the evolution of hot-carrier degradation is also challenging. This is because the damage creation itself may affect the temporal potential distribution during stressing, and therefore subsequent degradation characteristics.

Since the damage associated with HC degradation is non-uniform along the channel of the stressed transistor after hot-carrier stressing, it is desirable to resolve and understand the detailed mechanisms responsible at different portions of the stressed channel. In this work, a novel test structure called Hot-Carrier TFT (HCTFT) that serves this purpose is proposed and demonstrated. With the proposed structure, analysis of HC degradation and mechanism along the stressed channel become feasible. We also further investigate in detail the sensitivity and effectiveness of the test structure in revealing the impact of applied stress conditions, as well as the position dependence and the evolution of degradation.

4.2 Fabrication and operating principle of HCTFT

The top view of the test structure is shown in Fig. 4-2. The test structure is configured with 4 pairs of n^+ electrodes at the edge of channel. One pair of n^+ electrodes is placed along the x- (horizontal) direction to form the source and drain (S/D) of the normal (lateral) test transistor (TT, shown in Fig. 4-2(b)) that will be subjected to hot-carrier stressing, while the other three pairs are arranged along the y- (vertical) direction to form three separate monitor transistors (MTs, shown in Fig. 4-2(c)) to allow spatial characterization of the hot-carrier degradations along the channel of test transistor after stressing. A common gate electrode shared by the test transistor as well as all three MTs is lying over the entire channel. Since each pair of n^+ electrodes could be configured as the S/D of the respective MT, the current-voltage (I-V) characteristics of the corresponding MT could be characterized. The pair of S/D placed along the x-direction that serves to form the test transistor is subjected to hot-carrier stressing by applying a high voltage to its drain for inducing the hot-carrier degradations in the test transistor. According to their respective location relative to the channel of the test transistor, the three MTs are denoted as S-MT (source-side MT), C-MT (central MT), and D-MT (drain-side MT), respectively. This unique configuration allows us to resolve the damage and identify the associated mechanisms at different locations along the channel of test transistor after stressing. Important planar structural dimensions for the test structure characterized in this work are detailed in Fig. 4-2.

Samples were prepared on oxidized Si wafers. Poly-Si layers of 50nm were prepared by either as-deposited method or solid-phase crystallization (SPC) to serve as the channel layer. The as-deposited poly-Si layer was deposited by a low-pressure chemical vapor deposition (LPCVD) system at 620˚C, while SPC poly-Si was prepared by annealing an amorphous Si layer at 600˚C in N_2 for 24 hours.

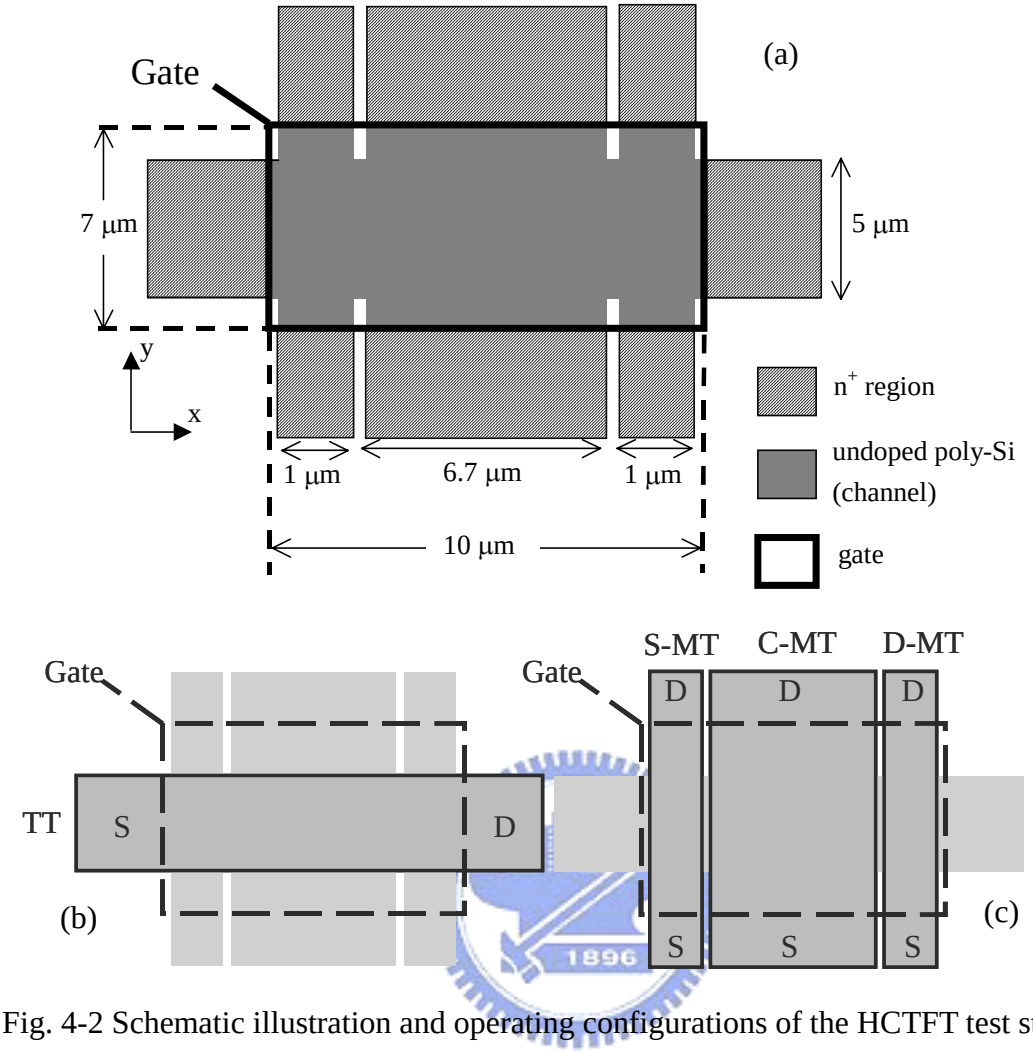

Fig. 4-2 Schematic illustration and operating configurations of the HCTFT test structure.

The active region was then formed after lithography and etching. The gate dielectric consisted of an LPCVD oxide layer of 35 nm. An in-situ n^+ doped poly-Si of 200 nm thick was employed as the gate electrode. Source/drain doping was formed self-aligned by implanting phosphorous ions with a dosage of $5x10^{15}$ cm^{-2} at 45 keV. The gate itself was used as the mask for the self-aligned implantation. An LPCVD oxide layer of 200 nm was used as the passivation layer to isolate humidity and impurity, followed by contact-hole formation. After the metallization step, the test structure further received a plasma treatment in NH_3 ambient at 300˚C. Unless mentioned otherwise, the treatment time was one hour in this work. It is worth noting that the proposed test structure requires only layout modifications, and could be easily integrated with the display panel processing without extra masks or processing

steps.

The subthreshold and output characteristics of the fabricated testers were measured by an Agilent™ 4165A semiconductor parameter analyzer and Interactive Characterization Software (ICS) software. A program written by VEE language was used to automatically perform the task of hot-carrier stressing. The characterized data is then fed into Excel and Matlab to extract the electrical parameters and calculate the difference before and after hot-carrier stressing.

The electrical characteristics of as-fabricated test transistors (TTs) are shown in Fig. 4-3. Both devices with as-deposited and SPC poly-Si channel are characterized in this figure. Mobility, subthreshold swing and other performance parameters for both devices are shown in Table 4-I. Devices with SPC channel outperform their counterparts with as-deposited channel in all aspects. This is reasonable since the grain size and the crystallinity is better in devices with SPC channel.

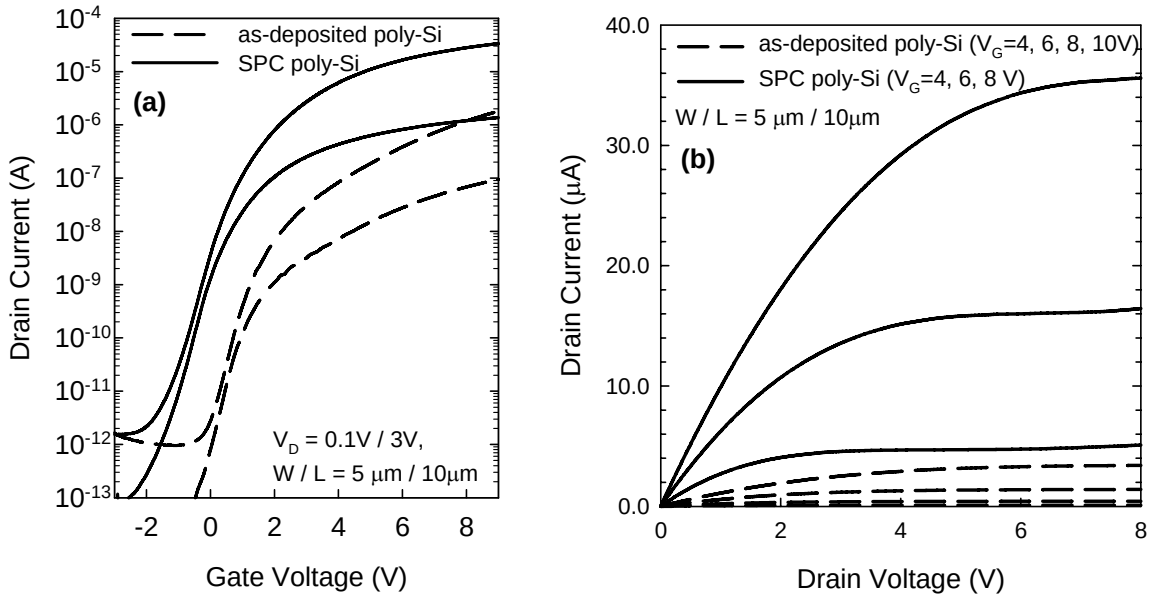

Fig. 4-3 (a) Subthreshold and (b) output characteristics of as-fabricated test transistors (TTs).

	Vth (V)	SS (mV/dec)	Mobility ($cm^2V^{-1}s^{-1}$)	On current (Amp)
As-deposited poly-Si	3.52	780	24.00	$1.41x10^{-6}$
SPC poly-Si	1.43	460	40.95	$3.56x10^{-5}$
W / L = 5μm / 10μm, Tox = 35nm, On current : I_D @ V_G = 8V, V_D=8V				

Table 4-I Major performance parameters for the test transistors.

4.3 Spatially resolving capability of HCTFT

In this section, spatially resolving capability of the proposed HCTFT will be demonstrated. Let us begin from test transistors, which acts as conventional TFTs. At first devices with as-deposited poly-Si channel were evaluated. After applying a hot-carrier stressing with V_G/V_D = 10V/20V for 1000 seconds, subthreshold characteristics of the test (i.e., lateral) transistor are degraded (shown in Fig. 4-4(a)). As can be seen in the figure, the degradation in device characteristics in terms of increased subthreshold swing and reduced on-current are indeed observed after the stress. The post-stress I-V shifts are more significant when measured at a low V_D of 0.1 V. These observations are consistent with the well-known belief that most of the damage events occur in the channel near the drain side of the test transistor. Hot-carrier stressing can generate additional interface states and/or grain-boundary defects [4.13], and form a defect-rich and resistive region near the drain side [4.12]. A larger drain bias during the measurements of subthreshold I-V characteristics tends to extend the drain depletion region. This would in turn screen out more defects induced in the channel near drain side, thus relieving the post-stress I-V shift. The phenomenon can also be evidenced by measuring the device with source and drain reversion. When the device is measured with reversed S/D mode, the defects near drain side now are located near the source side.

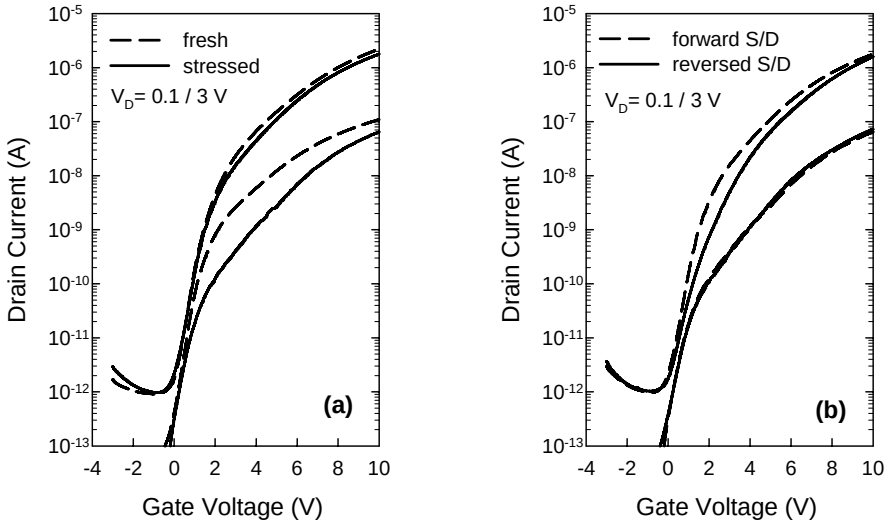

Fig. 4-4 (a) Subthreshold characteristics of the test transistors before and after the hot-carrier stressing at V_G/V_D of 10 V/20 V for 1000 sec. (b) Subthreshold characteristics which are measured under reversed S/D mode.

As can be seen in Fig. 4-4(b), defects which were originally screened out in the forward S/D mode will now be exposed when the device is operated in reversed S/D mode, so the device will exhibit obvious degradation in subthreshold I-V characteristics even at higher drain bias.

The aforementioned results from the conventional test transistors provide information regarding the major damage location in the stressed channel, as is well known in literature. However, detailed degradation mechanisms at different sections of the stressed channel could not be resolved by the conventional test structure. Besides, the conventional test structure is also insensitive in detecting the induced damage when the applied stress voltages are low. To address these shortcomings, MTs in the test structure were characterized and the results are shown in Fig. 4-5. It is worth noting that the characteristics of MTs shown in Fig. 4-5 were measured using the same test structure with its test transistor hot-carrier-stressed and measured in Fig. 4-4. It can be seen that among the three MTs, the D-MT shows the worst degradation. Note that the post-stress I-V shift is very significant even when measured at a

high V_D bias (e.g., 3 V), indicating that the induced traps are uniformly distributed along the entire channel of the D-MT. This observation confirms the inference made above in analyzing the results of Fig. 4-4. However, the remaining two MTs exhibit some interesting results that are not explicitly revealed in Fig. 4-4. First, the C-MT shows degraded subthreshold swing, albeit the on-current does not seem to be affected. This implies that the generation of interface states at oxide/channel interface is mainly responsible for the degradation. Second, the S-MT shows negative parallel shift in subthreshold characteristics, indicating that positive hole trapping is preponderant in the oxide near the source side of test transistor after stressing. These holes are generated by the impact ionization during the hot-carrier stressing of test transistor. Since no substrate contact is present in the TFT structure, these holes tend to drift toward the grounded source, and some of them with sufficient energy may surmount the barrier and be injected into the oxide. Based on the results shown in Fig. 4-5, major degradation mechanisms occurring at different channel sections could be clearly distinguished and identified by the proposed novel test structure.

Similar trends can be found in testers with an SPC poly-Si channel. The subthreshold characteristics of a test device is stressed at V_G/V_D = 9V/18V for 1000 seconds. The subthreshold characteristics of test transistor and three monitor transistors before and after the stressing are shown in Fig. 4-6. The MTs shown in Fig. 4-6 again provide the direct evidence that the degradation occurs near drain side. The aforementioned damage scenario has been characterized in the literature by a number of techniques, including reversed source/drain measurement [4.14], capacitance-voltage (C-V) measurement [4.15], device simulation [4.12][4.16], asymmetric drain/source structure [4.14], and pico-second time-resolved emission microscope [4.17]. However, all the above methods failed to directly and unambiguously pinpoint the damage location. By contrast, MTs in our proposed test structure provide useful degradation characteristics in different parts of the channel. These results

confirm that the location-dependence of HC degradation could be clearly resolved with the proposed test structure.

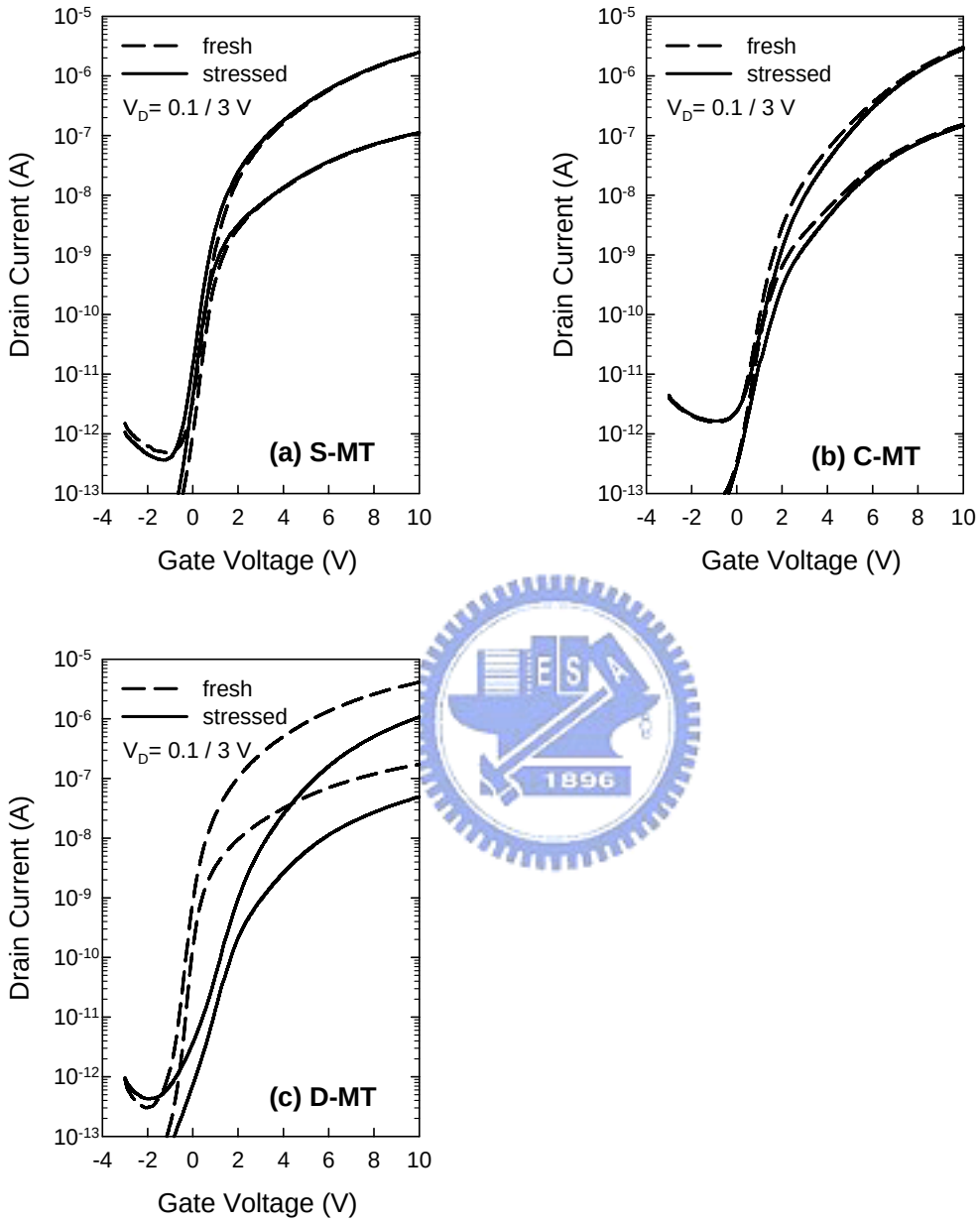

Fig. 4-5 Subthreshold characteristics of (a) S-MT, (b) C-MT, and (c) D-MT transistors in the same test structure characterized in Fig. 4-4 before and after the hot-carrier stressing at V_G/V_D of 10 V/20 V for 1000 sec.

4.4 Feature of sensitivity enhancement in HCTFT

The test structure also provides excellent sensitivity for the detection of hot-carrier

degradation. To induce visible degradation, researchers usually resorted to severe stress condition with high stress voltage and/or sufficiently long stress time.

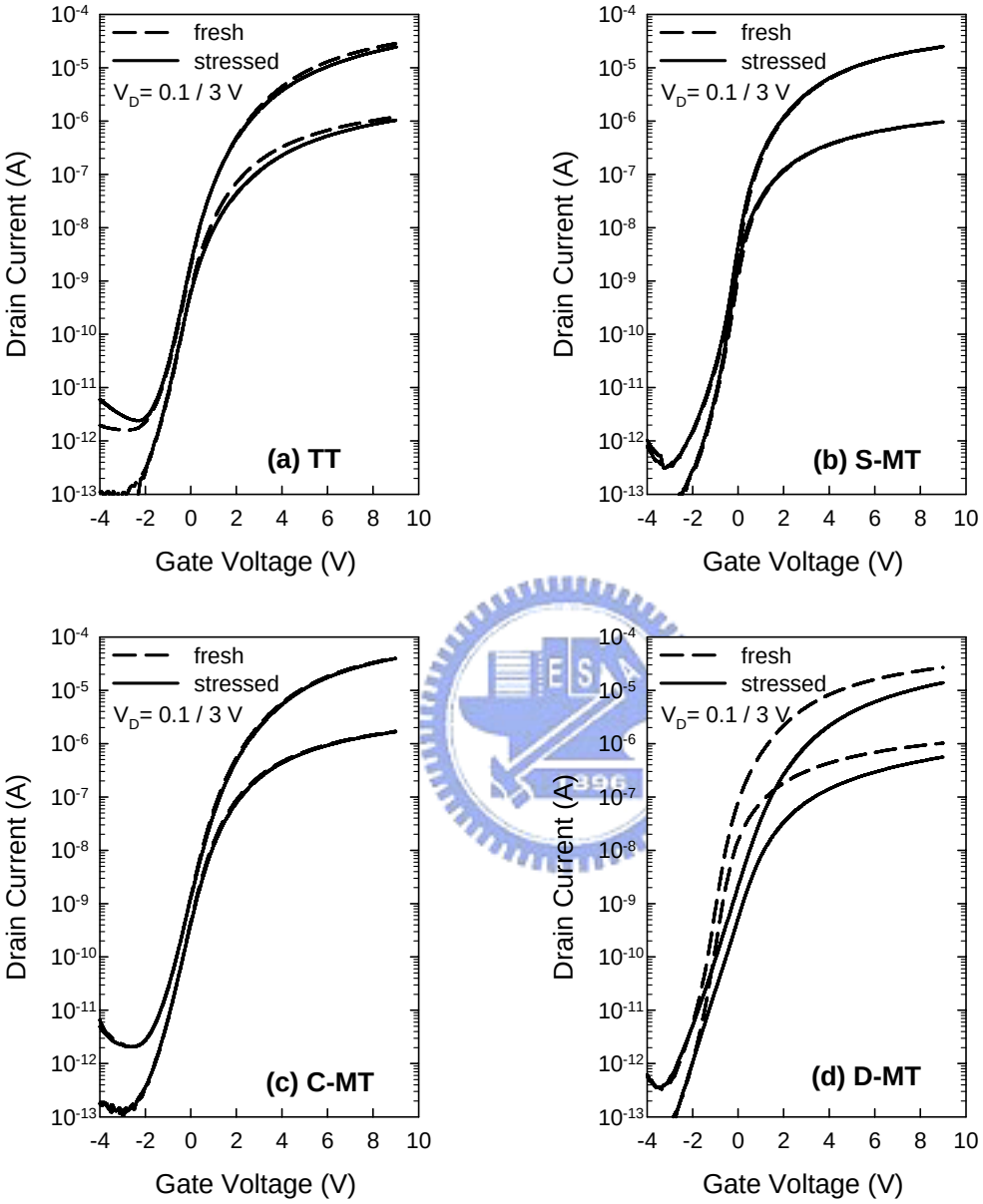

Fig. 4-6 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in a test structure with a SPC poly-Si channel before and after the hot-carrier stressing at V_G/V_D of 9 V/18 V for 1000 sec.

For practical device operation, however, the applied biases to the device are low, so the degradation is almost impossible to observe. Because the degradation in test transistor (TT) is amplified by the associated D-MT, the proposed structure is suitable to resolve this problem.

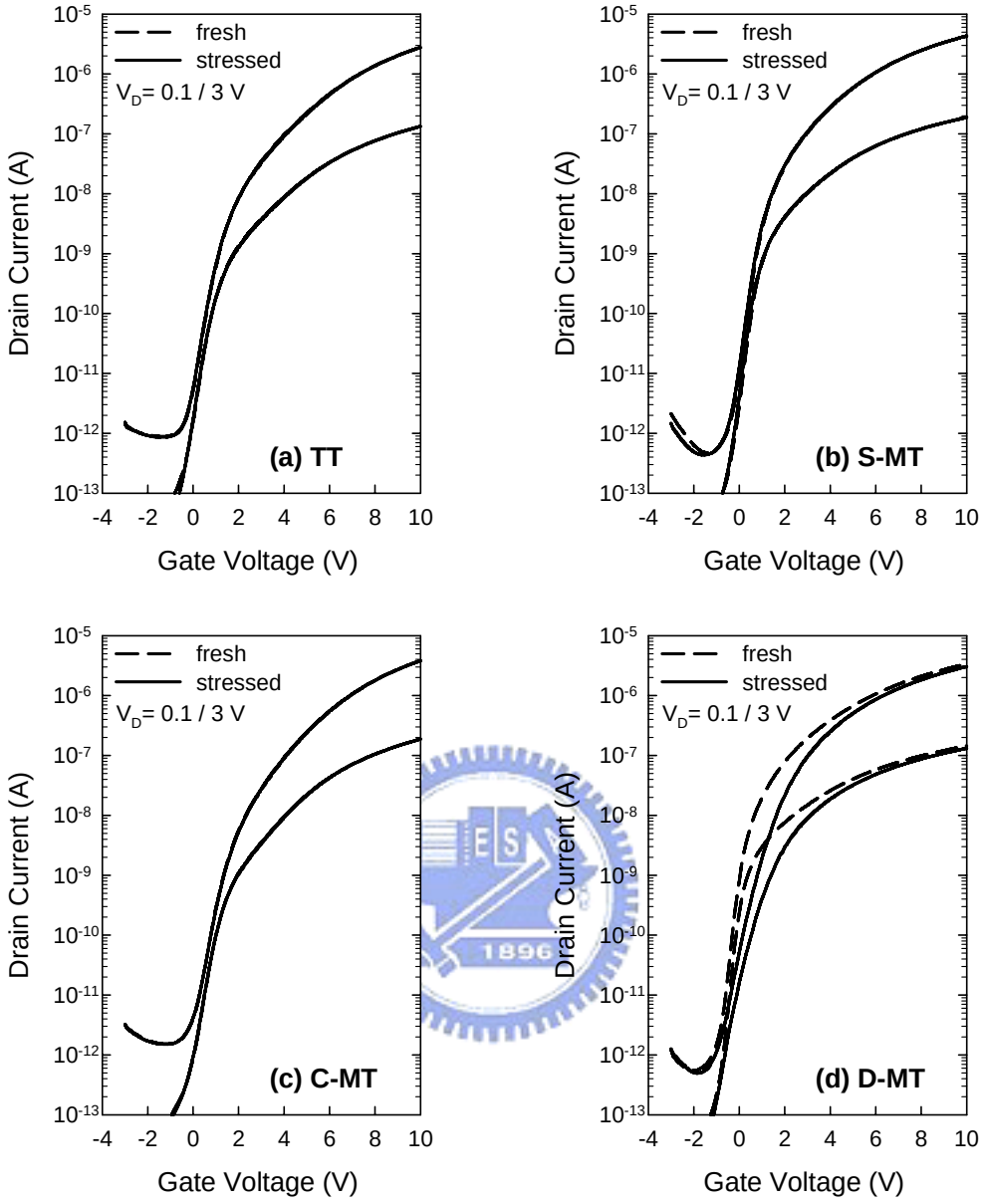

Fig. 4-7 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in a test structure with an as-deposited poly-Si channel before and after the hot-carrier stressing at V_G/V_D of 6 V/12 V for 1000 sec.

To further highlight this feature, a tester using as-deposited poly-Si as the channel material was stressed at a lower voltage (V_G / V_D = 6V /12V) for 1000 seconds, a condition where the stress field was much reduced than that in Fig. 4-4.The subthreshold characteristics of four sub-transistors are shown in Fig. 4-7. As shown in Fig. 4-7(a), the test transistor exhibits barely detectable degradation after the stressing, because of the milder stress

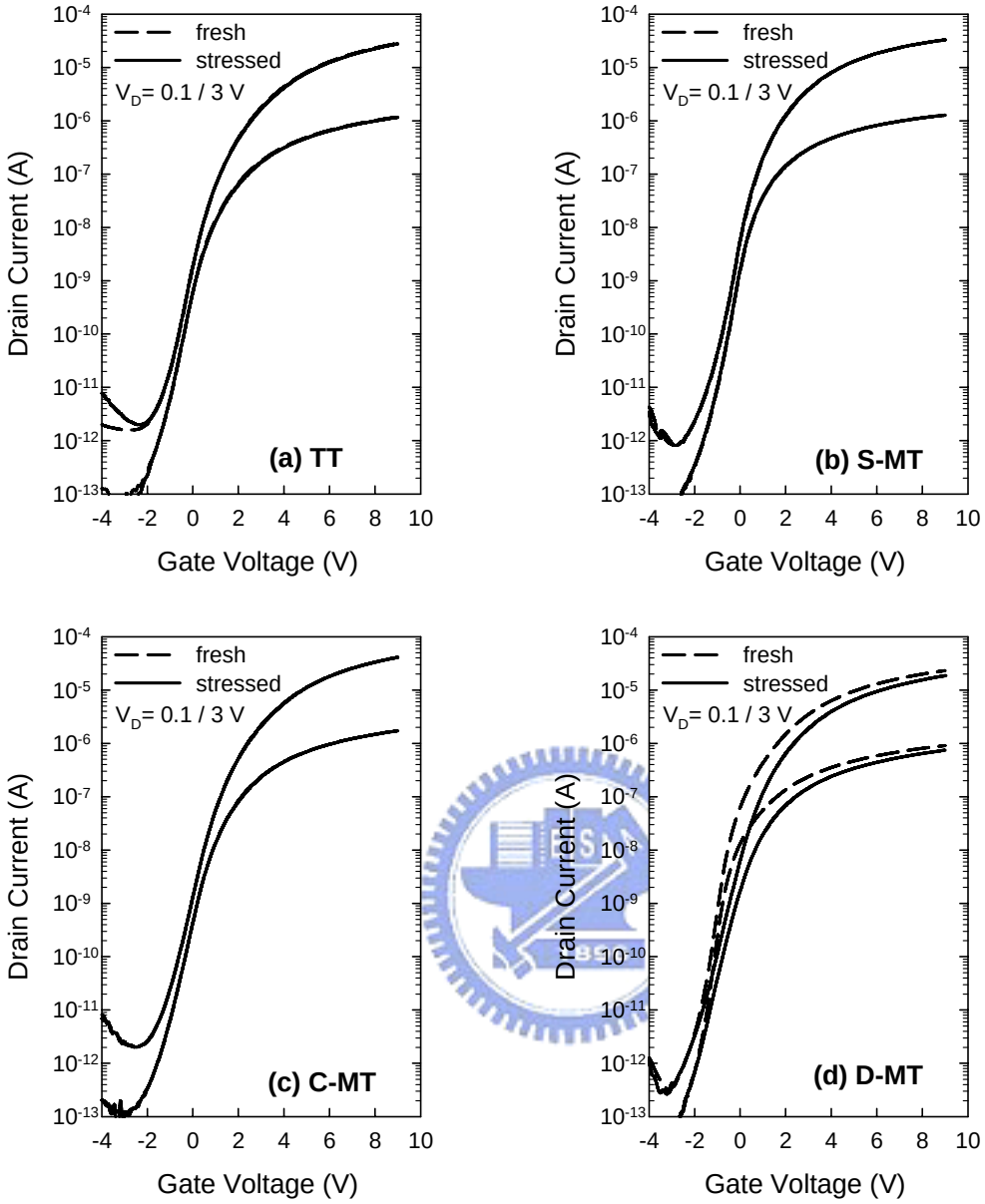

Fig. 4-8 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in a test structure with a SPC poly-Si channel before and after the hot-carrier stressing at V_G/V_D of 6.5 V/13 V for 1000 sec.

condition. This will call for a very long stress time for TT to yield detectable degradation. However, the associated D-MT shows visible degradation, as shown in Fig. 4-7(d). Like that using as-deposited poly-Si, the sample using SPC poly-Si as the channel material also shows similar trends in sensitivity enhancement. Similar results for SPC samples are shown in Fig. 4-8.

Figure 4-9 and Fig. 4-10 show the shift in threshold voltage (ΔVth) and subthreshold swing (ΔSS), respectively, as a function of stress V_D with V_G= 0.5 V_D for 1000 sec. Testers in these figure employ SPC poly-Si as the channel material. As expected, the degradation increases with increasing V_D. When V_D is less than 15 volt, TTs depict threshold voltage shift of less than 100mV, and negligible change in subthreshold swing.

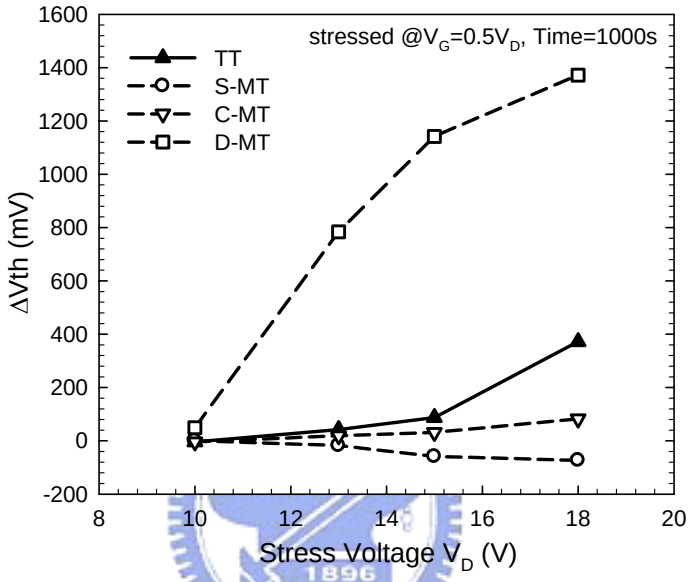

Fig. 4-9 Threshold voltage shift of test structures under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.

This again indicates that the traditional test structure is not suitable for monitoring milder stress conditions. In contrast, the minor damage can be unambiguously detected with the monitor transistors in the test structure. Moreover, the severely degraded characteristics of D-MTs after stressing clearly pinpoint the major damage site. In fact, it is possible to investigate the damage mechanisms in different parts of the channel. This point is further addressed in the following section.

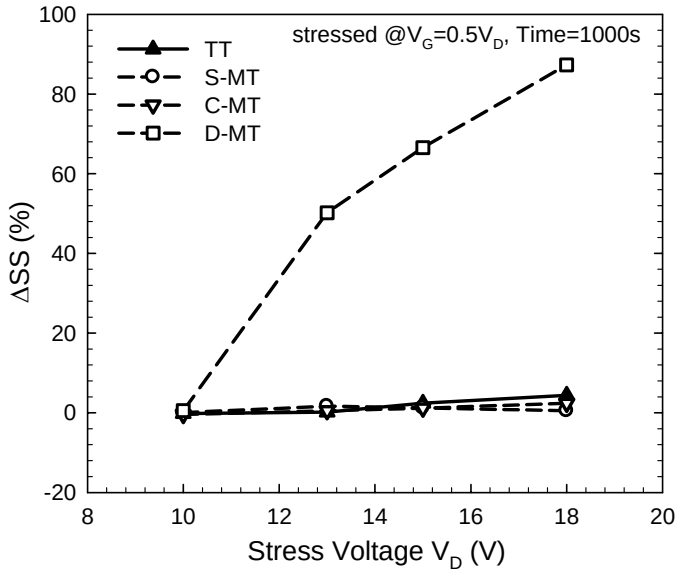

Fig. 4-10 Subthreshold swing degradation of test structures under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.

4.5 Effects of stress gate voltage

Figure 4-11 and Fig. 4-12 show shifts in threshold voltage and subthreshold swing, respectively, of TT and MTs after 1000-sec stress at V_D of 13 V and various V_G. It is seen that ΔVth of the test transistor is positive in the low V_G regime, monotonically decreases with increasing V_G, and becomes negative as V_G exceeds 10 volt. The information is, however, very limited. By contrast, MTs' data reveal several interesting features.

First, the drain-side damage is dominant in the low V_G regime, and peaks at around V_G= 0.5 V_D. Similar trend is also observed in ΔSS, as shown in Fig. 4-12, implying that the generation of oxide interface states and defects at grain boundaries are the likely culprits. The major damage site gradually moves toward the source as V_G increases. The negative threshold voltage shift in the S-MT device as V_G > 8 V indicates that hole trapping in gate oxide now dominates the degradation.

The subthreshold characteristics of the tester, which was stressed at V_G/V_D = 13V/ 13V

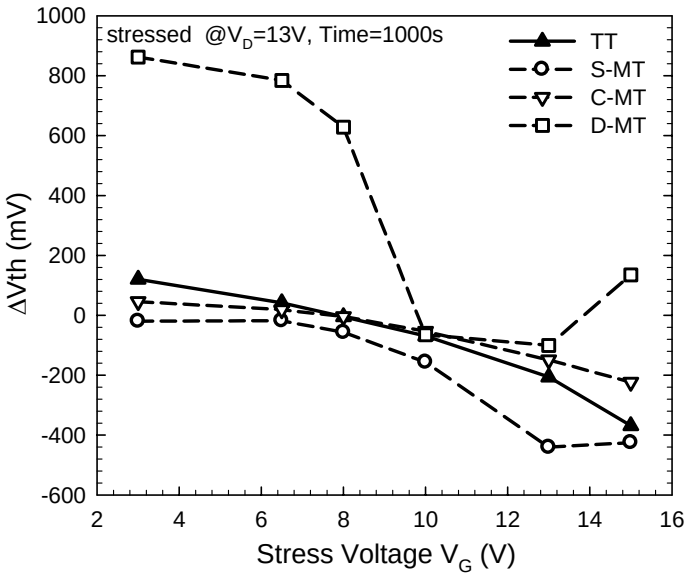

Fig. 4-11 Threshold voltage shift of test structures under various hot-carrier stress conditions at a fixed V_D of 13 V.

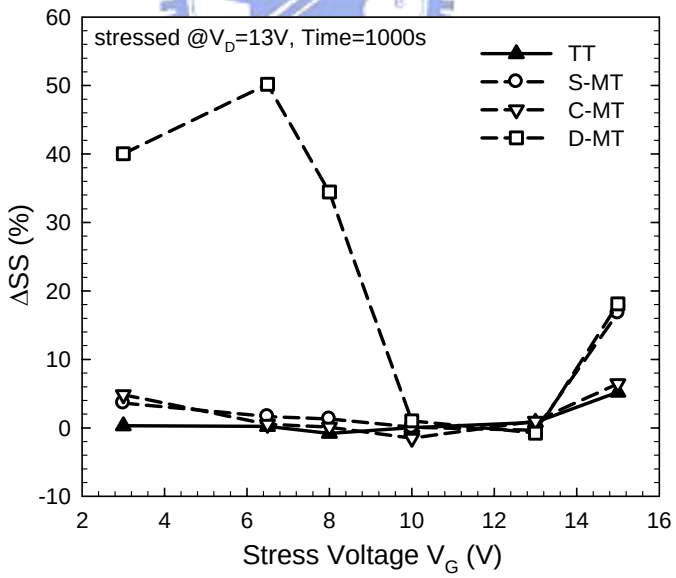

Fig. 4-12 Subthreshold swing degradation of test structures under various hot-carrier stress conditions at a fixed V_D of 13 V.

for 1000 seconds, are shown in Fig. 4-13. It can be clear seen that the S-MT shows the largest shift in subthreshold curve, but no degradation in subthreshold swing. This is consistent with

the result reported in Fig. 4-11 and Fig. 4-12. The detailed mechanism will be described in the next section.

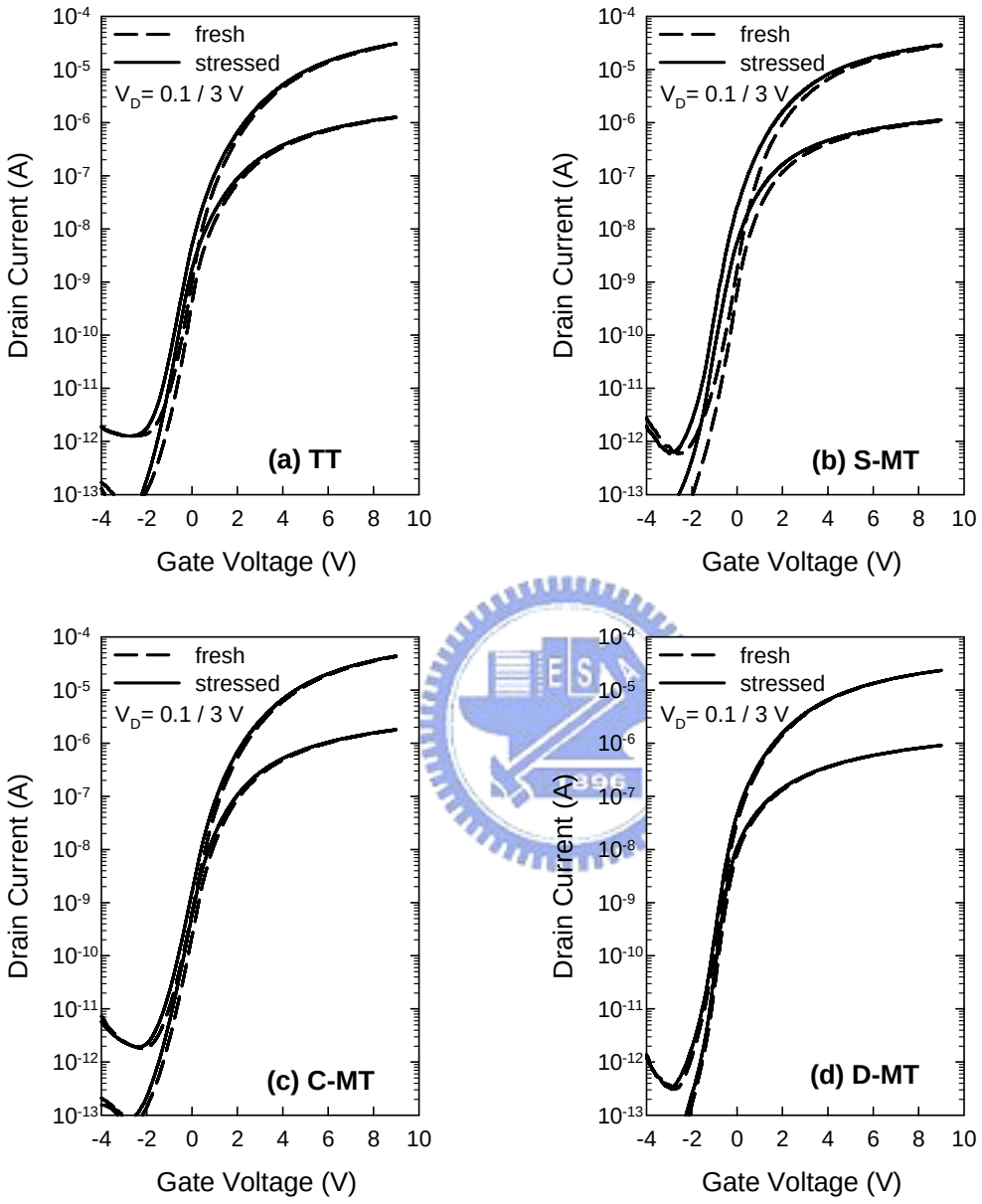

Fig. 4-13 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in the test structure with a SPC poly-Si channel before and after the hot-carrier stressing at V_G/V_D of 13 V/13 V for 1000 sec.

4.6 Evolution of HC degradation

From the above results, we can see that the degradation is complicated and is related to

both V_G and V_D. Next, we investigate the evolution of degradation under two distinctly different stress modes, namely, $V_G = 0.5\ V_D$ and $V_G = V_D$.

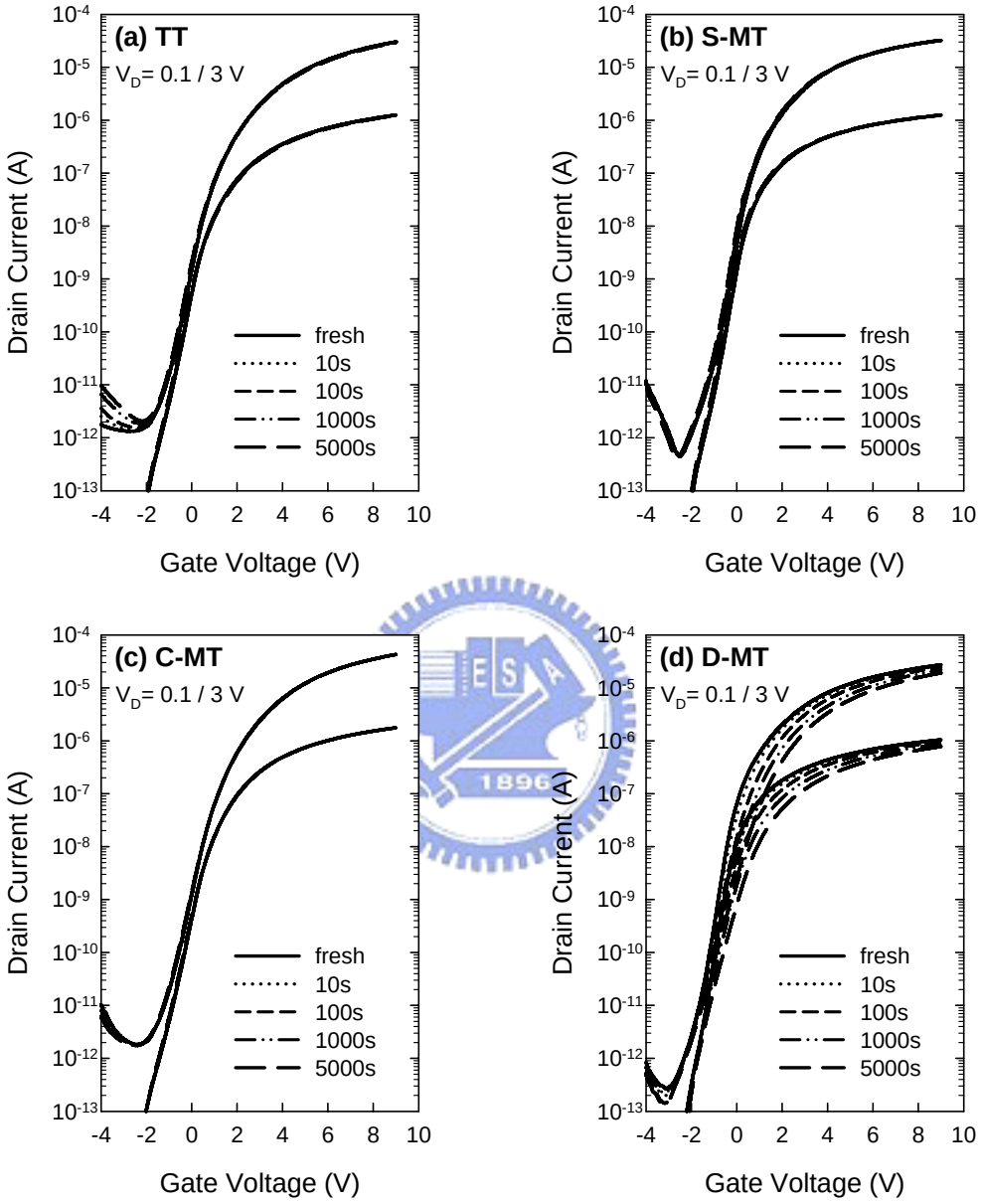

Fig. 4-14 Evolution of subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT in test structures with a SPC poly-Si channel during hot-carrier stressing under V_G/V_D=6.5V/13V.

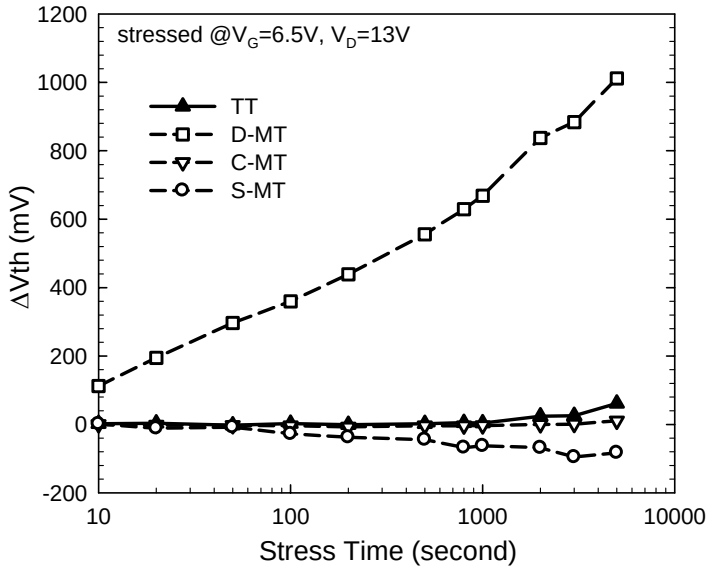

Fig. 4-15 Evolution of threshold voltage shift of a test structure during hot-carrier stress under V_G/V_D=6.5V/13V.

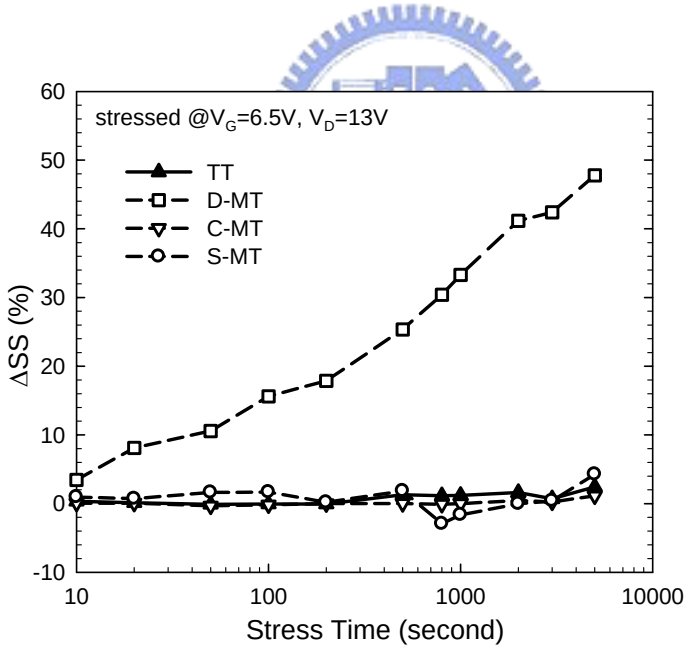

Fig. 4-16 Evolution of subthreshold swing degradation of a test structure during hot-carrier stress under V_G/V_D=6.5V/13V.

As shown in Fig. 4-14 to Fig. 4-16, the evolution of the degradation induced in different parts of the channel under V_G/V_D = 6.5V/13V can be directly resolved with the test structure. Specifically, although TT's data show negligible subthreshold shift after the stressing, D-MT

shows unambiguous degradation at a very early stage, and the degradation increases monotonically with increasing stress time. Moreover, negative threshold voltage shift in Fig. 4-15 for S-MT becomes clear when the stress time is longer than 100 sec. Similar findings can also be observed in Fig. 4-9 and Fig. 4-11, confirming that the dominant damage mechanism is indeed position-dependent. Although this has been well known in the literature, the direct observation of position-dependent damage mechanisms without involving complicated experimental scheme illustrates the uniqueness and usefulness of the proposed test structure.

From the aforementioned results, the degradation during HC stressing under V_G= 0.5 V_D condition is illustrated in Fig. 4-17. In this case, impact ionization occurs at drain side by the high field strength, and causes generation of electron-hole pairs. The generated hot carriers may release their energy in the channel or near oxide/channel interface where defects are created. Since no substrate contact is present in the TFT structure, the generated holes tend to drift toward the grounded source, some of them may have sufficient energy to surmount the barrier and are injected into the oxide. This mechanism explains the negative threshold voltage shift of S-MTs.

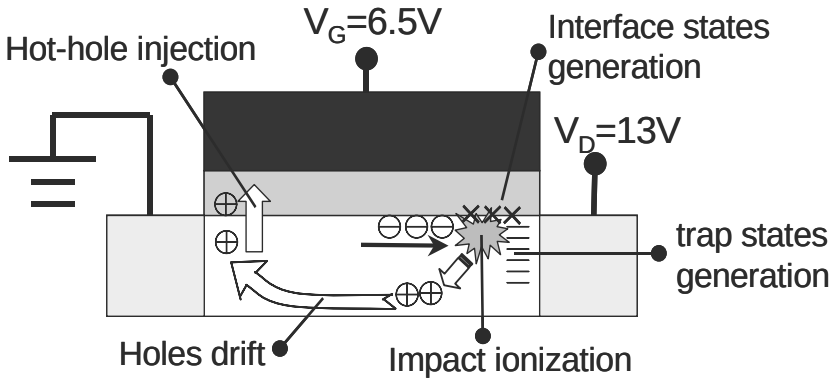

Fig. 4-17 Schematic illustration of the hot-carrier-degradation mechanisms under V_G/V_D=6.5V/13V.

Temporal evolution analyses for devices under $V_G = V_D$ stress mode are presented in Fig. 4-18 to Fig. 4-20. It is seen that all four sub-transistors depict negative threshold voltage shift, implying that generation of positive charges is mainly responsible for the degradation. Moreover, among these devices, S-MT exhibits the largest shift. It should be noted that, although the S-MT characterized in Fig. 4-15 under $V_G = 0.5V_D$ stress mode

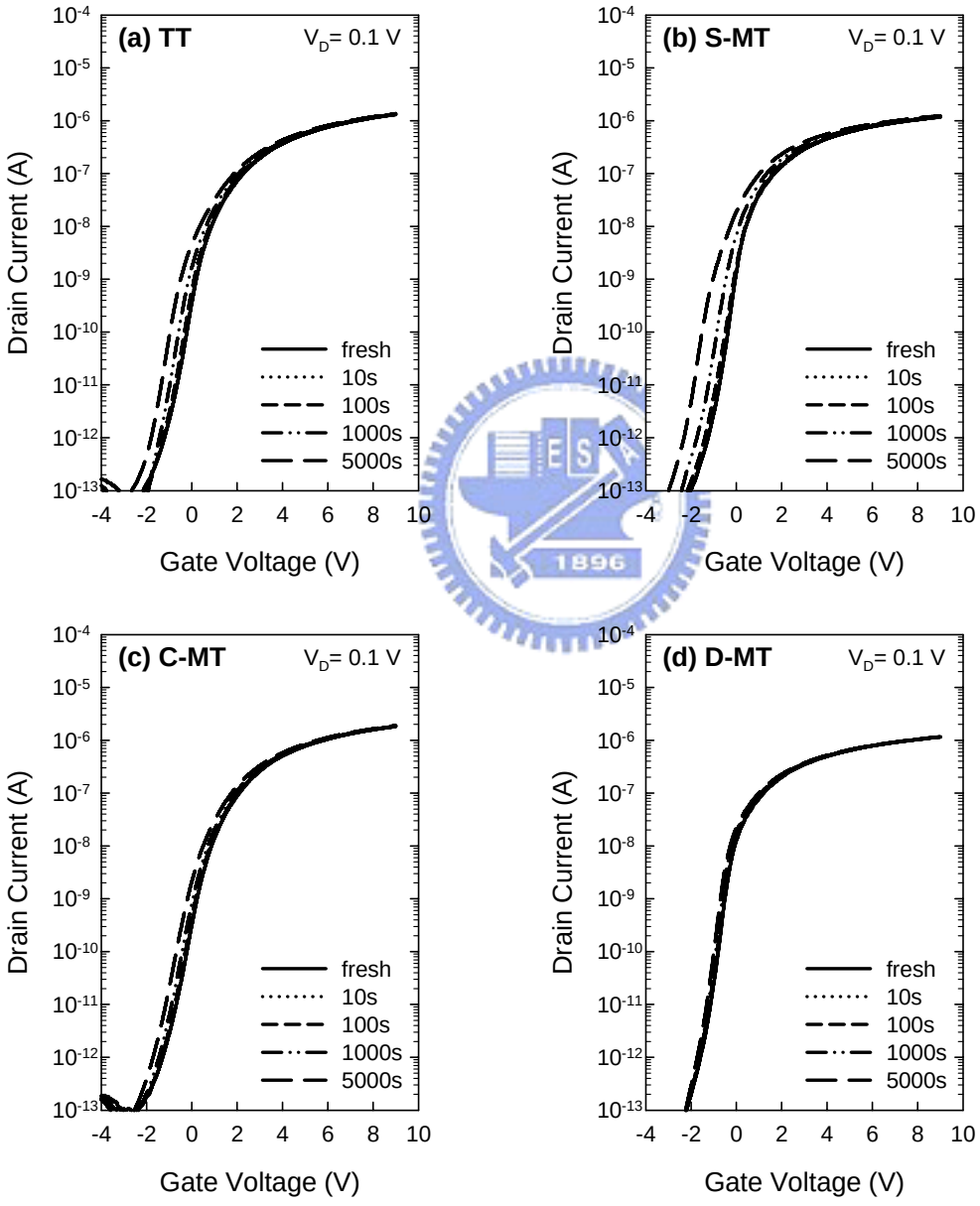

Fig. 4-18 Evolution of subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT in a test structure with a SPC poly-Si channel during hot-carrier stressing under V_G/V_D=13V/13V.

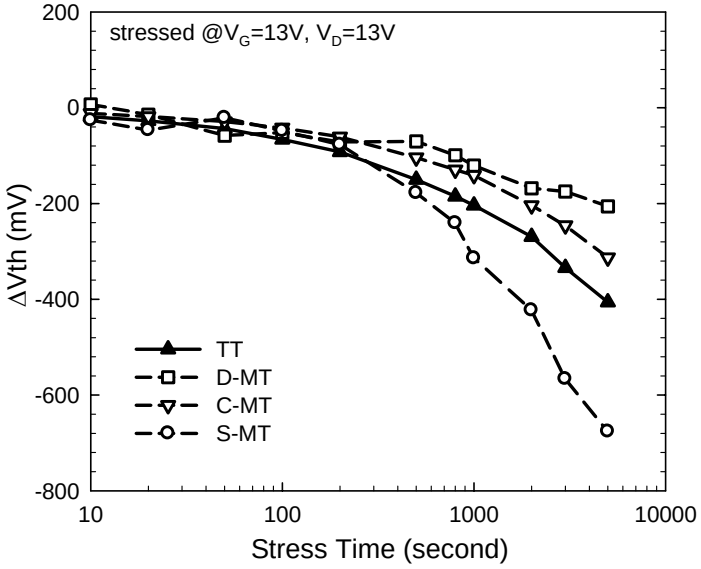

Fig. 4-19 Evolution of threshold voltage shift of a test structure during hot-carrier stress under V_G/V_D=13V/13V.

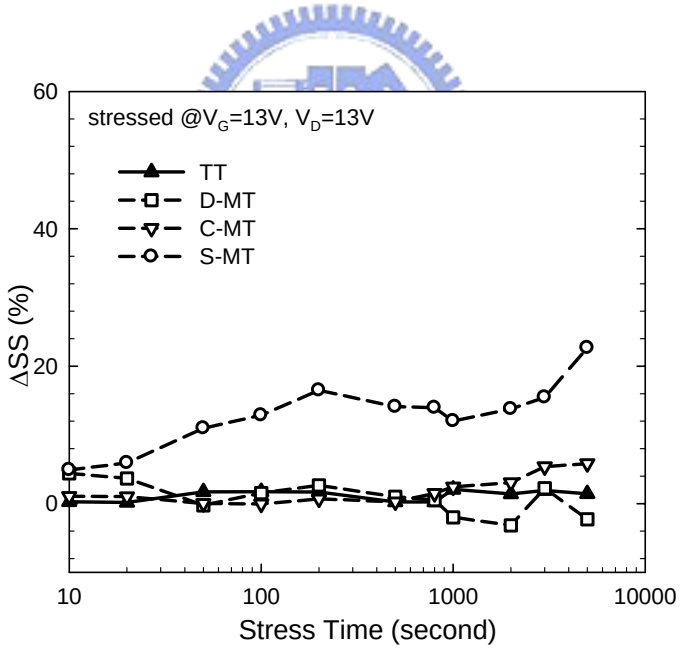

Fig. 4-20 Evolution of subthreshold swing degradation of a test structure during hot-carrier stress under V_G/V_D=13V/13V.

also exhibits negative threshold voltage shift, the extent of shift in the present case (Fig. 4-19) is much larger. For the two stress modes, it is well known that the impact ionization is suppressed under V_G= V_D stress mode [4.18]. This indicates that hole trapping illustrated in

Fig. 4-17 alone cannot account for the observation shown in Fig. 4-18, and some other mechanisms should be responsible for the degradation. It is likely that the oxide field between gate and channel play an important role, as a high gate voltage (e.g., 13V) applied during stressing exerts an oxide field (~ 3.7MV/cm) above the channel near the source side. It has been pointed out previously [4.19] that such field may lead to the generation of positive charges in oxide. The schematics of such process are illustrated in Fig. 4-21. This phenomenon can consistently explain the results observed in this stress mode.

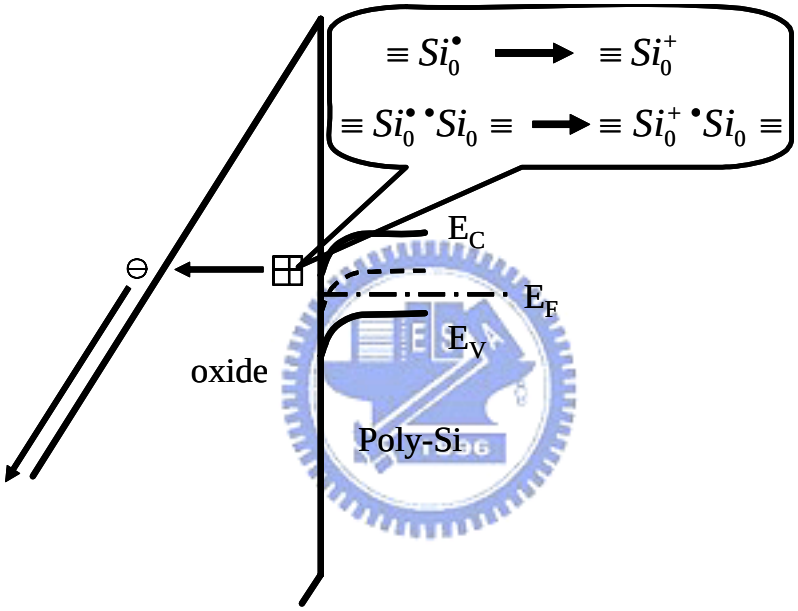

Fig. 4-21 Schematic illustration of the degradation mechanisms under V_G/V_D=13V/13V. The band diagram is taken near the source.

4.7 Effects of post-metal Plasma treatment

The effects of post-metal plasma treatment on density-of-states were also investigated. Hydrogen plasma treatment has been reported to effectively reduce both deep and tail states [4.20], and consequently enhance the performance of TFTs. In recent years, plasma treatments in other ambient such as deuterium [4.21], N_2/H_2 [4.22], and NH_3 [4.23] have been also employed. Diffused hydrogen and nitrogen species have been reported to effectively passivate

the dangling bonds, traps, and defects at grain boundaries and oxide/channel interface [4.19]. As a result, the device performances of TFTs improve, including better subthreshold characteristics, higher on/off current ratio, and lower barrier potential at the grain boundaries.

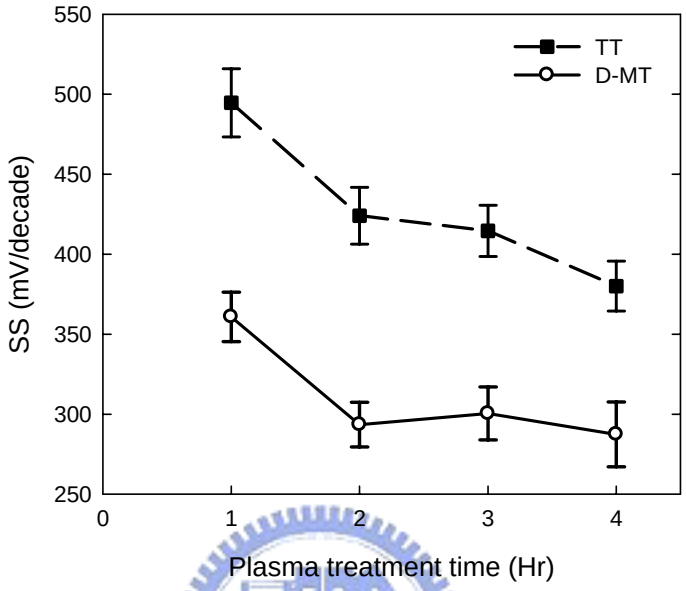

Fig. 4-22 Subthreshold swing of testers (TT and D-MT) after different duration of NH_3 plasma treatment.

Figure 4-22 demonstrates the subthreshold swing of the transistors which received various durations of NH_3 plasma treatment. As can be seen in the figure, for the TTs, the subthreshold swing improves monotonically with increasing treatment time up to 4 hours. The improvement does not saturate in this case because the treatment time is not long enough to passivate all defects inside the channel [4.24]. On the contrary, improvement in subthreshold swing tends to saturate for D-MTs which received more than 2-hours of treatment. This is reasonable since the D-MT, which is located near the edge of the tester, was passivated first and may reach the “saturation” state. Figure 4-23 shows the density-of-states distribution of the transistor which received various durations of NH_3 plasma treatment. The detail about how to extract density-of-states distribution will be introduced in Chapter 6. The defects in deep states ($E < 0.2eV$) were continually passivated up to 4 hours of the treatment. The

phenomenon is in agreement with the fact that deep states in grain boundaries will be passivated first while tail states remain high [4.25] or when the gate oxide is not thick enough so that large amount of hydrogen atoms can be transported into the poly-Si film [4.26].

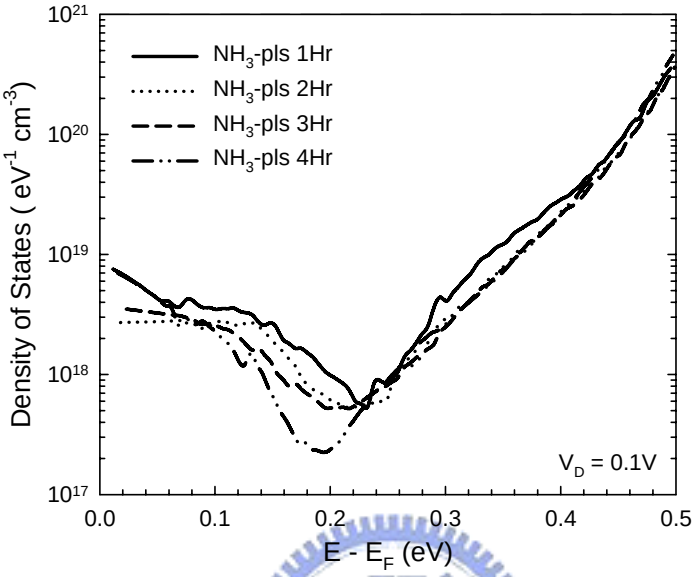

Fig. 4-23 Effective density-of-states distributions of TTs after different durations of NH_3 plasma treatment.

Figure 4-24 demonstrates the result of hot-carrier degradation under V_G/V_D=6.5V/13V for samples which received 1 and 2 hours of NH_3 plasma treatment. Because the tester is stressed under a moderate condition, only the monitor transistor near drain side (D-MT) is sensitive enough to detect the damage. To evaluate the effect of plasma treatment on the hot-carrier degradation, the extracted subthreshold swing shift as a function of plasma treatment time is shown in Fig. 4-25. In contrast to the monotonic improvement in unstressed devices with increasing plasma treatment time, as shown previously in Fig. 4-22, the subthreshold swing shift after the hot-carrier degradation does not show further improvement for devices which received longer plasma treatment. This result may be explained by as follows:

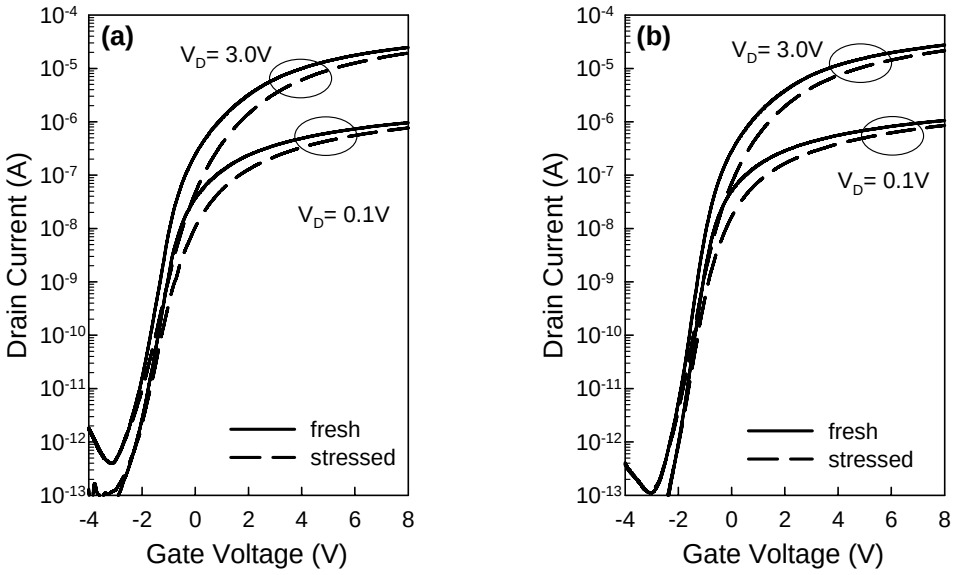

Fig. 4-24 Subthreshold characteristics of D-MTs before and after hot-carrier stressing of V_G/V_D = 6.5V/13V for 1000 sec. Samples received a plasma treatment of (a) 1 hour and (b) 2 hours.

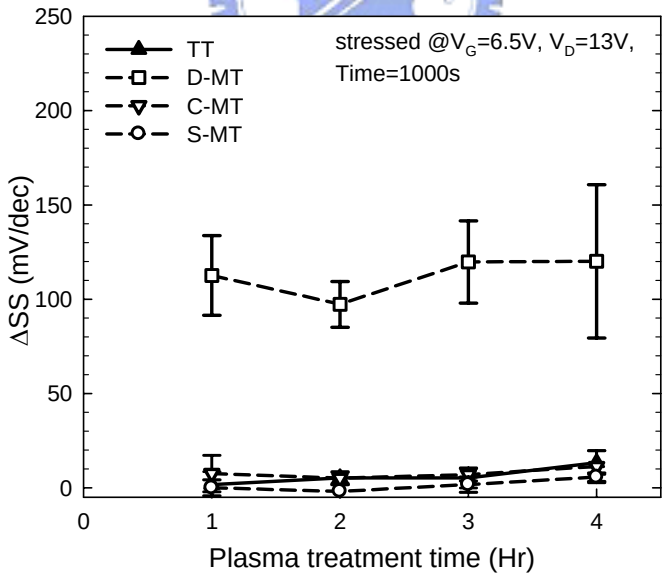

Fig. 4-25 Subthreshold swing shift of testers as a function of NH_3 plasma treatment time. The shift represents the difference of the SS measured before and after hot-carrier stressing.

First, SS of the unstressed D-MTs exhibit no further improvement for treatment time

longer than 2-hours, as shown in Fig. 4-22. This may indicate the saturation of hydrogen passivation. Because the hot-carrier degradation was induced within the region of D-MT, it may not benefit from the longer plasma treatment. Second, because the energy released by hot-carriers is higher than the bonding energy of passivated Si-H bonds, passivated silicon-hydrogen bonds are not strong enough to resist the attack of hot carriers [4.27].

4.8 Summary

In this chapter, we have proposed and successfully demonstrated a new test structure suitable for monitoring the spatial hot-carrier degradation in poly-Si TFTs not previously possible. The fabrication of the proposed test structure is simple and compatible with standard ULSI processing without extra masking.

Several advantages of the test structure are demonstrated in this work: (1) The capability of resolving the damage characteristics in different parts of channel; (2) The greatly enhanced sensitivity in detecting the localized damage, which is helpful for studying the damage characteristics under a milder stress condition; (3) The evolution of degradation in specific regions could also be detected directly; (4) Dominant damage mechanism could be identified. Specifically, in this study we found that at least two mechanisms are responsible for the negative threshold voltage shift detected by the monitor transistors.

Devices which received different NH_3-plasma treatments are also characterized to analyze the effect of treatment time on both unstressed characteristics and resistance against hot-carrier stressing. Although samples show performance enhancement with longer plasma treatment, their resistance against hot-carrier attacking does not improve further.

With these unique features, the proposed test structure represents a powerful tool in practical applications for studying the reliability of TFT devices.

Chapter 5

Analysis of HC Degradation Under AC Operations Using HCTFTs

5.1 Introduction

Poly-Si thin film transistors (TFTs) are important building blocks for system-on-panel (SOP) products [5.1] as well as flexible electronics applications [5.2]. During operations, high pulsed voltages are imposed on the transistors in either peripheral circuits or pixel TFTs [5.3]. Because voltage biases are varied and repeated during the pulse cycle, hot-carrier degradations in AC operations differ from that in DC operations [5.4] which we have discussed in the preceding chapter.

To address the hot-carrier (HC) reliability issues under AC operations, a number of studies were first reviewed. Uraoka *et al.* stressed devices by applying a pulse at gate and grounding source and drain [5.5]-[5.8]. They found that among frequency, rising time, and falling time, the latter one dominates the hot-carrier degradation in AC operations. They also employed pico-second time-resolved photon emission microscope for evaluating the intensity of emitted photons which originated from hot-carrier generation [5.9][5.10]. Their results showed that under dynamic operations, a peak of intensity was observed at gate falling edge. With the decrease of the falling time, the peak intensity increased.

Unlike Uraoka *et al.* who grounded the drain, Toyota *et al.* biased drain at a positive voltage similar to those experiments performed on DC conditions [5.11][5.12]. With the help

of a four-terminal TFT with an embedded p^+ substrate contact, substrate current can be used for evaluating hot-carrier generation. They also investigated and compared the results of hot-carrier degradation between DC and AC operations, and obtained similar conclusions that falling edge acts as the most important factor in AC stress. The LDD structure, which effectively reduces the electric field during transient stage, was demonstrated to successfully alleviate the degradation.

Chang *et al.* [5.13] also performed a series of experiment to investigate several factors, including voltage bias, frequency, rising and falling times, device dimensions, and temperature. They evaluated the degradation in terms of reduction in on-current, as well as the aforementioned source-drain-reversal technique to characterize the electrical properties.

In this work, the proposed test structure is further employed to investigate the HC degradation caused by AC stress. We will evaluate the factors including voltage bias, frequency, rising and falling times. The damaged locations can be directly observed by the structure, and evolutions of the hot-carrier degradation can be easily resolved. At last, we will demonstrate an experiment which resolves two types of degradation simultaneously.

5.2 Experimental setup

In this work, the hot-carrier degradation on TFTs under AC operations is investigated using the proposed HCTFT structure. Samples were fabricated on 6-inch oxidized wafers, with solid-phase recrystallized poly-Si as channel material. Details of the process can be found in Sec. 4.2.

The measurement was performed on the setup constructed by Agilent™ 8110A pulse generator, Agilent™ 4156A semiconductor parameter analyzer, Agilent™ E5250A switch, probe station, and personal computer (PC) with the HP VEE program installed. The computer

acted as the controller, and coordinated all the equipments via GPIB bus. The schematics of the setup are illustrated in Fig. 5-1. The AC stress waveforms used in this work are illustrated in Fig. 5-2. During AC stress, a train of voltage pulses is applied to the gate using Agilent 8110A pulse generator. Rising time (t_r) is defined as the time that the voltage signal rises from 10% to 90% of the amplitude (V_{G_high} - V_{G_low}), and vice versa for falling time (t_f). It should be noted that the total stress time is defined as the summation of t_{high} under the stress condition. In this work, V_{G_low} is set at 0 V and duty cycle is set at 50%. The pulse gate voltage (V_{G_high}) of 6.5 volt and 13 volt were tested in this work.

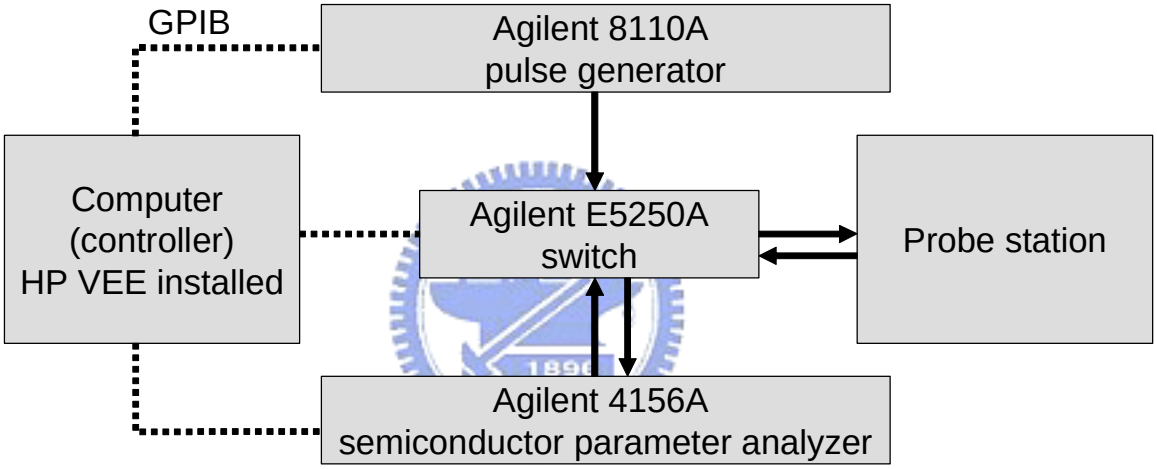

Fig. 5-1 Schematic illustration of the measurement setup.

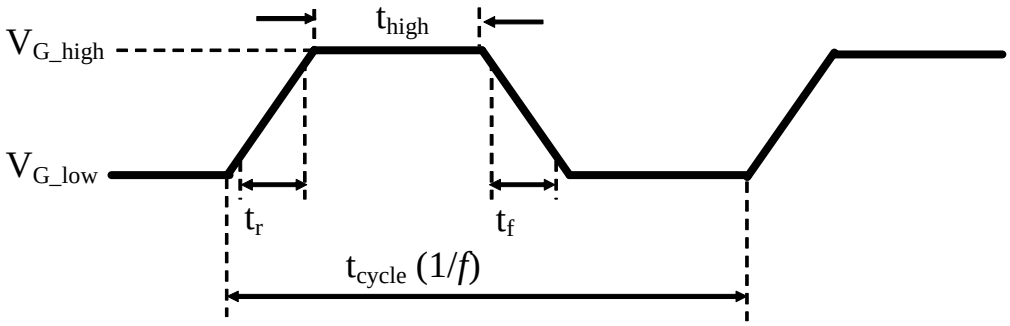

Fig. 5-2 Waveforms of the stress pulse applied to the gate.

5.3 Results and discussion

5.3.1 Effects of frequency

The testers were first stressed under the stress conditions of V_{G_high} = 6.5 V, V_D = 13V, and t_r = t_f = 100ns. Figure 5-3(a) and (b) show subthreshold curves of TTs before and after 1000-sec AC stress under 100kHz and 1MHz, respectively. Though the case of 1MkHz seems worse, the difference in degradation between the two cases is very minor and the damage location cannot be resolved without further examination. In contrast, the subthreshold characteristics of the D-MTs shown in Fig. 5-4(a) and Fig. 5-4(b) clearly indicate that an increase in stress frequency would lead to a higher degradation. In the figures, on-state current and subthreshold swing degradation are both observed under the AC stress. Contrary to the results characterized from the S-MTs, which are shown in Fig. 5-5(a) and Fig. 5-5(b), the location of the induced damage can be easily identified.

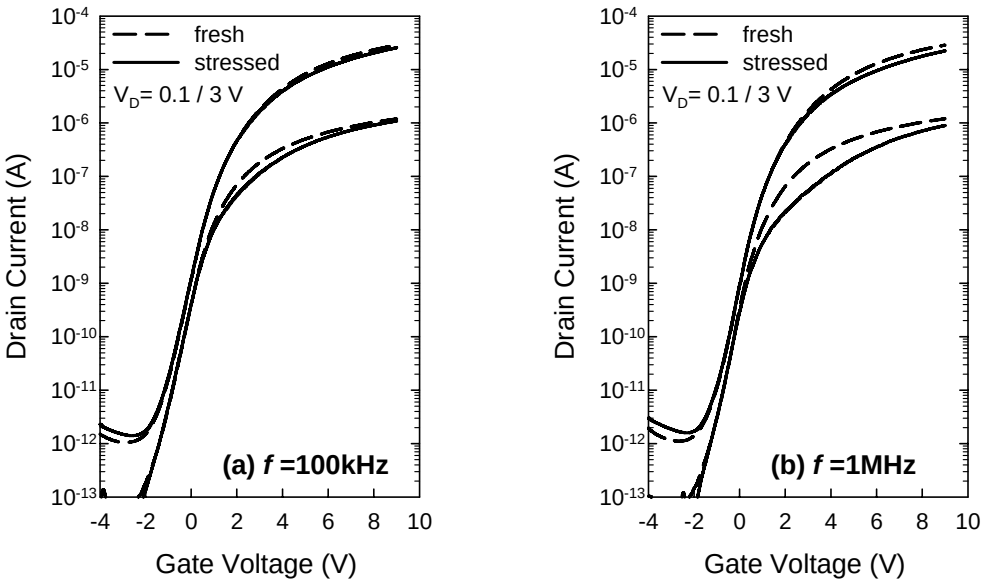

Fig. 5-3 Subthreshold characteristics of TTs before and after AC stress for 1000 seconds with the frequency of (a) 100kHz and (b) 1MHz.

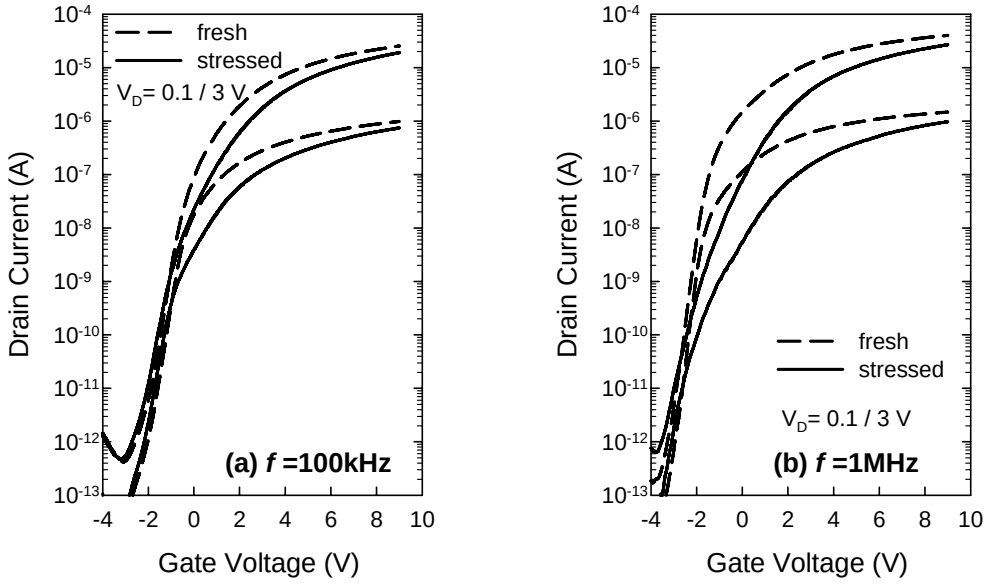

Fig. 5-4 Subthreshold characteristics of D-MTs before and after AC stress for 1000 seconds with the frequency of (a) 100kHz and (b) 1MHz.

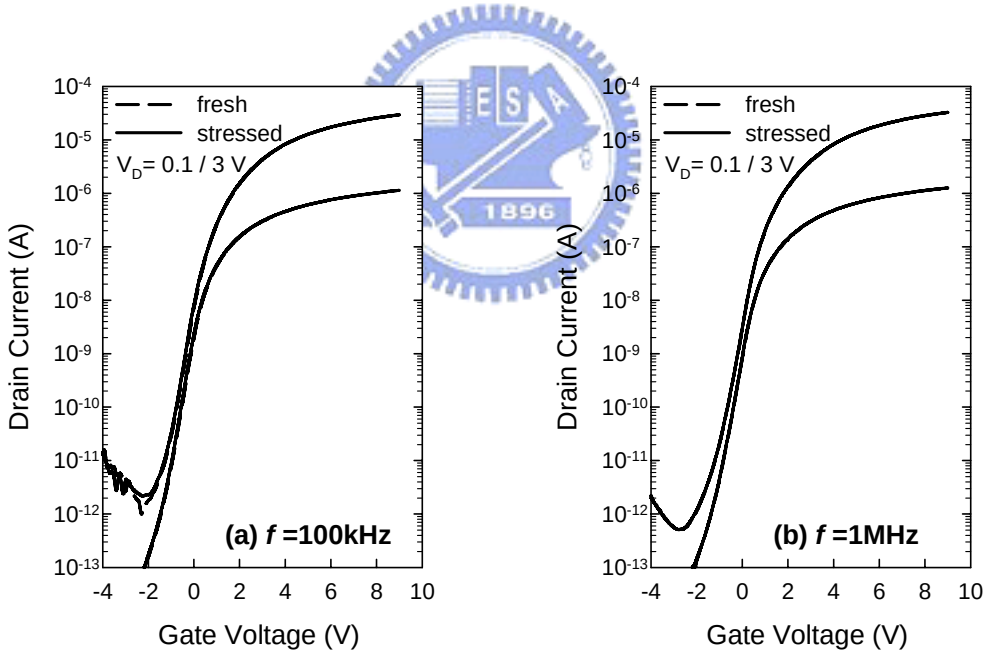

Fig. 5-5 Subthreshold characteristics of S-MTs before and after AC stress for 1000 seconds with the frequency of (a) 100kHz and (b) 1MHz.

To evaluate the impact of hot-carrier degradation more precisely, on-current degradation and threshold voltage shift are shown in Fig. 5-6 and Fig. 5-7, respectively, of TTs and all kinds of MTs. As the characteristics of monitor transistors are compared, major damage

location along the channel of TT is unambiguously identified to be near the drain side. These results again demonstrate the capability of the test structure in spatially resolving the damage location and its excellent sensitivity for detecting the frequency-dependent degradation.

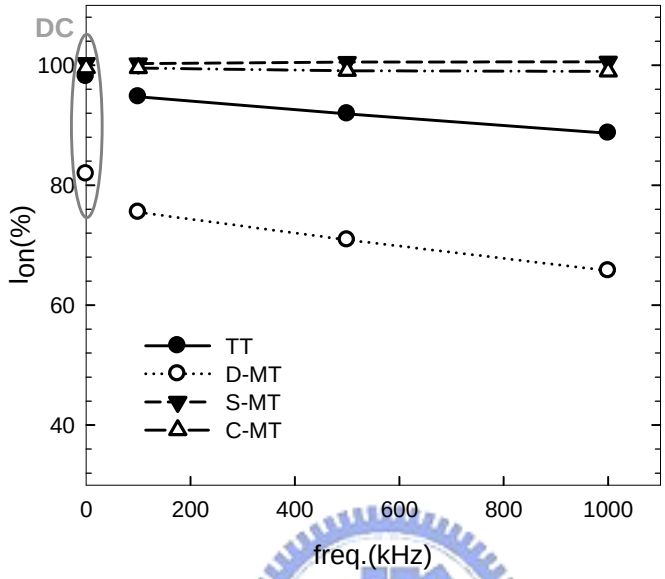

Fig. 5-6 On-current degradation under AC stress with different frequencies.

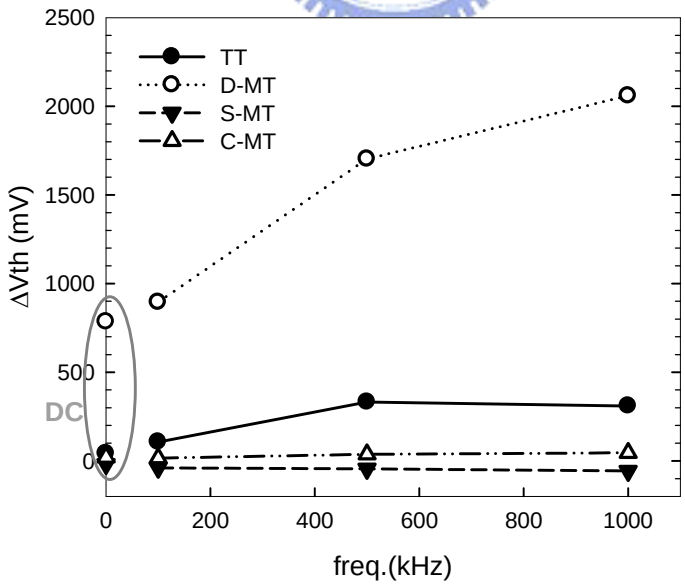

Fig. 5-7 Threshold voltage shift under AC stress with different frequencies.

Possible damage schemes of the tester under AC stress are illustrated in Fig. 5-8. The

waveform of the stress can be divided into four bias conditions: (1) on-state hot-carrier stressing, (2) transient state when gate voltage raises up from V_{G_low} to V_{G_high}, (3) transient state when gate voltage falls down from V_{G_high} to V_{G_low}, (4) off-state stressing caused by localized electric field. In addition to the on-state hot-carrier degradation shown in Fig. 5-8(a), the testers receive transient hot-carrier stressing when elections move rapidly from the inversion layer to the drain (Fig. 5-8(b)). Since for different frequency, the total time under V_{G_high} is the same, the transient stages (t_r and t_f) are the reasonable cause of damage. Most of the generated trap states are located near the drain side of TT, and can be easily detected by D-MT (Fig. 5-8(d)).

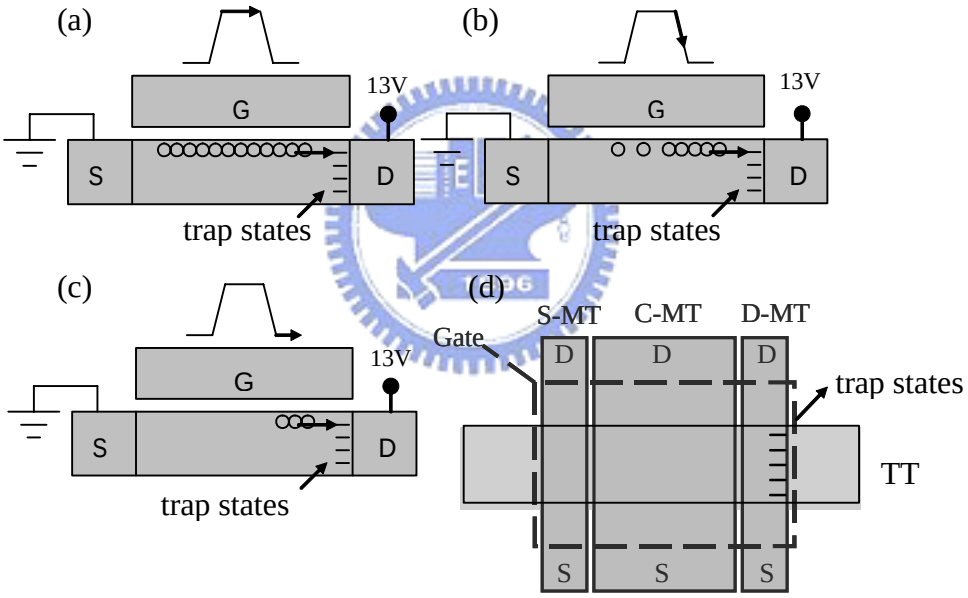

Fig. 5-8 Mechanism of AC stress induced degradation.

To further verify the existence of the stress during the transient stage, the degradation of the testers stressed under different frequencies, but with the same number of switching cycles (i.e., repetitions), are shown in Fig. 5-9. Assuming that the hot-carrier degradation under different frequencies is frequency-independent and instead depends on the repetitions of transient stage, the degradation should be the same for testers which received the same number of repetitions, even if the frequency is different. The result shown in Fig. 5-9

successfully confirms this hypothesis.

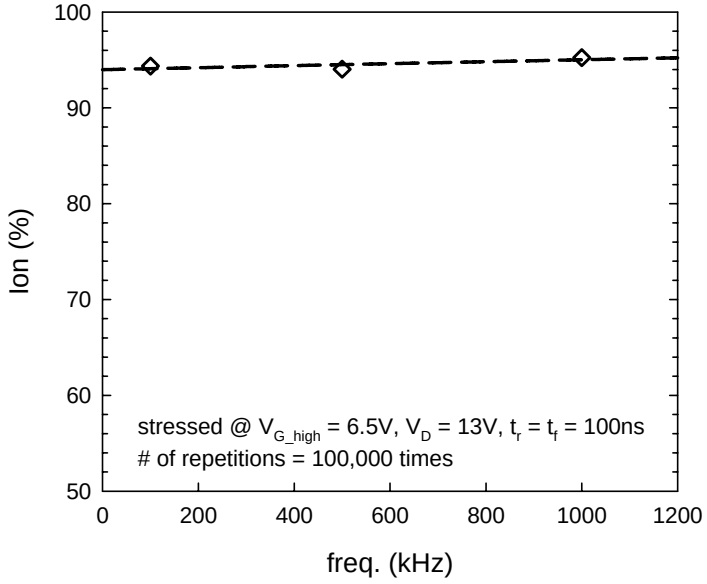

Fig. 5-9 On-current degradation after 100,000 repetitions of AC stressing as a function of frequency.

5.3.2 Effects of rising and falling times

It has been evidenced in the previous section that the transient stages, i.e., rising and falling times, play a very important role on hot-carrier degradation under AC operations. In this section, we will look into the impact of this factor, as well as the additional information which is provided by monitor transistors.

Falling time has been demonstrated to be the most dominant parameter in Uraoka's works [5.5][5.6]. When falling time gets smaller, testers suffer from more severe hot-carrier degradation in field-effect mobility. In contrast, the hot-carrier degradation is independent of the rising time. First the hot-carrier stressing of various rising time were evaluated. The result in terms of on-current (Ion) reduction is shown in Fig. 5-10. It appears that when the rising time varies from 100ns to 10ns, the testers (TTs) show almost identical degradation in

on-current. A similar experiment was also performed to investigate the effect of falling time, which is shown in Fig. 5-11. It clearly illustrates the impact of falling time on on-current. With smaller falling time, the testers receive more hot-carrier stress when operating in AC mode. The result is in agreement with the model proposed by Uroaka [5.5] and Toyata [5.11], which ascribes the transient electric field near drain side, when device is turning off from the on-state, as the culprit. As gate voltage is falling, the electrons in the inversion layer will be swept out from the channel to the source and the drain. Owing to the existence of the high electric field near the drain (V_{GD}), these electrons are accelerated and become the hot electrons. This model is illustrated in Fig. 5-8(b). When the falling time gets shorter, more electrons will remain inside the channel when gate voltage drops down to the level where the electric field is large enough to generate hot electrons. This explains why hot-carrier degradation depends on falling time.

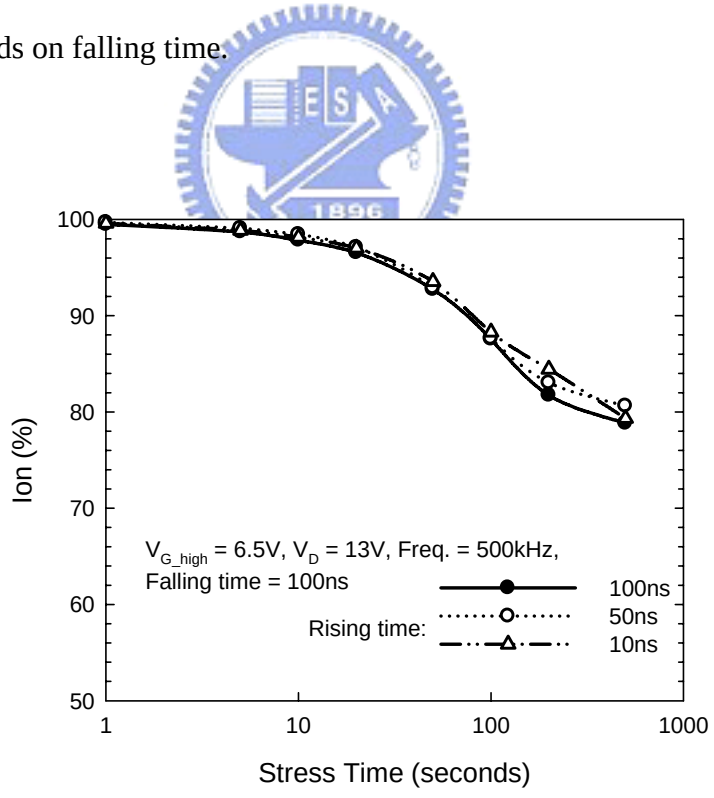

Fig. 5-10 On-current degradation of the testers after hot-carrier stressing with various rising time.

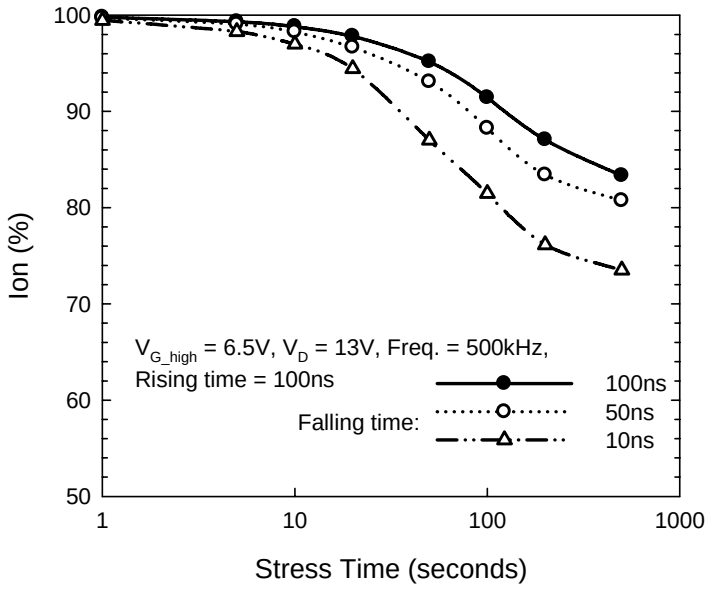

Fig. 5-11 On-current degradation of the testers after hot-carrier stressing with various falling time.

Again with the help of monitor transistors, the effect can be amplified and the damaged location can be directly resolved. The hot-carrier degradation in terms of on-current reduction for HCTFTs stressed with various rising and falling times are shown in Fig. 5-12 and Fig. 5-13, respectively. In both figures, it can be clearly seen that the damage region is located near drain, which is represented by the data from D-MTs. The result also shows that falling time dominates the degree of degradation, while rising time has no effect on the degradation.

To observe the effect of the falling time on hot-carrier degradation, subthreshold characteristics of TTs and MTs are shown in Fig. 5-14 and Fig. 5-15, respectively. As can be seen in these figures, the degradations of D-MTs are more obvious than those of TTs. As a result, the difference in degradation among various falling times can be observed more easily. As revealed in TT's data, the degradation in terms of on-current reduction, degradation of the current when gate is bias near the threshold voltage (V_G ~ V_{TH}), and increase of the

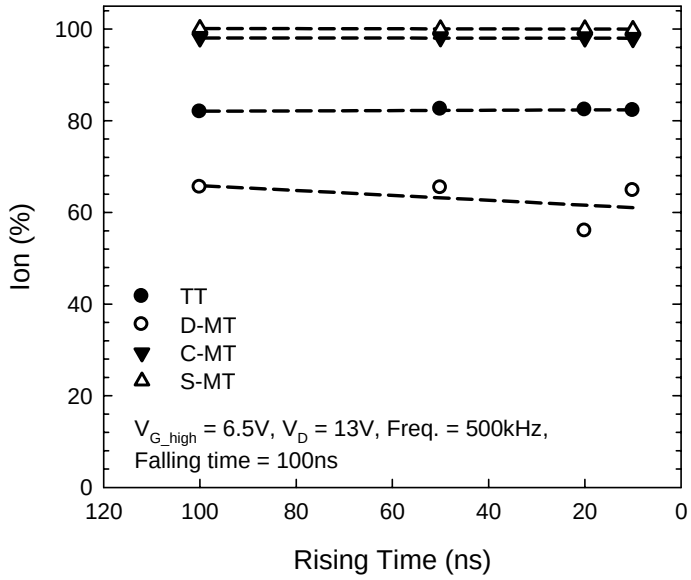

Fig. 5-12 On-current degradation of the testers after hot-carrier stressing as a function of rising time.

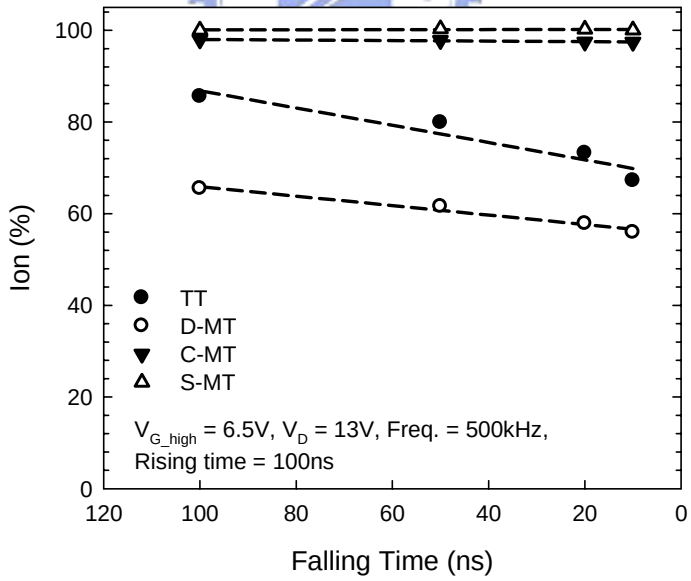

Fig. 5-13 On-current degradation of the testers after hot-carrier stressing as a function of falling time.

off-state current in higher V_D (V_D=3V). Detail mechanisms for the former two have been discussed in the previous chapter, and both can be observed more clearly in the result from the

D-MTs. Now we are going to discuss the difference in the off-state current between TTs and D-MTs. The increase of off-state current for the stressed devices is obvious in TTs (Fig. 5-14), but disappears in D-MTs (Fig. 5-15). Why?

In planar TFT structure, most of the off-state leakage originates near the drain junction due to the high electric field between gate and drain. Because the hot-carrier degradation in

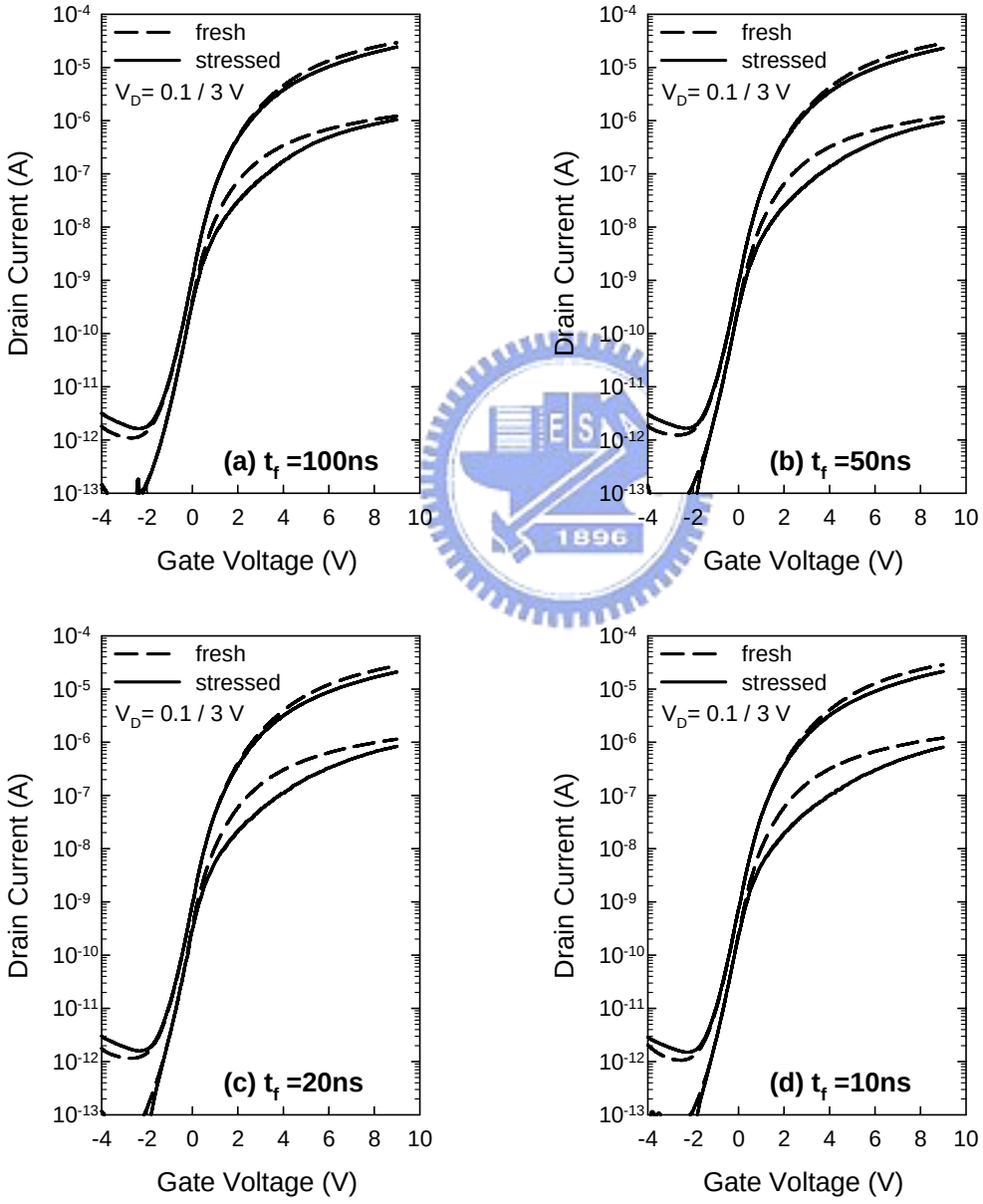

Fig. 5-14 Subthreshold characteristics of TTs after hot-carrier stressing with different falling time.

this case is also located at the same region, as shown in Fig. 5-16(a), the off-state leakage of the TT understandably increases. Now consider the case of D-MTs, as shown in Fig. 5-16(b). It is very clear that when the D-MT is biased at off-states, the leakage generation site differs from the region which is damaged by the hot-carrier stressing. This explains why the off-state leakage remains unchanged when using D-MT for monitoring the degradation.

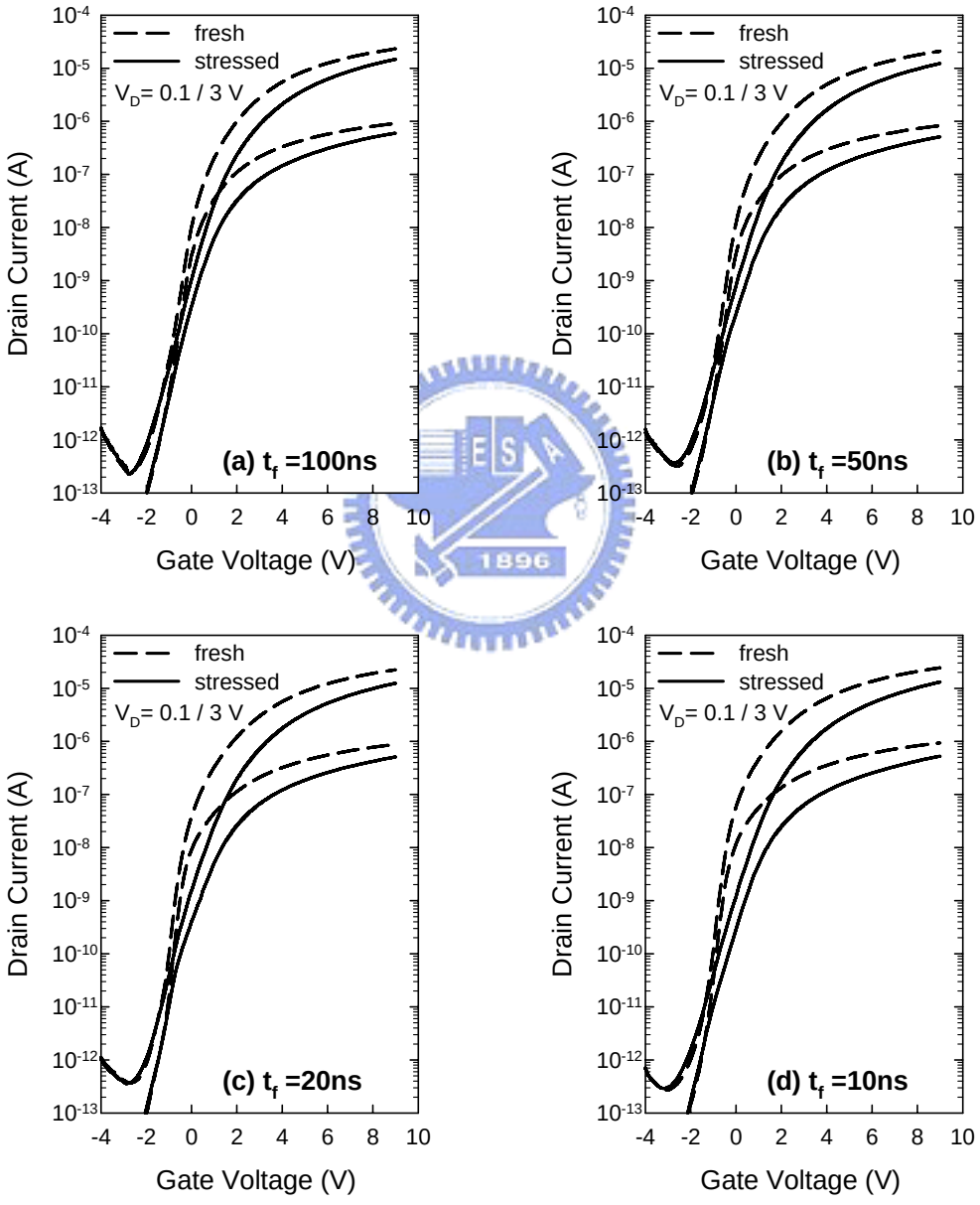

Fig. 5-15 Subthreshold characteristics of D-MTs after hot-carrier stressing with different falling time.

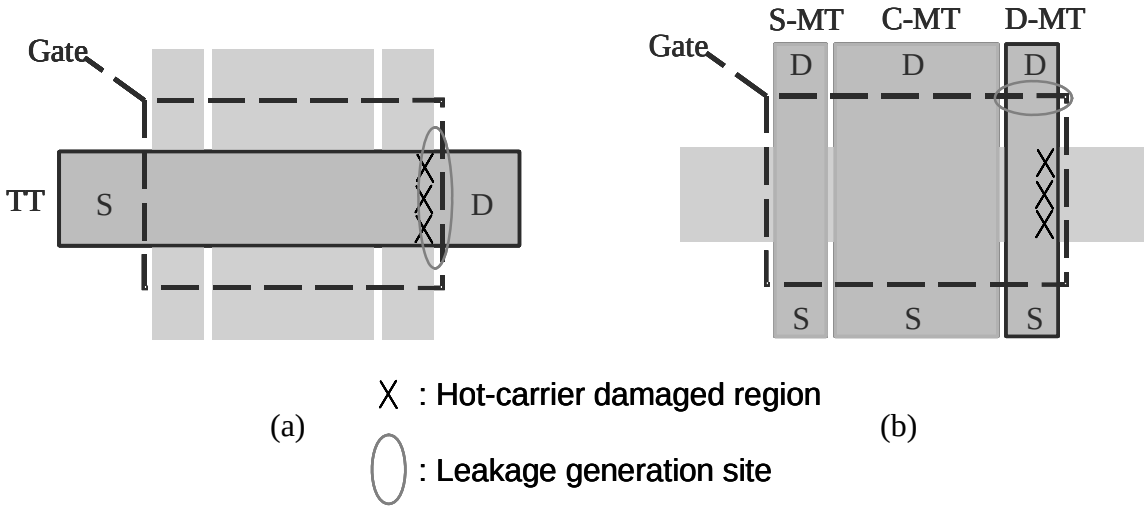

Fig. 5-16 Schematic illustration of the relative location between the hot-carrier-damaged region and the leakage generation site.

5.3.3 Temporal evolution under AC stressing

In this section, a complicated case where two different types of degradation simultaneously occur at different portions of channel, along with the analysis using temporal evolution, is demonstrated. It reveals the capability of resolving several reliability issues at the same time. In this case, the tester was stressed under the following conditions: V_{G_high} = 13V, V_D = 13V, frequency of 500 kHz, rising time of 100ns, and falling time of 100ns.

The evolution of subthreshold characteristics for the tester is shown in Fig. 5-17. The curves in TT (Fig. 5-17(a)) reveal that more than one type of degradation might have occurred, including slight parallel shift in bottom half of the subthreshold region, and degradation in the upper half. The combination of these two phenomena increases the difficulty in understanding the whole picture. After characterizing all monitor transistors, a clear picture can be easily resolved. The parallel shift in bottom half of subthreshold region can be detected in S-MT (Fig. 5-17(b)), with a great enhancement in sensitivity. The shift is mainly originated from the on-state stage (V_{G_high}) of the waveform. The detail of the shift under V_G = 13V, which is owing to the generation of positive charges in the oxide, has been discussed in Section 4.6. In

the mean time, another degradation observed in the D-MT (Fig. 5-17(d)) is contributed by the transient electric field near the drain, which is originated in transient stage.

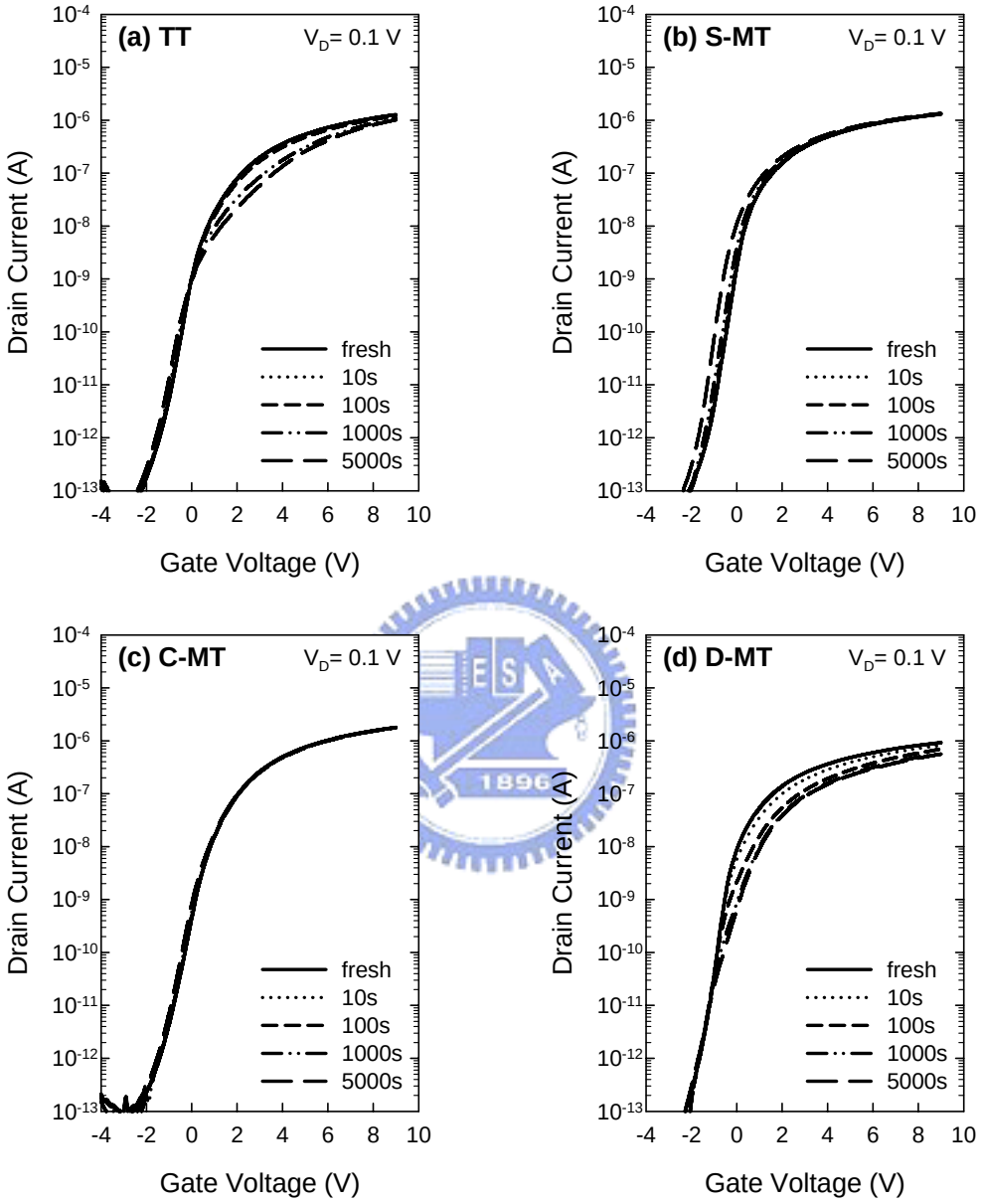

Fig. 5-17 Evolution of subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT in the tester during hot-carrier stressing under V_{G_high}/V_D=13V/13V, freq. = 500 kHz, $t_r = t_f$ = 100ns.

By extracting the evolutions of each MTs in terms of shift in threshold voltage, shift in subthreshold swing, and on-current degradation, the whole picture becomes more clear. They are shown in Fig. 5-18 to Fig. 5-20, respectively.

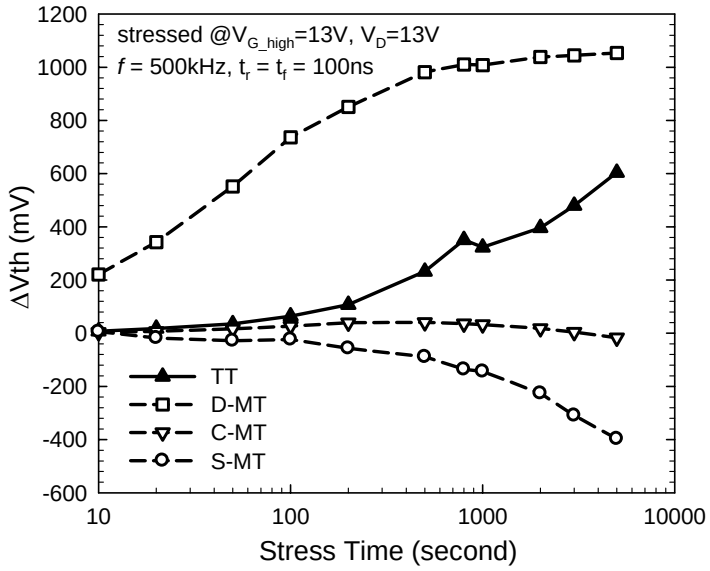

Fig. 5-18 Evolution of the shift in threshold voltage for the same tester shown in Fig. 5-17.

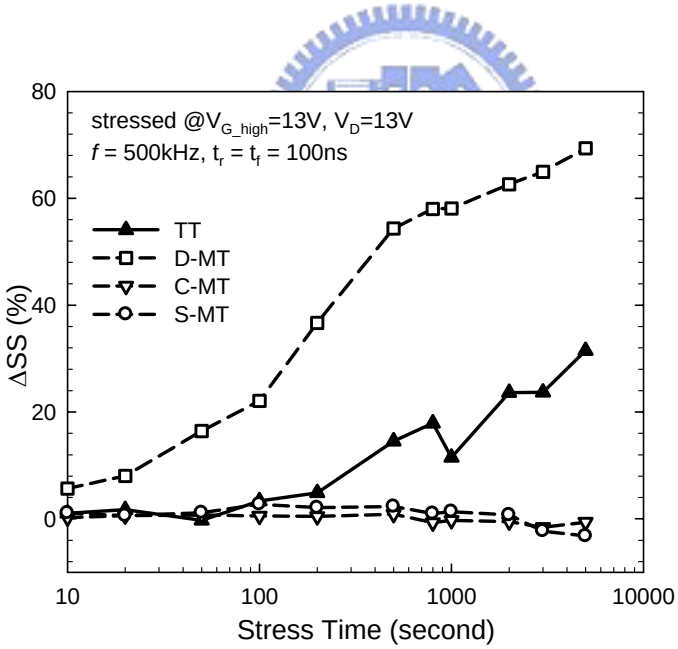

Fig. 5-19 Evolutions of the subthreshold swing shift of the same tester shown in Fig. 5-17.

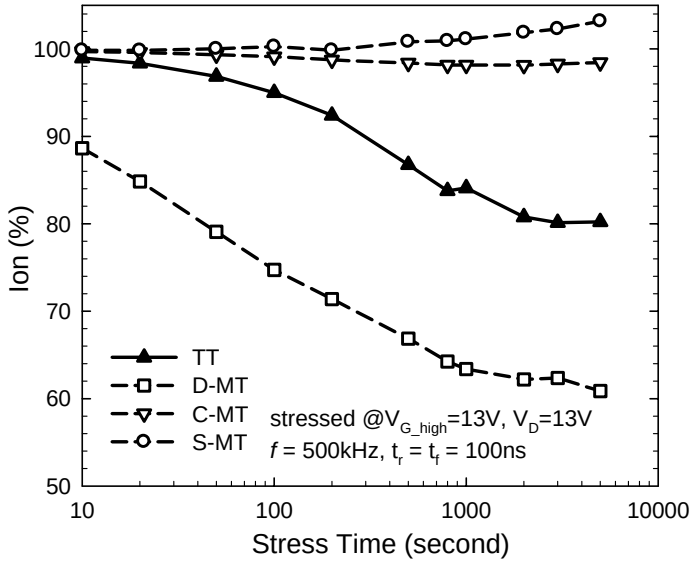

Fig. 5-20 Evolutions of on-current degradation of the same tester shown in Fig. 5-17.

The degradation detected in S-MT causes the negative shift in threshold voltage, and consequently increases the on-current of S-MT (because on-current is proportional to the square of V_G-V_{TH}). In the mean time, the degradation detected in D-MT unambiguously results in the positive shift in threshold voltage and subthreshold swing, and reduces on-current.

5.4 Summary

In this chapter, HCTFT was employed in the analysis of hot-carrier degradation under AC operations. The effect of several factors are investigated and discussed, including frequency, rising time, and falling time. The phenomena of hot-carrier degradation can be spatially resolved using the proposed novel tester. By applying such tester to AC hot-carrier stressing, the relationship between different stages of the input signal and resultant damage location can be established. The tester also shows a high sensitivity in detecting even mild AC degradation. The experiment provides unambiguous evidence that the damage occurs during transient stages, with the aid of the novel test structure.

We also demonstrated the capability of the tester in spatially and temporally resolving several degradations simultaneously occurring in different portions of channel. Two different types of degradation are simultaneously identified with the help of the monitor transistors.