Chapter 6

Effective Density-of-states Distributions for Hot-carrier Degradations in Poly-Si TFTs

6.1 Introduction

One of the major concerns associated with performance improvements in poly-Si TFTs is the stability and reliability issues. Hot-carrier (HC) degradation remains as one of the most critical concerns for practical applications [6.1]-[6.3]. Hot carriers are caused by high electric field existing in the channel. By releasing their energy, these hot carriers could cause defect generation and performance degradation [6.4]. Since the electric field across the channel is not uniformly distributed, hot-carrier induced damages are location-dependent in the channel. Owing to the lack of substrate contacts, together with the presence of numerous inter-/intra-grain defects [6.5], the whole picture is much more complicated for poly-Si TFTs, compared with their single-crystal counterparts. The damage scenario of the HC degradation has been characterized in literature by a number of techniques, including reversed source/drain measurement [6.6], capacitance-voltage (C-V) measurement [6.7], device simulation [6.8][6.9], asymmetric drain/source structure [6.6], and pico-second time-resolved emission microscope [6.10]. However, all the above methods failed to directly and unambiguously pinpoint the damage location.

To model the HC degradation is more challenging. Trap states associated with grain boundaries, intragranular defects, and hot-carrier-induced defects can be taken into account through the use of effective density-of-states (DOS) distribution within the band gap

[6.11]-[6.14]. Nevertheless, realistic DOS distribution is very difficult to obtain owing to the non-uniform distribution of the induced states during HC stressing.

Effective density-of-states distribution in poly-Si channel film can be calculated from the subthreshold current-voltage (I-V) characteristics using the field-effect conductance (FEC) method [6.15]. Unlike other methods such as optical absorption [6.11], doping dependence of conductivity [6.16], capacitance-voltage (CV) [6.17], and deep level transient spectroscopy (DLTS) [6.18], field-effect conductance method possesses several advantages and has been widely used. The method was first proposed by Suzuki *et al.* for amorphous silicon films [6.19]. Fortunato *et al.* applied this method to poly-Si films [6.20].

6.2 Experimental setup of density of states extraction using FEC method

Since FEC method was originally proposed for amorphous-Si films, it assumes the spatial distribution of defect states, including grain boundary and intragranular defects, is uniform throughout the channel [6.15]. This assumption is reasonable when the grain size of the poly-Si film is small.

6.2.1 Flat-band voltage determination

At first, the flat-band voltage must be obtained using temperature method. It is based on the following equation that differentiates the logarithmic conductance with respect to gate voltage [6.21]:

$$\frac{d\log G}{dV_G} \cong \frac{\varepsilon_{0x}}{t_{0x}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_s}{KT}\right)+O\left(\frac{q\psi_s}{KT}\right)^2 ...\right] \qquad \text{Eq. 6-1}$$

The flat-band voltage (V_{FB}) can be determined when $T\cdot(d\log G/dV_G)$ is independent

of the temperature. We will demonstrate the experiment later in Section 6.2.4.

6.2.2 Relationship between current-voltage and surface band-bending

To construct the relationship between measured current-voltage characteristics and surface band-bendings, the incremental method [6.15] is employed. This method begins with the field conductance defined in [6.19]:

$$G = G_0 - \frac{G_0}{d}\int_0^{\psi_s} \frac{\exp(q\psi / kT) - 1}{d\psi / dx} d\psi \qquad \text{Eq. 6-2}$$

Here G_0 and d represent the conductance for the flat band condition and the thickness of the poly-Si channel.

The electric field at the surface can be given from the voltage drop at the surface:

$$\frac{d\psi}{dx}|_{x=0} = -\frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{0x}}{t_{0x}} = -\frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_G - V_{FB} - \psi_S}{t_{0x}} \qquad \text{Eq. 6-3}$$

By differentiating Eq. 6-2 with respect to ψ_s, and substituting the Eq. 6-3 into the result, the following equation will be obtained:

$$\frac{d\psi_s}{dG} = \frac{1}{G_0} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{d}{t_{0x}} \cdot \frac{V_G - V_{FB} - \psi_s}{\exp(q\psi_s / KT) - 1} \qquad \text{Eq. 6-4}$$

By rewriting Eq. 6-4 using the differential form, and substituting the conductance by the drain current:

$$\frac{G_{i+1} - G_i}{G_0} = \frac{I_{D,i+1} - I_{D,i}}{I_{D,0}} \qquad \text{Eq. 6-5}$$

The relationship between current-voltages and surface band-bendings can be obtained:

$$\psi_{s,i+1} = \psi_{s,i} + \frac{I_{D,i+1} - I_{D,i}}{I_{D,Flatband}} \cdot \frac{d}{t_{0x}} \cdot \frac{\varepsilon_{0x}}{\varepsilon_{Si}} \cdot \frac{V_{G,i} - V_{FB} - \psi_{S,i}}{\exp(q\psi_{Si} / KT) - 1} \quad \text{Eq. 6-6}$$

Using the initial condition that $\psi_{S,i=0} = 0$, we can calculate $\psi_{S,1}$, $\psi_{S,2}$ ... $\psi_{S,N}$ for $V_{G,1}$, $V_{G,2}$ ... $V_{G,N}$.

6.2.3 Density of states in terms of surface band-bending

The band bending in such an "effective medium" can be expressed as a solution of one-dimensional Poisson's equation:

$$\left.\frac{d^2\psi}{dx^2}\right|_{x=0} = -\frac{\rho(x)}{\varepsilon_{Si}} \quad \text{Eq. 6-7}$$

Here ψ represents the band-bending, and $\rho(x)$ stands for the charge density per volume.

The $\rho(x)$ can be expressed as the integral of density of states $Ng(E)$ from Fermi level (E_F) to the potential of band-bending ($E_F + q\psi$):

$$\rho(\psi) = -q \int_{E_F}^{E_F + q\psi} Ng(E)dE \quad \text{Eq. 6-8}$$

Now multiplying Eq. 6-8 by $2 \cdot \partial\psi / \partial x$, and integrating from $x = 0$ to $x = d$ (from channel surface to bottom of the channel), the electric field at the surface ($\frac{d\psi}{dx}|_{x=0}$) can be given as:

$$\left(\frac{d\psi}{dx}|_{x=0}\right)^2 = \frac{2q}{\varepsilon_{Si}} \int_0^{\psi_s} d\phi \int_{E_F}^{E_F + q\psi} Ng(E)dE \quad \text{Eq. 6-9}$$

By rearranging the terms and differentiating the equation by $\frac{\partial^2}{\partial \psi_s^{\,2}}$, the DOS of a given energy inside the band-gap can be expressed as:

$$DOS(E_F + \psi_s) = \frac{\varepsilon_{Si}}{2q} \frac{\partial^2}{\partial \psi_s^{\,2}} \left(\frac{d\psi}{dx} |_{x=0} \right)^2 \qquad \text{Eq. 6-10}$$

In Eq. 6-10, E_F, ψ_s, and ε_{Si} represent Fermi energy, the surface band-bending at channel/gate-oxide interface, and dielectric constant of silicon, respectively.

6.2.4 Experimental setup for DOS extraction

Now we are going to demonstrate the experiment by extracting a set of DOS from a series of I-V data. First the I_D-V_G curves at different temperatures were measured, as shown in Fig. 6-1. For each gate voltage (V_G), the value of $T \cdot (d \log G / dV_G)$ was then calculated and plotted, as can be seen in Fig. 6-2. To satisfy the condition that $T \cdot (d \log G / dV_G)$ is

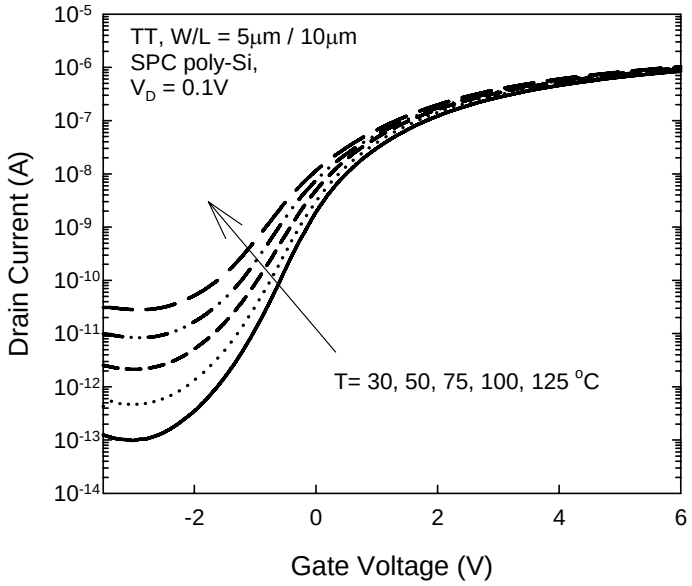


Fig. 6-1 Subthreshold characteristics of TT measured at different temperatures.

independent of the temperature, the plotted line of smallest slope was chosen. In this case, voltage of -3.2 volt was chosen as the flat-band voltage.

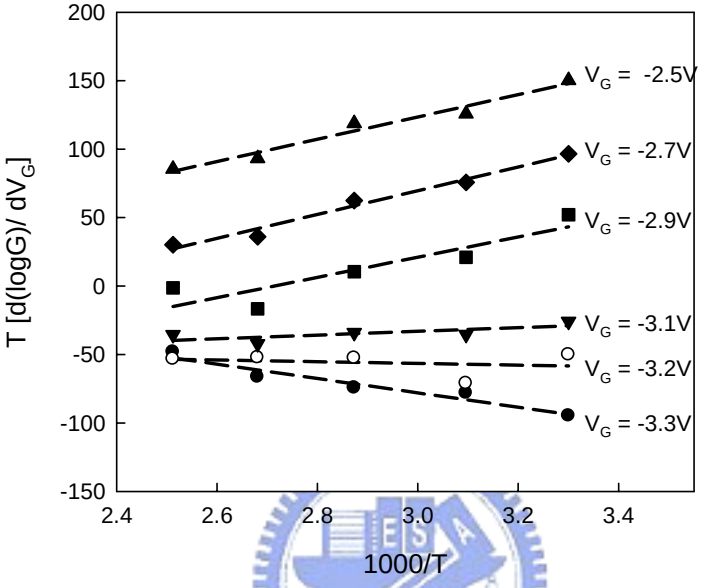


Fig. 6-2 Plots of $T \cdot (d \log G / dV_G)$ as a function of 1000/T.

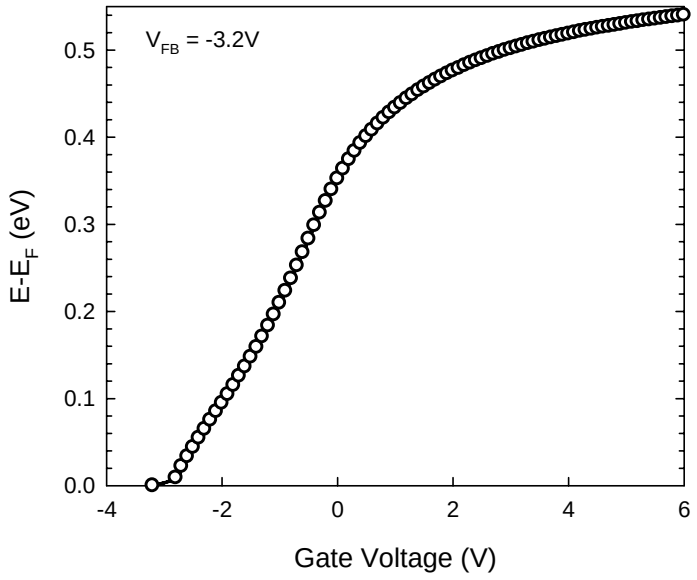


Fig. 6-3 Extracted surface band-bending as a function of gate voltage.

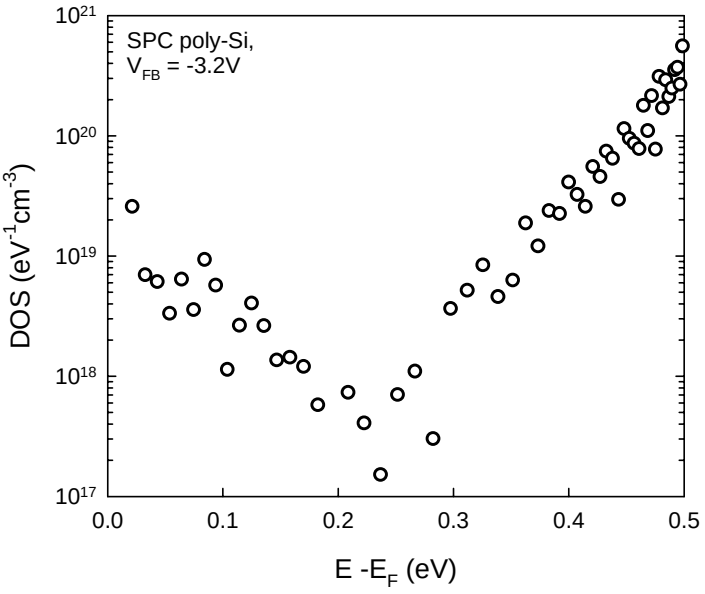


Fig. 6-4 Calculated density-of-states as a function of surface band-bending.

After flat-band voltage determination, the relationship between gate voltage and surface band-bending was constructed using the aforementioned incremental method. The result is shown in Fig. 6-3. Afterwards, the resultant DOS was calculated and plotted in Fig. 6-4.

In this work, flat-band voltages of test transistor and monitor transistors were first characterized, respectively. The tester was then stressed under the condition of V_G/V_D = 6.5/13V. The subthreshold characteristics before and after the stressing were then used to calculate the corresponding density-of-states, especially for the D-MT which represents the damaged region near the drain.

6.3 Experimental setup of device simulation

Integrated System Engineering (ISE) TCAD^{TM} was used to simulate the subthreshold I-V characteristics of poly-Si TFTs using the aforementioned device structure, size parameters, and the extracted DOS distributions. A two-dimensional structure was constructed using MDRAW^{TM} and MESH^{TM}. To match the realistic TFT characteristics, density-of-states

distributions inside poly-Si channel must be constructed according to the distribution extracted by the aforementioned method. One Gaussian and two exponential distributions were given to meet the DOS distribution used for simulation. For example, the extracted DOS distribution which was calculated from a test transistor is shown by the circles in Fig. 6-5. Three curves, marked as "sim part (1 to 3)", represent the corresponding distribution. It can be seen that the summation of these three curves, which is represented by the solid line, matches the experimental results.

After structural construction was completed, DESSIS^{TM}, which is a device simulator incorporated with several physical models, was then used to obtain simulated subthreshold characteristics of the tester.

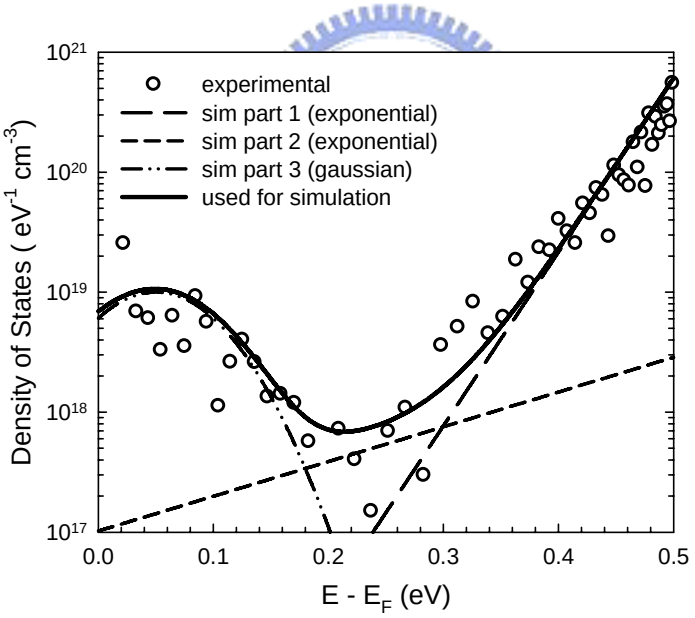


Fig. 6-5 One Gaussian and two exponential distributions used to represent the extracted DOS distribution.

6.4 Results and Discussion

In this work, all the samples characterized are identical to those used in the preceding chapter. The setup for characterizing the electrical properties and applying the hot-carrier

stressing is also the same as that described in the preceding chapter.

6.4.1 Density of states before and after the hot-carrier stress

Figure 6-6(a) shows the subthreshold characteristics of the test transistor before and after a moderate hot-carrier stressing. The device was biased under a gate voltage of 6.5 volt and a drain voltage of 13 volt for 1000 seconds. In this case, hot-carrier degradation cannot be observed through the subthreshold characteristics because the damaged region is very small compared to the whole channel. By contract, as shown in Fig. 6-6(b), the retarded I-V characteristics of the monitor transistor near drain (D-MT) clearly reveal the existence of damages in poly-Si film. The information from D-MTs can provide excellent sensitivity in characterizing the hot-carrier degradation.

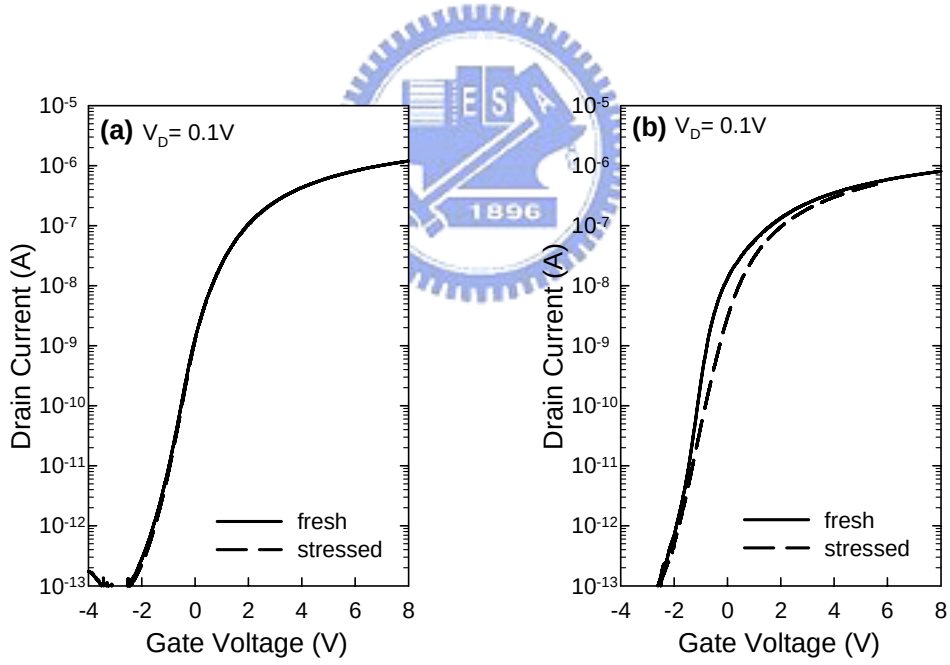


Fig. 6-6 Subthreshold characteristics of (a) TT and (b) D-MT, before and after hot-carrier stressing under V_G/V_D = 6.5V/13V for 1000 sec.

For the conventional tester, the task becomes more arduous when trying to resolve the difference in DOS distribution during HC degradation. The DOS distribution calculated from TT is shown in Fig. 6-7. It can be seen that it is very difficult to resolve the effect of

hot-carrier degradation. This is because only a small portion of the channel is damaged, and the increased DOS is averaged when extracting DOS distribution from the whole channel. In contrast, since the hot carrier degradation occurs near drain side, the generated states can be treated as more uniformly distributed inside D-MT. The DOS distributions calculated from the D-MT before and after the hot-carrier stressing are shown in Fig. 6-8(a) and Fig. 6-8(b), respectively. It can be clearly and easily seen that DOS increases, especially when the surface potential varies from 0.15 to 0.3 eV above the Fermi level.

The result is very similar to "Type 2 of stress-created defects" proposed by M. Hack *et al.* [6.22]. They proposed that two types of defects are generated during hot-carrier stressing. "Type 1" defect is generated when the device is stressed under linear conditions ($V_G > V_D$), and can be modeled as the increase in DOS near the mid gap. "Type 2" defect, which is similar to what we found, is generated when the device is stressed in saturation ($V_G < V_D$), and can be modeled as the increase in DOS located 0.2 to 0.3 eV above the Fermi level.

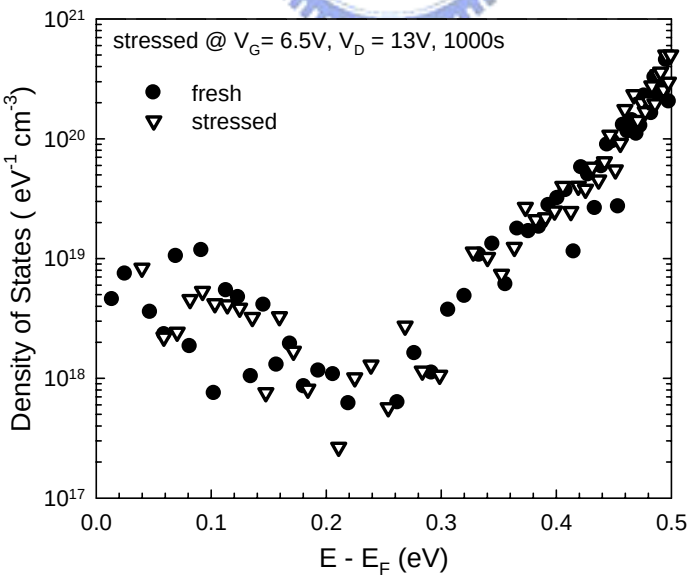


Fig. 6-7 Effective density-of-states distribution of TT before and after hot-carrier stressing under V_G/V_D = 6.5V/13V for 1000 sec.

They found that by adding "Type 2" defects in the region 1-μm near the drain, the simulated

subthreshold characteristics can match their experimental results. However, their conclusion is based on the simulated results which assume specific location of generated defects. In contrast, we provide a direct evidence for the corresponding position within the band-gap and the spatial location of such type of defect.

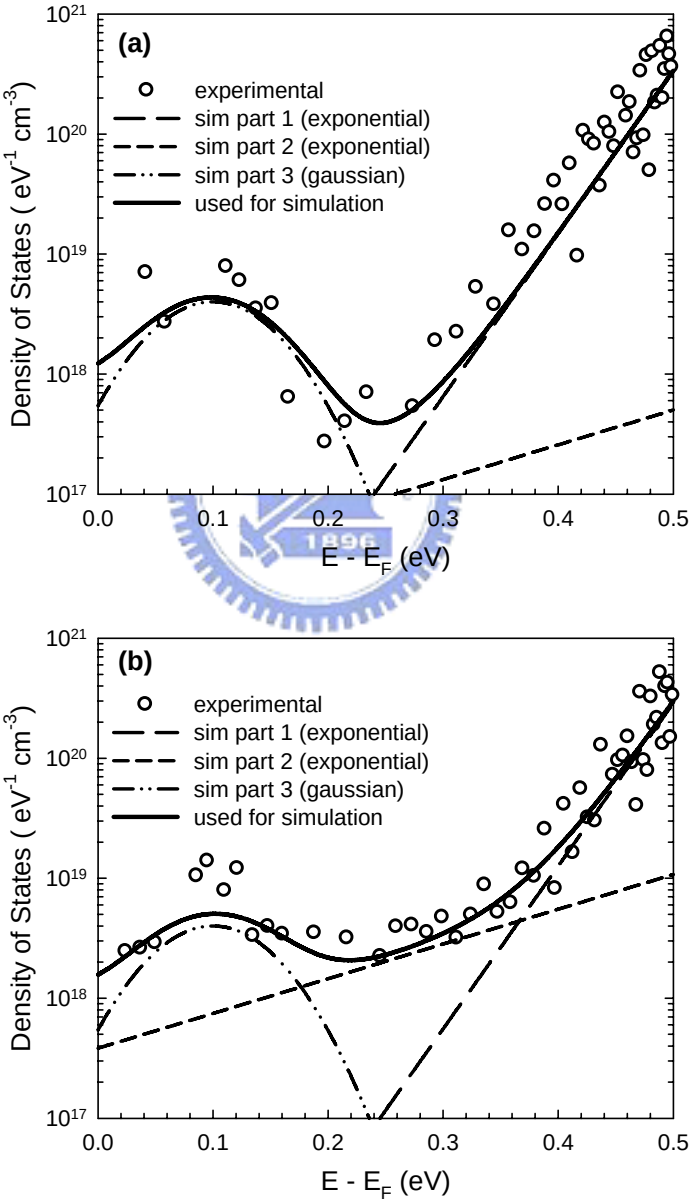


Fig. 6-8 Effective density-of-states distribution of D-MT (a) before and (b) after hot-carrier stressing under V_G/V_D = 6.5V/13V for 1000 sec.

The result demonstrates the capability to resolve the position of generated states within the band-gap, and enables us to identify the types of vulnerable bonds when the device is under the attack of hot carriers.

The region in which DOS increases can be mapped back to the original I-V characteristics, and helps us find out which portion of I-V curve is responsible for the degradation. The demonstration of such technique is shown in Fig. 6-9. The relationship between surface energy and gate voltage is plotted in Fig. 6-9(a). Once the energy between the two dashed lines ($0.15eV < E - E_F < 0.30eV$) is given, the corresponding gate voltage can be found. Afterwards, the marked region in Fig. 6-9(b) reveals the calculated regions where the increased DOS comes from. This opens up the possibility of monitoring the change of DOS from the change in the subthreshold characteristics.

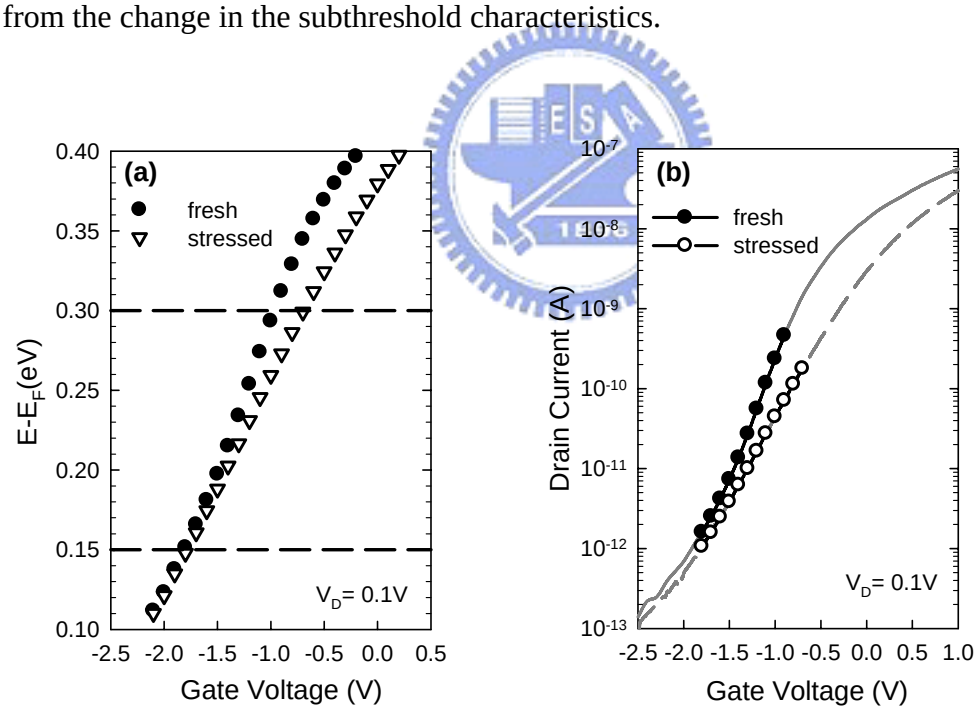


Fig. 6-9 (a) Relationship between gate voltage and extracted surface energy and (b) mapping of the increased DOS on subthreshold characteristics, before and after hot-carrier stressing under V_G/V_D = 6.5V/13V for 1000 sec.

The extracted DOS distributions were also used for device simulation, in order to recreate the I-V characteristics, and validate the extracted DOS results. Details of simulation

have been described in the previous section. After feeding the extracted DOS distributions into the simulator, which is described as the dashed line in Fig. 6-8, the subthreshold characteristics of the D-MT before and after the hot-carrier stressing were calculated. The simulated I-V curves, which are shown in Fig. 6-10(a) and (b), fit well with the measurement for both fresh and stressed samples.

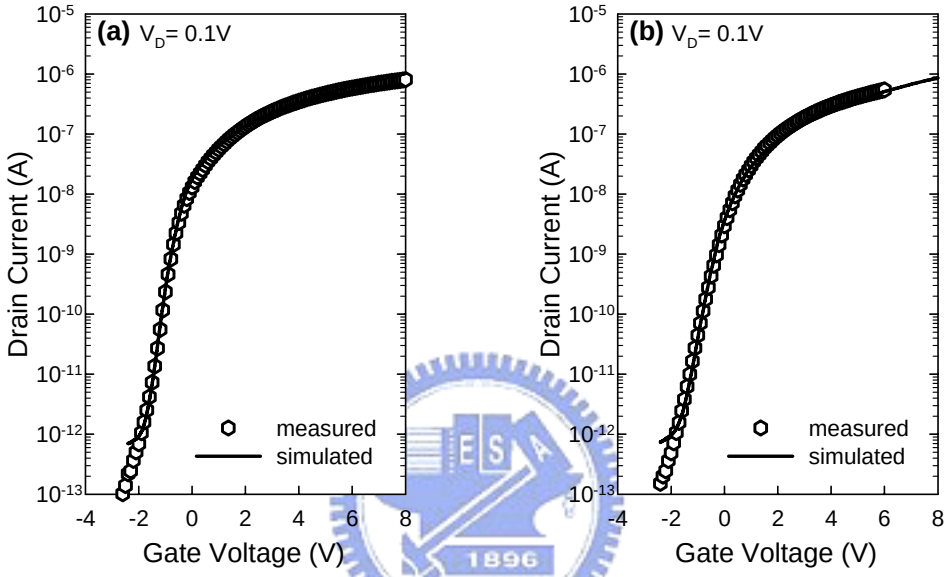


Fig. 6-10 Simulated subthreshold characteristics of D-MT (a) before and (b) after hot-carrier stressing under V_G/V_D = 6.5V/13V for 1000 sec.

6.4.2 Temporal evolution of DOS during hot-carrier stressing

Temporal evolution of hot-carrier degradation at specific locations in the channel can also be addressed. Figure 6-11 demonstrates the evolution of subthreshold characteristics of D-MT during the hot-carrier stress of V_G=6.5 volt and V_D=13 volt. The evolution of subthreshold characteristics in both logarithmic and linear scales are in agreement with the simulated results reported by Dimitriadis *et al.* [6.23], which suggest that this type of evolution is contributed by the increase of deep states.

Using the aforementioned technique, the temporal evolution of DOS distribution of the

degraded location, i.e., D-MT, during the hot-carrier stressing can also be observed. Increase in density-of-states distributions of D-MT during hot-carrier stressing are demonstrated in Fig. 6-12. It appears that during the hot-carrier stressing, DOS near the drain side continuously increases, especially for the states located at 0.2 to 0.4eV above the Fermi level.

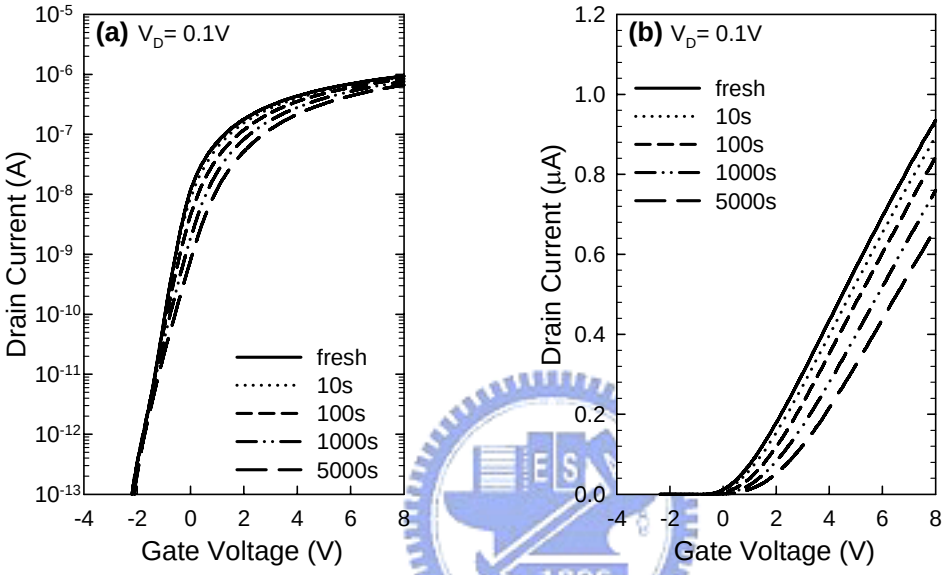


Fig. 6-11 Evolution of subthreshold characteristics of D-MT in (a) logarithmic and (b) linear scales during hot-carrier stressing under V_G/V_D=6.5V/13V.

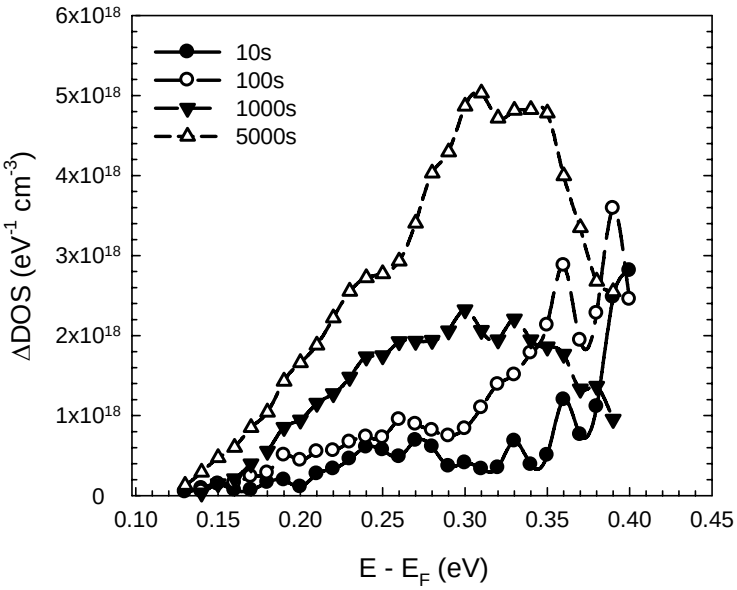


Fig. 6-12 Increase in density-of-states distributions of D-MT during hot-carrier stressing.

6.4.3 Recreating stressed IV characteristics using MTs

The density-of-states distribution extracted from monitor-transistors can be employed to simulate the evolution of subthreshold characteristics of test-transistors. In other words, the resultant subthreshold characteristics of TTs after the hot-carrier stressing can be exactly simulated by the data collected by MTs.

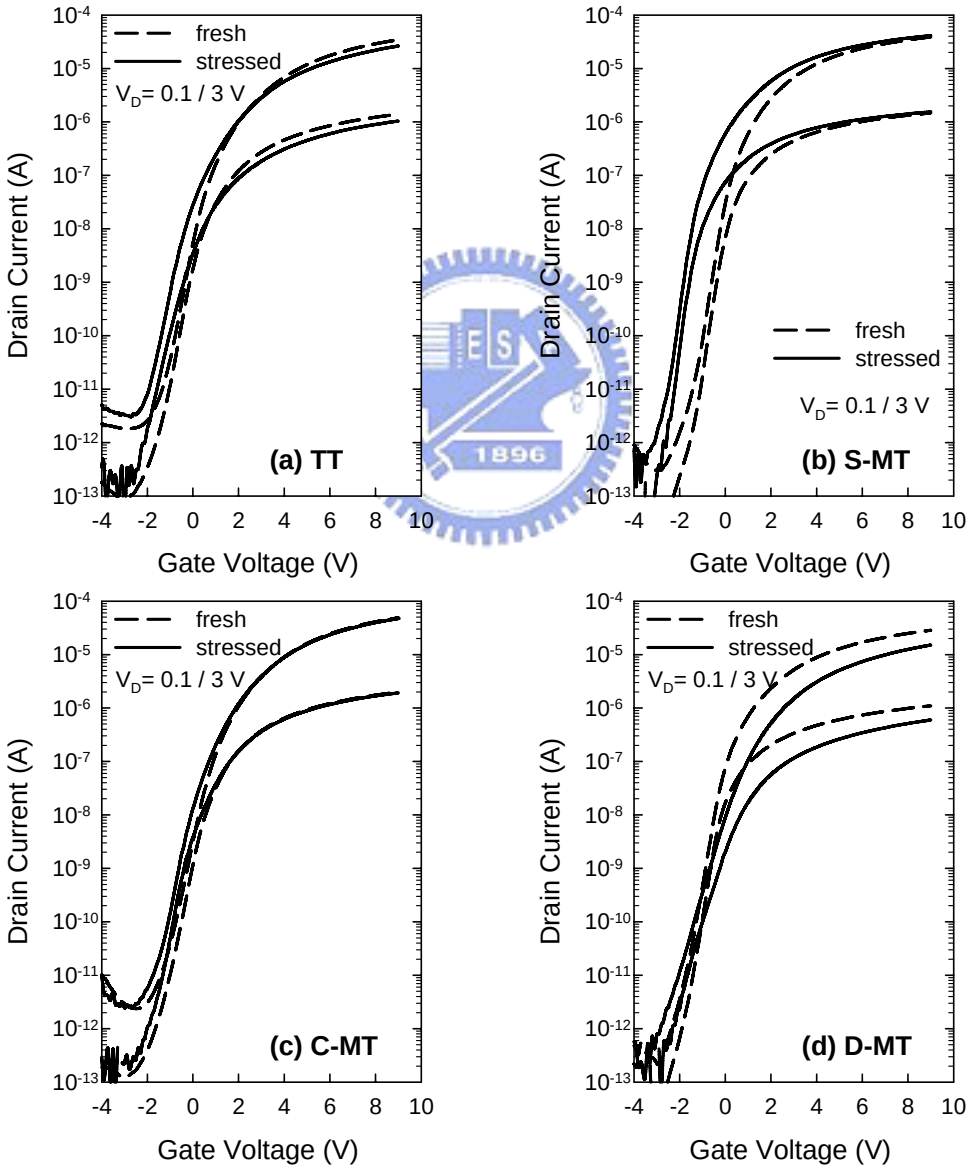


Fig. 6-13 Subthreshold characteristics of (a) TT, (b) S-MT, (c) C-MT, and (d) D-MT transistors in the test structure before and after the hot-carrier stressing at V_G/V_D of 10 V/20 V for 1000 sec.

For example, a tester was stressed under V_G / V_D = 10V / 20V for 1000 seconds. The subthreshold characteristics of all TT and MTs before and after the stressing were carefully measured. As shown in Fig. 6-13, the degradation in all transistors can be easily observed. The degradation of the test-transistor can be expressed as the combination of parallel shift in S-MT and degradations of subthreshold swing and on-current in D-MT. The mechanism of each phenomenon has been introduced and discussed before.

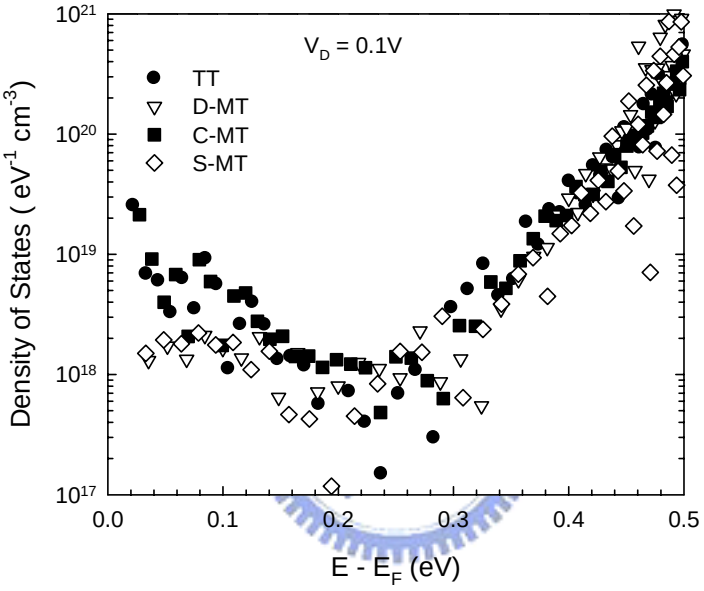
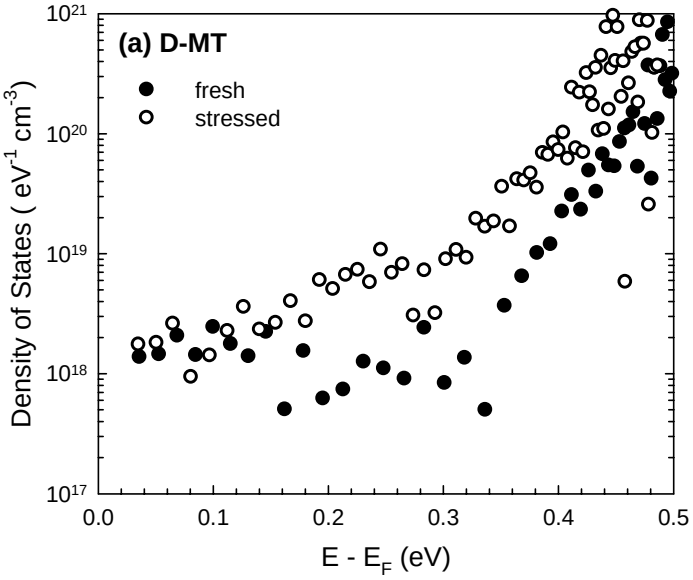


Fig. 6-14 Density-of-states distributions of the TT and three MTs before HC stressing.



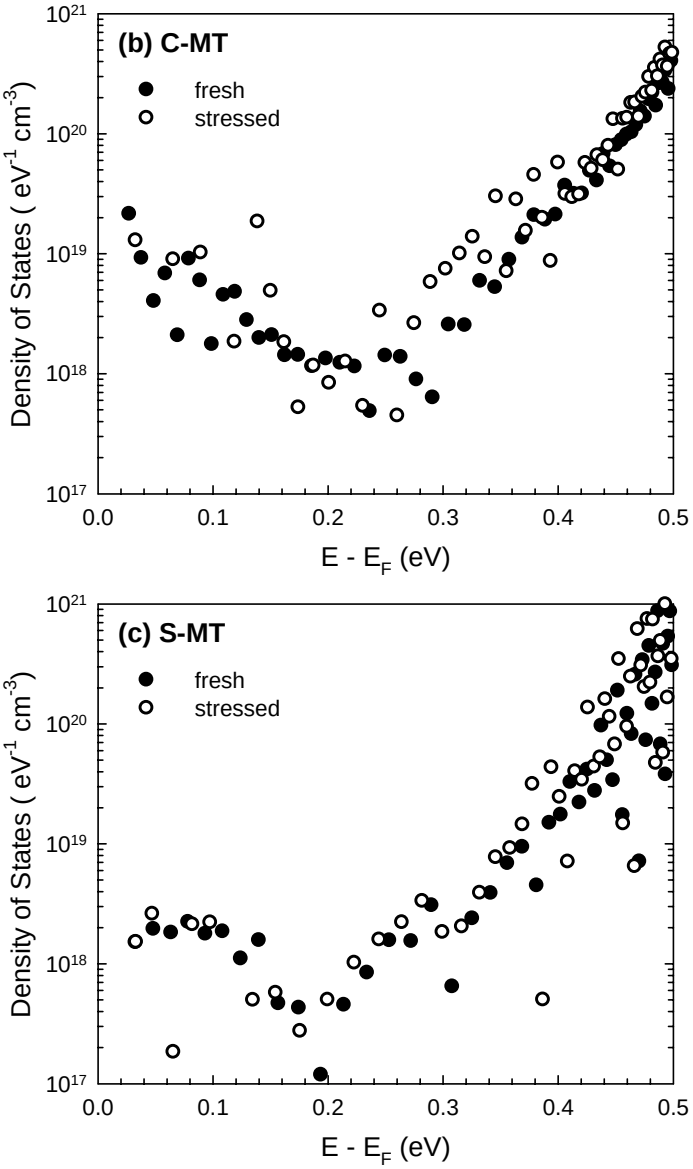


Fig. 6-15 Density-of-states distributions of (a) D-MT, (b) C-MT, and (c) S-MT before and after hot-carrier stressing at V_G/V_D of 10 V/20 V for 1000 sec.

The density-of-states distributions of all MTs were then extracted using the aforementioned technique. The resultant distributions of TT and three MTs before the stressing are shown in Fig. 6-14. It can be seen that all distributions are similar, indicating that the DOS are uniformly distributed along the channel. The DOS distributions for each MTs before and after the stressing are shown in Figs. 6-15(a)-(c). The increase of DOS in Fig. 6-15(a) indicates that many defects were generated near drain side during the stressing. In contrast, DOS distribution in Fig. 6-15(c) remains unchanged, because the creation of

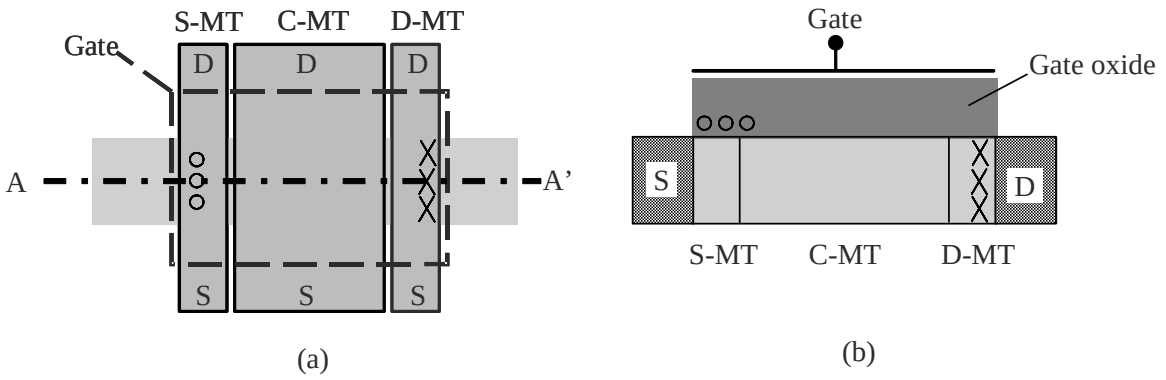


Fig. 6-16 Schematics of (a) top- and (b) cross-sectional view of the tester with indication of the induced damaged.

positive charge located in the oxide (as discussed in Section 4.6) affects the flat-band voltage only. As a result, the degradation along the channel of TT can be expressed be piecing together all MTs after the stressing, as shown in Fig. 6-16.

The channel of the TT was then split into three parts, as shown in Fig. 6-16(b). The DOS distribution of each part was set using the data collected from the corresponding MT. Simulated subthreshold characteristics of the TT before and after the hot-carrier stressing are

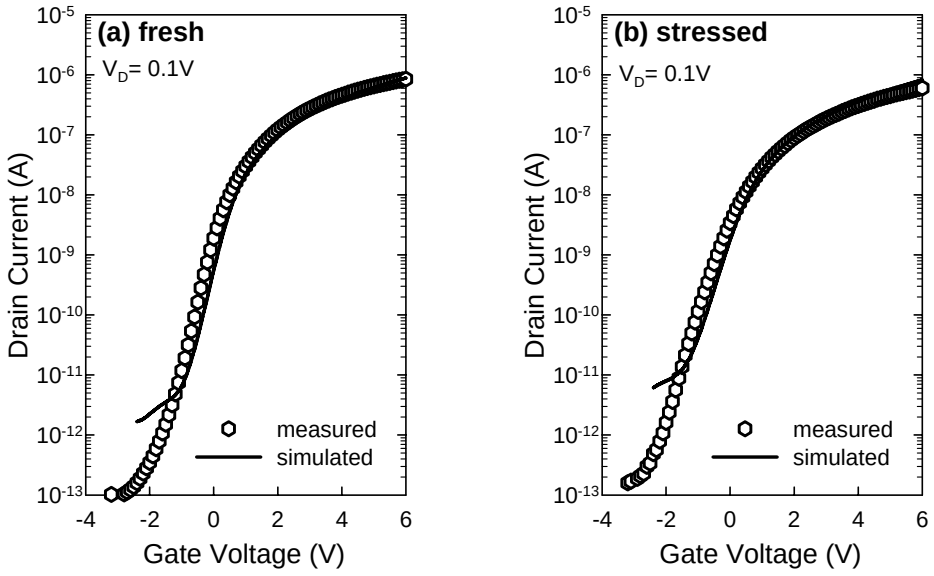


Fig. 6-17 Simulated subthreshold characteristics using data collected from MTs.

shown in Fig. 6-17(a) and Fig. 6-17(b), respectively. The simulated curves again fit well for both samples.

6.5 Summary

In this chapter, a high-sensitivity TFT structure capable of resolving hot-carrier degradation was employed. The non-uniform degradation could be clearly detected and characterized under moderate stress conditions. The density-of-states (DOS) distributions in specific locations were extracted using field-effect conductance (FEC) method. The DOS distributions revealed more useful and meaningful information in addition to traditional I-V characteristics. An increase of DOS was observed on certain position within the band gap, corresponding to deep states. The extracted DOS for both unstressed and stressed films were used to conduct simulations for subthreshold characteristics of the TFTs. The simulated I-V characteristics fitted well with the measurements. Temporal evolution during the hot-carrier stressing was also characterized, and the monotonic increase in DOS was observed. Finally we successfully simulated the subthreshold characteristics of the TTs before and after hot-carrier stressing using the DOS distributions extracted from all MTs.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Chapter 7

Conclusions and Future Prospects

7.1 Conclusions

In this dissertation, we have demonstrated and studied two types of novel thin film transistors. First, performances of novel TFTs configured with poly-Si NW channels was investigated in Chapter 2, accompanying with the effect of several process parameters on the shape of the nanowire. The proposed fabrication flow is simple and does not involve costly lithography tools. Pictures taken by cross-sectional TEM reveal that the width of fabricated nanowire exceeds 21 nm. Such nanowire structure has been shown to be excellent in terms of on-current per unit width and the controllability over short-channel effects. Owing to the fine nano-scale of NW width, hydrogenation would be very efficient for further performance improvement.

The mechanism of off-state leakage in the new NWTFT is proposed and discussed in Chapter 3. A gate-induced drain leakage (GIDL), which is generated in the overlapped region between gate and drain, is identified as the major culprit for the anomalous leakage. This leakage current is originated from the lightly-doped region at the gate/drain interface, which induces an additional current path. This off-state leakage is shown to be affected by several major factors: electric field between gate and drain, doping distribution at the gate-to-drain overlap region, and trap density in poly-Si material. All of them affect how much band-bending occurs near the oxide/silicon interface.

To address this issue, several modifications were proposed and demonstrated, including

additional ammonia plasma treatment, adoption of rapid-thermal annealing (RTA), insertion of a nitride layer over the overlapped region (HM), and employment of $Si_{1-X}Ge_X$ channel (SG). Experimental results show that the leakage current in control and RTA samples are still dependent on gate width (i.e., the overlapped region). In HM device, the additional leakage path is eliminated because of the relaxation of GIDL effect owing to the reduced gate-induced electric field. In SG device, the high DOS in $Si_{1-X}Ge_X$ material not only significant increases the resistance of the aforementioned leakage path, but also prohabits the band-bending needed for the GIDL. Both reasons prohibit the current path. In the last two cases, leakage mainly flows through the traditional path described in Fig. 3-19, therefore exhibiting only a weak dependence on GW.

In Chapter 4, a new test structure suitable for monitoring the spatial hot-carrier degradation in poly-Si TFTs was proposed and demonstrated. The fabrication of the novel test structure is simple and compatible with standard ULSI processing without extra masking. Several advantages of the test structure are demonstrated in this work, including (1) The capability of resolving the damage characteristics in different parts of channel; (2) The greatly enhanced sensitivity in detecting the localized damage; (3) Directly resolving the evolution of degradation in specific regions; (4) Identification of dominant damage mechanism. Specifically, we also found that at least two mechanisms are responsible for the negative threshold voltage shift detected by the monitor transistors.

Devices which received different NH_3-plasma treatment are subsequently characterized to analyze the effect of treatment time on both unstressed characteristics and the resistance against the hot-carrier stressing. Although samples depict performance enhancement after longer treatment, their resistance against hot-carrier stressing does not further improve.

The HCTFT was then employed in Chapter 5 for the analysis of the hot-carrier

degradation under AC operations. The effect of several factors were investigated and discussed, including frequency, rising time, and falling time. The phenomena of hot-carrier degradation can be spatially resolved using the proposed novel tester. By applying such tester to AC hot-carrier stressing, the relationship between different stages of input signal and resultant damage location can be established. The tester also shows a high sensitivity in detecting even mild AC degradation. The experiment provides unambiguous evidence that the damage occurs during transient stages, with the aid of the novel test structure. At the end of this chapter, we demonstrated the capability of the tester in spatially and temporally resolving several degradations simultaneously occur in different portions of the channel. Two different types of degradation were simultaneously identified with the help of monitor transistors.

In Chapter 6, the density-of-states distributions (DOS) in specific locations were extracted using field-effect conductance (FEC) method. The DOS distributions revealed more useful and meaningful information in addition to traditional I-V characteristics. An increase of the DOS was observed on certain position within the band gap, corresponding to deep states. The extracted DOS distributions for both unstressed and stressed film were used to conduct a simulation for subthreshold characteristics of the TFTs. The simulated I-V characteristics fitted well with the measurements. Temporal evolution during hot-carrier stressing was also characterized, and a monotonic increase in DOS was observed. The simulation of TTs before and after hot-carrier stressing was also demonstrated using the DOS distributions extracted from all MTs. The combination of the proposed novel test structure and density-of-states extraction technique provides a powerful tool for resolving the non-uniform DOS distribution of TFTs after HC stressing, which is impossible using traditional testers.

7.2 Future Prospects

Although many aspects and topics have been covered in this study, there are still several

interesting prospects for the proposed structures. Some of them are related to the improvement in device performance and optimization of the process condition, while others are their potential applications.

7.2.1 Mobility enhancement in nanowire TFTs

In this dissertation, the channel material of NWTFT was prepared by solid-phase crystallization (SPC). As has been demonstrated in this work, much higher on-current per unit width as well as steeper subthreshold swing can be achieved using the NW channels. Nevertheless, one potential concern associated with the fabricated devices of SPC

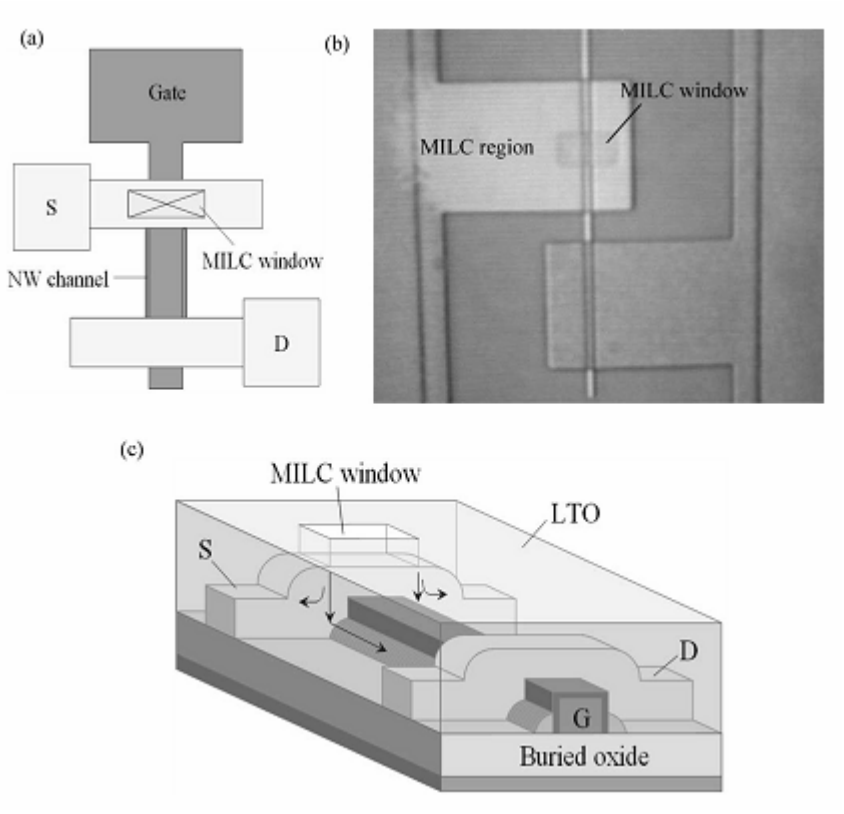

Fig. 7-1 (a) Top view of the layout, (b) the optical microscopy image and (c) the schematics of the poly-Si NWTFT enhanced by MILC.

poly-Si channel is the magnitude of the drive current since the carrier mobility is seriously degraded by the granular structure. Moreover, the nanoscale channel width could pose a

further limitation. The constraints could be relieved by increasing the number of channel in a device with comb-type gate structure, and/or by improving the performance with mobility-enhancement techniques, such as excimer laser crystallization [7.1] or metal-induced lateral crystallization (MILC) [7.2]. The latter approach has been adopted in one of our studies [7.3] which were carried out recently where MILC technique was applied to improve carrier mobility and on-current. The schematics of the NWTFT enhance by MILC are shown in Fig. 7-1.

7.2.2 Applications for the proposed nanowire TFTs

Owing to the inherent side-gated nature of the proposed NWTFTs, channels can be exposed after the formation of contact window. With this unique feature, detectors and bio-sensors can be easily fabricated by integrating the corresponding receptors to the channel. Figure 7-2 illustrates the schematics of the proposed bio-sensor realized by the NWTFTs.

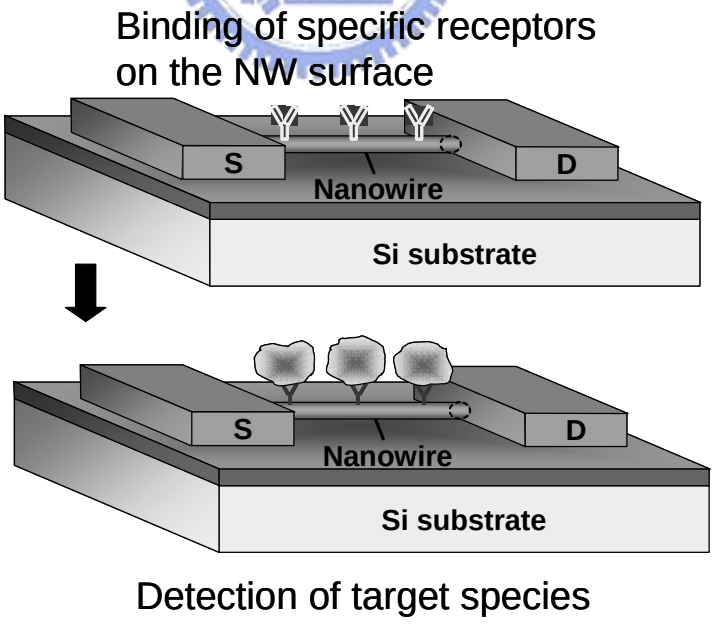

Fig. 7-2 Schematics of the proposed bio-sensor realized by the NWTFTs.

7.2.3 Resolution enhancement in HCTFT

By increasing the number of monitor transistors, it will be possible to increase the spatial resolution along the channel in detecting the hot-carrier induced degradation. In this way, it will be possible to detect experimentally the uniformity of degradation near the drain region, instead of relying simply on the numerical analysis of specific models for predicting the post-stress performance of the device [7.4][7.5]. Nevertheless, this methodology is limited when the device dimensions become small, since the current level of the monitor current decreases. Further work is needed to verify the limitation.

7.2.4 Hot-carrier degradation in p-channel TFTs

It has been shown that hot-carrier degradation in p-channel TFTs is different from that in n-channel TFTs [7.6]-[7.9]. In this study, only hot-carrier degradations in n-channel TFTs were investigated. Therefore, it is interesting to fabricate and study the effect in p-channel TFTs.

7.2.5 More bias conditions in AC stressing modes

TFTs may be operated in many different bias conditions. In this dissertation, we only investigated the well-known condition of dynamic gate pulse and constant drain bias. There are still more bias conditions such as pulse gate plus pulse drain, combined with the phase shift between two pulses. In realistic LCD driving, other driving method like multi-step voltage profile [7.10] may reveal different degradation model and failure sites which do not exist in conventional driving methods. The use of HCTFT on these stressing modes is still under investigation.

The reliability issues for the TFTs used in the peripheral circuits are more complicated.

Although hot-carrier reliability issue has been investigated and discussed for some basic building blocks such as inverters [7.11], shift registers [7.12], and ring oscillators [7.13], the information is still limited. By integrating HCTFTs into these circuits, the whole picture could be more clear when analyzing hot-carrier degradations in real circuit operations.


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Chapter 1

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論文題目：複晶矽薄膜電晶體中漏電流及可靠度課題之研究

A Study of Leakage Current and Reliability Issues in Poly-Si Thin-Film Transistors


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Publication List

A. International Journal:

1. H. C. Lin, **M. H. Lee**, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, vol. 53, pp. 2471-2477, Oct. 2006.

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E. Patent:

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