Chapter 1

Introduction

1-1. LTPS TFT

In recent years, with the flat-panel display technology development, flat- panel displays have replaced the traditional cathode ray tube (CRT) application for many aspects. Liquid crystal display (LCD) is one of the popular displays. Especially, thin film transistor liquid crystal display (TFT-LCD) is the most common display at present. According to the manufacture technique of thin film transistor (TFT), the TFT-LCD was categorized into amorphous-silicon (a-Si) TFT and low-temperature poly-silicon (LTPS) TFT and high- temperature poly-silicon (HTPS) TFT.

Among these TFTs, LTPS has been widely investigated as a material for mobile applications such as digital cameras and note book computers. In polysilicon film, the carrier mobility larger than 10 cm^2/Vs can be easily achieved, that is about 100 times larger than that of the conventional amorphous-silicon TFTs and fast enough to make peripheral driving circuit including n- and p-channel devices. This enables the monotheistic fabrication of peripheral circuit and TFT array on the same glass substrate, bringing the era of system-on-glass (SOG) technology [1]. They also have been applied into some memory devices such as dynamic random access memories

(DRAMs), static random access memories (SRAMs), electrical programming read only memories (EPROMs), electrical erasable programming read only memories (RRPROMs), linear image sensors, thermal printer heads, photo-detector amplifier, scanner, neutral networks. In the future, the application fields of LTPS TFTs will not be limited to displays but will be expanded to other electronic devices, such as LSIs, printers and sensors.

1-2. Variation

The LTPS TFTs suffer from bad uniformity. In this thesis, the consequences of the device variation in the reliability behaviors are systematically studied. The poly-Si material is a heterogeneous material made of very small crystals of silicon atoms in contact with each other constituting a solid phase material. These small crystals are called crystallites or grains. The presence of these crystallites that have any type of orientation means a break in the crystal from one crystallite to the other. Because the material remains solid, the atoms at the border of a crystallite are also linked to the neighbor crystallite ones. However, these atom bonds are disoriented in comparison with a perfect lattice of silicon. This border is called a grain boundary. Owing to the existence of grain boundary, the variation of poly-Si TFT is intrinsic.

Currently, the formation of the crystallites in polysilicon is achieved by solid

phase crystallization (SPC), excimer laser crystallization (ELA), or metal-induced lateral crystallization (MILC). None of the methods can control the growth of grain to be identical. Due to the variety of the grain boundary, each TFT have different trap states distribution in the poly-Si film.

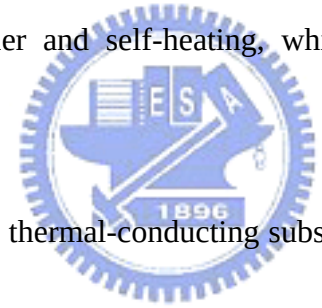
Thus, the TFT characteristics can be distinguished even fabricated with the same process and LTPS TFTs always have different characteristic. The fig. 1-1 shows the variation of the transfer characteristics of I_d-V_g curve and the fig. 1-2 shows the variation of the transfer characteristics of I_d-V_d curve. The disadvantage of the variation for LTPS TFTs is must be investigated.

For convenience these two types of variation will be called macroscopic and microscopic. The behaviors of the macroscopic and microscopic variation are the common and random variation, respectively. On the other hand, from the varying phenomena we can understand what variation type was occurred in the devices. The factors which caused the macroscopic variation in the devices include gate insulator thickness, ion implantation dose, channel length, LDD length…etc. The factors which caused the microscopic variation in the devices include defect sites, defect density, activation efficiency, grain boundary…etc. Fig. 1-3 shows the different TFTs with various amounts of grain boundaries existing in the channel.

1-3. Reliability

In order to realize the new applications for LTPS TFTs, we have to improve the performance such as enhancing mobility, decreasing the threshold voltage of TFTs, and shrinking the TFT size. However, the poly-Si TFT reliability improvements are as critical for the insurance of product lifetime.

There are several kinds of degradation phenomena in poly-Si TFTs have already been reported [2-11]. The sources of degradation are, for example, hot carriers, self-heating, water, contamination, and electrostatic discharge. The two main sources of degradation are hot carrier and self-heating, which are described in detail as follows.



Glass substrate is a poor thermal-conducting substrate and heat generated during the device operation is barely released. As a result, the device temperature can rise to a level that causes bonds to break. Such a phenomenon is called “self-heating” [2-8].The degradation rate caused by self-heating depends on the operating power and the capability of heat dissipation of the device. In general, wide-channel TFTs or small-scale TFTs suffer from serious self-heating.

Hot carrier effects [9-10] that originate from the high electric field near the drain junction have been widely investigated in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. Thus, such high energy carriers

can easily break the weak bonds existing in poly-Si, creating many defect states and oxide charges. Serious degradation can be generated in the hot carrier operation mode, and the degree of degradation depends on the strength of the electric field. Introducing electric-field-relief TFT structures, such as lightly doped drain (LDD), offset drain, and gate-drain overlapped LDD (GO-LDD), can reduce the hot carrier degradation.

1-4. Thesis Outline

Chapter 1. Introduction

- **1-1 LTPS TFT**
- **1-2 Variation**
- **1-3 Reliability**

Chapter 2. Stress Mapping for Reliability

- **2-1 Experiment**
- **2-2 Results and Discussion**
- **2-3. Discussion**
- **2-4. Conclusion**

Chapter 3. Diverse Degradation Behaviors

- **3-1 Experiment**
- **3-2 Results and Discussion**
- **3-3 Conclusion**

Chapter 4. Initial Characteristic Dependence

- **4-1 Experiment**
- **4-2 Results and Discussion**

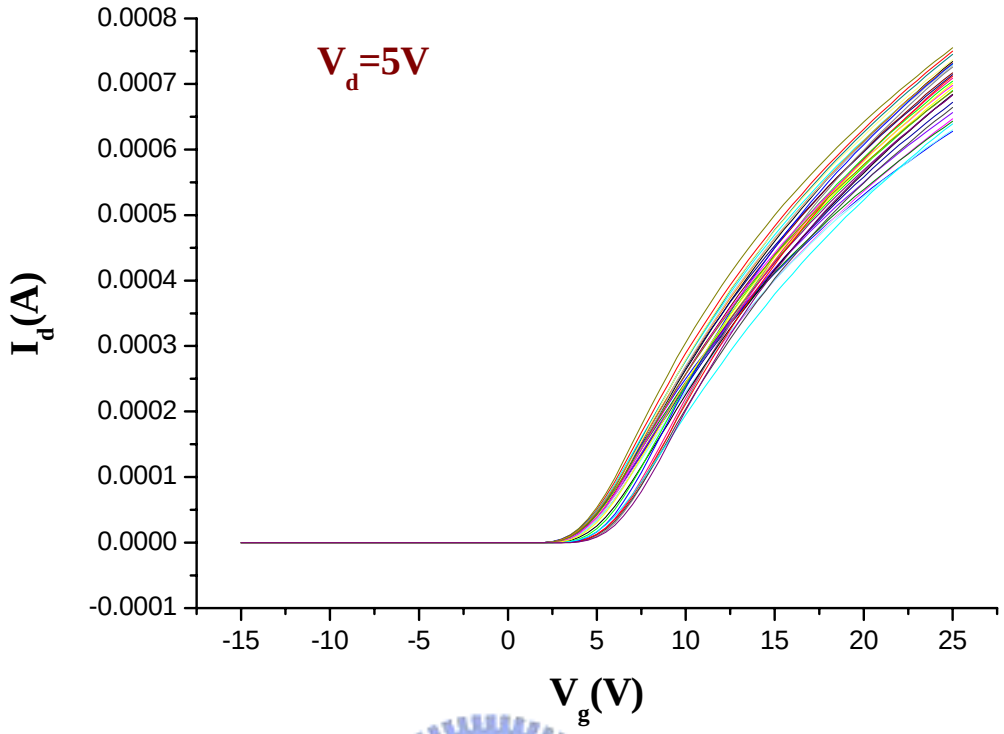


Fig. 1-1 The variation of the transfer characteristics of I_d-V_g curve for LTPS TFTs.

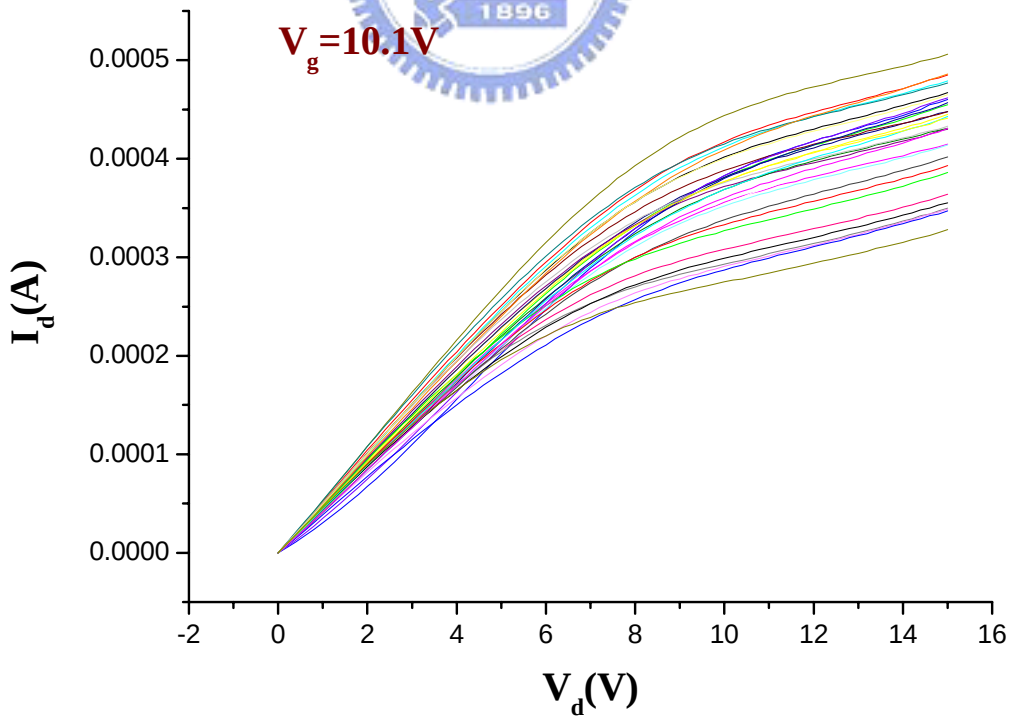


Fig. 1-2 The variation of the transfer characteristics of I_d-V_d curve for LTPS TFTs.

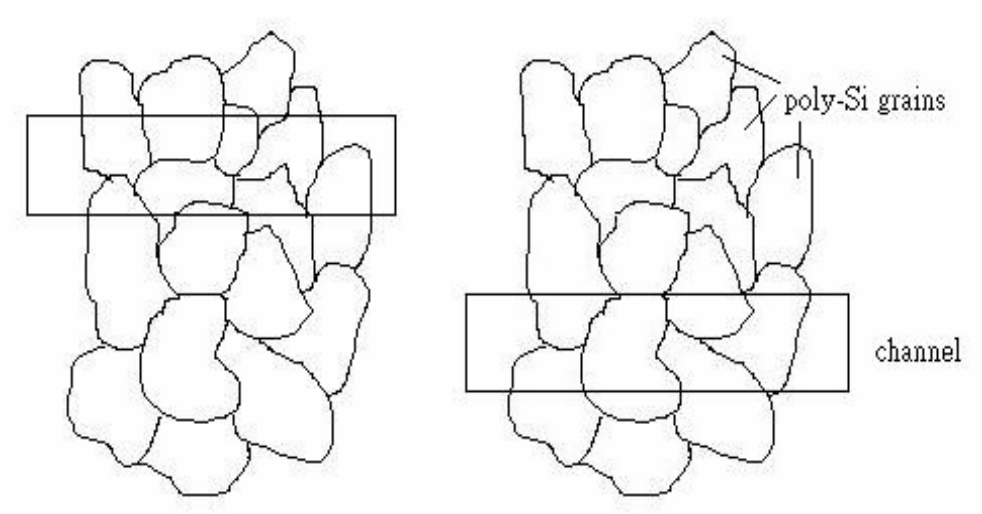


Fig. 1-3 The diagram of different TFTs with various amount of grain boundaries existing in the channel.

Chapter 2

Stress Mapping for Reliability

2-1. Experiment

As mentioned in section 1-3, the reliability of TFTs is aimed to be studied. The stress mapping of the stress voltages including different gate voltage (V_g) and drain voltage (V_d) for the different stress times are established firstly.

2-1-1. Device Fabrication

The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were de-posited on glass substrates, then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition. Subsequently, a gate insulator was deposited. Next, the metal gate formation and source/drain doping were performed. A Lightly doped drain (LDD) structure was used on the devices. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. The fig. 2-1 shows the Schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

2-1-2. Method of Device Parameter Extraction

In this section, we will introduce the methods of parameter extraction used

throughout the whole thesis, including threshold voltage (V_t), sub-threshold swing (S.S), drain current on/off current ratio, field-effect and mobility（μ_{FE}）.

2-1-2-1. Determination of the Threshold Voltage

Many ways are used to determinate the threshold voltage (V_t) which is the most important parameter of semiconductor devices. In this thesis, the method to determinate the threshold voltage (V_t) is the constant drain current method. The gate voltage at a specific drain current I_N value is taken as the threshold voltage (V_t). This technique is adopted in most studies of TFTs. Specifically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified at 10nA for V_D=0.1V and 100nA for V_D=10V as most papers to extract the threshold voltage of TFTs. So V_t is extracted at 10nA of the I_d-V_g curve for V_d=0.1V and V_t^* is extracted at 100nA of the I_d-V_g curve for V_d=10V.

2-1-2-2. Determination of the Sub-threshold Swing

Sub-threshold swing S.S (V/dec) is a typical parameter to describe the gate control toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. The sub-threshold swing (S.S) should be dependent of drain voltage and gate voltage. However, in reality, the sub-threshold swing might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The sub-threshold swing is also related to gate voltage due to undesirable factors such as

serial resistance and interface state. We defined the sub-threshold swing (S.S) is the minimum value of $S.S = \left[\frac{\partial(\log I_{ds})}{\partial V_{gs}}\right]^{-1}$. S.S is extracted at the I_d-V_g curve for V_d=0.1V and S.S* is extracted at the I_d-V_g curve for V_d=10V.

2-1-2-3. Determination of the Field-effect Mobility

While the field-effect mobility (μ_{FE}) is derived from the drain conductance, the field-effect mobility (μ_{FE}) is determined from the transconductance (g_m). The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right] \quad \text{(2-a)}$$

where C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_T is the threshold voltage. If V_D is much smaller than V_G-V_T (i.e. V_D<<V_G-V_T) and V_G>V_T, the drain current can be approximated as

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}(V_G - V_T)V_D \quad \text{(2-b)}$$

When the field-effect mobility is determined, the trans-conductance (g_m) is usually taken to be

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{eff}}{L}V_D \quad \text{(2-c)}$$

When this expression is solved for the mobility, it is known as the field-effect mobility (μ_{FE}) and given by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \quad \text{(2-d)}$$

Then we extract the parameter of mobility is the maximum value of the field-effect mobility (μ_{FE}) when V_d=0.1V.

2-1-3. Degradation Behavior Brief

As mentioned in 1-3, there are several kinds of degradation phenomena in poly-Si TFTs have already been reported. The two main sources of degradation are hot carrier and self-heating. We can easily to distinguish these two sources from the device I_d-V_g curves. The Fig. 2-2 is the typical I_d-V_g curve of device which undergoes in hot-carrier effect and the Fig. 2-3 is the typical I_d-V_g curve of device which was occurred self-heating effect with the application stress condition of V_g=4V with V_d=20V for different stress time. Features of this degradation are as follows：

(1) A decrease of the on-current value.

(2) Neither a shift of transfer characteristics nor a degradation of the sub-threshold swing.

The Fig. 2-3 shows the transfer characteristics of the n-channel TFTs which undergoes in self-heating effect with the application stress condition of V_g=25V with V_d=15V for different stress time. Features of this degradation are as follows：

(1) The shift of transfer characteristics toward the position direction.

(2) A decrease of the on-current value.

(3) The degradation of the sub-threshold swing.

2-1-4. Grids of Stress Map

Fig. 2-4 shows the four regions of the stress mapping. The horizontal axis is the stress gate voltage ($V_{g,stress}$) and the vertical axis is the stress drain voltage ($V_{d,stress}$). The region I is defined as the varied range of $V_{g,stress}$ and $V_{d,stress}$ is 0V to 10V and 0V to 10V, respectively. The region II is defined as the varied range of $V_{g,stress}$ and $V_{d,stress}$ is 0V to 10V and 10V to 20V, respectively. The region III is defined as the varied range of $V_{g,stress}$ and $V_{d,stress}$ is 10V to 20V and 0V to 10V, respectively. The region IV is defined as the varied range of $V_{g,stress}$ and $V_{d,stress}$ is 10V to 20V and 10V to 20V, respectively. The stress condition of region I is $V_{g,stress}$ from 0V to 10V which steps is 5V and $V_{d,stress}$ from 0V to 10V which steps is 5V. The stress condition of region II is $V_{g,stress}$ from 0V to 10V which steps is 2V and the stress drain voltage (V_d) from 10V to 20V which steps is 2V. The stress condition of region III is $V_{g,stress}$ from 10V to 20V which steps is 2V and $V_{d,stress}$ from 0V to 10V which steps is 2V. The stress condition of region IV is $V_{g,stress}$ from 10V to 20V which steps is 2V and the stress drain voltage (V_d) from 10V to 20V which steps is 2V. Furthermore, the condition of stress time is 10s, 20s, 50s, 100s, 200s, 500s and 1000s.

2-2. Results and Discussion

2-2-1. Threshold Voltage (V_t, V_t^*) Shift and Negative V_t, V_t^* shift

Fig. 2-5 and fig. 2-6 shows the stress voltage dependence of the threshold voltage (V_t) shift in the positive and negative direction of the typical n-type TFTs when V_d=0.1V, respectively. Fig. 2-7 and fig. 2-8 shows the stress voltage dependence of the threshold voltage (V_t^*) shift in the positive and negative direction of the typical n-type TFTs when V_d=10V, respectively. The stress application times were 10s, 20s, 50s, 100s, 200s, 500s and 1000s. The threshold voltage (V_t & V_t^*) shift was calculated as follows.

V_t Shift (V)=$V_t^{\text{after stress}}$ (V) - $V_t^{\text{before stress}}$ (V)

V_t^* Shift(V)=$V_t^{*\text{after stress}}$ (V) – $V_t^{*\text{before stress}}$ (V)

So, the V_t and V_t^* shift is the positive of $V_t^{\text{after stress}}$ (V) - $V_t^{\text{before stress}}$ (V) and the negative V_t/V_t^* shift is the negative of $V_t^{\text{after stress}}$ (V) - $V_t^{\text{before stress}}$ (V). Finally, from fig. 2-5 to fig. 2-8 we can know the following points.

【1】These four figures shows the V_t and V_t^* shift have no dependence relationship with the stress gate voltage (V_g) and the stress drain voltage (V_d).

【2】The serious V_t and V_t^* shift phenomena occur in the region IV.

【3】The serious negative V_t shift phenomenon occurs near the boundary of the region III and the region IV and the negative V_t^* shift phenomenon occurs even wider

regions.

【4】For long time stress, the V_t and V_t^* shift phenomena occur in the region II and the region III.

【5】The V_t and V_t^* shift phenomena occur in the region II is serious than in the region III.

【6】The degradation phenomena are very diverse even with the above trends.

2-2-2. I_{on}, I_{on}^* Degradation Rate and I_{on}, I_{on}^* Increase Rate

Fig. 2-9 and fig. 2-10 show the dependence of stress voltage on the I_{on} degradation and increase rate in the typical n-type TFTs when V_d=0.1V, respectively. Fig. 2-11 and fig. 2-12 shows the dependence of stress voltage on the I_{on}^* degradation and increase rate in the typical n-type TFTs when V_d=10V, respectively. The gate and drain voltage were each varied from 0V to 20V and the stress time were 10s, 20s, 50s, 100s, 200s, 500s and 1000s. We defined the I_{on} as the corrent value of the I_d-V_g curve when V_g=15V with V_d=0.1V and the I_{on}^* as the current value of the I_d-V_g curve when V_g=15V and V_d=10V. The I_{on} and I_{on}^* degradation rate as well as I_{on} and I_{on}^* increase rate were calculated as follows.

I_{on} Degradation Rate= the negative of $\{I_{on}^{\text{after stress}}-I_{on}^{\text{before stress}}\}/I_{on}^{\text{before stress}}$

I_{on}^* Degradation Rate= the negative of $\{I_{on}^{*\text{ after stress}}-I_{on}^{*\text{ before stress}}\}/I_{on}^{*\text{ before stress}}$

I_{on} Increase Rate= the positive of $\{I_{on}^{\text{after stress}}-I_{on}^{\text{before stress}}\}/I_{on}^{\text{before stress}}$

I_{on}^{*} Increase Rate= the positive of $\{I_{on}^{*\ \text{after stress}}-I_{on}^{*\ \text{before stress}}\}/I_{on}^{*\ \text{before stress}}$

From fig. 2-9 to fig. 2-12 we can know the following points.

【1】The serious of I_{on} and I_{on}^{*} degradation phenomena occur in the region II and the region IV.

【2】For long time stress all region have the I_{on} and I_{on}^{*} degradation phenomena.

【3】The serious of I_{on} and I_{on}^{*} increase phenomena occur near the boundary of the region III and the region IV.

【4】The I_{on} and I_{on}^{*} degradation phenomena occur in the region II is serious than in the region III.

【5】The I_{on}^{*} increase rate is smaller than the I_{on} increase rate.

2-2-3. Mobility Degradation Rate and Mobility Increase Rate

Fig. 2-13 and fig. 2-14 shows the dependence of stress voltage on the mobility degradation and increase rate in the typical n-type TFTs when V_d=0.1V. The gate and drain voltage were each varied from 0V to 20V and the stress time were 10s, 20s, 50s, 100s, 200s, 500s and 1000s. We defined the mobility as the extracted maximum value of the I_d-V_g curve for V_d=0.1V. The mobility degradation rate and the mobility increase rate were calculated as follows.

Mobility Degradation Rate = the negative of $\{\mu^{\text{after stress}}-\mu^{\text{before stress}}\}/\mu^{\text{before stress}}$

Mobility Increase Rate = the positive of $\{\mu^{\text{after stress}}-\mu^{\text{before stress}}\}/\mu^{\text{before stress}}$

From fig. 2-13 to fig. 2-14 we can know the following points.

【1】The serious of the mobility degradation phenomenon occur in the region corresponding to negative V_t shift.

【2】For long time stress, all region have the mobility degradation phenomenon.

【3】The serious of the mobility increase phenomenon occurs in the boundary of the region III and the region IV.

【4】The mobility degradation phenomenon occurs in the region II is serious than in the region III.

2-2-4. Sub-threshold Swing (S.S) Variation and S.S* variation

Fig. 2-15 and fig. 2-16 shows the dependence of stress voltage on the Sub-threshold swing (S.S/S.S*) variation in the typical n-type TFTs when V_d=0.1V and V_d=10V, respectively. The gate and drain voltage were each varied from 0V to 20V and the stress time were 10s, 20s, 50s, 100s, 200s, 500s and 1000s. The Sub-threshold swing variation was calculated as follows.

Sub-threshold Swing (S.S) Variation (V/dec) = $S.S^{\text{after stress}}$ (V/dec) – $S.S^{\text{before stress}}$ (V/dec)

Sub-threshold Swing ($S.S^*$) Variation (V/dec) = $S.S^{*\ \text{after stress}}$ (V/dec) – $S.S^{*\ \text{before stress}}$ (V/dec)

From fig. 2-15 to fig. 2-16 we can know the serious of the sub-threshold swing

(S.S/S.S*) variation phenomena occur in the region IV.

2-3. Discussion

For the region I, owing to the low electric field and the low power dissipation, we can not obviously observe the phenomenon of device degradation for the short stress time. However, for the long stress time, the device degradation still appears. Comparing to the other regions, TFTs operating in this region are reliable.

For the region II, we can obviously observe the phenomena of the V_t shift, I_{on} degradation and mobility degradation. The hot carrier effect dominates in this region, which generates the hot carrier of the electrons and/or holes gaining energy in the lateral electric field. They can create interface-trapped charge or some defects in the channel. This leads to the V_t shift owing to fixed charge, mobility degradation due to more Coulomb scattering, and thus I_{on} degradation. However, the S.S has almost no degradation in this region, which indicates the device during the stress has little change in the deep states. The dangling bonds are either not increased or created and then passivated. Moreover, the infant degradation for the short stress time is important. When the stress time increases the degradation phenomena seem to be saturated. The initially generated defects can reduce the electric field and retard the further creation of new defects.

For the region III, we still observe the V_t shift, I_{on} degradation as well as mobility degradation. In contrast, the degree of the degradation is higher than the region I but lower than the region II. The S.S also has minor change in this region. The proposed explanation for the different degrees of the degradation phenomena is the lower lateral field and the lesser power than those in the region II. The lateral electric field and the power in the region I are even smaller, resulting in the less degradation.

For the region IV, the degradation phenomena are more complicated. For the upper region, we can obviously observe the serious V_t shift, I_{on} degradation, mobility degradation and S.S increase. According to these behaviors, we can speculate not only hot carrier effect but also self-heating effect occur in this region. Owing to the larger power, joule heat drives the hydrogen away, leaves more dangling bonds, increases the deep states, and thus causes the S.S degradation. In the most severe stress condition of V_g=20V and V_d=20V, all the tested devices burn out immediately. It reveals the limit of the operation range for the devices. In addition, we can see the continuous degradation in this region. In other words, the created defects can not slow down or stop the generation of more defects. This observation is consistent with the hypothetic degradation mechanism of the out-diffusion of hydrogen.

Near the boundary of the region III and the region IV, we notice a special region with V_t negative shift, I_{on} increase and mobility increase. In the previous paper [1]

also seen the special region. The fig. 2-19 shows the negative V_t shift in typical TFTs after stress applications. They assumed that the degradation phenomenon was induced by the combination of contamination and self-heating. In TFTs, temperature during operation becomes high. When TFTs are contaminated with mobile ions, the ions can drift easily under the high temperature. Therefore, V_t shift in the negative direction is induced by the accumulation of mobile ions at the MOS interface in the n-channel TFTs. There might be other reasons causing the degradation phenomenon. We suggest that it may come from the incomplete activation of the LDD regions. When the temperature rises, the phenomenon like “anneal” might take place in the LDD regions. So, the LDD regions will be reactivated.

2-4. Conclusion

We separate the stress map into several regions. Fig. 2-19 and fig. 2-20 are the total summary of the stress map for V_d=0.1V and V_d=10V, respectively. The table 2-1 summarizes of the degradation phenomena in our stress map. The hot carrier effect and the self-heating effect can explain all most region degradation in the stress map which is almost consistent with the previous reports as shown in fig. 2-17 and fig. 2-18[2-3]. The special region near the boundary of the region III and the region IV is found for the first time but the mechanisms in this region need more investigation.

Furthermore, there is no clear dependence of V_g and V_d observed for the degradation phenomena. In other words, it is different to predict the unstable behaviors simply according to the stress conditions. Therefore, to observe the effect of characteristic variation at different stress conditions in the next chapter, we repeat the stress experiments for some conditions with several nominally identical devices.

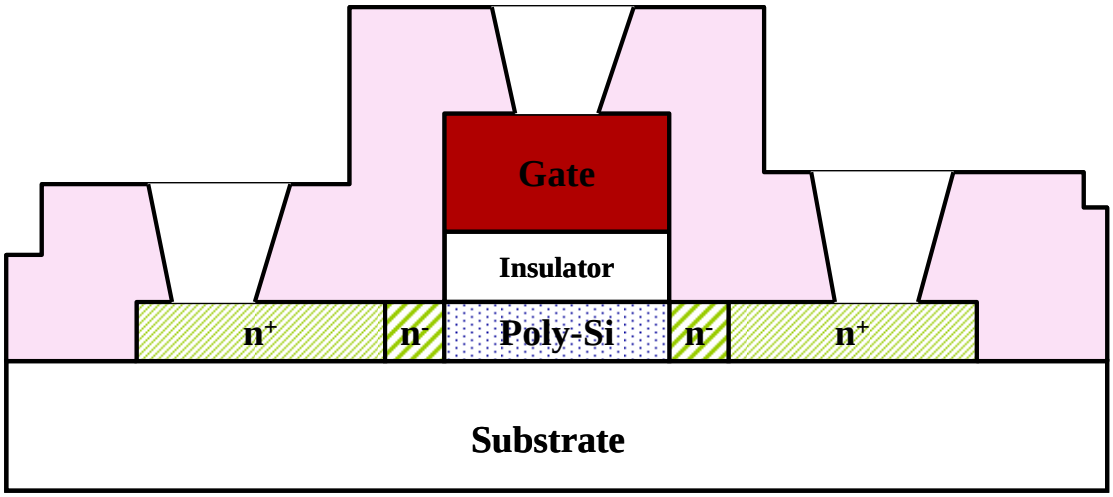


Fig. 2-1 Schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

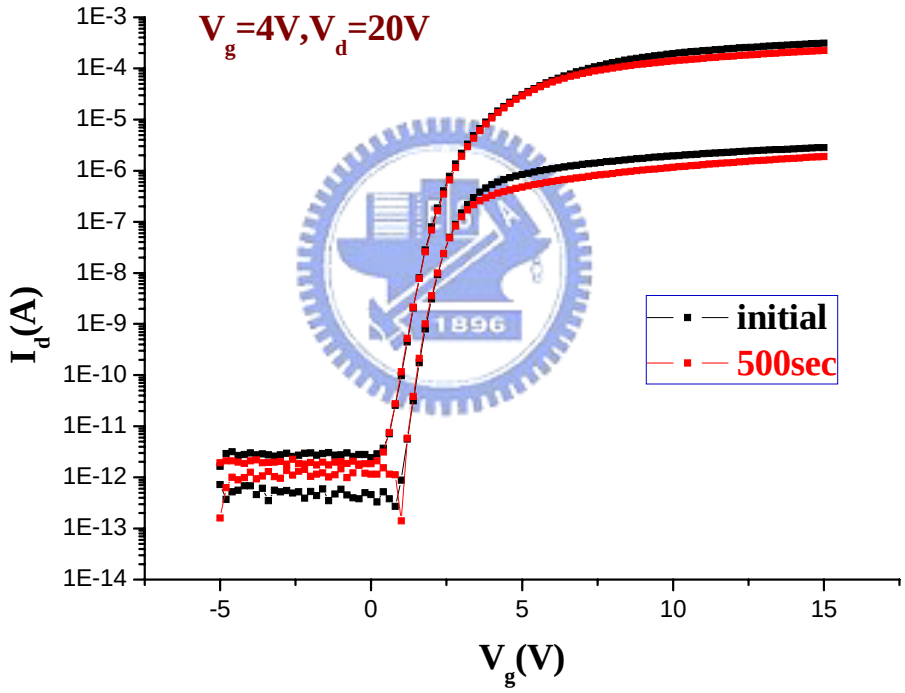


Fig. 2-2 Transfer characteristic of a typical TFT before and after the stress of V_g=4V and V_d=20V for 500sec stress time.

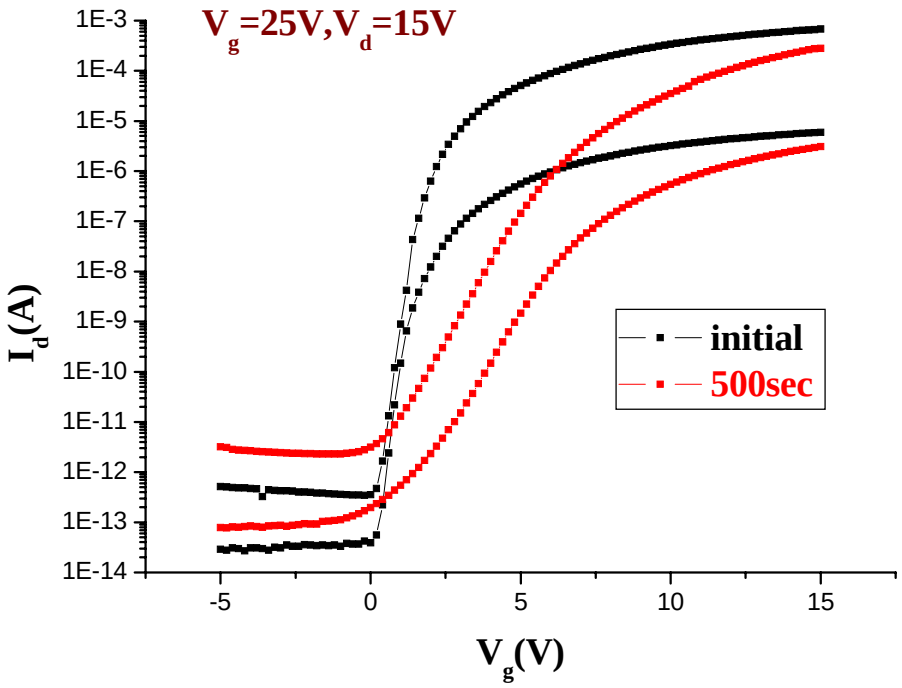


Fig. 2-3 Transfer characteristic of a typical n-type TFT before and after the stress of V_g=25V and V_d=15V for 500sec stress time.

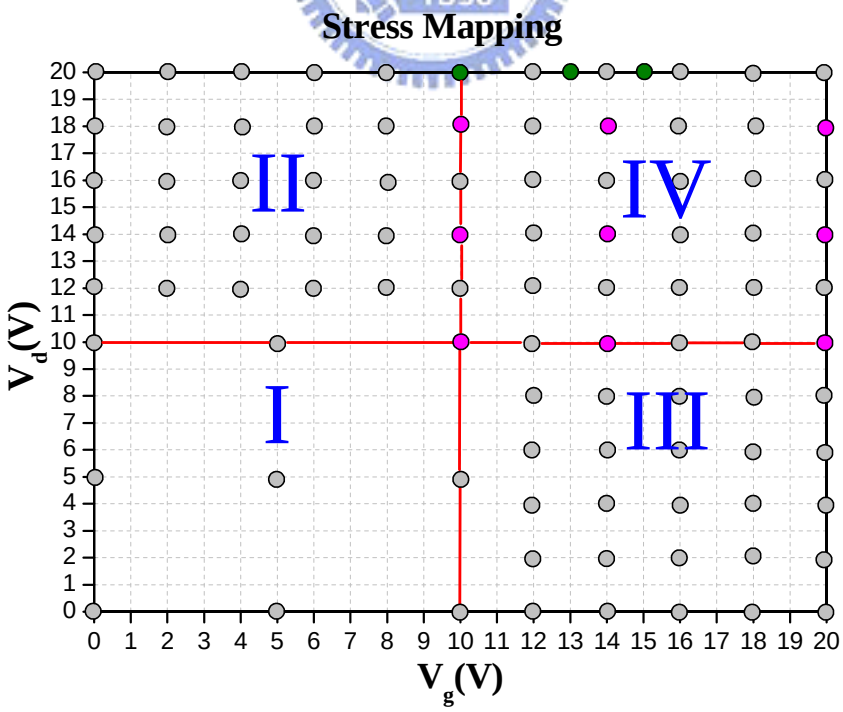


Fig. 2-4 Four regions of the stress mapping.

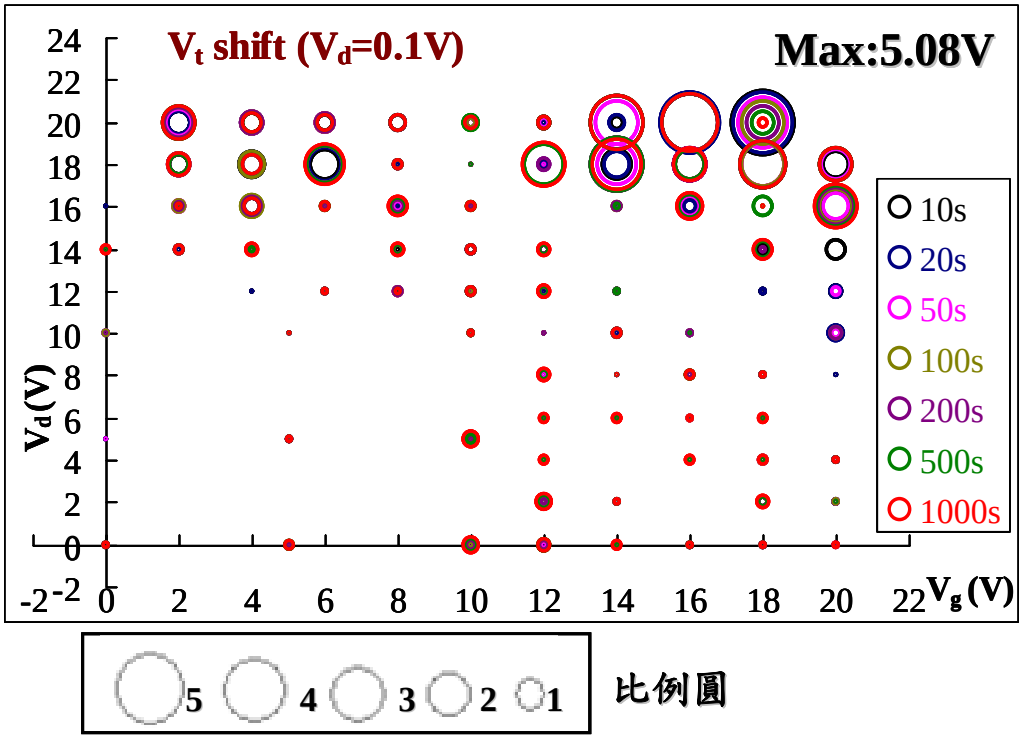


Fig. 2-5 Stress voltage dependence of the threshold voltage (V_t) shift in the ***positive*** direction (V_d=0.1V).

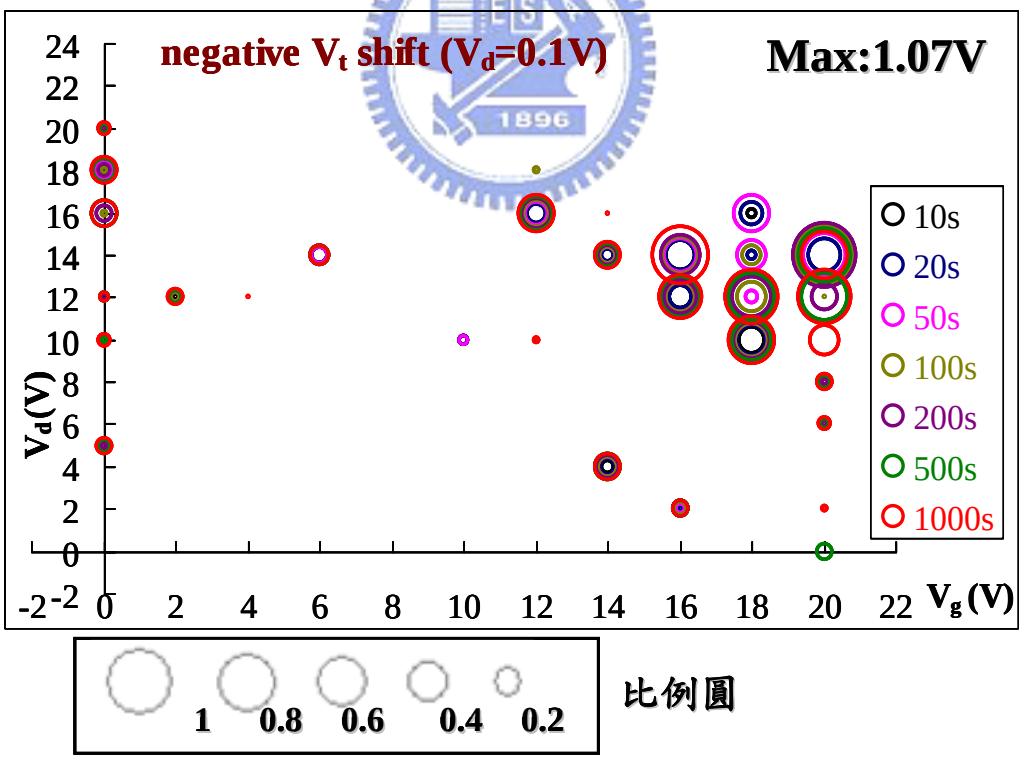


Fig. 2-6 Stress voltage dependence of the threshold voltage (V_t) shift in the ***negative*** direction (V_d=0.1V).

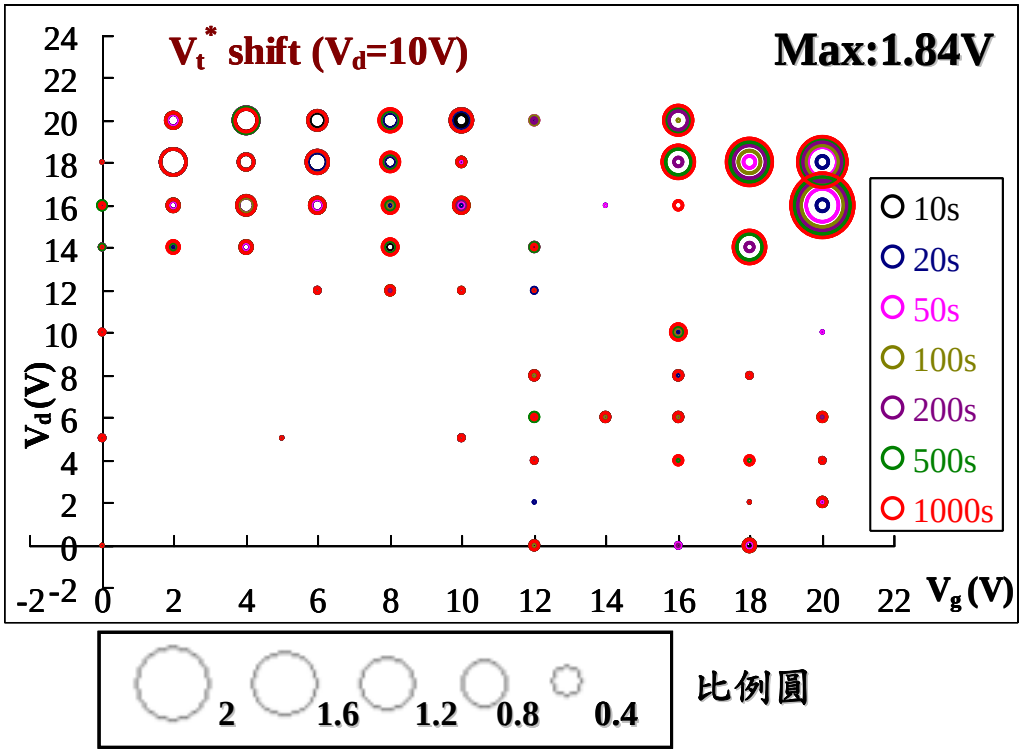


Fig. 2-7 Stress voltage dependence of the threshold voltage (V_t^*) shift in the ***positive*** direction (V_d=10V).

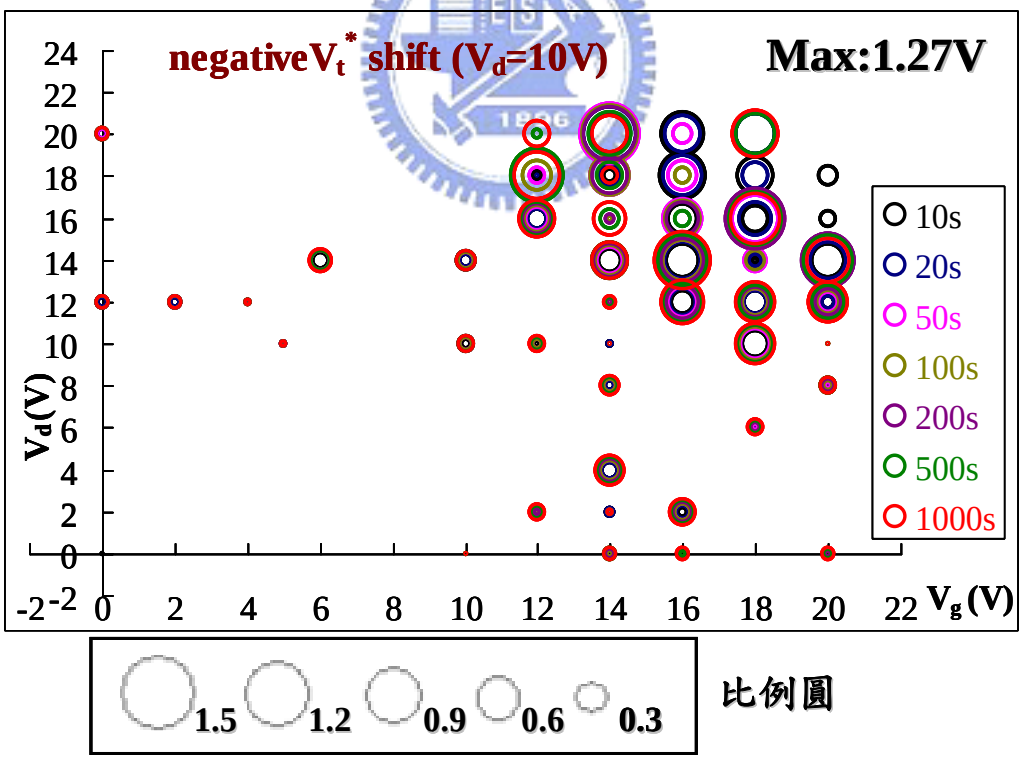


Fig. 2-8 Stress voltage dependence of the threshold voltage (V_t^*) shift in the ***negative*** direction (V_d=10V).

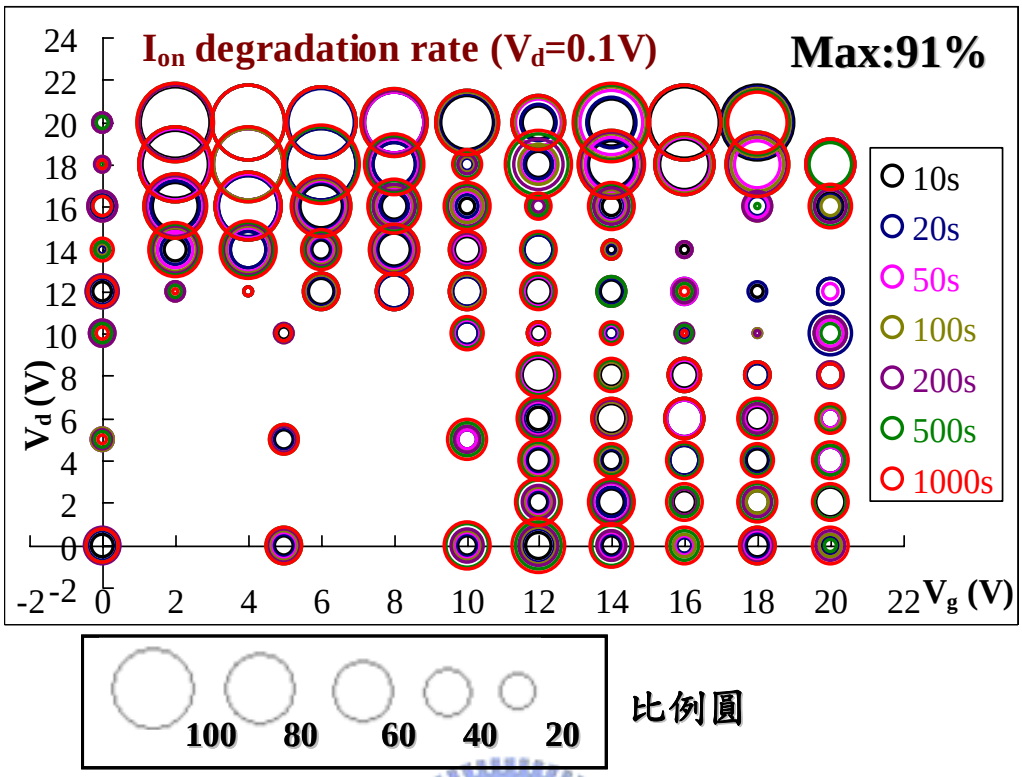


Fig. 2-9 Dependence of stress voltage on the I_{on} degradation in the typical n-type TFTs (V_d=0.1V).

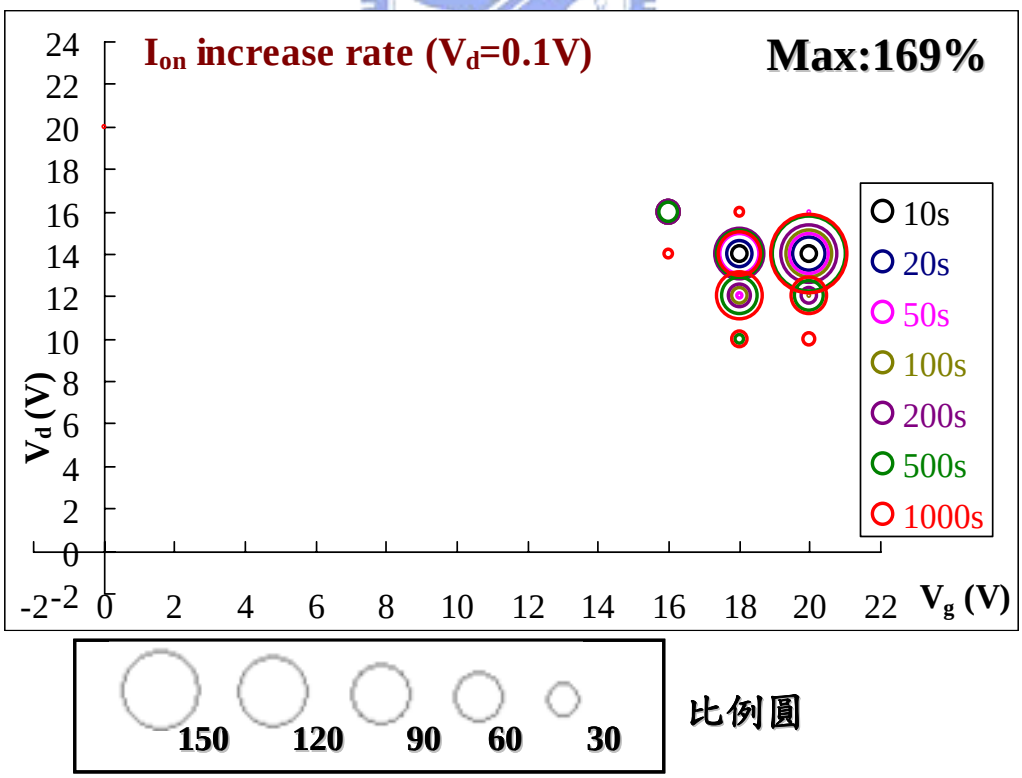


Fig. 2-10 Dependence of stress voltage on the I_{on} increase in the typical n-type TFTs (V_d=0.1V)

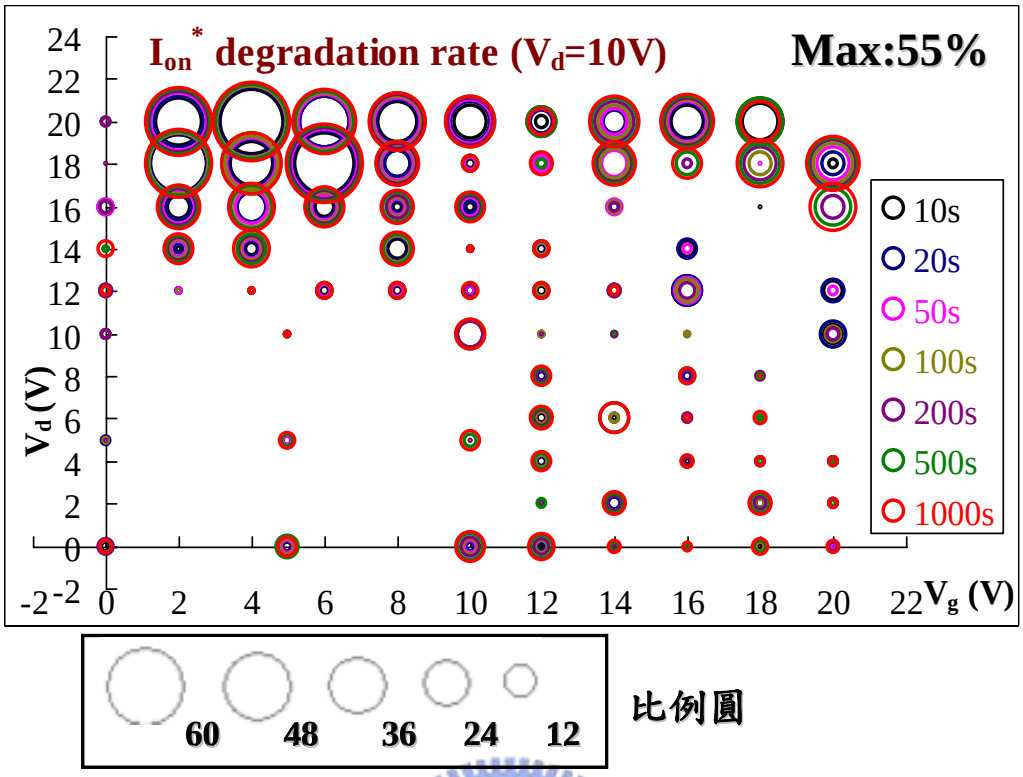


Fig. 2-11 Dependence of stress voltage on the I_{on}^* degradation in the typical n-type TFTs (V_d=10V).

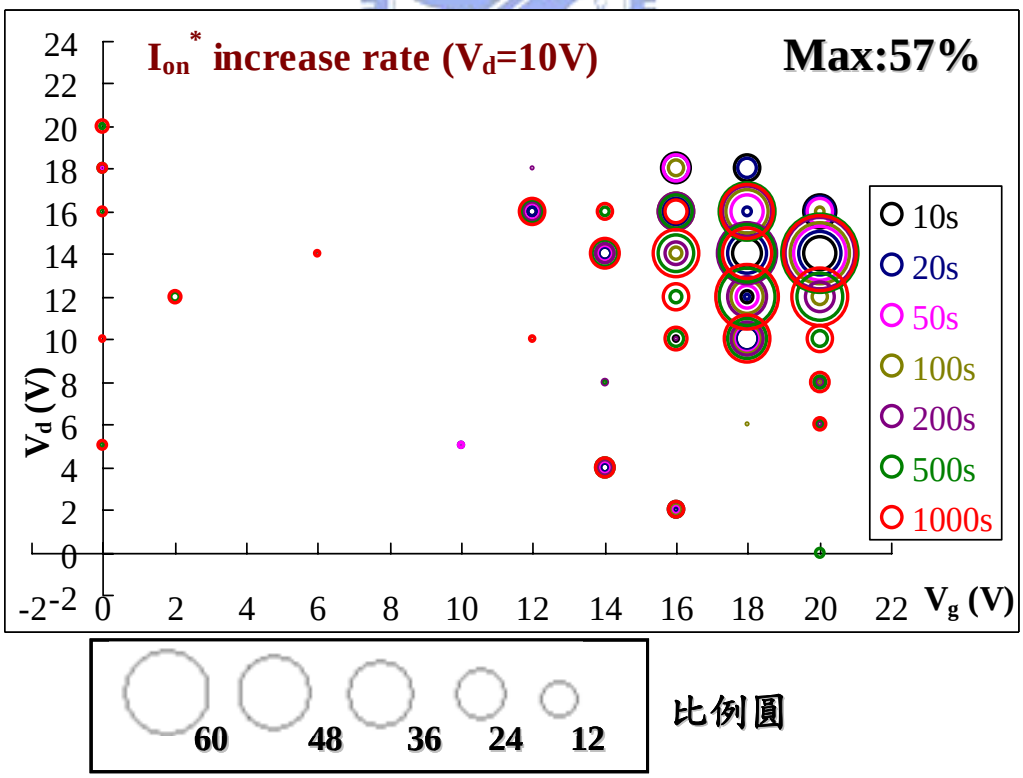


Fig. 2-12 Dependence of stress voltage on the I_{on}^* increase in the typical n-type TFTs (V_d=10V)

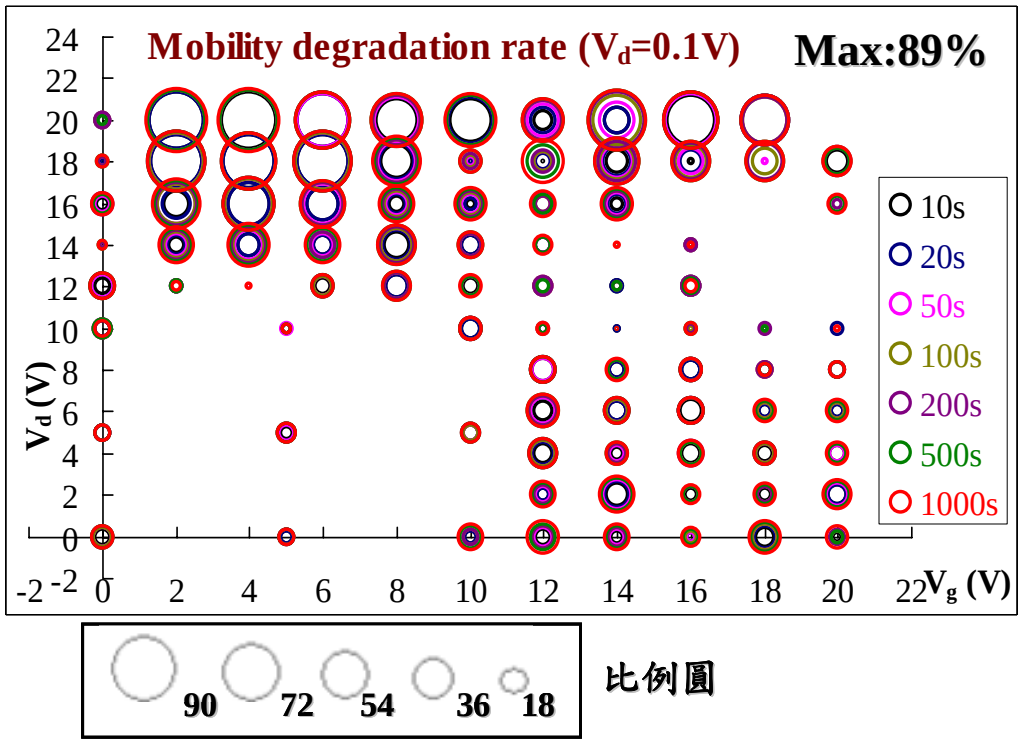


Fig. 2-13 Dependence of stress voltage on the mobility degradation in the typical n-type TFTs (V_d=0.1V)

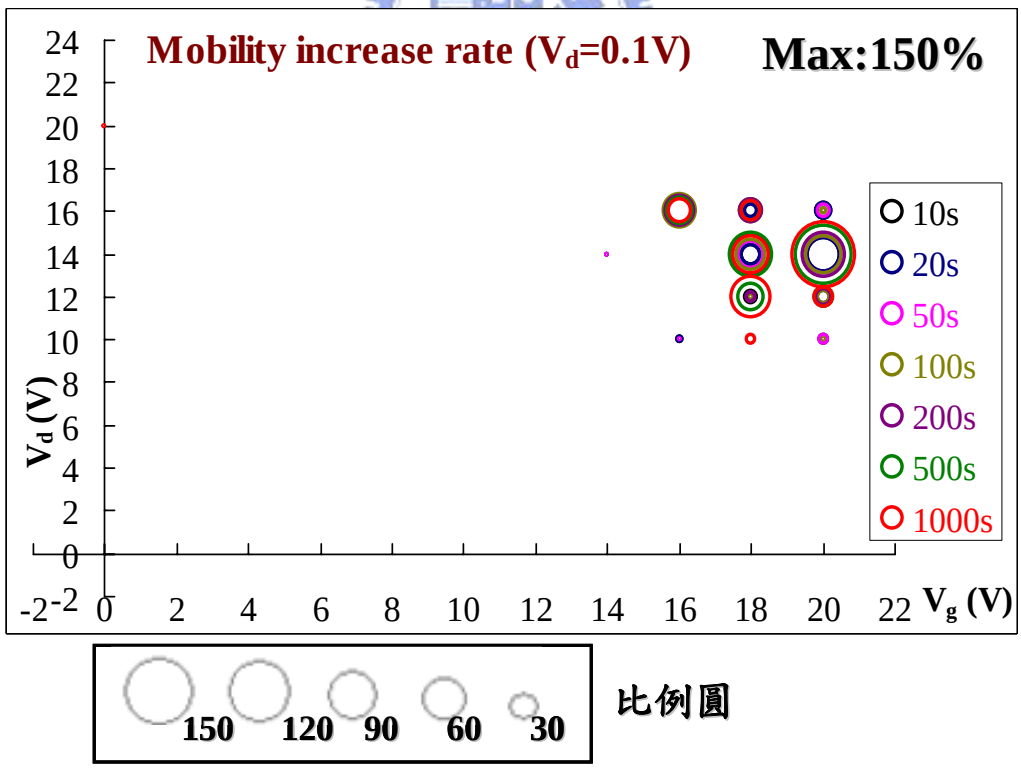


Fig. 2-14 Dependence of stress voltage on the mobility increase in the typical n-type TFTs (V_d=0.1V)

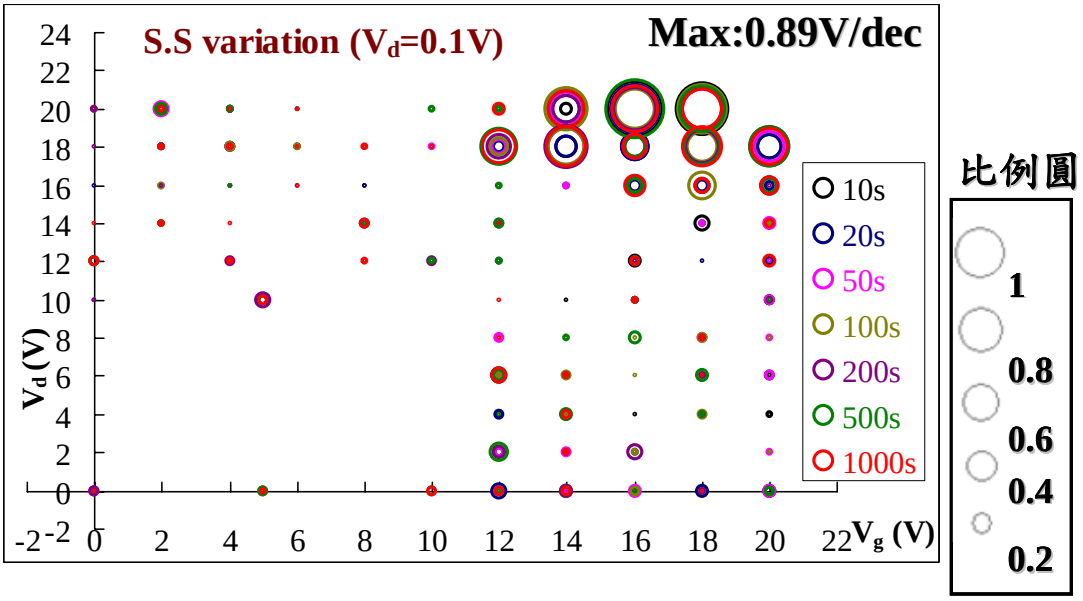


Fig. 2-15 Dependence of stress voltage on the Sub-threshold swing (S.S) variation in the typical n-type TFTs when V_d=0.1V.

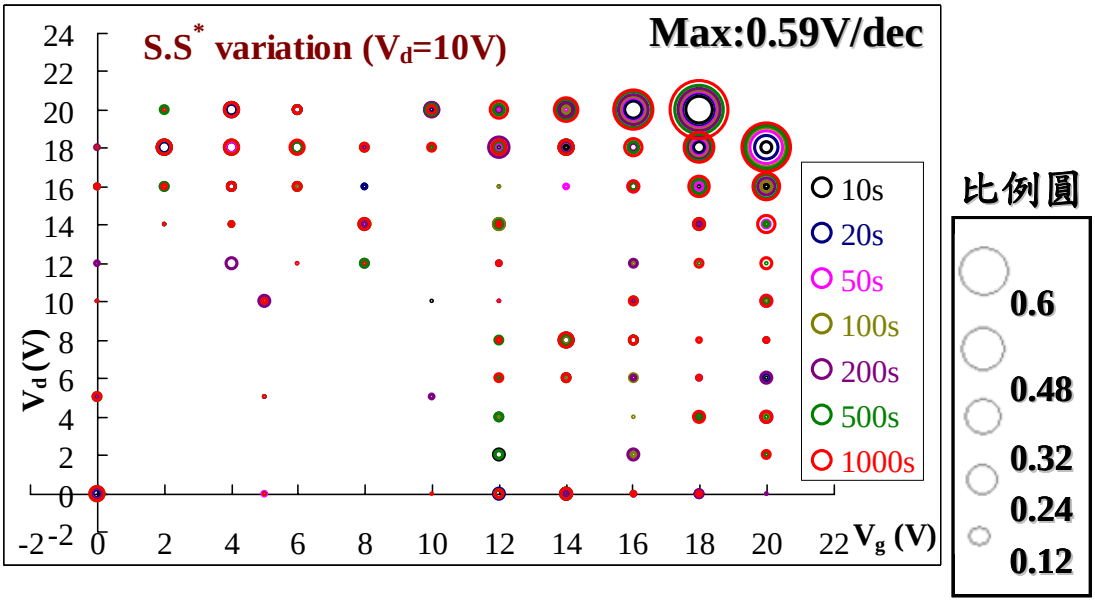


Fig. 2-16 Dependence of stress voltage on the Sub-threshold swing (S.S*) variation in the typical n-type TFTs when V_d=10V.

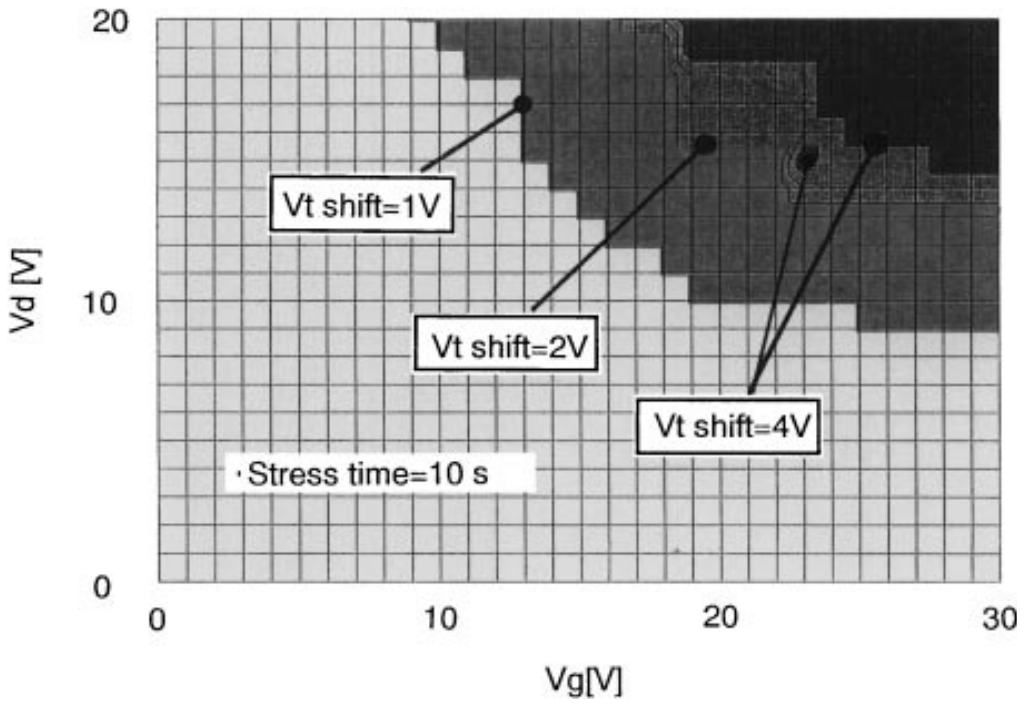


Fig. 2-17 Stress voltage dependence of the V_t shift of the typical TFTs. (JJAP Vol. 41 2002)

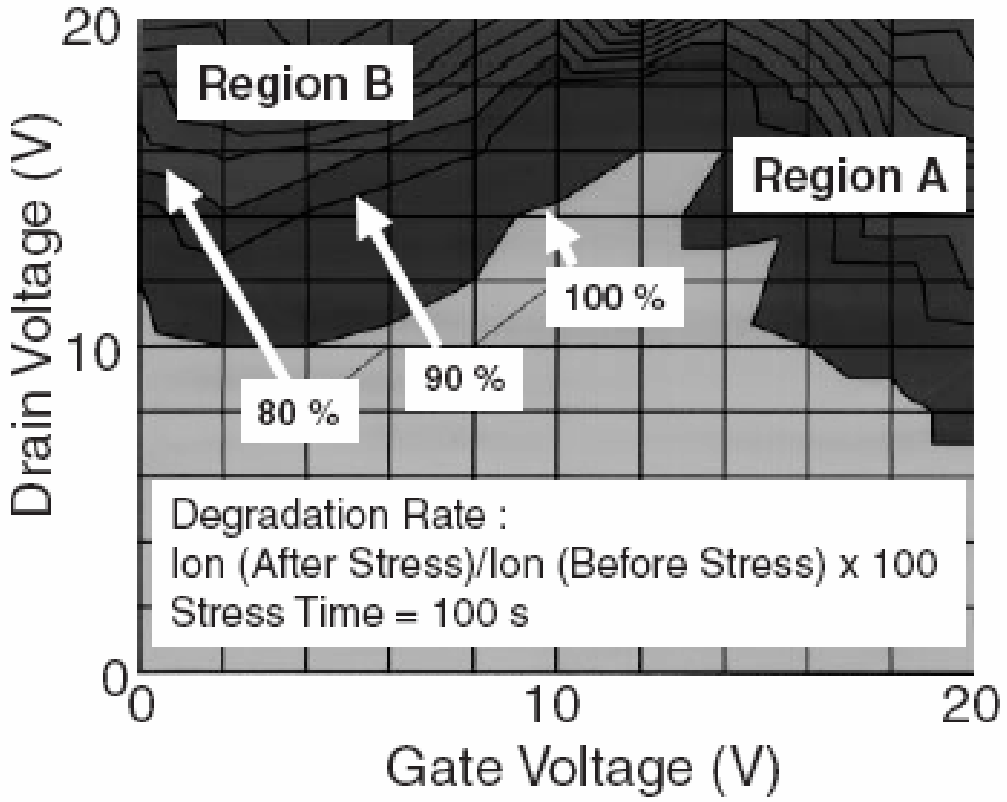


Fig. 2-18 Dependent of the stress voltage on the I_{on} variation in typical TFTs. The gate and drain voltages were each varied from 0V to 20V and stress time is 100s.(JJAP. Vol. 42 2003)

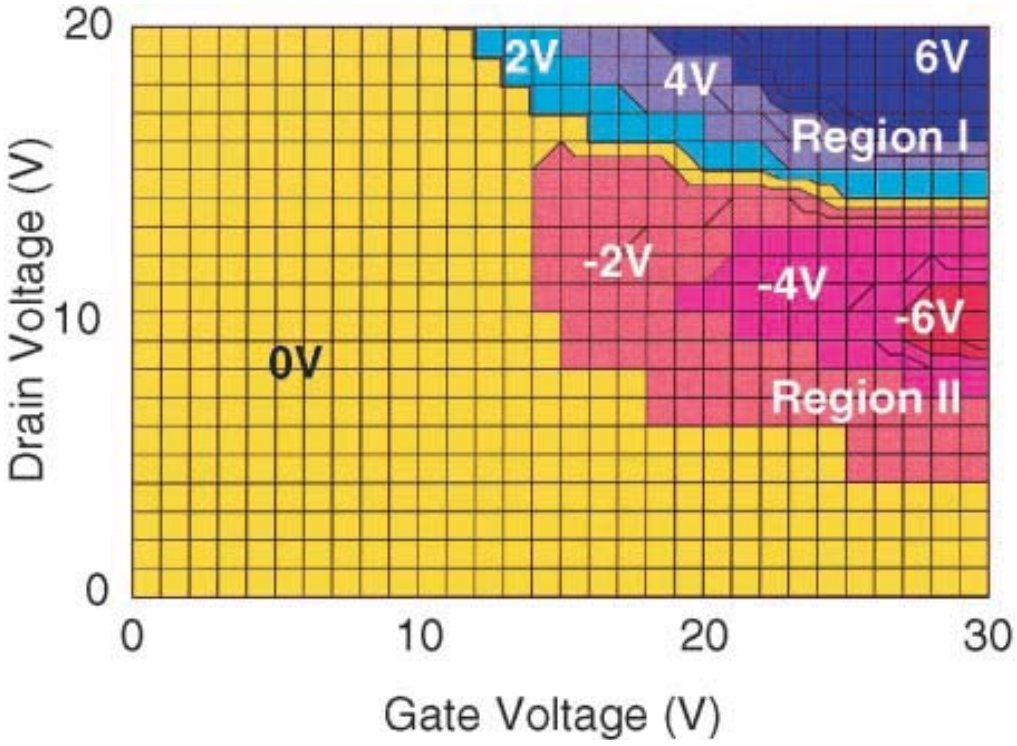


Fig. 2-19 Stress voltage dependence on the V_t shift in typical n-channel TFTs.

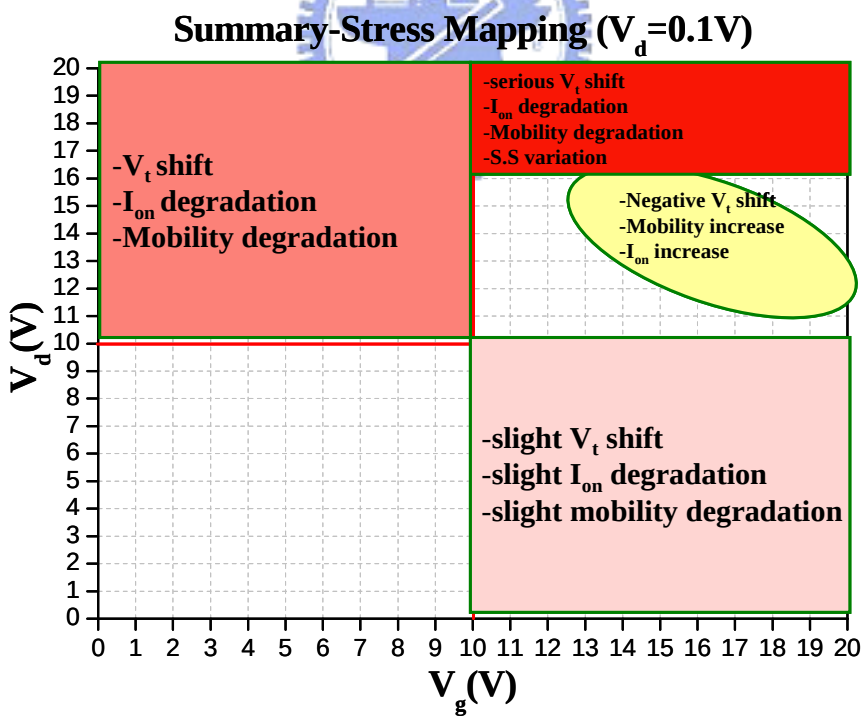


Fig. 2-20 Total phenomena summary of the stress map when V_d=0.1V.

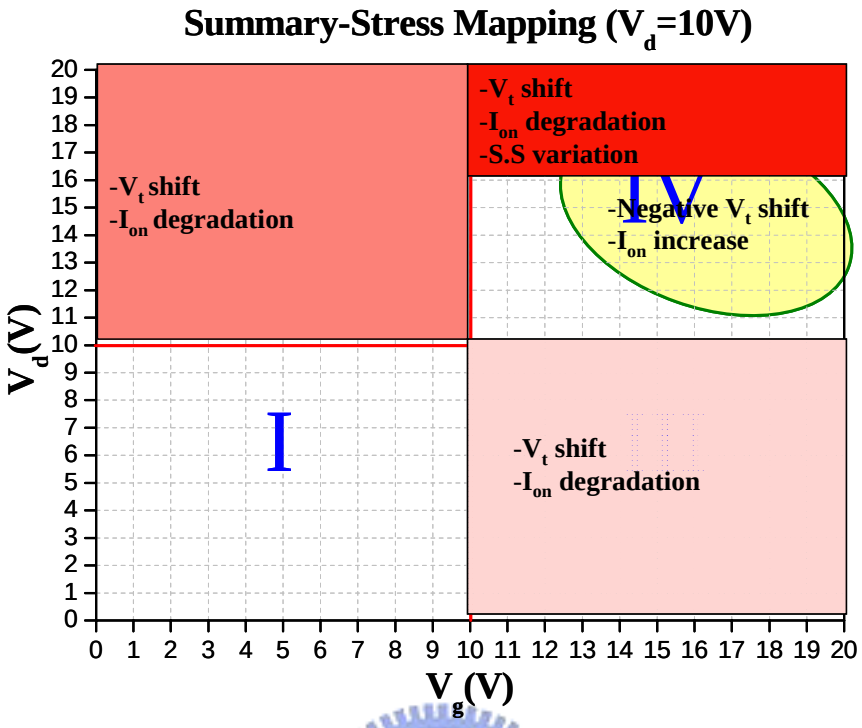


Fig. 2-21 Total phenomena summary of the stress map when V_d=10V.

Table 2-1 Summary the total phenomena in the region of the stress map.

region	phenomena	mechanism
Region I	ignore(for long time, still degradation)	none(for long time, hot carrier effect still happened)
Region II	V_t shift, I_{on} degradation, I_{on}^* degradation, Mobility degradation	hot carrier effect (low power and low lateral electric field)
Region III	slight V_t shift, slight I_{on} degradation, slight Mobility degradation	hot carrier effect (slight power and slight lateral electric field)
Region IV(upper)	serious V_t shift, V_t^* shift, negative V_t^* shift, I_{on} degradation, I_{on}^* degradation, I_{on}^* increase, Mobility degradation, S.S variation, S.S* variation	hot carrier effect and self-heating effect (large power and large lateral electric field)
Region IV(lower)	negative V_t shift, negative V_t^* shift, I_{on} increase, I_{on}^* increase, Mobility increase	oxide trapping effect

Chapter 3

Diverse Degradation Behaviors

3-1. Experiment

From the results of the chapter 2, we understood the factor of device variation has influence on the stress map. We also find out the special stress conditions with high stress gate voltage and medium stress drain voltage. Then, we choose several stress conditions including the special stress conditions with high stress gate condition and measure at least five devices in every stress conditions. The stress time is still up to 1000s.

3-2. Results and Discussion

Fig. 3-1 to fig. 3-60 show the time dependence of several device parameters degradation for vary initial characteristic device under the same stress condition. From these results we can know the degradation phenomena were diverse even in the same stress condition. Besides, some stress conditions still have the same tendency of the degradation. We sure the device variation has the great influence on the stress map. Fig. 3-61 to fig. 3-65 show the variation of several device parameters degradation under different stress conditions. The serious degradation variations were occurred in the high stress drain voltage and the high stress gate voltage. We know the degradation reasons of the threshold voltage and the sub-threshold swing come from

the deep state traps (dangling bonds). The degradation variation results of the V_t shift and the S.S degradation were similar.

3-3. Conclusion

From the previous discussion, we know the larger stress voltage will results in the worst degradation variation. The V_t shift degradation variation phenomenon was similar to the S.S degradation variation phenomenon. The device variation has the great influence on the device degradation. Except these, we also find out the special degradation variation region in boundary of the region II and the region IV. We will further discuss that in the fallowing chapter.

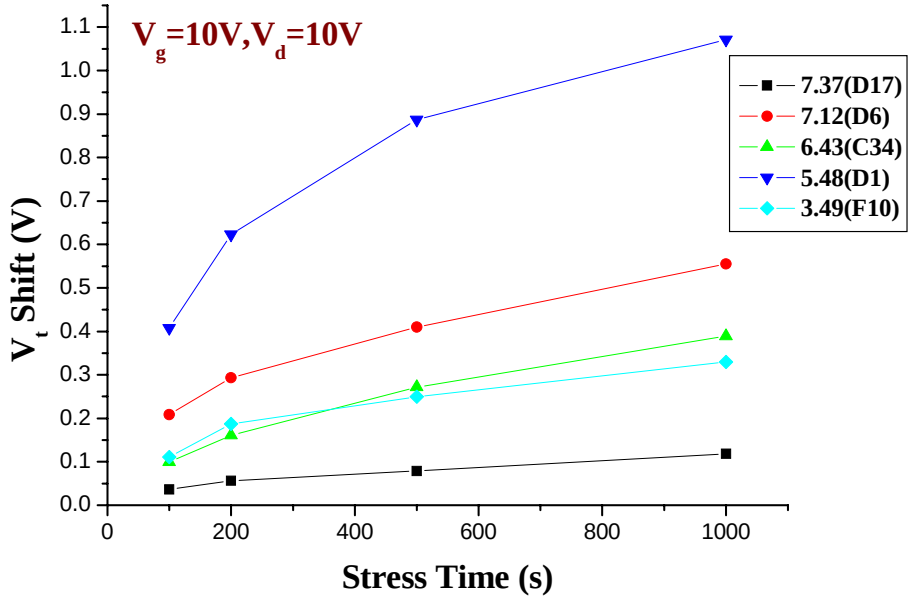


Fig. 3-1 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=10V.

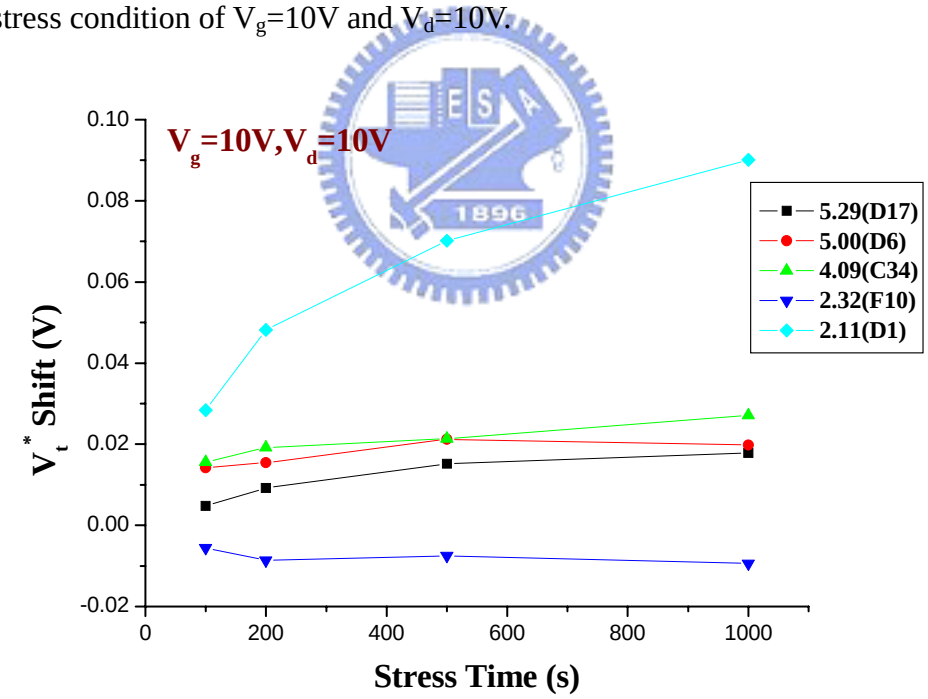


Fig. 3-2 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=10V.

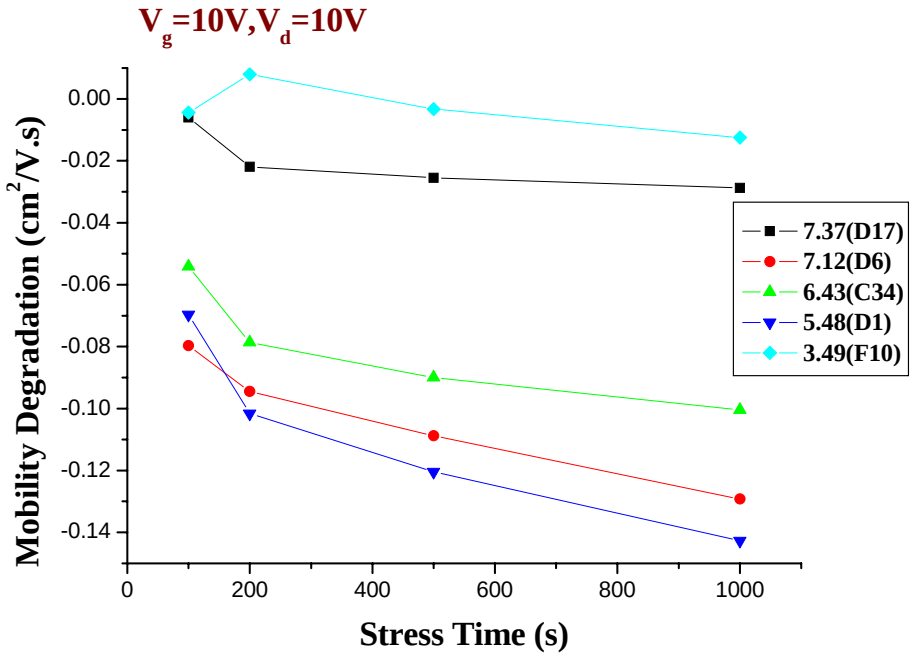


Fig. 3-3 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=10V.

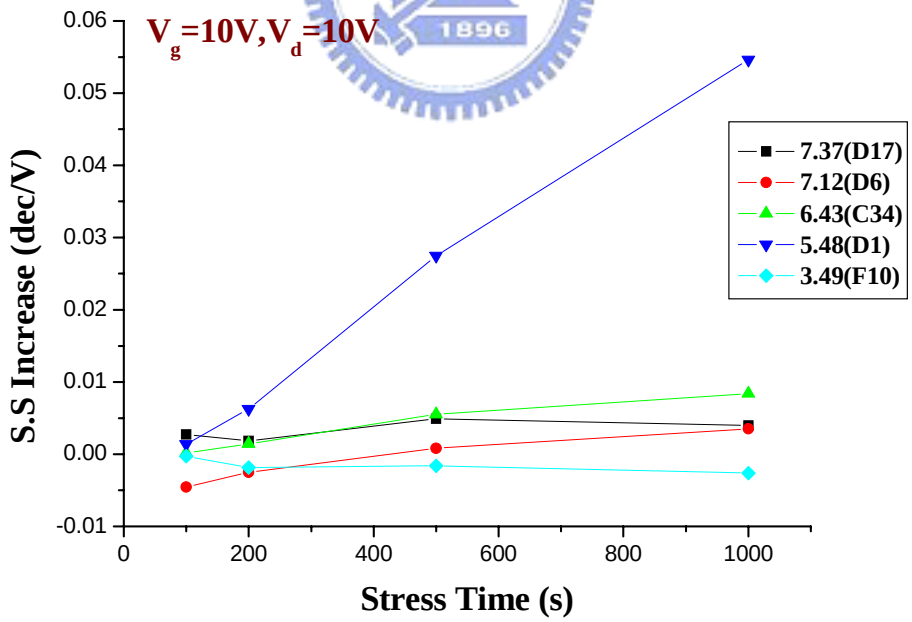


Fig. 3-4 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=10V.

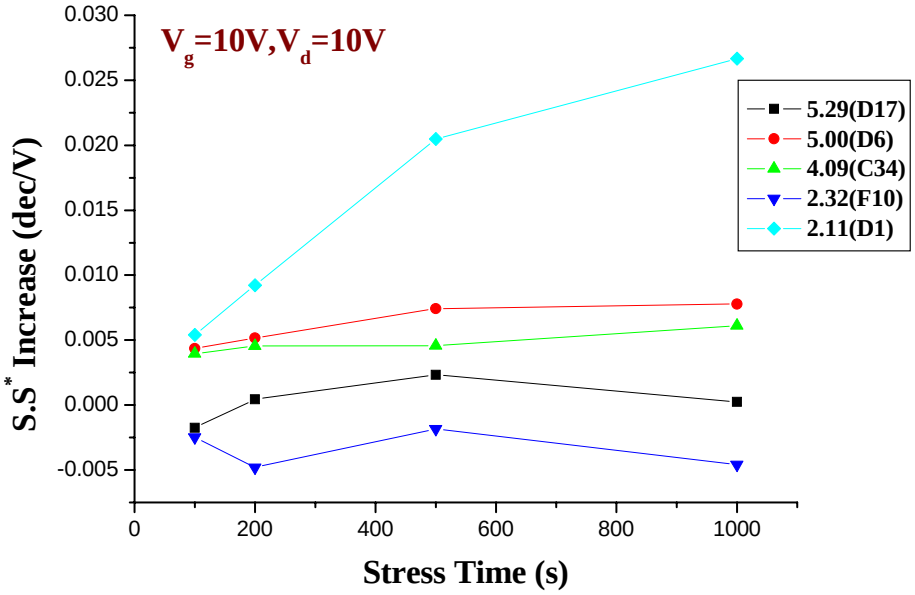


Fig. 3-5 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=10V.

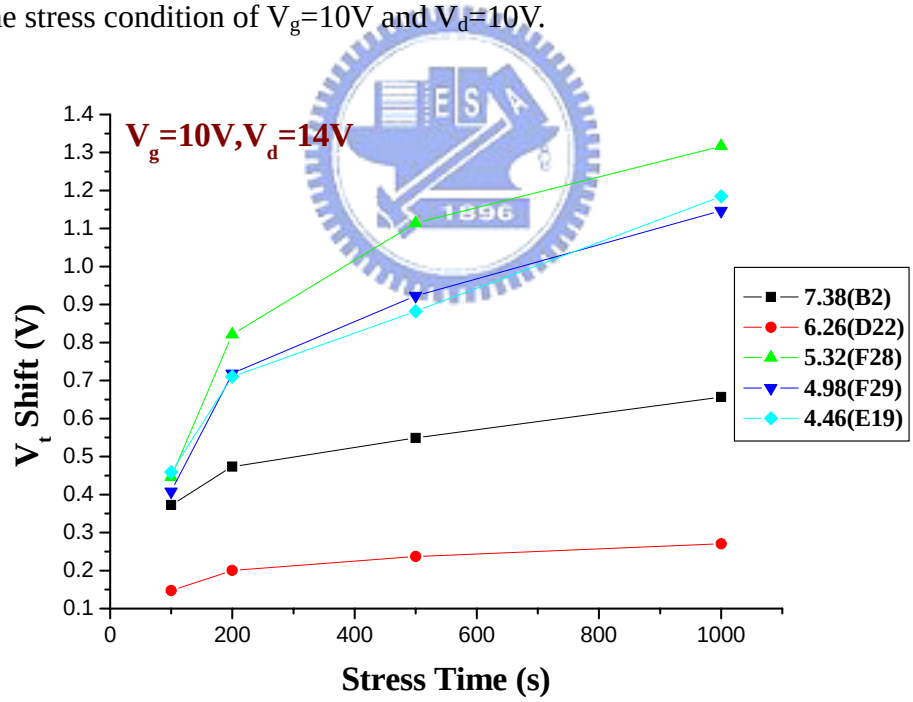


Fig. 3-6 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=14V.

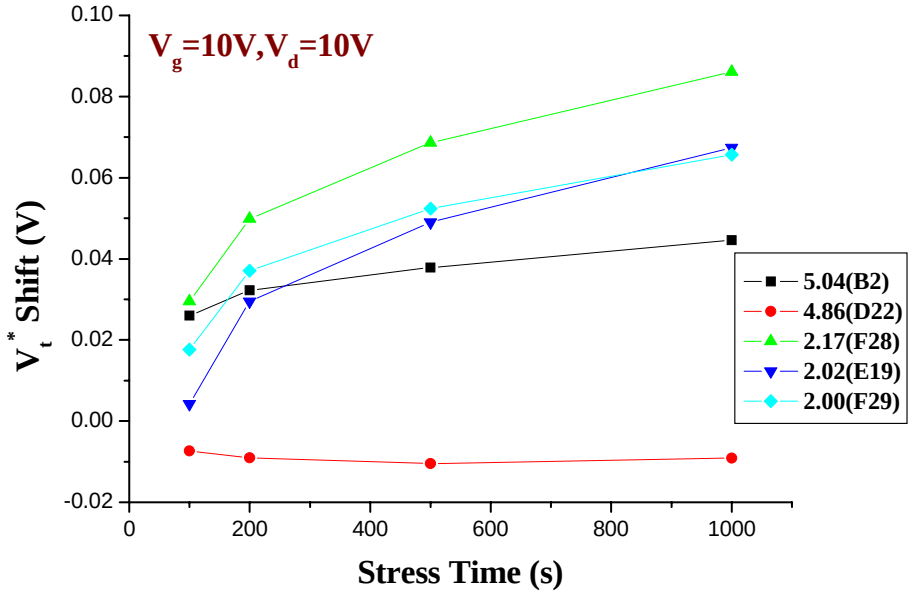


Fig. 3-7 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=14V.

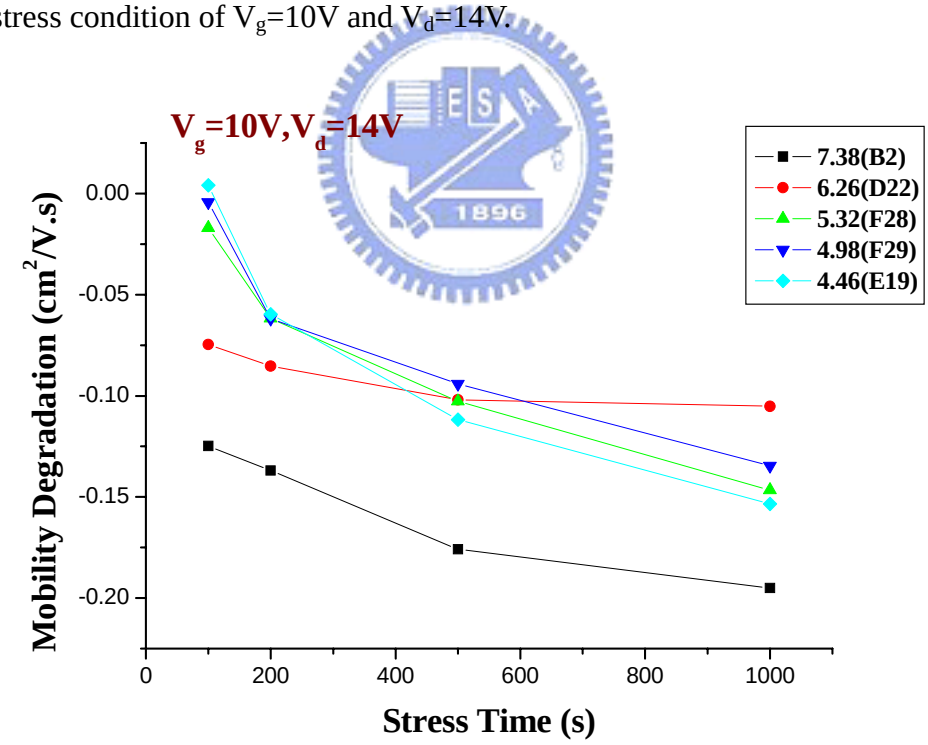


Fig. 3-8 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=14V.

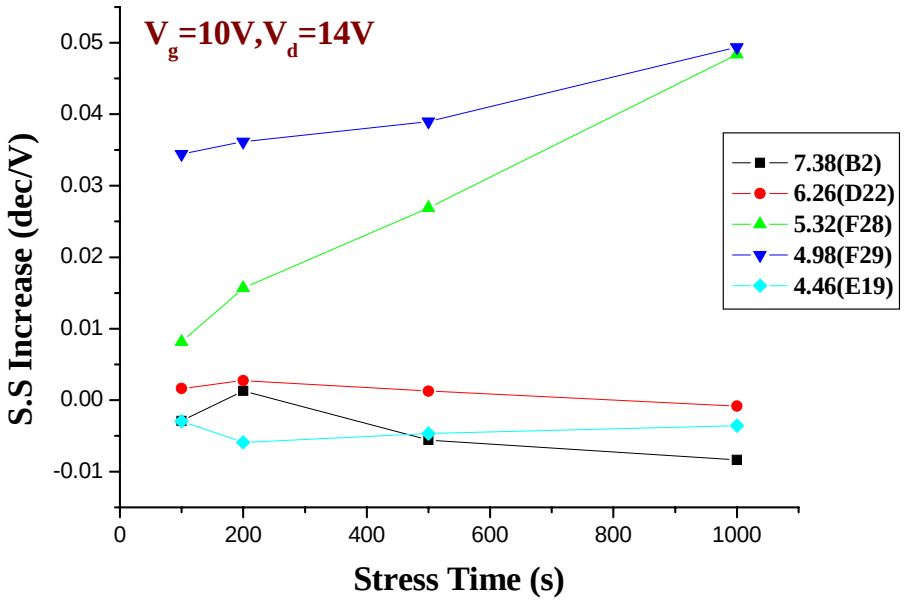


Fig. 3-9 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=14V.

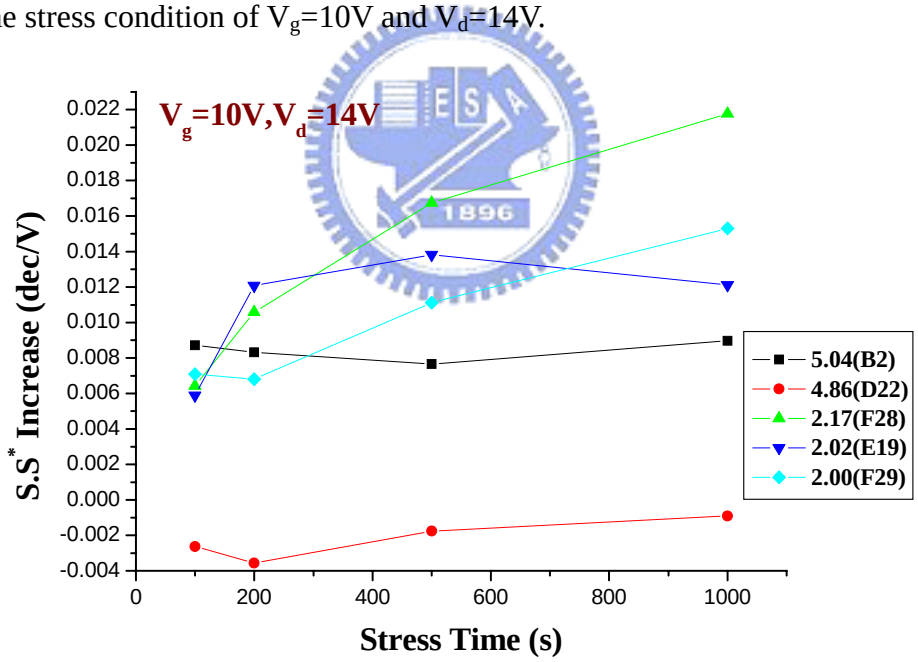


Fig. 3-10 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=14V.

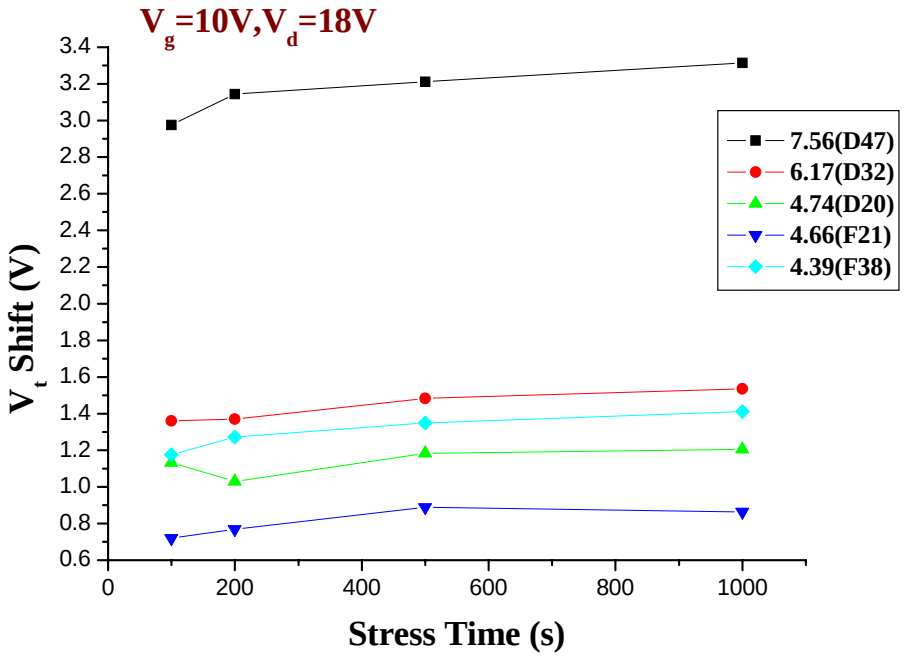


Fig. 3-11 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=18V.

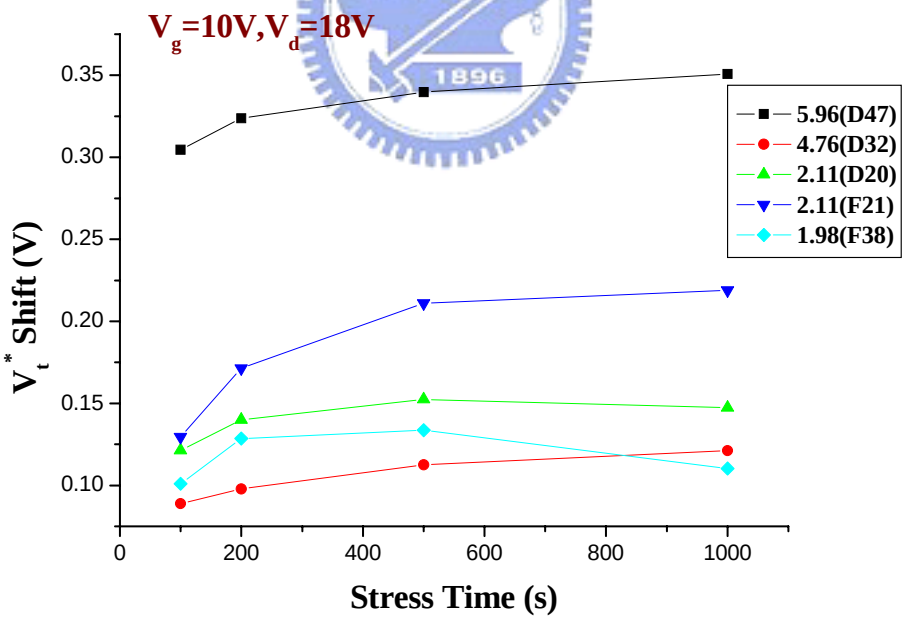


Fig. 3-12 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=18V.

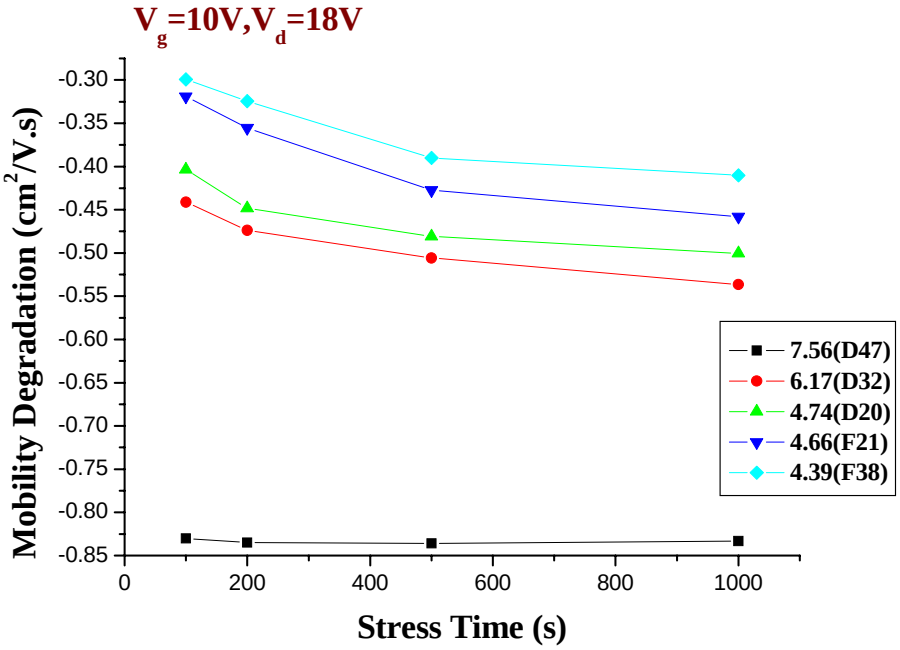


Fig. 3-13 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=18V.

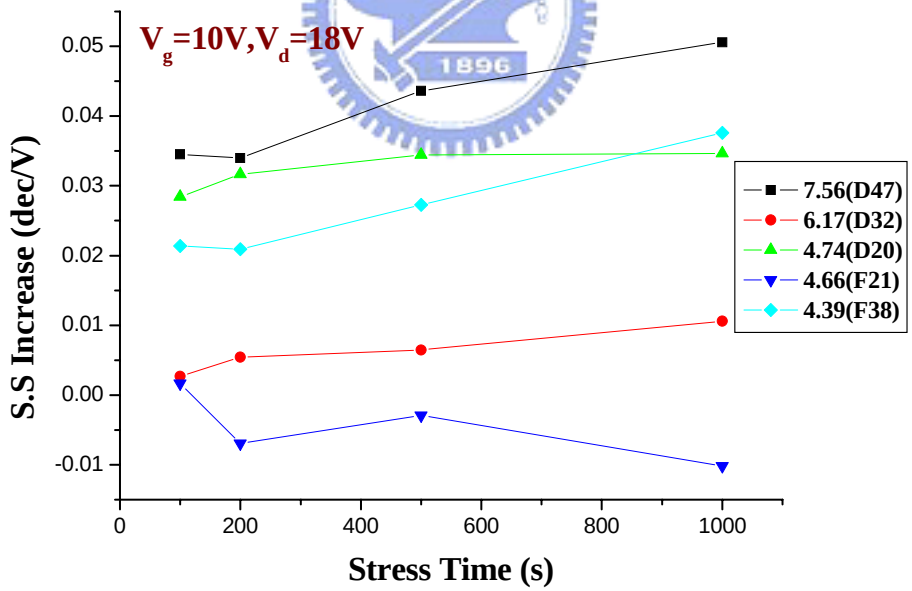


Fig. 3-14 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=18V.

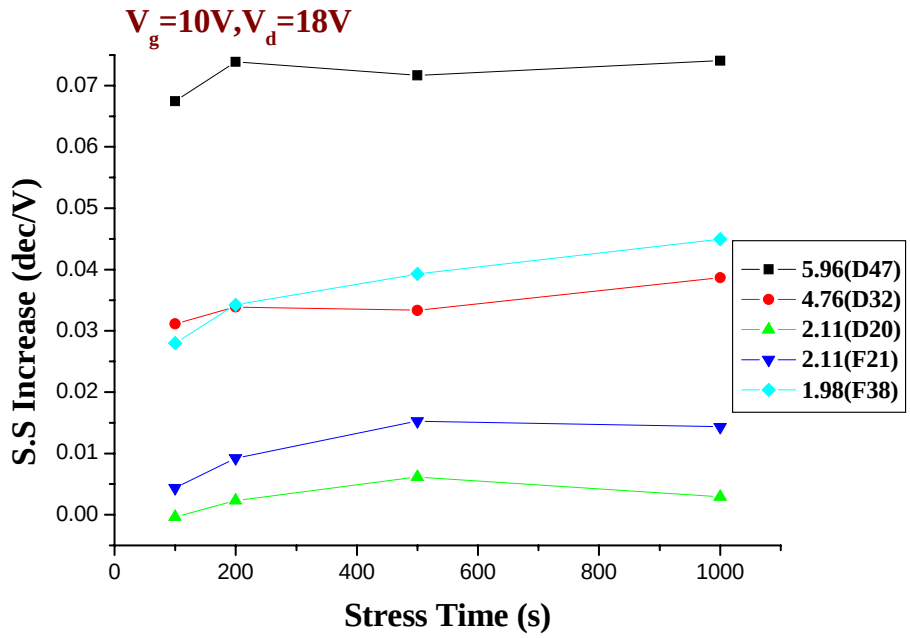


Fig. 3-15 Time dependence of S.S* increase for vary initial characteristic devices under the same stress condition of V_g=10V and V_d=18V.

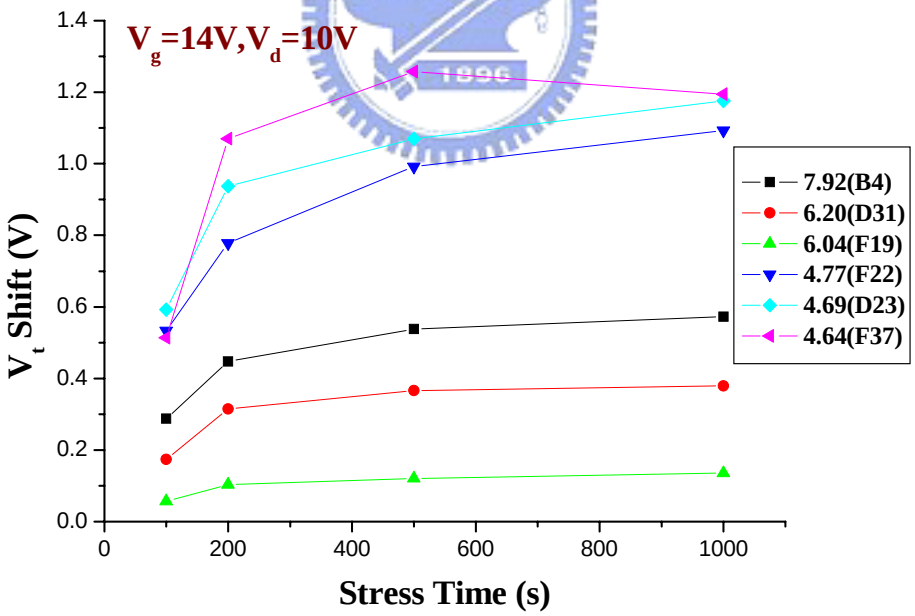


Fig. 3-16 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=10V.

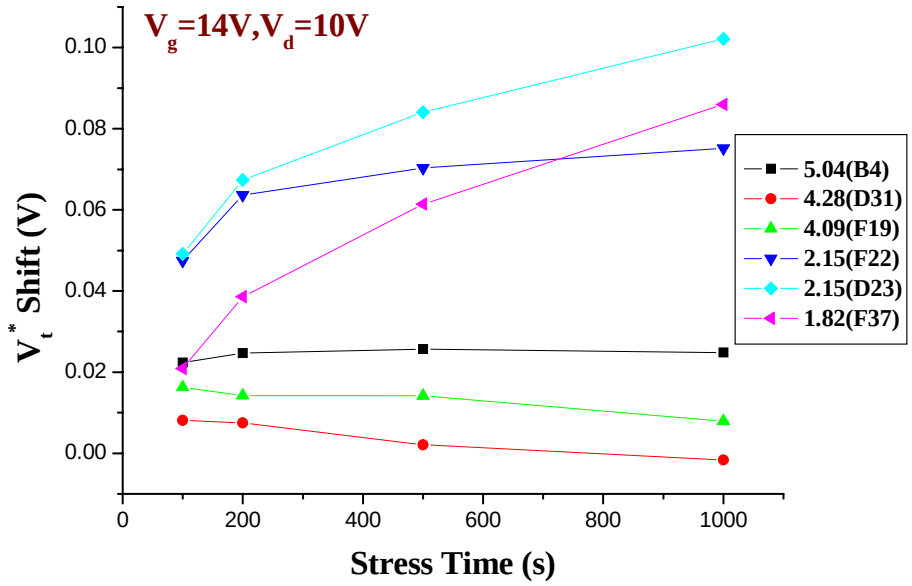


Fig. 3-17 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=10V.

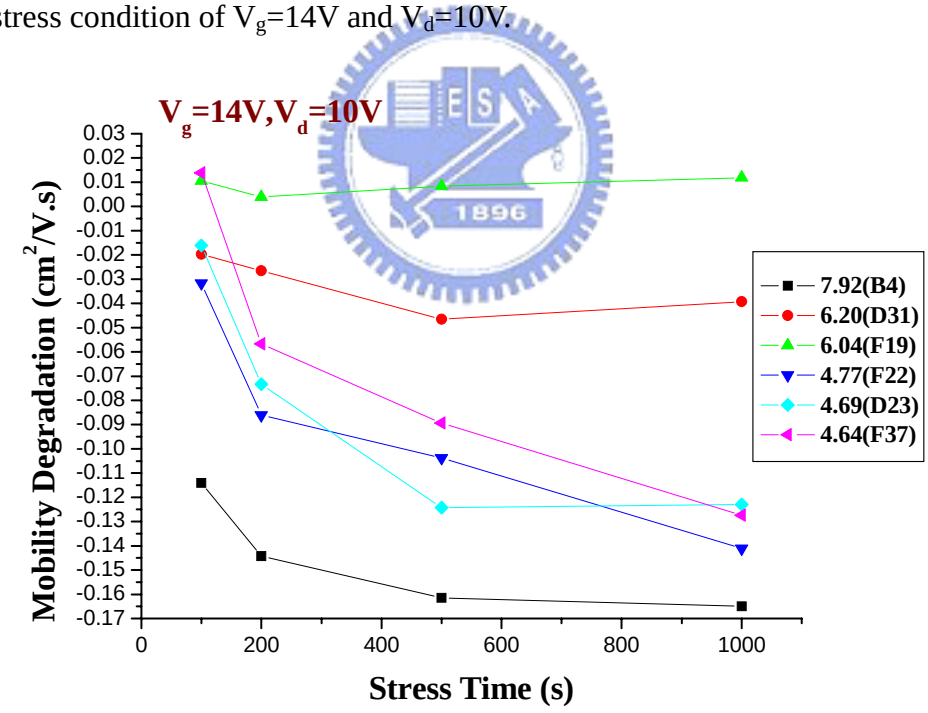


Fig. 3-18 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=10V.

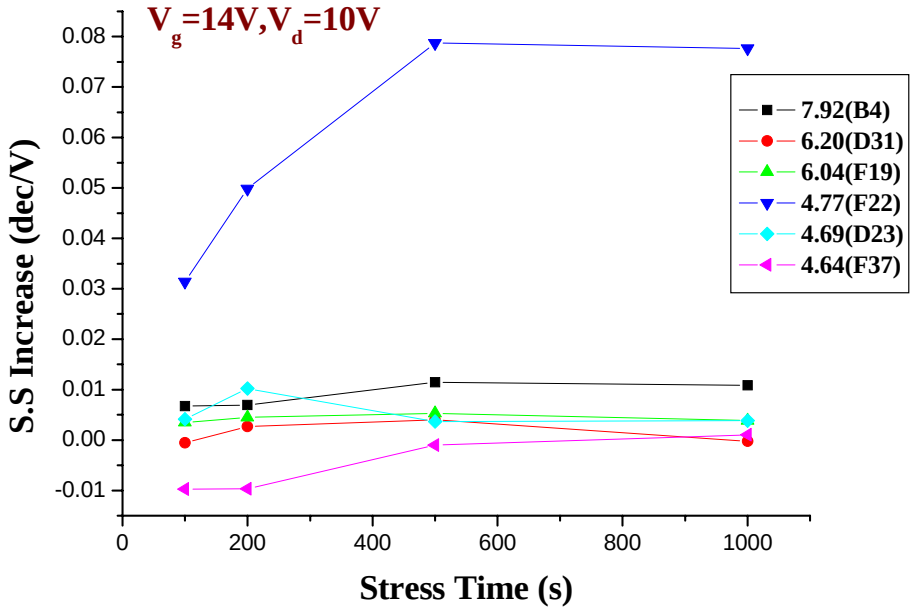


Fig. 3-19 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=10V.

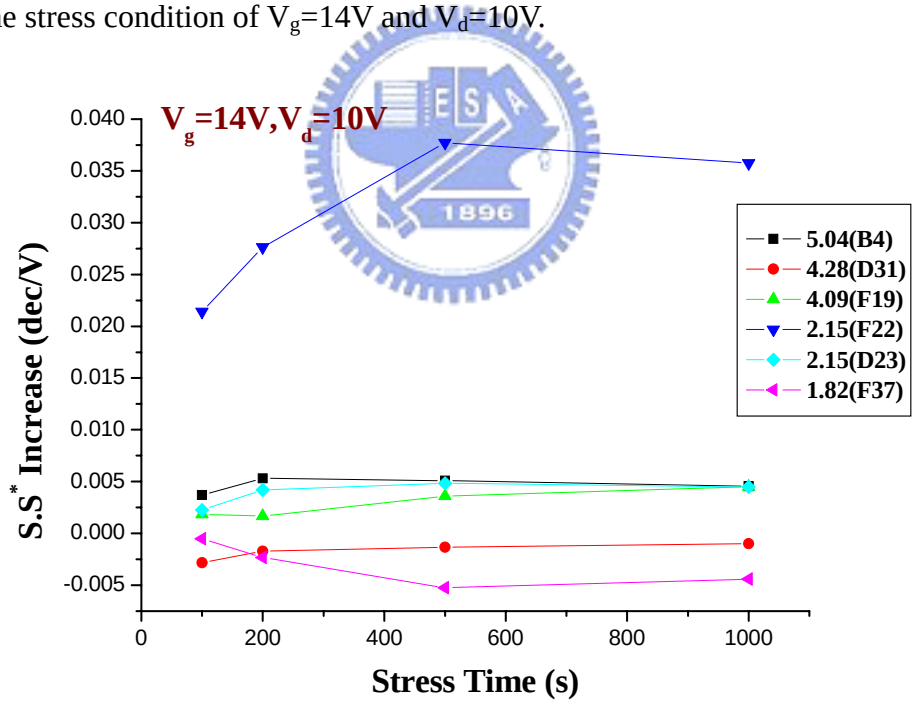


Fig. 3-20 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=10V.

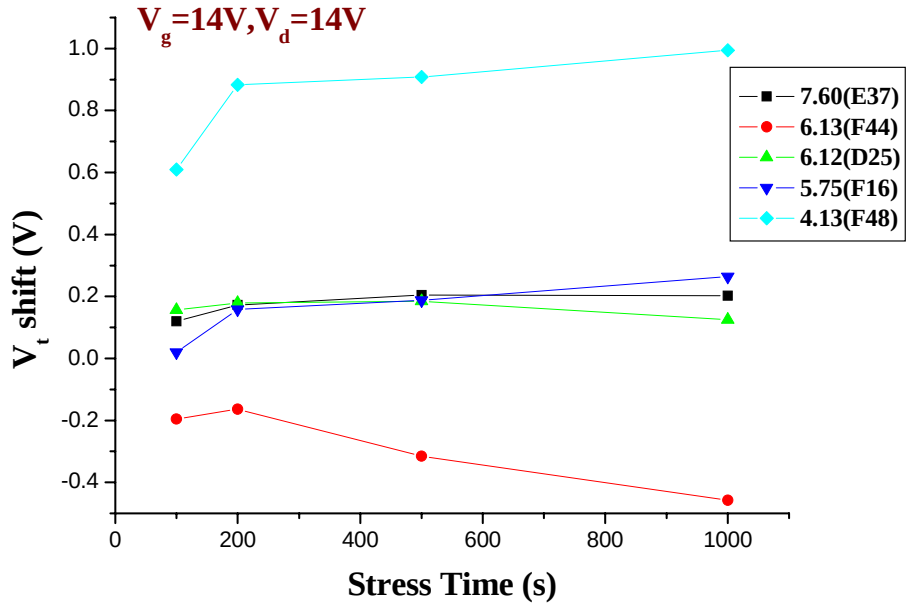


Fig. 3-21 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=14V.

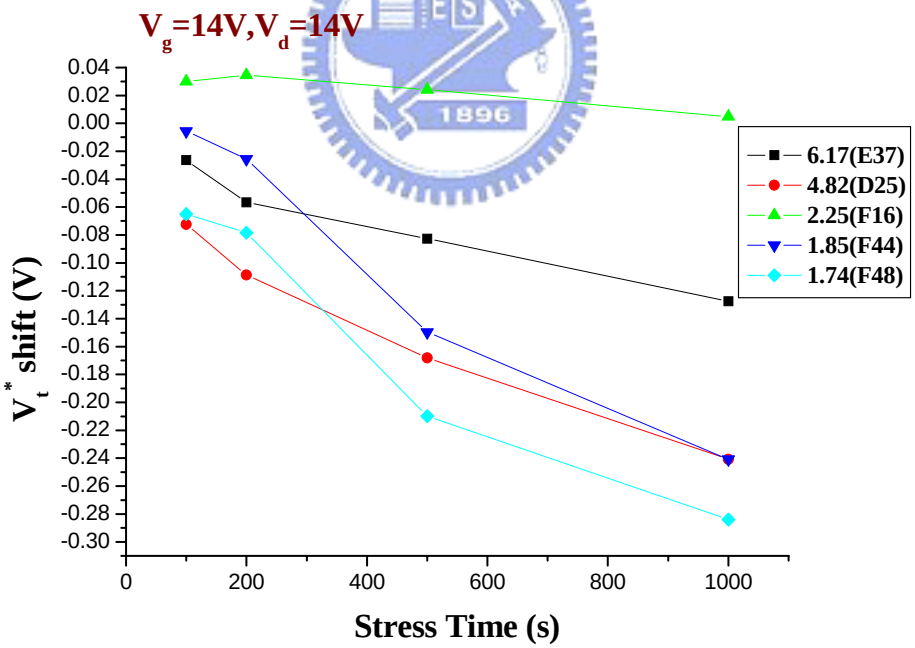


Fig. 3-22 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=14V.

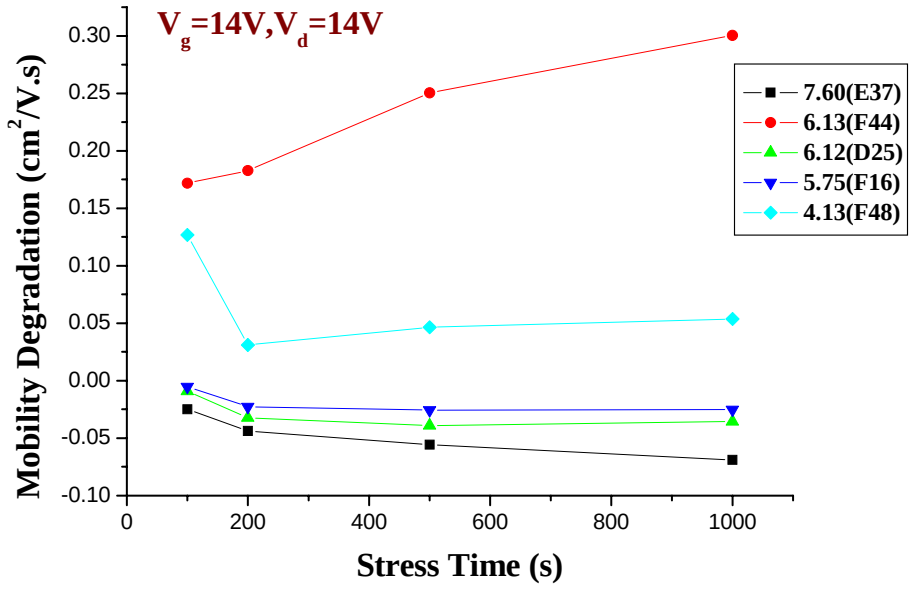


Fig. 3-23 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=14V.

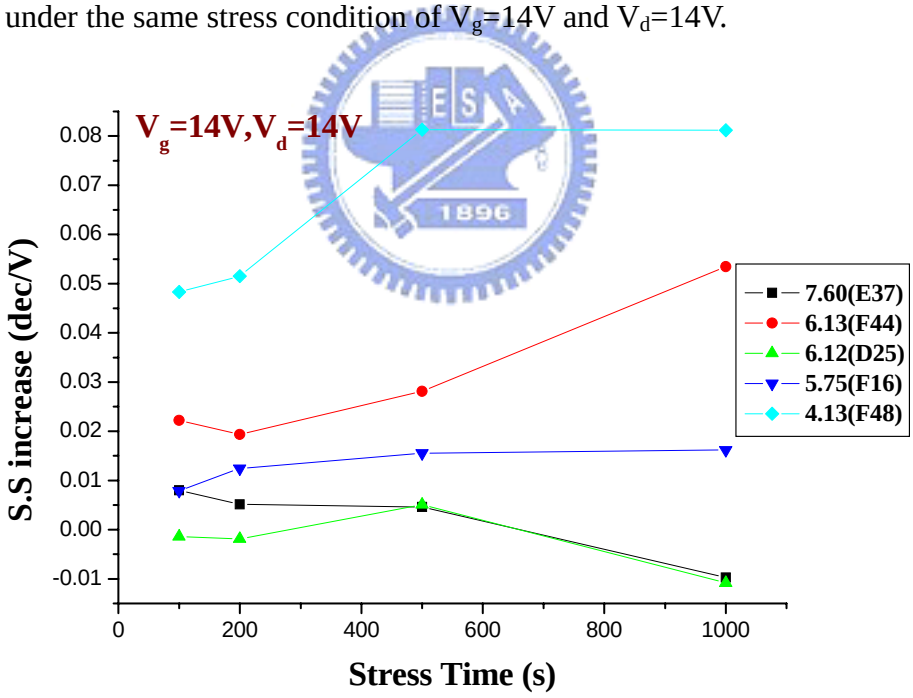


Fig. 3-24 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=14V.

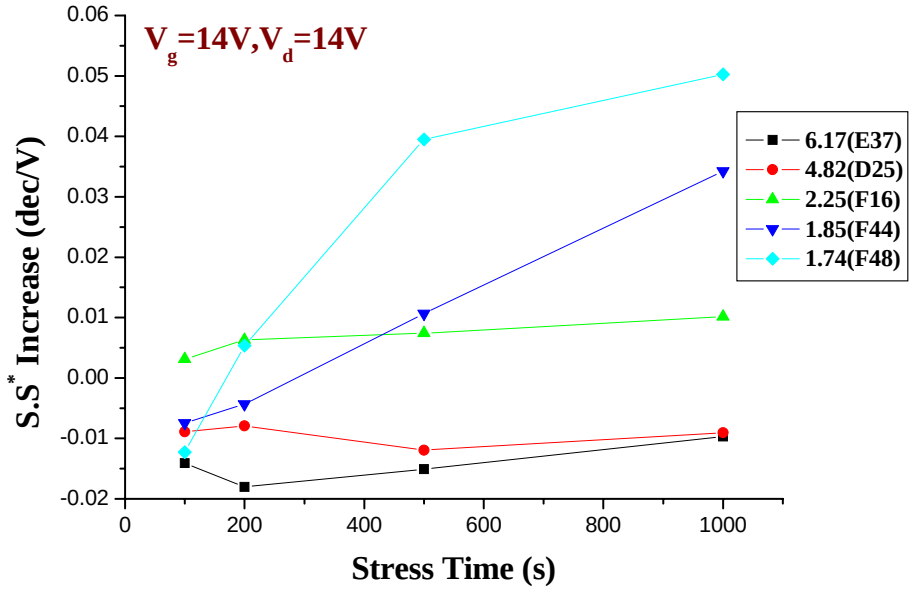


Fig. 3-25 Time dependence of $S.S^{*}$ increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=14V.

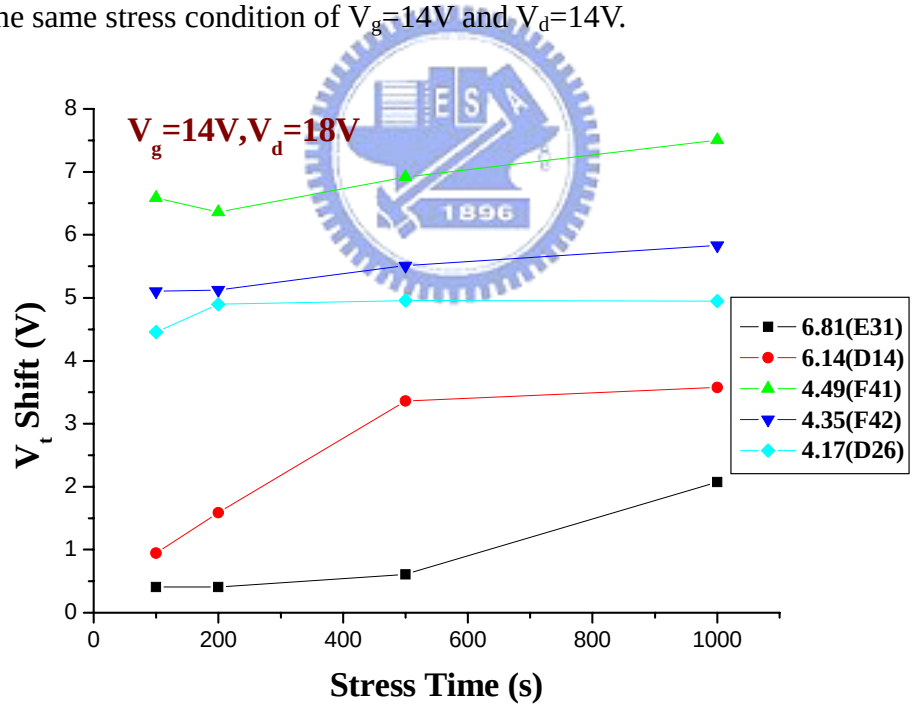


Fig. 3-26 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=18V.

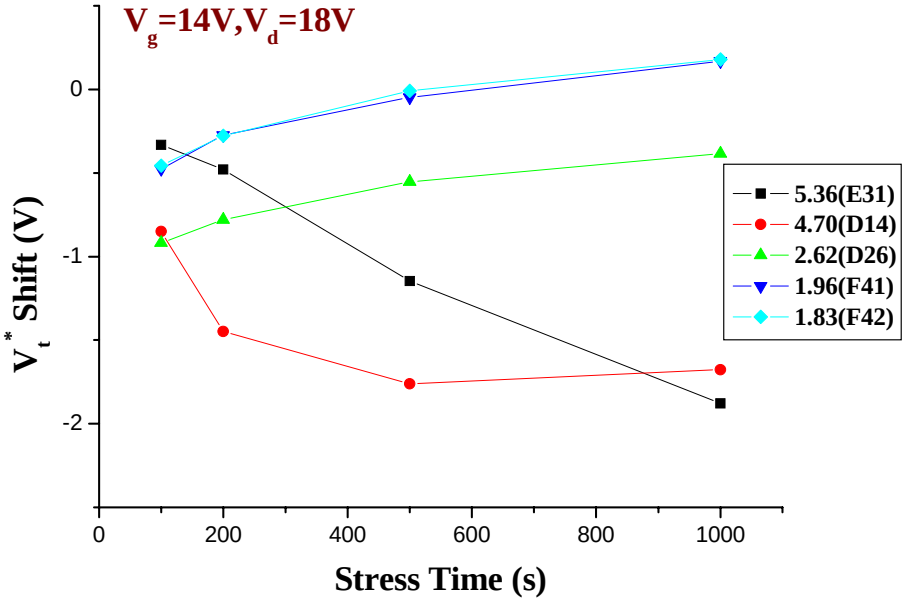


Fig. 3-27 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=18V.

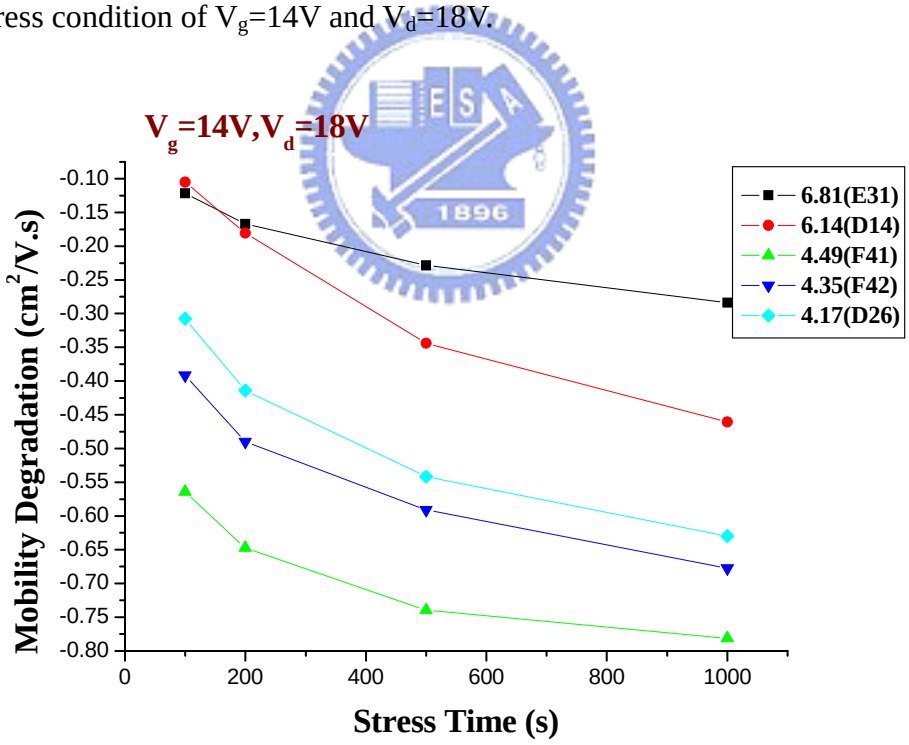


Fig. 3-28 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=18V.

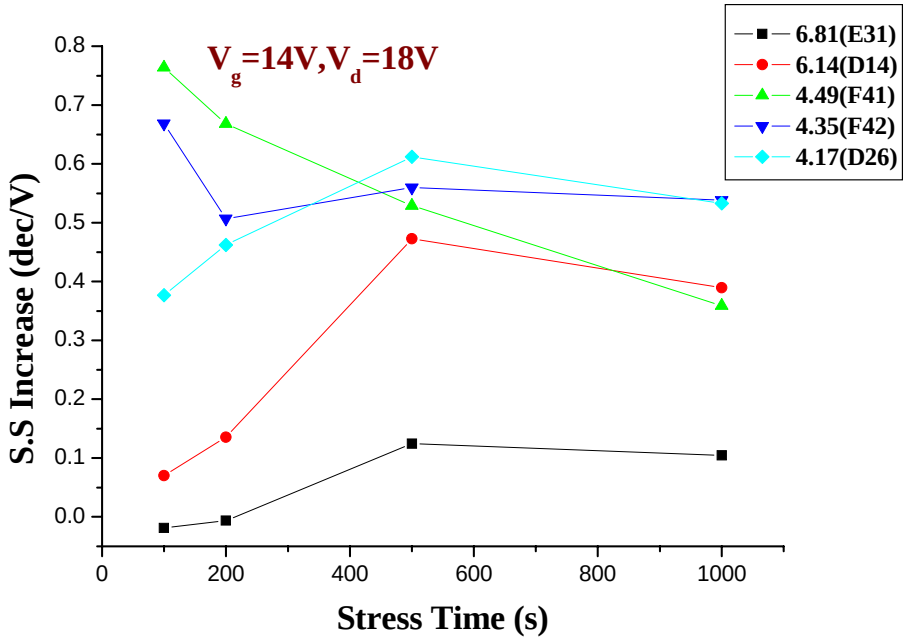


Fig. 3-29 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=18V.

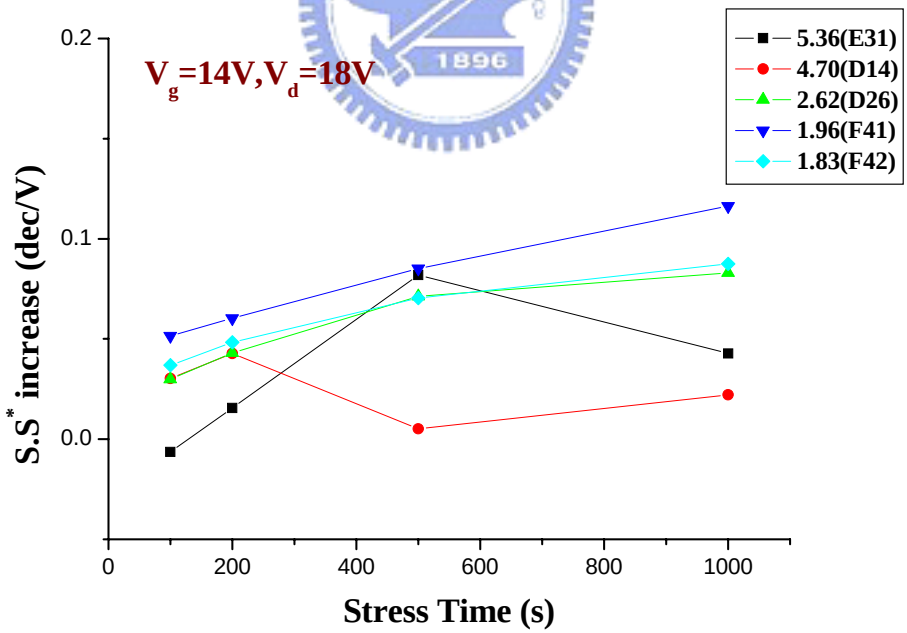


Fig. 3-30 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=14V and V_d=18V.

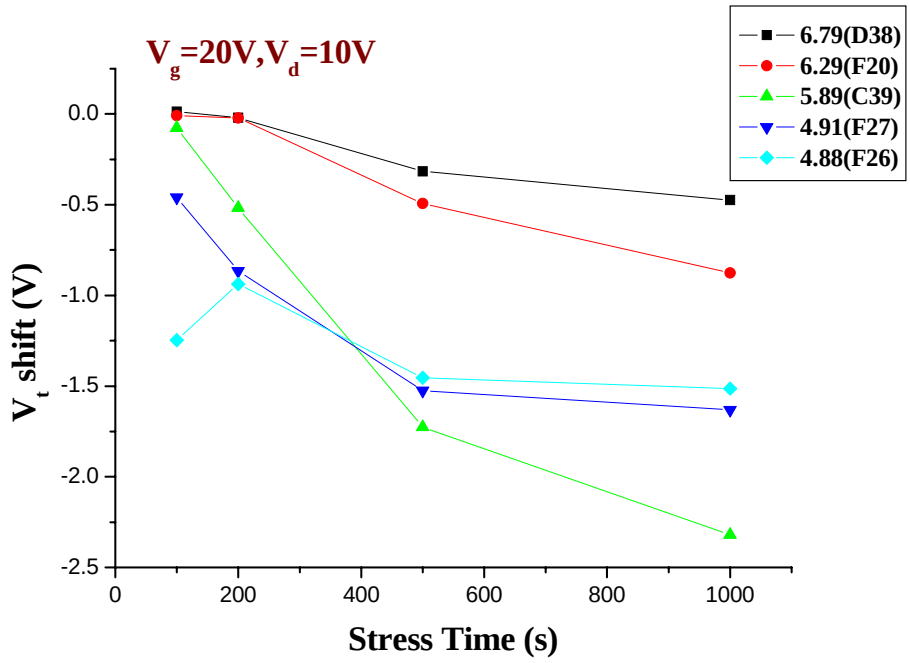


Fig. 3-31 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=10V.

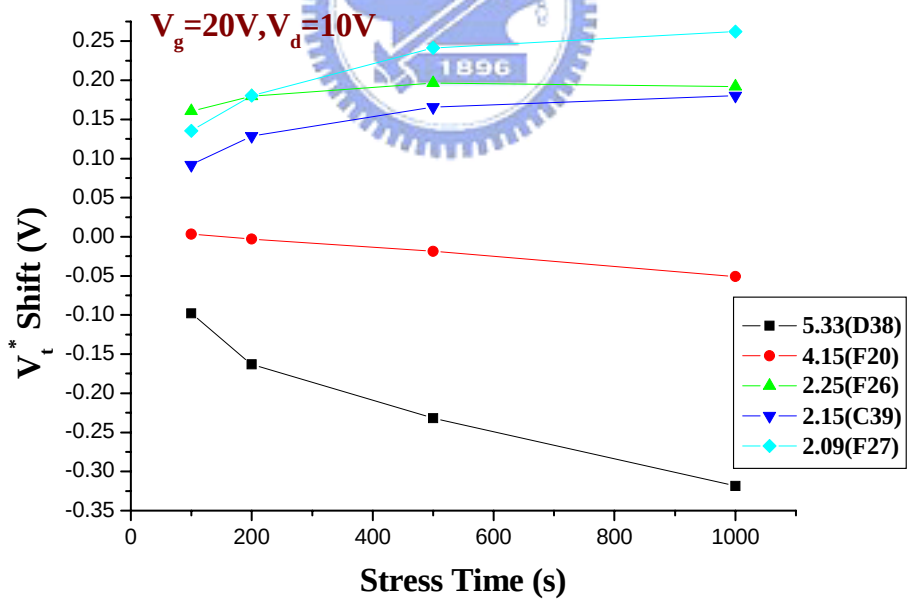


Fig. 3-32 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=10V.

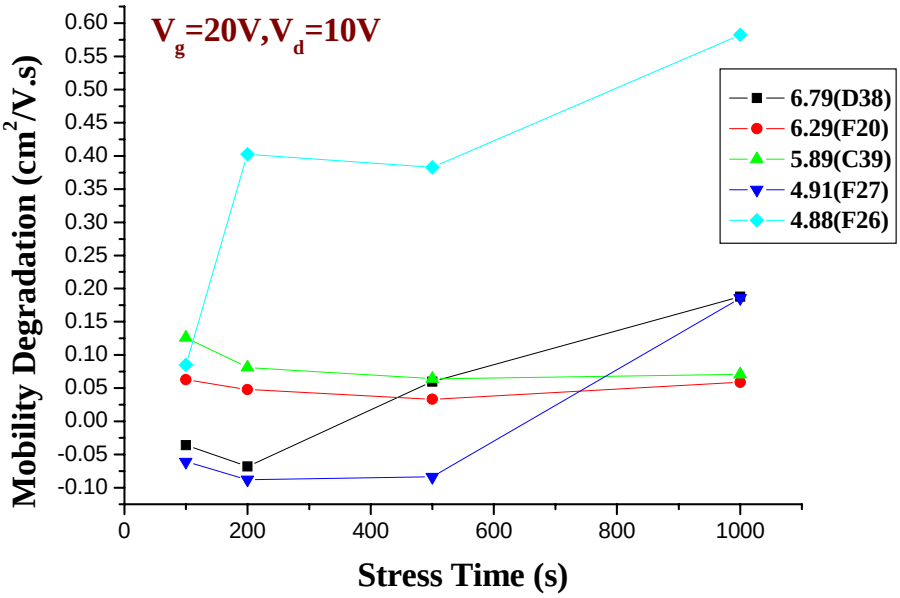


Fig. 3-33 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=10V.

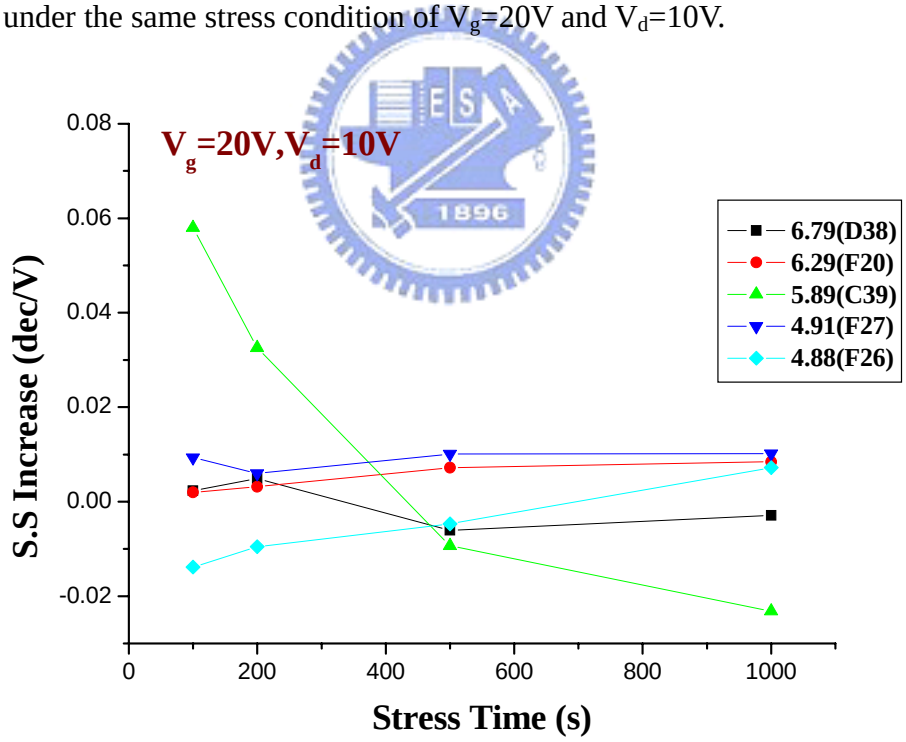


Fig. 3-34 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=10V.

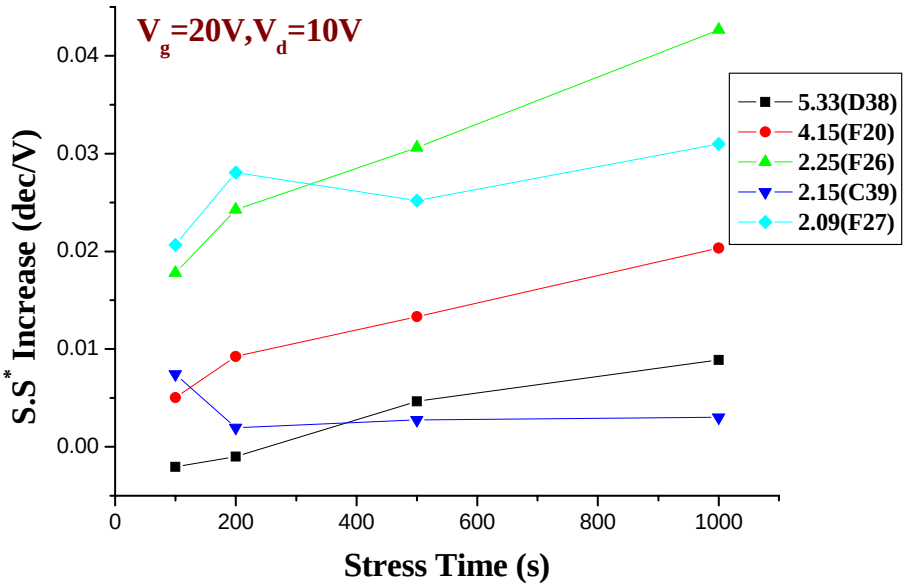


Fig. 3-35 Time dependence of $S.S^{*}$ increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=10V.

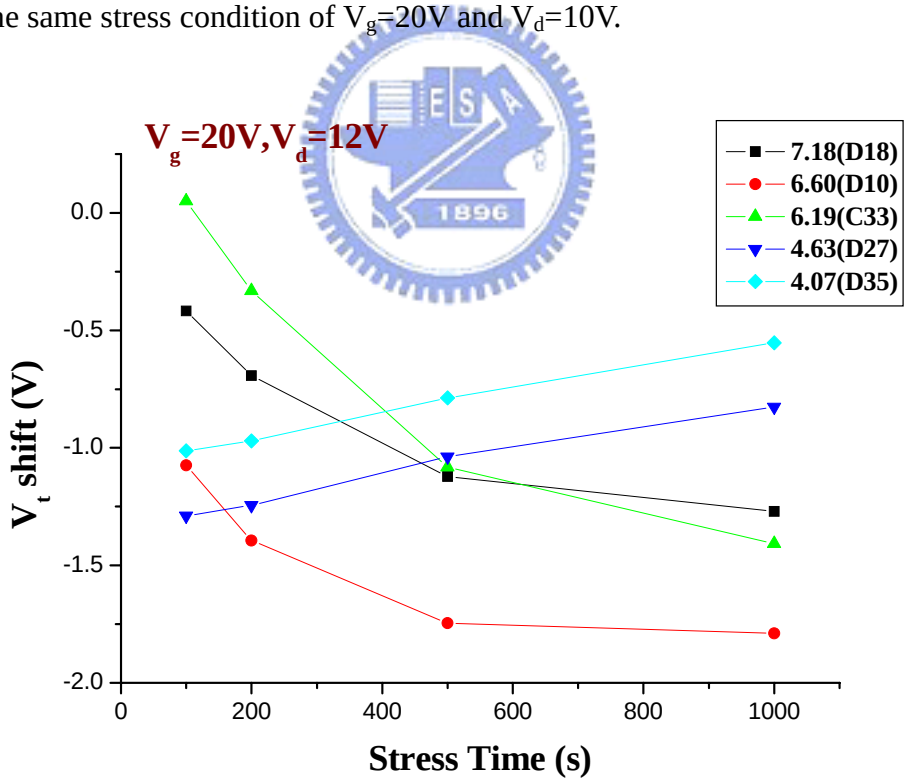


Fig. 3-36 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=12V.

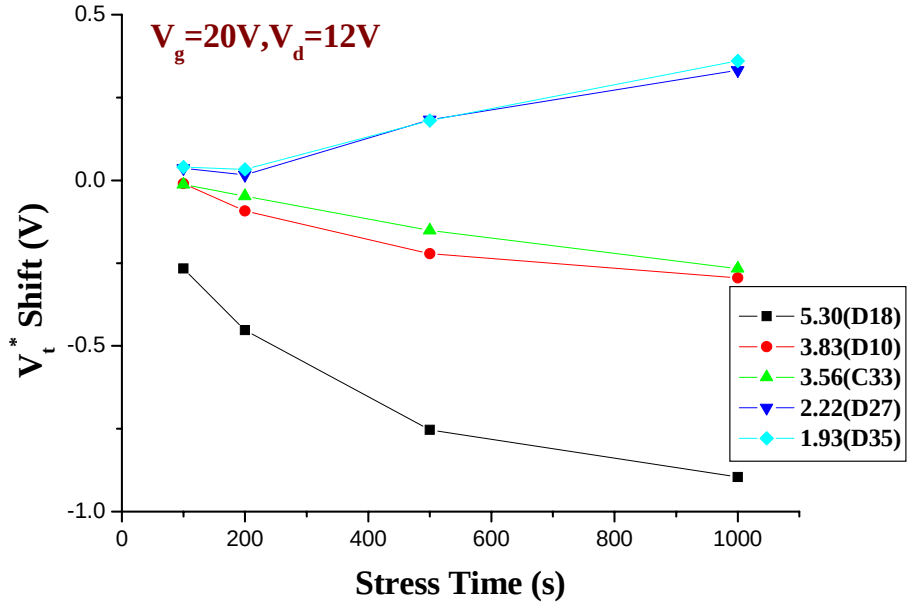


Fig. 3-37 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=12V.

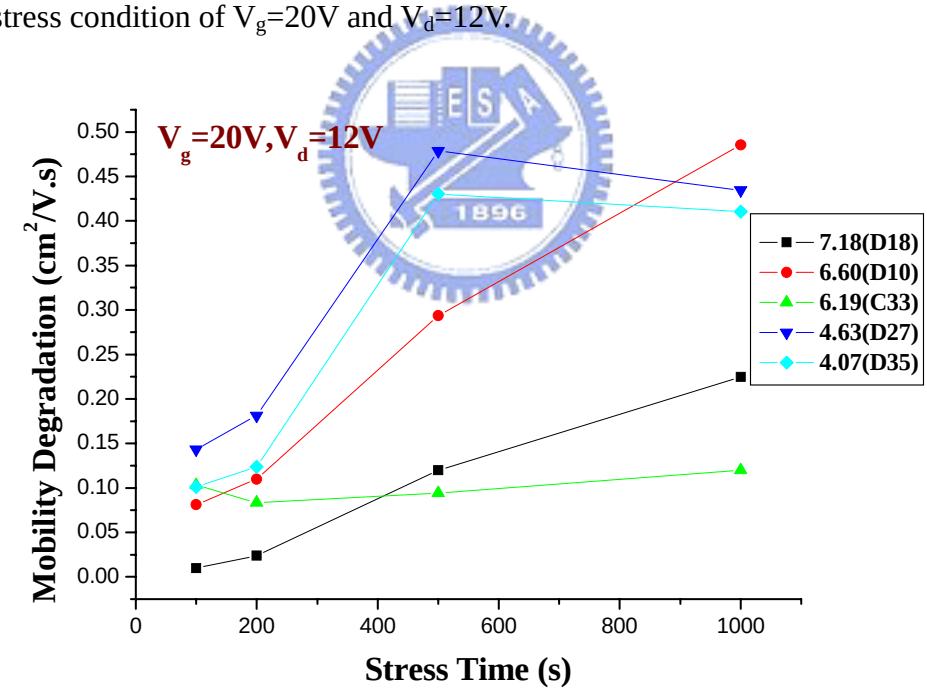


Fig. 3-38 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=12V.

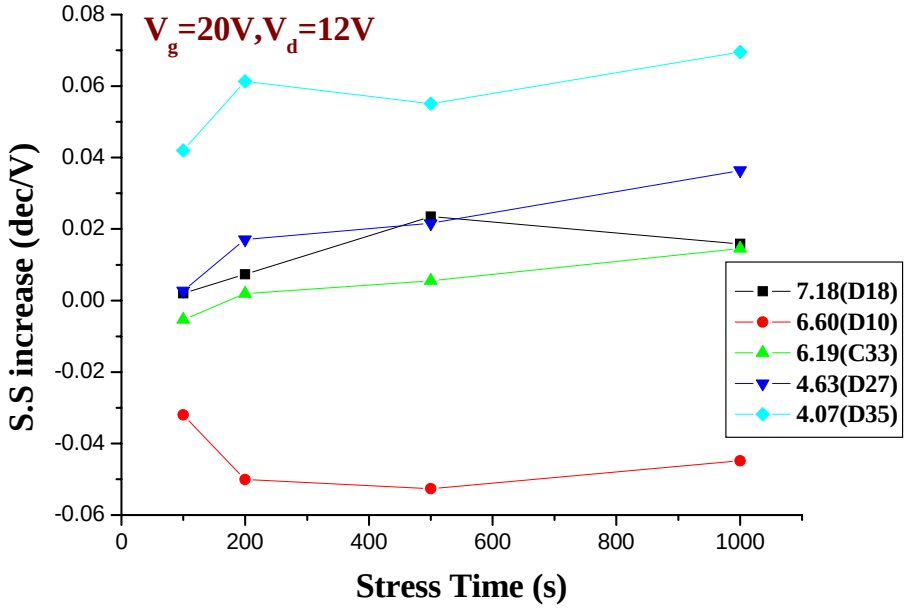


Fig. 3-39 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=12V.

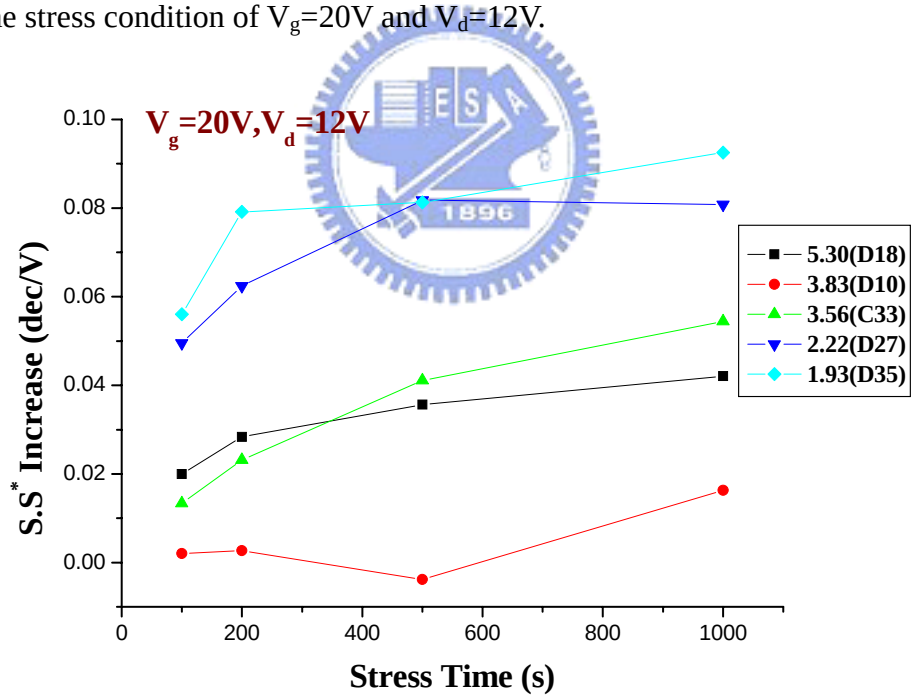


Fig. 3-40 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=12V.

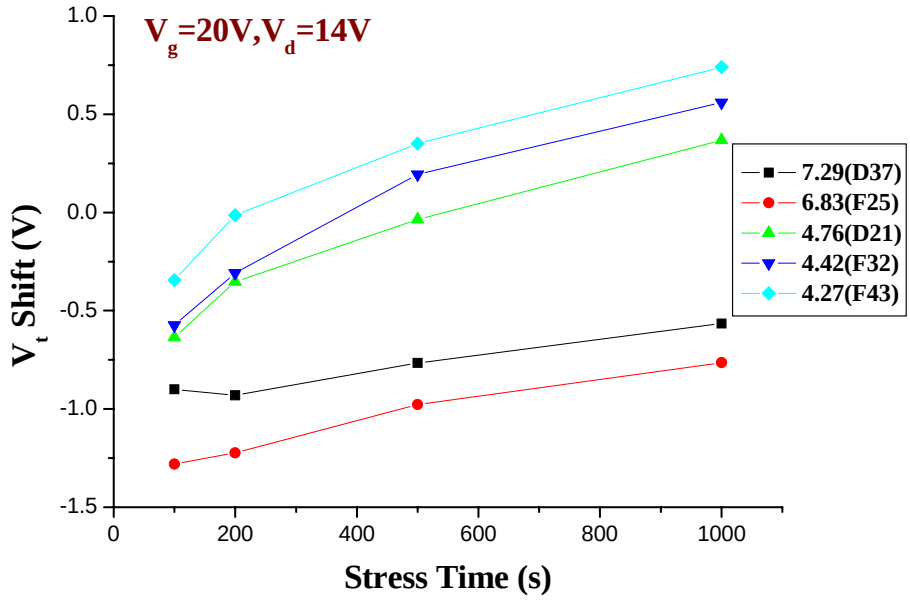


Fig. 3-41 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=14V.

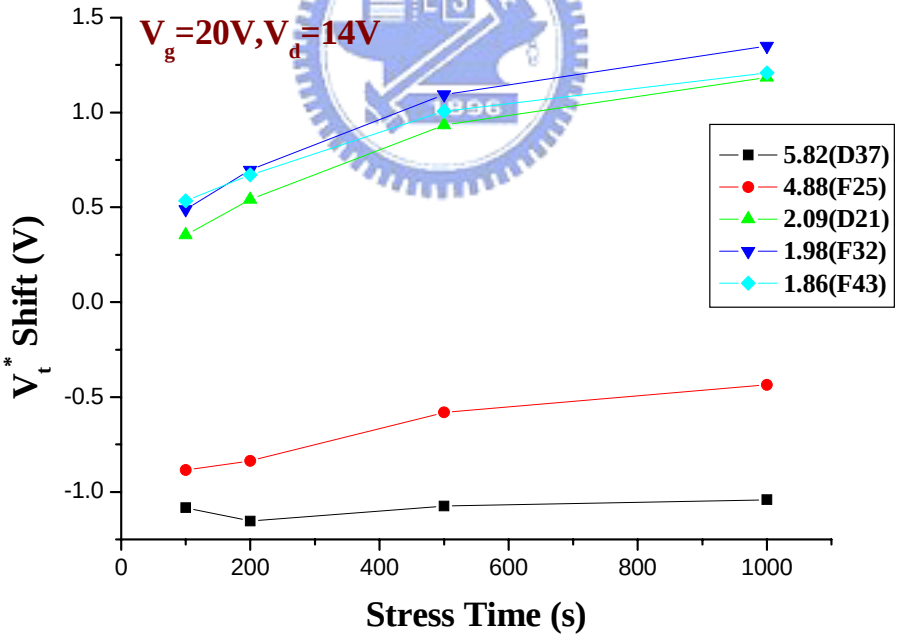


Fig. 3-42 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=14V.

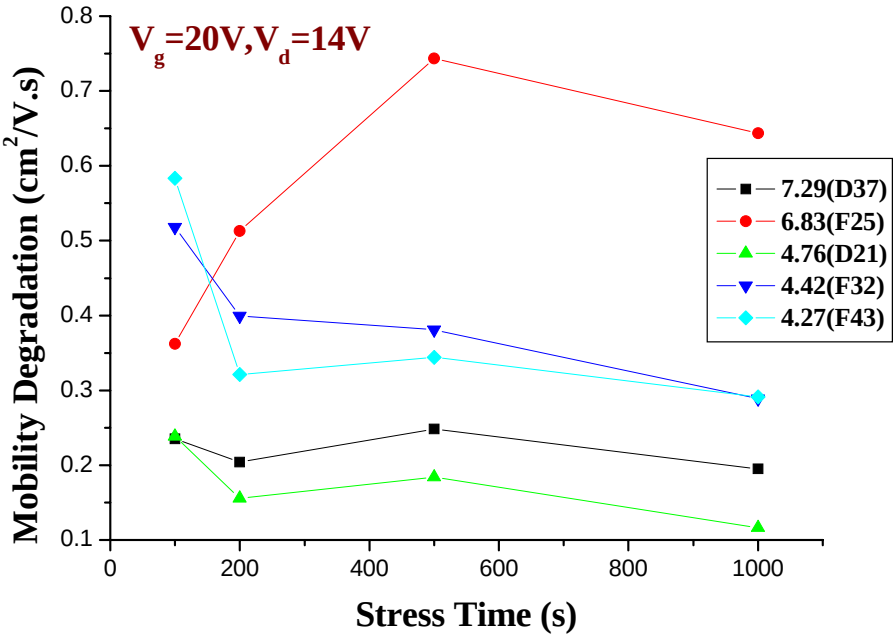


Fig. 3-43 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=14V.

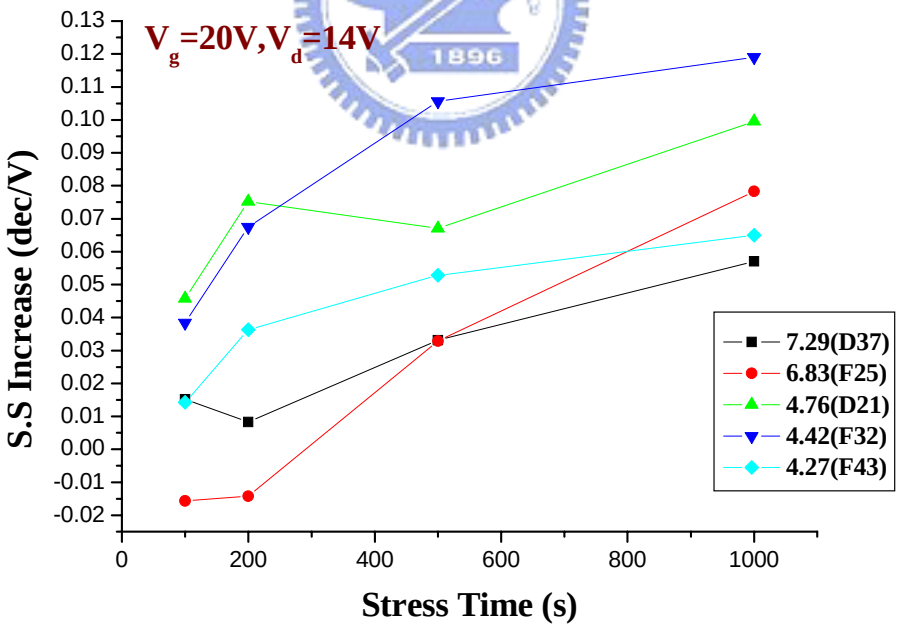


Fig. 3-44 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=14V.

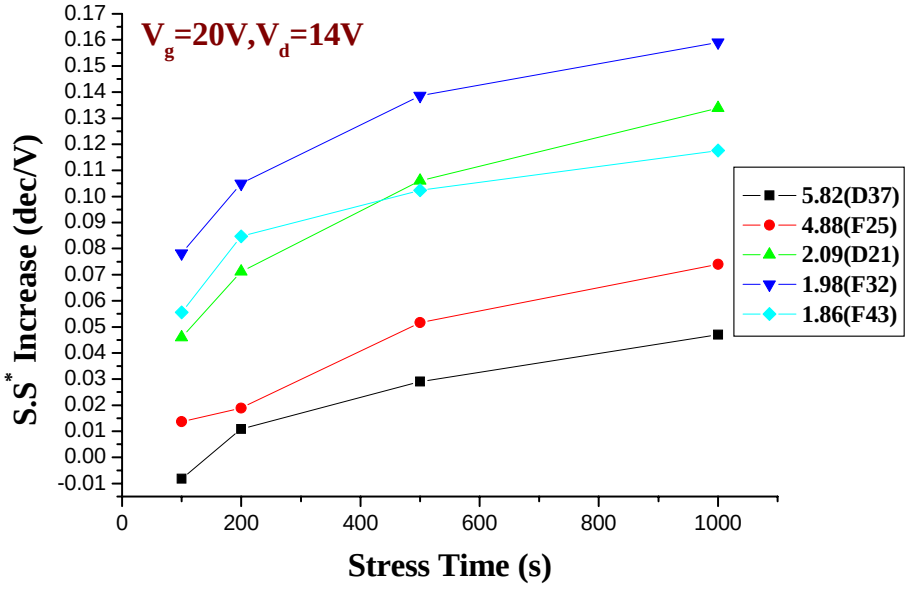


Fig. 3-45 Time dependence of S.S* increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=14V.

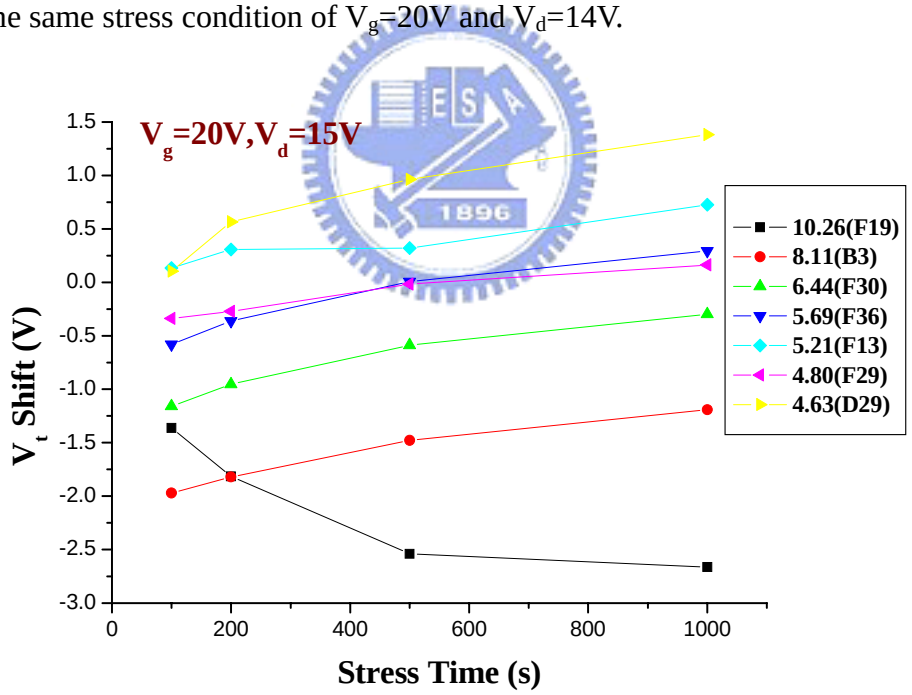


Fig. 3-46 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=15V.

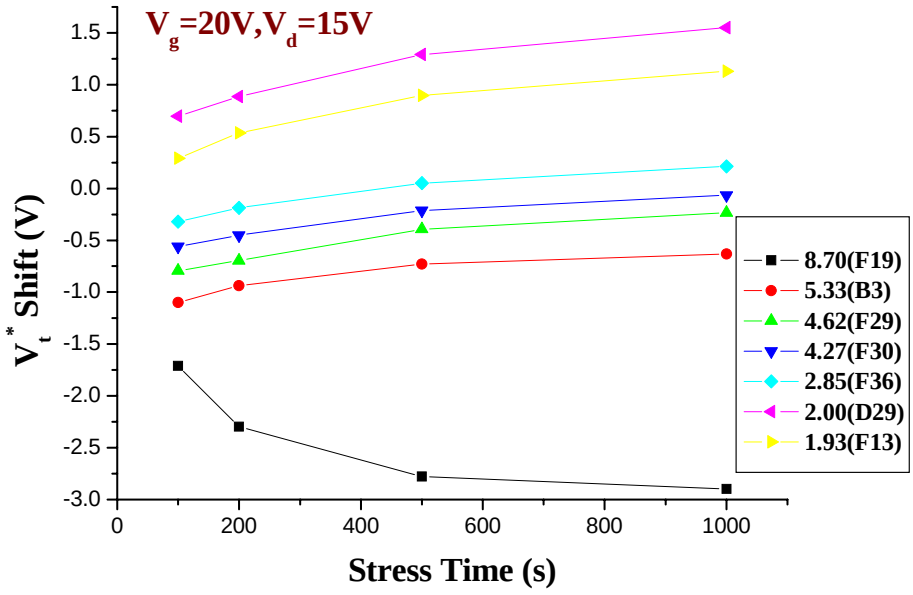


Fig. 3-47 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=15V.

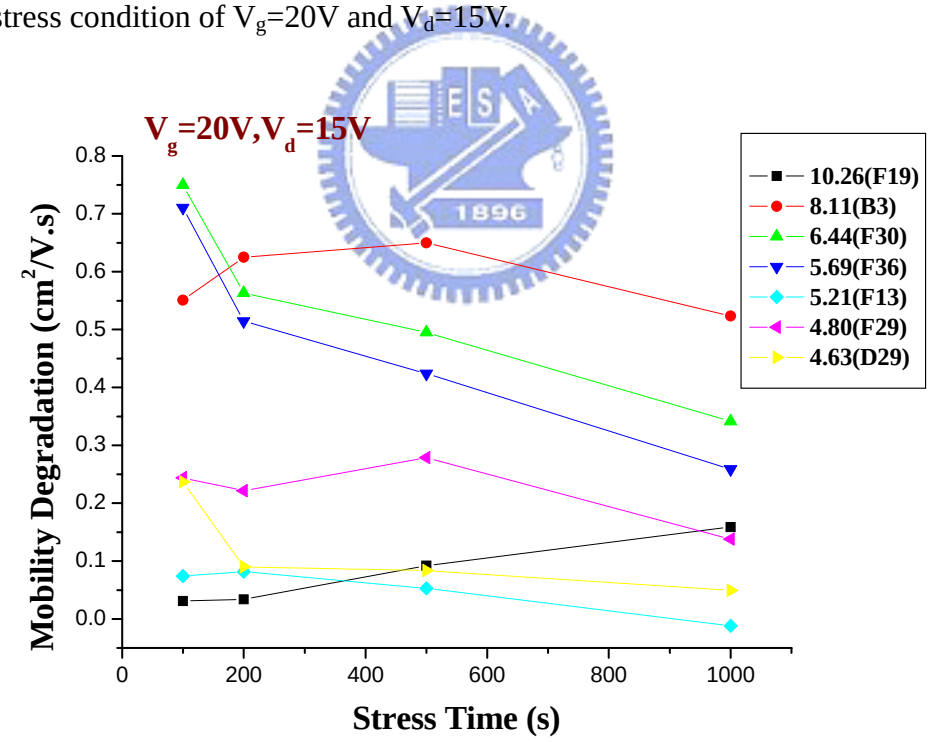


Fig. 3-48 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=15V.

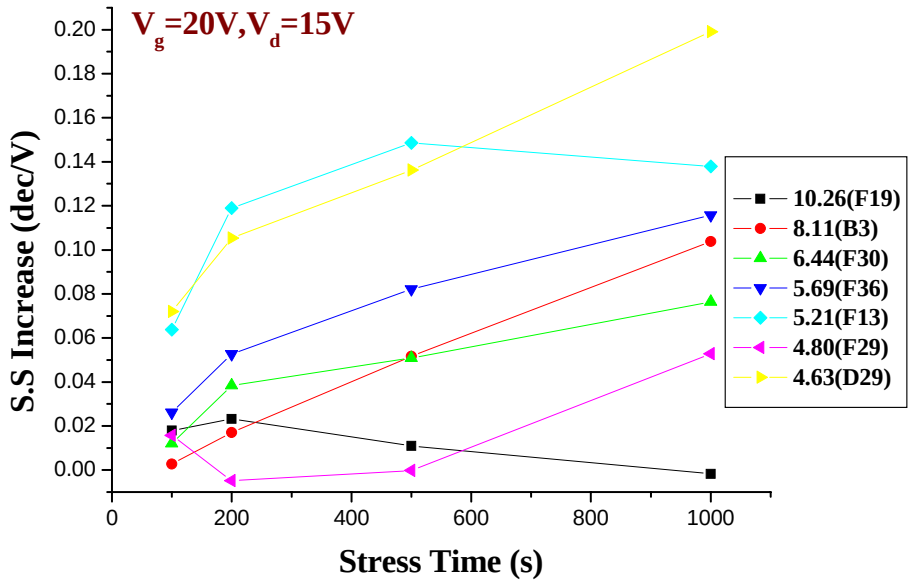


Fig. 3-49 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=15V.

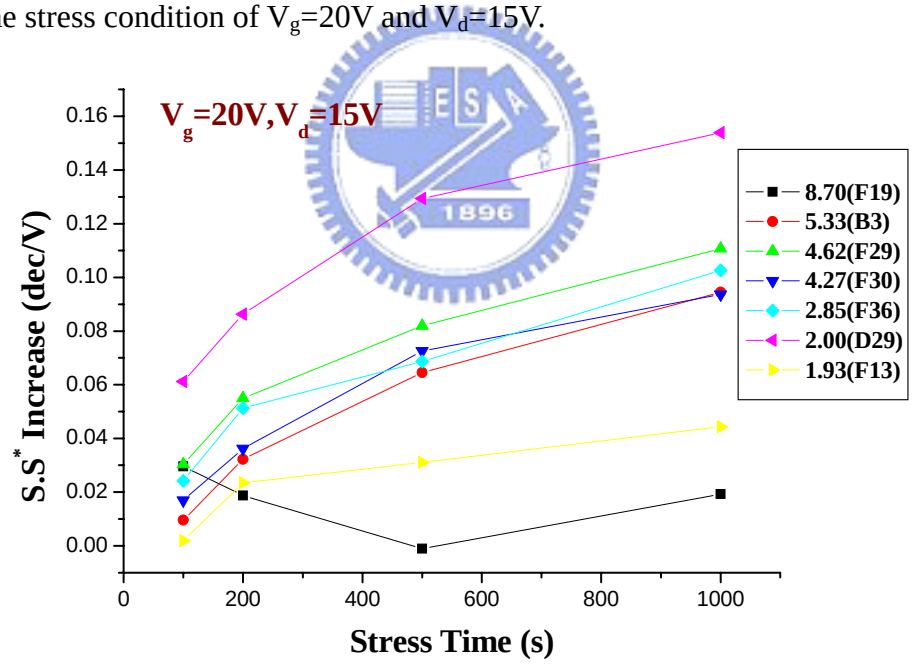


Fig. 3-50 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=15V.

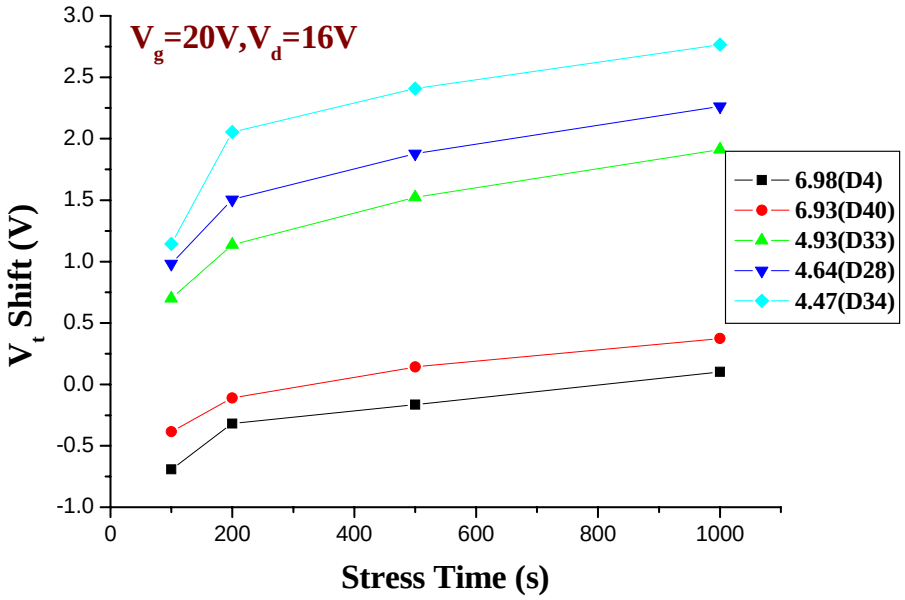


Fig. 3-51 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=16V.

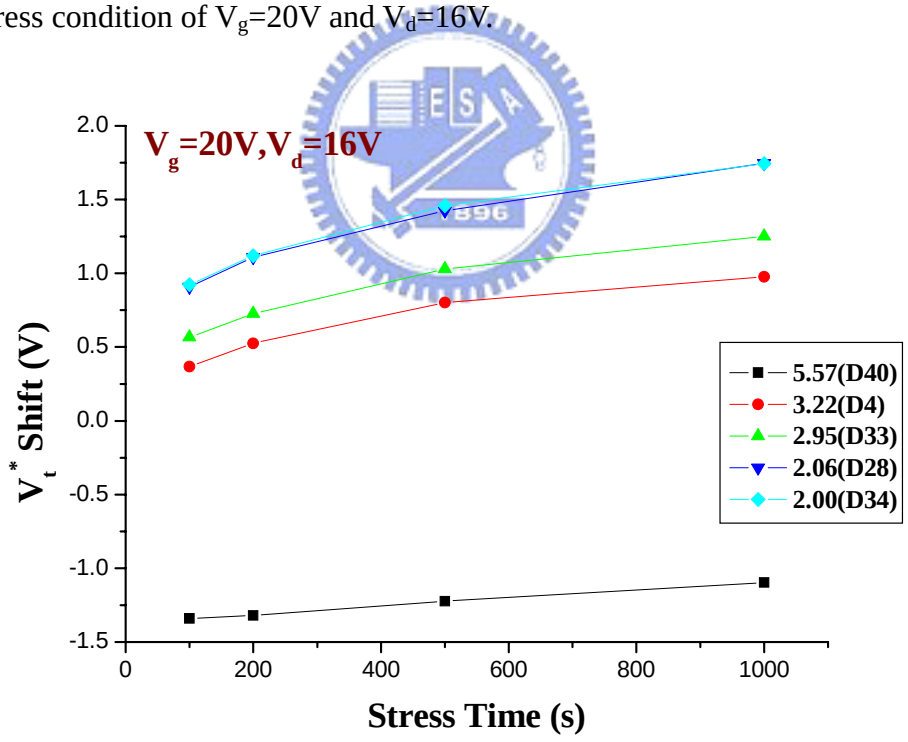


Fig. 3-52 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=16V.

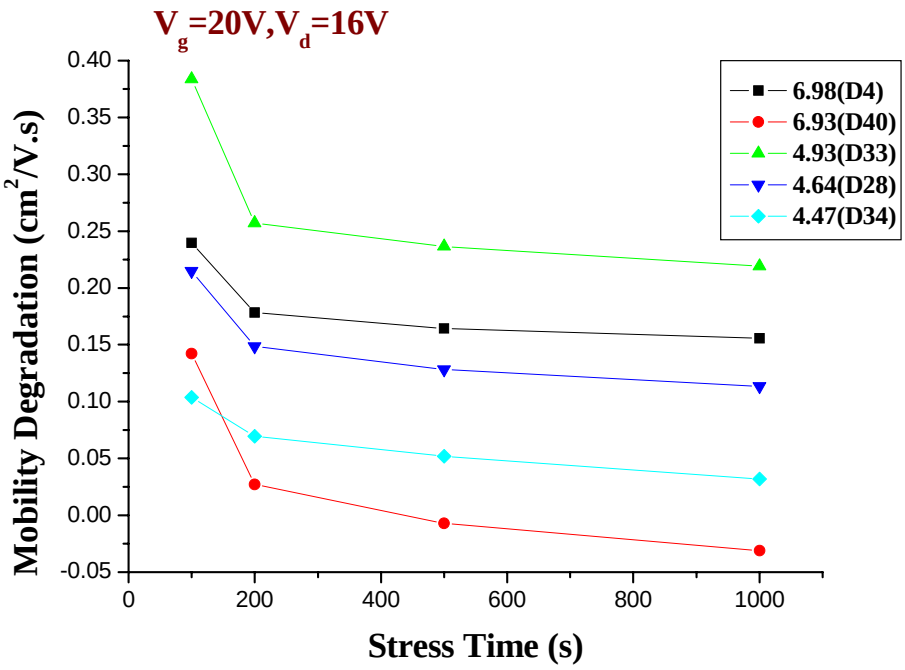


Fig. 3-53 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=16V.

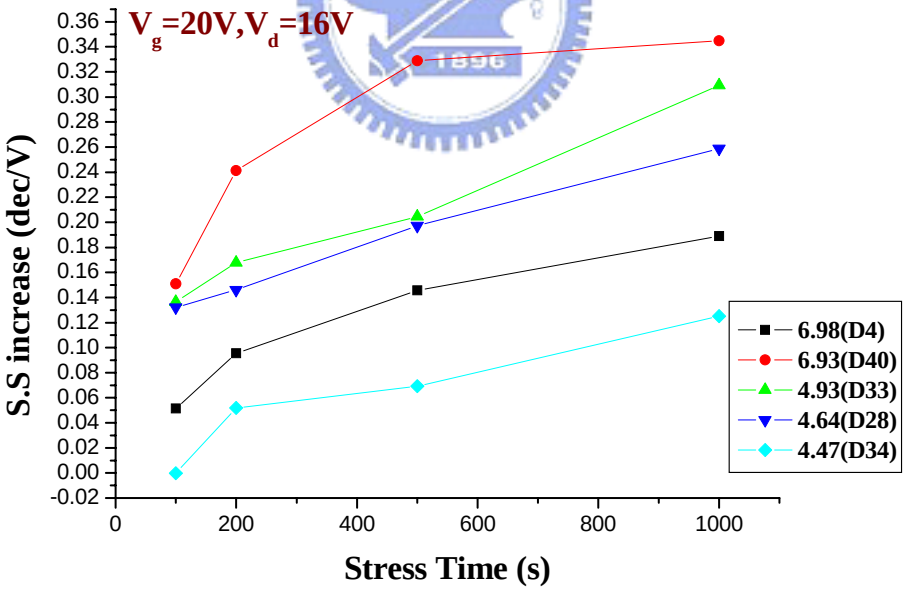


Fig. 3-54 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=16V.

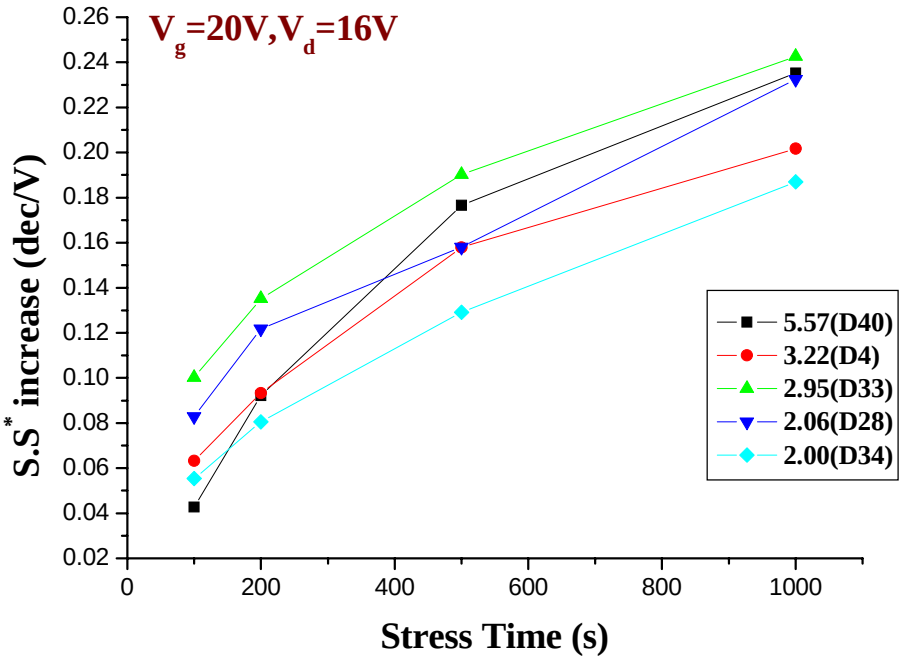


Fig. 3-55 Time dependence of S.S* increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=16V.

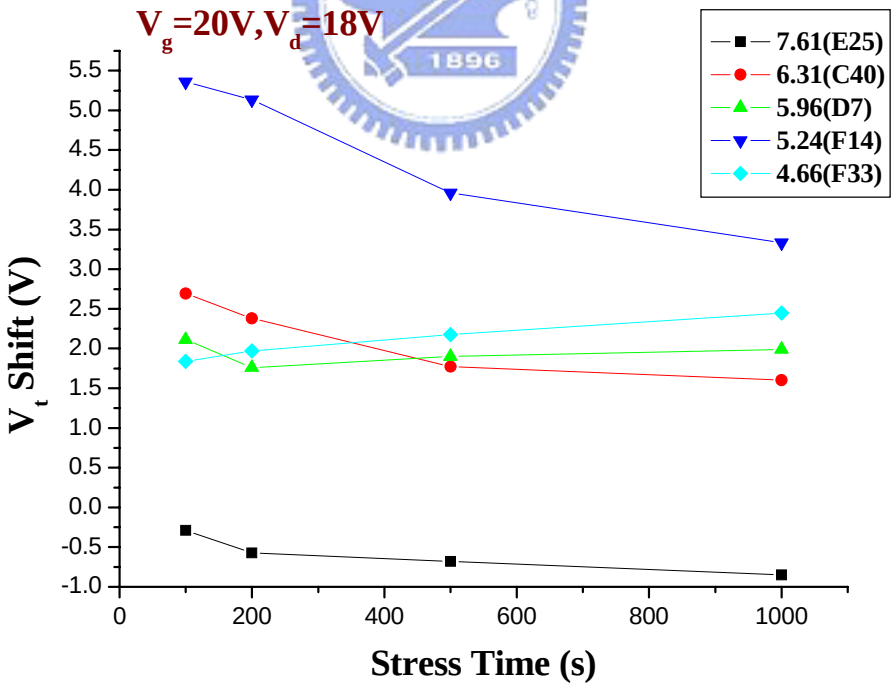


Fig. 3-56 Time dependence of V_t shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=18V.

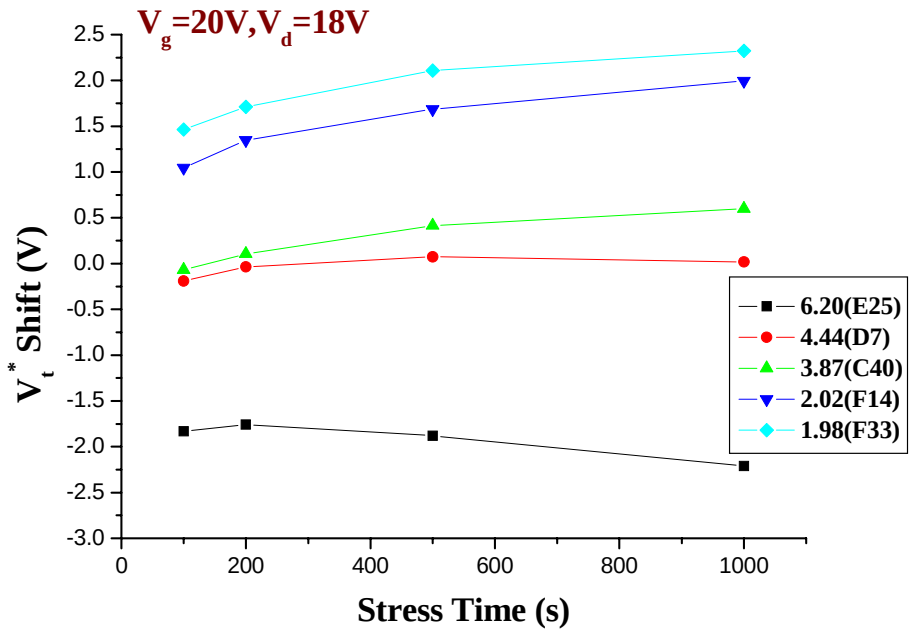


Fig. 3-57 Time dependence of V_t^* shift for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=18V.

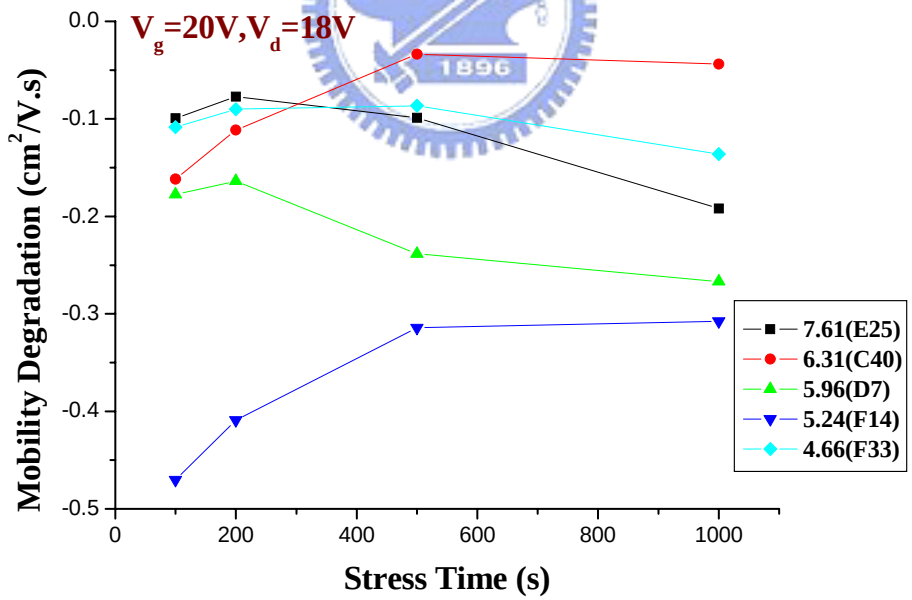


Fig. 3-58 Time dependence of mobility degradation for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=18V.

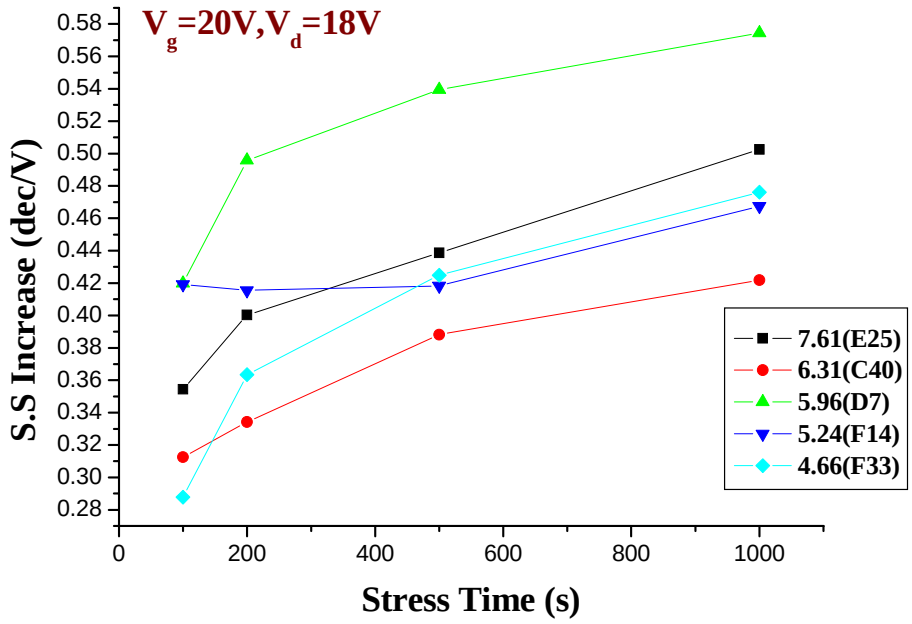


Fig. 3-59 Time dependence of S.S increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=18V.

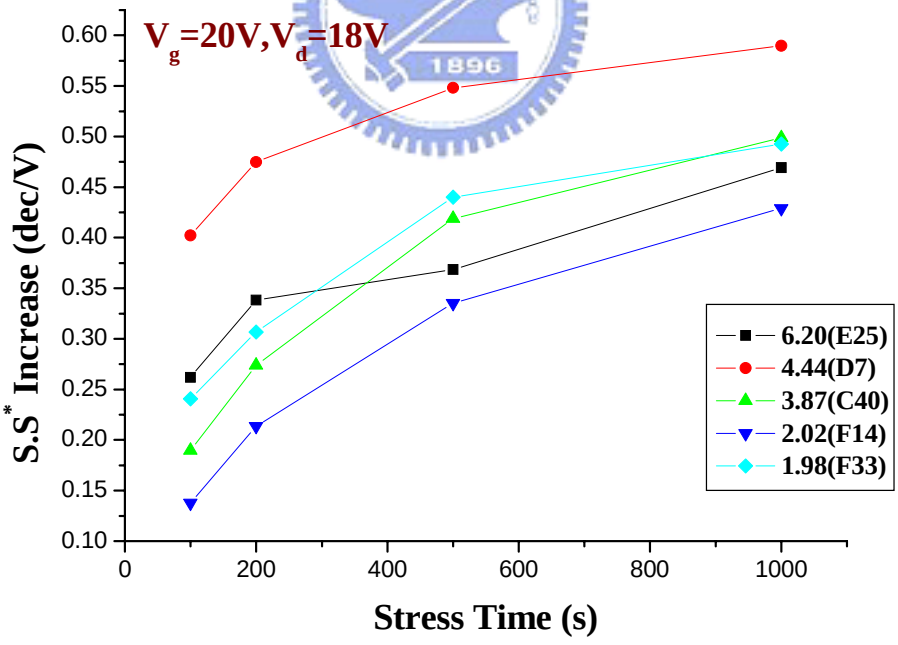


Fig. 3-60 Time dependence of $S.S^*$ increase for vary initial characteristic devices under the same stress condition of V_g=20V and V_d=18V.

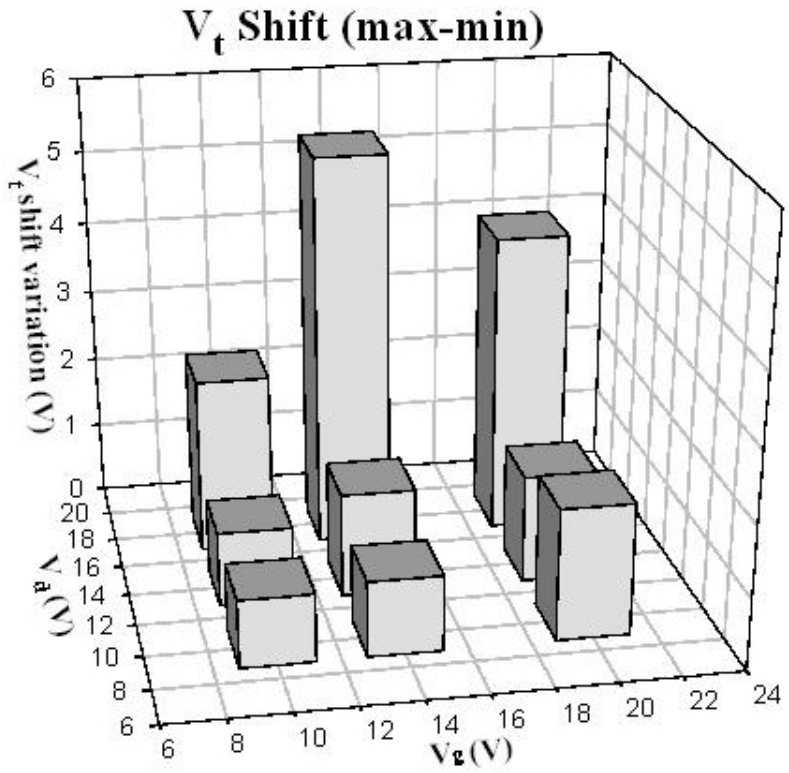


Fig. 3-61 The variation of V_t shift under different stress conditions.

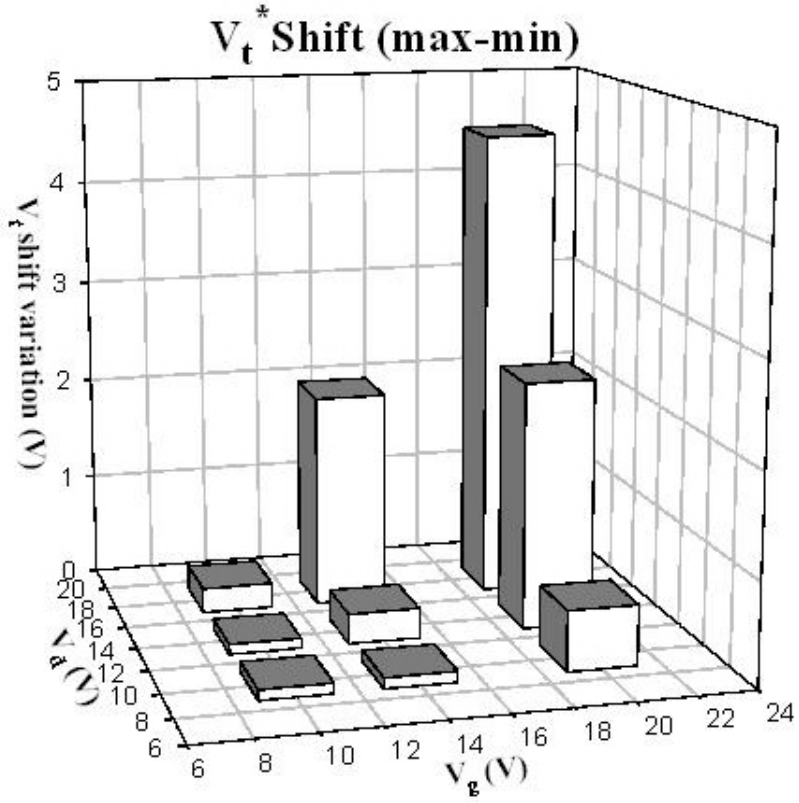


Fig. 3-62 The variation of V_t^* shift under different stress conditions.

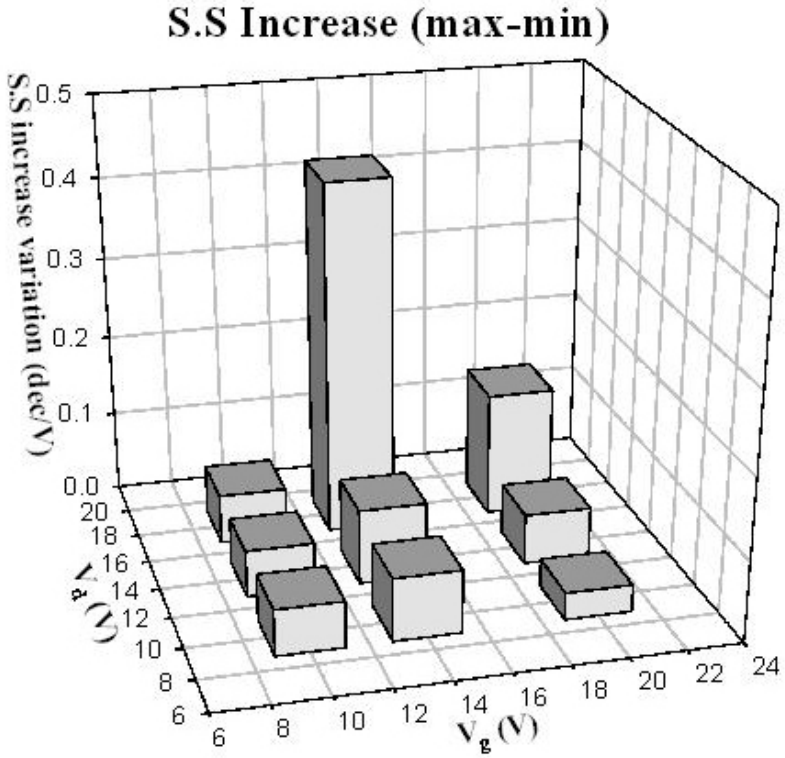


Fig. 3-63 The variation of S.S increase under different stress conditions.

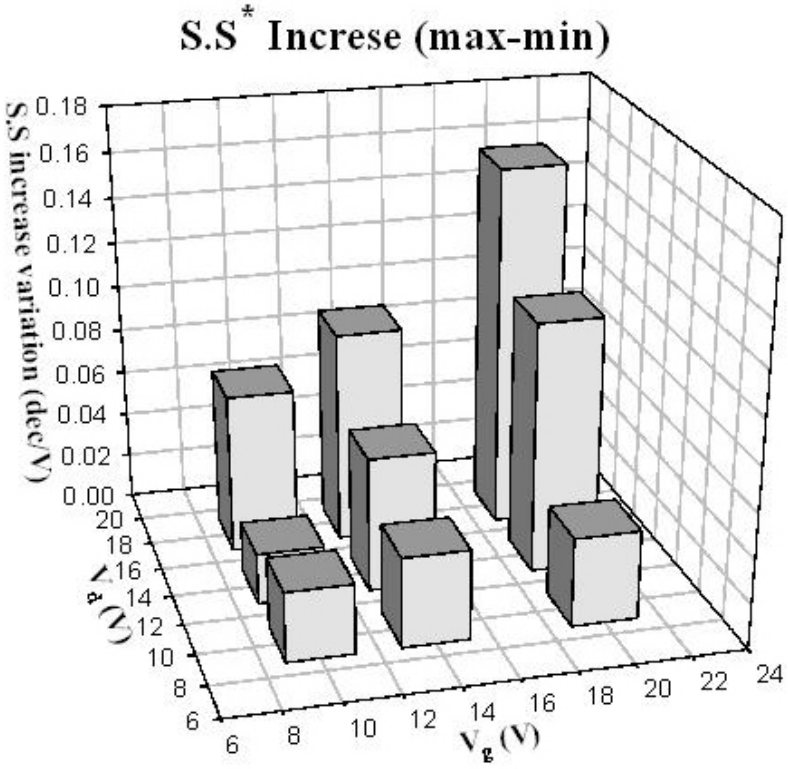


Fig. 3-64 The variation of S.S* increase under different stress conditions.

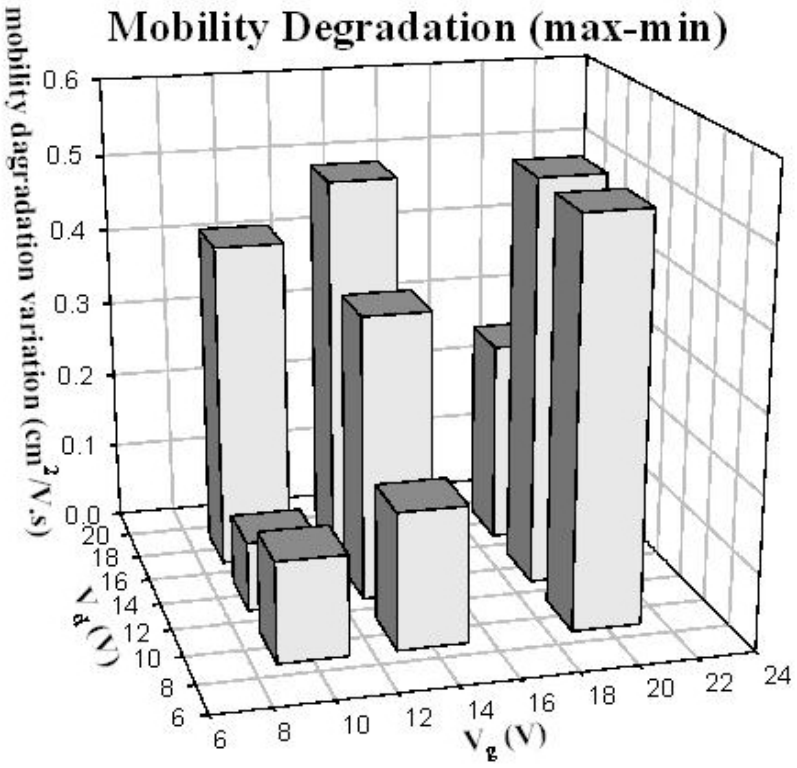


Fig. 3-65 The variation of mobility degradation under different stress conditions.

Chapter 4

Initial characteristic dependence

4-1. Experiment

As mentioned in chapter 2, we know the degradation phenomenon of devices is serious in region II and the region IV. In the experiment, we control different DC bias stress conditions applied to the nominally identical LTPS TFTs with channel width and length W/L=20μm/6μm for the stress time up to 1000s. Many electric characteristics of the TFTs were measured at the same condition.

4-2. Results and Discussion

Fig. 4-1 shows the dependence of the mobility ratio μ/μ_0 on different stress times under the varying bias stress conditions. For the bias stress conditions, V_d=20V was applied while the V_g was varied from 10V to 20V for 1000s. For the stress condition of V_g=10V and V_d=20V, the electric field near the drain side began to exhibit the hot carrier effect. Due to the TFTs with LDD structure, the electric field was subsequently suppressed and thus the degradation was not severe. For the condition of V_g=15V and V_d=20V, the lateral electric field became maximum [1],[2]. In such a string field the hot carrier stress was the most severe. Therefore, the degradation was the worst. Furthermore, the diversity of devices under the same bias stress condition can also be observed in Fig. 4-1. The conditions of V_g=12.5V with V_d=20V was chosen as the

bias stress conditions for further discussion.

As can be seen in Fig. 5, when the condition of V_g=17.5V, due to the high current effect, self-heating effect became observable and the degradation was severe. When the condition of V_g=17.5V, the standard deviation decreased and then increased. This phenomenon may be due to the fact that holes inject into the buffer oxide, causing the short-channel effect [3],[4]. As the stress times increase, the mobility ratio μ/μ_0 is increased. It is because when the stress time increase the TFTs devices were similar under the circumstance of “anneal”.

Fig. 4-2 shows the dependence of the mobility ratio μ/μ_0 on different stress times for the condition of V_g=12.5V and V_d=20V. It can be seen that devices degrade more seriously for the condition of V_g=12.5V with V_d=20V than those under the condition of V_g=10V with V_d=20V. Since the electric field was stronger than in the condition of V_g=10V and hot carrier effect became dominant, the degradation was more serious. Fig. 4-2 also indicates that variations in different devices were pronounced under this bias stress condition.

Fig. 4-4 presents the standard deviations among different devices under these bias stress conditions. When the condition of V_g=10V with V_d=20V, the standard deviation is relatively small. This is due to the small electric field near the drain side region that creates much fewer hot carriers compared to the case for other bias stress

conditions. Since the degradation is not severe, the corresponding variation is also small. For the condition of V_g=12.5V and V_d=20V, the standard deviation is the largest under the different stress times. This is because the weak Si-Si bonds in the grains and dangling bonds at the grain boundaries. Furthermore, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si film. These weak bonds can easily be broken under the device operation. For some circumstances, the carriers just get the energy which only can break the weak Si-H bonds and for some circumstances the carriers get the energy which can not break the weak Si-H bonds. As a result, for the condition of V_g=12.5V and V_d=20V, the standard deviation is the largest.

When the stressing V_g was increased to 15V, the hot carriers near the drain side obtained enough energy to break not only weak Si-Si and Si-H bonds but also strong ones at grain boundaries. Hence, the variation under this condition of V_g=15V was less than the condition of V_g=12.5V. As the stress time was increased, most bonds at grain boundaries were broken so that the standard deviation decreased.

Fig. 4-5 to Fig. 4-7 show the transfer characteristics of typical TFTs before and after the stress condition of V_g=12.5V and V_d=20V for stress times is 100s, 200s 500s and 1000s. The fig. 4-5 was the example of the serious situation and we defined it as the phenomenon A. The fig. 4-6 was the example of the situation and we defined it as

the phenomenon B. The fig. 4-7 was the example of the situation and we defined it as the phenomenon C. The phenomenon C can be observed as a combination of the phenomenon A with the phenomenon B.

3-3. Conclusion

The reliability and variation of n-channel LTPS TFTs under various bias stress conditions have been investigated in this paper. Such effects can be ascribed to the variations of the Si-Si dangling bonds under the medium hot carrier conditions due to the different grain structures. The discussion of variations in different bias stress conditions is inevitable for SOG applications.

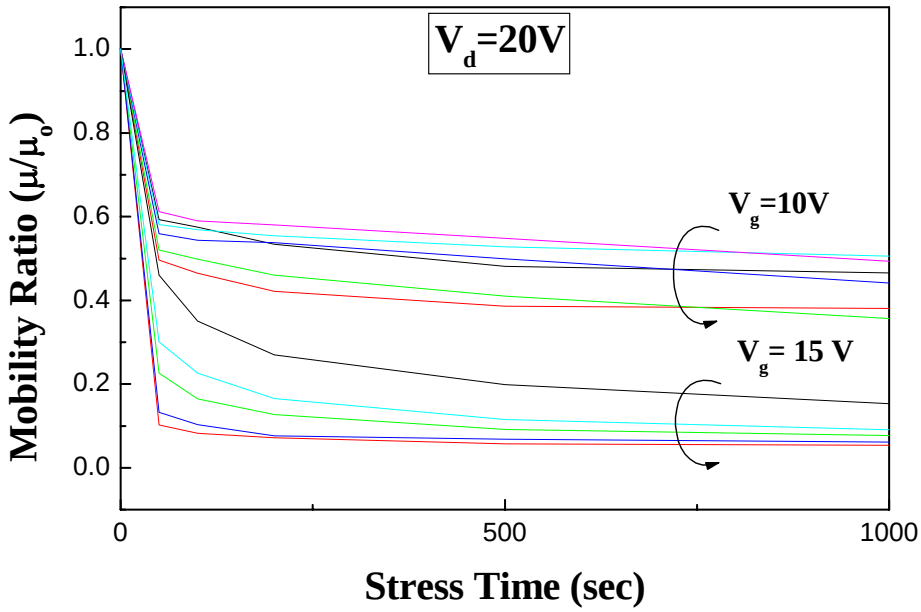


Fig. 4-1 Variations of the mobility ratio μ/μ_0 of different poly-Si TFTs stressed at the condition of V_d=20V when V_g=10V and V_g=15V.

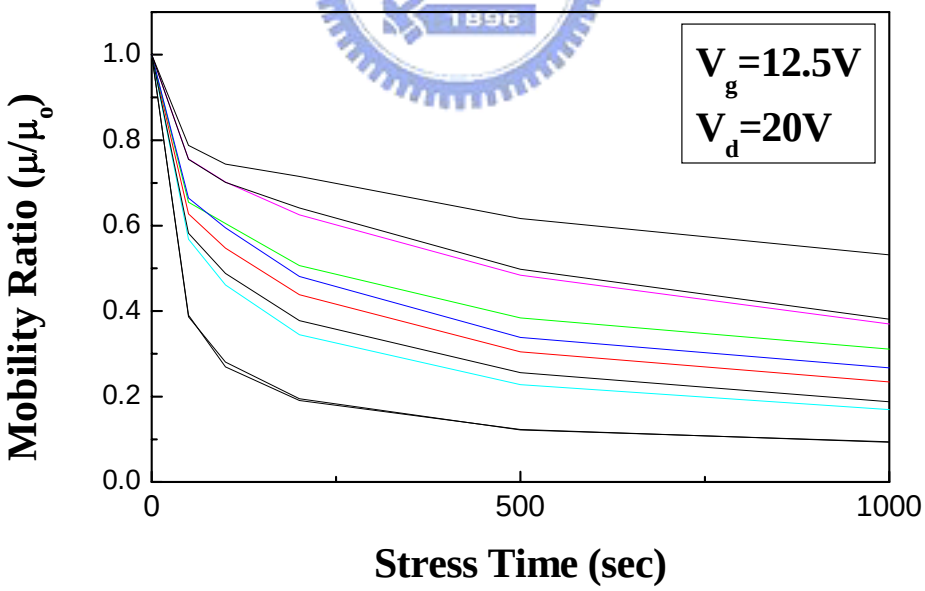


Fig. 4-2 Variations of the mobility ratio μ/μ_0 of different poly-Si TFTs stressed at the condition of V_d=20V and V_g=12.5V.

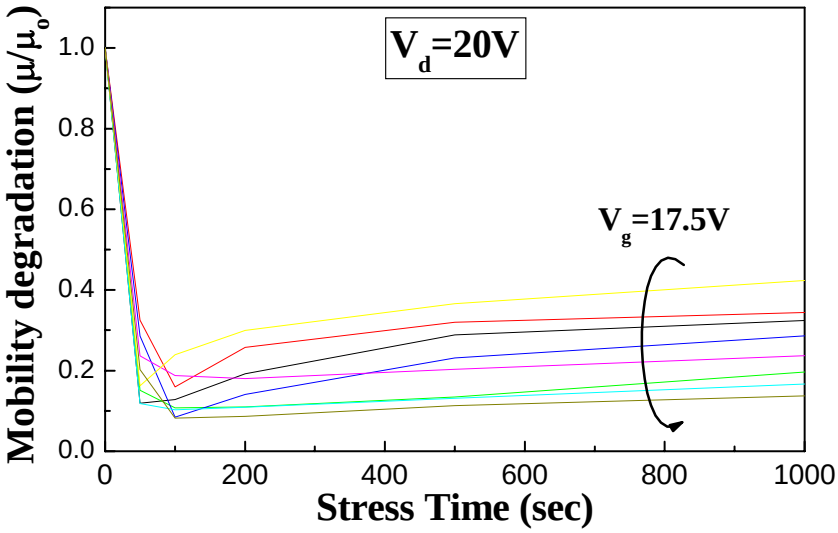


Fig. 4-3 Variations of the mobility ratio μ/μ_0 of different poly-Si TFTs stressed at the condition of V_d=20V and V_g=17.5V.

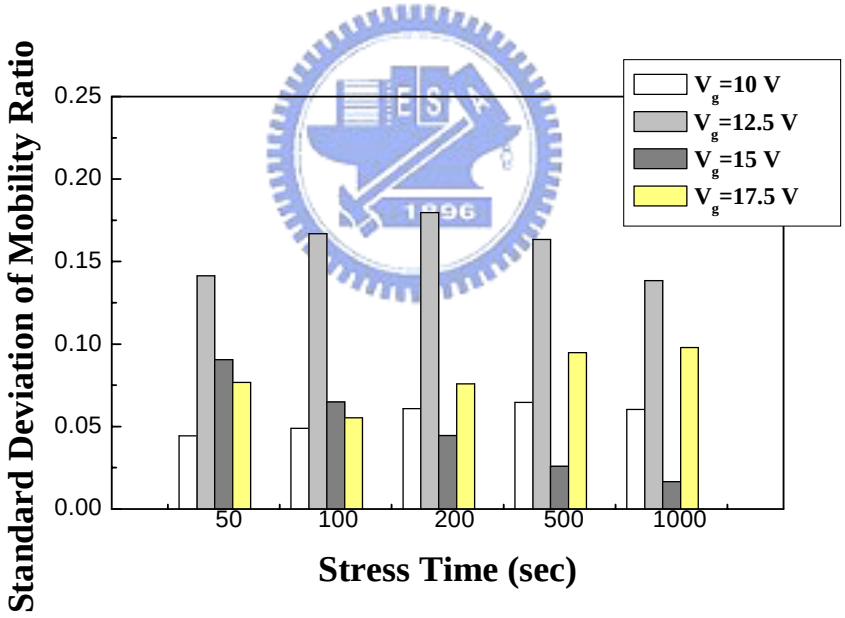


Fig. 4-4 Standard deviations of the mobility ratio of poly-Si TFTs under different stress conditions.

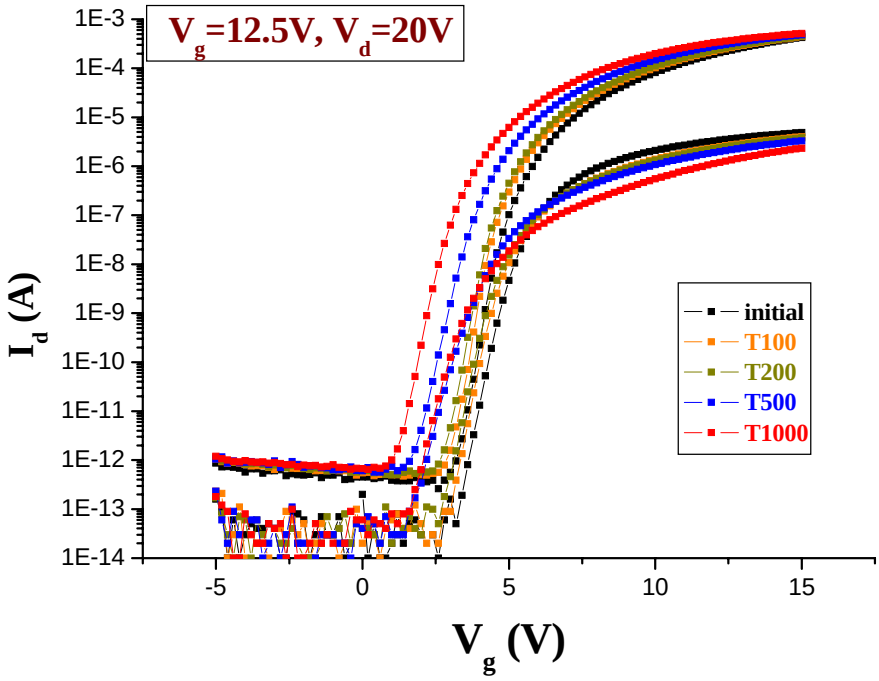


Fig. 4-5 Transfer characteristics of typical TFTs before and after the stress condition of V_g=12.5V and V_d=20V for stress times is 100s, 200s 500s and 1000s.

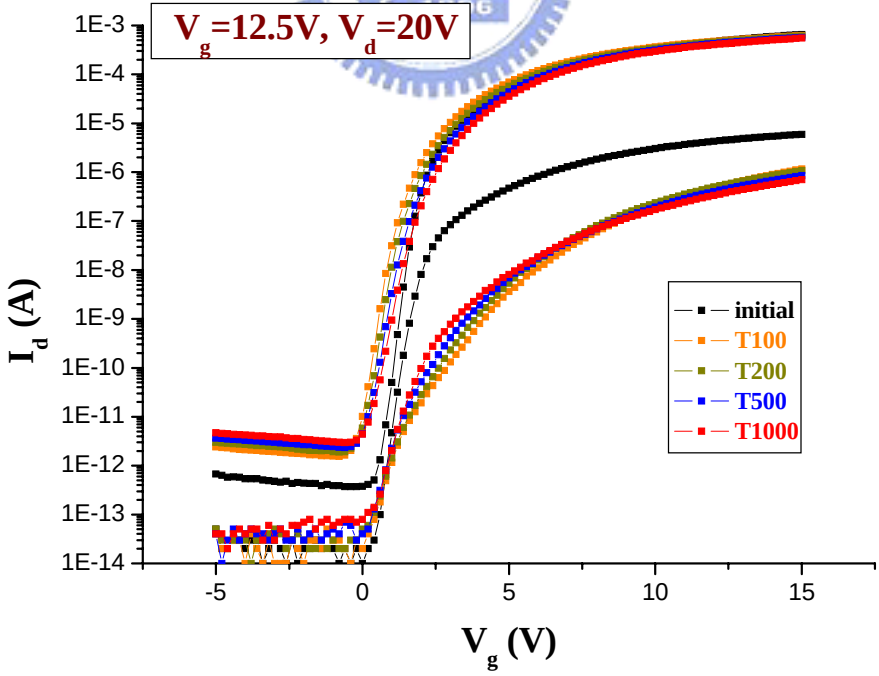


Fig. 4-6 Transfer characteristics of typical TFTs before and after the stress condition of V_g=12.5V and V_d=20V for stress times is 100s, 200s 500s and 1000s.

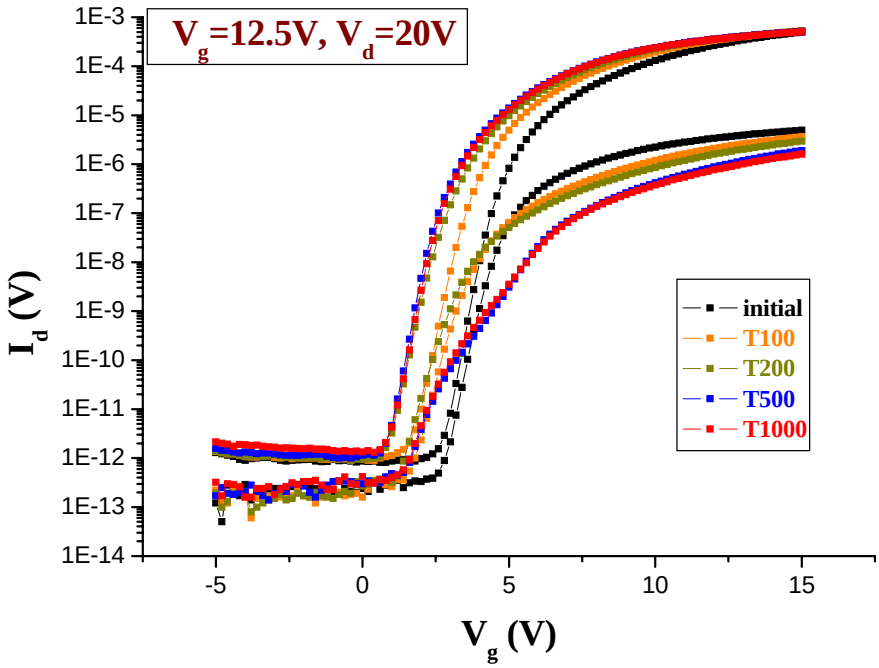


Fig. 4-7 Transfer characteristics of typical TFTs before and after the stress condition of V_g=12.5V and V_d=20V for stress times is 100s, 200s 500s and 1000s.

Chapter 5

Conclusion

The thesis studies the issues about the uniformity of low temperature poly-silicon (LTPS) thin film transistor (TFT) affecting on the device reliability. At firstly, devices fabricated by the identical process are used to establish the stress map of LTPS TFTs covering different DC bias stress conditions of gate and drain voltages for the stress time up to 1000s. The results are compared with the previous papers and some different phenomena which had never been seen before are observed. The special stress conditions with high gate voltages and medium drain voltages which have the distinguished unstable phenomena of mobility increase and negative threshold voltage shift are discovered. For the other stress conditions, the trend in our stress map is similar to the previous papers. The stress map can be divided into several regions and their corresponding degradation mechanisms are discussed. The unstable behaviors are very diverse in their tendencies and degree, indicating the difficulty in the device lifetime prediction. Finally, we demonstrate the device reliability variation in a special stress condition, which is at the boundary of regions for the hat carrier effect and the self-heating effect. In the special stress condition, we can observe distinct unstable behaviors can happen according to the initial device

characteristic because the main degradation mechanisms, including oxide trapping effect and hot carrier effect. Therefore, the degradation phenomena are sensitive to the initial device characteristic and become diverse. All of our results show that the device variation has great influence on the device reliability. The reliability database is helpful to the development of accurate device lifetime model.