Chapter 1

Introduction

1-1. Introduction to LTPS TFTs

Nowadays, the amorphous silicon thin film transistors (a-Si TFTs) are commonly used to be the switches of the pixel in active matrix liquid crystal displays (AMLCDs). Fig. 1-1 shows the block diagram of active matrix display. All the driver chips are buried together with the other application-specified ICs on PCB because the current driving capacity of a-Si TFTs is not good enough for the system integration. However, the integration of driver circuitry with display panel on the same substrate is very desirable not only to reduce the module cost but to improve the system reliability.

For this reason, the polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention because of their widely applications in AMLCDs and active matrix organic light-emitting diodes (AMOLEDs) due to its high electron mobility. In polysilicon film, the carrier mobility larger than 10 cm^2/Vs can be easily achieved, which is about tens times larger than that of the conventional amorphous-silicon TFTs (typically below 1 cm^2/Vs). This characteristic allows the pixel-switching elements made by smaller TFTs size, resulting in higher aperture ratio and lower parasitic gate line capacitance for the improvement of display performance. Furthermore, the integration of peripheral circuits in display electronics can be achieved by poly-Si TFTs due to its higher current driving capability, which is illustrated in Fig. 1-2. In addition to flat panel displays, poly-Si TFTs have also been applied into some memory devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), electrical programming read

only memories (EPROM), and electrical erasable programming read only memories (EEPROMs). Among the poly-Si technologies, low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) are primarily applied on glass substrates for the display electrons since higher process temperature may cause the substrate bent and twisted.

However, there are still some issues in LTPS TFTs such as reliability, device variation, and the speed limitation of device, etc. Our thesis will be focused on the device variation and its reliability.

1-2. Diverse reliability behaviors

The Fig. 1-3 and Fig. 1-4 show the variation of threshold voltage and mobility degradation under different stress conditions. These figures reveal that diverse degradation behaviors occur even under the same stress condition [1]. These degradation phenomenons are deeply affected by the initial parameters of the devices. In order to obtain the more consistent experimental results, the initial parameters of the devices should be more uniform and form the same glass substrate. The experiment for the reliability will be discussed in detail in chapter 4.

1-3. Device variation

The LTPS TFTs are found to suffer serious variation of their electrical parameters. The poly-Si material is a heterogeneous material made of very small crystals of silicon atoms in contact with each other constituting a solid phase material. These small crystals are called crystallites or grains. The irregular boundaries of these crystallites are the side lines of the grains. Because the material remains solid, the atoms at the border of a crystallite are also linked to the neighbor crystallite ones.

However, these atom bonds are disoriented in comparison with a perfect lattice of silicon. This border is called a grain boundary. As the result of various distributions of grain boundaries in the channel of TFTs, the initial characteristics of LTPS TFTs are different from one another, which are shown in Fig. 1-5. The Fig. 1-6 shows site variation of the threshold voltage variation for an LTPS TFT fabrication line plotted in the format of lot trend and the degree of variation can be up to four times of the standard deviation. These variations can be also observed in MOSFETs (Metal-Oxide-Silicon Field Effect Transistors) but they are more critical in LTPS TFTs due to the existence of grain boundary. The device variation will lead to the variation of the circuit performance. It will be reflected directly on the image uniformity of the display. For the circuit design in display, the device variation must be taken into consideration.

1-4. Motivation

The Poly-Si TFTs displays with integrated driving circuits have recently been developed. At present, the poly-Si TFT is the best candidate to realize the system on panel (SOP) and is widely considered for AMLCDs and active matrix organic light-emitting diodes (AMOLEDs). In previous research, it is shown that the LTPS TFTs have some non-ideal characteristics such as device variation and diverse reliability behaviors. Until to the present time, very few researches have been made on the variation issue of LTPS TFTs. Most researches about LTPS TFTs aim at the improvement of the device performance. However, before LTPS TFTs can be widely-applied in mass production, yield of the production should be evaluated firstly. The aggressive design strategy will get lower yield while conservative design strategy will underestimate the circuit performance. Consequently, the statistically study of

device variation in this thesis is for looking after both yield and circuit performance. It will be reported in the chapter 2 in detail.

The variation models and their applications for circuit performance will be demonstrated in chapter 2 and 3. The purpose of these studies is to establish reliable models to estimate precisely on the circuit performance influenced by the device variations. These models will improve the accuracy of the simulation result compared with other simulation models. Besides, another key factor for application, reliability of LTPS TFTs will be analyzed by means of stress mapping. We will get the more consistent reliability behaviors and the safe operation conditions for circuit in the chapter 4.

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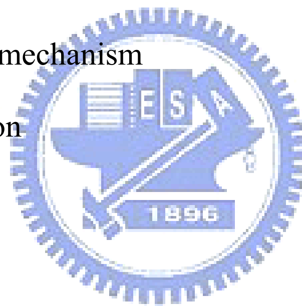


Chapter 2

Statistical analysis of crosstie TFT device parameters

2-1. Introduction to crosstie TFTs

In prior studies, it is known that LTPS TFTs suffered from severe device variation even under well-controlled process. Since the device variation is inevitable in LTPS TFTs, it is essential to classify the sources of variation. In MOSFETs (Metal-Oxide-Silicon Field Effect Transistors), the local variations can be characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances. If this distance is lower than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g. a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g. the gate oxide thickness across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other.

In order to investigate the relationship between uniformity issue and device distance, a special layout of the devices adopted in this work is shown in Fig 2-1. The red, blue and yellow regions respectively represent the polysilicon film, the gate metal and the source/drain metal. The structure of the poly-Si film and the gate metal are in the order that resembles the crosstie of the railroad and therefore this layout is called the crosstie type layout of LTPS TFTs. The distance of two nearest active regions is equally-spaced 40μm. The global variation may be ignored within this small distance,

and the variation of device behavior can therefore be reduced to only local variation. For this reason, we can find out the relationship between the variation behaviors and the distance of mutual devices by adopting the crosstie layout TFTs.

2-2. Device fabrication and parameter extraction

2-2-1. Device fabrication

Top gate LTPS TFTs with width/length dimension of 20μm / 5μm were fabricated using low temperature process. The process flow of fabricating LTPS TFTs is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates, and then XeCl excimer laser was used to crystallize the a-Si:H film, followed by poly-Si active area definition.

Subsequently, a gate insulator was deposited. Next, the metal gate formation and source/drain doping were performed. A lightly doped drain (LDD) structure was used on the devices. Dopant activation and hydrogenation were carried out after interlayer deposition. Finally, contact holes formation and metallization were performed to complete the fabrication work. The Fig. 2-2 shows the schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain (LDD).

2-2-2. Parameter extraction

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). The threshold voltage in the thesis is determined from this method, which extracts V_{th} from the gate voltage at the normalized drain current $I_N=I_D/(W_{eff}/L_{eff})=10nA$ for V_D=0.1V.

The field effect mobility (Mu, μ_{FE}) is derived from the transconductance g_m. The

transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si. The MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{th}) V_D - \frac{1}{2} V_D^2] \tag{2-1}$$

Where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller compared with $V_G - V_{th}$ (i.e. $V_D << V_G - V_{th}$), then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \tag{2-2}$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{2-3}$$

We can get the field-effect mobility by taking the maximum value of the g_m into (2-3) when $V_D = 0.1V$.

The subthreshold swing S.S (V/dec) is a typical parameter to describe the gate control toward channel. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. In our thesis, it is defined as the minimum value of the gate voltage required to increase drain current by one order of magnitude for $V_D = 0.1V$.

$$S.S = \left[\frac{\partial \left(\log I_{ds} \right)}{\partial V_{gs}} \right]^{-1} \tag{2-4}$$

2-3. Initial parameter distribution

Firstly, we introduce the statistical expressions for the following analysis. The average value μ is defined as

$$\overline{X} = \frac{\sum_{i=1}^{n} x}{n} \quad \text{Where } x \text{ is the observe value} \tag{2-5}$$

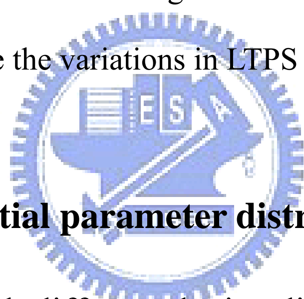
The standard deviation value, σ, is usually used to investigate the distribution of the observed value. The standard deviation value is given as

$$\sigma \equiv \sqrt{\frac{1}{n} \sum_{n} \left(x - \overline{X} \right)^2} \quad \text{Where } x \text{ is the observe value} \tag{2-6}$$

In order to obtain the more accurate parameter distributions of crosstie layout TFTs, large amount of device parameters are required. In this work, more than one thousand of devices were measured within 45μm on the glass substrate. Taking out the failure devices, there are 1009 devices taken into statistical analysis. The distributions of threshold voltage (V_{th}), mobility (Mu), and subthreshold swing (S.S) of measured devices are shown respectively in Fig. 2-3, Fig. 2-4, and Fig. 2-5. The average and standard deviation of V_{th} are 1.69 V and 0.03 V, and those of Mu and S.S are 59.66 cm^2 /Vs, 7.84 cm^2/Vs, 0.241 V/dec, and 0.0083 V/dec, accordingly.

These figures show the variation behaviors in different parameters of LTPS TFTs. For the distrubtion of Vth, it reveal the slight left-skewed property and the sharper peak compared with the Gaussian distribution. The distribution of Mu are apparently right-skewed and incisive in its peak. This phenomenon indicates that field effect mobility exhibits severe non-uniformity behavior compared with threshold voltage.

As for the distribution of S.S, it is similar to Gussian distribution. On the basis of our data, it can be predicted that the distribution of density of deep state in LTPS TFTs will follow the Gaussian distribution. Fig. 2-6 shows the simulation result of grain boundary number in the channel length direction, it can be possibly transfered under cretain transformation. Althought several studies have been made on the relationship between the grain boundaries in channel and threshold voltage and field effect mobility [2-4], there seems to be no well-established theory to explain. Let me take a look in Fig. 2-7, it indicates that the distributions of initial parameters vary with the different sites on glass and lot. If we want to find the variation behaviors with respect to the distance, it can not just classify them via these distributions. Another grouping method mentioned in the next section will get the more identical distributions, which will be more useful to evaluate the variations in LTPS TFTs.



2-4. The difference of initial parameter distribution

2-4-1. The distribution with different device distance

In order to identify the effects of the global and local variation, the parameters differences of two devices under certain distance are divided with several groups according to the distance between two devices. In prior studies [5], the averages of parameters differences stand for global variation of LTPS TFTs, while the standard deviation of parameter differences shows the local variation in the devices. In this thesis, we characterize the global variation and local variation as the variation in the range and micro variation for the analysis of LTPS TFTs, respectively. Fig. 2-8, Fig. 2-9, and Fig. 2-10 show the average and the standard deviation of the differences of V_{th}, Mu, and S.S. As the mutual device distance increases, the deviations of device differences are not changing with the device distance.

It can be explained that the micro variation will merely vary with distance as we expect. As for the variation in a range, these figures show the diverse results. In the difference of V_{th} and S.S, the averages are increasing with device distance. However, the average of the difference of Mu seems no significant trend when the distance of mutual devices is increasing. Although the averages of the differences of these parameters show different behaviors, they still appear in linear form. On the other hand, the effects of variation in a range are still minor than those of the micro variation under short device distance.

The variation in a range results from the issues of process control, such as gate insulator thickness, LDD length fluctuation and ion implantation uniformity. This non-uniformity of process control will lead to the common shift for device parameters. On the other hand, micro variation may come from the difference of the defect site, defect density in the active region and the activation efficiency. Since these conditions differ from device to device, the micro variation will lead to the random distribution of device parameters. For the circuit simulation, Monte Carlo method is generally adopted. However, the worst case simulation will be more suitable when the variation in a range of device is increasing.

Fig. 2-11 illustrates the threshold voltage distribution along the device position. We can take this graph as a part of Fig. 2-12, which is the same kind of graph but in longer distance. Analogy to the small signal analysis in the circuit theory, the variation in a range just likes the range near the bias point and appears in piecewise linear form, while the micro variation can be taken as the noise.

2-4-1. The models of distributions

Since we know the device variation behaviors by above statistical analysis, how

to apply these results to evaluate the effects of variation on circuit performance is a topic we are interested in. The variation in a long range is not our concern because the distance between two devices will not be too long for the layout of the same circuit. A good place to start is finding the proper mathematical expression for the distribution of the differences of these parameters. In the beginning, we take the coefficient of determination (R square) to evaluate the fitness of our work, which is defined as

$$r^2 = \frac{SSR}{SST} = 1 - \frac{SSE}{SST} \quad \text{, where}$$

$$SSR = \sum(\hat{y} - \bar{y})^2 = \sum \hat{Y}^2 = b_1^2 \sum X_1^2 + b_2^2 \sum X_2^2 + 2b_1 b_2 \sum X_1 X_2$$

$$SST = \sum(y - \bar{y})^2$$

$$SSE = \sum \hat{e}^2 = \sum(y_i - \hat{y}_i)^2$$

Generally speaking, the values of R square above 0.7 represnent the good fitness for the chosen funcion. For the distribution of the difference of V_{th}, Gaussian-Lorentzian cross product is apply to the fitting, which is

$$y = \frac{a}{\left(1 + d\left(\frac{x - b}{c}\right)^2\right) * \exp\left((1 - d) * \frac{1}{2}\left(\frac{x - b}{c}\right)^2\right)}$$

Where

a is the peak value of the distribution

b is the center of the distribution

c is fitting parameter related to the width of the distribution

d is fitting parameter varying from 0 to 1; 0 represent the pure Gaussain function while 1 is a pure Lorentzian distribution

As for the distribution of the difference of Mu, the Lorentzian distribution is apply to the fitting, which is

$$y=\frac{a}{1+\left(\frac{x-b}{c}\right)^{2}}$$

Where

a is the peak value of the distribution

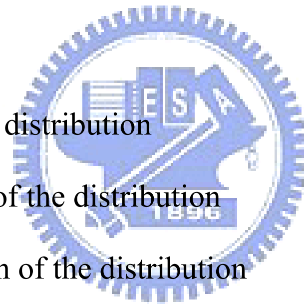
b is the center of the distribution

c is fitting parameter related to the width of the distribution

As mentioned above, the distribution of S.S follows the Gaussian distribution. Similarly, the Gaussian function is a good choice to fit the distribution of the difference of S.S, which can be expressed as

$$y=\frac{a}{\exp(\frac{1}{2}(\frac{x-b}{c})^{2})}$$

Where



a is the peak value of the distribution

b is the center (average) of the distribution

c is the standard deviation of the distribution

We polt the fitting results with different device distance in Fig. 2-13 (a) ~ (f), Fig. 2-14 (a) ~ (f), and Fig. 2-15 (a) ~ (f) for the distributions of the differences of V_{th}, Mu, and S.S, respectively. The values of R squre of the above fittng curves both higher than 0.95. It clearly shows the good fitness of our proposed mathemtical model. The fitting parameters show in Fig. 2-16 (a) (b) , Fig. 2-17, and Fig 2-18. Most of the fitting parameters slightly changing with distance supports the effects of the variation in the range are minor than those of micro variation we mentioned before. However, we still have to notice that micro variation increasing rapidly with distance and saturate about the device distance of 2000 μm. Since we establish the mathematical models for the distributions of the parameters differences, the applications for these models for circuit simulation will be discussed in the following chapter.

Chapter 3

Effects of device distribution on circuit performance

3-1. Introduction to the differential pair

In the integrated circuit application, coupling effect is a serious problem for signal transmission. Fig. 3-1 (a) shows that clock will couple some noise to adjacent signal line during the rising and falling time. If we transmit the difference of signal by two separated signal lines shown in Fig. 3-1 (b), the coupling effect of clock will be cancelled by getting the difference of the signal. For this reason, the differential pairs are widely used for analog circuit design because of the immunity for the noise. For the display applications, the differential pairs are commonly used in every block of display electronics such as the input stage of OP amplifier, driving circuit and so on. Fig. 3-2 shows the basic differential pair structure, where R_D is resistive load and Rss represents the output impedance of current bias; differential signals are applied to the gate terminal of transistor M1 and M2.

The quality of data transmission will benefit by differential signal. However, the device mismatch is a serious problem to differential pair. The mismatch of V_{th} and mobility will cause severe variation of circuit performance such as the variation of common mode reject ratio (CMRR) due to the imbalance current. In conventional CMOS, these mismatch effects can be suppressed under the well-controlled process. When compared to CMOS, LTPS TFTs suffered form more serious device variations. In order to evaluate the circuit performance of differential pair done by LTPS TFTs, the variation models we mentioned before can be adopted to simulate the circuit performance. The detail of circuit simulation and the comparison of other simulation

skills and models will be discussed in the next section.

3-2. Evaluation of the circuit performance with proposed models and other simulation skills

In this section, we use a commonly-used differential pair configuration, which maybe the simplest function block, to examine the circuit performance affected by device variation. The simulation will done by different simulation skill and model.

Now we divide the operation of differential pair into two operation mode. For the common mode, the two input terminals are connected to the same voltage, while the differential mode is that the two input terminals are connected to the two signals of different voltage. The mismatch of resistive load R_D will be ignored and set to identical value in following discussion because the influence of R_D mismatch is usually less than the transistor mismatch [6]. For common mode analysis, the circuit appears in Fig. 3-3. The transconductance g_m of M1 and M2 can be expressed as

$$g_{m1} = \mu_1 C_{ox} \frac{W}{L}(V_{GS} - V_{th1}) \ ; \ g_{m2} = \mu_2 C_{ox} \frac{W}{L}(V_{GS} - V_{th2}) \qquad (3\text{-}1)$$

Where

μ is field effective mobility

C_{ox} is the gate oxide capacitance per unit area

V_{th} is the threshold voltage

Let us calculate the small signal current runs through M1 and M2. Then, we will get the voltage of node p, which are

$$i_{d1} = g_{m1}(Vin,cm - Vp)$$
$$i_{d2} = g_{m2}(Vin,cm - Vp)$$
$$\Rightarrow (g_{m1} + g_{m2})(Vin,cm - Vp)Rss = Vp$$

$$Vp = \frac{(g_{m1} + g_{m2})Rss}{(g_{m1} + g_{m2})Rss + 1} Vin,cm$$

$$Vx = -g_{m1}(Vin,cm - Vp)R_D = \frac{-g_{m1}}{(g_{m1} + g_{m2})Rss + 1} R_D Vin,cm$$

$$Vy = -g_{m1}(Vin,cm - Vp)R_D = \frac{-g_{m2}}{(g_{m1} + g_{m2})Rss + 1} R_D Vin,cm$$

$$Vx - Vy = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})Rss + 1} R_D Vin,cm$$

$$\Rightarrow A_{cm-dm} = -\frac{\Delta g_m}{(g_{m1} + g_{m2})Rss + 1} \quad ; \quad \Delta g_m = g_{m1} - g_{m2} \qquad (3-2)$$

The common mode to differential mode gain (A_{cm-dm}) can be derived by (3-2).

As for the differential mode analysis, the superposition principle is used to solve the differential mode gain (A_{dm}). Fig. 3-4 (a) and (b) shows the equivalent circuit for turning off Vin1 and Vin2, respectively. The value of A_{dm} can be derived by following calculation :

Vin1 on, Vin2 off

$$Vx = \frac{-R_D}{\frac{1}{g_{m1}} + \left(\frac{1}{g_{m2}} // Rss\right)} Vin1$$

$$Vy = \frac{g_{m1} g_{m2} R_D Rss}{(g_{m1} + g_{m2})Rss + 1} Vin1$$

$$\Rightarrow (Vx\text{-}Vy)\Big|_{Vin1} = \frac{-2g_{m1}g_{m2}R_D Rss - g_{m2}R_D}{(g_{m1} + g_{m2})Rss + 1} Vin1$$

for Vin1 off, Vin1 on

Using Thevenin's Theorem, $V_T = V_{in2}$; $R_T = \frac{1}{g_{m1}}$

$$\Rightarrow (Vx\text{-}Vy)\Big|_{Vin2} = \frac{2g_{m1}g_{m2}R_D Rss + g_{m1}R_D}{(g_{m1} + g_{m2})Rss + 1} Vin2$$

by using superpositon and $Vin1 = -Vin2$, we get

$$(Vx\text{-}Vy)\Big|_{total} = \frac{-4g_{m1}g_{m2}R_D Rss - g_{m1}R_D - g_{m2}R_D}{(g_{m1} + g_{m2})Rss + 1} Vin1$$

Finally, the differential mode gain will be expressed as

$$\left|A_{dm}\right| = \frac{Vx\text{-}Vy}{Vin1\text{-}Vin2} = \frac{Vx\text{-}Vy}{2Vin1} = \frac{R_D}{2}\frac{4g_{m1}g_{m2}R_DRss + g_{m1}R_D + g_{m2}R_D}{(g_{m1} + g_{m2})Rss + 1} \qquad (3\text{-}3)$$

Since the advantage of differential signal is for its good immunity to the noise, a specification to evaluate this characteristic is needed. The common mode rejection ratio is a common index for the capability of differential pair against the common mode noise, which can be written as

$$CMRR = \left|\frac{A_{dm}}{A_{cm\text{-}dm}}\right|$$

(3-4)

By substituting (3-2) and (3-3) into (3-4), we can get

$$CMRR = \left|\frac{A_{dm}}{A_{cm\text{-}dm}}\right| = \frac{4g_{m1}g_{m2}R_DRss + g_{m1}R_D + g_{m2}R}{2\Delta g_m}$$

$$\cong \frac{g_m}{\Delta g_m}(1 + 2g_mRss)$$

$$,which \quad g_m = {(g_{m1} + g_{m2})}/{2}$$

$$\Delta g_m = C_{ox}\frac{W}{L}[\mu(V_{GS}\text{-}V_{th}) - (\mu+\Delta\mu)(V_{GS} - (V_{th}+\Delta V_{th}))]$$

$$=C_{ox}\frac{W}{L}[\mu\Delta V_{th} - \Delta\mu(V_{GS}\text{-}V_{th})+\Delta\mu\,\Delta V_{th}]$$

$\Delta\mu\,\Delta V_{th}$ can be ignored becuse this term is relative smaller than other term

$$\Rightarrow CMRR = \frac{\mu(V_{GS}\text{-}V_{th}) + 2\mu^2C_{ox}\frac{W}{L}(V_{GS}\text{-}V_{th})^2Rss}{\mu\Delta V_{th} + \Delta\mu(V_{GS}\text{-}V_{th})} \qquad (3-5)$$

In our thesis, we take the CMRR value for our simulation target to exam the accuracy of each simulation skill and model. In (3-5), the ΔV_{th} and $\Delta\mu$ terms represent the differences of threshold voltage and mobility.

Before the simulation, it is essential to transform the distribution into the corresponding value for Monte Carlo simulation. For example, the Fig. 3-5 is a simple distribution with four variables. The random values from 0 ~ 1 are uniformly generated by computer and the transformed values can be obtained according to the Fig. 3-6. If we get 0.3 from computer, the variable B will be chosen according to Fig.

3-6. In the light of statistics thoery, a certain number of data for each distribution will be generated in order to get the stable and reliable simulation result. In this work, 210,000 times of data transformation for each distribution were executed to obtain the best and stable result for the Monte Carlo simulation.

The following is to determine the parameters for simulation. In (3-5), we set the V_{GS} to 5V, which is the voltage at the quiescent point. The output impedance of current bias is 3 MΩ, which is extracted from the output resistance at the corresponding bias point.

To compare the effects of the device variation on circuit performance, two distribution models are adopted in the Monte Carlo simulation for (3-5) to calculate the CMRR value under the constant device distance of 200 μm in our work. One is the proposed model mentioned in chapter 2 and the other is Gaussian distribution. The parameters of Gaussian distribution used here are 1.69V, 0.03V, 59.66 cm^2/Vs and 7.84 cm^2/Vs, which are corresponding to the mean value and the deviation of the threshold voltage and mobility, respectively. Another simulation skill, worst case simulation is done by subsituting the boundary values of threshold voltage and mobility form our measured device into (3-5). This method also considered in our thesis for the comparsion with Monte Carlo simulation.

The simulation for CMRR value in dB is shown in Fig. 3-7. Generally speaking, the specification of the CMRR value in commerical IC is usually above 60dB. The result of worst case simulation is 35.6 dB. Obviously, design with this simulation method will underestimate the circuit performace of differential pair compared with Monte Carlo method. This is the reason why the five concer simulation is not suitable for circuit design in LTPS TFTs. The results of Monte Carlo method with Gussian distribution and our proposed model are represnted by red, blue, and green line, individually. The red line was plotted by Monte Carlo method with Gussian

distribution. As for the green line and blue line, they were done by Monte Carlo method with our proposed models. For the green line, the threshold voltage and mobility and their difference are subsituted with real distribtion and proposed model ,whlie the green line only take the average value of threshold voltage and mobility into simulation instead of their real distribution.

It can be obsevre that the blue line and green line are almost overlap, and this phenomenon shows that the difference terms dominate the simulation result of CMRR value. So, we can simplify our simulation procedure to only change for the difference terms instead. It was found that the curves of the cumulative probability exhibit a difference of 10 dB in average and cross at about 55 dB. It is attributted to the sharper distribution of the difference of V_{th} and Mu in reality than the Gaussian distribution.

If we put the all real measured data into simulation (dark blue line) under the constant device distance 200 μm, it can be observe that dark blue, blue, and green lines are very alike. We can recognize form above simulation result that the Monte Carlo method with our proposed model is more accurate compared to the Monte Carlo method with Gaussian model. However, it still will be noticed if we want to reach a confidence level of 98 % , the CMRR specification of the circuit should be below 50 dB based on the proposed model, instead of 53 dB corresponding to Gaussian model. As for the average performance, simulation adopting Gaussian distribution might give an underestimated prediction. This simulation approach can also be used to evalute the performance of other driving circuit of AMOLED by using matched TFTs [7] and other circuits which are sensitive to device mismatch.

3-3. Discussion and conclusion

We have proposed a new model of the device distributions describing the

differences in V_{th} and Mu of the LTPS TFTs. It provides an improved fitness and thus a better simulation result of the circuit performance compared with five-corner simulation or Monte Carlo simulation with an assumption of Gaussian distribution. These models can be also applied to the simulation for the uniformity of the AMOLED using matched TFT in the pixel design and other analog circuit design in display electronics with LTPS TFTs.

Chapter 4

Stress mapping for reliability

4-1. Motivation

In order to realize the new applications for LTPS TFTs, we have to improve the performance of devices such as enhancing mobility, decreasing the threshold voltage of TFTs, and shrinking the TFTS size. However, the improvement of reliability on poly-Si TFTs is as critical for the insurance of product lifetime. Because of the existence of grain boundary in channel, reliability becomes an important topic for application. In prior study [1], the diverse degradation behaviors occur due to different sources of LTPS TFTs and the variation of the initial value of device parameters. In our work, crosstie layout was adopted to obtain the uniform results. The stress mapping under the different stress voltages including different gate voltage (Vg) and drain voltage (Vd) for the different stress time will be established in this chapter.

4-2. Experiment and degradation mechanism

4-2-1. Setup for the stress map

The Fig. 4-1 shows the four regions of the stress map. The stress condition for region I is defined as the ranges of the stress bias applied to gate (Vg) and the stress bias applied to drain (Vd), which are from 0V to 10V and 0V to 10V, respectively. The region II is defined as the ranges of Vg and Vd, which are from 0V to 10V and

10V to 20V, individually. In the same way, the region III is defined as the ranges of Vg and Vd, which are from 10V to 20V and 0V to 10V. The region IV is defined as the ranges of Vg and Vd, which are 10V to 20V and 10V to 20V, respectively. The stress condition of region I for Vg is from 0V to 10V by taking 5V for a step. For the stress condition of Vd is also swept with the same step as Vg. The stress condition of region II for Vg is from 0V to 10V by taking 2V for a step, and the Vd is from 10V to 20V by also taking 2V for a step. The stress condition of region III for Vg and Vd are from 10V to 20V and 0V to 10V, and the all steps in this region are 2V. The stress condition of region IV for Vg and Vd are both from 10V to 20V, and the step is 2V. Furthermore, the conditions of stress time are 10sec, 50sec, 100sec, and 1000sec, respectively. We take the fewer grids for stress measurement in region I because the slighter degradation phenomenon we expected in this region. It will be proven in the result we will discuss later.

4-2-1. Degradation mechanism

The mechanism of degradation under DC stress for the LTPS TFTs will be introduced in this section. There are several kinds of degradation phenomenon in poly-Si TFTs have already been reported [8-16]. For example, the sources of degradation are hot carriers, self-heating, water, contamination, and electrostatic discharge. The two main sources of degradation are hot carrier and self-heating, which will be described in detail as follows.

Hot carrier effects [8-9] resulting from the high electric field near the drain junction have been widely investigated in LTPS TFTs. Conduction carriers can obtain energy from the high electric field and become “hot”. Thus, the carriers with high kinetic energy can easily break the weak bonds existing in poly-Si, creating many

defect states and oxide charges. Serious degradation can be generated in the hot carrier operation mode, and the degree of degradation depends on the strength of the electric field. Since the number of traps is larger in poly-Si than conventional MOS, the hot carrier effect is accordingly worse. Introducing electric-field-relief TFT structures, such as lightly doped drain (LDD), offset drain, and gate-drain overlapped LDD (GO-LDD), can reduce the hot carrier degradation.

As the gate voltage increases and correspondingly the equivalent lateral electrical field decreases, the hot carrier effect will be reduced. Instead, the power dissipation in the device is becoming high, causing the increase of device temperature due to Joule heat, which is known as self-heating or thermal effects [10-16]. Since TFTs are fabricated on glass substrate, the heat dissipation to the substrate is relatively low compared with Si substrate. It will make the degradation worse. Besides, the influence of self-heating effects will increase with the width of TFTs.

4-3. Results and discussion

The stress maps under different stress conditions of Vg and Vd are demostrated in Fig. 4-2, Fig. 4-3, Fig. 4-4. The stress maps for threshold voltage under different stress time, 10sec, 50sec, 100sec, and 1000sec are shown in Fig. 4-2 (a) to 4-2 (d), respectively. Likewise the stress maps for mobility and subthreshold swing under different stress time are shown in Fig. 4-3 (a) to 4-3 (d) and Fig. 4-4 (a) to 4-4 (d).

For the region I, owing to the low electric field and the low power dissipation, we can not obviously observe the phenomenon of device degradation. The operation of TFTs in this region are more reliable for normal circuit purpose.

As for the region II, we can obviously observe the phenomenon of the mobility degradation and V_{th} shift, but slight degradation in S.S. The hot carrier effect

dominates in this region, which generates the hot carrier of the electrons by high lateral electric field. They can create interface-trapped charges or some defects near the drain region. We consider that the V_{th} shift owing to fixed charge in oxide, and the mobility degradation is due to Coulomb scattering of the fixed chatge. However, there is almost no degradation of S.S in this region, which implies that the device has few changes in the deep states during the stress. This phenomenon also implies that the dangling bonds are neither increased nor created. Moreover, the degradation behaviors apear in a few tens of seconds and tend to saturation as the stress time increasing. We belive that defects generated initially can reduce the electric field and retard the further creation of new defects.

In the region III of stress map, we observe the slighter V_{th} shift and S.S degradation, but it is seem to be no degradation or even slight increase in mobility. In contrast to region II, the degrees of the degradation in V_{th} shift and S.S are higher than the region I but lower than the region II. The proposed explanation for the different degrees of the degradation phenomenon is the lower lateral electric field and the less power than those in the region II. The lateral electric field and the power in this region is relative small compared to region II and IV. Consequently, the hot-carrirer effect and self-heating effect are not so obvious.

For region IV, the degradation phenomenons are more complicated. We can obviously observe the serious Vt shift, mobility and S.S degradation. According to these behaviors, we can speculate not only hot carrier effect but also self-heating effect occuring in this region. Owing to the larger power, Joule heat drives the hydrogen running away and dangling bonds are left. For the reason of the increase of the deep states, S.S in this region is suffered form severe degradation. Under the condition of Vg and Vd which are both higer than 18V, the device will be burn out during our experiment. In addition, we can see the continuous degradation in this

region. In other words, the created defects can not slow down or stop the generation of more defects. This observation is consistent with the hypothetic degradation mechanism of the lasting diffusion of hydrogen.

The crosstie layout LTPS TFTs were adopted in our work. In the relative short range, the initial characteristics in these TFTs we used to compelete our stress test are very similar. For this reason, we got the more consistent degradation behaviors in our bias stress tests. On the basis of our stress maps, the gate and drain bais (Vg and Vd) will be applied below 10V for the safe and continous opreation for LTPS TFTs.

Chapter 5

Conclusion

In this thesis, we investigate the reliability and the variation behaviors of LTPS TFTs by statistical means. In prior study, reliability behaviors will be strongly relative to initial characteristics of TFTs. For this reason, a special layout of TFTs called "crosstie" is adopted in this work. By introducing this kind of TFTs, we can get the more consistent reliability behaviors. Besides, the TFTs are placed in order and we can find the dependence of distance for device variations. In chapter two we classify two kinds of variation behaviors by grouping the difference of parameters in TFTs under different device distances. We find out that the variation in the range will be piecewise linear and the micro variation will be invariant in device position. The following is the proposed models for the difference of parameters. In this model, it can be observed that the shape of these distributions seem to be no changes in their shape. This result tells us the micro variation will be invariant in device position indeed.

The following is the application for these models we proposed. The simulations of the mismatch due to the device variation in differential pair are demonstrated. We can obtain the very similar results in CMRR value by using our proposed models compared with the real data. It was also found that Gaussian model we commonly assumed might underestimate the circuit performance.

Finally we report the reliability of LTPS TFTs in form of stress map by adopting

the crosstie layout TFTs to get the consistent reliability behaviors. The two main degradation mechanisms, hot carrier and self heating effects, are also observed in our work. We can also define a safe operation region for circuit applications via our stress map, and this reliability database is helpful to the development of accurate device lifetime model.

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Figures

Chapter 1

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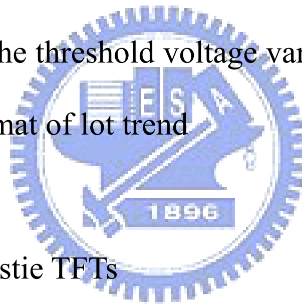
Fig. 1-5 The initial characteristics of LTPS TFTs are different from one another due to various distributions of grain boundaries

Fig. 1-6 The site variation of the threshold voltage variation for LTPS TFT fabrication line plotted in the format of lot trend



Chapter 2

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Fig. 2-13 (d) The distribution of Vth deference and its fitting curve under the device distance of 4000 μm

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Fig. 2-14 (a) The distribution of mobility deference and its fitting curve under the device distance of 40 μm

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Fig. 4-3 (a) The degradation behaviors of mobility under the stress time of 10 sec

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Fig. 4-3 (c) The degradation behaviors of mobility under the stress time of 100 sec

Fig. 4-3 (d) The degradation behaviors of mobility under the stress time of 1000 sec

Fig. 4-4 (a) The degradation behaviors of S.S under the stress time of 10 sec

Fig. 4-4 (b) The degradation behaviors of S.S under the stress time of 50 sec

Fig. 4-4 (c) The degradation behaviors of S.S under the stress time of 100 sec

Fig. 4-4 (d) The degradation behaviors of S.S under the stress time of 1000 sec

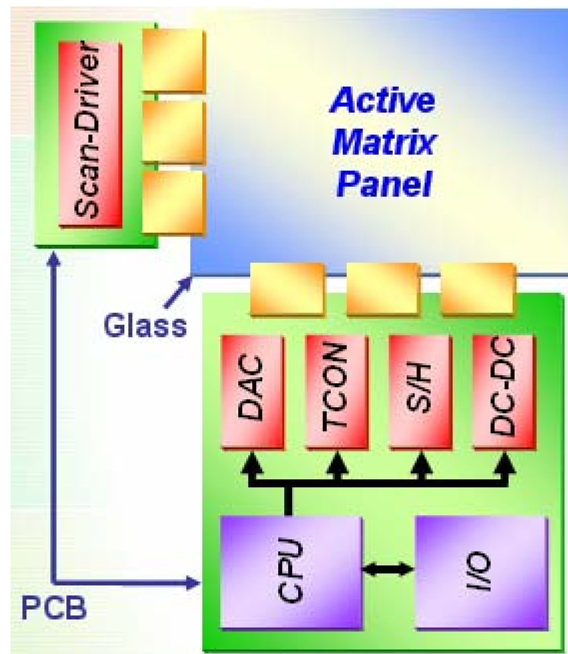

Fig. 1-1 The block diagram of an active matrix display

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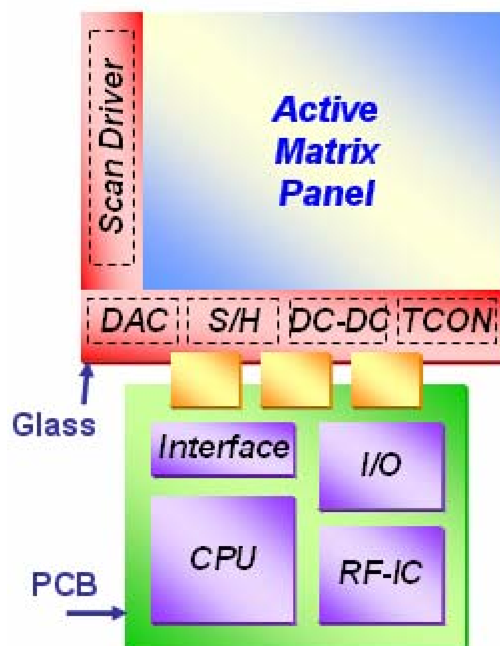


Fig. 1-2 The integration of peripheral circuits in a display achieved by poly-Si TFTs

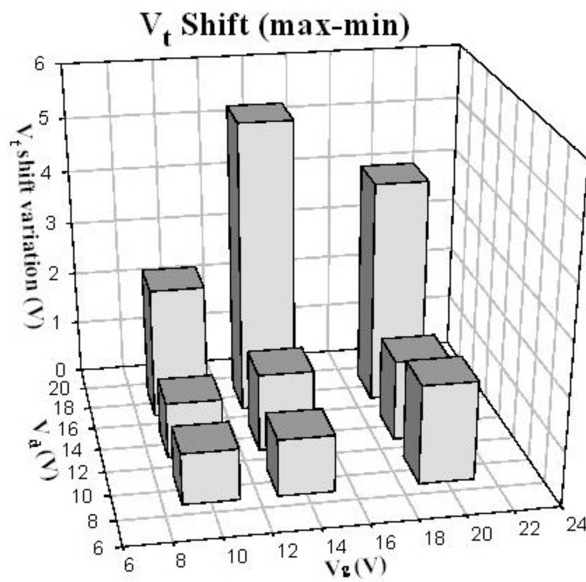


Fig. 1-3 The variation of threshold voltage shift under different stress conditions

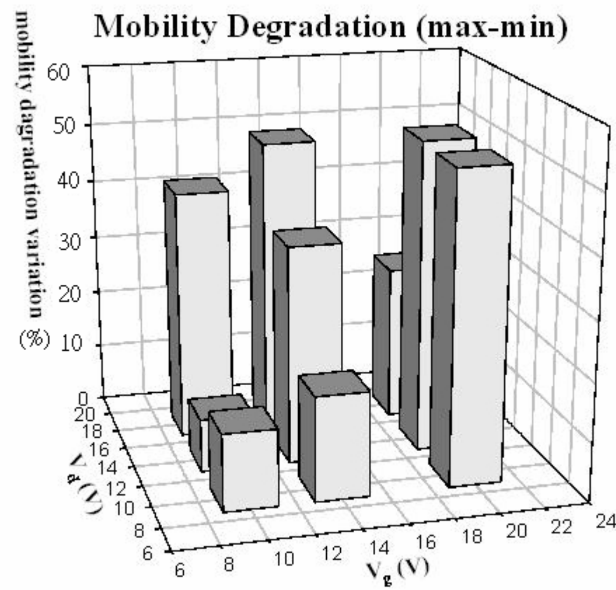


Fig. 1-4 The variation of mobility degradation under different stress conditions

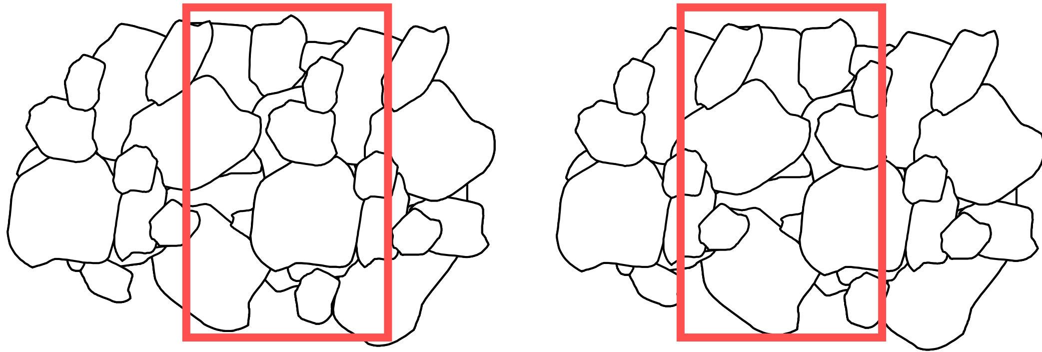


Fig. 1-5 The initial characteristics of LTPS TFTs are different from one another due to various distributions of grain boundaries

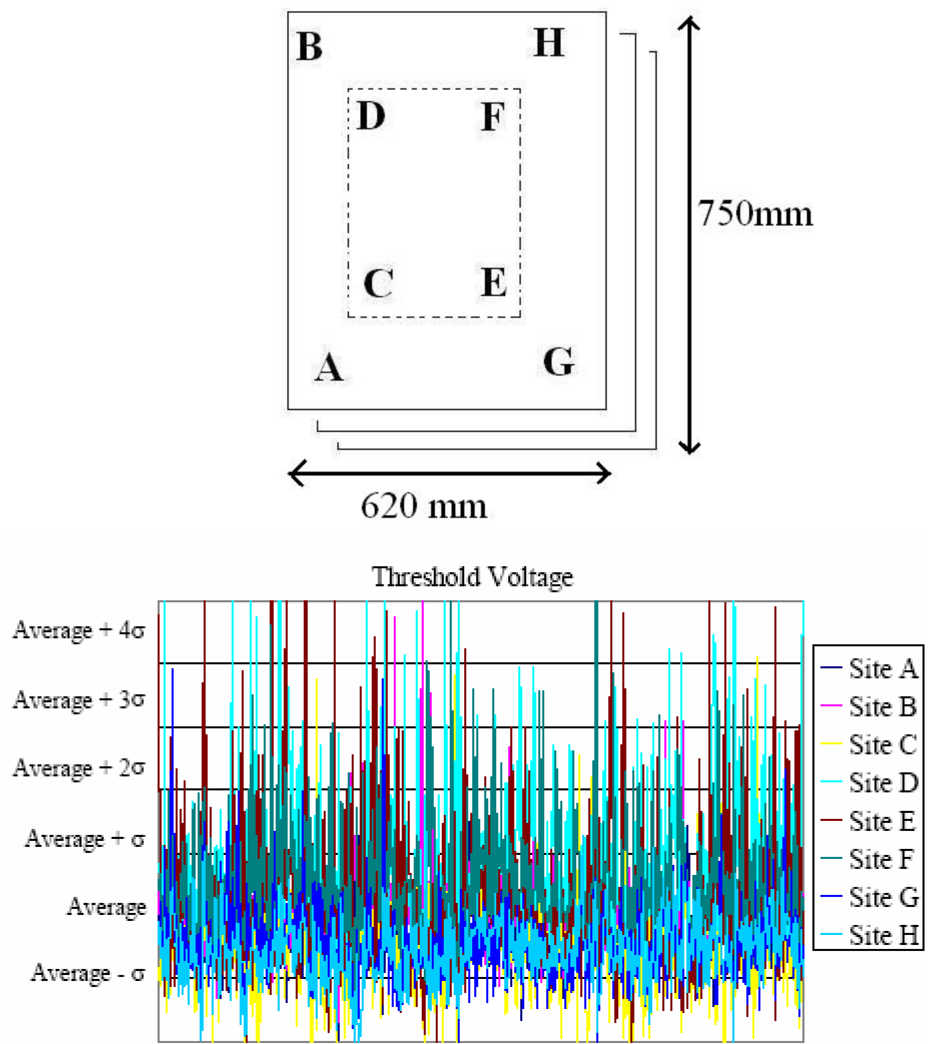


Fig. 1-6 The site variation of the threshold voltage variation for LTPS TFT fabrication line plotted in the format of lot trend

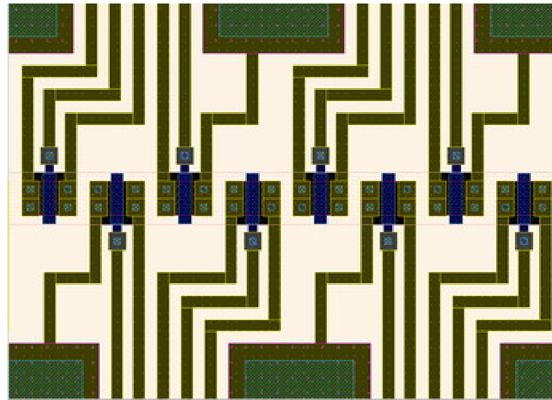


Fig. 2-1 The layout of the crosstie TFTs

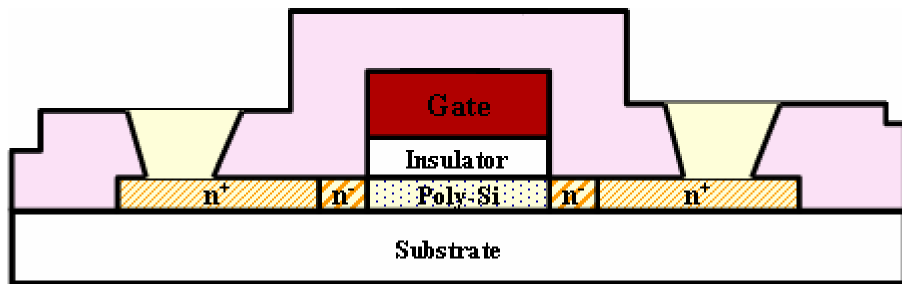


Fig. 2-2 The schematic cross-section structure of the n-type poly-Si TFT with lightly doped drain

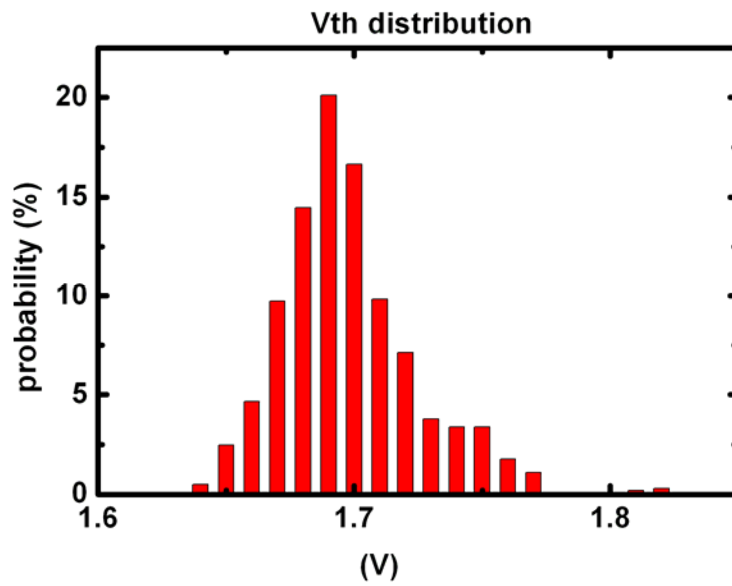


Fig. 2-3 The distributions of threshold voltage for crosstie TFTs

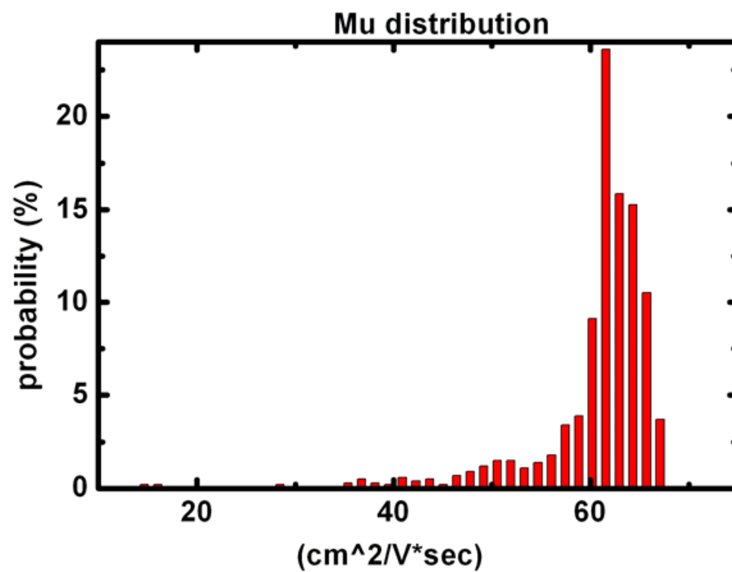


Fig. 2-4 The distributions of mobility for crosstie TFTs

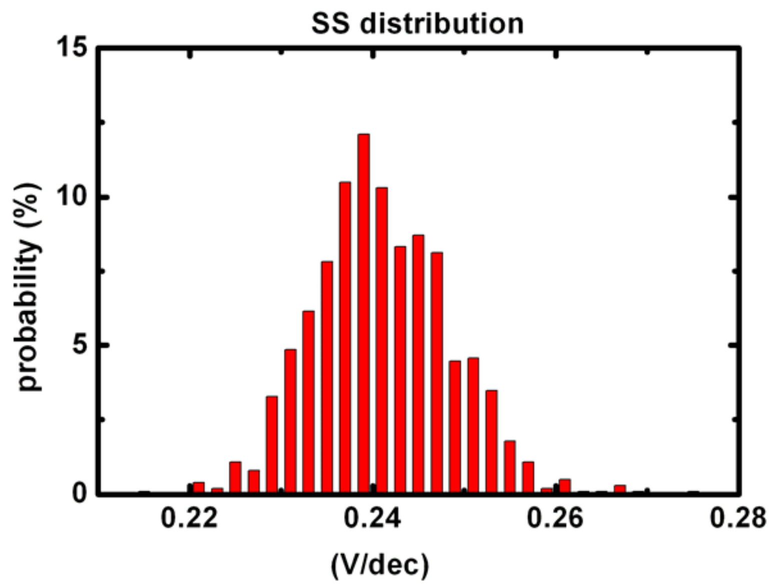
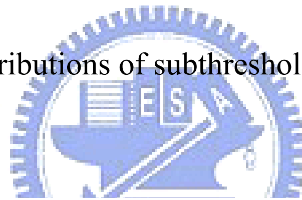


Fig. 2-5 The distributions of subthreshold for crosstie TFTs



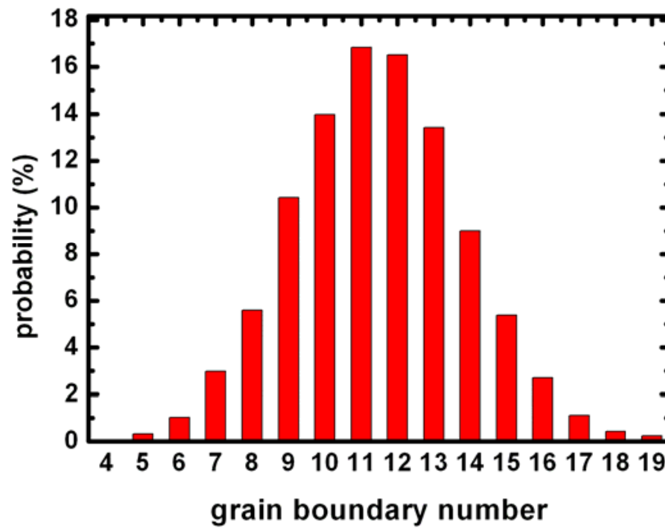


Fig. 2-6 The grain boundary number in the channel length direction

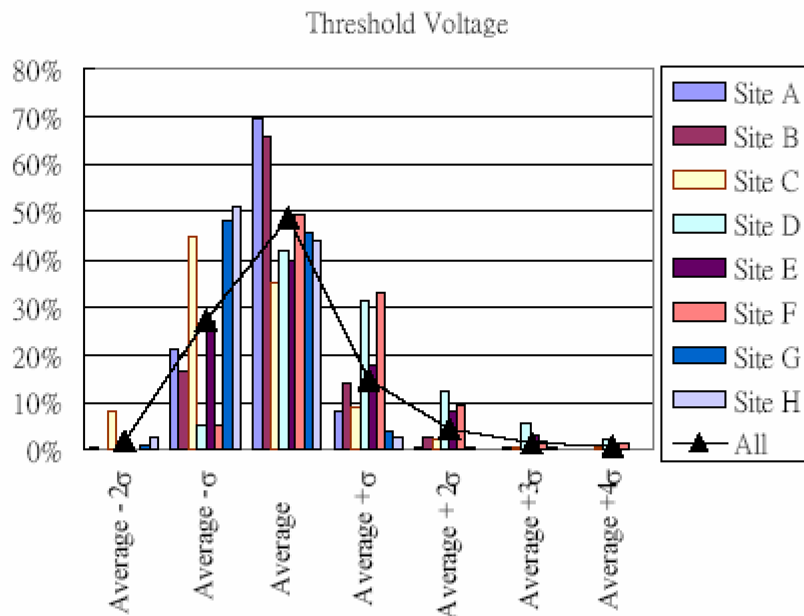


Fig. 2-7 The distributions of initial parameters vary with the different sites on glass and lot

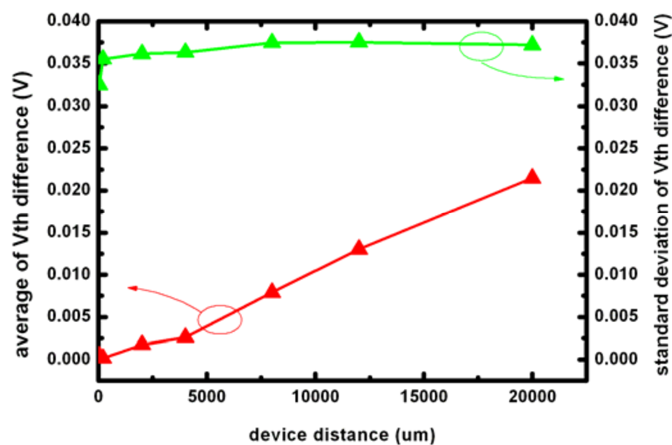


Fig. 2-8 The average and the standard deviation of the differences of threshold voltage

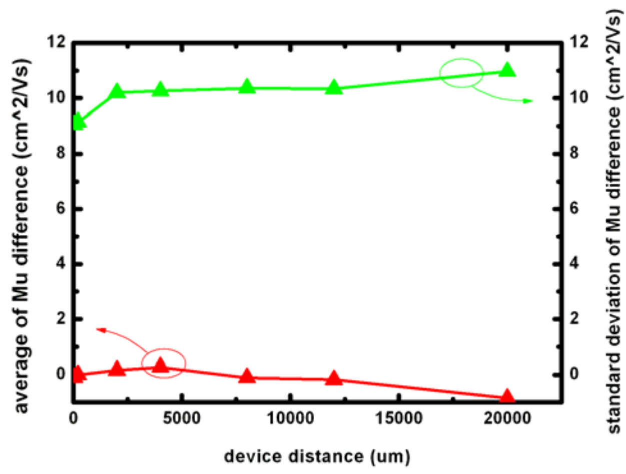


Fig. 2-9 The average and the standard deviation of the differences of mobility

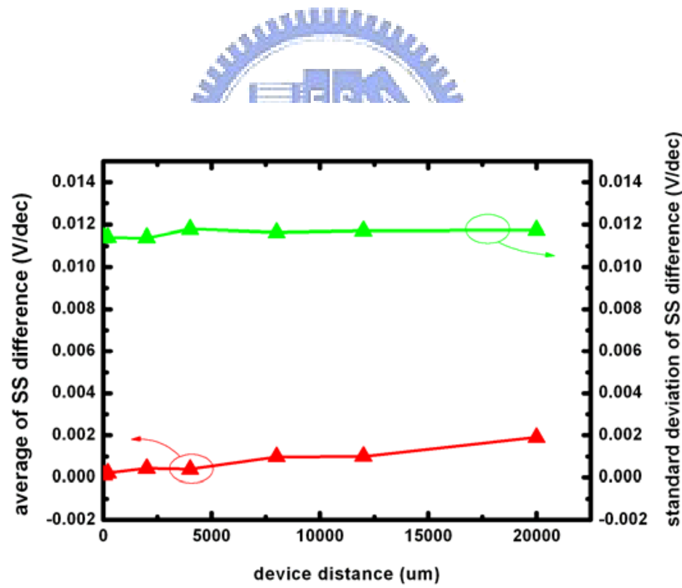


Fig. 2-10 The average and the standard deviation of the differences of subthreshold swing

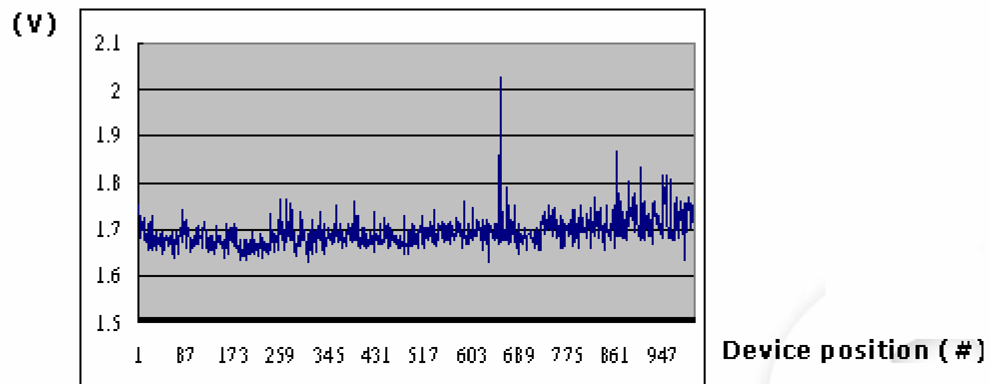


Fig. 2-11 The threshold voltage distribution along the device position

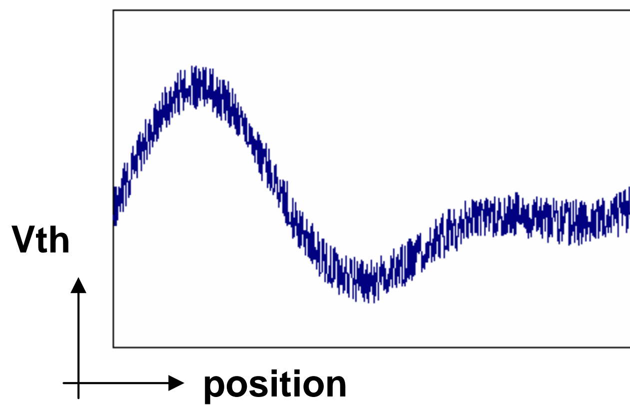


Fig. 2-12 Simulation of the threshold voltage distribution along the device position for a long range

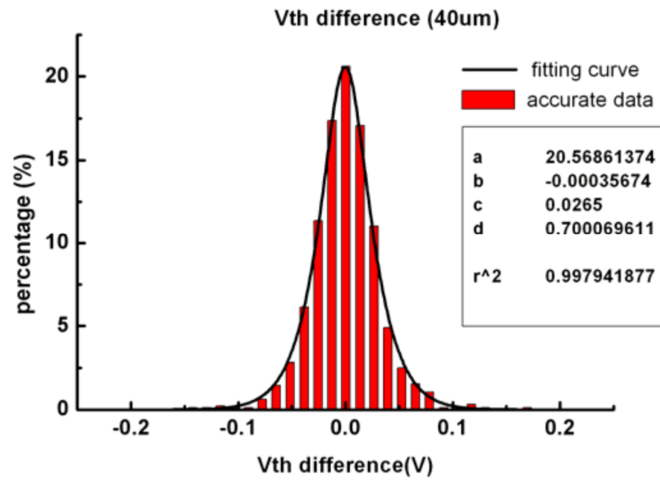
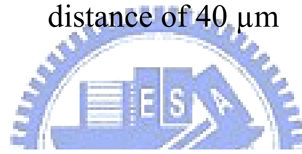


Fig. 2-13 (a) The distribution of Vth deference and its fitting curve under the device distance of 40 μm



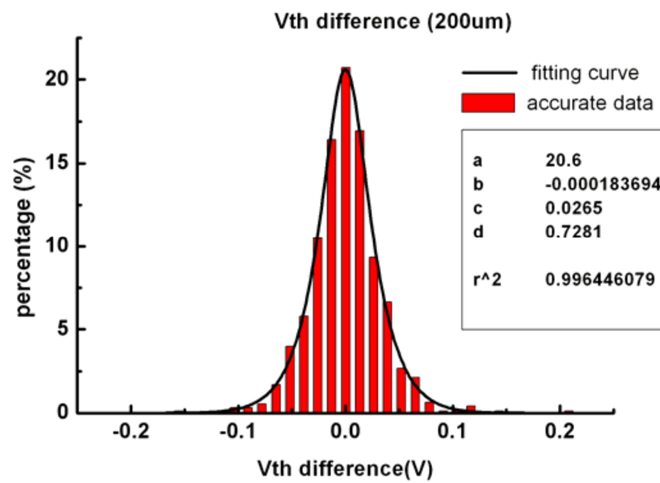


Fig. 2-13 (b) The distribution of Vth deference and its fitting curve under the device distance of 200 μm

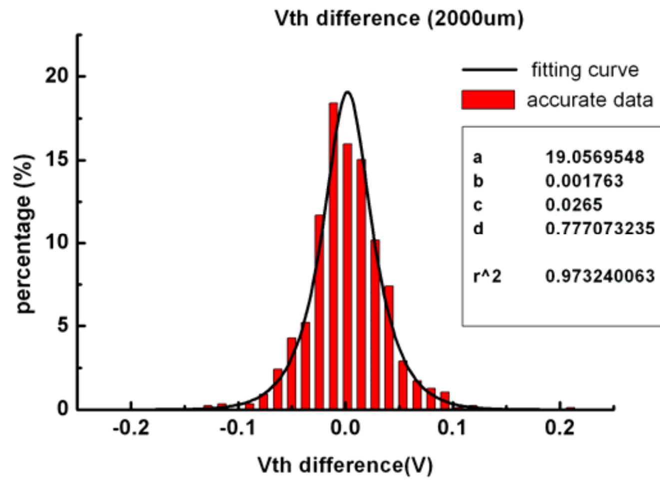


Fig. 2-13 (c) The distribution of Vth deference and its fitting curve under the device distance of 2000 μm

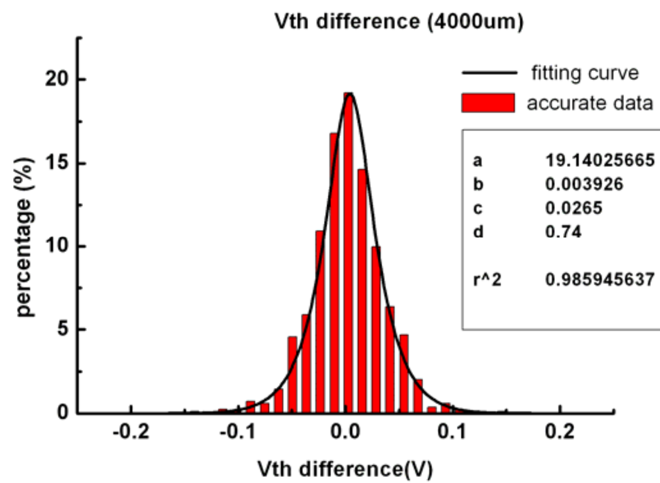


Fig. 2-13 (d) The distribution of Vth deference and its fitting curve under the device distance of 4000 μm

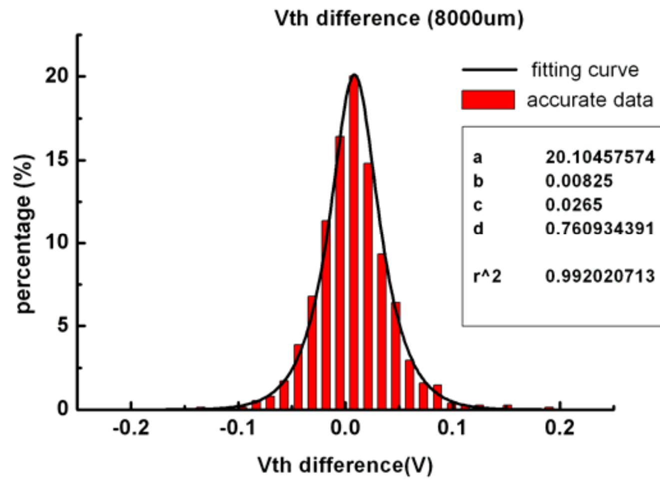


Fig. 2-13 (e) The distribution of Vth deference and its fitting curve under the device distance of 8000 μm

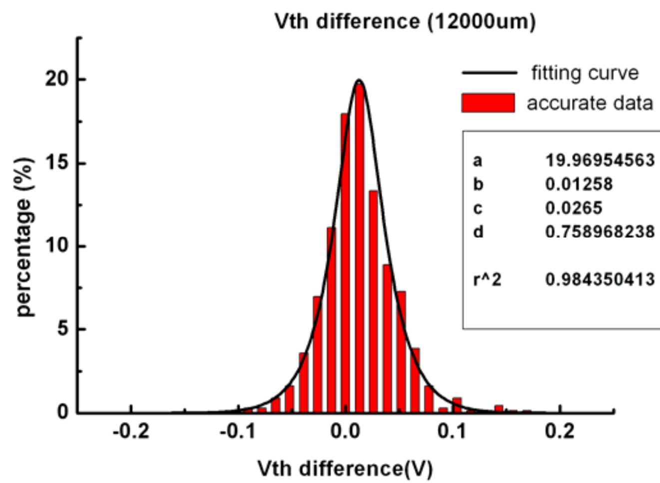


Fig. 2-13 (f) The distribution of Vth deference and its fitting curve under the device distance of 12000 μm

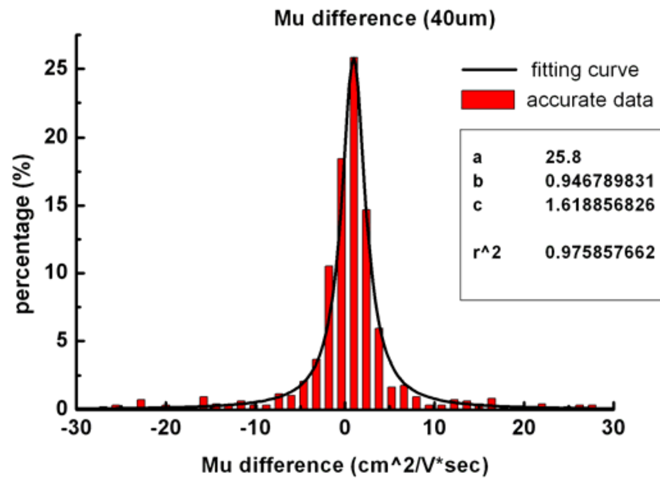
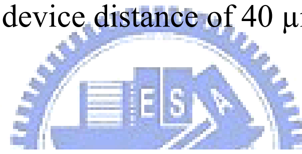


Fig. 2-14 (a) The distribution of mobility deference and its fitting curve under the device distance of 40 μm



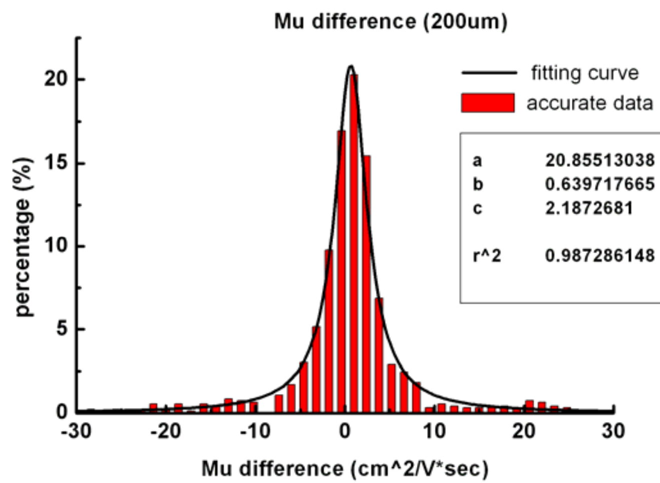


Fig. 2-14 (b) The distribution of mobility deference and its fitting curve under the device distance of 200 μm

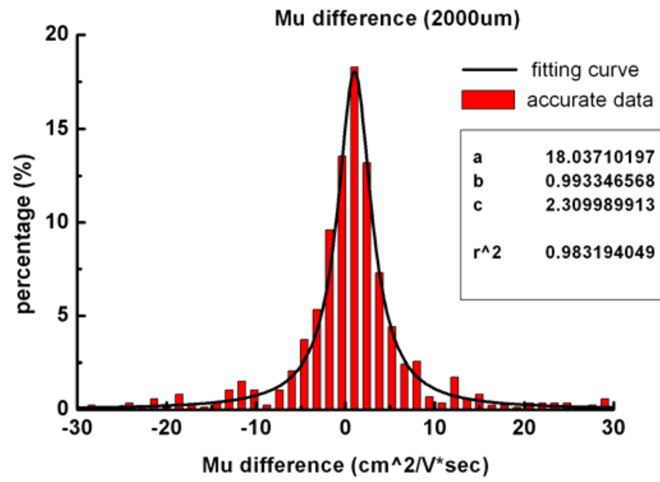


Fig. 2-14 (c) The distribution of mobility deference and its fitting curve under the device distance of 2000 μm

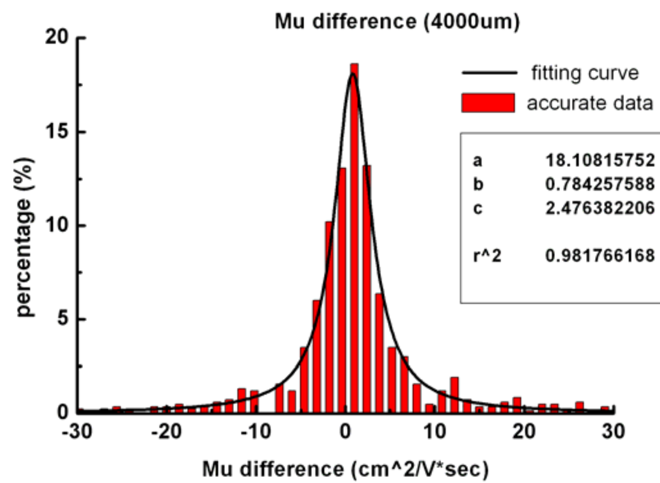


Fig. 2-14 (d) The distribution of mobility deference and its fitting curve under the device distance of 4000 μm

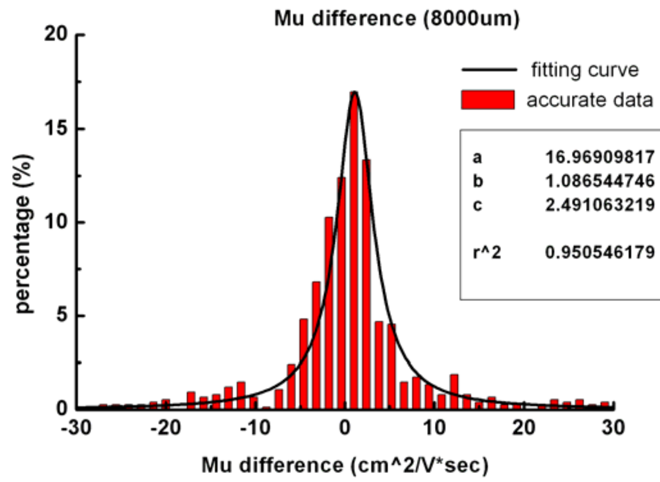


Fig. 2-14 (e) The distribution of mobility deference and its fitting curve under the device distance of 8000 μm

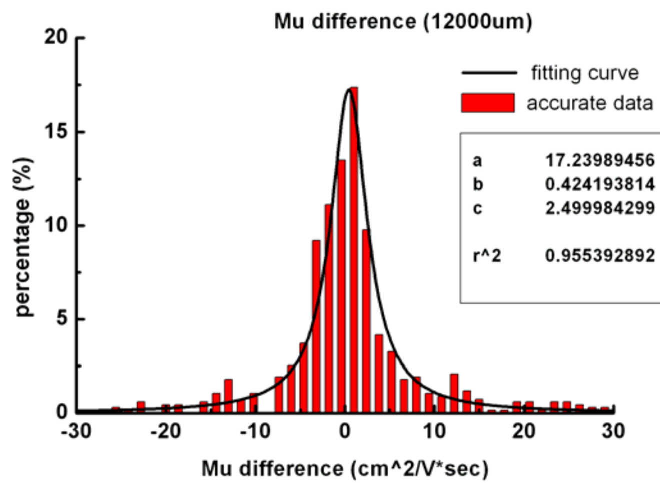


Fig. 2-14 (f) The distribution of mobility deference and its fitting curve under the device distance of 12000 μm

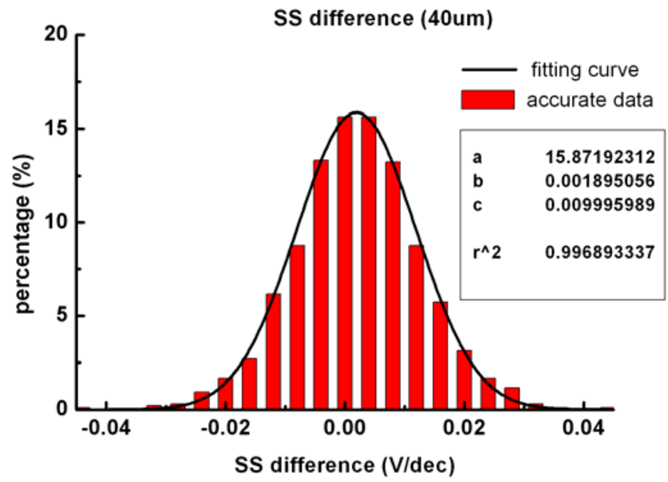
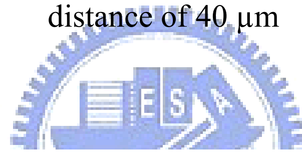


Fig. 2-15 (a) The distribution of S.S deference and its fitting curve under the device distance of 40 μm



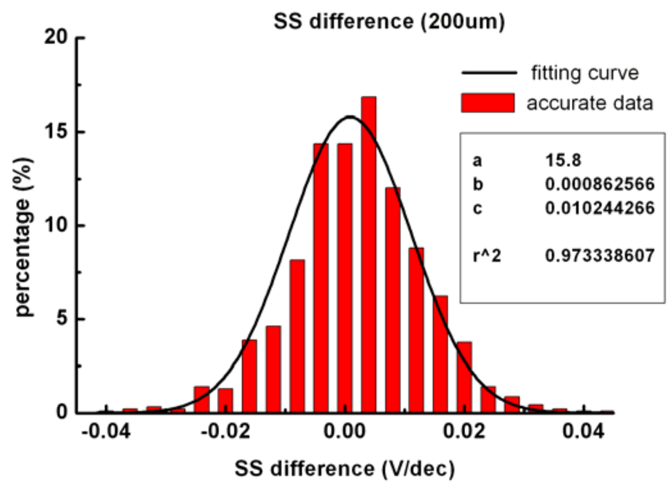


Fig. 2-15 (b) The distribution of S.S deference and its fitting curve under the device distance of 200 μm

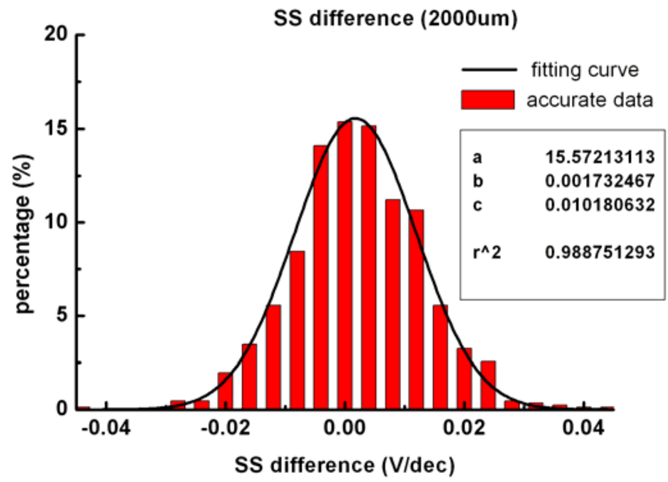


Fig. 2-15 (c) The distribution of S.S deference and its fitting curve under the device distance of 2000 μm

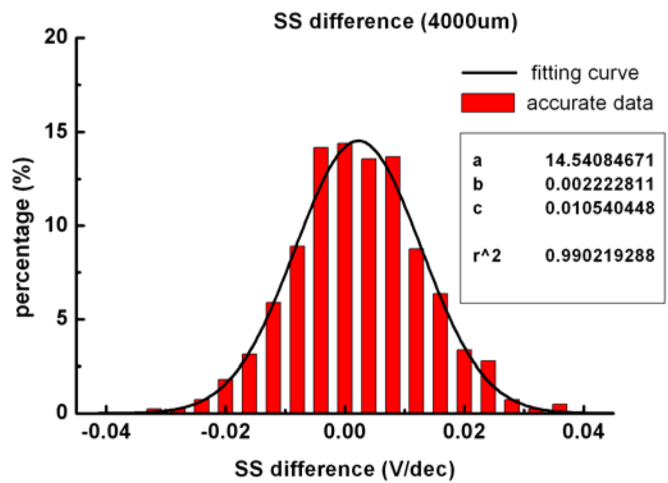


Fig. 2-15 (d) The distribution of S.S deference and its fitting curve under the device distance of 4000 μm

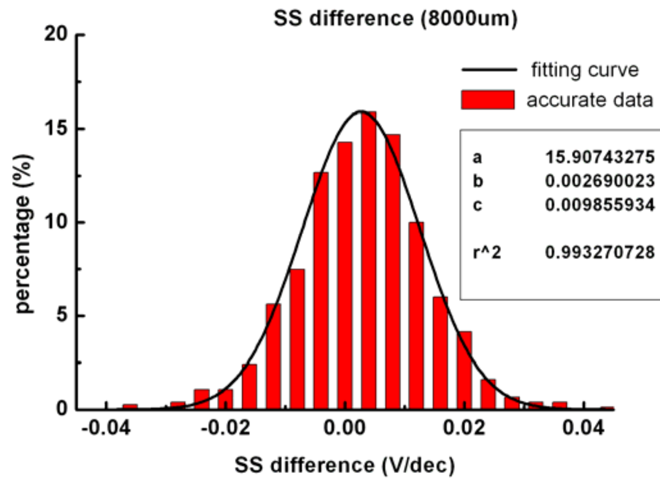


Fig. 2-15 (e) The distribution of S.S deference and its fitting curve under the device distance of 8000 μm

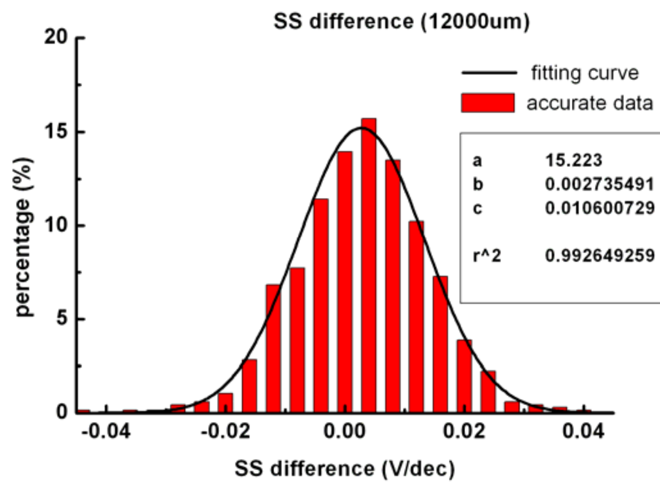
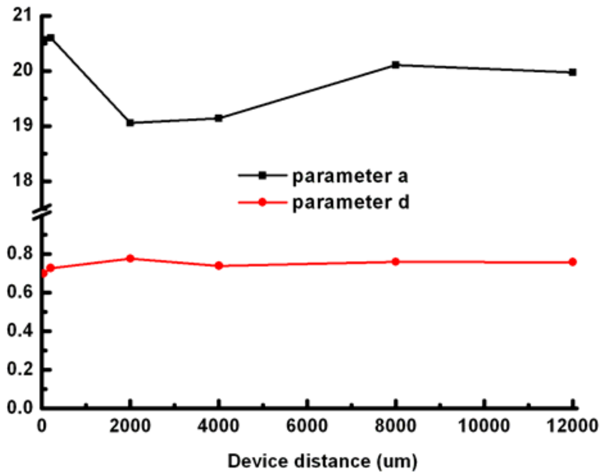


Fig. 2-15 (f) The distribution of S.S deference and its fitting curve under the device distance of 12000 μm



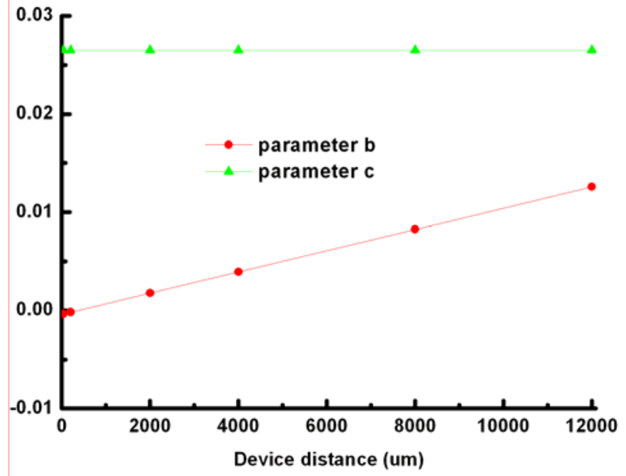


Fig. 2-16 (a) The fitting parameters, *a* and *d* of V_{th} difference versus the device distance

Fig. 2-16 (b) The fitting parameters, *b* and *c* of V_{th} difference versus the device distance

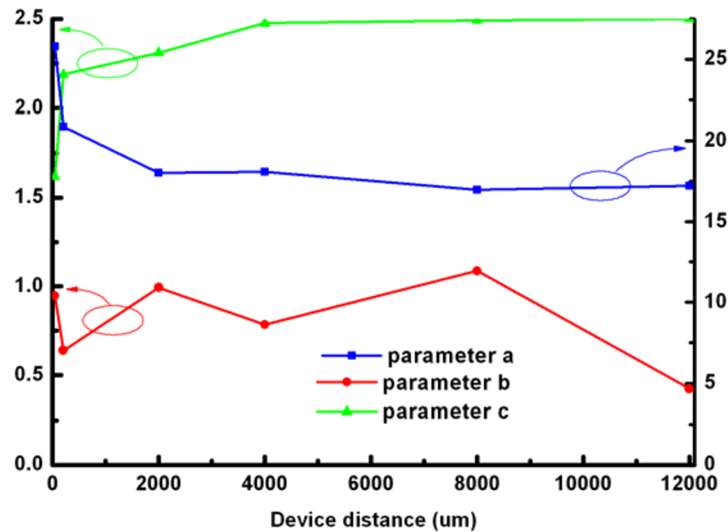


Fig. 2-17 The fitting parameters of Mu difference versus the device distance

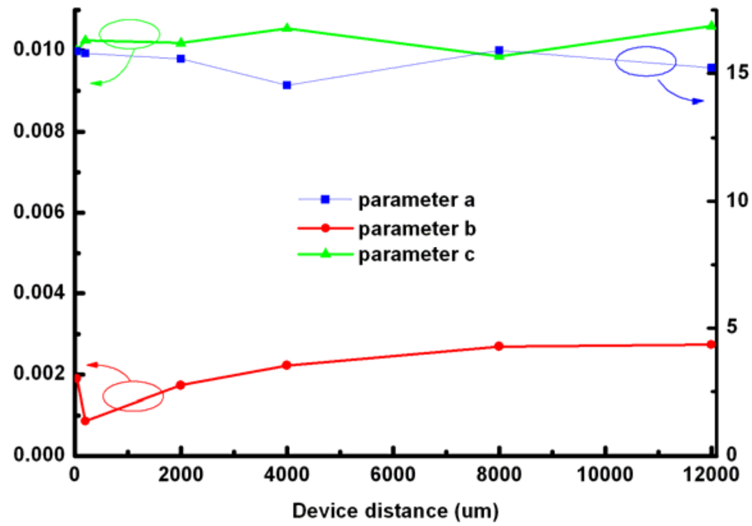


Fig. 2-18 The fitting parameters of Mu difference versus the device distance

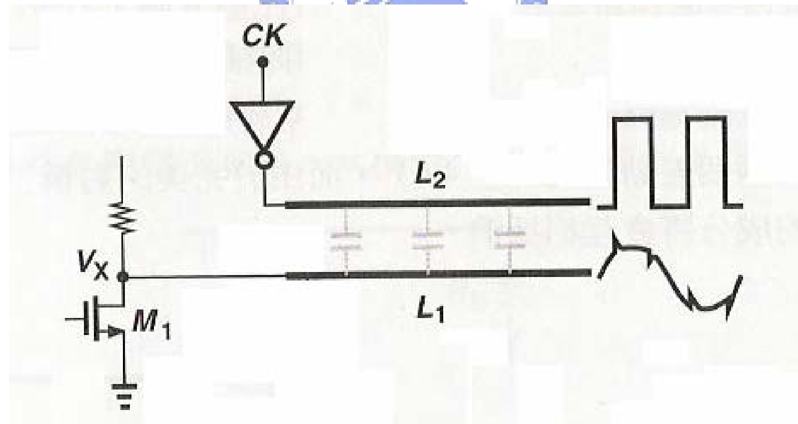


Fig. 3-1 (a) The coupling effects of the clock signal

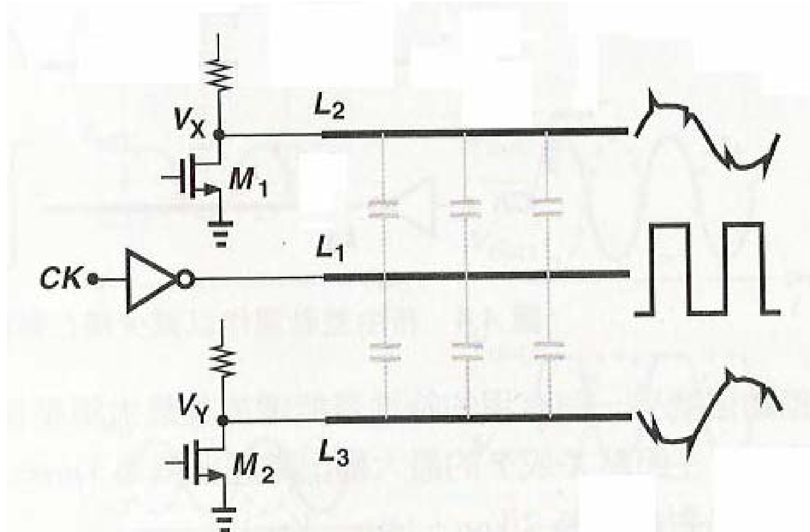


Fig. 3-1 (b) The signal transmission is done by differential signal

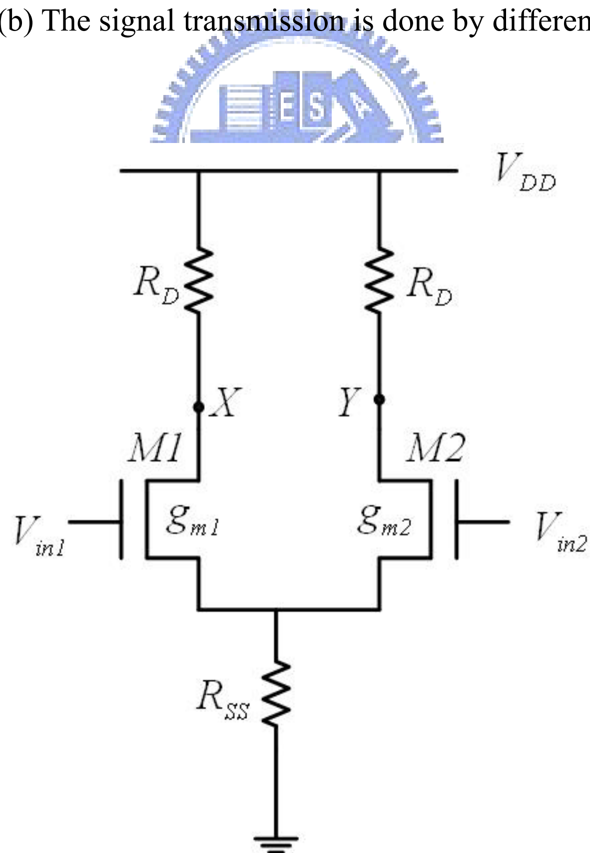


Fig. 3-2 Basic differential pair structure

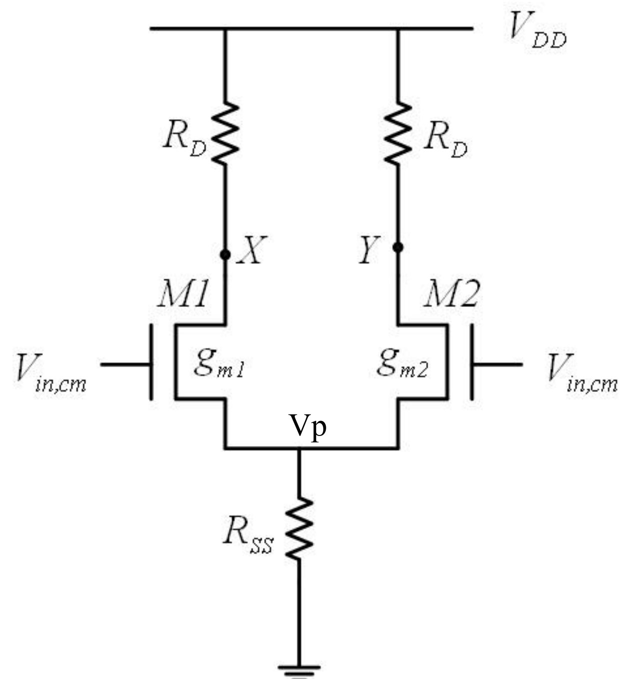
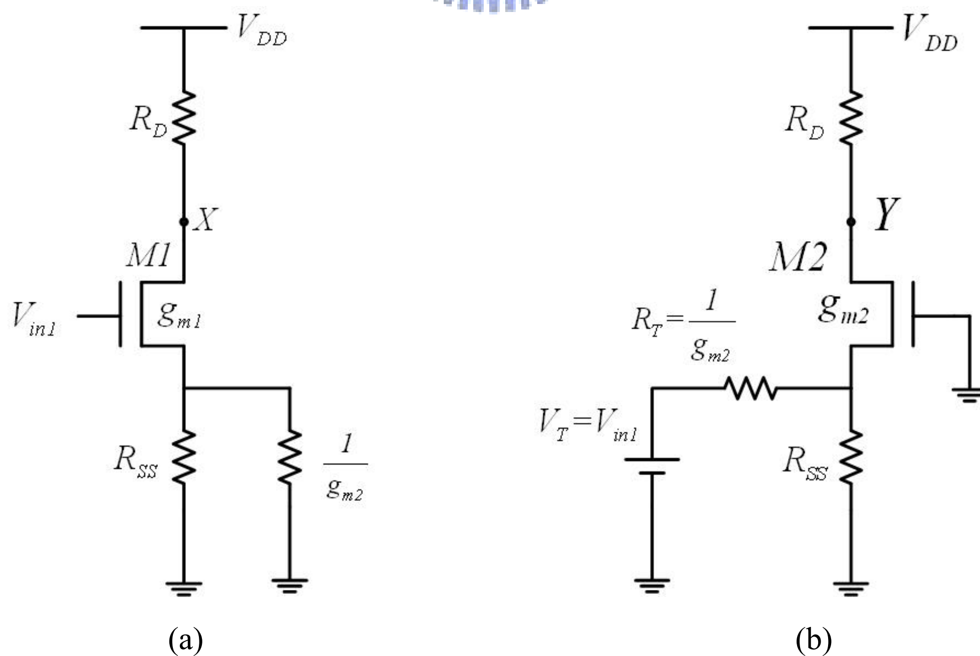


Fig. 3-3 The equivalent for common mode operation



(a) (b)

Fig. 3-4 (a) The equivalent for common mode operation (Vin1 on, Vin2 off)
(b) The equivalent for common mode operation (Vin1 off, Vin2 on)

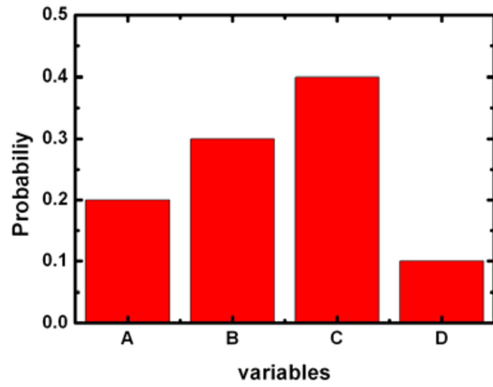


Fig. 3-5 Simple distribution with four variables

Random value	Corresponding variable
0 ~ 0.2	A
0.2 ~ 0.5	B
0.5 ~ 0.9	C
0.9 ~ 1.0	D

Fig. 3-6 The chart for data transformation

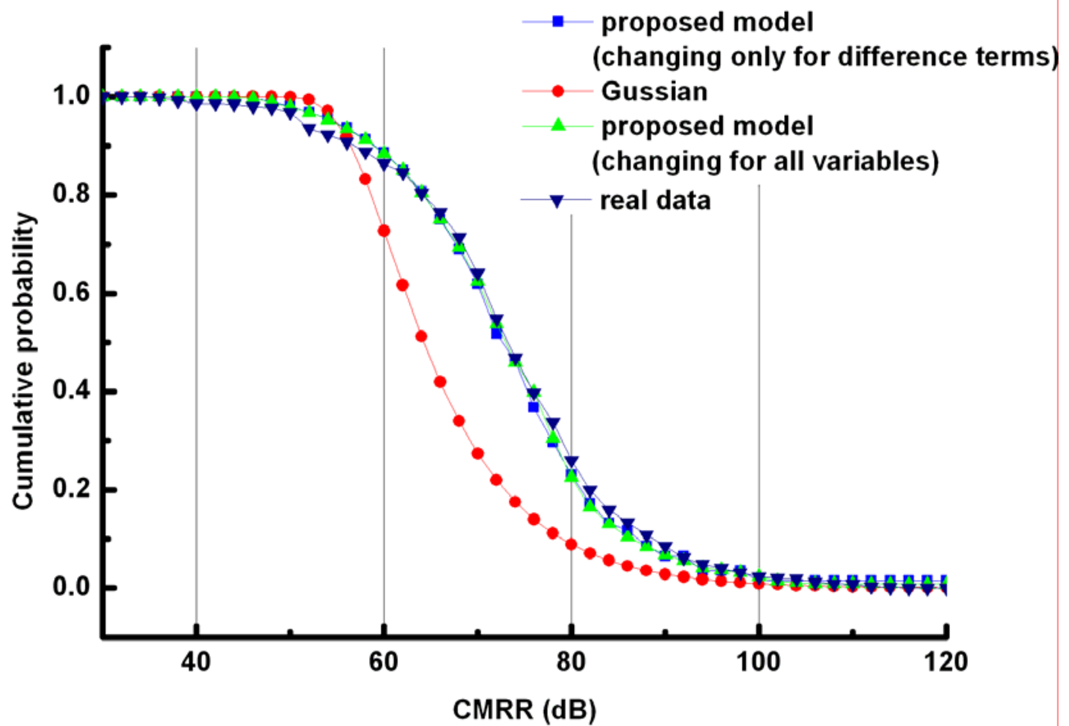


Fig. 3-7 The simulation results for CMRR value with different models

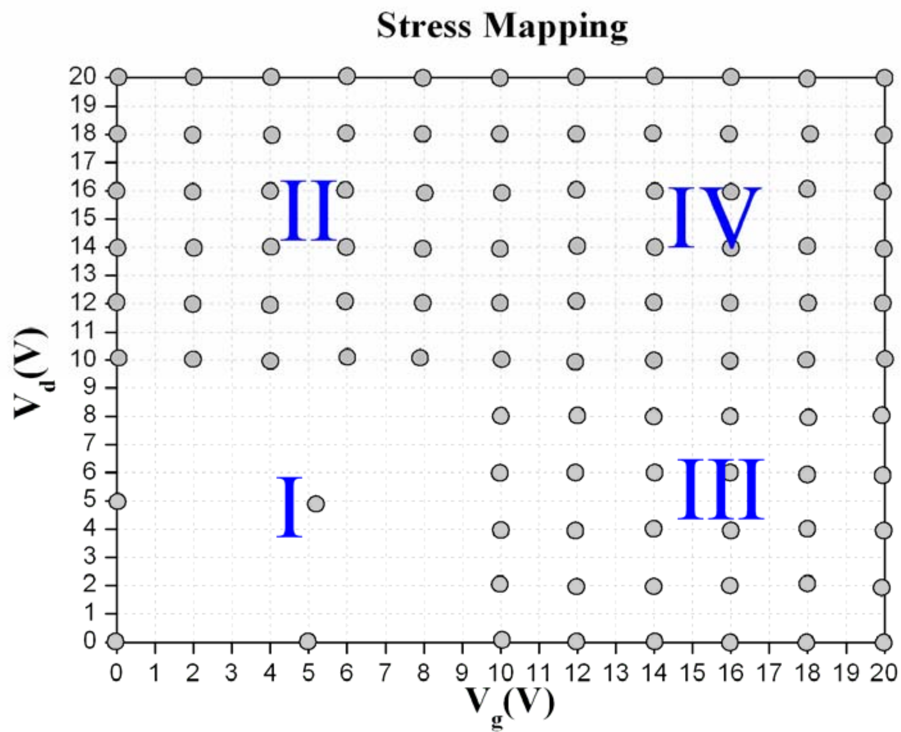


Fig. 4-1 Four regions of stress mapping and the gray circles are the stress conditions for the test

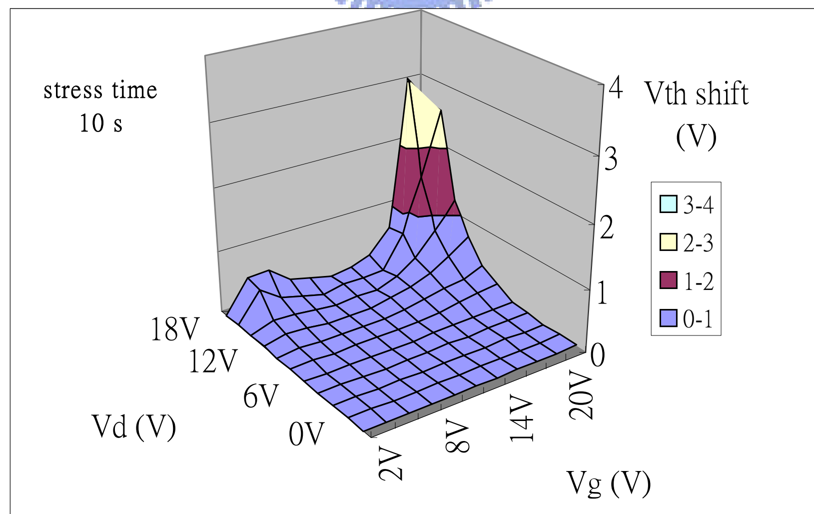


Fig. 4-2 (a) The degradation behaviors of V_{th} under the stress time of 10 sec

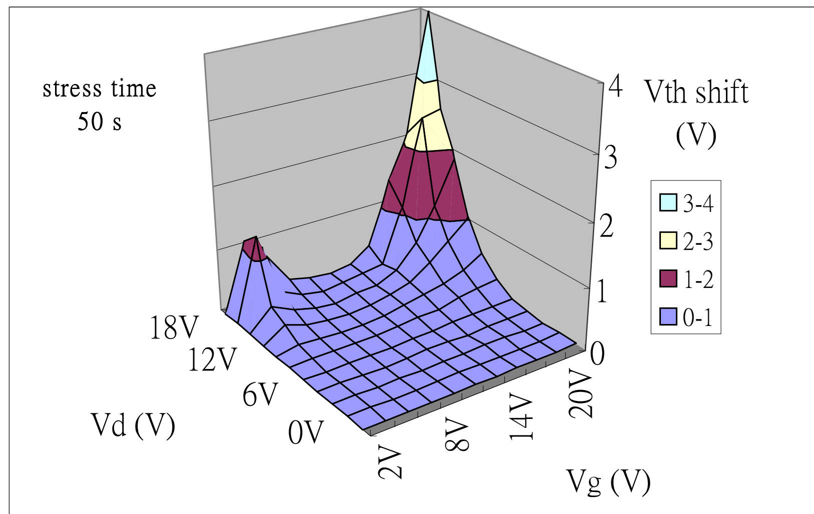


Fig. 4-2 (b) The degradation behaviors of V_{th} under the stress time of 50 sec

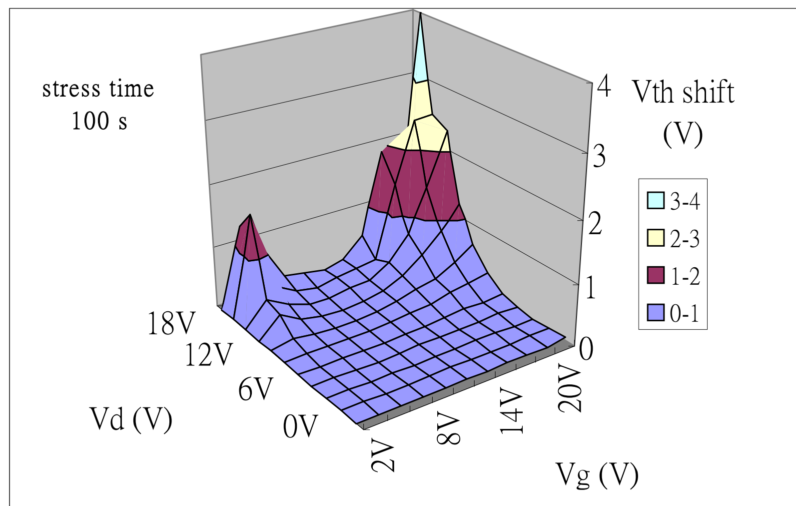


Fig. 4-2 (c) The degradation behaviors of V_{th} under the stress time of 100 sec

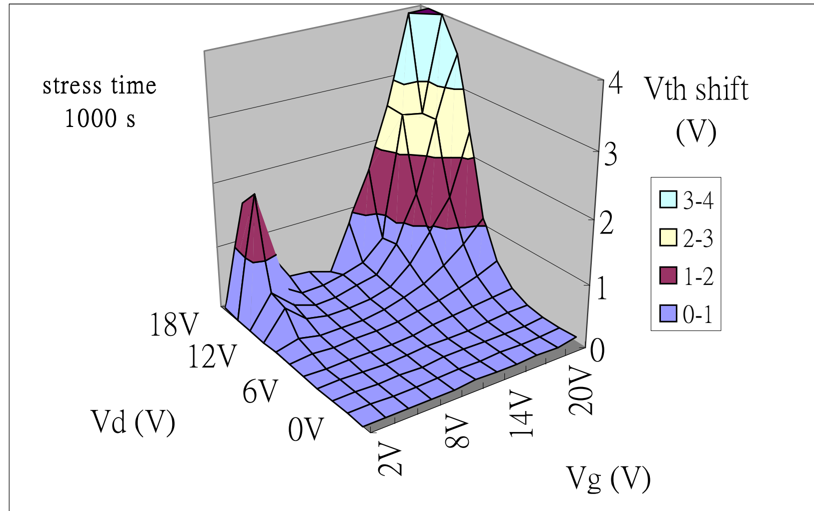


Fig. 4-2 (d) The degradation behaviors of V_{th} under the stress time of 1000 sec

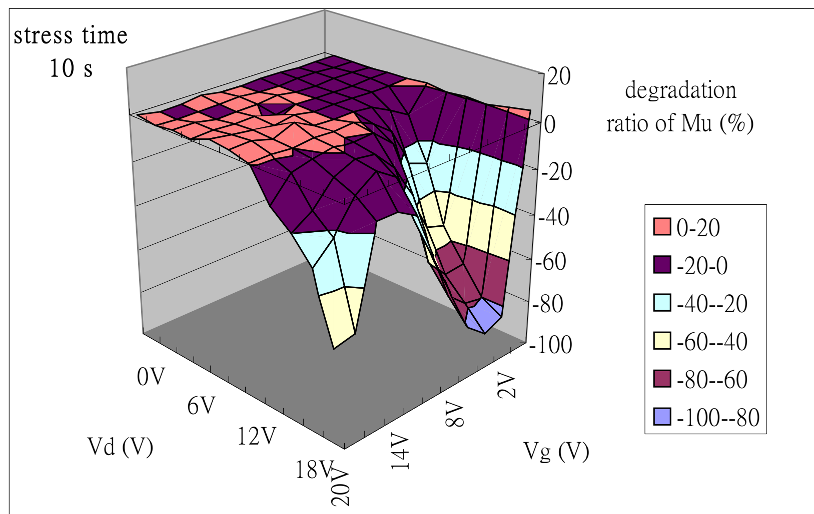


Fig. 4-3 (a) The degradation behaviors of mobility under the stress time of 10 sec

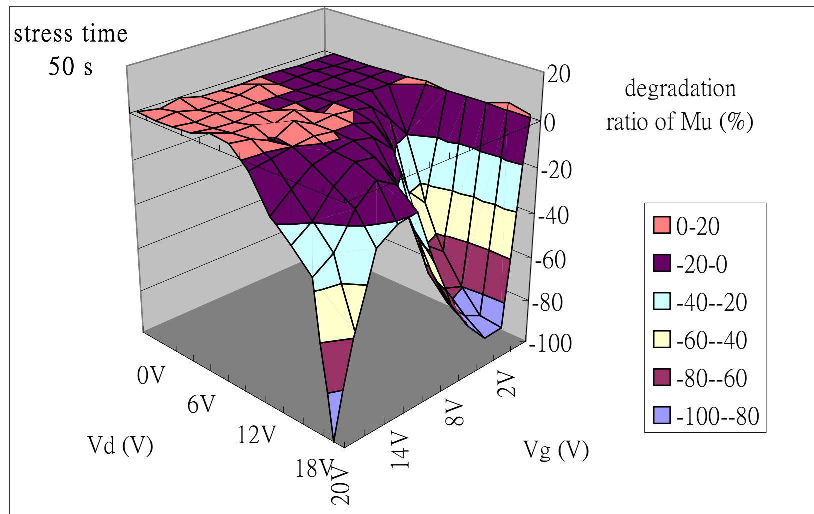


Fig. 4-3 (b) The degradation behaviors of mobility under the stress time of 50 sec

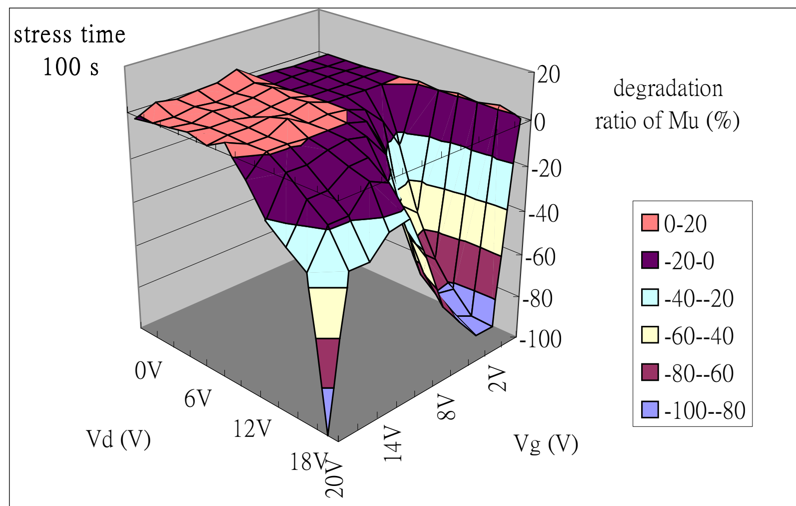


Fig. 4-3 (c) The degradation behaviors of mobility under the stress time of 100 sec

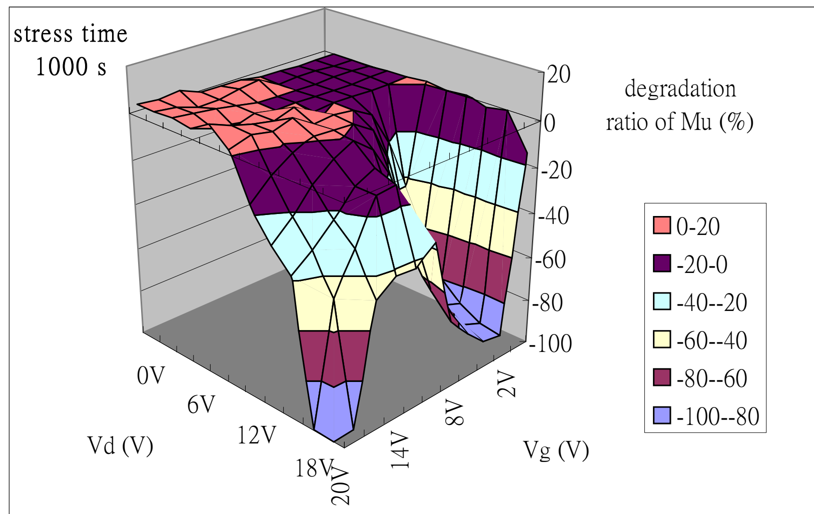


Fig. 4-3 (d) The degradation behaviors of mobility under the stress time of 1000 sec

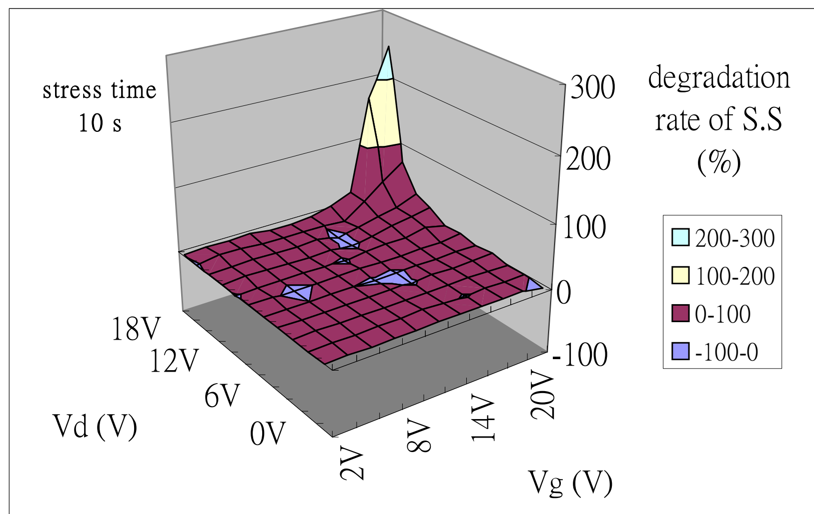


Fig. 4-4 (a) The degradation behaviors of S.S under the stress time of 10 sec

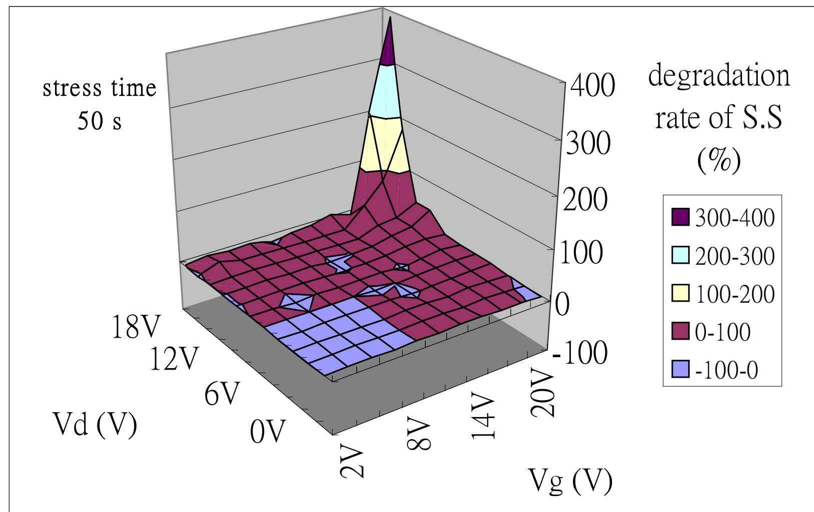


Fig. 4-4 (b) The degradation behaviors of S.S under the stress time of 50 sec

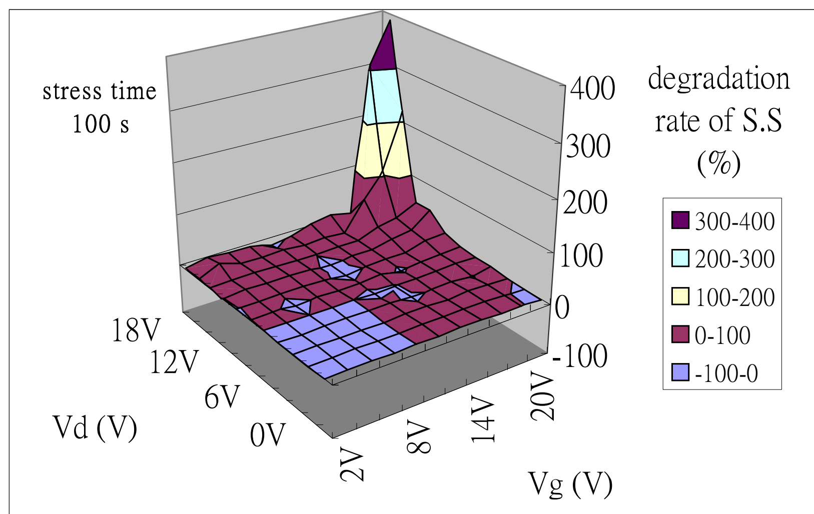


Fig. 4-4 (c) The degradation behaviors of S.S under the stress time of 100 sec

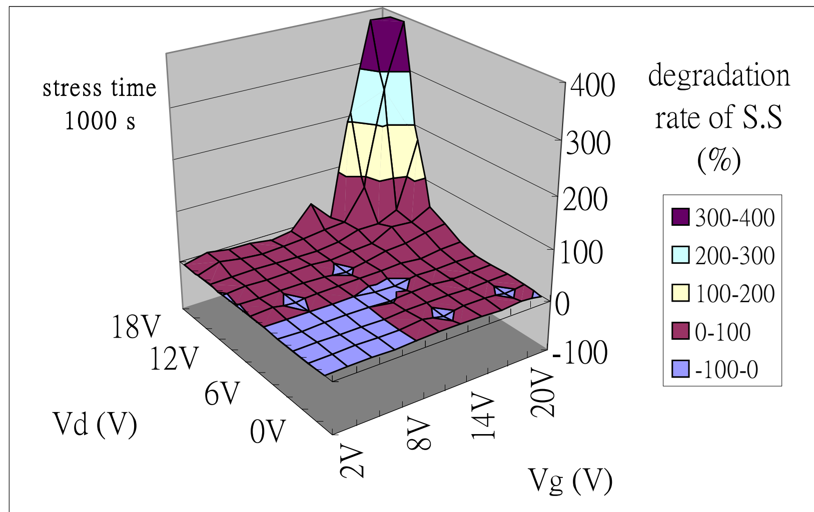


Fig. 4-4 (d) The degradation behaviors of S.S under the stress time of 1000 sec

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碩士班論文題目：

N 型低溫多晶矽薄膜電晶體元件特性及可靠度之統計性研究

(Statistical Study on the Characteristics and Reliability Behaviors of N-type LTPS TFTs)