Chapter 1

Introduction

1.1 Background and development of OTFTs

In 2000 the Nobel Prize in chemistry was awarded for the development of conducting polymers. After Shirakawa began the research on the conducting property of polymers in late 1970s[1], the first demonstration of organic thin-film transistors (OTFTs) based on polyacetylene was reported in 1983[2], but the mobility is quite low, on the order of $10^{-5}cm^2/Vs$. The conductivity of the polymer can be altered from insulator to conductor through the method of doping. The possibility of fabricating OTFTs with small conjugated molecules was shown in 1989[3] with sex thiophene rings linked at alpha positions, showed mobility on the order of $10^{-1}cm^2/Vs$, which has reached the requirement for displays and is comparable to that of amorphous-Si TFTs. The comparisons between amorphous-Si TFTs, poly-Si TFTs and OTFTs are listed in Table1.1[4].

Nowadays, a large number of conjugated molecules and polymers have been used to be the active material of OTFTs. The most significant parameter distinguishing those devices is the technique used for deposition. Organic semiconductors are potentially soluble in organic solvent and are therefore amenable to deposit at low temperatures on plastic substrates. Using low cost fabrication techniques such as spin-coating and inkjet-printing can avoid the complex vacuum evaporation system.

Since organic semiconductors can be processed at low temperatures and are compatible with plastic substrates, OTFTs may be used in applications requiring structural flexibility, large-area coverage, and especially low cost in fabrication. Such applications include active-matrix liquid crystal displays (AMLCDs), active-matrix organic light-emitting diodes

(AMOLEDs), and electronic paper displays. Additionally, organic sensors, organic solar cells, low-end smart card, radio-frequency identification (RFID) tags, and other electronic elements consisting of organic integrated circuits have been proposed.

The bonding between organic semiconductors is by van der Waals forces between the hydrogen atoms, which are dangling on the ends of the benzene rings. It is much weaker than that of the covalent force in inorganic materials, which is the reason for small mobility. In Fig. 1.1[5], we can compare the increase of mobility in the past years for different organic semiconductors. If we want to exceed the limitation of the materials, there are several points we have to notice. First, the injection from the contact electrode has to be optimized. Second, the fabrication parameters such as the deposition conditions have to be optimized to get the best molecular ordering and morphology. And third, synthesis of new materials provides more opportunities to various kinds of applications.

While currently researches on OTFTs still focus on p-type semiconductors, the development of n-type semiconductors is expected and under investigation, shown in Fig. 1.2[6]. The reliability, stability, and reproducibility are also important. There is still room for the fabrication technique to improve, and the choices of materials for the electrode, the insulator layer, even the substrate are also important issues. Finally, the interface treatment is an effective method for improving the characteristics of the device.

Table 1.1: Comparisons of TFTs using different materials for the channel region.

	Amorphous Si	Poly-Si	Organic
Status	Mature	Development	Research
TFT type	N-TFT	N-TFT or P-TFT	P-TFT or N-TFT
Mobility (cm^2/Vs)	0.1-1.0	50-200	0.005-3
Uniformity	Good	Poor	Unknown
Stability	Poor	Good	Unknown
Cost	Low	High	Very low
Ion/Ioff	$>10^6$	$>10^6$	10^3-10^8
Size and voltage to drive 10μA (Gate dielectric is 300nm and channel length is 5μm) (W=channel width)	W=92μm (V_{GS}-V_{TH})=7V	W=10μm (V_{GS}-V_{TH})=1.5V	W=181μm (V_{GS}-V_{TH})=25V

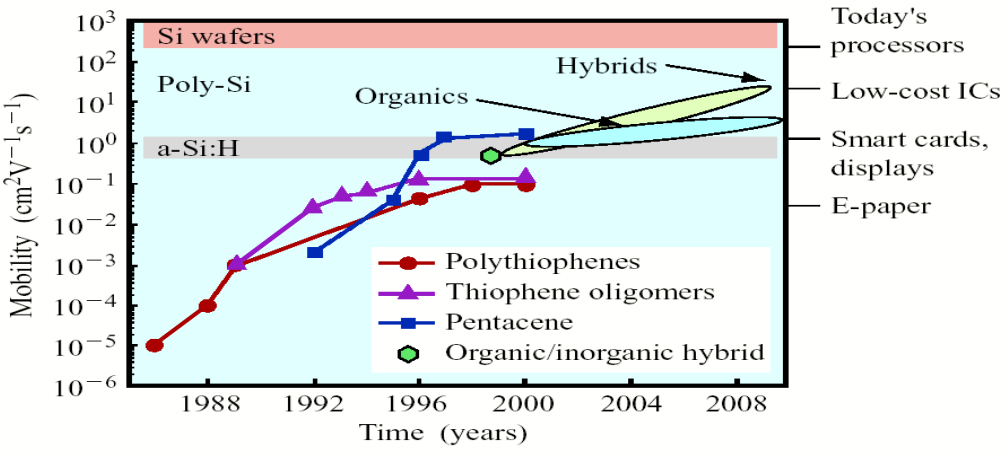


Fig. 1.1 The mobility of the organic semiconductors has been improved by five orders of magnitude over the past 15 years.

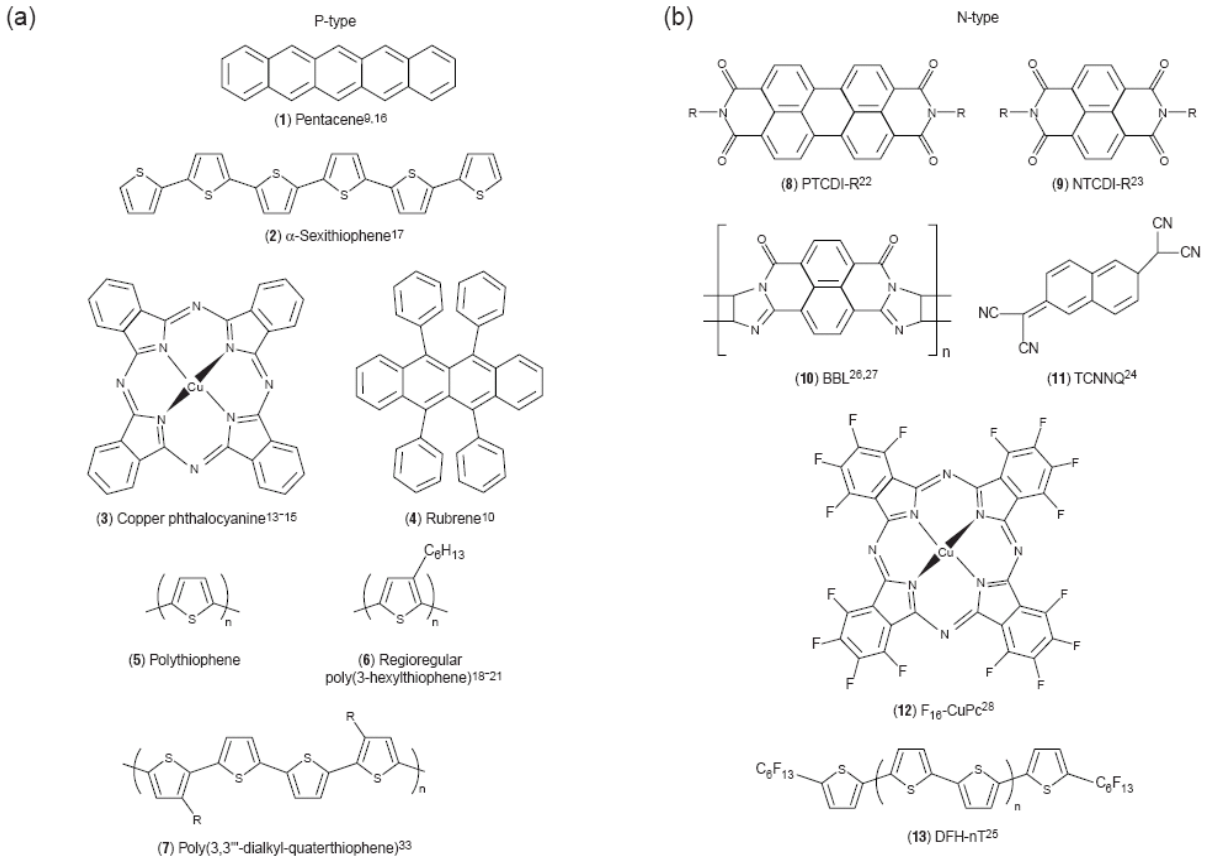


Fig. 1.2 Prominent (a) p-type and (b) n-type organic semiconductor materials.

1.2 Motivation

OTFTs have received much attention recently because they can be fabricated in large scale at low temperatures on plastic substrates with low cost. Among them, pentacene-based TFTs have the most promising electrical performances[7, 8]. Their mobility is proven to be comparable to the mobility of amorphous Si TFTs, which means that they are suitable for display applications.

The quality of the pentacene film is very important for devices[9]. The deposition temperature, deposition pressure, deposition rate, and the film thickness are the parameters determining the characteristics of the organic film. The carrier transport path occurs in the

channel region between the organic semiconductor and the insulator. We can observe the morphology of the grain from AFM images. The transportation of carrier is limited by the grain boundaries. The traps in the grain boundaries generally decrease the conductivity, and the larger grain size is expected to get better characteristics. We choose different pentacene film thicknesses to discuss the relationship between the electrical characteristics and the film thicknesses.

The carrier injection in OTFTs is usually influenced by the contact. The carriers have to overcome the barrier between the contact electrode and organic semiconductor. We can extract the effect of contact resistance from the dependence between the general current equation in the linear region and the channel length. After excluding the effect of contact resistance, the discussions about what happened in the channel region are more reasonable.

There are many investigations on improving the performance of OTFTs. The most effective technique is surface treatment. It can improve the molecule ordering and the flatness of the interface. There are several kinds of materials used for surface treatments and the improvement is obvious.

The carrier transportation is still under investigation. And the mobility is believed to be gate-voltage and temperature dependent. Based on the assumption of thermal activated transportation, the relation between the mobility and the temperature can be figured out from the measurements at different temperatures. Since there is a large concentration of traps inside the organic semiconductor and around the contacts, the dependence on temperature may be disturbed. We can still find out the relationship between the gate voltage and the activation energy to check the grain boundary barrier model. This may be helpful as we discuss the transportation mechanism of OTFTs.

1.3 Organization of this thesis

In Chapter 1, we describe the background of OTFTs and motivation of the thesis. In Chapter 2, we introduce the characteristics of the organic materials, operation of OTFTs, and parameters extractions. In Chapter 3, the fabrication and structure of OTFTs are presented. Different pentacene film thicknesses, thermal characteristics, contact resistance, and surface treatment are investigated. Finally, we will provide conclusions in Chapter 4.

Chapter 2

Properties of Organic Thin Film Transistors

2.1 Characteristics of the organic materials

Organic conjugated materials used in OTFTs can be generally sorted into polymers and small molecules. They exhibit contiguous sequences of double bonds separated by one single bond. The π orbital in the conjugated system is linked with the neighboring π orbital, and spreads in the whole molecule. The π electrons are delocalized across the molecule, which makes semiconducting or conductive characteristics of the conjugated system. Not like the case in inorganic semiconductors, the carrier transport is band-like transport which is determined by the Bloch wave states. Carrier transport is via hopping between localized states in disordered organic semiconductors.

Mobility is the most important parameter when we mention about OTFTs. The localized wave functions in organic semiconductors lead to small inter-molecular interactions, typically the van der Waals or weak π-π overlap. That is the main cause of the low mobility. But it can be improved by modifying the materials and device architectures. Pentacene is one of the most widely-used materials in OTFTs. Its mobility has reached the fundamental limit (> $3cm^2/Vs$)[10, 11] which is obtained with a single crystal at room temperature. Organic semiconductors are soluble in organic solvents or vaporizable at low temperatures due to such small inter-molecular interactions. This implies that there may be a trade-off between the mobility and processability in organic semiconductors of OTFTs. The mobility of organic semiconductors ranged from 10^{-3} to 10^{0} cm^2/Vs is comparable to that of amorphous silicon which is widely developed and used in active matrix liquid crystal displays.

2.1.1 Polymers

Conjugated polymers are more suitable than small molecules for solution processability due to their high viscosity. However, the mobility of conjugated polymer is generally smaller than that of small molecule semiconductors for the more random orientation of molecular units or relatively short conjugated length in polymer backbones. The mobility as high as 0.1cm^2/Vs has been achieved with regioregular head-to-tail poly(3-hexylthiophene)[12]. More recently, it has been shown that the mobility can be raised to 0.2cm^2/Vs when the polymer film is applied by dip-coating to a thickness of only 2-4nm[13]. Polymer-based TFTs offer the advantage of inkjet printing or spin-coating, but the purity defects in material may give rise to charge-trapping sites, which in turn decreases the mobility.

2.1.2 Small molecules

Since the spin-coated polymer is disordered in structure, the structure of thermal evaporated small molecule is well ordered. Small molecules can be classified into linear fused ring compounds, 2-D fused ring compounds, oligomers, and 3-D molecules.

Most organic materials tend to transport holes better than electrons. This is because p-type semiconductors are more stable in air and larger mobility is obtained in OTFTs. Most n-type organic semiconductors are sensitive to air and moisture due to the organic anions. Particularly, the carbanions can easily react with oxygen and water under operating conditions, which causes the low mobility of n-type organic semiconductors.

In our experiments, we choose pentacene as material of the semiconductor region. The largest mobility and stability make pantacene the most expected candidate.

Pentacene is an aromatic compound with five condensed benzene rings and therefore, the chemical formula is $C_{22}H_{14}$ with molecular weight 278.3. The volume of the unit cell is about 705Å^3. The permittivity is 4[14], and the electron affinity is about 2.49eV. Silinish et al.

determined the adiabatic energy gap (E_G^{Ad}) by using the threshold function of intrinsic photoconductivity of pentacene[7]. The second transition is from the excited state to the ionic state, which is called the optical energy gap (E_G^{Opt}). According to Fig. 2.1, the adiabatic energy gap as 2.47eV and the optical energy gap as 2.83eV are reported[15].

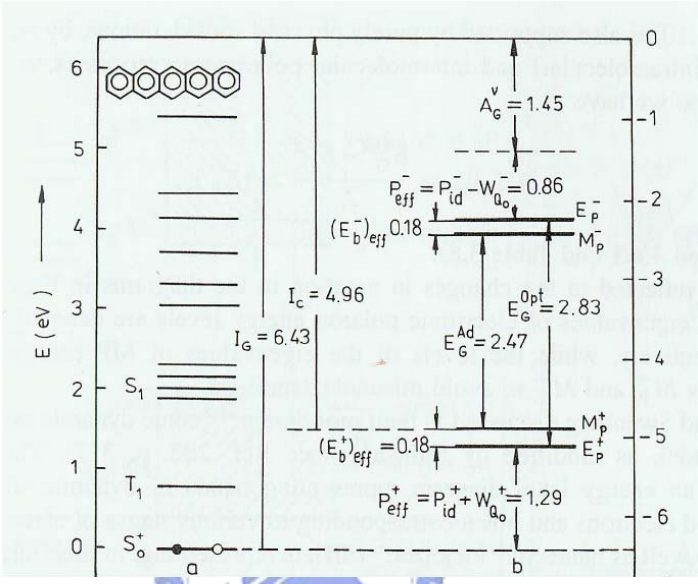


Fig. 2.1 The energy band diagram of pentacene. The optical energy gap and adiabatic energy gap are determined.

2.2 Operation of OTFTs

The general operation concept of p-type pentacene-based OTFTs comes from inorganic TFTs. The MOSFET is traditionally operated in inversion mode. However, the operation of OTFTs is generally in accumulation mode. The typical I-V characteristics can be used to calculate important parameters such as mobility, threshold voltage, and on/off current ratio.

Since pentacene is a p-type semiconductor. First, a negative bias is applied to the gate, the voltage drops over the insulator and semiconductor regions, which gives rise to band bending in the semiconductor. The additional positive charges provided by the source and

drain electrodes accumulate charges in this region. The insulator serves as a capacitance which stores charges and can be represented as C_{OX}. It is assumed that a little voltage drop across the semiconductor is negligible. In this situation, the applied drain bias can direct the current from source to drain. The conduction is determined by mobility μ which represents how the electrical field drives the accumulated charges. Therefore, the increased gate voltage δV_G accounts for the increased charges $C_{OX}\delta V_G$ and the total charges increased over the channel are $WLC_{OX}\delta V_G$, where W and L correspond to the channel width and length. The increased drain current δI_D is then represented as

$$\delta I_D \approx \frac{W}{L}\mu C_{OX} V_D \delta V_G \tag{2.1}$$

In general, we can divide the operation of OTFTs into two regions, linear and saturation regions. The drain current in the linear region is determined from the following equation

$$I_D = \frac{W}{L} C_{OX}\mu(V_G - V_{TH} - \frac{V_D}{2})V_D \tag{2.2}$$

Since the drain voltage is quite small, sometimes equation (2.2) can be simplified as

$$I_D = \frac{W}{L} C_{OX}\mu(V_G - V_{TH})V_D \tag{2.3}$$

For $-V_D > -(V_G - V_{TH})$, I_D tends to saturate due to the pinch-off of the accumulation layer. The current equation is modified as

$$I_D = \frac{W}{2L} C_{OX}\mu(V_G - V_{TH})^2 \tag{2.4}$$

The energy band diagrams for p-type and n-type OTFTs are shown in Fig. 2.2.

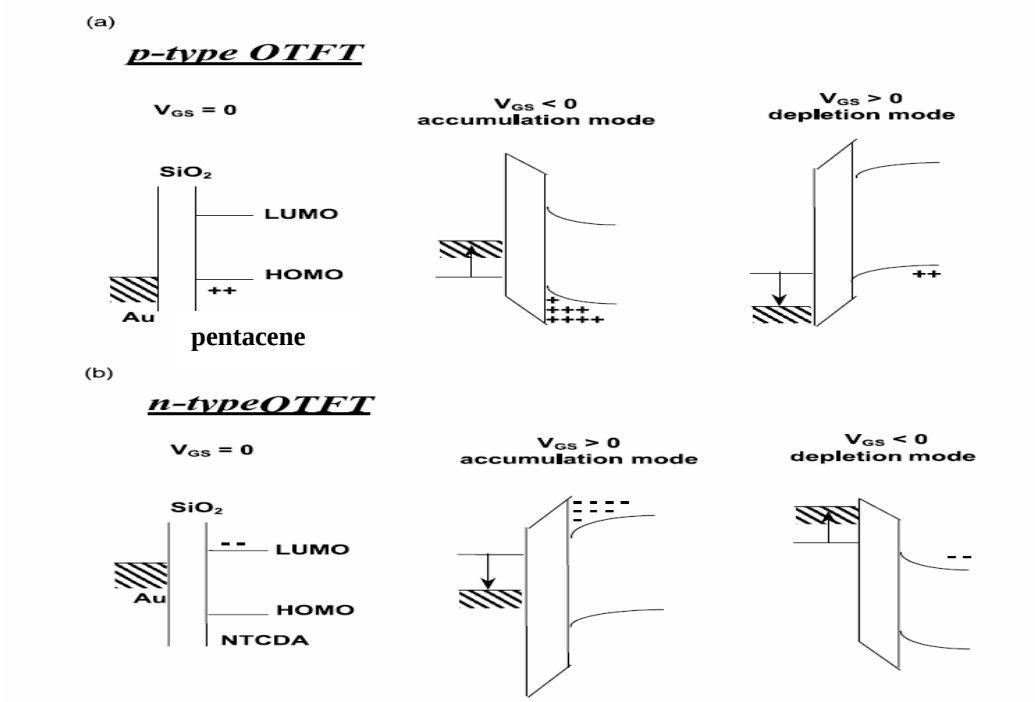


Fig. 2.2 Energy band diagrams (a) for a p-channel (pentacene) and (b) for a n-channel (NTCDA) OTFT. The left side shows the devices at zero gate bias, while in the centre and in the right parts the accumulation and depletion mode operation regimes are presented[16].

2.3 Transportation mechanisms

2.3.1 Band like transport

Multiple trapping and release (MTR) model assumes that most of the carriers injected in the semiconductor are trapped in states localized in the forbidden gap. MTR model is widely used in amorphous Si TFTs[17, 18] and explains reasonably well the observed characteristics in vapor-deposited polycrystalline pentacene films. The model assumes that the intrinsic charge transport mechanism is the one involving extended states, and a distribution of traps exists in the forbidden gap above the valence-band edge. At low gate biases, most of the holes injected in the semiconductor are trapped into these localized states. The deepest traps are first filled and carriers can be thermally released. As the negative gate bias increases in p-type materials,

the Fermi level approaches the valence-band edge and more traps are filled. At an appropriately high gate voltage, all trap states are filled and subsequently injected carriers move with the microscopic mobility in the delocalized (valence) band[19, 20]. Several trap levels have been reported for polycrystalline vapor-deposited pentacene films at depths ranging from 0.06eV to 0.68eV[21], which can account for the MTR model. Traps are sometimes caused from the impurities and structure defects in the crystalline pentacene film which include point defects, dislocations, and most importantly, the grain boundaries[22]. The concept of grain boundaries has been used to explain the gate-voltage dependence of mobility in polycrystalline oligothiophene films[23, 24]. The energy barrier created in the grain boundaries is a function of trapped charge states, carrier concentration within the grains, and temperature.

At high temperatures, the charge transport is dominated by the thermionic emission over the potential barrier at grain boundaries. At low temperatures, the carrier transport is dominated by tunneling. However, mobility in molecular crystal is still moderate at very low temperatures. The corresponding mean free path does not exceed the inter-molecular distance, which is not physically acceptable for a diffusion-limited transport. Polaron models have been proposed to rationalize the discrepancy[25]. In spite of the recent efforts, the best explanation and exact phenomenon describing the carrier transport in molecular crystals are still under investigation.

2.3.2 Hopping

The concept of variable range hopping (VRH)[26] is usually used in amorphous organic transistors, where the carriers transport by hopping: thermally activated carriers tunneling between localized states including percolation, rather than by the activation of carriers to a transport level.

The model describes the conductivity in the polymer as equivalent to transport through a resistor network. The percolation criterion through the network is then related to the temperature, the position of Fermi level, and the width of the exponential tail of the density of states (DOS).

A carrier may either hop over a small distance with high activation energy or hop over a long distance with low activation energy. As the accumulated charges fill the lower-lying states, any additional charges will occupy states with relatively higher energy. Therefore, these additional charges just need less energy to hop away to neighboring sites, and the mobility will rise as the gate voltage increases.

2.4 Parameters extraction

In this section, we introduce the methods for the extraction of mobility, threshold voltage, and on/off current ratio.

2.4.1 Mobility

Generally, mobility can be extracted from the transconductance g_m in the linear region:

$$g_m = \left[\frac{\partial I_D}{\partial V_G}\right]_{V_D=\text{constant}} = \frac{WC_{OX}}{L}\mu V_D \qquad (2.5)$$

Mobility can also be extracted from the slope of the curve of the square-root of drain current versus gate voltage in the saturation region, i.e. $-V_D > -(V_G - V_{TH})$:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu C_{OX}}\,(V_G - V_{TH}) \qquad (2.6)$$

2.4.2 Threshold voltage

Threshold voltage is related to the operation voltage and the power consumptions of an OTFT. Many researches on OTFTs are suffered from the large threshold voltage. Threshold

voltage is influenced by the ratio of the mobile and trapped carriers at the interface between the organic semiconductor layer and insulator. There are also researches on lowering the threshold voltage by adjusting the insulator layer[27]. In our experiments, we extract the threshold voltage from equation (2.6), the intersection point of the square-root of drain current versus gate voltage when the device is in saturation mode operation.

2.4.3 On/Off current ratio

Devices with high on/off current ratio represent large turn-on current and small off current. It determines the gray-level switching of the displays. High on/off current ratio means there are enough turn-on current to drive the pixel and sufficiently low off current when the device is turned off.

Chapter 3

Device Fabrication and Experiments Results

The devices used in this series of experiments come from ERSO and NCTU. Both kinds of devices are the bottom contact (BC) structure, which means the organic semiconductor layer is deposited on the top of the contact electrodes. There are some things differences between the two devices. The substrate materials are glass and Si, and the source and drain contact electrodes are ITO and Pd/Ti for the two devices, respectively. Differences in the fabrication techniques and variations in processes also have influences on the results.

3.1 Device structures and fabrication

3.1.1 Devices from ERSO

The substrate is glass and the total size of the test sample is 5cm×5cm. The gate electrode is ITO with thickness 1000Å, and the insulator layer is PECVD-deposited silicon dioxide with thickness 3000Å. Source and drain are made of 1000Å-thick ITO are deposited by sputtering. Pentacene serves as the active semiconductor region and is thermal evaporated. The deposition rate, deposition temperature, and deposition pressure are 1Å/s, 70^{o}C, and 1.1×10^{-5} torr, respectively.

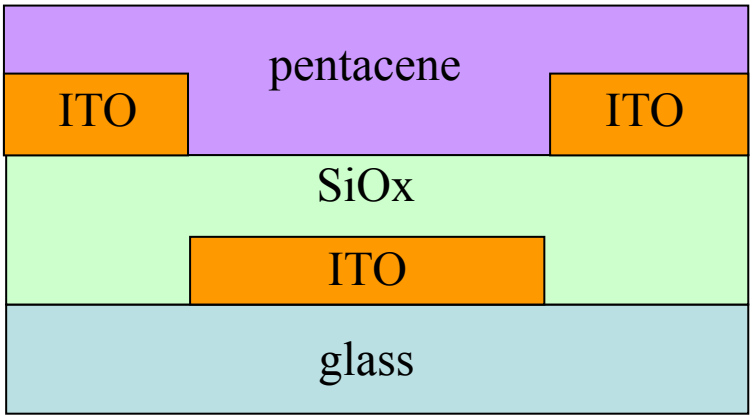


Fig. 3.1 Schematic structure of devices from ERSO.

3.1.2 Devices from NCTU

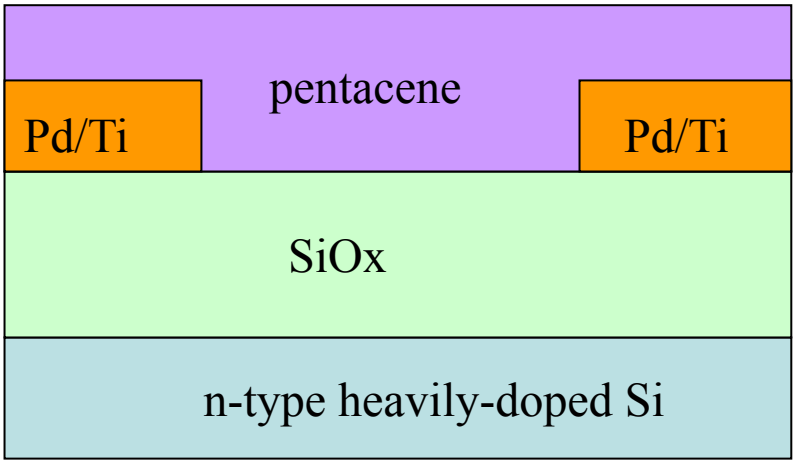


Fig. 3.2 Schematic structure of devices from NCTU.

Step1. Substrate and gate electrode

4-inch n-type heavily-doped single crystal silicon wafer with (100) orientation is used as substrate and gate electrode.

Step2. Gate oxide formation

After the initial RCA cleaning, the gate oxide layer is formed in furnace. Thermally grown oxide is the best choice for the insulator layer. The thickness is 2000Å.

Step3. Pd/Ti deposition

The injection barrier of the OTFT device is determined by the materials of the source and drain electrodes. Materials with large work function are preferred to form Ohmic contact. The source and drain of the device are Pd/Ti. Pd with work function 5.1eV does help to provide a better injection, and Ti can improve the adhesion between Pd and the oxide layer. Pd/Ti are deposited by dual E-gun EBX-10C at deposition pressure 3×10^{-6} torr. The thicknesses of the Pd and Ti layer are 1000Å and 10Å, respectively.

Step4. Source/Drain definition

After the formation of the Pd/Ti layers, the source and drain electrodes are defined by photolithography.

The photoresist FH-6400 is spin-coated with 1000 rpm for 10 seconds followed by 4000rpm for 40 seconds and then soft-baked at 90^{o}C for 1 minute.

The exposure energy and exposure time are 300W and 50 seconds. And then, the device is developed by FHD-5. After rinsed with water, hard bake of 3 minutes at 120^{o}C is used to expel the solvent inside the photoresist.

After pattern definition, the Pd/Ti layers are etched by aqua regia. Finally, photoresist is stripped by acetone.

Step5. Pentacene film deposition through shadow mask

It is well known that the deposition temperature, deposition pressure, and deposition rate are the three critical parameters to the quality of the organic film. The deposition is started at a pressure lower than 3×10^{-6} torr. The deposition rate is controlled at 0.5Å/s. Slower deposition rate is expected to result in smoother and better ordering of the organic molecules. The deposition temperature is also a factor influencing the pentacene film formation. The temperature we use in depositing pentacene films is 70^{o}C. We use shadow mask to define the active region of each device.

In section 3.2, 3.3, and 3.4, we investigate different pentacene film thicknesses, different measurement temperatures, and contact resistance with devices from ERSO. In section 3.5, we discuss the effect of surface treatment for the devices we fabricated in NCTU.

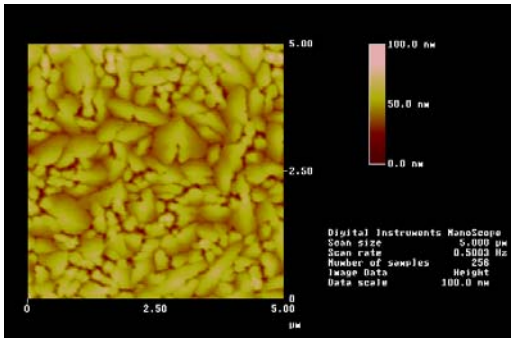
3.2 Different pentacene film thicknesses

3.2.1 AFM images

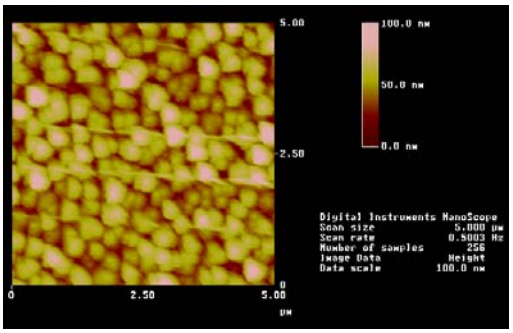
In the AFM images, we can observe the size of the grain. In this part of experiments, the devices are provided by ERSO. In Fig. 3.3, the substrate is Si wafer and the pentacene film thicknesses are 1000Å, 3000Å, 4000Å, and 5000Å. The difference in grain size is not obvious, but the 1000Å one seems a little larger than others. The smoothest case also occurs when the thickness is 1000Å.

Grain size is believed to be related to transport property[28, 29]. As mentioned previously, carrier transportation in the channel region is limited by the grain boundaries. Larger grain size represents less grain boundaries. In this experiment, we find that the dependence of film thickness on grain size is not obvious. We should also mention that the critical region is the interface between the insulator layer and the organic semiconductor layer. The AFM images just reveal the top morphology of the pentacene film. Therefore, what actually matters can not be directly observed by this method. Experiments such as scanning Kelvin probe microscopy, for example, can provide the potential difference in the channel region[30,31].

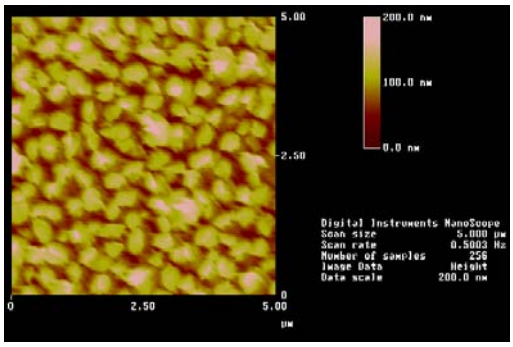
According to electrical characteristics, the drain current is very small when the film thickness is over 3000Å. The effective channel thickness for carrier transport is just monolayer. More traps in thicker film may not be helpful for carrier transportation.



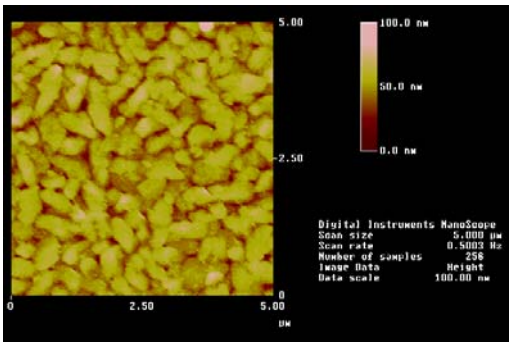
(a) 1000Å



(b) 3000Å



(c) 4000Å



(d) 5000Å

Fig. 3.3 AFM images of different thickness pentacnene films deposited on Si. From (a) to (d) are 1000, 3000, 4000, and 5000 Å, respectively.

3.2.2 XRD

First, we compare X ray diffraction (XRD) results for different film thicknesses. The intensity of the peak represents the film quality. In Fig 3.4, the larger intensity of the 1000Å film corresponds to better electrical performances when used in devices. The well-defined X-ray diffraction corresponds to (001) reflections with a d-spacing about 15.4Å, which corresponds to a crystalline structure with the long axis of the pentacene molecules being almost perpendicular to the substrate surface[32,33]. The structure of this thin film is different from the single crystal of pentacene molecules.

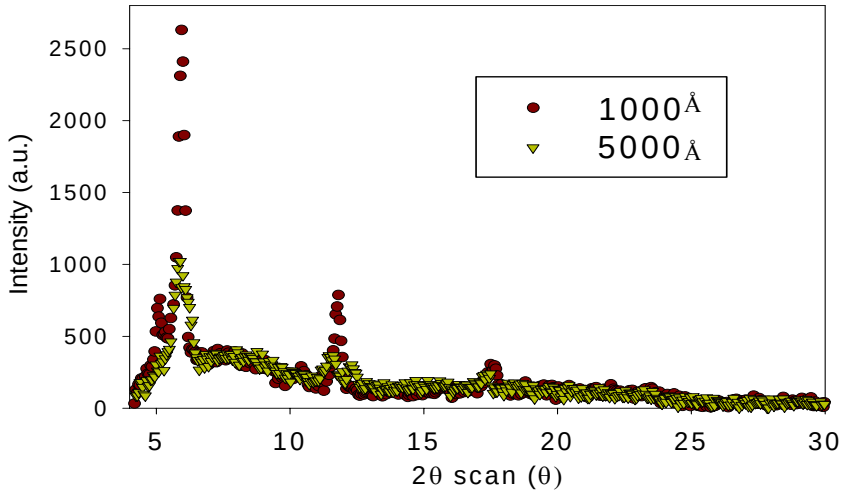


Fig. 3.4 XRD measurements of pnetacene films with thicknesses 1000 Å and 5000 Å.

3.2.3 Electrical characteristics

In this series of experiments, we compare devices with different pentacene film thicknesses. The channel width is 500μm and length is 10~50μm. In Fig. 3.5 for I_D-V_D measurements, we provide the drain voltage from 0 to -50V and change the gate voltage from 0 to -50V, step by -10V. The I_D-V_D curves show the turn-on operation of the device. We can observe that the turn-on current is largest in the 1000Å-thick device. For devices with thicker film, 3000Å and 4000Å, the drain currents are much smaller, and the degradation is very serious, which means that the film quality is worse. As for the thinner film, device with 500Å-thick film is not as good as the one with 1000Å-thick film. The maximum drain currents for devices with different pentacene film thicknesses are listed in Table 3.1.

In Fig. 3.6 for I_D-V_G characteristics, the gate bias ranged from 20 to -50V, and the drain voltage -40V are provided for the device with 1000Å-thick film. We can also compare devices with different pentacne film thicknesses. From the I_D-V_G data, we can extract the mobility and threshold voltage from the square-root of drain current versus gate voltage curves and the results are shown in Fig. 3.7 and Fig. 3.8. Both the mobility of 0.0023cm^2/Vs and threshold voltage of -19V are the best for the 1000Å–thick device.

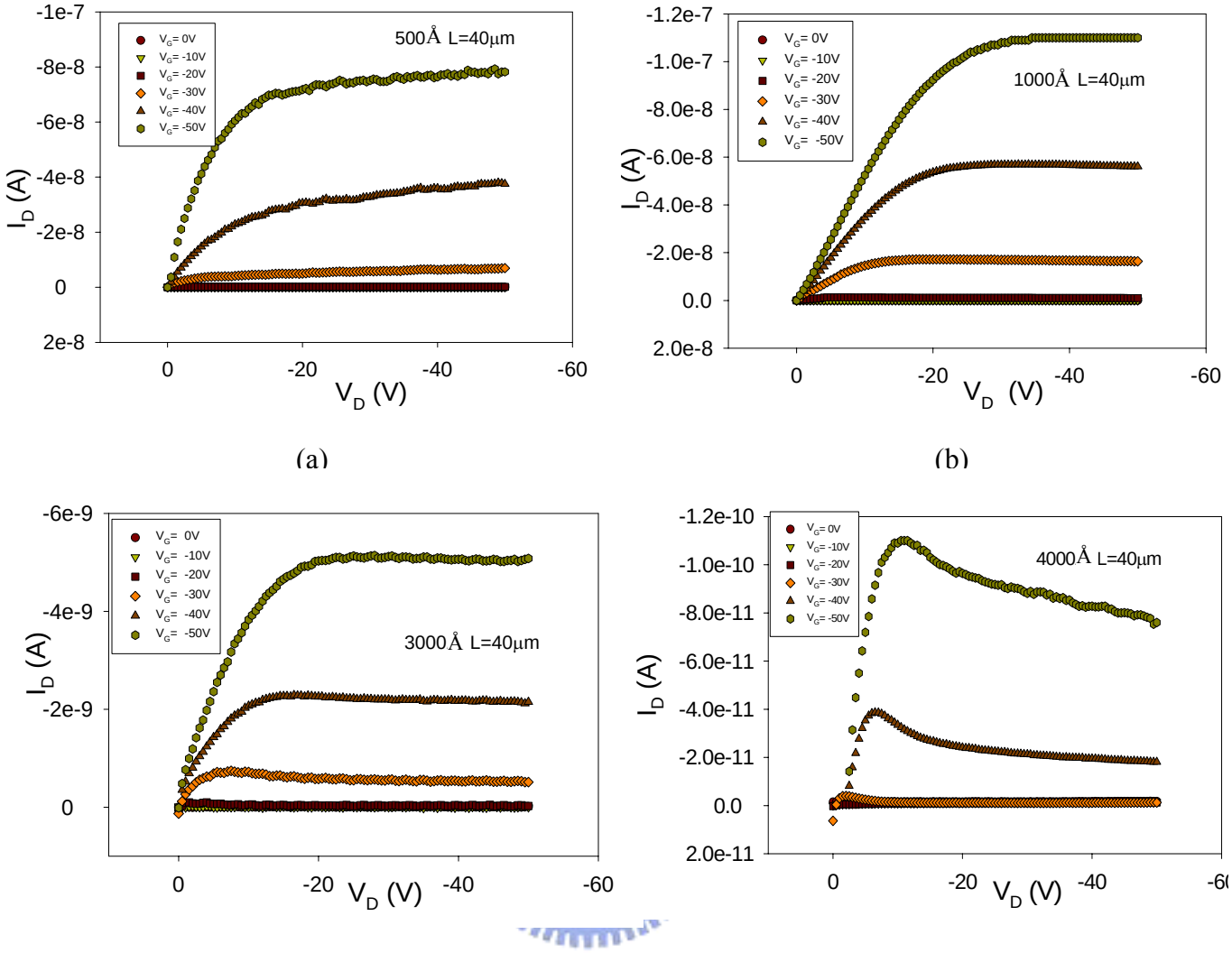


Fig. 3.5 I_D-V_D curves for different pentacene film thicknesses, (a) 500Å, (b) 1000Å, (c) 3000Å, and (d) 4000 Å. The gate voltages are provided from 0 to -50V. The channel width and length are 500μm and 40μm.

Table 3.1 List of the maximum drain currents for devices with different pentacene film thicknesses.

Thickness (Å)	Drain current (max) (A)
500	7.8E-08
1000	1.1E-07
3000	5.1E-09
4000	1.1E-10

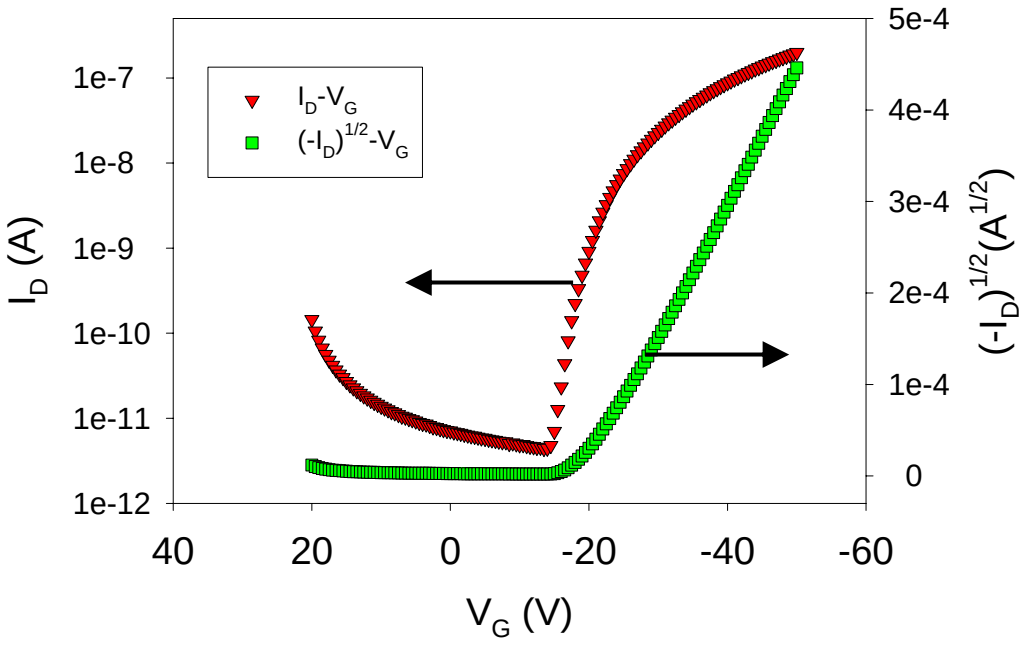


Fig. 3.6 Transfer characteristic of a 1000Å-thick device. The drain voltage is -40V.

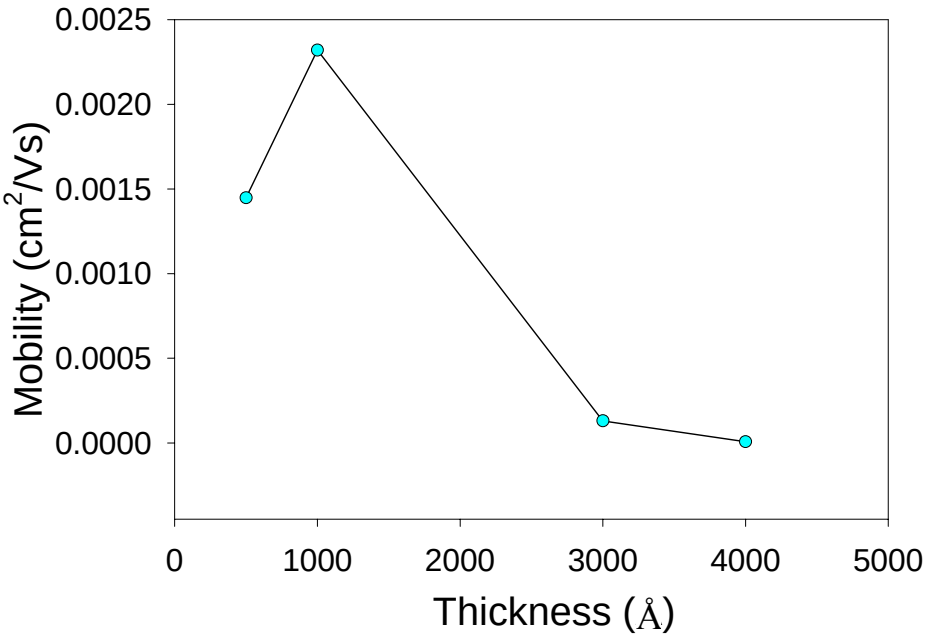


Fig. 3.7 Mobility for devices with pentacene film thicknesses 500, 1000, 3000, and 4000Å.

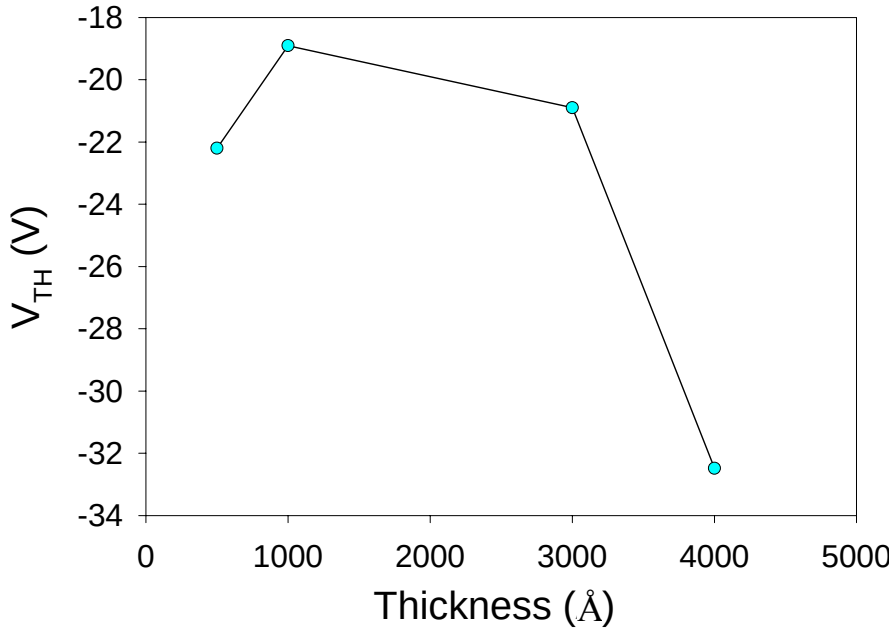


Fig. 3.8 Threshold voltage for devices with pentacene film thicknesses 500, 1000, 3000, and 4000Å.

3.3 Different measurement temperatures

OTFTs need to be operated under different kinds of fields for various applications, however, many organic materials are not heat-resistant[34] and there will be problems when the devices are operated at high temperatures. Measurements of different temperatures[35,36] not only provide us the information for device operation but also help us to understand the transportation mechanism. We change the measurement temperatures from room temperature (25 ^{o}C), 55^{o}C, 85 ^{o}C, to 105 ^{o}C continuously. And every time we raise the temperature, 30 minutes are needed for temperature to be stable. We will discuss the I_D-V_D and I_D-V_G curves in Fig. 3.9 and Fig. 3.13. The comparison about drain current at different temperatures is shown in Fig. 3.10. In Fig. 3.11 and Fig. 3.12, we discuss the phenomenon after the temperature over 85^{o}C.

The device channel length is 40μm. From the I_D-V_D measurements in Fig. 3.9, we observe several interesting phenomenon. The maximum drain current at a fixed V_G increases as the substrate temperature rises. For example, the maximum drain currents for substrate temperatures 25°C, 55°C, 85°C, and 105°C at V_G = -50V are 1.10×10^{-7}A, 1.84×10^{-7}A, 2.03×10^{-7}A, and 1.38×10^{-7}A, respectively. This is because mobility increases as the substrate temperature rises before T = 85^{o}C. At V_D = -40 V, the mobility for substrate temperatures of 25°C, 55°C, 85°C and 105°C are 0.00230, 0.00397, 0.00551, and 0.00534 cm^2/Vs, respectively. This also implies that the potential barrier height at the grain boundary is lowered when the substrate temperature rises.

For substrate temperatures at 85°C and 105°C, the degree of increase of the saturated drain current with increased gate voltage does not follow the current equation in saturation region. In the I_D-V_D curves, we can also observe the self-heating effect for substrate temperatures at 85°C and 105°C. The drain current dropped after it reached a maximum

saturation value as V_D continues to increase. The higher the substrate temperature and the larger the gate voltage, the more severe this effect becomes. There are two transport mechanisms involved. At first, the grain boundaries act as trap sites and thermally-activated transport process dominates. As a result, mobility increases with increasing temperature. Above certain temperature, scattering effect starts to affect the saturation characteristics as we increase V_G. Inside each grain the lattice vibrations cause strong scattering, and hence reduce I_D and cause serious self-heating effect.

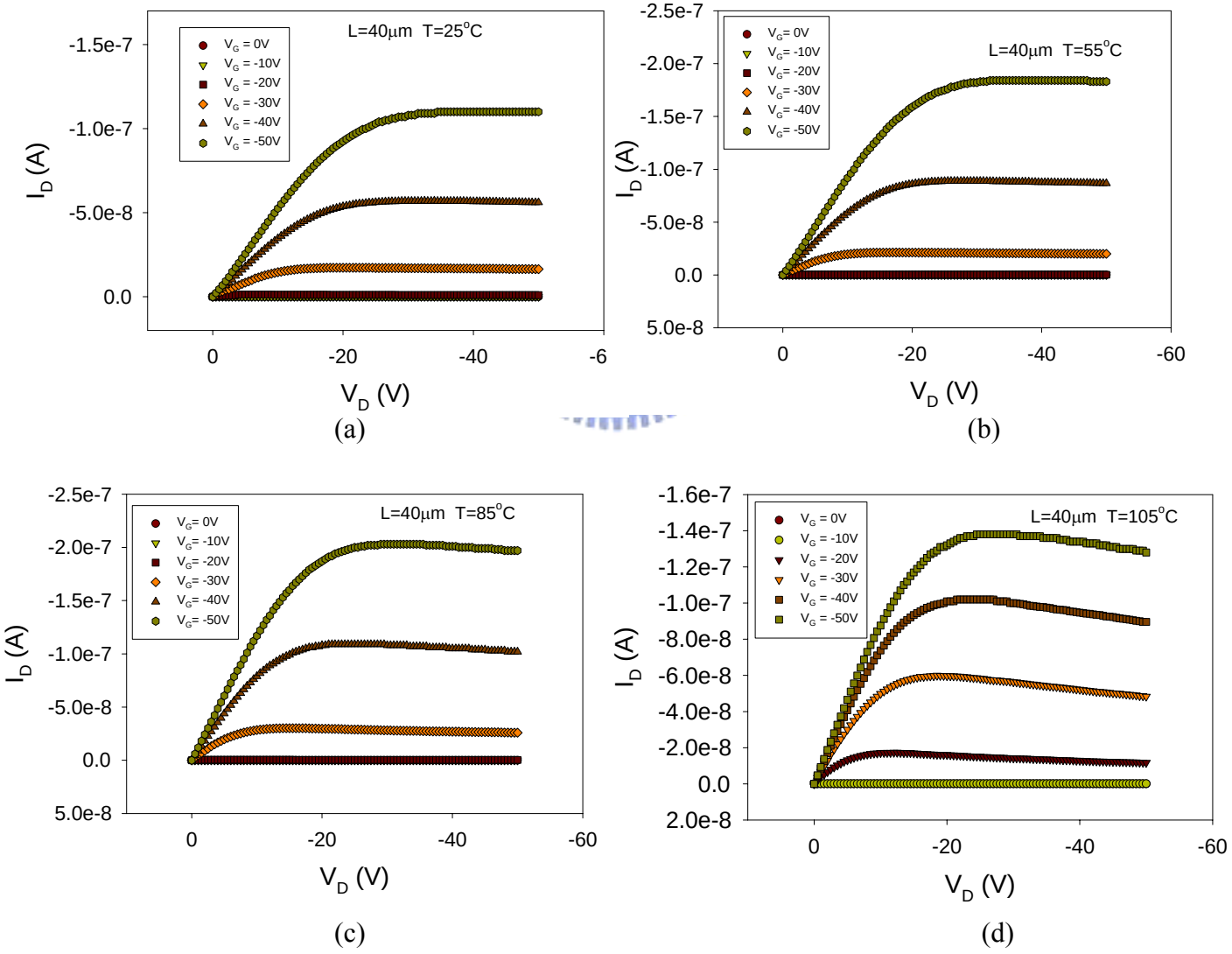


Fig. 3.9 I_D-V_D curves for devices under different measurement temperatures (a) 25°C, (b) 55°C, (c) 85°C, and (d) 105°C. The gate voltages are from 0 to -50V. The channel width and length are 500μm and 40μm.

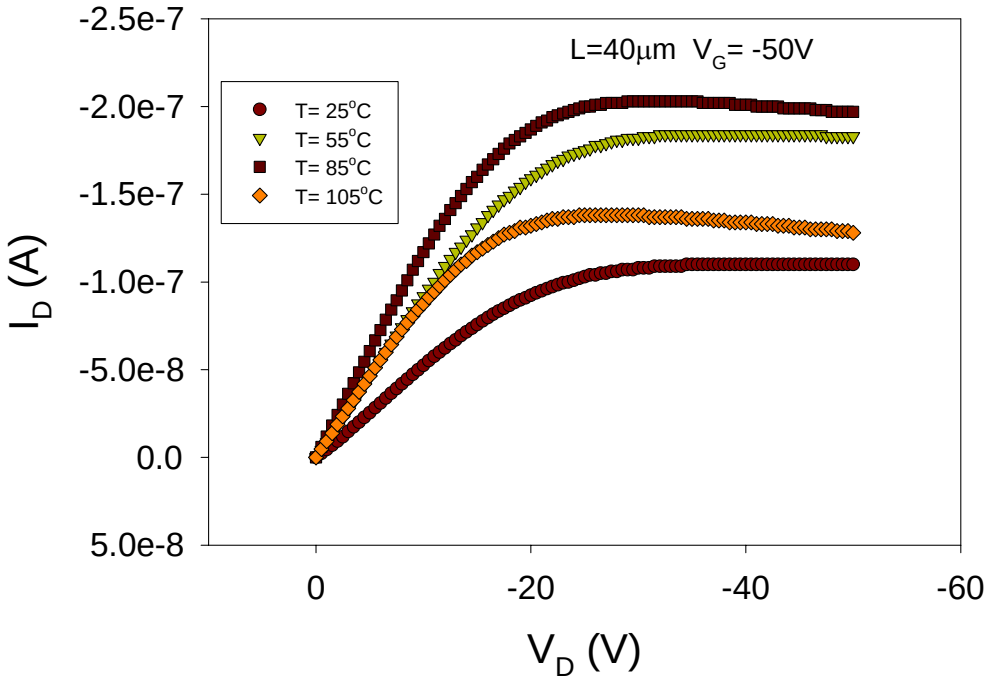


Fig. 3.10 I_D-V_D curves for measurement temperatures at 25, 55, 85, and 105°C. The channel width and length are 500μm and 40μm.

The drain current decreases as increasing the drain voltage beyond certain value when the temperature is above 85°C. We define the degree of drain current degradation after the drain current reaches maximum value associated to the drain voltage at a fixed gate voltage $\left.\frac{\partial I_D}{\partial V_D}\right|_{V_G}$ in order to describe the behavior of this self-heating effect. The phenomenon of the current degradation is more serious when the temperature is higher. We can also observe in the Fig. 3.11 that the value of difference is larger when T = 105°C, which means the self-heating effect is more serious, and the difference between T = 85°C and T = 105°C gets smaller as the gate voltage increases.

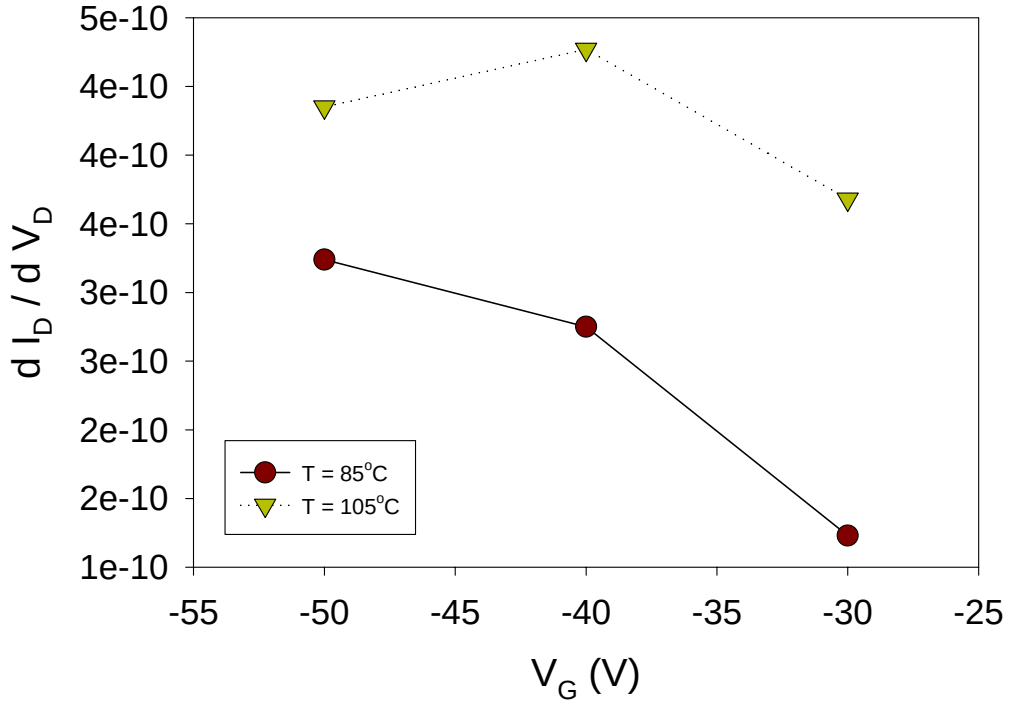


Fig. 3.11 $\left.\frac{\partial I_D}{\partial V_D}\right|_{V_G}$ at three different gate voltages when T = 85°C and T = 105°C. The degradation is larger at T = 105°C.

The relationship between the mobility and the temperature is shown in Fig. 3.12. The mobility increases linearly when the temperature increases from 25°C to 85°C. This means that more carriers are released from the delocalized states.

It should be noted that when the temperature is higher than 85°C, the mobility begins to decrease. The increased temperature leads to higher carrier scattering rate, which tends to limit the increase of field effect mobility at high temperatures.

We can express the relation between the mobility and the temperature into two regions as below:

$$\begin{cases} \mu = \mu_c + \delta(T - T_c), & T < T_C \\ \mu = \mu_c + \delta'(T - T_c), & T > T_C \end{cases} \tag{3.1}$$

We assume that μ_c, δ, and δ' are fitting parameters and T_c is the characteristic temperature. After fitting, we obtain μ_c = 0.0055cm^2/Vs, δ = -5.45×10^{-5}cm^2/KVs, δ' = -4.5×10^{-5}cm2/KVs, and T_C = 85°C.

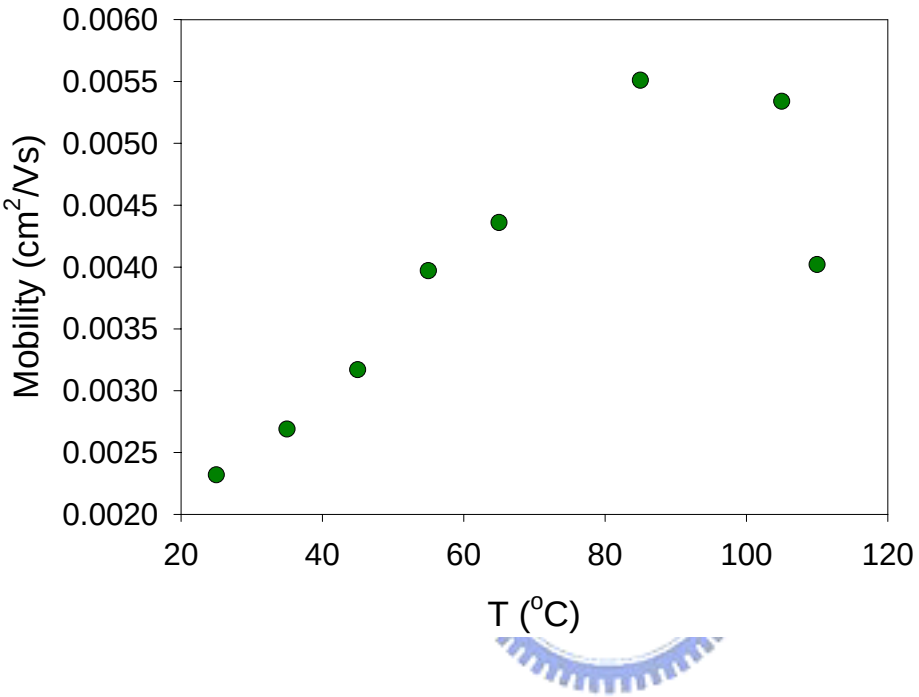


Fig. 3.12 Mobility for T = 25°C, 35°C, 45°C, 55°C, 65°C, 85°C, 105°C, and 110°C at V_D = -40V.

We can also find the mobility for devices with different channel lengths increase with temperature until 85°C and then decrease. As for devices with 3000Å-thick pentacene, the mobility increases before temperature reaches 65°C, after that, the mobility decreases.

In the I_D-V_G measurements, the gate voltage ranges from 20 to -50V and the drain bias is provided from -10 to -50V, step by -10V. The curves are shown in Fig. 3.13. We also compare the I_D-V_D curves when the gate bias is -50V and I_D-V_G curves when drain bias is -40V at temperature 25°C, 55°C, 85°C, and 105°C in Fig. 3.14.

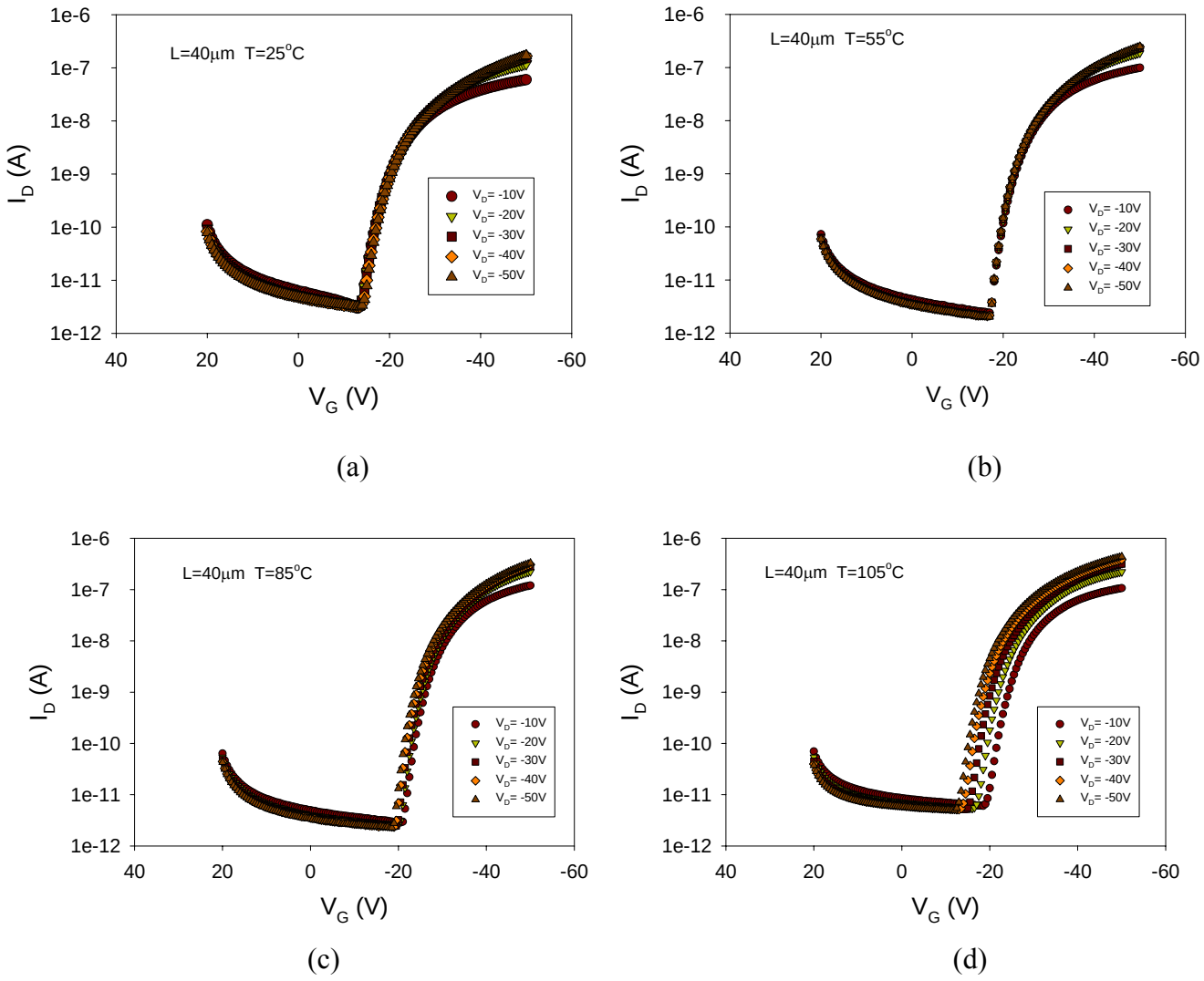


Fig. 3.13 I_D-V_G curves for devices under different measurement temperatures (a) 25°C, (b) 55°C, (c) 85°C, and (d) 105°C. The drain voltages are from -10 to -50V. The channel width and length are 500μm and 40μm.

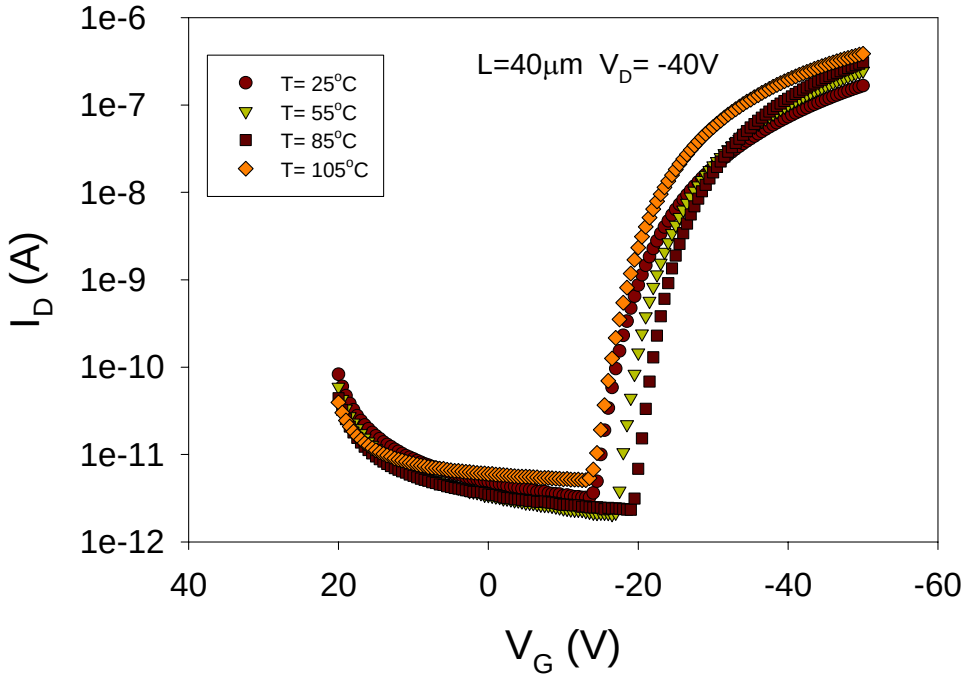


Fig. 3.14 I_D-V_G curves for measurement temperatures at 25, 55, 85, and 105°C. The channel width and length are 500μm and 40μm.

In the poly-Si grain boundary theory, the activation energy E_A is an important parameter as we discuss the fundamental transport mechanism. It's assumed that the traps are concentrated at the grain boundary, and inside the grain, there is trap-free. Increasing the gate voltage is firstly used to fill the traps at the grain boundary. Until the gate voltage is above threshold voltage, the carrier transportation begins. So, as we increase the gate voltage in the above threshold voltage region, the activation energy becomes lower, which means that the transportation is much easier. The same trend can be observed in Fig. 3.15 for our OTFT devices.

For OTFT devices from ERSO, we find in Fig. 3.16 that the order between the activation energy and V_G minus V_{TH} is -0.2 instead of -1 in poly-Si TFTs. As for the devices fabricated in NCTU, the trend that the activation energy decreases with increasing gate voltage above threshold is the same, but the difference in order may correspond to the film quality. So, if we

want to chase the true mechanism, the boundary conditions of the Poisson's equations should be modified. The accumulation mode operation and the film characteristics should be taken into consideration as well.

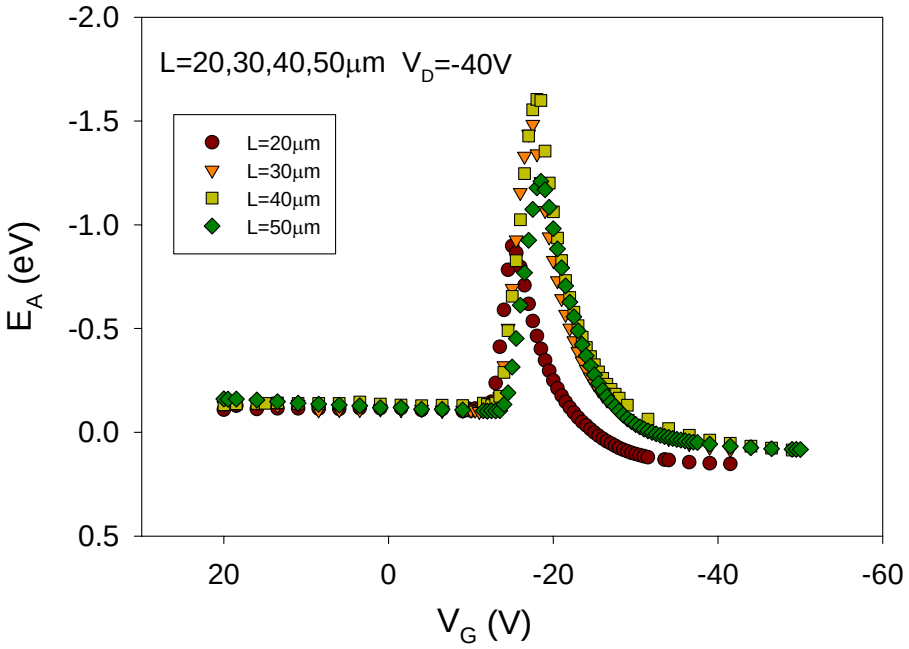


Fig. 3.15 Activation energy versus the gate voltage for device channel lengths 20, 30, 40, and 50μm.

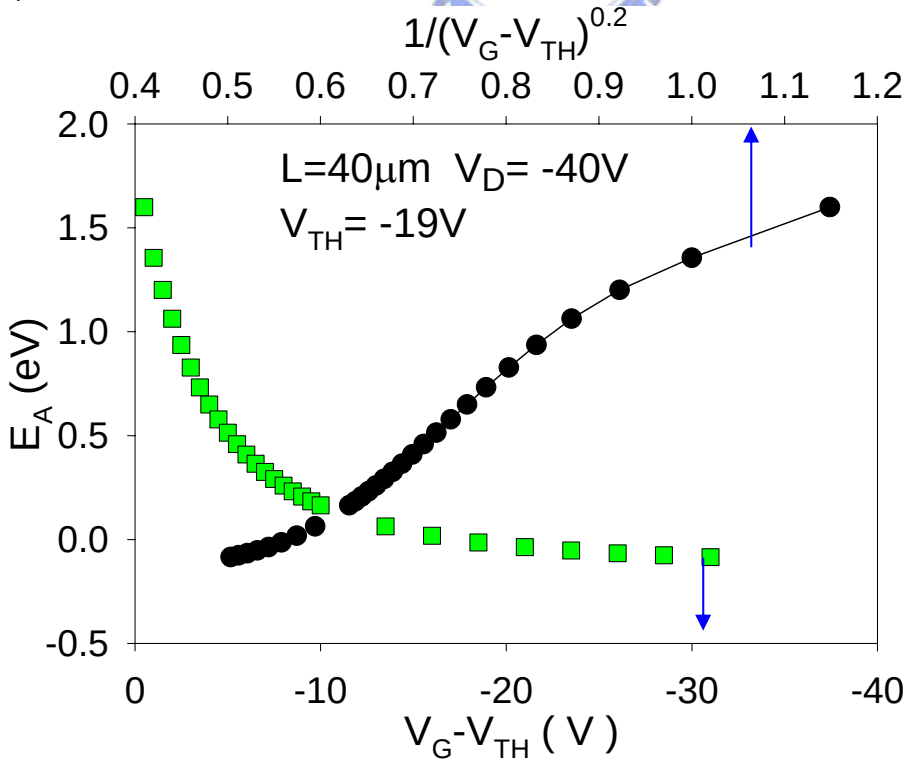


Fig. 3.16 E_A versus V_G-V_{TH} and $1/(V_G-V_{TH})^{0.2}$ for the device channel length L=40μm.

3.4 Contact resistance

There are several issues affecting the performance of OTFTs. The air-stability of the organic film is bad, the quality of the organic film is not well-controlled, and the injection is limited by barrier between the source/drain contact and the channel. Hence, the contact resistance is important and serious in OTFTs[37, 38].

In the operation of OTFT devices, the gate bias is provided to open the channel for carriers, and the drain bias is used to direct and guide the carrier transportation. The path from the source to the drain can be represented as a circuit with loaded resistances.

The choice of the contact materials is related to the injection efficiency. If the work function of the electrode is not close to the HOMO or LUMO level, there will be a potential barrier formed at the interface. High work function metals such as Au, Pt, and Pd are preferred to provide better injection efficiency, and the contact will be Ohmic-like.

In the linear operation region of OTFTs for small drain voltage and large gate voltage, the ratio of the drain voltage and drain current represents the total resistance R_{ON}. From equation (2.3), we can obtain

$$R_{ON} = R_{CH} + R_C = \left(\frac{\partial I_D}{\partial V_D}\right)^{-1} = \frac{L}{W}\frac{1}{\mu C_{OX}}\frac{1}{V_G - V_{TH}} \tag{3.2}$$

The total resistance in transport path can be divided into channel resistance R_{CH} and contact resistance R_C. The contact resistance is independent of the channel length. Therefore, as we take the relationship between the total resistance and the channel length as shown in Fig. 3.17, the contact resistance can be extracted from the R_{ON} versus L curve when the length equals zero. The drain voltage from 0 to -5V and the gate bias with -30, -34, -38, -42, -46, -50V are provided. When the gate bias is larger, the barrier between the contact and the semiconductor layer is lowered and the injection of carriers gets better. In Fig. 3.18, we can observe that as the gate voltage increases, the magnitude of the contact resistance becomes smaller.

We can also extract the contact resistance from different temperatures. The magnitude of the contact resistance decreases as the temperature increases. Therefore, the influence of increasing temperature to electrical characteristics such as self-heating effect does not come from contact resistance.

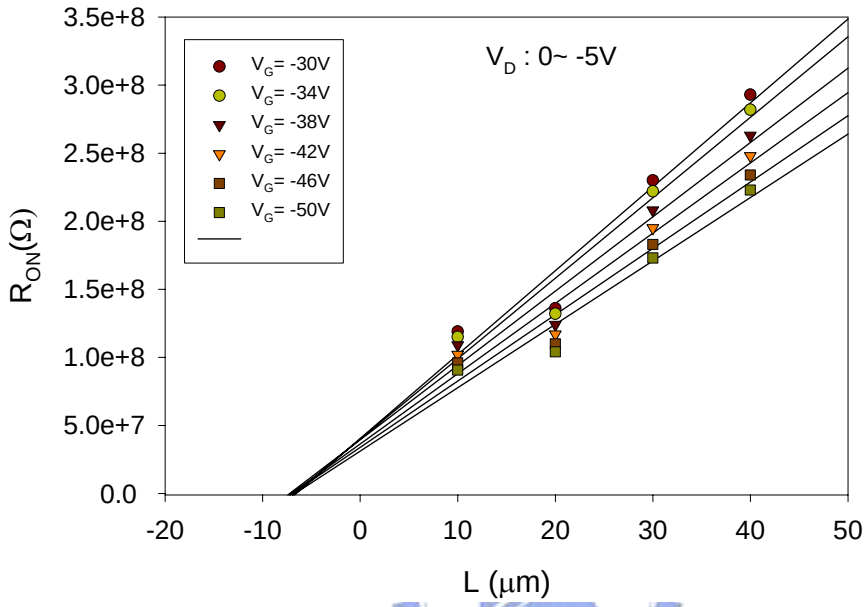


Fig. 3.17 The relationship between total resistance R_{ON} and channel length L.

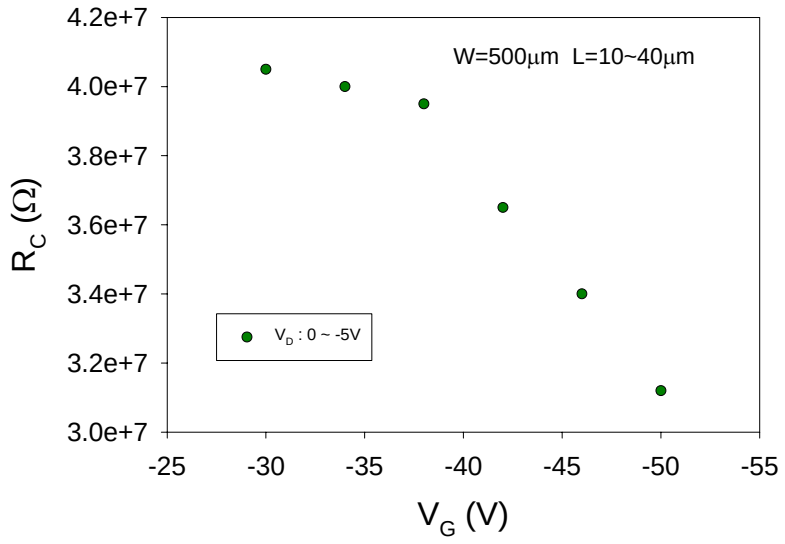


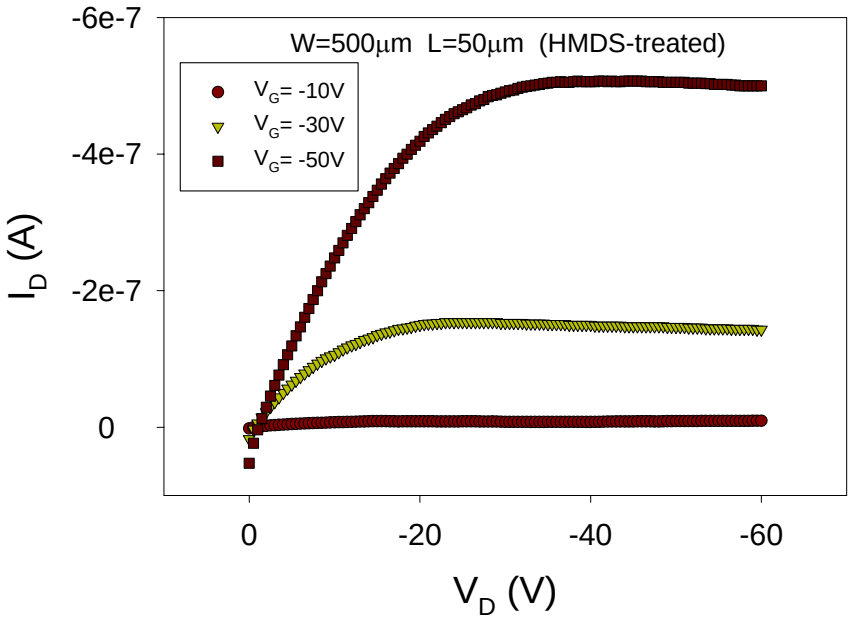
Fig. 3.18 The relationship between the contact resistance and the gate voltage.

3.5 Surface treatment

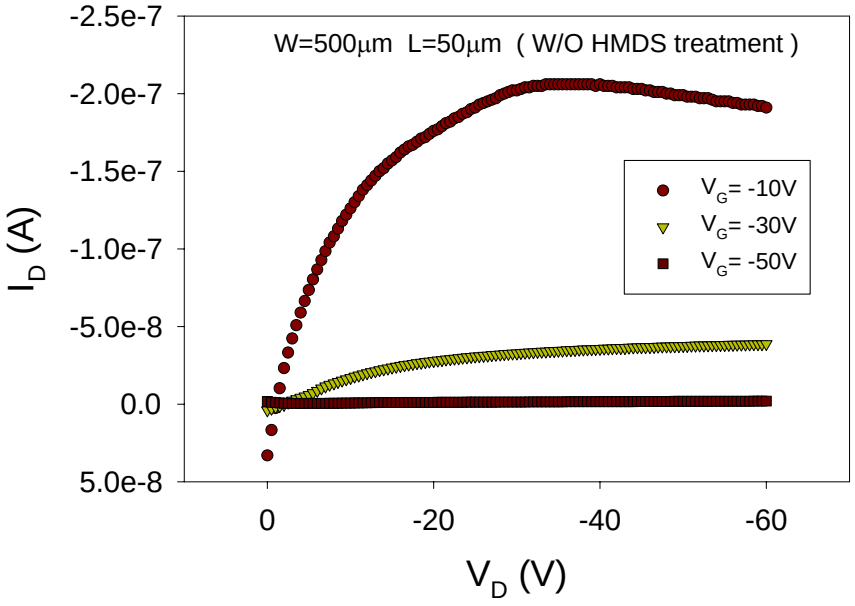
Surface treatment is usually employed to improve the device performance. Due to the very different physical natures of the insulator layer and the organic layer, their association may result in a highly disordered interface, leading to poor performance. In the past years, considerable efforts have been exerted to improve the film qualities such as crystalline and ordering to get larger mobility. A better film quality may be obtained by heating the substrate and depositing the organic film at a low rate.

Another alternative is to modify the surface of the insulator layer with a self-assembled monolayer (SAM) layer[39]. OTS (octadecyltrichlorosilane) and HMDS (hexamethyldisilazane) both show good results with the SiO_2 insulator layer. There are two effects possibly contribute to the improved characteristics of the devices. One is the effect of morphological change of organic materials such as lager grain size. And the other is the change of the electronic structure at the interface that affects the injection property[40].

In our experiments, we observe that the characteristics of the HMDS-treated devices are much better. In the I_D-V_D measurements shown in Fig. 3.19, the drain bias ranges from 0 to -60V and the gate voltages are -10, -30, and -50V, respectively. In the I_D-V_G measurement, the gate voltage ranges from 20 to -60V and the drain biases are -10, -25, and -40V, respectively. The mobility and threshold voltage for devices with and without HMDS treatment are listed in Table 3.2. The low threshold voltage of -1.19V for HMDS-treated devices is much improved. Surface treatment helps to improve the morphology, roughness of interface, and the orientation of the molecules[41]. The injection barrier of the HMDS-treated device is lowered. And the better subthreshold swing is obtained as the interface trap state density has been reduced.

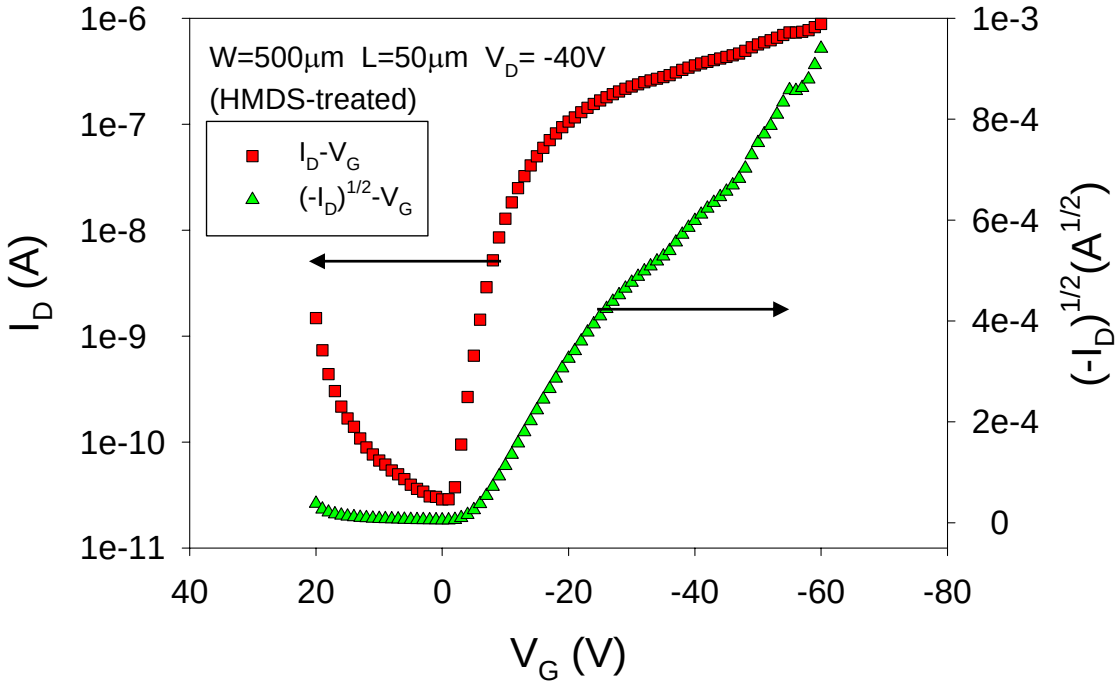


(a)

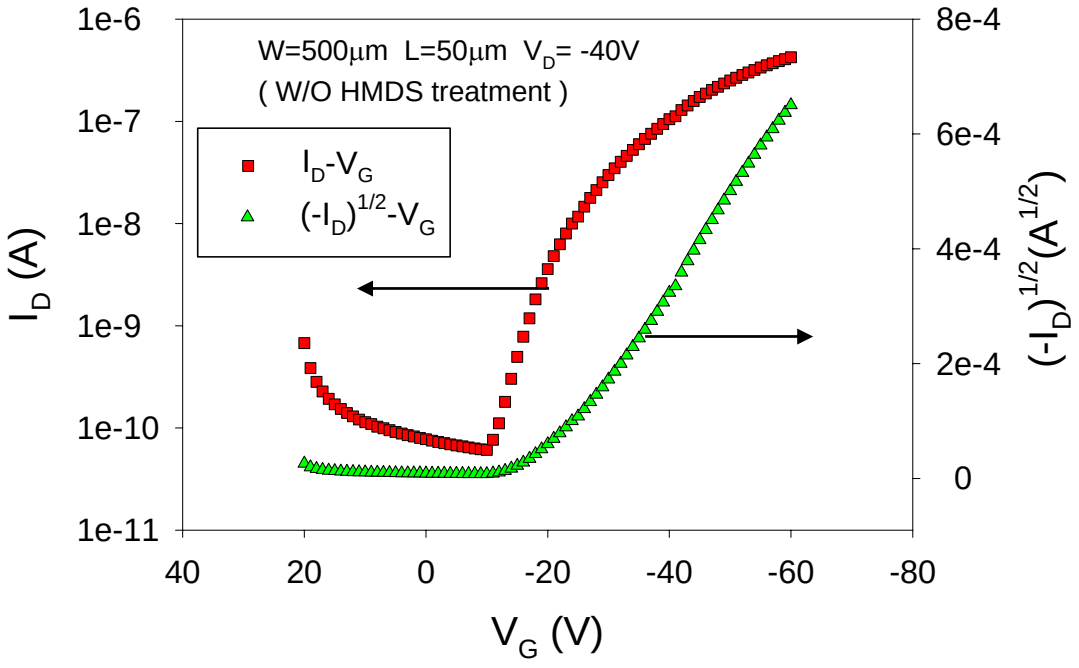


(b)

Fig. 3.19 I_D-V_D curves for devices (a) with and (b) without HMDS treatment.



(a)



(b)

Fig. 3.20 I_D-V_G and square-root of I_D-V_G curves for devices (a) with and (b) without HMDS treatment.

Table 3.2 Comparisons of the mobility and threshold voltage for devices (a) with and (b) without HMDS treatment.

	Mobility (cm^2/Vs)	Threshold voltage(V)
HMDS treatment	0.0028	-1.19
No HMDS treatment	0.0023	-15.59

Chapter 4
Conclusions

In the beginning of this thesis, we compare the devices with different pentacene film thicknesses. The AFM and XRD measurements indicate that the morphology and film quality in the 1000Å-thick device are the best, which in turn corresponds to the best electrical performance. The mobility of 0.0023cm^2/Vs and threshold voltage of -19V in the 1000Å-thick device are obtained.

We next change the measurement temperatures from 25^oC to 110^oC. As we increase the measurement temperatures, the maximum drain current becomes larger. But the self-heating effect is observed when the temperature is above 85^oC, which makes drain current lower in the saturation region. Therefore, the carrier transportation is dominated by grain barrier lowering in the lower temperature region; and in the higher temperature region, the carrier transportation is influenced by scattering effect. The trend between the activation energy and the gate voltage is the same as that in poly-Si TFTs, but the barrier is found to be dependent on the film quality. This implies that when we investigate the transportation mechanism in OTFTs, the boundary conditions of the Poisson's equations, accumulation mode operation, and even the complex material characteristics should all be taken into consideration.

We extract the contact resistance from the relationship between the I_D-V_D measurement and the channel length L. The influence of contact resistance on OTFTs is quite serious. We can observe that the value of contact resistance decreases with increasing gate voltage, which means that the contact resistance is gate bias dependent and the efficiency of carrier injection is improved as gate bias increases. Also, the contact resistance does not increase with temperature, which illustrates that the film characteristics contribute to the self-heating effect.

Surface treatment is investigated in this series of experiments. Better performance is obtained from the HMDS-treated device. Surface treatment is an effective method to improve the characteristics of the device. Dramatic reduction of the threshold voltage from -15.59V to -1.19V is achieved.

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