Chapter 2

Analogue Buffer Circuit

2.1 Introduction

Poly-Si TFTs have recently attracted much attention in the application on the integrated peripheral circuits of AMLCDs and AMOLED displays due to the high current driving capability and thereby achieve a compact, low-cost and low-power display system. However, it is well known that the integration of the whole driving circuit with poly-Si TFTs is very difficult due to the rather poor characteristics and non-uniformity of poly-Si TFTs compared with single crystal Si MOSFETs. Besides, the sub-threshold characteristics of poly-Si TFTs are rather poor, so that the sub-threshold current should not be ignored.

Among the many driving circuits using poly-Si TFTs, analogue buffers are indispensable to drive the load capacitance of the data buses in the panel, so that various analogue buffers shown in Fig. 2.1 have been reported [2-15]. To implement the analogue buffer circuit with poly-Si devices, several critical issues must be considered, such as output voltage accuracy, driving capability, layout area and power consumption, and so on.

Although an operational amplifier (op-amp) is usually connected as a unit-gain buffer, the op-amp using poly-Si TFTs shows a very large variation of the output voltage due to the large variation of poly-Si TFT characteristics [2-4]. In addition to the large variation of the output voltage, an op-amp needs many transistors, which occupy a large area.

Recently, the source follower is considered an excellent candidate of the analogue buffer circuit for the SoP application because of its simplicity, low power consumption and high immunity to the variation of poly-Si TFTs [5-15]. But, applications of the circuit structure will cause the unsaturated phenomenon of the output voltage due to the poor sub-threshold

characteristics of poly-Si TFTs. The source-follower-type analogue buffer uses an n-type driving TFT to charge the load capacitance of the data bus. When the voltage of the load capacitance approaches near a target voltage, the driving TFT is operating in the sub-threshold region. Thus, there is still a sub-threshold current of the driving TFT to charge the load capacitance. This phenomenon causes the final output voltage not to be kept constant for different charging times. Besides, its current driving capability is also reduced so that the output voltage is not settled within a line time. This is the critical drawback for application to large-sized and high-resolution displays.

In this thesis, the design consideration of an analogue buffer used in poly-Si TFT-controlled displays will be discussed. A new source-follower-type analogue buffer with an active load is proposed to eliminate the output unsaturated phenomenon and the output variation from poly-Si device characteristics, and meanwhile, increase the driving capability of a source-follower structure. The output target voltage is settled perfectly with a short charging time, so the proposed circuit is suitable for large-sized and high-resolution displays. Furthermore, the deviation is less dependent on the input voltage, reflecting the good compensation of the proposed circuit.

2.2 Architecture of display and analogue buffer

Fig. 2.2 shows the architecture of the display with integrated analogue buffers. In active matrix displays, the line-at-a-time (LAAT) is one of the most commonly used data addressing methods. In this addressing method, a data of each individual pixel of each row is first stored in the buffer. When all data in a row is stored, the pixels of the whole row will charge up at the same time. The advantage of this addressing method is that it can allow whole horizontal row time for charging and discharging the pixel capacitor. When applying this addressing method in full color displays, sample-&-hold circuits for data storage and analogue buffers

are required. The analogue video data is sampled and latched at the input of the analogue buffer, and then transferred to the data lines in a line-at-a-time (LAAT) mode. The function of the analogue buffer in the data driver is to act as a buffer to drive the load capacitance of the data bus in the panel. When the output signal of a D/A converter is not capable of driving the load capacitance of the data, an analogue buffer is used to enhance the driving capability of the D/A converter. As the panel size increases, a larger analogue buffer is required. The function of the analogue buffer is to quickly charge or discharge the load capacitance, so that the voltage across the load capacitor becomes equal to the input voltage, which is the output voltage of a D/A converter. We can sample the input data with a smaller capacitor instead of charging a larger capacitor of the data bus by the D/A converter directly. Accordingly, the effective loading for the D/A converter can be reduced. Besides, charging data buses in an LAAT mode, the analogue buffer has a longer time to charge the loading to avoid the problem of insufficient charging time in high-resolution displays.

As there are several hundreds of analogue buffers used in an active matrix display, these circuits will use up a lot of area and increase cost. Thus, it is necessary to develop an analogue buffer which not only has high immunity to the variation of poly-Si TFT characteristics but also a very simple configuration for high-resolution displays.

2.3 Op-amp-type analogue buffer

2.3.1 Simple analogue buffer

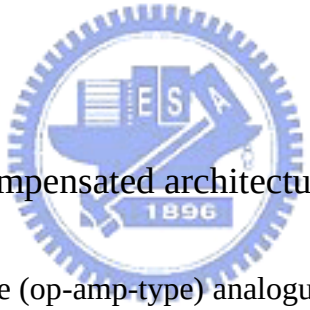
For the case of single crystal MOSFETs, it is usual to use an operational amplifier (op-amp) connected as a unit-gain buffer as shown in Fig. 2.3.

Fig. 2.4(a) shows a simple op-amp-type analogue buffer. Fig. 2.4(b) shows the input-output characteristic of the simple op-amp-type analogue buffer. The simulation result confirms good linearity and small output error of this circuit.

However, the inevitable non-uniformity of the poly-Si TFTs electrical characteristics, such as the threshold voltage and the mobility variations due to fluctuations in excimer laser energy, result in the poor performance in the circuit operation.

To study the effect of the device variation on the circuit performance, Monte Carlo simulation with an assumption of normal distribution shown in Fig. 2.5(a) is executed where in the mean value and the deviation of the threshold voltage and the mobility are 1V, 1V, 77.1 cm^2/vs and 20 cm^2/vs, respectively. Each of the poly-Si TFTs in the circuit simulation varies independently.

Fig. 2.5(b) shows the Monte Carlo simulation results of the simple op-amp-type analogue buffer. It is obvious that the circuit suffers from huge variations due to the poly-Si TFT characteristics. To solve this problem, some compensating methods as discussed below have been studied.



2.3.2 Analogue buffer compensated architecture

An operational-amplifier-type (op-amp-type) analogue buffer to compensate for the poly-Si TFT variation has been reported by Itou [2]. Fig. 2.6 shows the Itou's circuit configuration of the differential amplifier. Compared with the conventional differential amplifier, one additional capacitor and three switches are used for the circuit. In this circuit, when the switches S1 and S2 are turned on, and S3 is turned off, the circuit is in the compensation period, and is shown in Fig. 2.7(a). In this period, both the gate voltages of M1 and M2 are V1, and the drain currents, $I_{di,\ i=1,2,3,4}$, of the transistors, Mi, are formulated by the following equations;

$$I_{d1} = K1\{(V1 - Vs) - |V_{THP1}|\}^2 \qquad (2.1)$$

$$I_{d2} = K2\{(V1 - Vs) - |V_{THP2}|\}^2 \qquad (2.2)$$

$$I_{d3} = K3\left(V_{g3} - V_{THN3}\right)^2 \qquad (2.3)$$

$$I_{d4} = K4\left(V_{g4} - V_{THN4}\right)^2 \qquad (2.4)$$

where V_{THPi} and V_{THNi} are the threshold voltages of p-type and n-type TFTs. In the compensation period, the diode-connected M3 and M4 produce $I_{d1}=I_{d3}$ and $I_{d2}=I_{d4}$, and V_{g3} and V_{g4} shown in Fig. 2.7(a) are formulated as

$$V_{g3} = V_{THN3} + \sqrt{\frac{I_{d3}}{K3}} = V_{THN3} + \left\{\left(V1 - Vs\right) - \left|V_{THP1}\right|\right\}\sqrt{\frac{K1}{K3}} \qquad (2.5)$$

$$V_{g4} = V_{THN4} + \sqrt{\frac{I_{d4}}{K4}} = V_{THN4} + \left\{\left(V1 - Vs\right) - \left|V_{THP2}\right|\right\}\sqrt{\frac{K2}{K4}} \qquad (2.6)$$

and the stored charge Q1 on the capacitor C1 are represented by Q1=C1 (V_{g3}-V_{g4}).

When the switches S1 and S2 are turned off, and S3 is turned on, the circuit is in the operation period, and is shown in Fig. 2.7(b). In this period, the output current Iout flows through the node A shown in Fig. 2.7(b) is calculated. The drain current equations of M1, M2 and M3 are represented by equations (2.1), (2.2) and (2.3), accordingly. The gate voltage of M4, V'_{g4}, is derived from V_{g3} and the stored charge Q1 on the capacitor C1. Then, V'_{g4} = V_{g3}-Q1/C1 is obtained. Finally, the drain current of M4, I'_{g4}, is formulated by the following equation:

$$I'_{d4} = K4\left(V'_{g4} - V_{THN4}\right)^2 = K4\left\{V_{THN4} + \left[\left(V1 - Vs\right) - V_{THP2}\right]\sqrt{\frac{K2}{K4}} - V_{THN4}\right\}$$

$$= K2\left\{\left(V1 - Vs\right) - V_{THP2}\right\}^2 \qquad (2.7)$$

This result shows the drain current of M2, I_{d2}, is equal to the drain current of M4, I'_{d4}. This means Iout becomes zero.

Namely, using the circuit, when the two differential input voltages are the same, the output current of the differential amplifier is zero. Therefore, the input offset is fully canceled in the operation period.

Fig. 2.8(a) shows the Itou's unit-gain analogue buffer using his differential amplifier configuration and the time chart of the control switches. In this circuit, the switch, S1, is realized by M6 and M7. M8 is the dummy switch, which is used to absorb the channel charge when M6 and M7 are turned off.

The Monte Carlo simulation results shown in Fig. 2.8(b) indicate the output voltage variation is reduced, but remains. This output voltage variation is caused by the mismatch of the output stage of the analogue buffer.

Although op-amps are generally used for analogue buffers, op-amps using poly-Si TFTs show a very large variation of the output voltage due to the large variation of poly-Si TFT characteristics. In addition to the large variation of the output voltage, an op-amp needs many transistors, which occupy a large area. As there are several hundreds of analogue buffers used in an active matrix display, these circuits will use up a lot of area and increase cost. Thus, it is necessary to develop a different circuit configuration of the analogue buffer which not only has high immunity to the variation of poly-Si TFT characteristics but also a very simple configuration for high resolution displays.

Some researches on poly-Si TFT analogue circuits have been tried to realize a buffer that can operate insensitively on the poor characteristics of poly-Si TFTs, and the source-follower-type analogue buffers are representative results of those efforts. In next section, we will discuss the source-follower-type analogue buffers.

2.4 Source-follower-type analogue buffer

2.4.1 Match-TFT analogue buffer

The matching devices are widely applied in many circuits such as differential pairs. For matching poly-Si TFTs, they are even used as a compensation technique for analogue buffer and AMOLED pixel circuits. It is believed that TFTs in pairs placed very closely in the

matching configuration will have identical characteristics. However, the micro variation in the grain structures can still make the discrimination between the matching TFTs, as shown in Fig. 2.9.

Fig. 2.10 shows the Jung's analogue buffer, which consists of 7 n-type TFTs and 3 switching signals, and its timing diagram [12]. The circuit is a source-follower-type analogue buffer and does not use any capacitor to store the threshold voltage of the driving TFT (N3). In this case of the match-TFT structure, Jung assumes that all TFT have same characteristics.

The detailed operation is as follows. When the "Reset" signal is high, the previous data voltage in the load capacitor is reset. When the data voltage is applied, the gate voltage of N3 becomes about Vdata-V_{TH} by diode connection and N3 is turned on. Then N4 is turned on by the "Active" signal and the high voltage is transferred to the load capacitor. At this time, the gate voltage of N3 also becomes high by "boot-strapping". When the gate voltage of N3 becomes over Vdata+V_{TH}, N2 is turned on. This circuit acts as a source follower, so that the source voltage of N3 is about Vdata when the gate voltage of N3 is Vdata+Vth. The gate of N3 is not floating node any more and the "boot-strapping" action is stopped.

Fig. 2.11(a) shows the Monte Carlo simulation results assumed that TFT characteristics are matched in the same pixel. The results show that this circuit can effectively eliminate the TFT's V_{TH} variation by using the driving TFT (N3), provided that the characteristics of the compensating TFT (N2) are same as those of the driving TFT (N3).

However, it is encountered to the mismatch problem between the driving TFT (N3) and the compensating TFT (N2) in the same pixel. It is difficult to achieve exactly same TFT characteristics by using the conventional poly-Si TFT process. Fig. 2.11(b) shows the Monte Carlo simulation results assumed that mismatch-TFT characteristics in the same pixel. Compared to Fig. 2.11(a), the output variations are very large. Therefore, it can't achieve enough compensating ability for the threshold voltage variation. To solve the mismatch problem of poly-Si characteristics, some circuits named the V_{TH}-self-compensated structure as

discussed below are proposed to compensate the device variation by themselves.

2.4.2 V_{TH}-self-compensated analogue buffer

2.4.2.1 Chung's push-pull analogue buffer and simulated results

The source-follower-type analogue buffer with the V_{TH}-self-compensated method compensates for the threshold voltage variation by using a storage capacitor to store the $|V_{GS}|$ of the driving TFT.

The Chung's push-pull analogue buffer with a simple configuration [6] is shown in Fig. 2.12. The n-type driving TFT (NTFT) pushes the current to the load capacitor and the p-type driving TFT (PTFT) pulls the current from the load capacitor; thus, Chung calls it a push-pull analogue buffer. However, the circuit has a dead-band in the middle of the signal swing because of its class-B structure. The width of the dead-band is unpredictable because it is determined by the threshold voltages of n-type and p-type driving TFTs.

The push-pull analogue buffer is composed of a complementary source follower output stage, a storage capacitor (Cvt) which stores the threshold voltage of the driving TFT, and three switches (S1, S2, S3).

The operating sequence for positive polarity input voltage is as follows. In the compensation period (1), the switches S1 and S2 are turned on. An input voltage (Vin) is applied to the gate of the n-type driving TFT (NTFT). The output voltage then reaches Vin-V_{THN}. Thus, the threshold voltage of the NTFT is stored in Cvt. In the data-input period (2), only the switch S3 is turned on. The gate voltage becomes Vgate-V_{THN} = Vin. In a similar way, the negative voltage signal is buffered by the p-type driving TFT (PTFT) after compensating the threshold voltage of the PTFT. In this way, the wide variation of poly-Si TFTs can be compensated.

Fig. 2.13(a) and Fig. 2.13(b) shows the Monte Carlo simulation results for different

compensating times. The simulation results confirm good variation-tolerant characteristics. The output variation of the Chung's circuit is much less that of the op-amp-type analogue buffer using poly-Si TFTs. However, the final output voltages are not kept constant for different charging times and an exact threshold voltage of the driving TFT is not saved in the storage capacitor (Cvt) due to the poor sub-threshold characteristics of poly-Si TFTs. Besides, the output voltages are not settled within a line time. Owing to the limit on data changing rate, the Chung's analogue buffer is not suitable for high-speed applications.

The output error analysis of the Chung's analogue buffer shows two major sources of error. The first source is the charge loss of the V_{TH} storage capacitor (Cvt); the second source is the poor sub-threshold characteristic of the driving TFT. The fabricated poly-Si TFTs, however, have small sub-threshold slopes and large leakage currents. If the poly-Si TFTs with larger sub-threshold slope and lower leakage current are used, the error of the push-pull analogue buffer can be reduced further and the push-pull analogue buffer would find wide application as integrated data driver circuits of poly-Si TFTs.

2.4.2.2 Proposed source-follower-type analogue buffer

2.4.2.2.1 Unsaturated phenomenon of the output voltage

The typical model of the poly-Si TFTs used in this paper is represented by the RPI parameters, which gives the I_D-V_{GS} curves shown in Fig. 2.14. In this work, the charging time is about 50μs and the load capacitance of the data bus is assumed 20pF, which almost corresponds to a 2-inch QVGA LCD.

A conventional source follower and its output waveform are shown in Fig. 2.15(a) and 2.15(b), respectively. It is observed that the final output voltage is not kept constant, but exceeds the value of Vin-V_{TH} expected with MOSFET's principle. This phenomenon implies that the voltage saved in the storage capacitor (Cvt) is not the exact threshold voltage of the

driving TFT. It is ascribed to the sub-threshold current. As shown in Fig. 2.14 inset, the sub-threshold swing of poly-Si TFTs is about 0.3V/dec which is much larger than that of MOSFETs (0.06V/dec). Consequently, it will be sensitive to the charging time for various product specifications such as frame rates. Besides, when the voltage of the load capacitor approaches near a target voltage, the voltage drop $|V_{GS}|$ between the gate and the source of the driving TFT is reduced, so its current driving capability is also reduced. This causes the output voltages not to be settled within a line time and applications of the source follower structure not suitable for large-sized and high-resolution displays.

An active load shown in Fig. 2.16(a) is added to eliminate this phenomenon. The active load is designed to have large channel length (L) for minimizing the DC current and reducing the kink effect. The simulation result is shown in Fig. 2.16(b). It is distinct that the unsaturated phenomenon of the output voltage is diminished and the shorter charging time is suitable for high-speed applications. Fig. 2.17 plots the offset voltage (Vin-Vout) versus the input voltage. It is observed that the offset voltage of the conventional source follower varies with different charging time. On the contrary, the one with the active load does not. Although the offset voltage of the source follower with the active load is larger, it can be eliminated by a properly corresponding gamma correction. As a result, the source follower with an active load is superior to possess the charging time variation-tolerant characteristics.

2.4.2.2.2 Distributed phenomenon of the output voltage

Fig. 2.18(a) shows the Monte Carlo simulation results of the source follower with the active load when the input voltage is 4V and 6V where in the simulation conditions is the same as used in sec. 2.3.1. It is clear that the circuit suffers from huge variations due to the poly-Si TFT variation. To deal with this, a new analogue buffer shown in Fig. 2.19 is proposed for the compensation of the device variation. It consists of two TFTs, a capacitor and four switches.

Due to the simple circuit configuration, the proposed analogue buffer can be easily applied to integrated data driver circuits of poly-Si TFT displays. The operating principles can be described as two periods shown in Fig. 2.19. The gate voltage of the TFT as the active load is constantly biased at Vbias. In a compensation + initialization period (1), only S1, S2 are turned on. Thereby, a voltage drop is stored in Cvt. In the meantime, the previous data voltage stored in the load capacitor is reset from the pre-charge signal line. In a data-input period (2), only S3, S4 are turned on, while the gate voltage of the driving TFT is applied with the voltage difference hold in Cvt added to the input voltage. Thus, the output voltage is compensated by the voltage stored in Cvt. Fig. 2.18(b) shows the output voltage variation of the proposed analogue buffer from the Monte Carlo simulation including both the driving and biasing TFTs. Compared to Fig. 2.18(a), the output voltage variation decreases drastically. In this way, the wide variation of poly-Si TFTs can be easily compensated. Furthermore, the unsaturated phenomenon of the output voltage is diminished and the output target voltage is settled perfectly with a shorter charging time, so the proposed circuit is suitable for large-sized and high-resolution displays.

2.4.2.2.3 Source-follower-type analogue buffers with an active load

In this section, several source-follower-type analogue buffers with an active load are discussed. Fig. 2.20(a) shows a schematic of the modified Chung's analogue buffer [6] with an active load and its operating principles, and Fig. 2.20(b) shows the Monte Carlo simulation results of the output voltage variation. It has not only high immunity to the variation of poly-Si TFT characteristics but also a very simple configuration. Since the voltage drop $|V_{GS}|$ of the driving TFT stored in Cvt in the compensation period will be influenced by the input voltage due to the poor sub-threshold characteristic of the poly-Si TFT, the output variation is dependent on the input voltage. The modified Kida's double offset canceling

analogue buffer [7] with an active load is shown in Fig. 2.21(a) and its Monte Carlo simulation results are also shown in Fig. 2.21(b). It is distinct that the unsaturated phenomenon of the output voltage is suppressed and the compensation results are excellent.

Fig. 2.22 compares the standard deviations of the output voltage in the conventional source follower, Chung's analogue buffer [6], Kida's double offset canceling analogue buffer [7] and the proposed analogue buffer calculated from the Monte Carlo simulation results. All of the circuits include the active load to eliminate the unsaturated behavior. The merits of the proposed one including wide operation range and small deviation are distinguished. Furthermore, the deviation is less dependent on the input voltage due to the compensation from the constant voltage source (Vdd). Compared to Chung's compensation from the input voltage, the proposed circuit reflects the good compensation result.

The standard deviation of the output voltage and the power consumption related to the Vbias are shown in Fig. 2.23. It reveals that the Vbias should be properly designed to minimize the deviation with lowest power consumption.

2.5 Conclusions

In this thesis, the device variation is described. Its influences on the analogue circuits and circuit design techniques to compensate for the variation are also discussed. A new source-follower-type analogue buffer with an active load is proposed to eliminate the output unsaturated phenomenon and the output variation from poly-Si device characteristics, and meanwhile, increase the driving capability of a source-follower structure. The output target voltage is settled perfectly with a short charging time, so the proposed circuit is suitable for large-sized and high-resolution displays. Furthermore, the deviation is less dependent on the input voltage, reflecting the good compensation of the proposed circuit.

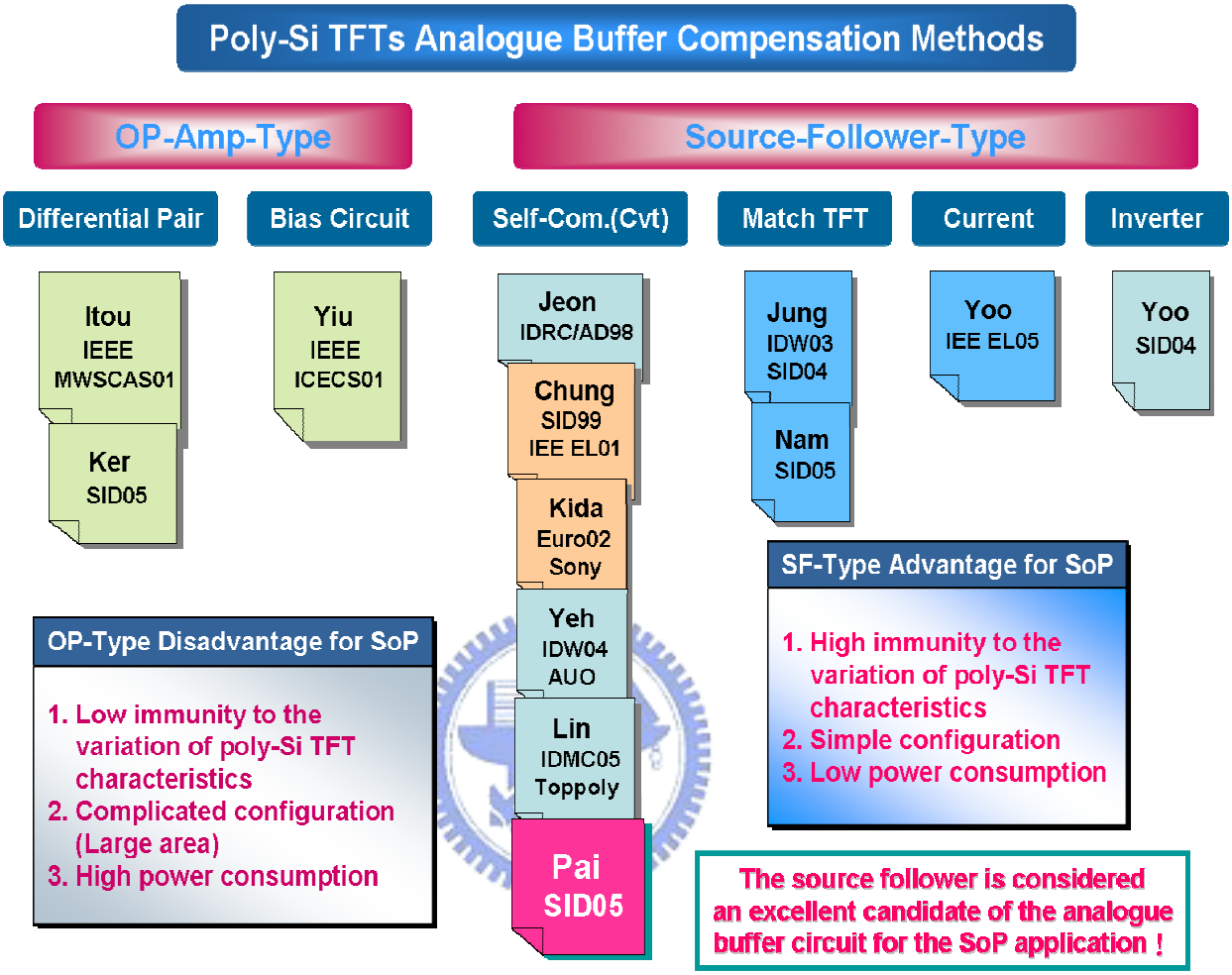


Fig. 2.1 Poly-Si analogue buffer compensation methods

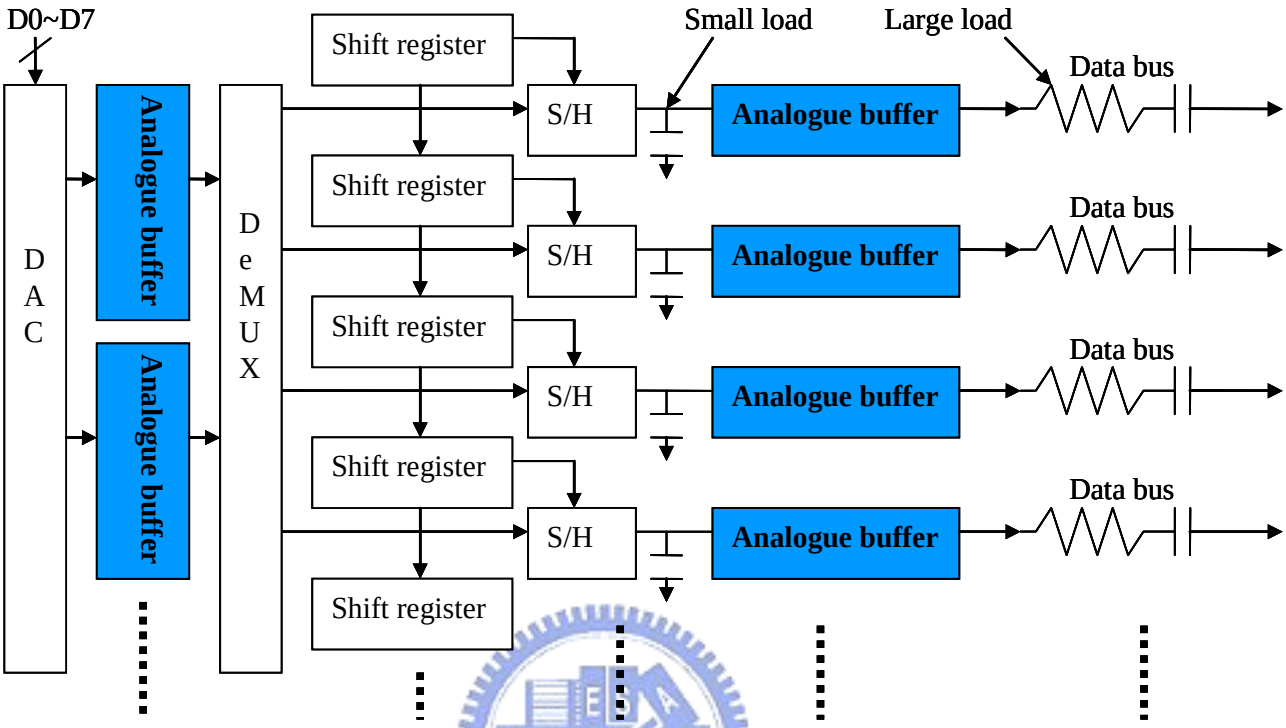


Fig. 2.2 The architecture of the display with integrated analogue buffers

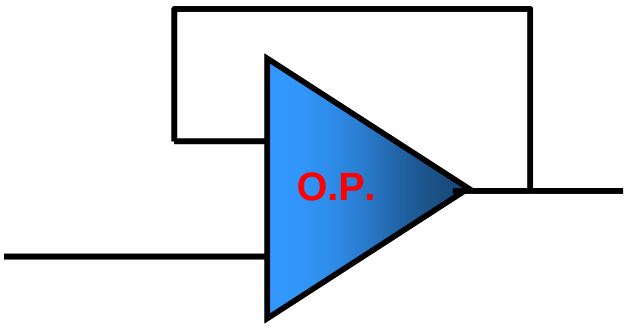


Fig. 2.3 An operation amplifier connected as a unit-gain buffer

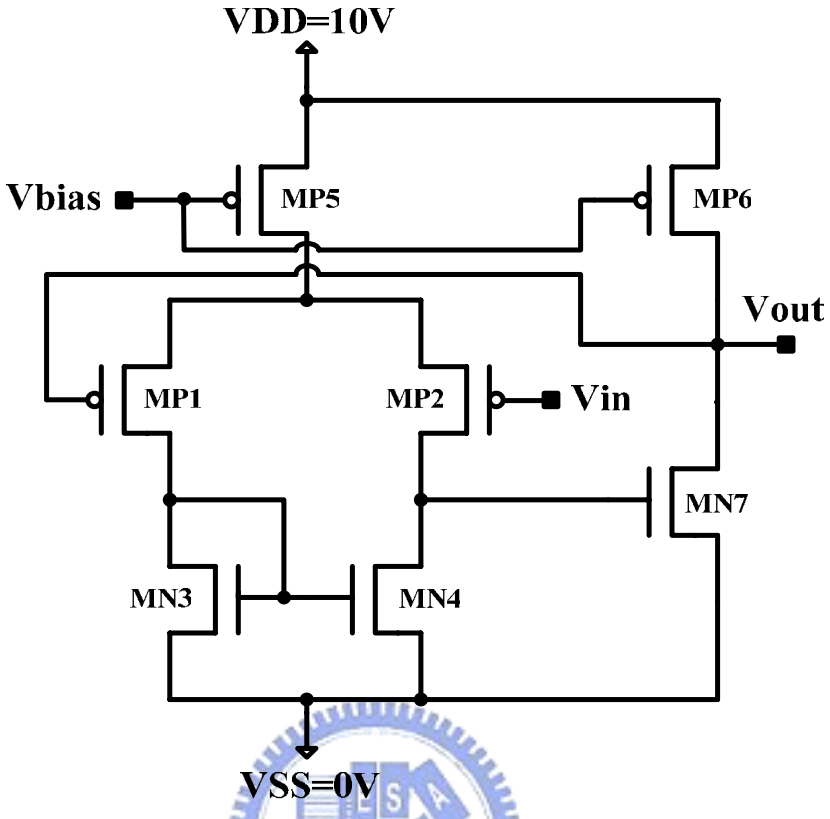


Fig. 2.4(a) A simple op-amp-type analogue buffer

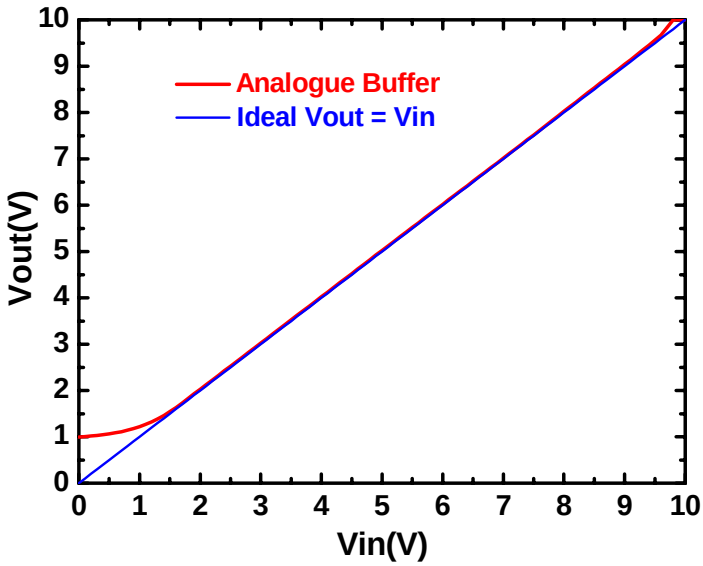


Fig. 2.4(b) The input-output characteristic of the simple op-amp-type analogue buffer

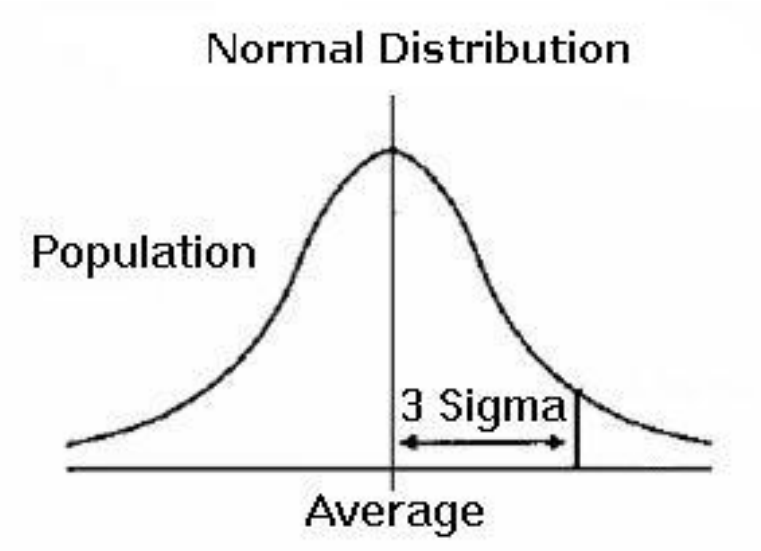


Fig. 2.5(a) Monte Carlo simulation with an assumption of normal distribution

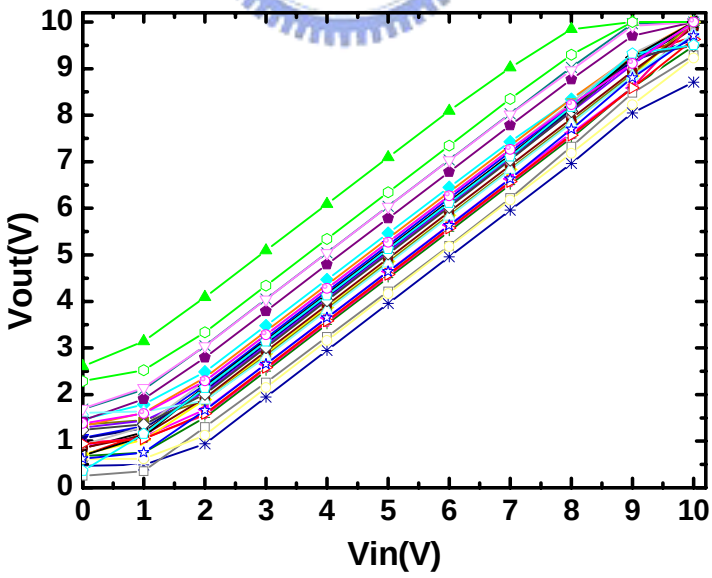


Fig. 2.5(b) The Monte Carlo simulation results of the simple op-amp-type analogue buffer

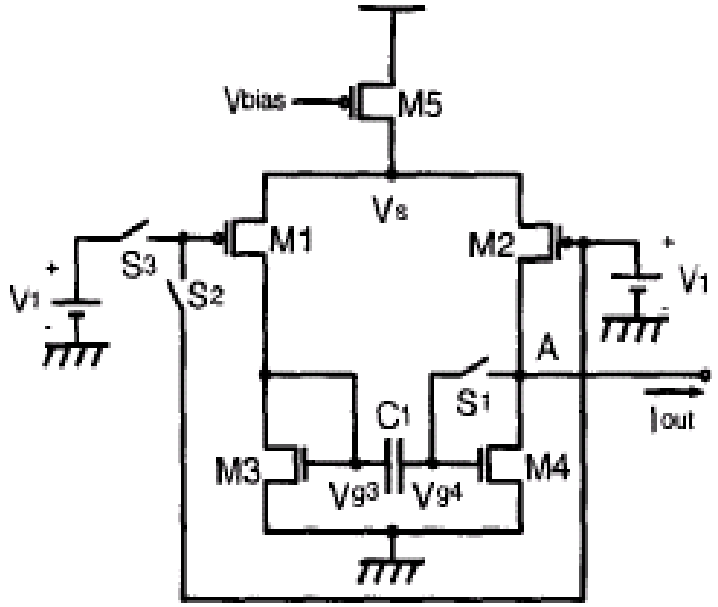


Fig. 2.6 Itou's circuit configuration of the differential amplifier [2]

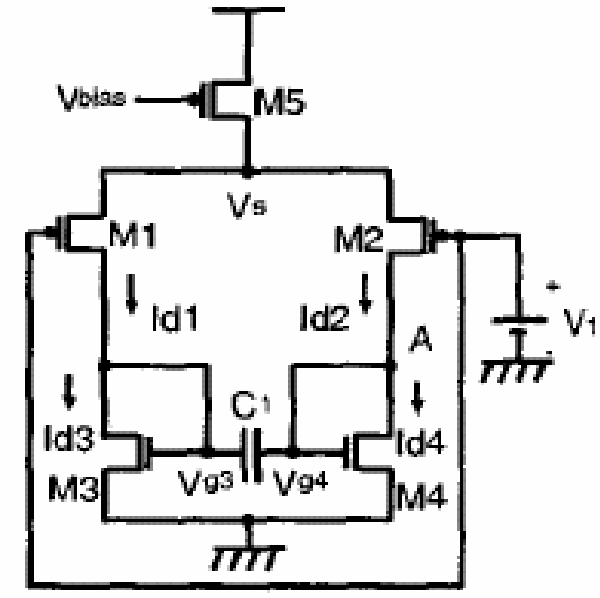


Fig. 2.7(a) In the compensation period

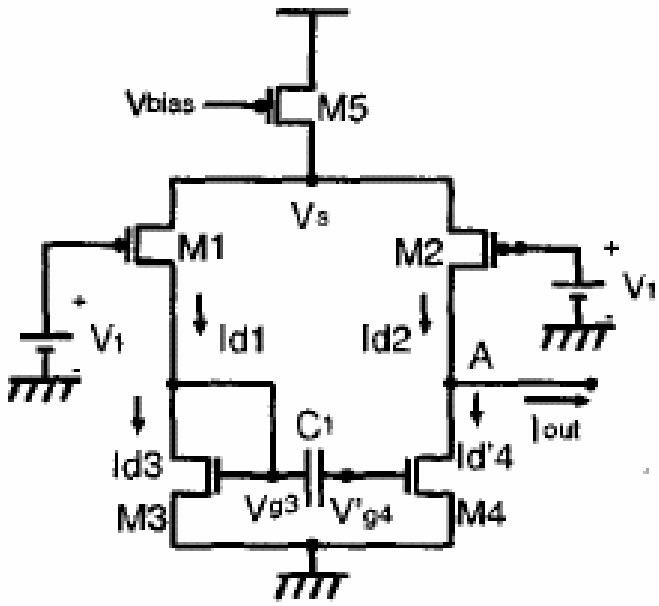


Fig. 2.7(b) In the operation period

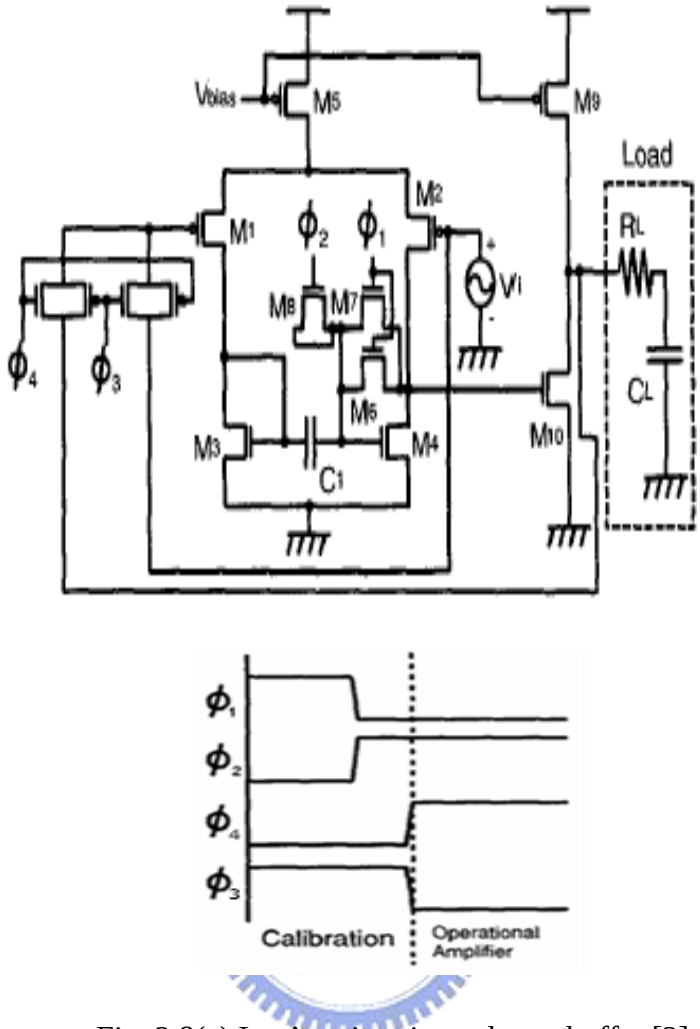


Fig. 2.8(a) Itou's unit-gain analogue buffer [2]

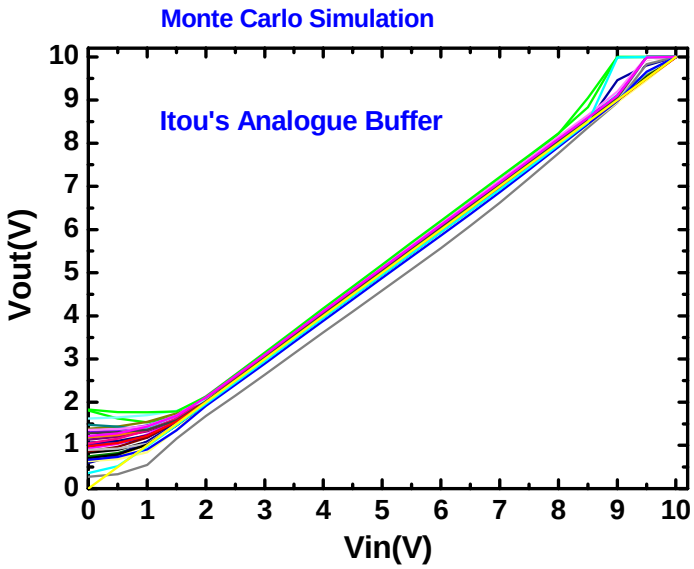


Fig. 2.8(b) The Monte Carlo simulation results of the Itou's unit-gain analogue buffer

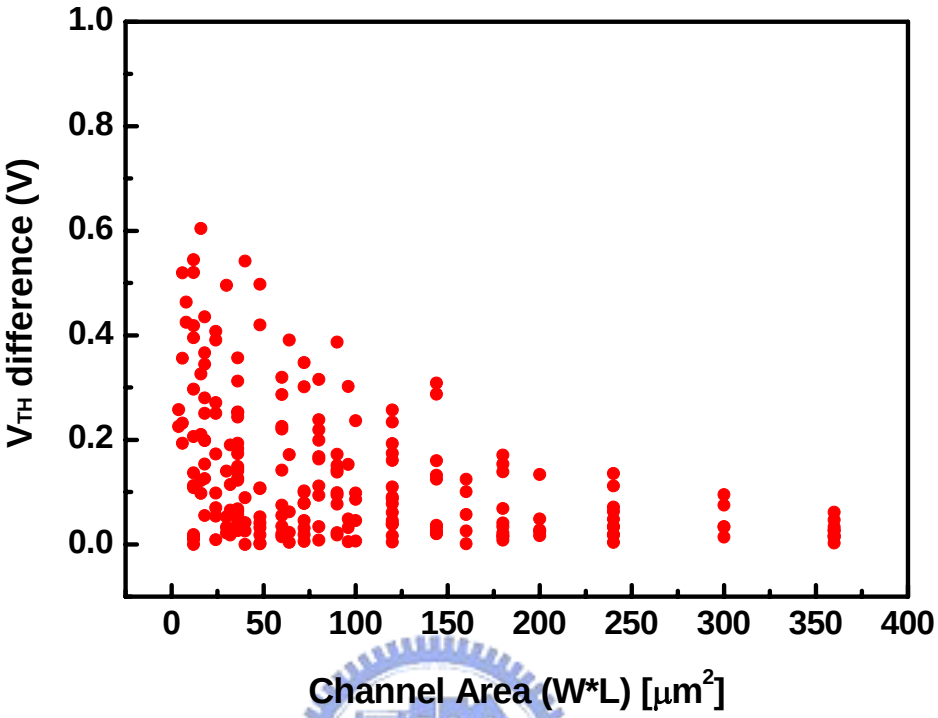


Fig. 2.9 The V_{TH} difference of match TFTs with respect to channel area

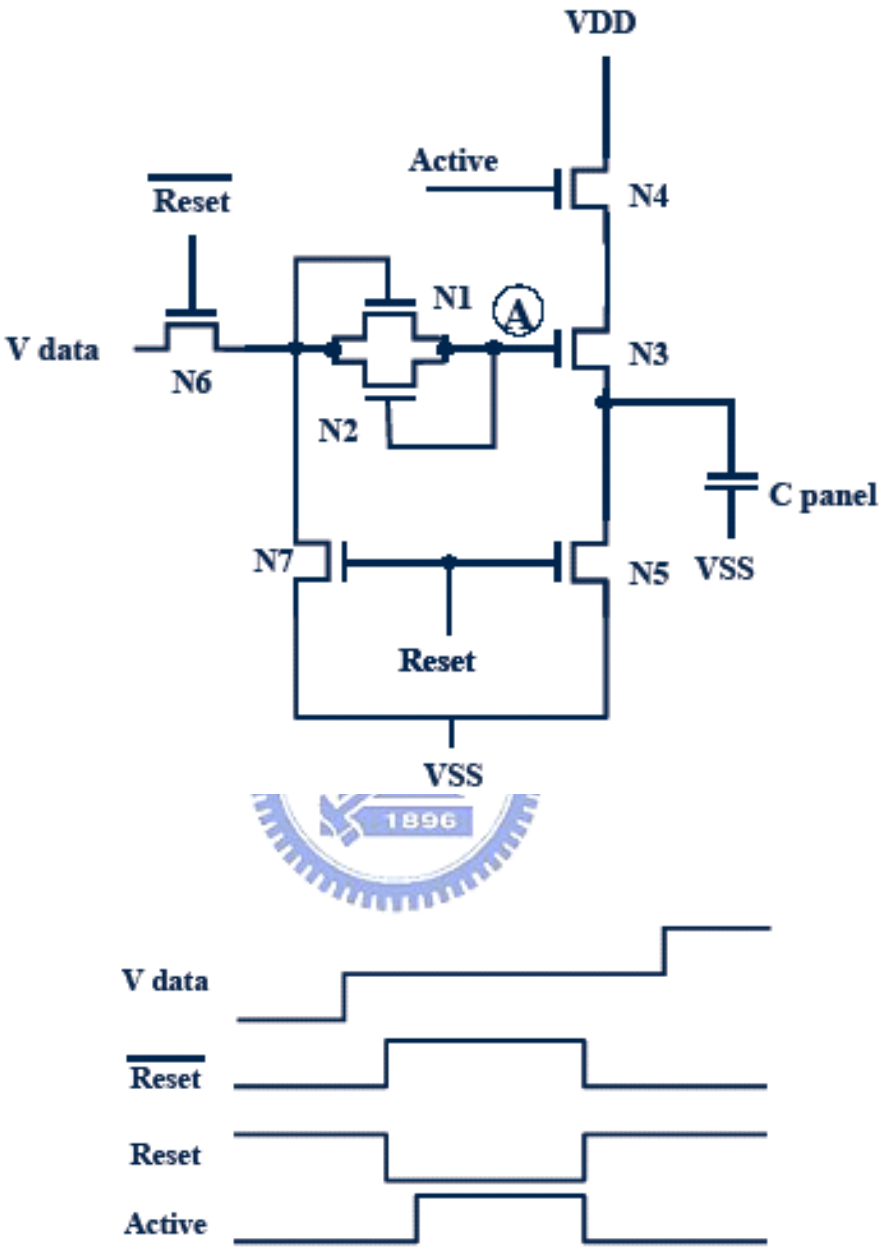


Fig. 2.10 Jung's analogue buffer [12]

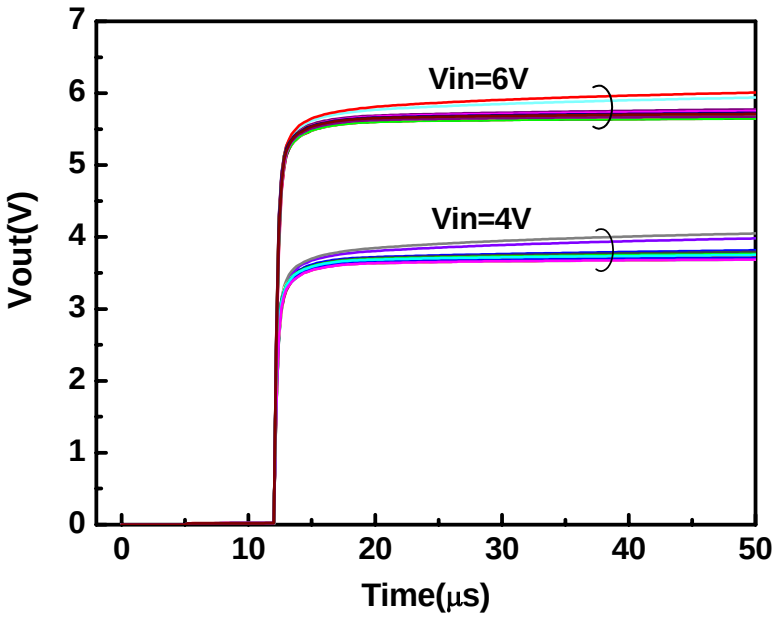


Fig. 2.11(a) The Monte Carlo simulation results assumed that TFT characteristics are matched in the same pixel

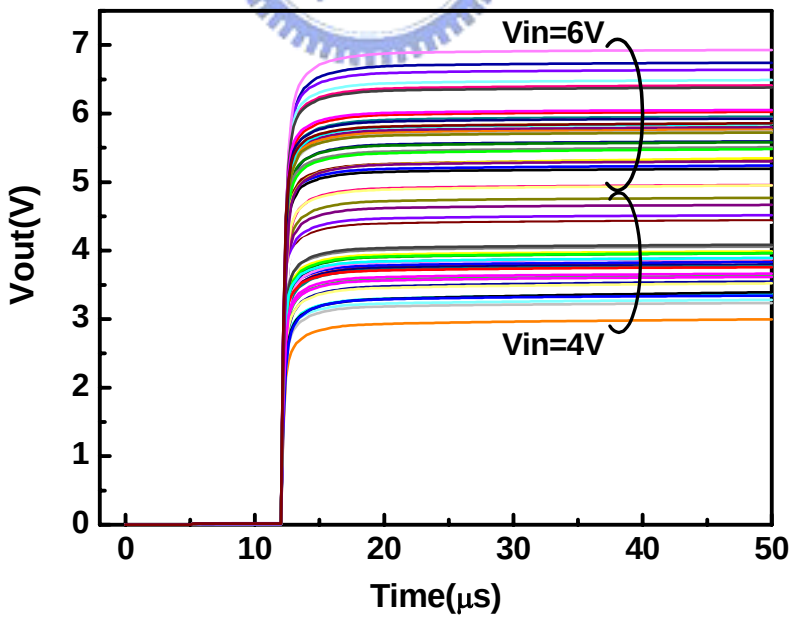


Fig. 2.11(b) The Monte Carlo simulation results assumed that mismatch-TFT characteristics in the same pixel

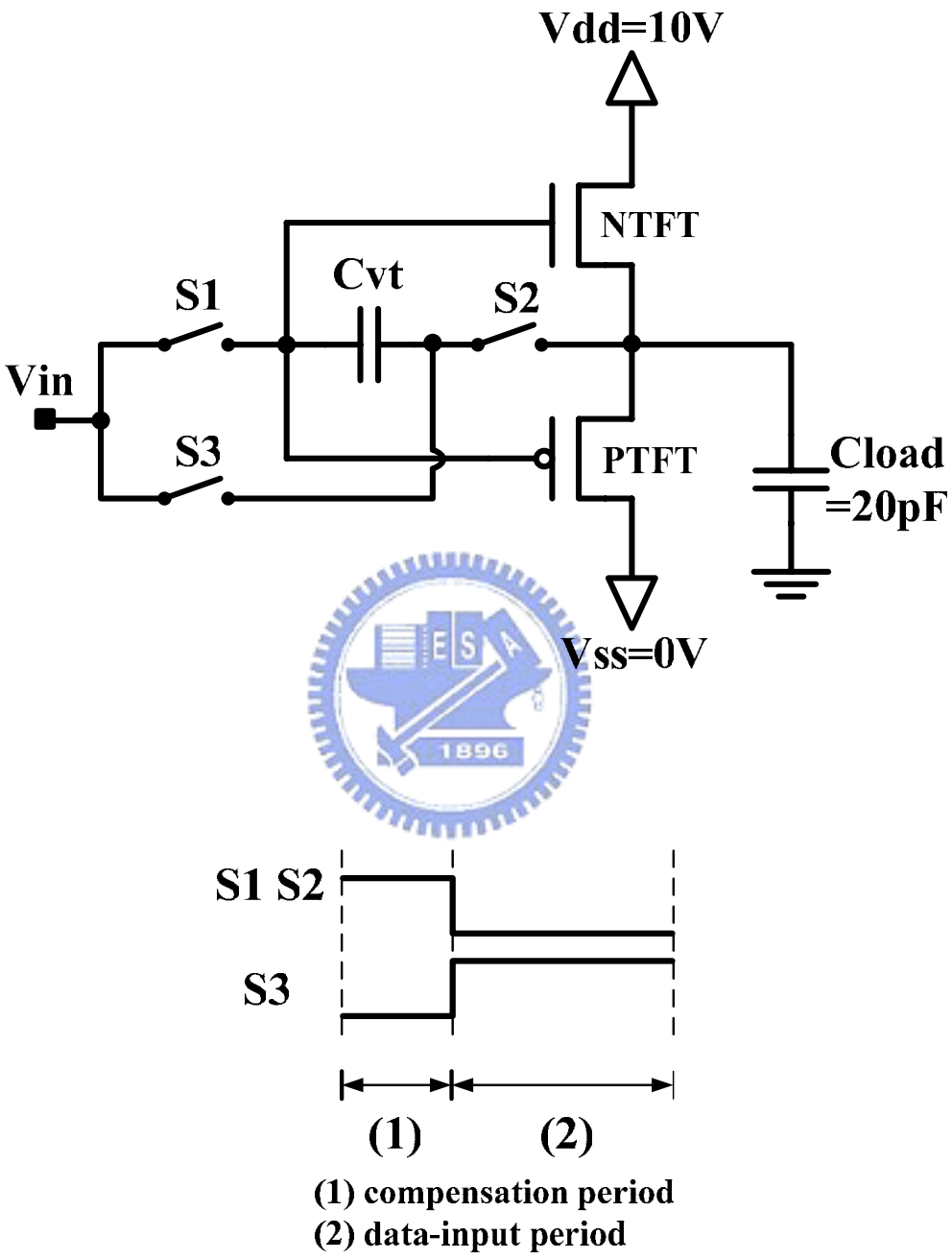


Fig. 2.12 Chung's push-pull analogue buffer [6]

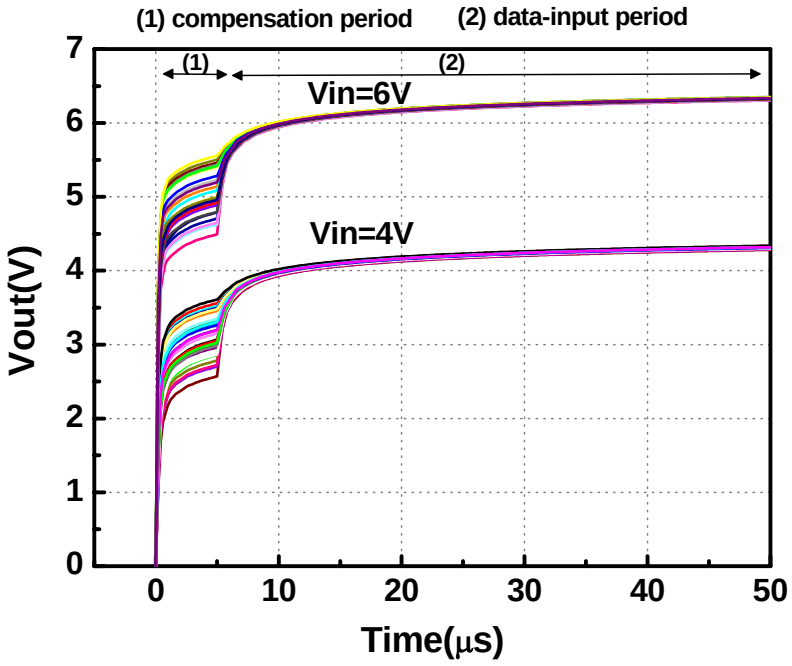


Fig. 2.13(a) The Monte Carlo simulation results with 5 μ s compensation period

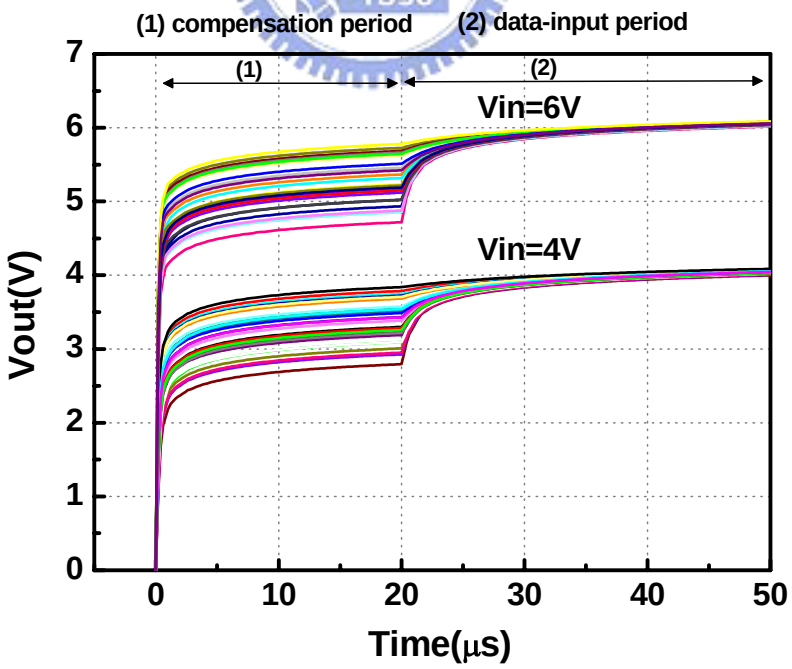


Fig. 2.13(b) The Monte Carlo simulation results with 20 μ s compensation period

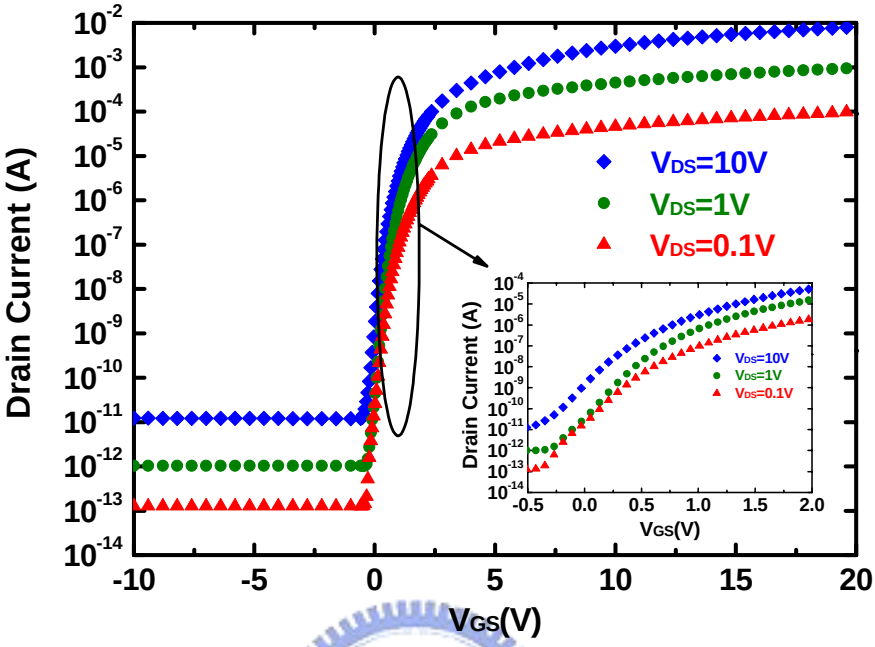


Fig. 2.14 The I_D-V_{GS} of poly-Si TFT curves

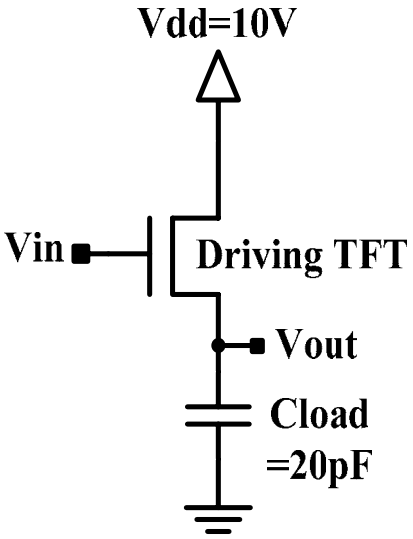


Fig. 2.15(a) The conventional source follower

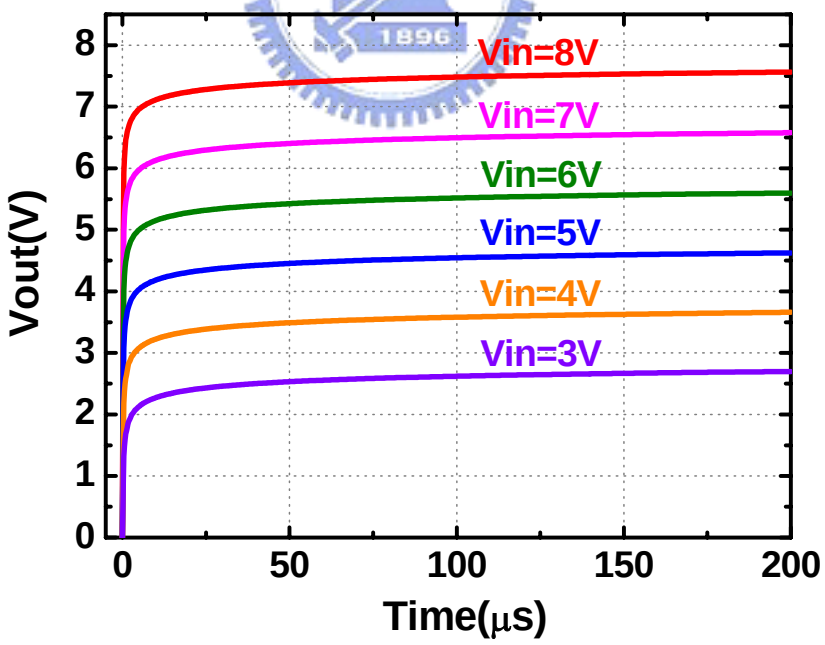


Fig. 2.15(b) Its output waveform

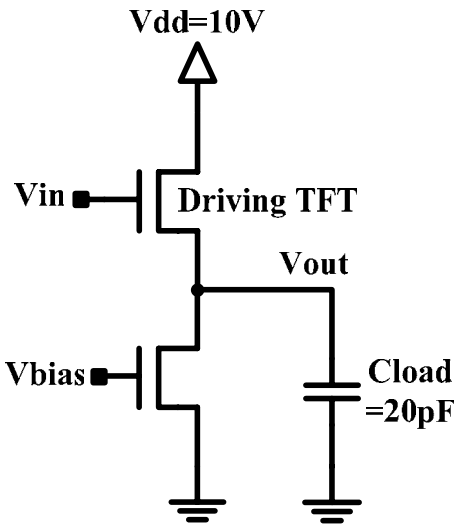


Fig. 2.16(a) The source follower with an active load

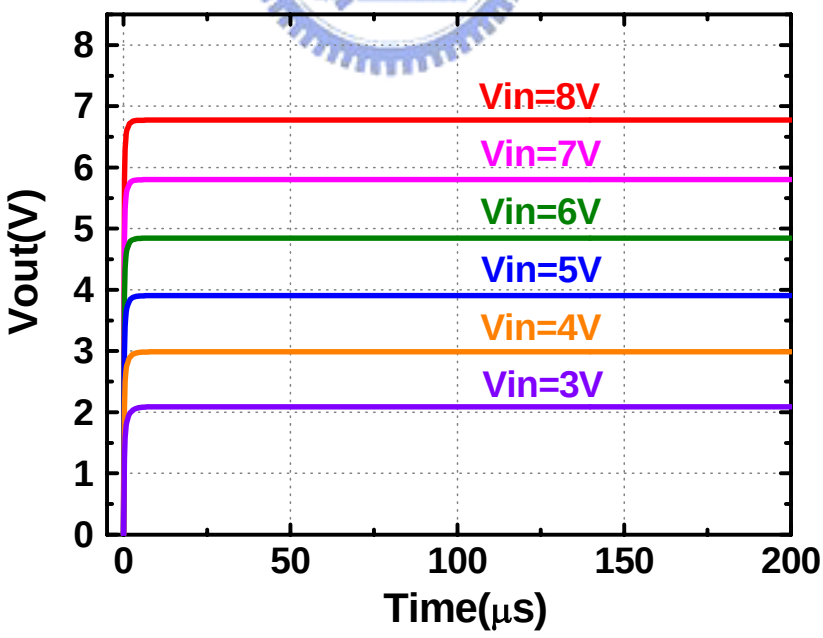


Fig. 2.16(b) Its output waveform

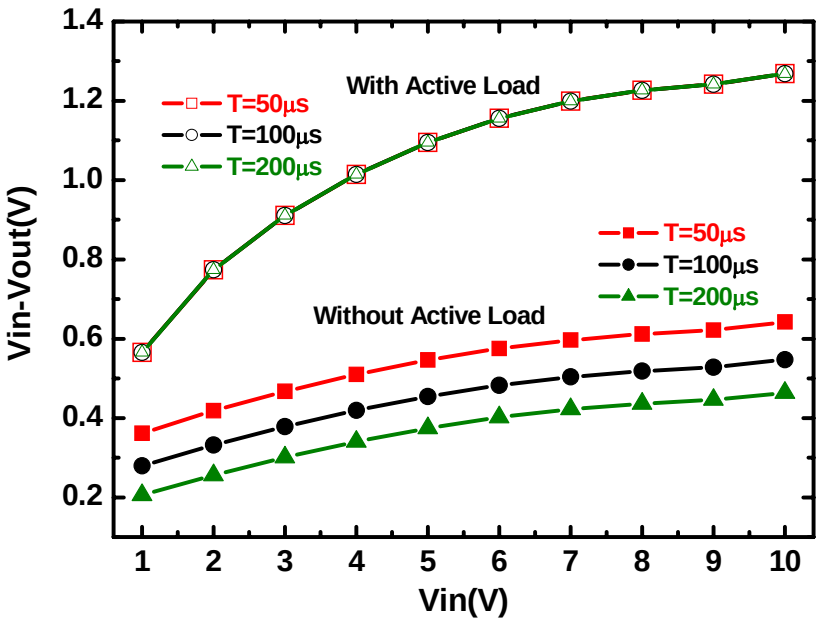


Fig. 2.17 Comparison of the conventional source follower and the source follower with an active load in various charging time

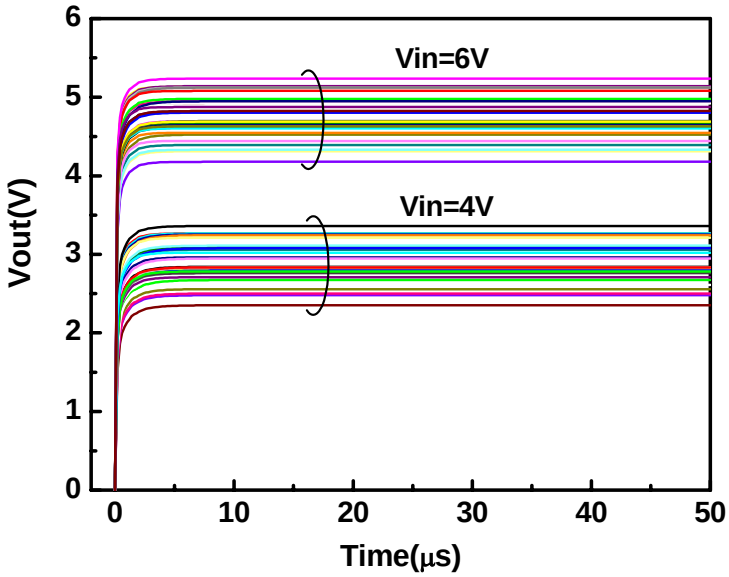


Fig. 2.18(a) Monte Carlo simulation for the source follower with an active load

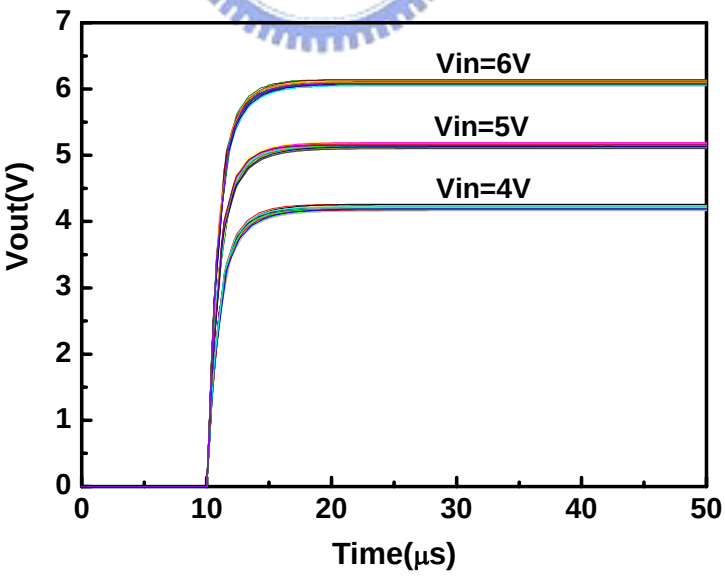


Fig. 2.18(b) Monte Carlo simulation for the proposed analogue buffer

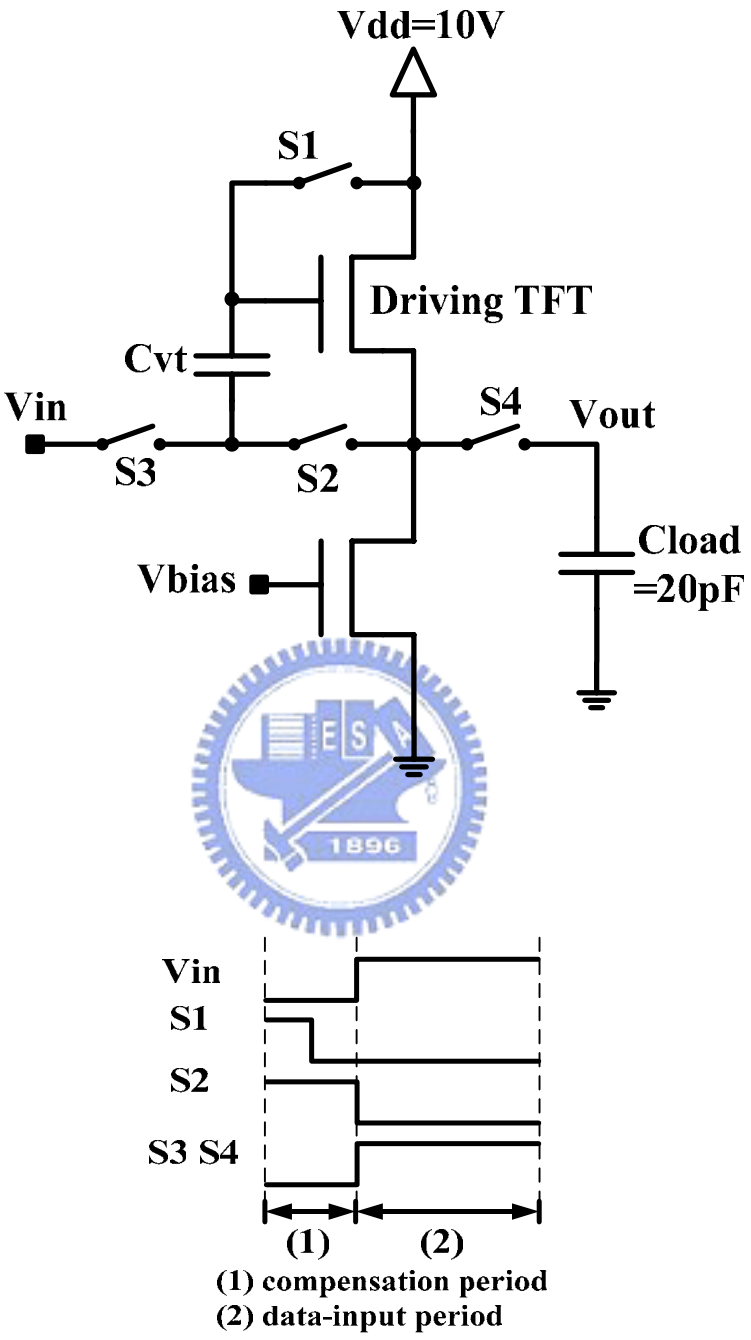


Fig. 2.19 Proposed analogue buffer and its timing diagram

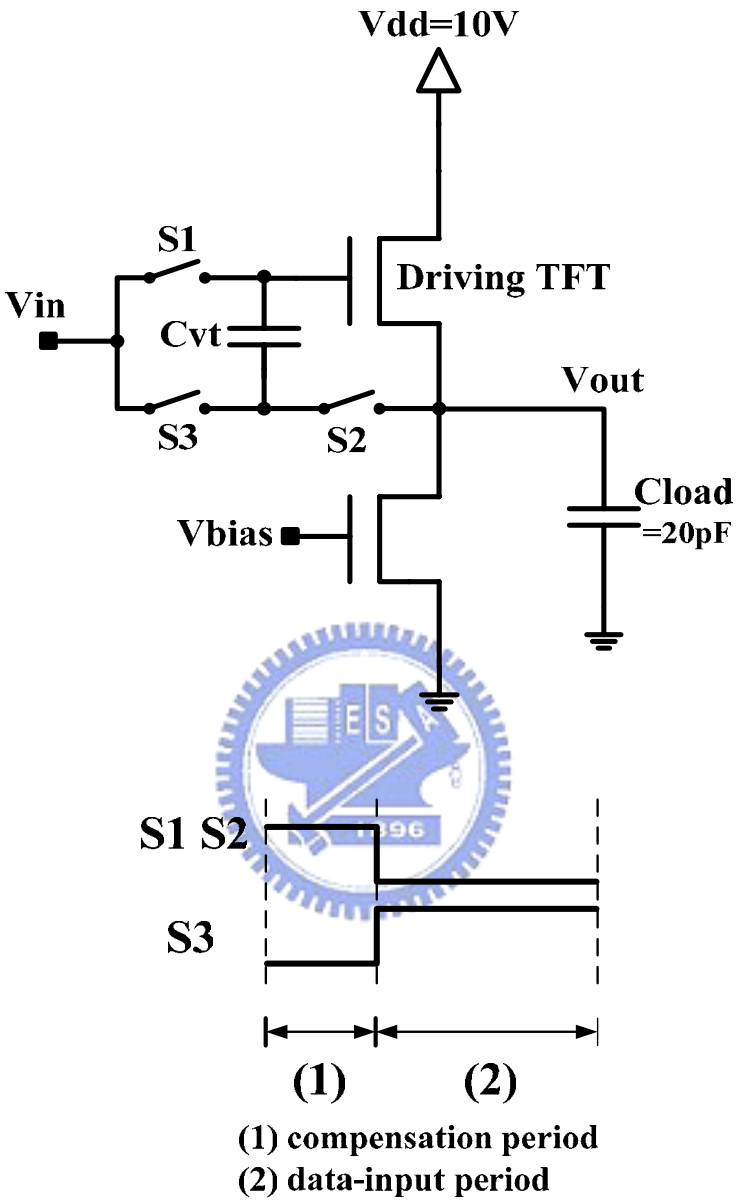


Fig. 2.20(a) Modified Chung's analogue buffer [6] with an active load and its timing diagram

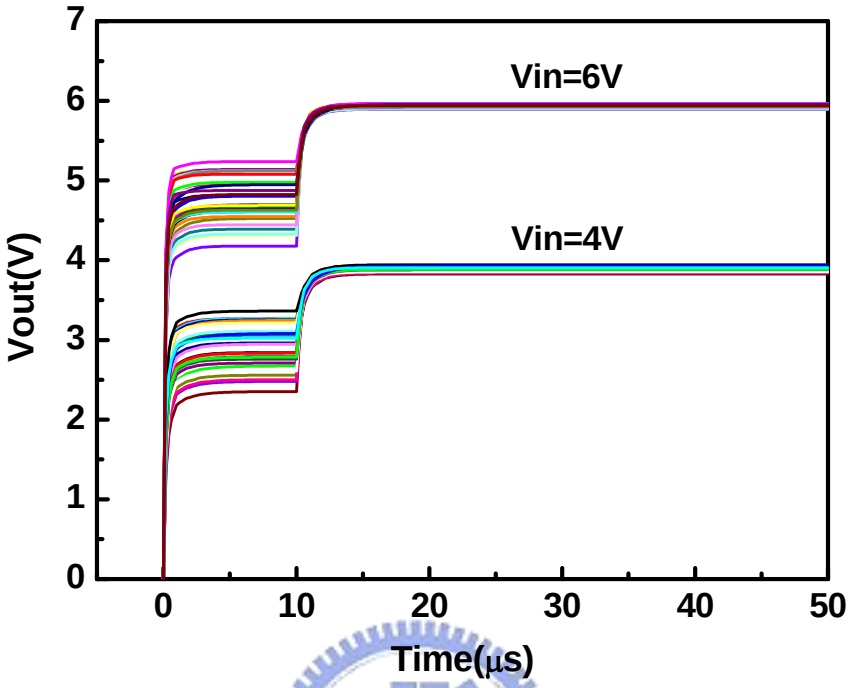


Fig. 2.20(b) Monte Carlo simulation results of the modified Chung's analogue buffer

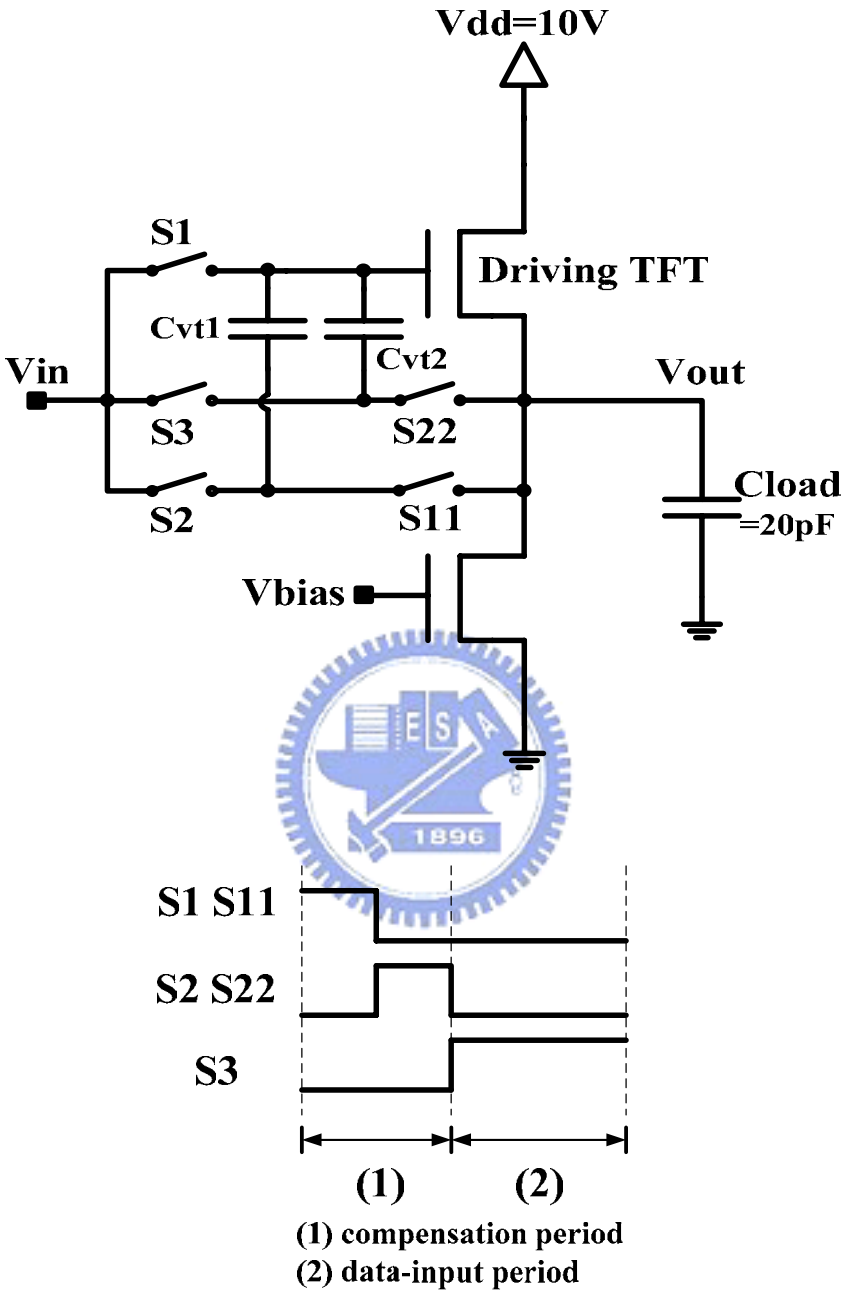


Fig. 2.21(a) Modified Kida's double offset canceling analogue buffer [7] with an active load and its timing diagram

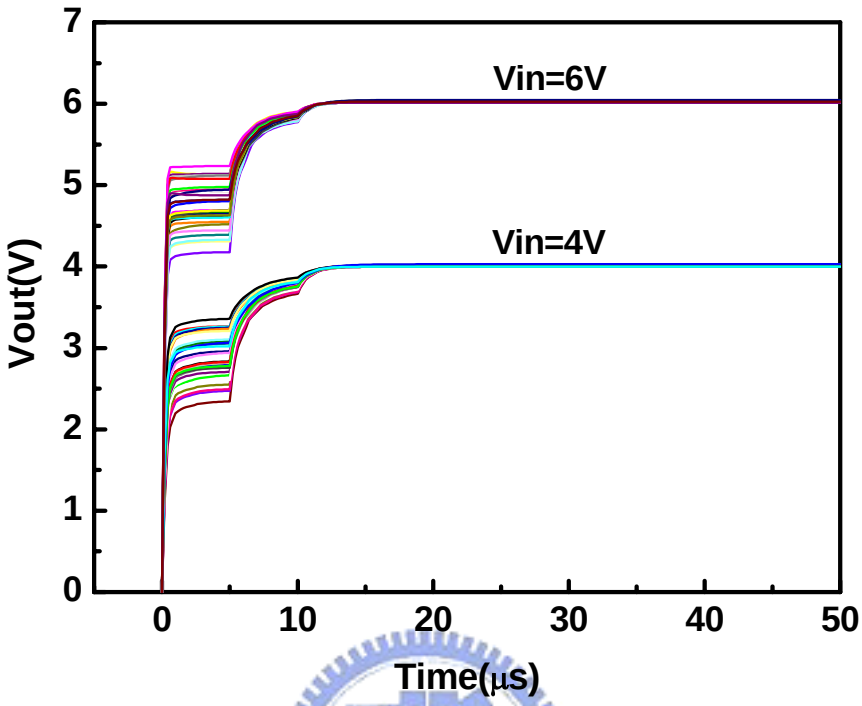


Fig. 2.21(b) Monte Carlo simulation results of the modified Kida's analogue buffer

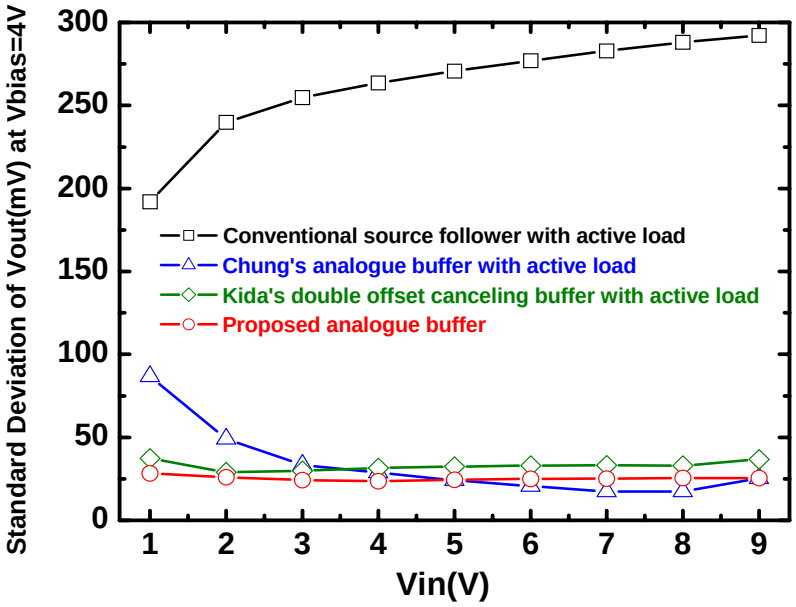


Fig. 2.22 Standard deviation of output voltage calculated from the Monte Carlo simulation results

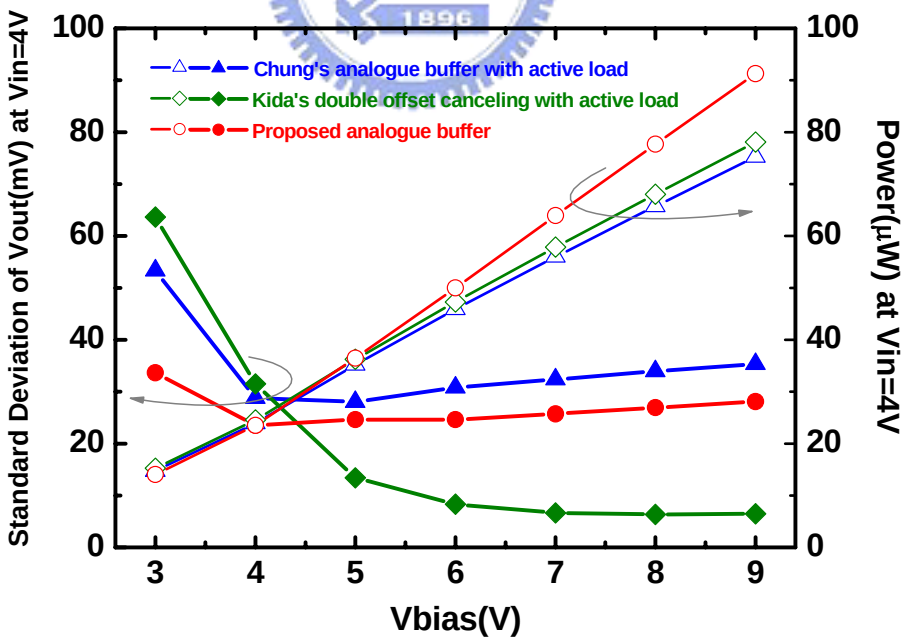


Fig. 2.23 The standard deviation of output voltage and the power consumption related to Vbias