國 立 交 通 大 學
光電工程研究所碩士班
碩 士 論 文

複晶矽薄膜電晶體晶粒邊界位障效應之研究

The Analysis of Grain Boundary Barrier Effect in Polycrystalline Silicon Thin-Film Transistors

研 究 生：丘兆仟
指導教授：冉曉雯 博士

中華民國九十四年六月

複晶矽薄膜電晶體晶粒邊界位障效應之研究

The Analysis of Grain Boundary Barrier Effect in Polycrystalline Silicon Thin-Film Transistors

研 究 生：丘兆仟　　Student：Chao-Chian Chiu

指導教授：冉曉雯 博士　　Advisor：Dr. Hsiao-Wen Zan

國 立 交 通 大 學

光電工程研究所碩士班

碩 士 論 文

A Thesis

Submitted to Institute of Electro-Optical Engineering

College of Electrical Engineering and Computer Science

National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of

Master

in

Electro-Optical Engineering

June 2005

Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 四 年 六 月

複晶矽薄膜電晶體晶粒邊界位障效應之研究

研究生： 丘兆仟　　指導教授： 冉曉雯 教授

國立交通大學

光電工程研究所碩士班

中文摘要

複晶矽薄膜電晶體在面板技術的應用上，由於其具有高遷移率，可以實現系統面板(System on Panel)的技術。為了要將周邊電路直接以複晶矽薄膜電晶體實現在玻璃基板上，與面板矩陣電路結合成所謂的系統面板，所以一個準確的元件物理模型是最重要的基礎。在本論文內，我們特別著重在複晶矽薄膜電晶體中，晶粒邊界位障(Grain boundary barrier)效應的研究。

首先，我們將元件處於各種不同的偏壓狀態，來研究此時的活化能特性，並提出一個新的活化能模型。然後，利用變化不同的通道長度和不同的薄膜品質，來萃取出模型中的各個參數。根據基本的元件模型和我們所研究的晶粒邊界位障效應，推導出元件的電性模型。模型產生的電性，可以準確描述元件在通道長度 5.5 μm – 31.5 μm的輸出特性。除了基本的電流輸出特性，我們也分析元件的載子遷移率和通道表面平坦度在不同偏壓下的變化，並利用前述的模型解釋晶粒邊界位障所造成的影響。

另外，我們觀察到了缺陷密度對於閘極電壓和通道厚度之間的關係有很大的影響。藉由製作不同品質的複晶矽薄膜，來清楚的探討這個現象，並建立模型來加以解釋。同時，我們也利用了元件模擬軟體來加以比較缺陷密度所產生的影

響。最後，我們成功建立了包含薄膜差異性、不同操作偏壓下對於元件特性影響的模型。

The Analysis of Grain Boundary Barrier Effect in Poly-Si TFTs

Student: Chao-Chian Chiu Advisor: Dr. Hsiao-Wen Zan

Institute of Electro-Optical Engineering

National ChiaoTung University

Abstract

Polycrystalline silicon thin-film transistors (TFTs) have been studied extensively for their applications on system-on-panel (SOP) technology. In order to integrate the peripheral driving circuitry onto the glass substrate, the accurate physical-based model for circuit design and simulation is needed. In this thesis, we especially focus on the analysis of grain boundary barrier effect in polycrystalline silicon thin-film transistors.

Firstly, the conduction behavior of Poly-Si TFTs had been carefully studied by analyzing their activation energy under different bias condition, and a new activation energy model has been proposed. Then, activation energy model parameters were extracted from devices with various channel length and film quality. An accurate I-V model was established by combining basic TFT model and the grain boundary barrier effects. The model had been verified for devices with channel length varied from 5.5 μm to 31.5 μm. The mobility and scattering behavior are also well explained by our proposed model.

The trapped charge screening effect of poly-Si film is also observed when the devices with large defect densities. We used various film quality devices to clarify this effect and established adequate model to explain this phenomena. Finally, the

influence of defect densities on the dependence between grain barrier and gate bias was examined by device simulation results. Good agreements are found when comparing the simulated results and the experimental results.

誌　謝

時光飛逝，轉眼間已過了兩個寒暑，在交大的碩士班求學期間，首先要感謝我的指導老師 冉曉雯教授，謝謝老師在學業與實驗上的指導與教誨，讓我在量測分析、論文寫作及未來規劃等方面獲益良多，同時也讓我在遇到瓶頸的時候能夠有所突破，而老師對於事物的遠見及胸襟更是我未來努力學習的方向，在此對老師致上內心最誠摯的敬意與謝意。

此外，也感謝實驗室陳世青學長、顏國錫學長、吳興華學長對我平時的照顧並給予我課業上的幫忙與建議，幫助我解決了不少問題。還有要感謝許多同學，像是一起為計畫而努力的士欽，協助我使用機台與實驗的中良，一起討論元件物理的凱傑、銘龍，一起去報告的學妹貞儀以及實驗室的許多夥伴，德章、政偉、士強、天山、士哲、承和、宏光、彥甫和學弟妹們，有了你們的陪伴，讓我不管是在做實驗或是研究中都充滿動力，也因為你們，讓我在電資大樓601實驗室的生活充滿歡樂。

最後，絕對不會忘記的，我要感謝我的父母多年來辛苦的栽培與教誨，在我求學階段中給予我無窮的支持與鼓勵，讓我能夠順利的完成我的學業，取得碩士學位，如果我有任何的榮耀，都是因為有你們無可取代的存在，在此我要獻上內心最深的謝意。

僅以此篇論文獻給我的老師、家人與好友

兆仟 2005　於交大電資

Contents

Figure Captions

Chapter 1.

Chapter 2.

Chapter 3.

Conclusion (a) temperature = 25 ℃ (b) temperature = 60 ℃.

Fig. 3-4-2 The comparison of experimental (symbols) and simulated (solid line) *I-V* output characteristics for $W/L = 6\mu m/5.5\mu m$ ELA poly-Si TFTs

Conclusion (a) temperature = 25 ℃ (b) temperature = 60 ℃.

Table Captions

Chapter 1

Introduction

1-1 An Overview of poly-Si TFTs Technology

In recent years, polycrystalline silicon thin-film transistors (polysilicon TFTs) present great interest for applications in static random access memories (SRAMs)[1], active matrix liquid crystal displays (AMLCDs)[2-6], high performance EEPROMs[7], and three-dimensional (3D) ICs[8].

However, some problems still exist in poly-Si TFTs. In comparison with single-crystalline silicon, poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously. Moreover, the relatively large leakage current is one of the most important issues of conventional poly-Si TFTs under OFF-state operation. To achieve poly-Si TFTs with low leakage current, high on current and high-performance, a number of techniques to enlarge the grain size at the channel region of a TFT have been developed, such as solid-phase crystallization (SPC)[9], laser crystallization [10] and metal-induced-lateral crystallization (MILC)[11].

Currently, the main application of poly-Si TFTs is the liquid crystal display (LCD). For poly-Si TFTs, carrier mobility larger than 100 cm^2/V-s is easily achieved by present mature technology, which is enough to be used as peripheral driving circuits [1]. The poly-Si TFT LCD integrates drivers into the structure, and therefore,

reduces the size of the total panel. The driver contact number of the poly-Si TFT LCD is more than one order of magnitude smaller than that of the a-Si:H TFT LCD. The poly-Si TFT plate also has a larger aperture ration in each pixel than that of the a-Si:H TFT plate, which allows a higher panel resolution. Most important, poly-Si TFTs can be used in existing products, such as the large area LCDs, to reduce the manufacturing cost or to increase the product reliability. In summary, the poly-Si TFTs will becomes more important in future technologies, especially when the 3-D circuit era is coming.

1-2 Defects in Poly-Si Film

Because the granular structure of the poly-Si film, there are many grain boundaries and intragranular defects exist in the film. The break in the lattice at grain boundary creates dangling bonds and also breaks the periodicity of the potential in the material. In other words, this means that the energy states are created at grain boundaries. They act as acceptor-like or donor-like states which depending on the position of the Fermi level in the band gap. Carriers trapped by these trap states can no longer contribute to conduction, which forms local depletion region and potential barriers in these grain boundaries. Therefore, the basic characteristics such as subthreshold swing, mobility, ON current and threshold voltage of poly-Si TFTs are inferior to MOSFET. As for the leakage current, it is well known that it increase with the drain voltage and gate voltage. The dominant mechanism of the leakage current is field emission via grain boundary traps due to the high electric field near the drain side. In order to minimize the defect densities in the poly-Si film, some useful method such as hydrogen plasma is to passivate these dangling bonds. As the number of trapped carrier decreases, the potential barriers in grain boundaries decrease.

1-3 The influences of grain structure on carrier transport

As previously mentioned, the poly-Si material contains a lot of grain boundaries. The device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. J.Y. Seto proposed the first credible model[12], and this simple grain boundary trapping model has been described by many authors in details[13-16]. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite, as Fig. 1-3-1. Figure. 1-2-1 gives a one-dimensional presentation of the energy band diagram for an n-type polycrystalline film having a constant grain size. The presence of active traps at grain boundaries induces a bend in the energy bands. Indeed, a space charge layer made of ionized doping atoms, donors in this case, is created on both sides of the grain boundaries to maintain the total neutrality and to compensate the equivalent trapped charges located at the grain boundary. In Figure 1-3-1, the space charge layer extension (clear zone) is smaller than the grain size; a part of the grain remains neutral (gray zone).

The model is based on the calculation of the energy barrier at grain boundaries, which affects the transport of electrons in the film. To calculate the energy barrier, the simplest way consists of solving the Poisson's equation in the grain.

Barrier height calculation

We consider the different following parameters:

- X, extension of the space charge region,
- N_D, donor doping atom concentration,
- N_{TA}, acceptor like trap surface density at grain boundaries,

- ε_0, permittivity in vacuum,
- ε_s, semiconductor permittivity,
- L_G, size of the grain,
- V, the electrostatic potential,
- x, the position coordinate,

The distribution of the charges in the material is schematically described in Fig. 1-3-2.

In the space charge region, $0 < x < \frac{X}{2}$ $\frac{d^2V}{dx^2} = -\frac{qN_D}{\varepsilon_r\varepsilon_0}$ (1-1)

Out of the space charge region, $\frac{X}{2} < x < \frac{L_G}{2}$ $\frac{d^2V}{dx^2} = 0$ (1-2)

At the border of the space charge region, the electric field is null: $[\frac{dV}{dx}]_{X/2} = 0$

$$0 < x < \frac{X}{2} \ : \ \frac{dV}{dx} = -\frac{qN_D}{\varepsilon_s\varepsilon_0}x + cst = \frac{qN_D}{\varepsilon_s\varepsilon_0}\left(\frac{X}{2} - x\right) \quad (1\text{-}3)$$

$$\rightarrow V(x) = -\frac{qN_D}{2\varepsilon_s\varepsilon_0}\left(\frac{X}{2} - x\right)^2 + V\left(\frac{X}{2}\right) \quad (1\text{-}4)$$

$$\frac{X}{2} < x < \frac{L_G}{2} \ : \ \rightarrow V(x) = V\left(\frac{X}{2}\right) \quad (1\text{-}5)$$

And the energy barrier height (E_B) is defined as the energy difference between the positions $x = 0$ and $x = \frac{X}{2}$.

$$V_B = -\left(V(0) - V\left(\frac{X}{2}\right)\right) = \frac{qN_D}{2\varepsilon_s\varepsilon_0}\left(\frac{X}{2}\right)^2 = \frac{qN_D}{8\varepsilon_s\varepsilon_0}X^2 \quad (1\text{-}6)$$

The value of X has to verify for the electrical neutrality of the global material, which means $XqN_D^+ = qN_{TA}^-$. N_{TA}^- is the ionized part of N_{TA}. The Seto's model defines a critical concentration (N_D^*), which corresponds to this limit:

$$\frac{X}{2} = \frac{L_G}{2} \ \rightarrow \ X = L_G \ \rightarrow \ N_D^* = \frac{N_{TA}}{L_G} \quad (1\text{-}7)$$

For a fixed trap density, if the effective doping concentration is higher than the critical concentration, the space charge extension is lower than the crystallite site.

$$N_D > N_D^* \ : \ X = \frac{N_{TA}}{N_D} \quad \text{and} \quad V_B = \frac{q}{8\varepsilon_s \varepsilon_0} \frac{N_{TA}^2}{N_D} \tag{1-8}$$

On the contrary, the crystallite is fully depleted.

$$N_D < N_D^* \ : \ X = L_G \quad \text{and} \quad V_B = \frac{qN_D}{8\varepsilon_s \varepsilon_0} L_G^2 \tag{1-9}$$

For partially-depleted poly-Si film, the carrier transport can be described by the thermionic emission over the barrier. Its current density can be written as[17]

$$J = qn\nu_c \exp[-\frac{q}{kT}(V_B - V)] \tag{1-10}$$

where ν_c is the collection velocity ($\nu_c = \sqrt{kT/2\pi m^*}$), n is the free-carrier density, V_B is the barrier height without applied bias, and V_g is the applied bias across the grain boundary region. For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier increases by an amount of $V_g/2$ in the reverse-bias. In the forward-bias direction, the barrier decreases by the same amount. In these two directions, the current density then can be expressed as

$$J_F = qn\nu_c \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_g)] \tag{1-11}$$

$$J_R = qn\nu_c \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_g)] \tag{1-12}$$

the net current density is then given by

$$J = 2qn\nu_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_g}{2kT}) \tag{1-13}$$

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, Eq. (1-13) then can be simplified as

$$J = 2qn\nu_c \exp(-\frac{qV_B}{kT})\frac{qV_g}{2kT} = \frac{q^2 n\nu_c V_g}{kT}[\exp(-\frac{qV_B}{kT})] \quad (1\text{-}14)$$

the average conductivity $\sigma = J/E = JL_g/V_g$ and the mobility $u = \sigma/qn$ then can be obtained

$$\sigma = \frac{q^2 n\nu_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \quad (1\text{-}15)$$

$$u = \frac{q\nu_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv u_0 \exp(-\frac{qV_B}{kT}) \quad (1\text{-}16)$$

where u_o represents the carrier mobility inside grain region. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap density.

In poly-Si TFTs, the carrier density n induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_T)}{qt_{ch}} \quad (1\text{-}17)$$

where t_{ch} is the thickness of the inversion layer. Therefore, the drain current I_D of poly-Si TFT then can be given by

$$\begin{aligned} I_D &= J \times W \times t_{ch} = (qun \times \frac{V_D}{L}) \times W \times \frac{C_{ox}(V_G - V_T)}{qn} \\ &= u_o C_{ox}\frac{W}{L}(V_G - V_T)V_D \exp(-\frac{qV_B}{kT}) \end{aligned} \quad (1\text{-}18)$$

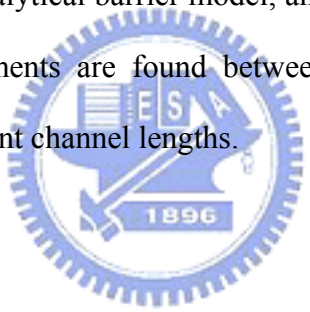
where drain voltage $V_D = V_g \times n_g = V_g \times L/L_g$. Obviously, this *I-V* characteristics is very similar to that in MOSFETs, except that the mobility is activated.

1-4 Motivation

As mentioned in 1-3, many models had been proposed to explain the transport mechanism in polycrystalline silicon film. The grain barrier trapping model and also the thermionic emission had been widely accepted to explain the energy band distribution and the related conduction behavior in poly-Si TFTs. However, the

barrier under various bias conditions and film qualities has not been compared before. Therefore, in this paper, the activation energy for devices operated in turn-on region is extracted and compared. The measured results are consistent with the proposed grain barrier trapping model. Except turn-on characteristics, we also studied the cut-off region activation energy for devices with or without lightly-doped drain (LDD) structure.

It is found that the trapped-charge screening effect is also an important parameter that cause the grain barrier behavior differs for devices with different poly-Si thin film. For this reason, the influence of thin film property on activation energy is studied carefully, and it was also examined by ISE-TCAD device simulation. Finally, a physically-based analytical barrier model, and accordingly a new *I-V* model are established. Good agreements are found between experimental and simulated results for devices with different channel lengths.



1-5 Thesis Outline

This thesis is organized into the following chapters:

In the chapter 1, a brief overview of thin-film transistor technology is introduced to describe the various applications. Then, the meaning of grain barrier height is discussed and its equation is deduced based on the Seto's model. The motivation of the studies is also described here.

In the chapter 2, the process flow of poly-Si films with different conditions is introduced. We measured activation energy of thin film transistor with different bias, and studied the trapping effects and the DIGBL effects. Then, a physically-based activation energy model has been proposed and verified. The turn-on and cut-off

region activation energy of devices with or without LDD structure was also compared in this paper.

In the chapter 3, we studied the influence of the trap charge screening effect on the grain barrier. Comparisons between simulated and measured date are also demonstrated and discussed. Then we established a channel thickness model for poly-Si TFTs. And we compared the mobility model with different assumptions. Finally, a new activation energy model considering not only DIGBL effect but also charge screening effect had been established and implemented into the device *I-V* model.

In the chapter 4, the results of our experiments and analysis are concluded.

Chapter 2

Analysis of Thermal Activation Energy for Poly-Si TFTs

2-1. Device fabrication

In this paper, we use two groups of devices. The figure 2-1-1 shows that cross-sectional view of a poly-Si TFT. The first-group devices are typical top-gated structure which fabricated on glass substrate. Except conventional devices without LDD/offset structure, devices with 0.75-μm-thick LDD region are also fabricated. The poly-Si film is crystallized by excimer laser annealing (ELA). The thickness of poly-Si film and the oxide film were 50 *nm* and 100 *nm* respectively. The device channel length varies from 5.5 μm to 31.5 μm when the channel width is fixed as 6, 10, 30 μm.

The second-group devices are fabricated on silicon wafer with 500-*nm*-thick buffer oxide. Device structure is also the typical top-gated structure. To investigate the influence of film properties on device characteristics, the poly-Si film is formed by as-deposited process and also the solid phase crystallization (SPC) process. The thickness of poly-Si film and the oxide film were 100*nm* and 50*nm* respectively. It is known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. Therefore, in order to further moderate the trap density of the poly-Si film, some devices are passivated by NH_3 plasma for 1 and 2 hours at 300 ℃.

2-2. Unified activation energy model

In chapter 2, we analysis the thermal activation energy mainly by using the first group devices, and discussed the thin film properties (chapter 3) by using these two groups. The activation energy (E_a) of the on current was obtained from the slope of Arrhnius plot (Fig. 2-2-1) of drain current. The data, which was taken over a temperature range from 25℃ to 130℃, follow a straight line. This allows accurate determination of E_a. The turn-on region activation energy for a conventional poly-Si TFT is plotted in Fig. 2-2-2. It is observed that when gate voltage is high, the activation energy is very low and is almost independent of the drain bias. When the gate voltage is just above threshold voltage, the activation energy increases with increasing drain bias in linear region, reaches a peak value at the onset of channel pinch-off (V_D=V_{DSAT}~V_G-V_T), and then decreases in the saturation region. The former phenomenon can be accounted for the scattering effect since the activation energy is lower than thermal energy and even turns to be negative when gate voltage is higher than 12 V. The latter phenomenon, which will be discussed as follows, can be addressed for the changing of grain boundary barrier under different bias conditions. It is well-known that the conduction behavior of poly-Si TFTs exhibits a thermionic emission character. The effective mobility is therefore modified by

$$\mu_{eff} = \mu_0 \exp(\frac{-E_B}{kT}) \qquad (2\text{-}1)$$

where V_B represent the grain boundary barrier height that can be expressed by Eq. (2-2) in above-threshold region. N_T represents the effective grain boundary trap density and n is the gate-induced carrier density,

$$V_B = \frac{qN_T^{\,2}}{8\varepsilon n} \qquad (2\text{-}2)$$

As a result, the measured activation energy can be served as the grain boundary energy barrier when there is no other temperature-sensitive mechanism. When drain voltage is increased, it has been proposed that the potential barrier is lowered as shown in Fig. 2-2-3, which is called drain-induced grain barrier lowering (DIGBL) effect [18,19]. When the device is operated in the linear region and the drain voltage is low, the barrier increases with increasing drain voltage. This can be explained by the influence of drain bias on the surface potential along the channel. The average carrier density is therefore expressed as [20]

$$n = C_{ox}(V_G - V_{fb} - \alpha V_D)/qt_{ch} \tag{2-3}$$

where C_{ox} is the gate oxide capacitance per unit area, V_{fb} is the flatband voltage, and α is a parameter indicating the influence of drain voltage. The channel thickness is expressed as

$$t_{ch} = 8V_{th}t_{ox}\sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}(V_G - V_t)}} \tag{2-4}$$

where t_{ox} is the oxide thickness, V_{th} is the thermal voltage, and V_t is the threshold voltage. Many authors assumed that the channel thickness was constant and equal to the thickness of the polysilicon film t. However, this simplifying assumption is permissible only for very thin films (t < 10 nm). Contrary to this assumption, the other authors assumed that the t_{ch} was proportional to $(V_G\text{-}V_t)^{-1}$ [21]. This definition is to define the channel thickness as the thickness at which 80 percent of the total charge, induced by the gate. However, by substituting the second assumption into Eq. (2-5) to fit the experimental curve of the activation energy versus V_D at V_D = 0.1 V point, it was found that the channel thickness in ELA poly-Si TFTs should be proportional to $(V_G\text{-}V_t)^{-0.55}$ rather than $(V_G\text{-}V_t)^{-1}$ in single crystal MOSFETs. This may be due to the inferior control ability of gate voltage on channel carrier in poly-Si

TFTs. Screening effect related to interface charge and trapped charge is plausible reason to explain the wider channel thickness in poly-Si TFTs, and we will give a detail discussion in chapter 3.

When drain voltage increases, from Eq. (2-2) and (2-3), we can conclude that the grain boundary barrier is higher due to the reduced carrier density. Fig. 2-2-4 compares the activation energy measured under different drain biases. The increase of barrier with increasing drain voltage is obviously observed again when the gate voltage is lower than 8 volt. According to the grain boundary barrier height given by Ref.[22], the barrier height considering the influence of the drain voltage and the DIGBL effect (Fig. 2-2-3) is given by

$$E_B = \frac{t_{ch}[(qN_T)^2 - 4qN_T\varepsilon_s\eta\frac{V_D}{L}]}{8\varepsilon_s C_{ox}(V_G - V_T - \alpha V_{DSe})} \tag{2-5}$$

where η is an nonlinear factor of the electric field for the DIGBL effect. For simplicity, the models for all regimes of operation should be combined into a single expression which is everywhere continuous and smooth. This is accomplished by defining effective drain voltages as [23],

$$V_{DSe} = \frac{V_{DS}}{[1+(\frac{V_{DS}}{V_{sat}})^m]^{\frac{1}{m}}} \tag{2-6}$$

V_{DSe} is approximately V_{DS} for $V_{DS} < \alpha_{sat}V_{GT}$, but remains constant at V_{sat} in saturation; m is a fitting parameter that controls the transition from V_{DS} to V_{sat}. The calculated results of drain current activation energy with different gate voltage are compared with experimental results in Fig. 2-2-2(a). It is observed that the simulated activation energy at low gate bias (e.g., V_G = 4 V, 6 V and 8 V) agrees very well with the experimental measurements. From Eq. (2-4)(2-5) and Table I, it is shown that when drain voltage is not high enough, the influence of DIGBL is not pronounced. And it

demonstrated that the activation energy increases with increasing drain bias in the linear region; however, the influence of the DIGBL becomes predominant in the saturation region. The combination of the two effects has been correctly modeled by Eq. (2-5). Our model fits the activation energy of a wide range of channel length using only the parameter values shown in Table I. So in contrast to previous studies that considered only the influence of the gate voltage, we have successfully demonstrated that by considering both the influence of the gate and drain voltage simultaneously, the grain barrier height can be simulated accurately over a wide range of drain bias.

The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so the first order I-V relation in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}[(V_G - V_T)V_{DSe} - \frac{V_{DSe}^2}{2\alpha_{sat}}] \quad (2\text{-}7)$$

where

W is the channel width,

L is the channel length,

V_T is the threshold voltage,

α_{sat} account for velocity saturation, that reduces the value of the saturation voltage as the channel length is decreased.

By combing our activation energy model and drain current Eq. (2-7), the simulation I_D-V_D curve versus measured data is shown in Fig. 2-2-5. The agreement with the measurement results is good.

2-3. Method of parameter extraction

In this section, we will introduce the methods of parameter extraction. And in section 2-4 we will compare and discuss the extracted parameters with different channel length. The current-voltage characteristic measurement of thin film transistor devices was performed by HP 4156A semiconductor parameter analyzer with source grounded.

Plenty ways are used to determinate the threshold voltage which is the most important parameter of semiconductor devices. Here, the method to determinate the threshold voltage is the *constant drain current method* that the voltage at a specific drain current I_N is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can be give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current $I_N = I_D/(W_{eff}/L_{eff})$ is specified at 10 nA for V_D = 0.1 V and 100 nA for V_D = 5 V in most papers to extract the threshold voltage of TFTs.

Because the influences of the lower drain bias on the activation energy can be neglected, therefore, by best fitting the experimental curve of the activation energy versus V_D at V_D = 0.1 V point and invoking Eq. (2-5), N_T can be extracted. By optimizing the fitting results with Eq. (2-5), m, α and V_{sat} can be extracted. η, extracted from $V_{sat} \leqq V_D$ regime by using Eq. (2-5) with the parameters extracted previously. All parameters extracted for the model are shown at Table I.

2-4. Physical meanings of the extracted parameters

It should be noted that α and η increases with decreasing channel length are due to the influence of drain bias on the surface potential along the channel increasing.

Figure 2-4-1 and 2-4-2 compare the influence of parameter α and η on the simulated activation energy (W/L = 6μm/13.5μm). When the device is operated in the linear region and the drain voltage is low, the barrier increases with increasing drain voltage, therefore, the trapping effects is the dominant mechanism. In Fig. 2-4-1, we can observe that the trapping effect influences the slope and the peak values of the activation energy in the linear region. Figure 2-4-2 shows the activation energy increases with decreasing η, especially at high drain biases. And it was due to the drain-induced grain barrier lowering (DIGBL) effect.

At high gate bias, the simulated activation energy at high gate bias is overestimated. This is because that the scattering effect rather than the grain boundary trapping effect dominates device activation energy. As a result, measured activation energy tends to become very low and even become negative value. The discrepancy under high gate voltage, however, is negligible since the barrier height is already very low and has trivial influence on device performance.

2-5. The turn-on region activation energy with different LDD length

The turn-on region activation energy of devices with or without LDD structure was also compared in this section. As shown in Fig. 2-5-1, it is observed that when the devices have LDD structure, the activation energy is higher than the devices without LDD structure. And its dependence on drain bias has not so obviously. This may due to the LDD structure significantly suppresses the drain side electric field[24], so the influence of drain bias on activation energy was also decreased. Because the influence of the trapping effects and the DIGBL effects was decreased, it makes the

activation energy become higher, as we observed.

2-6. The cut-off region activation energy with or without LDD structure

It is well-known that, when drain electric field increases, the dominant leakage current mechanism changes from thermionic emission, thermionic field emission, to pure tunneling [25]. This phenomenon can be observed in Fig. 2-6-1(a), at a low drain field (0.1 V), the lowest activation energy is 0.52 eV. Since the E_a is about $E_g/2$, thermionic emission is the dominant leakage current mechanism at low field. As the drain bias increases, the drain depletion field increases and E_a decreases. This suggest that the high field in the drain depletion region has reduced the barrier that carrier must overcome. As such, the dominant leakage current mechanism is thermionic field emission. This process could be accomplished by combination of emission and tunneling processes. Further increase of the drain bias, there are almost no barrier to the carrier motion, so the dominant leakage mechanism is pure tunneling.

For devices with LDD structure, however, the variation of activation energy with increasing drain and gate bias is much more suppressed (Fig. 2-6-1(b)). We use ISE-TCAD simulator, as in Fig. 2-6-2, to compare the maximum drain electric field for devices with and without LDD structure. It is found that the LDD structure significantly suppresses the electric field and its dependence on gate bias. This gives a conclusion that, with LDD structure, the leakage current mechanism can be dominated by thermionic emission effect only.

Chapter 3

Modeling through thin film properties

3-1. Trapped charge screening effect

In order to test the validity of the grain-barrier height model in various film quality, the poly-Si film is formed by excimer laser annealing (ELA), as-deposited process and also the solid phase crystallization (SPC) process. The curve of E_B versus V_G is shown in Fig. 3-1-1, and the curve of E_B and 1/ E_B versus V_G for different film quality is shown in Fig. 3-1-2(a) and (b). Due to the inverse of grain barrier is proportional to the gate voltage, it is found that the channel thickness is constant in as-deposited devices. However, the channel thickness is not constant in ELA devices. Therefore, the channel thickness is a important point that we must study carefully. For MOSFET devices, the estimated channel thickness is reversely proportional to the gate bias and can be expressed as [21]:

$$t_{ch} = \frac{8V_{th}t_{ox}\sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}}}}{V_G - V_T} \tag{3-1}$$

where t_{ox} is the oxide thickness and V_T is thermal voltage. However, because there are still many defects in poly-Si TFTs, some electric fields emanating from the gate electrode may be terminated by the trapped charge, as shown in Fig. 3-1-3. This screening effect becomes more pronounced with increasing the trap density. As a result, the bulk depletion charges far away from the SiO_2/Si interface cannot be "seen" by the gate electrode. Therefore, only the effective depletion charges near the surface region can terminate the electric field lines originated from the gate electrode.

For this reason, the effective normal surface electric field in a poly-Si TFTs is sensitive to the variations of the trap density, and the channel thickness would be further affected. This feature is called the trapped-charge screening effect. Accordingly we modified the channel thickness as

$$t_{ch} = \frac{8V_{th}t_{ox}\sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}}}}{(V_G - V_T)^{\gamma-1}} \tag{3-2}$$

where γ is the parameter that represents the trapped charge screening effect. Finally, by substituting Eq. (2-5) into Eq. (3-2), grain barrier height model of poly-Si TFT is expressed as:

$$E_B = \frac{t_{ox}V_{th}(q^2 N_T{}^2 - 4qN_T\varepsilon_s\eta\frac{V_D}{L})}{\sqrt{\varepsilon_{ox}\varepsilon_s}C_{ox}(V_G - V_T - \alpha V_{DSe})^{\gamma}} \tag{3-3}$$

The curves of E_B versus V_G and $1/E_B$ versus V_G for devices with different film properties are shown in Fig. 3-1-4(a) and (b), where E_B is obtained from the Arrhenius plot for the drain-source current. It should be noted that there is a strong scattering effect when the devices are measured at high gate voltage and high temperatures. We should be careful not to include these data into the extraction of grain barrier height. As shown in Fig. 3-1-4(b), the inverse grain barrier height of the as-deposited device is linearly proportional to the gate voltage. This indicates that the trapped charge screening effect is serious and the channel thickness keeps constant is not dependent on gate voltage (γ=1). For the devices with SPC or ELA recrystallized poly-Si films, it is obviously that there is a nonlinear relation between the inverse grain barrier height to the gate voltage, which suggests that the screening effect is more suppressed and the channel thickness depends on the gate voltage ($\gamma > 1$). Table II lists values of γ for different grain growth conditions. As mentioned in 2-2, it should be pointed out

that care must be taken when comparing the values for N_T calculated by different poly-Si film quality. If the channel thickness was assumed constant (γ=1) and equal to the thickness of the polysilicon film t, due to the channel thickness t_{ch} is usually about 10 times smaller than the film thickness, the extracted Q_T will be underestimated. However, if the authors assumed that the t_{ch} was proportional to $(V_G\text{-}V_t)^{-1}$ [21], γ=2, the calculated Q_T will be overestimated, especially in high defect density poly-Si film (Tabel III). The improved fitting is illustrated in Fig. 3-2-1, and demonstrated that the modified channel thickness model allows the determination of precise values for N_T. This precision allows one to study very accurately the influence of variations in processing conditions on N_T. As shown in Table II, the trap density of ELA sample is $6.9\text{x}10^{11}$ (cm^{-2}), and is the best film quality compares to other. The trap density of no passivation as-deposited sample is $2.42\text{x}10^{12}$ (cm^{-2}), and is the worst film quality as expected. It is well known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. The calculated N_T also shows that the passivated devices have the smaller trap density by invoking the modified channel thickness model.

To observe the trapped-charge screening effect more clearly, we use ISE-TCAD simulator to study the channel carrier distribution in poly-Si film by changing the trap density as in Fig. 3-1-5. When defining the channel thickness (t_{ch}) as the depth at which maximum electron density has decreased to 20%, we can compare the influence of trap density on channel thickness as in Fig. 3-1-6(a). Figure 3-1-6(a) shows the dependence of the channel thickness t_{ch} on variation of the trap density. The channel thickness definition in MOSFET is defining the channel thickness (t_{ch}) as the depth at which maximum surface potential has decreased one thermal voltage. If we adopted this assumption, the similar result was also observed, as shown in Fig.

3-1-5(b). It is found that larger trap density significantly decreases the dependence of t_{ch} on gate voltage. This gives a conclusion that, electric fields emanating from the gate electrode may be terminated by the trapped charge, and this effect increases with increasing the trap density.

3-2. Method of parameter extraction

γ, V_T, N_T extraction: Firstly, by using long channel length device (ex. L = 30 *um*) under small V_D bias, γ can be defined by best fitting of the E_B vs. V_G curve as in Fig. 3-2-1. Then the N_T can be extracted from the slope of the curve. It is found that γ is closer to 2 when the film property is better. This proves the above screening effect mechanism. Table II lists values of γ for different grain growth conditions. Figure 3-2-2 shows that the line merges at x-axis. The value of x-axis is defined as the threshold voltage V_T [26].

α, η extraction: By increasing V_D bias, the x-axis intersection of the $E_B^{-1/\gamma}$ vs V_G curve will shift to larger x value. This relationship gives the α value. As seen in Fig. 3-2-3, the slope of the curve is defined as α. After the determination of γ, V_T, N_T and α, η can be obtained by calculation from the experimental data.

3-3. Discussion of mobility modeling

The mobility in polysilicon TFT's has been shown to be dependent on the grain size and grain boundary structure [13][27][28]. Seto observed a minimum in the mobility for polysilicon resistors at a critical doping concentration [13]. A corresponding behavior can be observed in polysilicon TFT's; as shown in Fig. 3-3-1, where the effective mobility for electrons is plotted against the gate voltage. In case of

rather small-grain polysilicon TFT, the effective mobility is given by

$$\mu_{eff} = \mu_0 \exp(\frac{-E_B}{kT}) \tag{3-4}$$

But when the polysilicon grain size increases, this equation is no longer valid. Therefore, we adopt a model [29] that separates grain and grain boundaries taking into account the average number of grain boundaries into the channel. It is demonstrated that this model is useful for two main reasons: first because grain and grain boundary regions exhibit different dependencies against technological parameters. Therefore, this model serves to optimize polysilicon TFTs technology. Second, this model leads to a better physical understanding of the functioning of large-grain polysilicon TFTs in the linear regime of operation, and it is reliable within a temperature range from 150 K to 300 K. By considering that the grain region behaves as in a bulk MOSFET, the mobility model can be defined as [29]

$$\frac{1}{\mu_{FET}} \equiv \frac{1}{\mu_G} + \frac{1}{\mu_0 \exp\left(\frac{-E_B}{kT}\right)} \tag{3-5}$$

where μ_0 represents the intrinsic mobility in the grain region; μ_G stands for the influence of scattering effect on mobility under large gate voltage. This mobility model given in Eq. (3-5) is plotted with measured values of μ_{FET} in Fig. 3-3-1. A reasonable fit is observed.

In order to test the validity of this model at various temperatures, we performed electrical measurements in linear regime (V_D = 0.1 V) in the temperature range from 300K to 370K, as shown in Fig. 3-3-2. Applying Eq. (3-5), we extracted the device parameters at temperature of 300 K. Considering that the extracted parameters are not modified with temperature, and by changing only the value of temperature T in Eq. (3-5) we obtained a similar tendency (Fig. 3-3-3) between the theoretical model and the experimental data. It demonstrates that this model can provide reliable predictions

for mobility variation under various temperatures. The most important is that as temperature increases, the field effect mobility μ_{FET} increases without incorporating other empirical equations.

3-4. Out-put characteristics

Above threshold, the drain current, I_D, is given by [23]

$$I_D = \mu_{FET} C_{OX} \frac{W}{L}[(V_G - V_t)V_{DSe} - \frac{V_{DSE}^{\ 2}}{2\alpha_{sat}}] \tag{3-6}$$

Finally, we combine the proposed mobility model in Eq. (3-5) into the *I-V* model in Eq. (3-6). The calculated results and the measured results for devices at different temperature are depicted in Fig. 3-4-1 and Fig. 3-4-2. The validity of the proposed model within a temperature range from 300 K to 370 K is demonstrated. Good agreement is found to verify our proposed model.

Chapter 4

Conclusion

In this thesis, first, the thermal activation energy in typical top-gated poly-Si TFTs with LDD structure was studied. Then, we demonstrated the poly-Si TFT modeling incorporating with the experimentally defined grain barrier height model. Due to the bias condition had influences on grain barrier, the trapping effects dominate activation energy in linear region, while the DIGBL effect was pronounced in saturation region. A simple analytical model is proposed to present these effects. By considering both the trapping effects and the DIGBL effects, excellent fitting with experimental data is achieved over a wide range of drain bias and channel length. Simulations were also performed showing that LDD structure influences the maximum electric field seriously.

Then, in order to investigate the influence of film properties on device characteristics, the poly-Si film is formed by as-deposited process and also the solid phase crystallization (SPC) process. It was found that film property had influences on grain barrier and therefore strongly affected the device characteristics. Consequently, we established a modified channel thickness model to fit the inverse of grain barrier height. When comparing the measured data and the simulated results, good agreements were found for devices with different channel length.

References

[1] S. D. S. Malhi, H. Shichijio, S. K. Banerjee, R. Sundaresan, M. Elahy, G. P. Polack, W. F. Richardaon, A. h. Shah, L. R. Hite, R. H. Womoack, P. K. Chatterjee, and H. W. Lan, "Characteristics and Three-Dimenssional Integration of MOSFETs in Small-Grain LPCVD Polycrystalline Silicon,'' *IEEE Trans. Electric Devices*, Vol.32, No.2, pp.258-281, 1985.

[2] A. G. Lewis, I-W. Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, "Active matrix liquid crystal display design using low and high temperature processed polysilicon TFTs,'' *IEDM Tech. Dig.*, 1990,pp.843-846

[3] Y. Matsueda, M. Ashizawa, S. Aruga, H. Ohshima, and S. Morozumi, "New technologies for compact TFT LCDs with high-aperture ratio,'' *soc. Information Display, Tech. Dig.*, pp, 315-318, 1990.

[4] R. G. Stewart, S. N. Lee, A. G. Ipri, D. L. Jose, D. A. furst, S. A. Lipp, and W. R. Roach, "A 9V polysilicon LCD with integrated gray-scale drivers," *soc. Information Display, Tech. Dig.*, pp, 319-322, 1990.

[5] I. W. Wu, "Cell design considerations for high-aperture-ratio direct-view and projection poly-Si TFT-LCD's," *Dig. Tech. Papers, SID*, 1995, pp. 19-22.

[6] H. Oshima, and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates," *IEDM Tech. Dig.*, 157 (1989).

[7] K. YoShizaki, H. Takahashi, Y. Kamigaki, T.Yasui, K. Komori, and H. Katto, *ISSCC Digest of tech. Papers*, p.166, February 1985.

[8] Y. Takao, H. Shimada, N. Suzuki, Y. Matsukawa, and N. Sasaki, "Low-power and high-stability SRAM technology using a laser-recrystallized p-channel SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 39, pp. 2147-2152, Sept. 1992.

[9] T. Noguchi, “Appearance of single-crystalline properties in fin-pat-terned Si TFTs by solid phase crystallization,” *Jpn. J. Appl. Phys.*, pt.2, vol. 32, no. 11A, pp. 1584-1587, Nov. 1993.

[10] N. Kubo, N. Kusumoto, T. Insushima, and S. Ymaazaki, “Characterization of polycrystalline-Si thin-film transistors fabricated by excimer laser annealing method,” *IEEE Trans. Electron Devices*, vol. 40, pp. 1876-1879, Oct. 1994.

[11] S.-W. Lee and S.-K. Joo, “Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization,” *IEEE Electron Device Lett.*, vol. 17, pp. 160-162, Apr. 1996.

[12] J. Y. Seto, “The electrical properties of polycrystalline silicon films,” *J. Appl. Physics*, 46, 5247, 1975.

[13] H. Lhermite, O. Bonnaud, Y. Colin, A. Mercier, “Analysis of the field effect in a metal-oxide-semiconductor small grained silicon structure: experimental and modeling,” *IEEE trans. on ED.*, ED 35, 675, (1988).

[14] G. Baccarani, B. Ricco, G. Spadini, “Transport properties of polycrystalline silicon,” *J. Appl. Phys.*, 49,565 (1978).

[15] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, “Conductivity behavior in polycrystalline semiconductor thin film transistors,” *J. Appl. Physics*, Vol. 53, pp.1193-1202, 1982.

[16] H. N. Chern, C. L Lee, and T. F Lei, “An Analytical Model for the Above-Threshold Characteristics of Polysilicon Thin-Film Transistors,” *IEEE Trans. Electron Devices*, Vol. 42, No. 7, JULY 1995.

[17] ”Polycrystalline silicon for integrated circuits and displays”, second edition, written by Ted Kamins, pp.200-210.

[18] P. S. Lin, J. Y. Guo, and C. Y. Wu, "A quasi-two-dimensional analytical model for the turn-on characteristics of polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, Vol. 37, No. 3, March 1990.

[19] H. L. Chen, C. Y. Wu, "A New I-V Model Considering the Impact-Ionization Effect Initiated by the DIGBL Current for the Intrinsic n-Channel Poly-Si TFT's," *IEEE Trans. Electron Devices*, Vol. 46, No. 4, April 1999.

[20] H. W. Zan, T. C. Chang, P. S. Shih, D. Z. Peng, T. Y. Huang, and C .Y. Chang, "Analysis of Narrow Width Effects in Polycrystalline Silicon Thin Film Transistors," *Jpn. J. Appl. Phys.*, Vol. 42 (2003) pp. 28-32

[21] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and Electrical Properties of Undoped Polycrystalline Dilicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, Vol. 36, No. 9, September 1989.

[22] G. Y. Yang, S. H. Hur, and C. H. Han, "A Physical-Based Analytical Turn-On Model of Polysilicon Thin Film Transistors for Circuit Simulation," *IEDM*, pp.953-956 1995.

[23] M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack, and B. Iniguez, "A Short-Channel DC SPICE Model for Polysilicon Thin-Film Transistors Including Temperature Effects," *IEEE Trans. Electron Devices*, Vol. 46, No. 6, June 1999.

[24] K. Y. Choi, and M. K. Han, "A novel gate-overlapped LDD poly-Si thin-film transistor," *IEEE Electron Devices Lett.*, Vol. 17, pp. 566-568, 1996.

[25] K. R. Olasupo, and M. K. Hatalis, "Leakage Current Mechanism in Sub-Micron Polysilicon Thin-Film Transistors," *IEEE Trans. Electron Devices*, Vol. 43, No. 8, AUGUST 1996.

[26] Hsin-Li Chen; Ching-Yuan Wu, “An Analytical Grain-Barrier Height Model and Its Characterization for Intrinsic Poly-Si Thin-Film Transistor” *IEEE Trans. Electron Devices*, Vol. 45, No. 10, OCTOBER 1998.

[27] R. E. Proano, and D. G. Ast, “Effects of the presence/absence of HCl during the gate oxidation of the electrical and structural properties of polycrystalline silicon thin film transistors,” *J. Appl. Phys.*, Sept. 1989.

[28] W. C. Chan, and C. H. Chan, “An Empirical Model to Determine the Grain Size of Metal-Induced Lateral Crystallized Film,” *IEEE Trans. Electron Devices*, Vol. 49, No. 8, AUGUST 2002.

[29] F. V. Farmakis, J. Brini, G. Kamarinos, C. T. Angelis, C. A. Dimitriadis, and M. Miyasaka, “On-Current Modeling of Large-Grain Polycrystalline Silicon Thin-Film Transistors,” *IEEE Trans. Electron Devices*, Vol. 48, No. 4, APRIL 2001.

TABLE I

PARAMETERS USED TO SIMULATE THE E_B-V_D CHARACTERISTICS WITH DIFFERENT CHANNEL GEOMETRY.

W (μm) / L (μm)	6 / 7.5	6 / 10.5	6 / 13.5	30 / 31.5
N_T (cm^{-2})	9×10^{11}	7.4×10^{11}	7.21×10^{11}	6.91×10^{11}
α	0.8	0.78	0.765	0.72
η	2.17	2.43	2.49	2.6

TABLE II

Key Parameters of Grain Barrier Model for devices with different film properties

	γ	N_T ($10^{12}cm^{-2}$)	V_T (V)
As-Deposited (plasma=0 Hrs)	1	2.42	5.11
As-Deposited (plasma=2 Hrs)	1	1.95	3
SPC (plasma=0 Hrs)	1.3	1.93	2.98
SPC (plasma=1 Hrs)	1.3	1.89	0.41
SPC (plasma=2 Hrs)	1.3	1.51	0.27
ELA	1.55	0.69	-0.24

As-Deposited and SPC sample are W/L=10μm /10μm

ELA sample is 30μm /31.5μm

TABLE III

The calculated trap density by different channel thickness assumption

	$1/E_B \sim (V_G-V_T)^2$	$1/E_B \sim (V_G-V_T)^{\gamma}$
As-Deposited (plasma=0 Hrs)	$N_T=1.46\times10^{13}$ cm^{-2}	$\gamma=1$ $N_T=2.33\times10^{12}$ cm^{-2}
As-Deposited (plasma=2 Hrs)	$N_T=1.11\times10^{13}$ cm^{-2}	$\gamma=1$ $N_T=1.95\times10^{12}$ cm^{-2}
SPC (plasma=0 Hrs)	$N_T=5.80\times10^{12}$ cm^{-2}	$\gamma=1.3$ $N_T=1.93\times10^{12}$ cm^{-2}
SPC (plasma=1 Hrs)	$N_T=6.37\times10^{12}$ cm^{-2}	$\gamma=1.3$ $N_T=1.89\times10^{12}$ cm^{-2}
SPC (plasma=2 Hrs)	$N_T=5.09\times10^{12}$ cm^{-2}	$\gamma=1.3$ $N_T=1.51\times10^{12}$ cm^{-2}
ELA	$N_T=1.16\times10^{12}$ cm^{-2}	$\gamma=1.55$ $N_T=6.00\times10^{11}$ cm^{-2}

As-Deposited and SPC sample are $W/L=10\mu m/10\mu m$

ELA sample is $30\mu m/31.5\mu m$

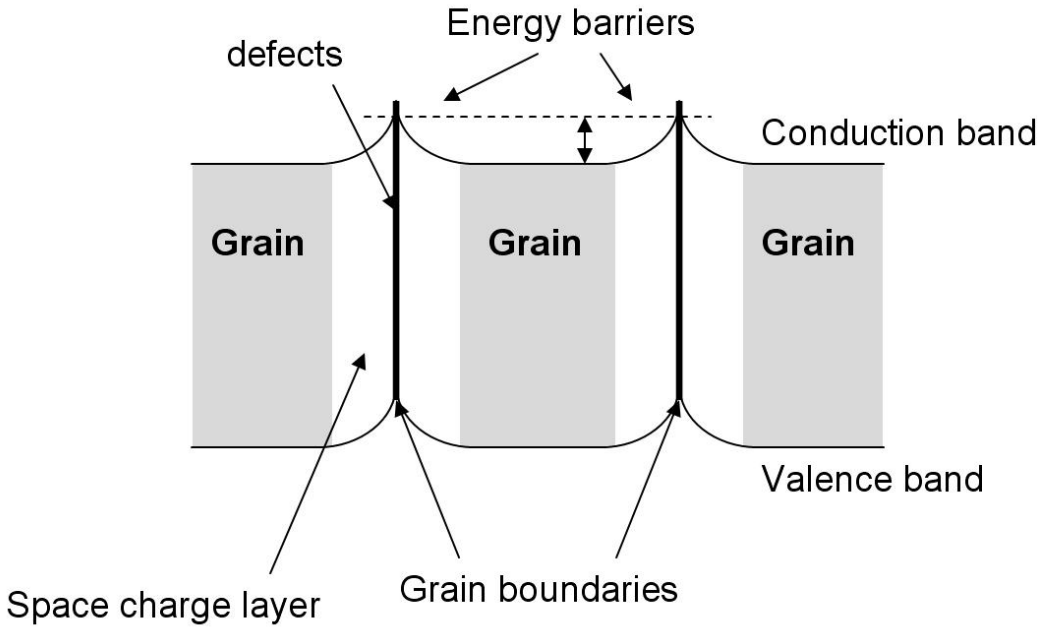


Fig. 1-3-1 One-dimensional energy band diagram in polycrystalline material. The grain size is assumed to be constant. At grain boundaries, defects are electrically active.

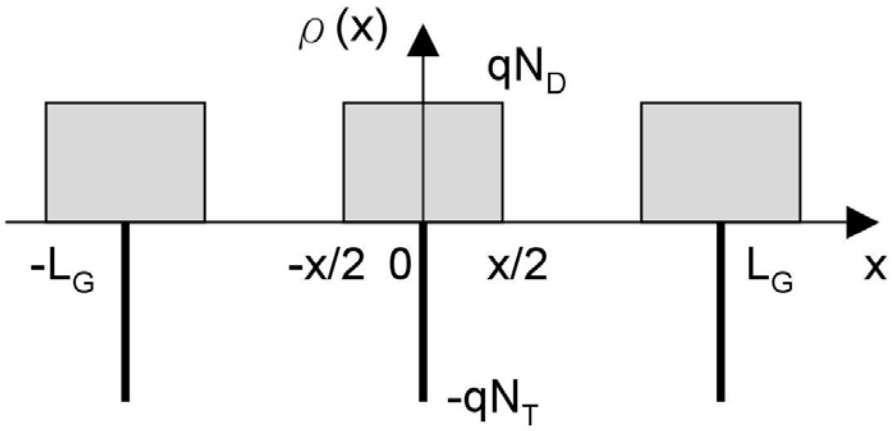


Fig. 1-3-2 Simplified distribution of charges within the grain and at grain boundaries. At grain boundaries, the trap state density is defined per surface unit, while N_D is a doping volume concentration.

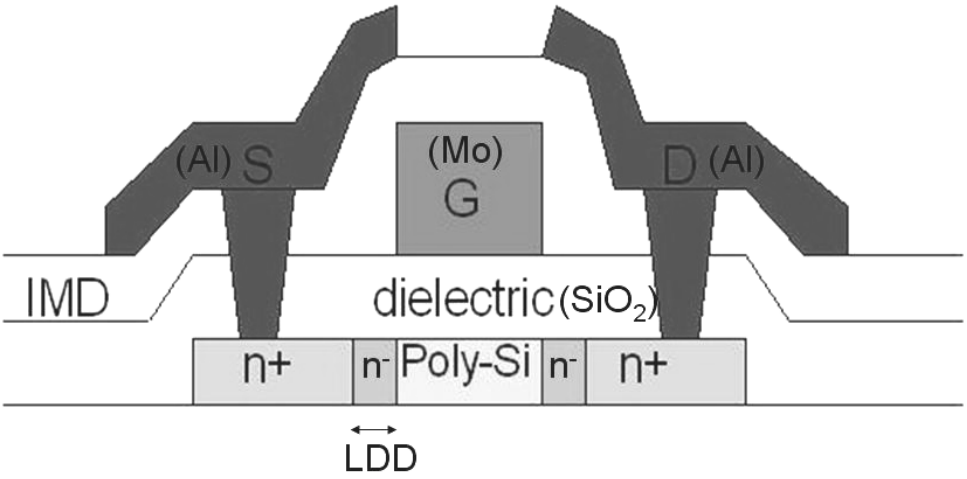


Fig. 2-1-1 Schematic cross sectional view of poly-Si TFT.

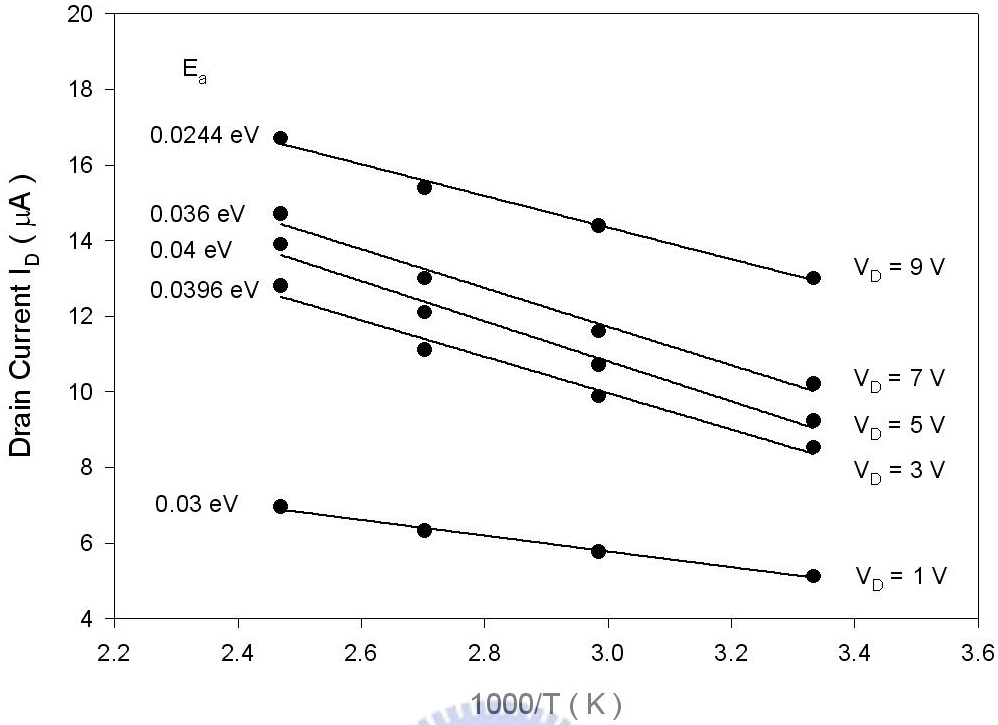
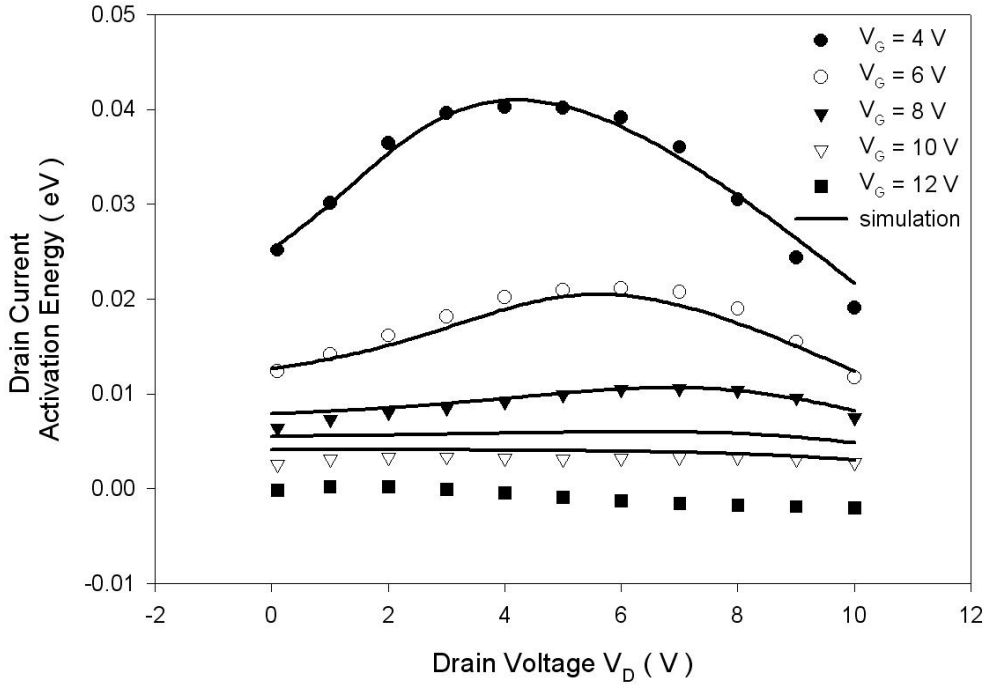
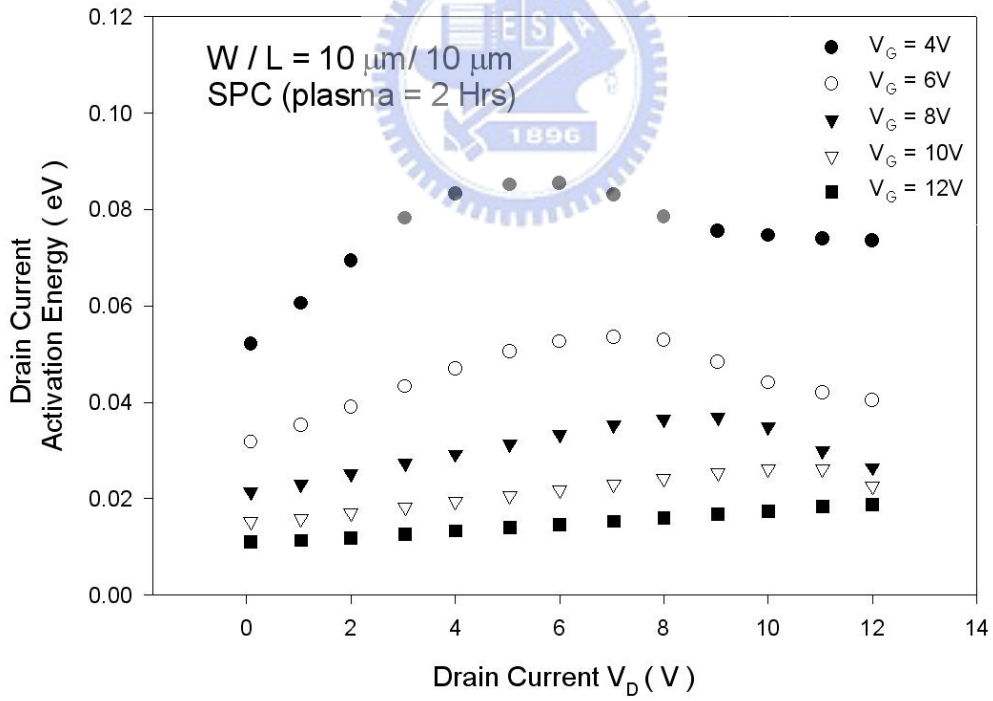


Fig. 2-2-1 Arrhenius plot of the drain current of W/L = 6μm /13.5μm n-channel device for different drain voltages and V_{GS} = 4 V. The slope of each line defines the activation energy (*Ea*).



(a)



(b)

Fig. 2-2-2 The relationship of activation energy versus drain voltage for different gate voltages. (a)ELA sample. The solid lines represent the simulated result and the symbols represent the experimental data ($W/L = 6\mu m$ /13.5μm). (b)SPC sample.

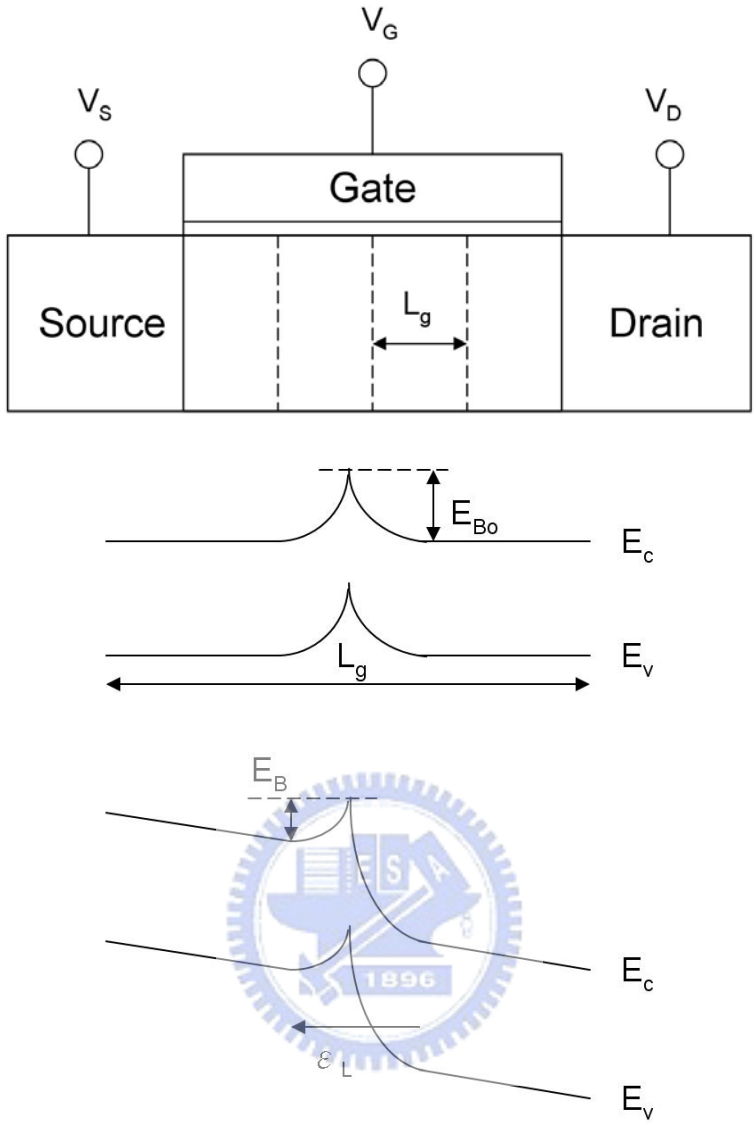


Fig. 2-2-3 Cross-sectional view of a poly-Si TFT and the potential distribution around the grain boundary.

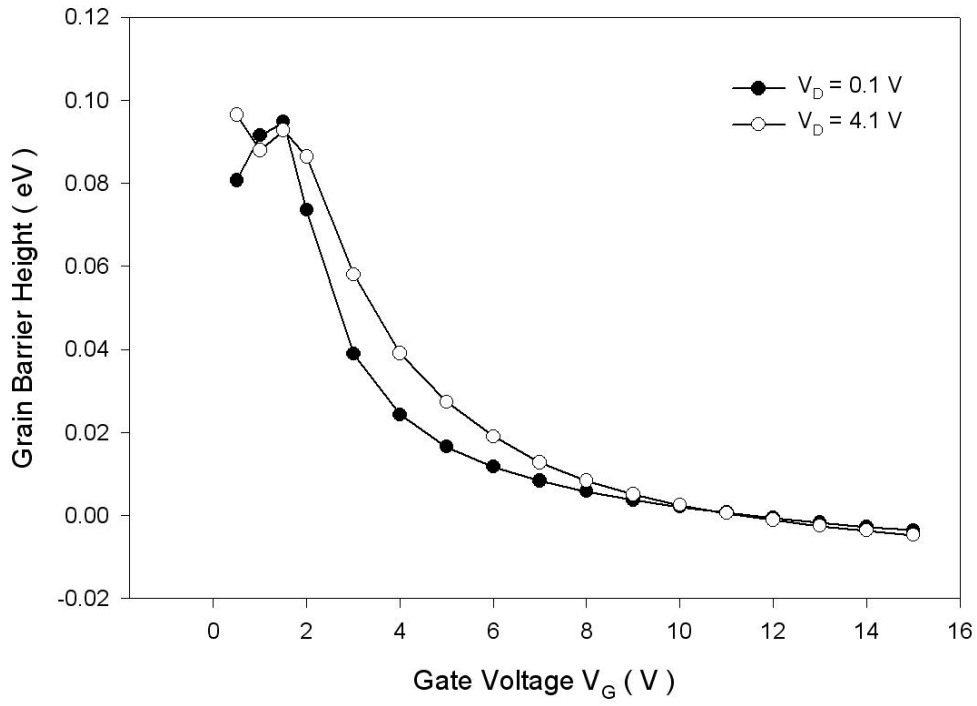


Fig. 2-2-4 The relationship of grain barrier height versus gate voltage for different drain voltages ($W/L = 6\mu m$ /13.5μm).

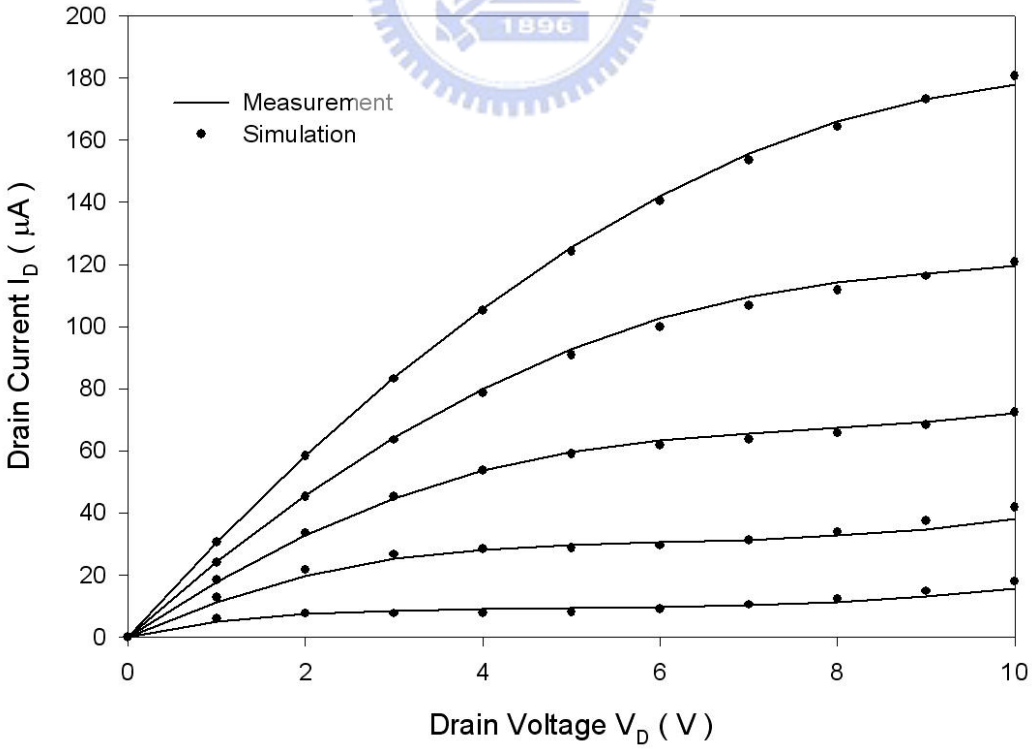


Fig. 2-2-5 Comparison of the output characteristics between simulation (dotted line) and the experiment (solid line) for TFTs ($W/L = 6\mu m$ /13.5μm).

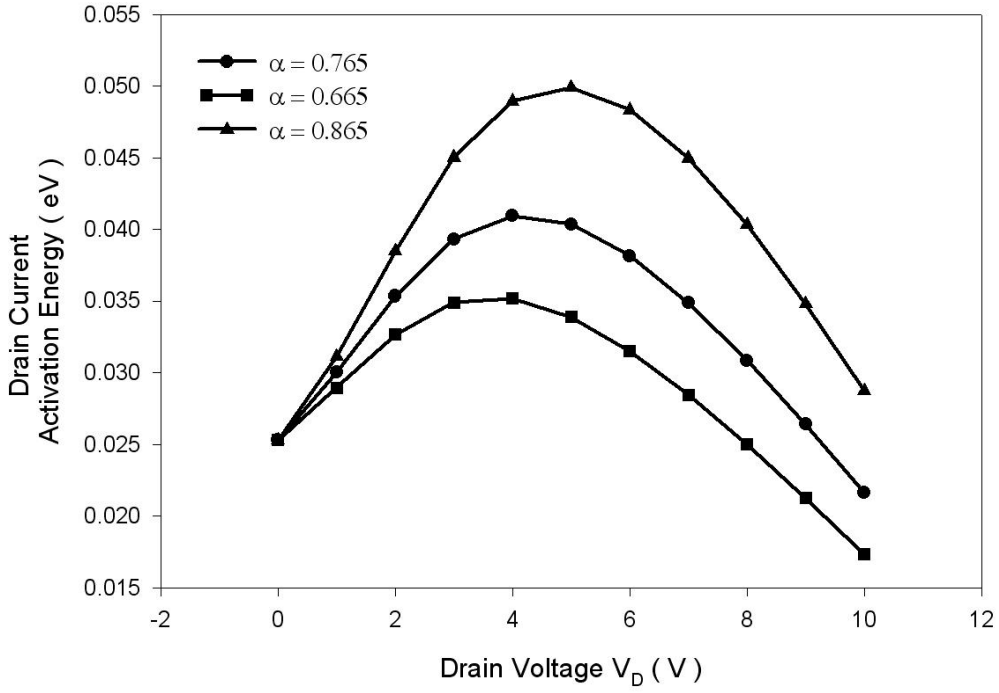


Fig. 2-4-1 Comparison of calculated output characteristics with different α values ($W/L = 6\mu m$ / $13.5\mu m$, $\eta = 2.49$).

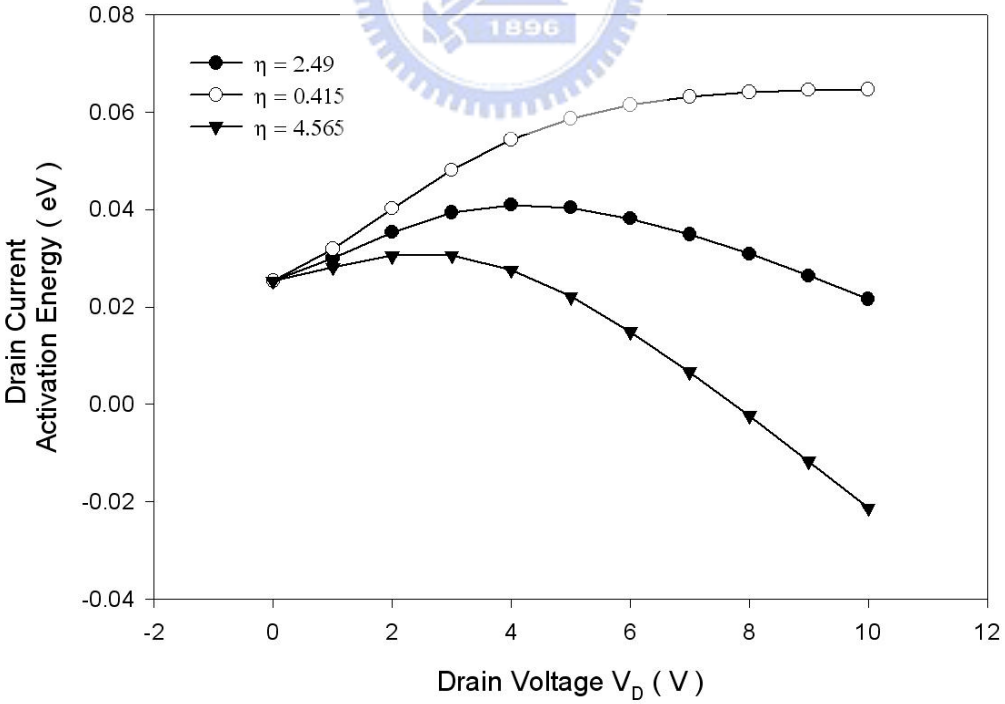
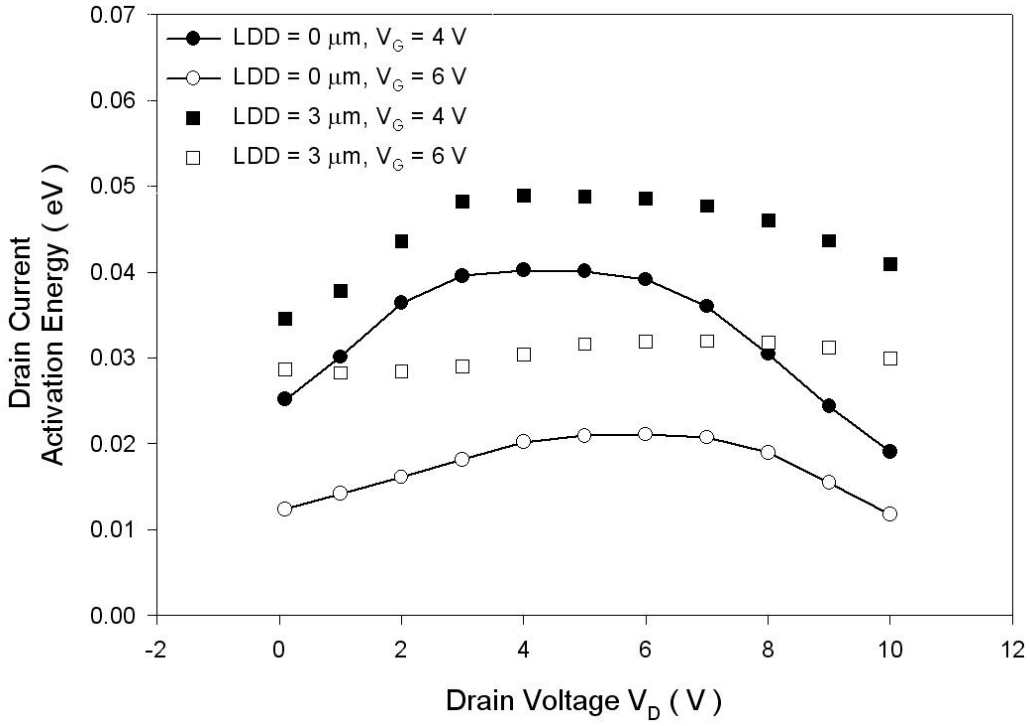
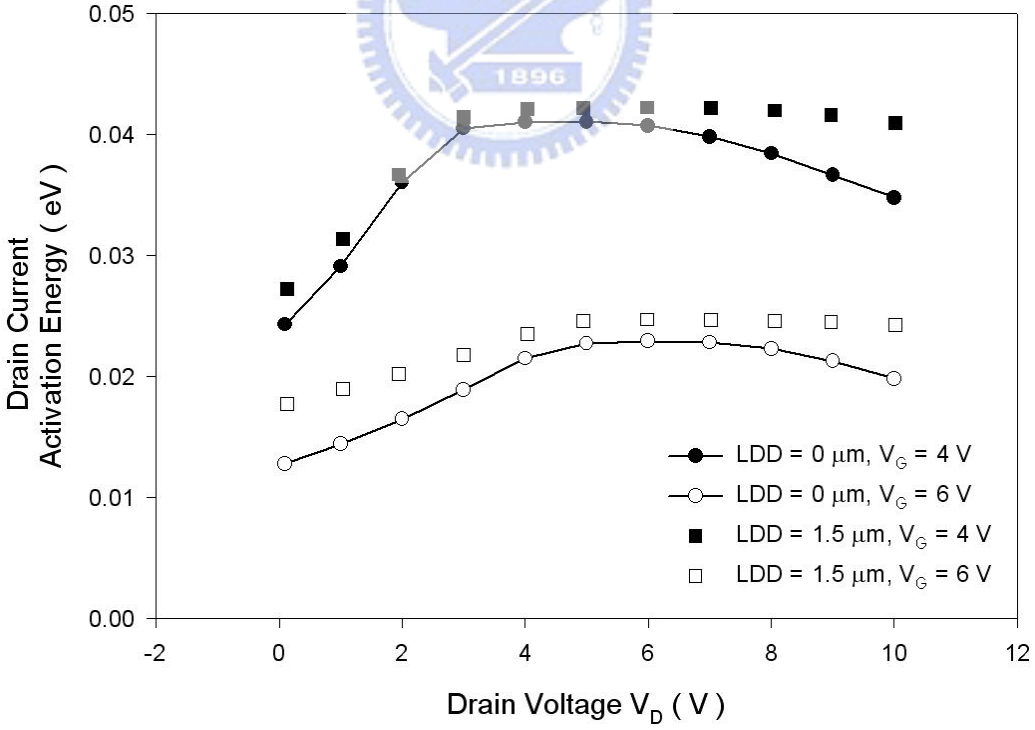


Fig. 2-4-2 Comparison of calculated output characteristics with different η values ($W/L = 6\mu m$ / $13.5\mu m$, $\alpha = 0.765$).

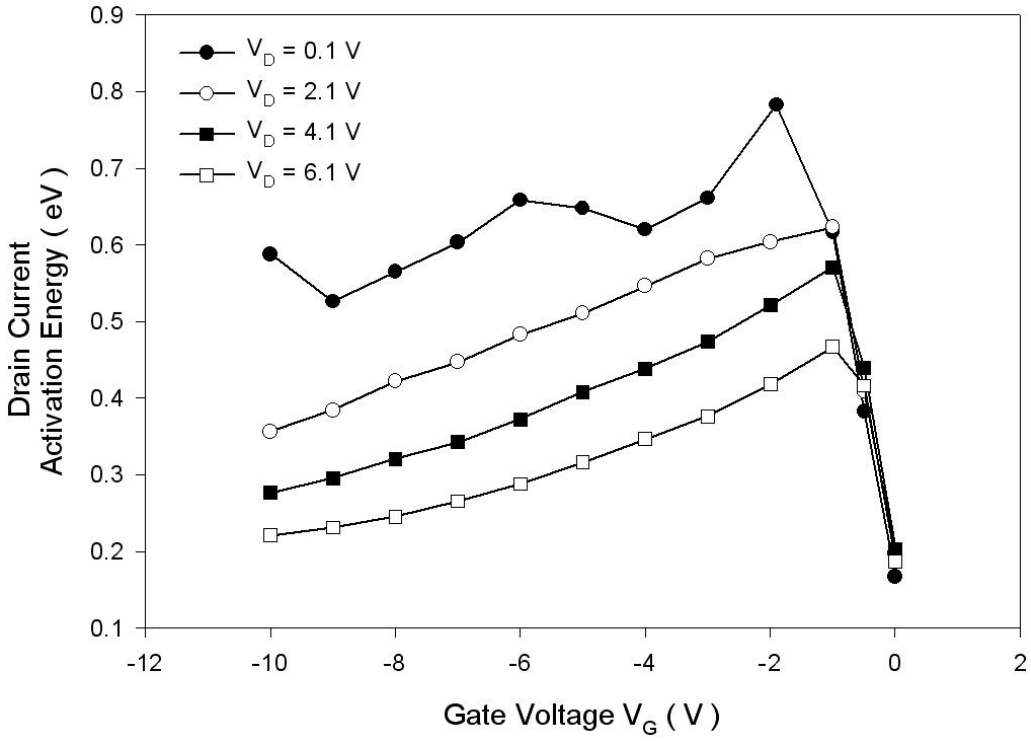


(a)

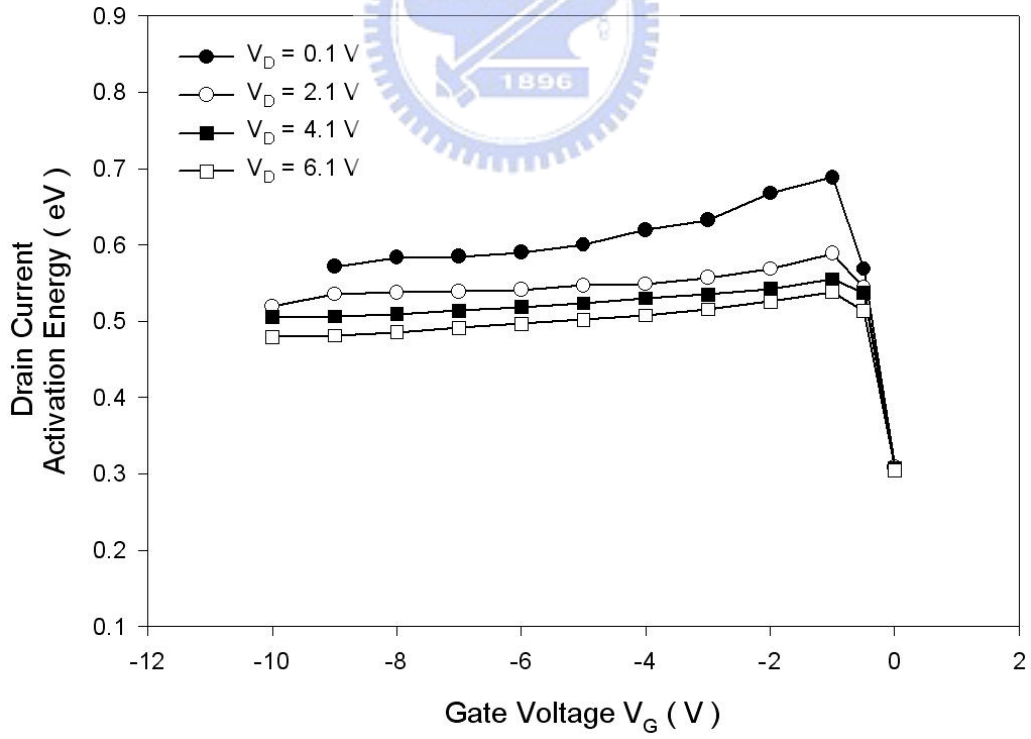


(b)

Fig. 2-5-1 The relationship of activation energy versus drain voltage for different LDD length. (a)$W/L = 6\mu m$ /13.5μm(b) $W/L = 30\mu m$ /31.5μm.



(a)



(b)

Fig. 2-6-1 Dependence of activation energy on gate and drain voltages for (a) conventional device and (b) devices with LDD = 1.5μm (W/L = 30μm /31.5μm).

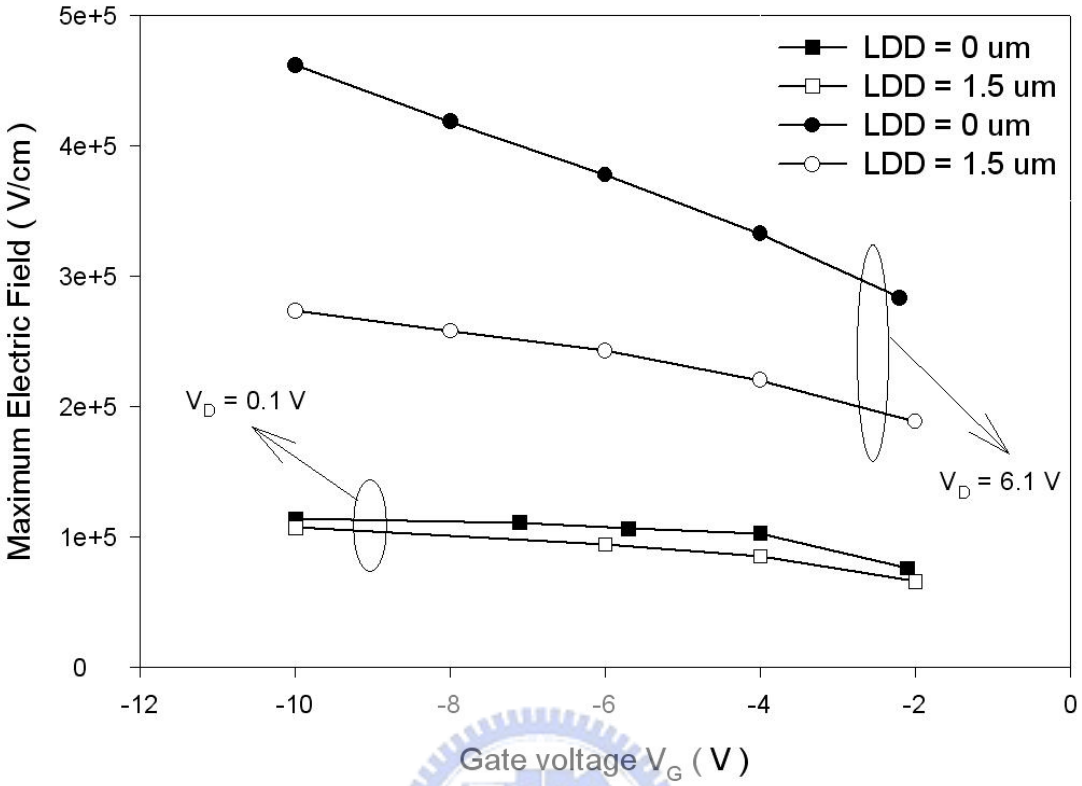


Fig. 2-6-2 The simulated maximum electric field versus the gate voltages. Simulated depth is 10 *nm* from oxide interface (L = 31.5 μm).

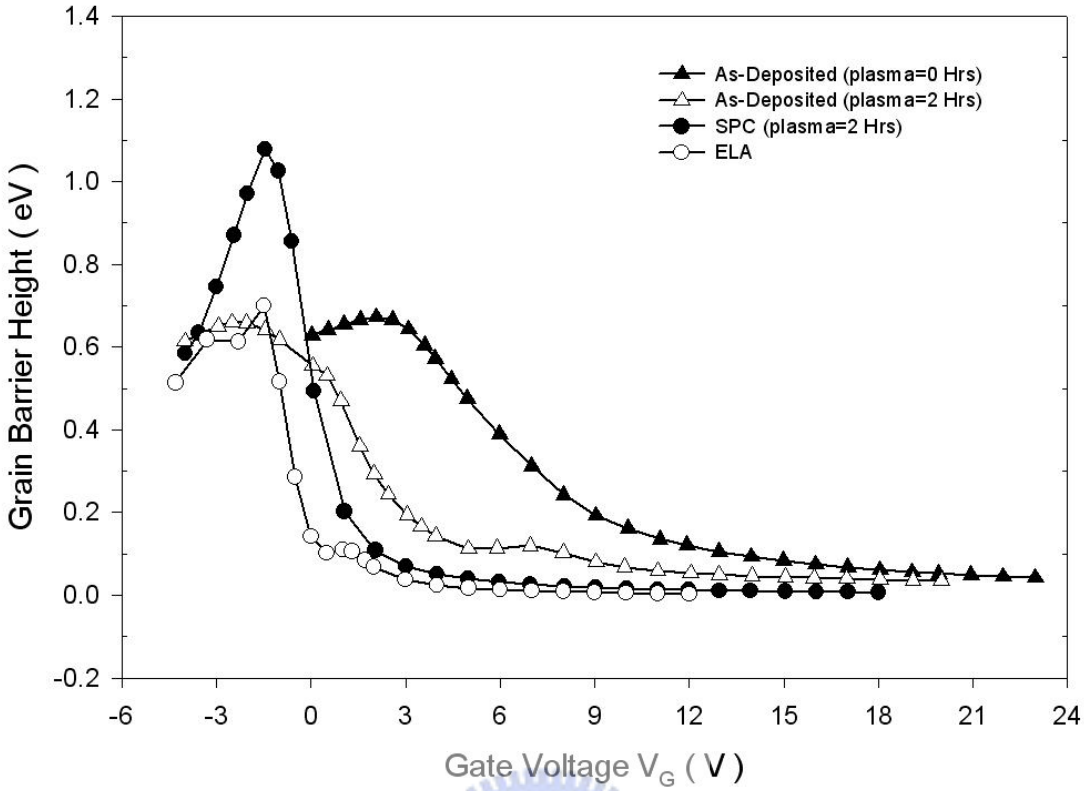
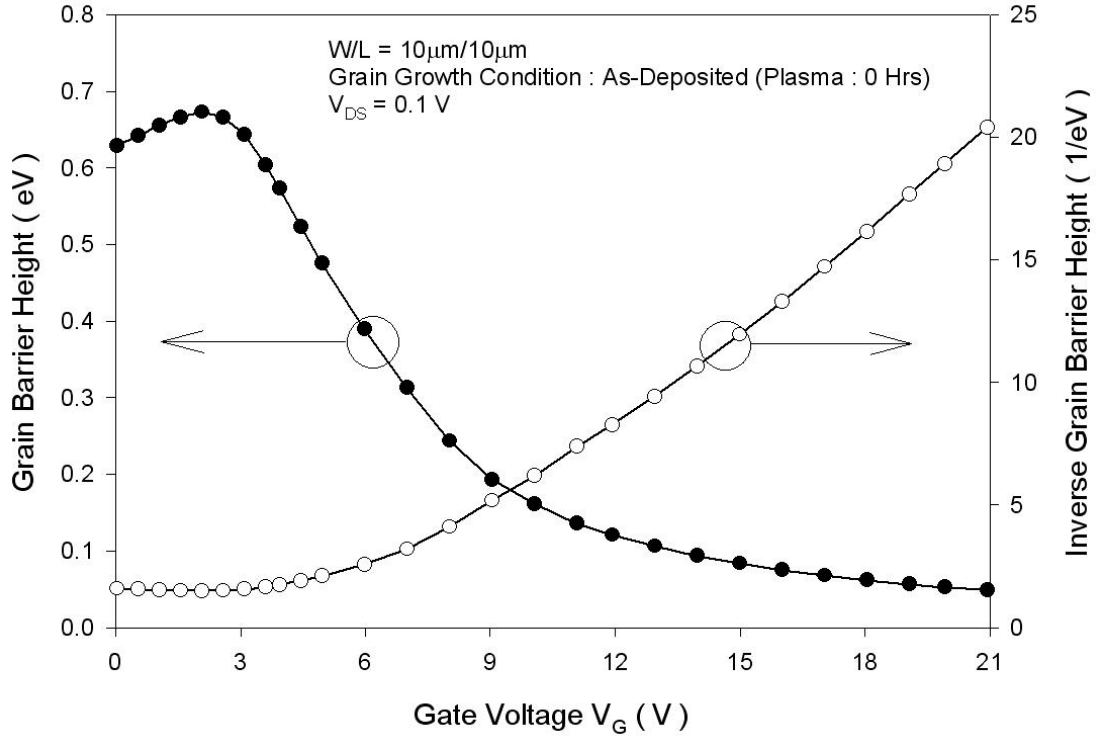
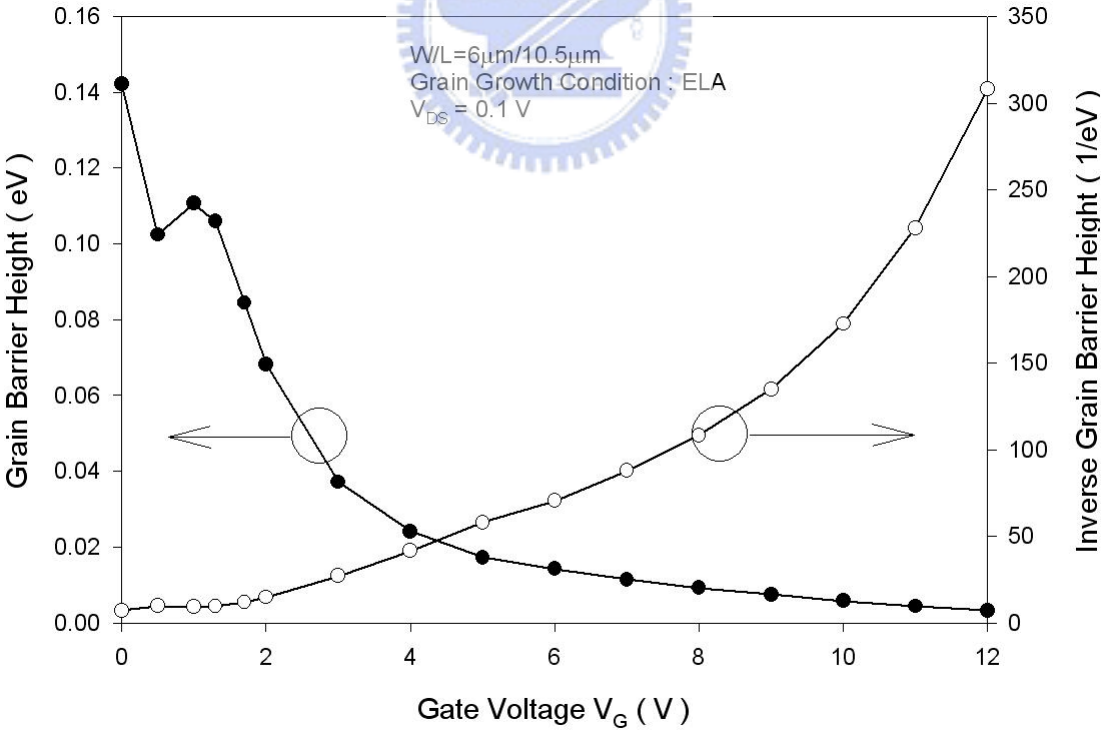


Fig. 3-1-1 The experimental grain barrier height versus the gate voltage for different grain growth conditions. (ELA sample: $W/L = 6\mu m/10.5\mu m$, ; As-Deposited and SPC sample : $W/L = 10\mu m/10\mu m$)

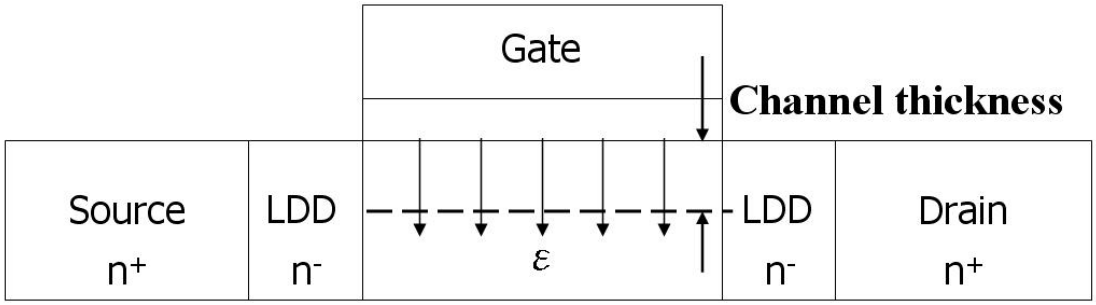


(a)

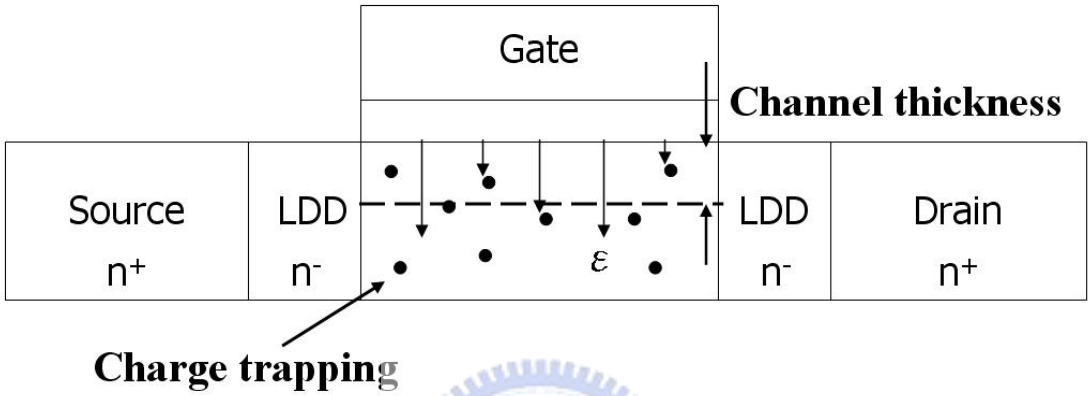


(b)

Fig. 3-1-2 The curves showing comparisons of the grain-barrier height and its inverse versus the gate voltage. (a) grain growth conditions: as-deposited, plasma = 0 *Hrs* (b) grain growth conditions: excimer laser crystallize.



(a)



(b)

Fig. 3-1-3 Illustration of the trapped charge screening effect. (a) no defect device (b) many defects device.

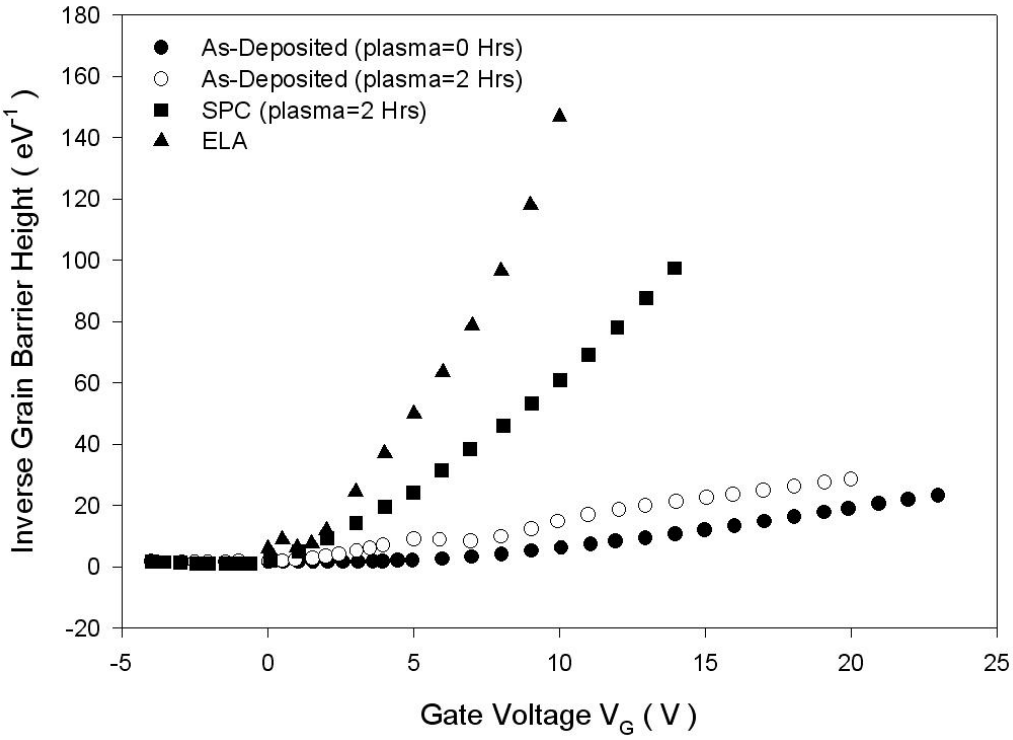


Fig. 3-1-4 The experimental inverse of grain barrier height versus the gate voltage for different grain growth conditions. (ELA sample: W/L = 30μm/31.5μm, ; As-Deposited and SPC sample : W/L = 10μm/10μm)

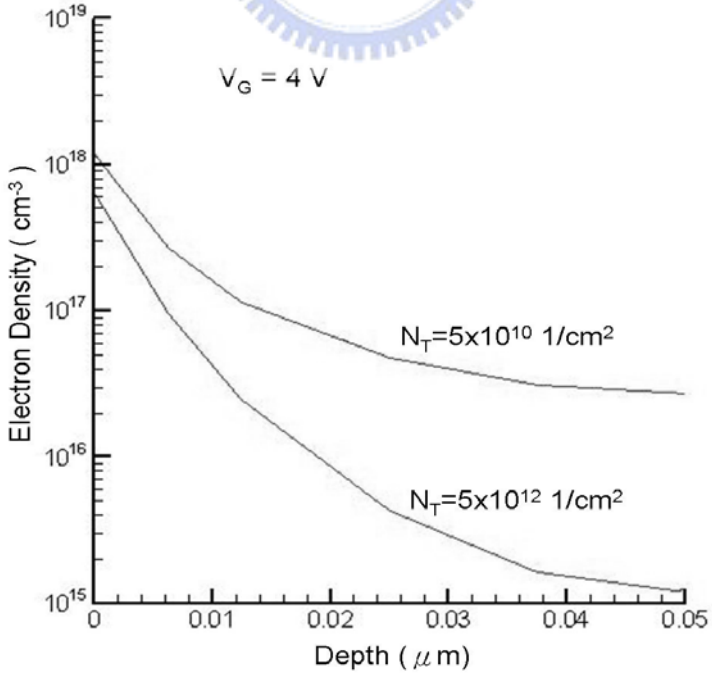
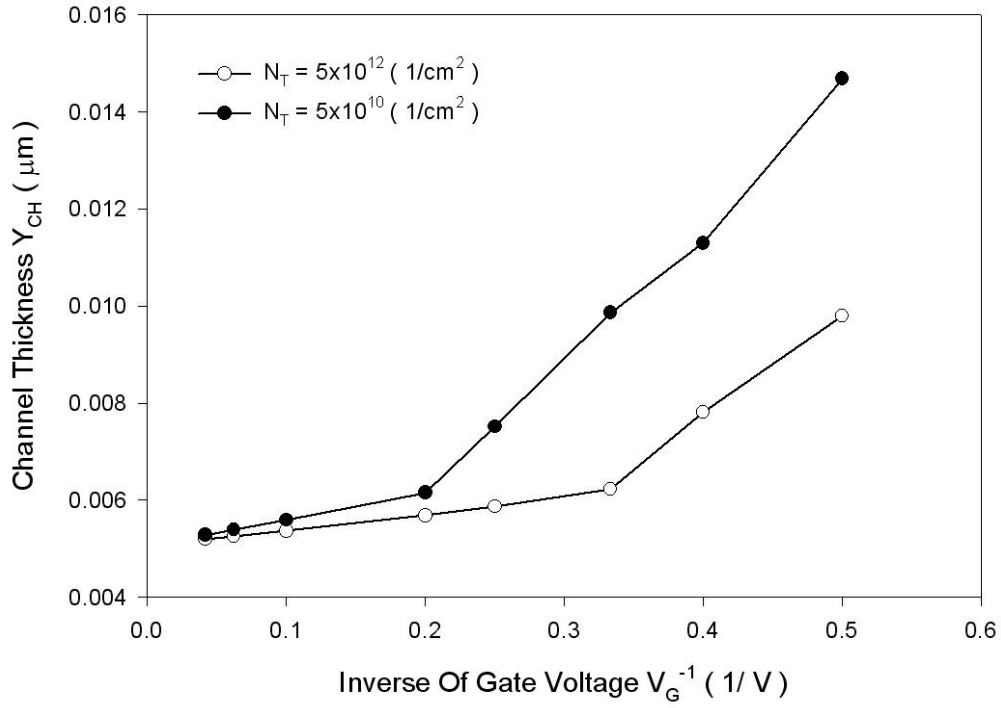
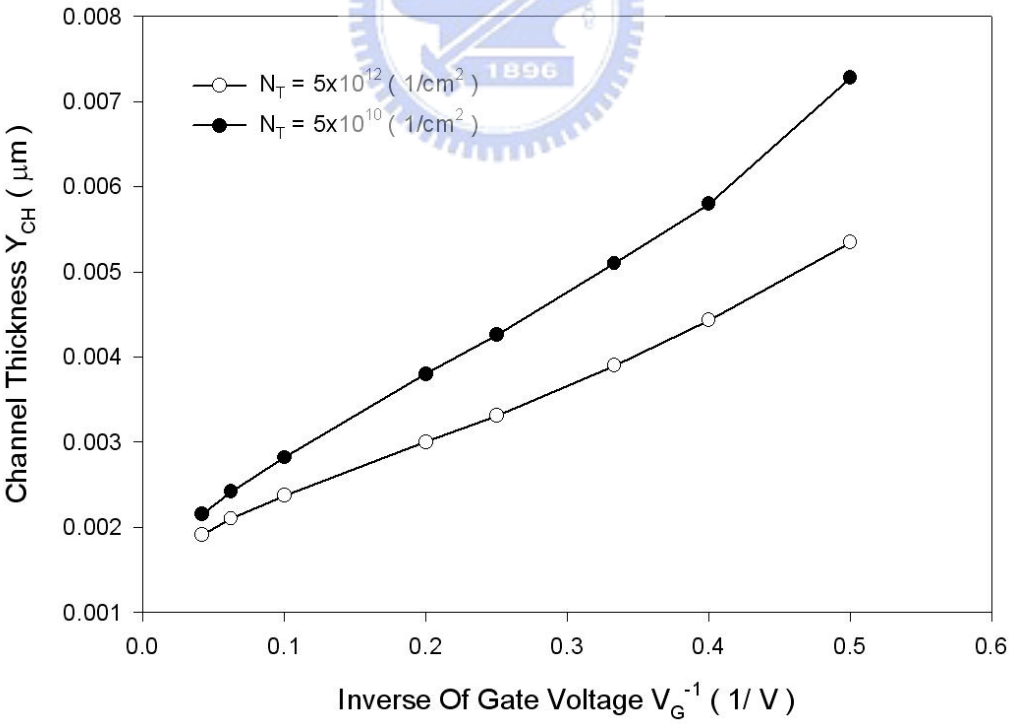


Fig. 3-1-5 The simulated electron density versus the depth which is the distance comes from gate oxide interface.



(a)



(b)

Fig. 3-1-6 The channel thickness (extracted from simulated results) versus the inverse of gate voltage (L=30 μm).

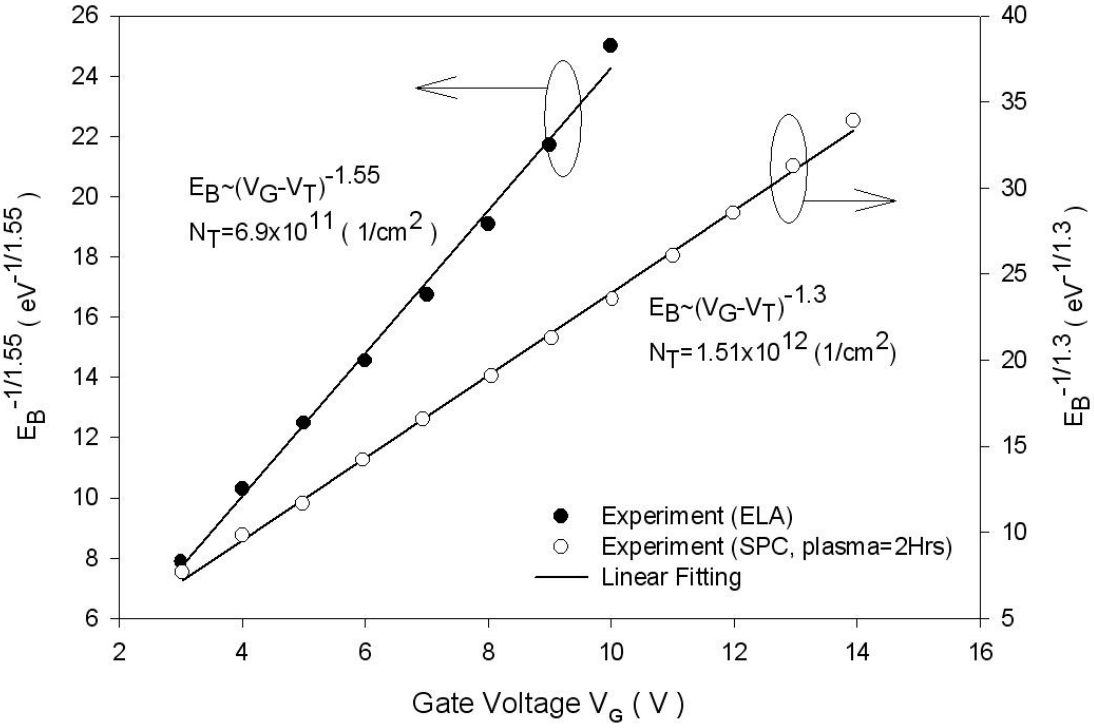


Fig. 3-2-1 N_T was extracted from curve in the plot of $E_B^{-1/\gamma}$ vs. V_G

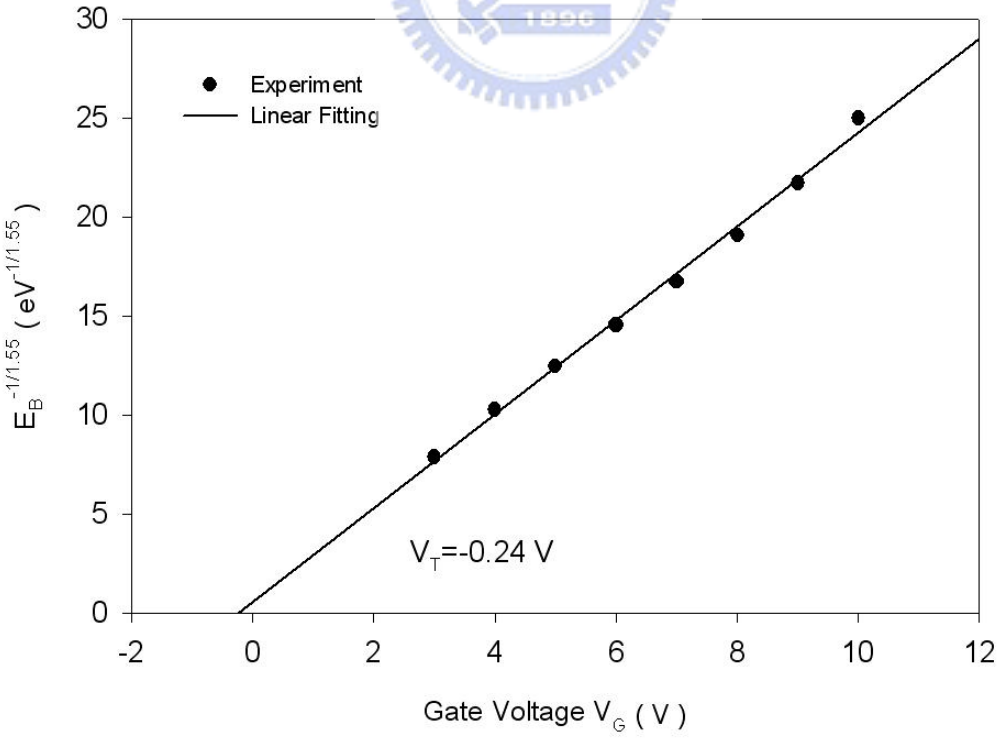


Fig. 3-2-2 V_T was extracted from x-axis intersection in the plot of $E_B^{-1/\gamma}$ vs. V_G (V_D = 0.1V)

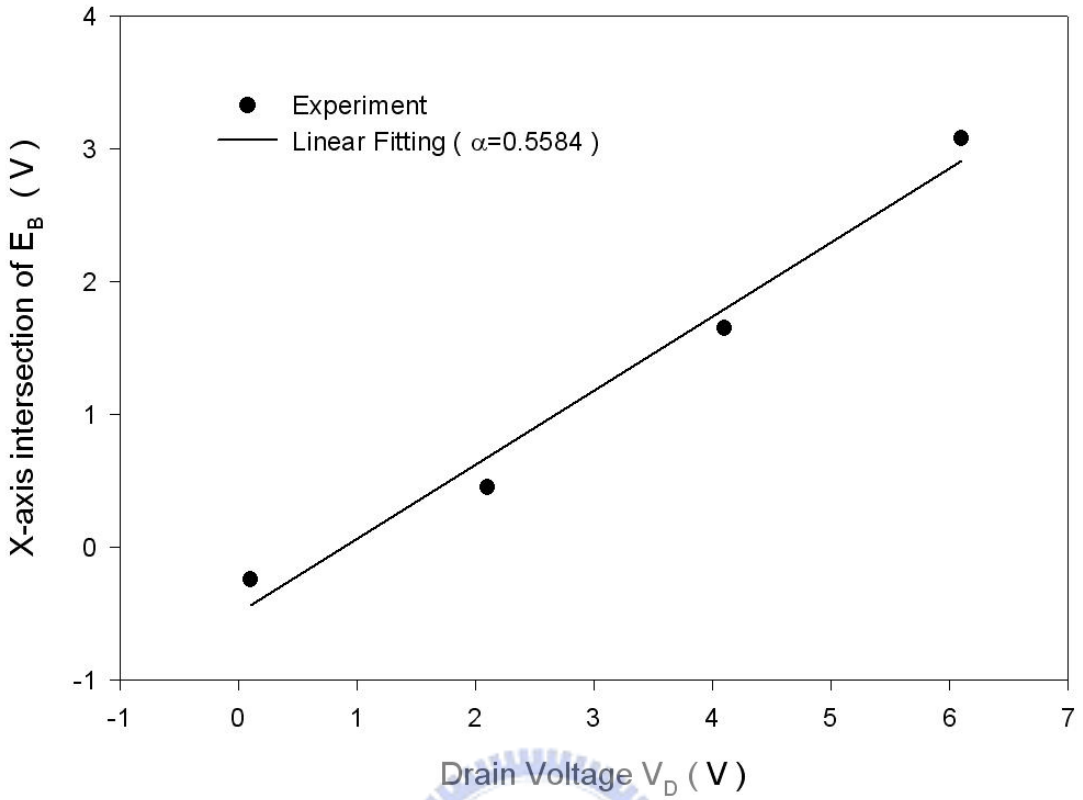


Fig. 3-2-3 α was extracted from the intersection of $E_B^{-1/\gamma}$ vs. V_G at different drain voltage conditions. (W/L = 30μm/31.5μm, ELA sample)

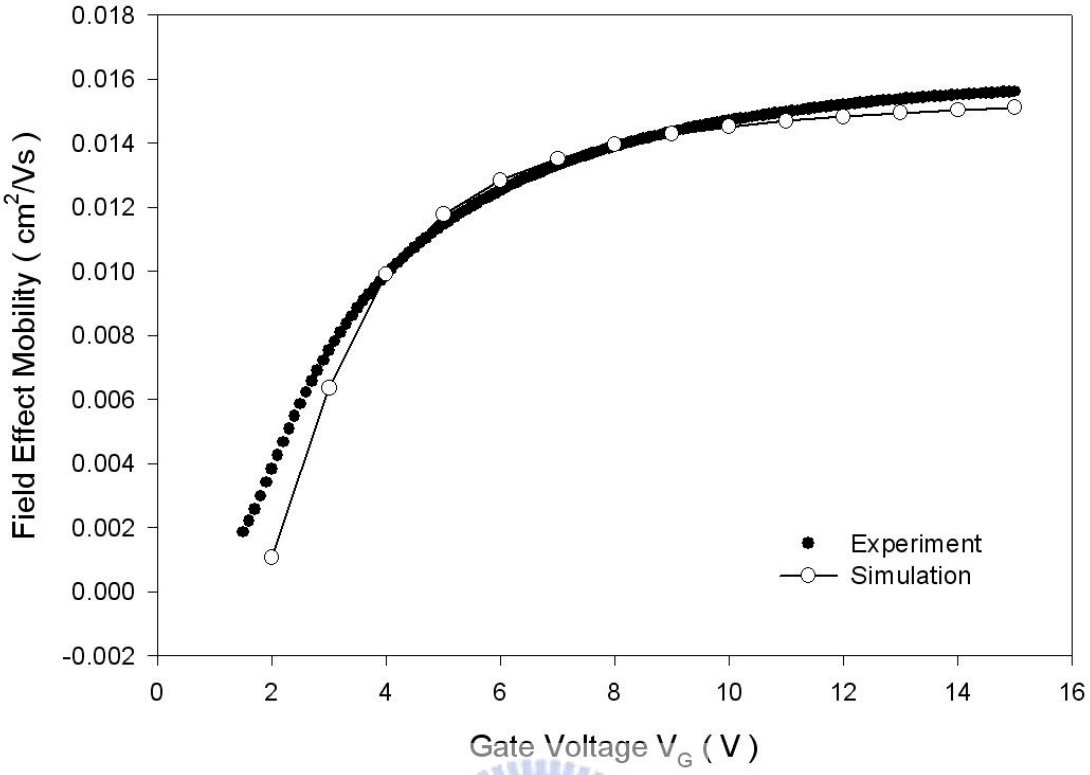


Fig. 3-3-1 Comparison of the simulation results with experiment data. Data is from a 30 μm/31.5 μm n-channel TFT with $V_D = 0.1\ V$. ($\mu_o = 400\ cm^2/Vs$, $\mu_G = 260\ cm^2/Vs$)

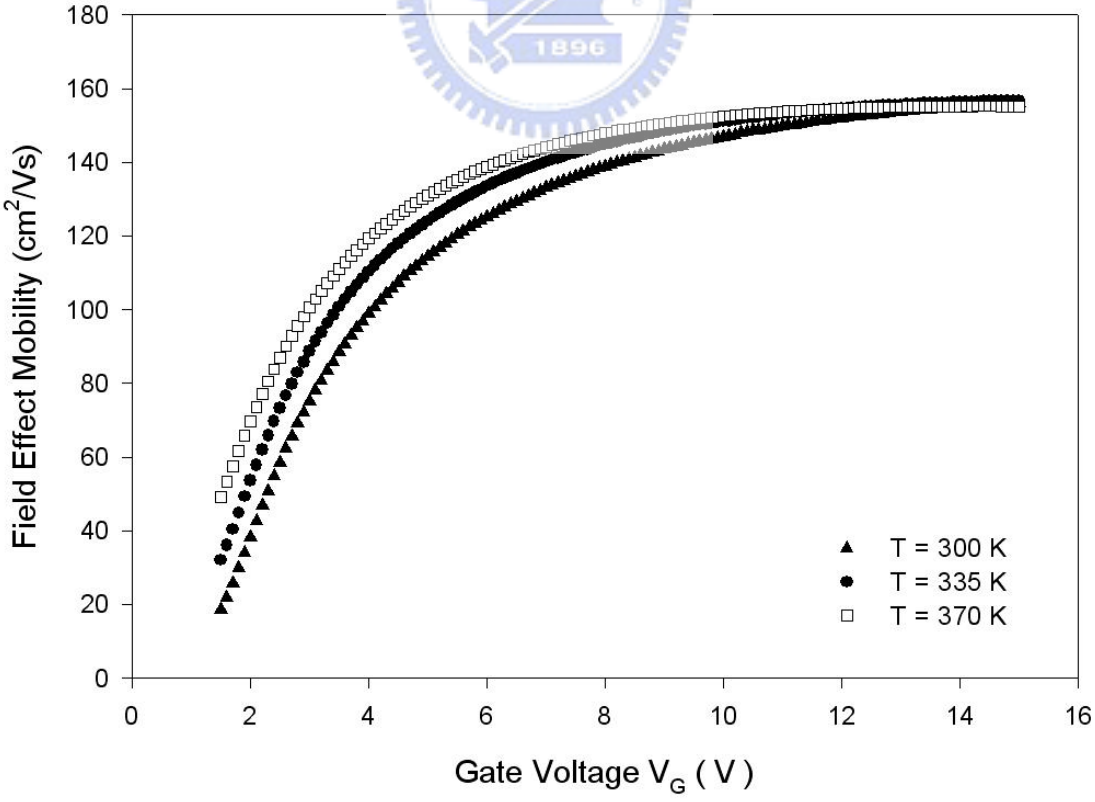


Fig. 3-3-2 The field effect mobility versus gate voltage at different measurement temperature. Data is from a 30 μm/31.5 μm n-channel TFT with $V_D = 0.1\ V$.

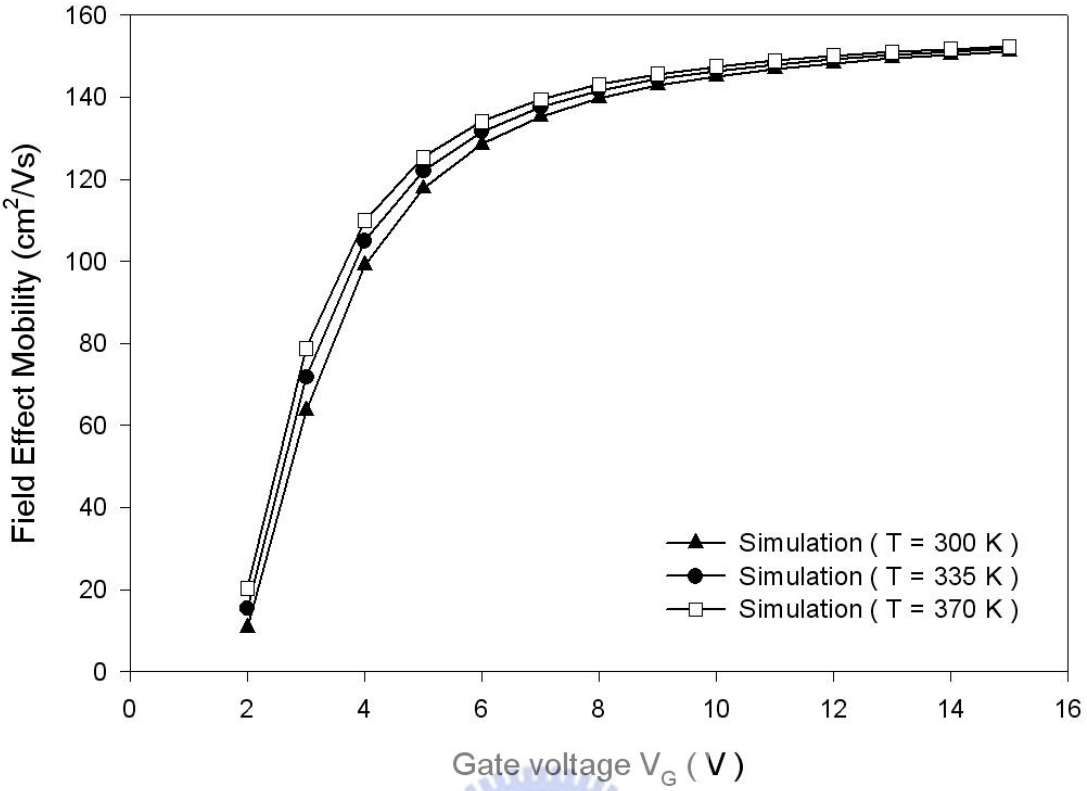
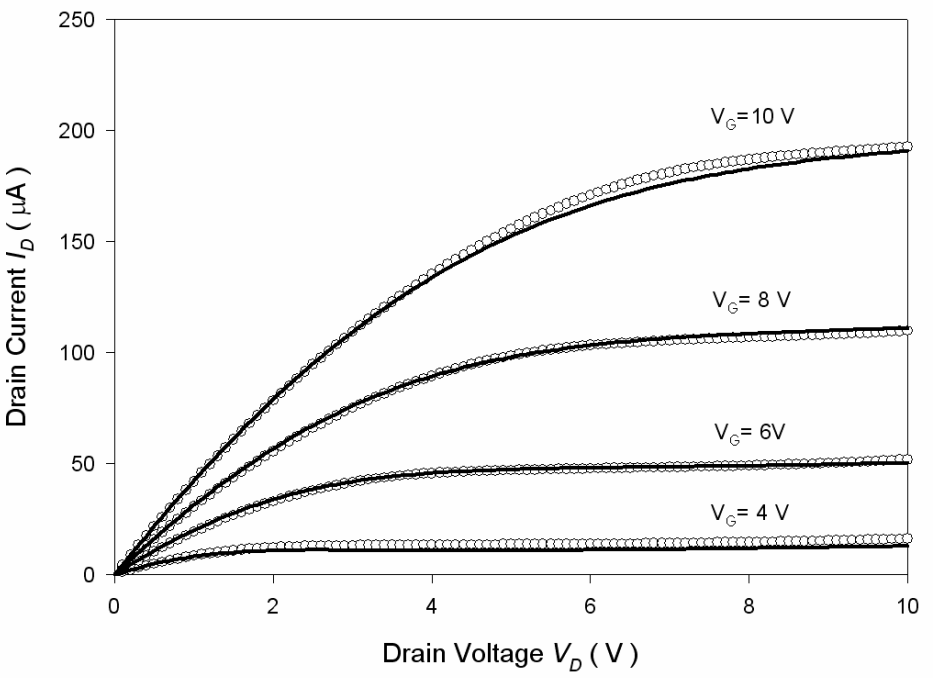
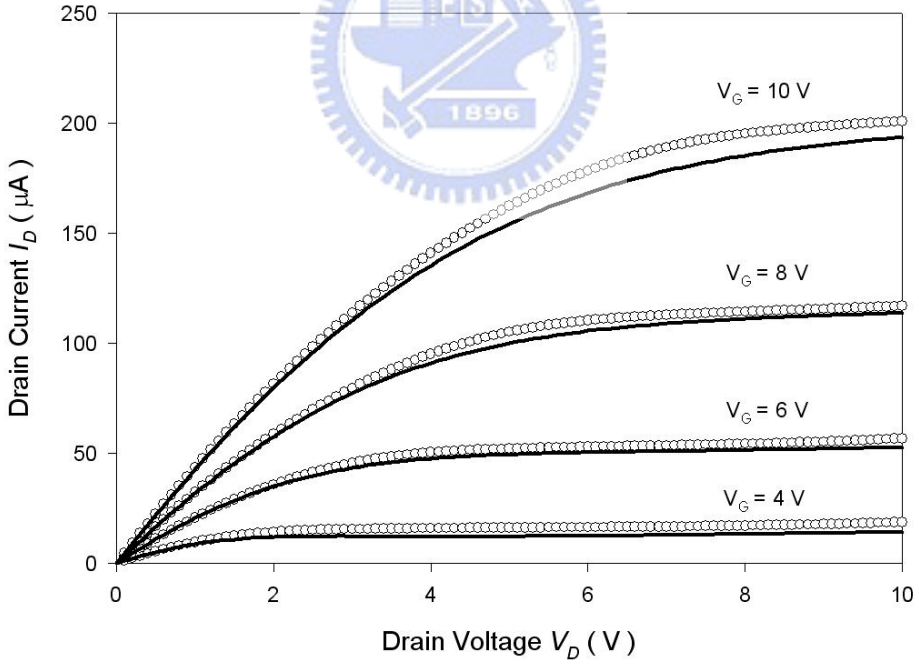


Fig. 3-3-3 The simulation results of the field effect mobility versus gate voltage at different temperature. Simulation is from a 30 μm/31.5 μm n-channel TFT with V_D = 0.1 V. (μ_o = 400 cm^2/Vs, μ_G = 260 cm^2/Vs)

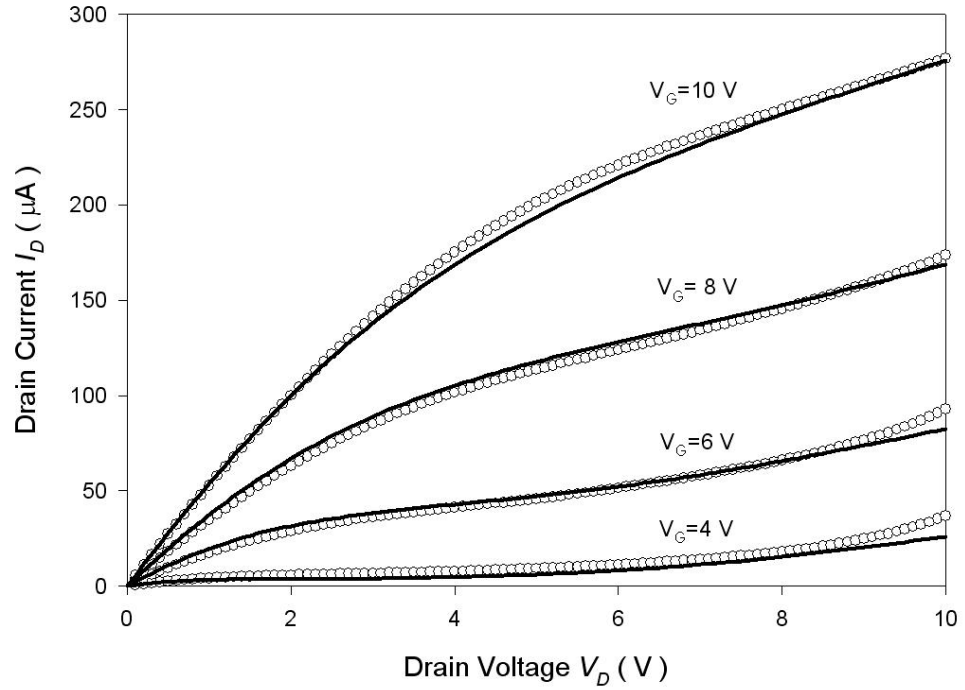


(a)

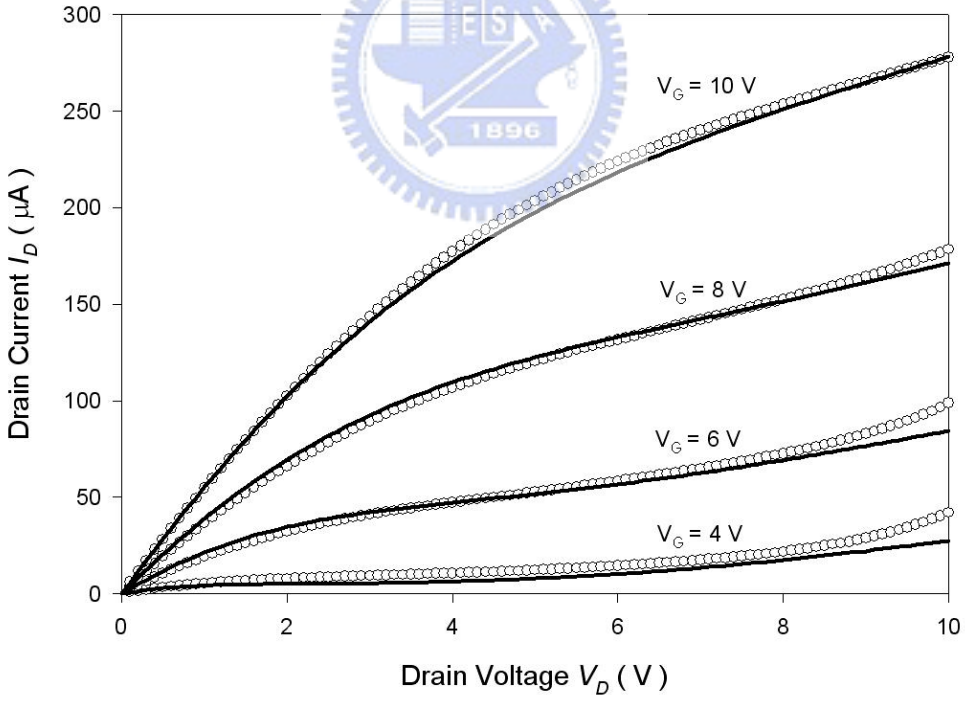


(b)

Fig. 3-4-1 The comparison of experimental (symbols) and simulated (solid line) *I-V* output characteristics for W/L = 30μm/31.5μm ELA poly-Si TFTs Conclusion (a) temperature = 25 ℃ (b) temperature = 60 ℃.



(a)



(b)

Fig. 3-4-2 The comparison of experimental (symbols) and simulated (solid line) *I-V* output characteristics for $W/L = 6\mu m/5.5\mu m$ ELA poly-Si TFTs Conclusion (a) temperature = 25 ℃ (b) temperature = 60 ℃.

簡　歷

姓名 ： 丘兆仟（ Chao-Chian Chiu ）

出生日期 ： 民國七十年五月三日（1981.5.3）

住址 ： 台北縣永和市福和路327號7樓

學歷 ：

國立清華大學 原子科學系 學士

（1999.09-2003.06）

國立交通大學 光電工程研究所 顯示組 碩士班

（2003.09-2005.06）

論文題目 ：

複晶矽薄膜電晶體晶粒邊界位障效應之研究

The Analysis of Grain Boundary Barrier Effect in Poly-Si TFTs