Chapter 1

Introduction

1-1. Development of Displays

In recent years, with the flat-panel display technology development, flat- panel displays have replaced the traditional cathode ray tube (CRT) application for many aspects. Liquid crystal display (LCD) is one of the popular displays. Especially, thin film transistor liquid crystal display (TFT-LCD) is the most common display at present. According to the manufacture technique of thin film transistor (TFT), the TFT-LCD was categorized into amorphous-silicon (a-Si) TFT and low-temperature poly-silicon (LTPS) TFT and high- temperature poly-silicon (HTPS) TFT.

Among these TFTs, LTPS has been widely investigated as a material for mobile applications such as digital cameras and note book computers. In polysilicon film, the carrier mobility larger than 100 cm^2/Vs can be easily achieved, that is about 500 times larger than that of the conventional amorphous-silicon TFTs and fast enough to make peripheral driving circuit including n- and p-channel devices. This enables the monotheistic fabrication of peripheral circuit and TFT array on the same glass substrate, bringing the era of system-on-glass (SOG) technology [1]. There are considerable interests in poly-Si thin film transistors (TFTs) because of their wide application in active matrix liquid crystal displays (AMLCDs) [2]. They also have been applied into some memory devices such as dynamic random access memories (DRAMs) [3], static random access memories (SRAMs) [4], electrical programming read only memories (EPROMs) [5], electrical erasable programming read only memories (RRPROMs) [6], linear image sensors [7], thermal printer heads [8],

photo-detector amplifier [9], scanner, neutral networks [10] and three dimension LSIs [11].

In the future, the application fields of LTPS TFTs will not be limited to displays but will be expanded to other electronic devices, such as LSIs [11], printers and sensors. Among these, the application of poly-Si TFTs in AMLCDs is most noticeable and brings about rapid process in poly-Si TFT technology.

Therefore, it is possible to integrate poly-Si TFTs and surrounding driving circuit on the same substrate. This will reduce the assembly complication and the cost dramatically. In addition, since the mobility of poly-Si is higher, the dimension of poly-Si TFTs can be made smaller than that of amorphous silicon ones. This is beneficial to fabricate high density and high resolution AMLCDs.

1-2. LTPS TFTs

Low temperature poly-Si (LTPS) TFT technology appears to be one of the most promising technologies for the ultimate goal of building fully-integrated AMLCD system on glass. The LTPS TFT LCDs achieve high resolution, high luminance displays as well as "System on glass" displays, which allow us to integrate various functional circuits on to the display panels. The so-called system on glass (SOG) TFT-LCD with LTPS technology enables to spare the silicon driver ICs and to enhance the productivity by reducing the module process steps. System-on-panel (SOP) has the merits of high brightness, low power consumption, thin thickness, light weight, fast response, high integration, high reliability, and good image quality. Comparing with the conventional a-Si TFT LCD with silicon ICs on it, the SOG-LCD requires high-performance TFTs such as high carrier mobility (μ), low threshold voltage (V_T), and small sub-threshold swing to meet the high speed driving circuits

that result in good display quality and a small form factor. The LTPS TFT has also the possibility for realizing far more value-added circuit monolithically with the pixels on the array glass. Therefore, the research efforts also have been focused on realization of system integration for LTPS TFT LCDs and have been developed various types of circuit-integrated LCDs so far.

1-3. Integrated Circuits of System on Panel

Fig.1 shows the system block diagram of this panel. As shown in Fig.1, this panel consists of the following seven circuits: the interface circuit to change input logic level to higher level needed for TFT circuitry, the timing generator to generate control pulses for drivers, the reference driver to generate 64-step voltage, the VCOM driver to generate common voltage, the source driver to supply analog voltage to source lines according to input digital signals, the gate driver to select gate lines, and the DC-DC converter to supply negative voltage of gate drivers. The signal processing in the module works with following flows. Data signals are supplied to a driver IC from an external circuit by way of one of the following interfaces (I/Fs) including parallel CPU I/F or serial CPU I/F or RGB I/F. Then the signals are stored to frame memories. Data signals in the frame memories are read out at a constant frequency, and then transferred to D/A converters, which output data to an LCD panel. Output signals include serially composed RGB signals.

The most fundamental display driver circuit (for both active- and passive-matrix displays) is the shift register. Assuming the simplest driving scheme, the rows and the columns of the display matrix are activated one by one, which is accomplished by the active shift register output (which can be high or low level signal) being shifted to the next bit, and eventually cycled to the register's input (Hsync or Vsync) again.

When the characteristics of the LTPS TFT are improved by the evolution of the

design rule and processing, the high-speed operation of the circuit becomes possible. It means that shift registers can be operated easily more than MHz.

1-4. Motivation

The method of predicting the yield and power dissipation of digital circuits in VLSI has been extensively studied. In the traditional IC design, Worst Case analysis is the most commonly used technique for considering manufacturing process tolerances on the design of digital integrated circuits. In other words, as soon as we realize the worst component characteristic of transistors, the voltage and operation frequency correspondence of the shift register can be quickly calculated. The frequency decides the resolution of products in the application of system on panel. If one can reduce the voltage, the power can be reduced by a wide margin. However, conventional predictions do not consider the problem of device variation caused by the device characteristics of LTPS TFTs. By the same token, the range of regular voltage corresponding in the maximum frequency, or regular frequency corresponding in minimum voltage may widely distribute over whole circuit design.

Generally speaking, the Monte Carlo method used to simulate device variations is quite straightforward. It is also reliable and accurate for all methods used in practice, but for high accuracy, it costs a large computational time. Based on the above, how to develop a front-end simulation skill which quickly and accurately estimates the yield during design phase is became a key point of product competitiveness.

To overcome the above problems, we firstly describe the relation between delay time and operation frequency. Moreover, we drive the formula for delay time based on polysilicon TFT RPI model. In chapter 3, we analyze the effects of device

variations in LTPS TFTs digital circuit. The simulation results demonstrate that Vth

variation is the most impact factor comparing to the other parameters in LTPS TFTs.

A quick simulation skill to save Monte Carlo time will be describe in chapter 4.

It is founded that the operation frequency of an n-stage shift register can be obtained

through simplifying propagation delay from an n-stage one to an 1-stage one. The

power dissipation of an n-stage shift register is also estimated in the same way. The

trends of operation frequency correspond to resolution will also be discussed in this

chapter. Finally, chapter 5 will give a conclusion on the results obtained.

1-5. Thesis Organization
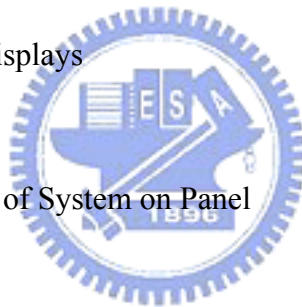
Chapter 2

Simulation and Analysis Methods

2-1. Simulation Methods

There are two major methods of simulation to analyze circuit performance, which are the worst-case and Monte Carlo analysis as described below.

2-1-1. Worst-Case Method [1]

Worst-Case analysis is the most commonly used technique in industry for considering manufacturing process tolerances in the design of integrated circuits. These approaches are relatively inexpensive compared to the yield maximization approaches in terms of computational cost and designer effort, and they also provide high parametric yields. At any design point, uncontrollable fluctuations in the circuit parameters cause circuit performance to device from their nominal design values. The goal of worst case analysis is to determine the worst values that the performance may have under these statistical fluctuation. In addition to finding the worst-case values of the circuit performance, this analysis also finds the corresponding worst-case values of noise parameters. A noise parameter is treated as a random variable. Any random variable is characterized by probability density function (and by a mean and a standard deviation which depends on the density function), as shown in Fig. 2-1-1. The worst-case noise parameter vector is used in circuit simulation to verify whether circuit performances are acceptable under these conditions. Similar to worst-case analysis, one can also perform best-case analysis. In fact, industrial designs are often simulated under best, worst, and nominal noise parameter conditions, which provide designers with quick estimates of range of variation of circuit performances.

2-1-2. Monte Carlo Method

Yield, expressed as a multi-dimensional integral, can be evaluated numerically using either the quadrature-based, or Monte Carlo based methods. The quadrature-based methods have computational costs that explode exponentially with the dimensionality of the statistical space. Monte Carlo methods, on the other hand, are less sensitive to the dimensionality. The Monte Carlo method is a computer simulation of real distributions of random noise parameters, and it is the simplest, most reliable and accurate of all methods used in practice, but for high accuracy it requires a large number of sample points. Typically, hundreds of trials are required to obtain reasonable accurate yield estimation. For nonlinear and/or time domain circuit analysis, this is computational expensive. Hence, a fundamental problem to solve is to increase the efficiency of the Monte Carlo method and its accuracy, measured by the variance of the yield estimation.

2-2. RPI Model

The poly-Si TFT models could be divided into three categories: the models that try to incorporate the physics related to individual grain boundaries[2], the models that use close form analytical expressions for current-voltage characteristics[3,4], and the models based on effective medium. In recent years, several models for poly-Si TFTs have been proposed. Lin et al. obtained an expression for grain barrier height as a function of gate bias and the lateral electric field from a quasi-two-dimensional formulation of Poisson's equation. This solution was incorporated in an expression for the drain current in poly-Si TFTs. Further insight relating the characteristics to the poly-Si material parameters was provided by Fortunato and Magliorato [5]. Other solutions use Poisson's equation with the inclusion of space charge due to traps. Still

others seek formulations with a minimum of empirical approximations. Although useful for the insight they provide, these expressions tend to be too complication for implementation in circuit simulators. The effective medium approach permits the development of comparatively simple models with only a few easily extractable parameters. Although these parameters cannot always be directly related to material properties, such models are attractive for use in SPICE type circuit simulators.

The above models are mainly developed for long-channel poly-Si TFTs although later versions by Jacunski et al. [6,7] have included physics based formulations of important mechanisms such as the kink effect, the field effect mobility in moderate inversion, and the subthreshold current. Finally, the most recent models based on these semi-empirical effective medium approach also include short-channel effects, drain induced barrier lowering (DIBL), velocity saturation, temperature effects, and mobility degradation at high gate bias [6,8-10].
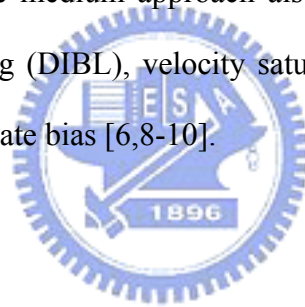
2-3. Shift Register

The most fundamental display driver circuit (for both active- and passive-matrix displays) is a shift register. In this section, we will describe the operation principle of a clocked CMOS (C^2MOS) type edge-triggered shift register.

2-3-1. Introduction

The periphery circuit blocks of LCD panel are composed of four parts-display panel, timing controller, scan driver and data driver. In Fig. 2-3-1 is the system diagram of the LCD panel driver circuits [11]. Timing controller is responsible for transiting RGB (red, green and blue) signals to data driver and controlling the behavior of scan driver.

Generally speaking, TCON (timing controller) is a key element in LCD panel. It

is essentially the brain, the control center, and the heart of a LCD panel. The circuit blocks of timing controller are composed of a counter and an output generating circuit (clocked flip-flops and shift registers), which decodes the output from the counter to generate control signals at corresponding time. Please refer to Fig. 2-3-2 for input and output signals employed.

Data driver, shown in Fig. 2-3-3, mainly contains shift register, data latch, level shifter, digital to analog converter and output buffer. Furthermore, the first three parts classify as digital architectures. The other two parts belong to analog architectures. Shift register and data latch manage to transit and store the RGB signals. They must work under higher frequency while operating in higher resolution display. For a 320× 240 QVGA product as an example, if its sweep frequency of scan driver is 60 Hz, the operating frequency of data driver and timing controller will up to 13MHz.

2-3-2. Selection of Shift Register

A conventional master-slave D flip-flop [12](type of D-latch shift register) is shown in Fig. 2-3-3. It is composed of two level-sensitive latches. Each latch consists of two CMOS transmission gates and two inverters. The block chain generates the clock signal ($\varphi1$) and its inverse ($\varphi2$). The total number of transistors used, including the clock chain is 20. To reduce the transistor count, the NMOS or PMOS transmission gate can be used to replace the CMOS transmission gate. Thus, a low power D flip-flop can be constructed as show in Fig. 2-3-4. However, it suffers from the subthreshold currents if there is a voltage difference across the feedback PMOS pass transistor [13,14].

In addition, our experience with NMOS digital circuit such as shift registers and AMLCD line drivers on a polysilicon process has confirmed the disadvantages well know to those involved with crystalline silicon. The power dissipation at low and

medium frequencies is higher because NMOS inverters draw a DC standing current. Furthermore the pull-up enhancement load of a NMOS inverter severely limits circuit performance. At best one can trade off performance with voltage and power dissipation since the load device requires higher gate voltage to maintain speed and voltage swing.

Based on the above, it has been said that fewer transistors lead to less power dissipation, but that is not strictly true [15]. Broadly speaking, a D flip-flop consists of the CMOS transistor is the reasonable design for LTPS TFTs. Fig. 2-3-5 shows a different version of the CMOS D flip-flop. Although the circuit appears to be quite different from that show in Fig. 2-3-3 , the basic operation principle of the circuit is the same as that shown in Fig. 2-3-5. The operation of a clocked CMOS (C^2MOS) flip-flop will be described below.

2-3-3. Operation of Clocked CMOS (C^2MOS) Shift Register

The first tristate inverter acts as the input switch, accepting the input signal when the clock is high. At this time, the second tristate inverter is at its high-impedance state, and the output Q is following the input signal. When the clock goes low, the input buffer becomes inactive, and the second tristate inverter completes the two-inverter loop, which preserves its state until the next clock pulse.

Considering the two-stage master-slave flip-flop circuit which is constructed by simply cascading two D-latch circuits. The first stage (master) is driven by the clock signal, while the second stage (slave) is driven by the inversed clock signal. Thus, the master stage is positive level-sensitive, while the slave stage is negative level-sensitive. The timing diagram which is shown in Fig. 2-3-6 displays the start pulse and the n-stage output signal.

2-4. Determination of the Delay Time and Operation Frequency

Propagation delay has a deep connection with operation frequency. The operating frequency means that of the dot clock (CLK and inversed CLK) when the pulse was not forwarded to the next shift resistor. The maximum clock frequency of a shift register (defined as the maximum frequency for bit error-free operation) depends on the register's propagation delay and, as such, is a function of device characteristics (e.g., effective mobility and threshold voltage), device geometry (e.g., primarily channel length) and operation conditions (e.g., supply voltage and clock signal levels). Fig. 2-4-1 and Fig. 2-4-2 show the typical simulation results from 1st stage (Q [1]) to 3rd stage (Q [3]) while operating at 15MHz and 19MHz of 5V, respectively. From Fig. 2-4-2, as we have mentioned before, the increase of operation frequency causes the pulse was not forwarded to the next shift resistor.

For investigating the transition mechanism of delay effect, a shift register simulation used Monte Carlo method at 15MHz are shown in Fig. 2-4-3 and Fig. 2-4-4. By definition, T_{delay} is the time delay between the V50%-transition of the rising/falling clock voltage and V50%-transition of the rising output voltage. The simulation waveforms from nth stage (Q [n]) to (n+1)th stage (Q [n+1]) in Fig. and Fig. display two results. When T_{delay} is smaller than 1/2 clock cycles, the signal propagation from forward stage (Q[n]) to next stage (Q[n+1]) can be operated normally. On the contrary, there is showing the failed results for bit error operation, i.e., transition characteristic distortion if T_{delay} is larger than 1/2 clock cycles.

In fact, T_{delay} consists of T_{C2MOS} and T_{Inv} ($T_{delay} = T_{C^2MOS} + T_{Inv}$). We will refer to Fig. 2-4-5 for the determinations of T_{C2MOS} and T_{Inv}. T_{C^2MOS} is defined here as the time delay between the V50%-transition of the rising/falling clock voltage and V50%-transition of the falling output voltage of clocked inverter. Similarly, T_{Inv} is

defined here as the time delay between the V50%-transition of the falling output voltage of clocked inverter and V50%-transition of the rising output voltage of inverter. We shall have more to say about derivation of T_{delay} in next section later on.

Chapter 3

Impact Analysis of Device Parameters

3-1. Model Analysis

In this section, we firstly start from the equation derivation of T_{delay} based on the RPI model of HSPICE. From the equations, we observe that the Vth and mobility are the dominate factors affect the circuit performance. Before simulating, therefore, we have to discuss the distribution device parameters in practice.

3-1-1. Derivation of Delay Time

A unified model can be obtained for the drain current (I_d) by combining the above-threshold and the subthreshold currents as follows:

$$\frac{1}{I_d} = \frac{1}{I_{sub}} + \frac{1}{I_a} \tag{3-1}$$

In the operation of digital circuit, the V_G always works larger than subthreshold region, that is to say Eq. (3-1) can be written as $\frac{1}{I_d} \approx \frac{1}{I_a}$.

The poly-Si TFT models developed by Jacunski et al.[1] are essentially unified models for long-channel devices. Above threshold ($V_{GT}>0$), the conducting channel (I_a) in the non-saturated regime and saturation region is given by an expression similar to that used for long-channel crystalline MOSFETs. The transfer I-V characteristics of polysilicon TFT based on HSPICE RPI model [2] can be expressed as

$$I_a = \frac{\mu_{FET} \cdot C_{ox} \cdot W_{eff}}{L_{eff}} (V_{GT} \cdot V_{DS} - \frac{V_{DS}^2}{2 \cdot \alpha_{sat}}) \ \text{ For } \ V_{DS} \leq \alpha_{sat} \cdot V_{GTE} \tag{3-2}$$

$$I_a = \frac{\mu_{FET} \cdot C_{ox} \cdot W_{eff} \cdot V_{GT}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} \quad \text{For} \quad V_{DS} \geq \alpha_{sat} \cdot V_{GTE} \tag{3-3}$$

Here, μ_{FET} is the gate voltage dependent field-effect mobility that includes the effects of the trap states; $C_{ox} = \varepsilon_i/d_i$ is the oxide capacitance per unit area, where ε_i is the dielectric permittivity and d_i is the thickness of the gate oxide; W and L are the effective gate width and length, respectively; α_{sat} is the body constant; $V_{GT} \equiv V_{GS} - V_T$ is the effective extrinsic gate voltage swing, where V_{GS} and V_T are extrinsic gate-source voltage and threshold voltage given by the following interpolation function that tends to V_{DS} in the linear regime and to the saturation voltage V_{sat} in saturation.

In poly-Si TFTs, not all charge carriers induced in the channel by the gate voltage will be free to contribute to the drain current. Instead, a significant of the carriers will be captured by traps associated with the grain boundaries, especially near and below threshold. This effect can be taken into account by proposing so-call field effect mobility as follows:

$$\mu_{FET} = \frac{1}{MU0} + \frac{1}{\mu 1 \cdot (\frac{2 \cdot V_{GTE}}{V_{sth}})^{MMU}} \tag{3-4}$$

Where MMU, $MU0$ and μ_1 are extractable mobility parameter.

The second term of Eq. (3-4) is the low filed effect of polysilicon TFTs. Assuming the supply voltage is larger than 5V in digital circuit, the low filed effect can be usually neglected, which reduce the α_{sat} value to be 1.

Therefore, the drain current I_D of polysilicon TFT can be simplified to

$$I_D = \frac{1}{2} MU0 \cdot C_{ox} \cdot \frac{W}{L} \left[2(V_G - V_{to}) - V_D^2 \right] \quad \text{For linear region} \tag{3-5}$$

$$I_D = \frac{1}{2} MU0 \cdot C_{ox} \cdot \frac{W}{L} (V_G - V_{to})^2 \quad \text{For saturation region} \tag{3-6}$$

Obviously, this I-V characteristic is very similar to that in MOSFETs, expect that the mobility and threshold voltage are modified.

Once we determine the equations of drain current I_D of polysilicon TFT, we will calculate T_{delay} by solving the state equation of the output node in the time domain. For deriving the equation of T_{delay}, see the definition of propagation delay times τ_{PHL} and τ_{PLH} [3], then T_{C^2MOS} and T_{Inv} can be expressed as

$$T_{C^2MOS} = \frac{C_{load1}}{k_n(V_{DD}-V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD}-V_{T,n}} + ln(\frac{4(V_{DD}-V_{T,n})}{V_{DD}} - 1)\right] \qquad (3\text{-}7)$$

$$T_{Inv} = \frac{C_{load2}}{k_p(V_{DD}-|V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD}-|V_{T,p}|} + ln(\frac{4(V_{DD}-|V_{T,p}|)}{V_{DD}} - 1)\right] \qquad (3\text{-}8)$$

where the first term of delay component in the above equations is obtained during the NMOS/PMOS transistor operates in the saturation region. The second term of delay component is obtained during the NMOS/PMOS transistor operates in the linear region.

It is obvious that Eq. (3-6) and Eq. (3-7) are too complex to analyze because of including ln factor in the delay equations. In order to analyze the equations briefly, the first order Taylor's approximation is used for simplification process, Eq. (3-6) and Eq. (3-7) then can be approximated as

$$T_{C^2MOS} = \frac{V_{DD}}{2C_{ox}} \cdot \frac{C_{load1}}{MU0_n \cdot (W_1/L)(V_{DD}-V_{ton})^\beta} \qquad (3\text{-}8)$$

$$T_{Inv} = \frac{V_{DD}}{2C_{ox}} \cdot \frac{C_{load2}}{MU0_p \cdot (W_2/L)(V_{DD}-|V_{top}|)^\beta} \qquad (3\text{-}9)$$

Finally, the complete equation of T_{delay} consist of T_{C^2MOS} and T_{Inv} can be written as

$$Tdelay = \frac{V_{DD}}{2C_{ox}} \left(\frac{C_{load1}}{MU0_n \cdot (W_1/L)(V_{DD} - V_{ton})^{\beta}} + \frac{C_{load2}}{MU0_p \cdot (W_2/L)(V_{DD} - |V_{top}|)^{\beta}} \right) \qquad (3\text{-}10)$$

Thus, we will adopt Eq. (3-10) to discuss the impact sensitivity of the Vth and mobility while operating at a regular frequency.

3-1-2. Distribution of Device parameters

Before simulating, we have to know the distribution of device parameters. In order to examine the distribution of measured data and deviation from the normal distribution, we adopt the histogram, the Q-Q plot (quantile-quantile plots) and the detrend Q-Q plot. The histogram is the most common graph of a frequency distribution. To test the normality of the distribution, the graphical methods include the use of probability plots are develop. These can be either P-P plots (probability-probability plots), in which the empirical probabilities are plotted against the theoretical probabilities for the distribution, or Q-Q plots (quantile-quantile plots), in which the sample points are plotted against the theoretical quantiles. The Q-Q plots are more common because they are invariant to differences in scale and location. If the assumed population is correct, then the observed value and the excepted value for each case would be very close to each other. If the observations come from a specific distribution, then the plotted point should roughly lie on a straight line. On the other hand, if the assumed population is not correct, then the observed and excepted value would not be approximately the same and the points in this plot would not follow the 45° straight line. Thus, if the points in this plot are close to the line of identity, this plot supports the reasonableness of the assumed population distribution. For the same reason, if the plotted points deviate markedly from the line of identity, then the plots also provide evidence that the assumed distribution is not the appropriate model to describe the observed values. Especially for the normal distribution, the Q-Q plots are

known as the normal probability plots, which are adopted in this thesis.

A residual is the difference between an observed value and the corresponding anticipated value. A graphic presentation of residuals, call a residual plot, is useful for highlighting major departures between the observed and the anticipated patterns or relationships in a data set. The detrend Q-Q plot is one of the residual analysis. The residual analysis refers to ser of diagnostic methods for investigating the appropriateness of a regression model utilizing the residuals. If a regression model us appropriate, the residuals should reflect the properties ascribed to the mode error terms ε_i. For example, since regression model assumes that the ε_i are normal random variables with constant variance, the residuals should show a pattern consistent with these properties. If the model is appropriate, the residuals should reflect the properties ascribed to the model error terms. Using the normal probability plots of the residuals, where the ranked residuals are plotted against their expected values under normality, we may further investigate the difference between the distribution of the measured data and the normal distribution.

We first start from the device on different glass. Fig. 3-1-1 and 3-1-2 are the average and deviation values of the threshold voltage and electron mobility of specific device position on different glasses. The relative position of site A to H is defined in Fig. 3-1-3. From Fig. 3-1-1, it can be seen that the average value range of the Vth of these sites is from 0.96V to 1.29V, while the standard deviation range is from 0.33V to 0.52V. The standard deviation of total devices is about 0.446V.

Fig. 3-1-4. to Fig. 3-1-9 are the histogram plot, the corresponding Q-Q plot, and the detrend Q-Q plot of, the Vth and mobility. It can be seen that Vth is similar to normal distribution. Refer to the Q-Q plot and the detrend Q-Q plot, the observed values the fitting normal distribution values are both very close. The distribution of

Vth meets our expectation since from the view point of statistical process control, the device parameters should exhibit normal distribution under well-controlled process condition. However, the distribution of mobility shows abnormal distribution based on the Q-Q plot and the detrend Q-Q plot.

3-2. Monte Carlo Simulation V.S. Sensitivity Analysis

To observe the sensitivity of delay, we have two ways to analyze it. The simplest analysis method of sensitivity obtained from derivation of delay equations. Instead, the other method uses Monte Carlo runs. In this section, we will discuss the differences of deviation of delay equations compared with Monte Carlo simulation.

3-2-1. Classical Sensitivity Function

Specifically, for analyzing propagation delay we are usually interested in finding how sensitive their deviations are relative to device variations. These sensitivities can be quantified using the classical sensitivity function S_x^y, defined

$$S_x^y \equiv \lim_{\Delta x \to 0} \frac{\Delta y / y}{\Delta x / x} \qquad (3\text{-}11)$$

Thus

$$S_x^y = \frac{\partial y}{\partial x} \cdot \frac{x}{y} \qquad (3\text{-}12)$$

Here, x denotes the values of component (e.g., Vth, mobility or swing) and y denotes a circuit a circuit parameter of interest (e.g., propagation delay).

We will refer above definition to observe the relationship between device variations and propagation delays.

3-2-1. Simulation Condition

To simulate the sensitivity of propagation delay at a regular frequency the

parameters given in Table I varied one at a time with the rest at nominal value. The threshold voltage parameters VTO and mobility parameters MU0 of N-type and P-type TFTs are +1.5 and -1.5V with the 3σ variation range of ±1.5V, as well as 77.1 and 85 cm^2/Vs with the 3σ variation range of ±21cm^2/Vs, respectively. One stage shift register is simulated by Monte Carlo method for 100 times with 5V at 1MHz. The width design of inverter is twice of colocked inverter due to the loading of inverter is twice than clocked inverter. Here, the designs of W_n/W_p and L are 4/5 and 6um, respectively.

3-2-2. Vth effect

Here, we rewrite Eq. (3-10) again for convenient derivation of sensitivity.

$$Tdelay = \frac{V_{DD}}{2C_{ox}}(\frac{C_{load1}}{MU0_n \cdot (W_1/L)(V_{DD}-V_{ton})^\beta} + \frac{C_{load2}}{MU0_p \cdot (W_2/L)(V_{DD}-|V_{top}|)^\beta})$$

The sensitivity of Vth variation relative to delay time can be defined as

$$S_{T_{delay}}^{V_{th}} = \frac{\partial T_{delay}}{\partial V_{th}} \cdot \frac{V_{th}}{T_{delay}} \tag{3-13}$$

Thus, the sensitivities of the threshold voltage parameters VTO of N-type and P-type TFTs can be written as

$$S_{T_{delay}}^{V_{ton}} \propto \frac{\beta \cdot V_{ton}}{MU0_n \cdot (V_{DD}-V_{ton})} \tag{3-14}$$

$$S_{T_{delay}}^{V_{top}} \propto \frac{\beta \cdot |V_{top}|}{MU0_p \cdot (V_{DD}-|V_{top}|)} \tag{3-15}$$

Fig. 3-2-1 and 3-2-2 show the dependences of Vth variation on average and deviation delay for Monte Carlo simulation, respectively. From Fig. 3-2-2, it can be seen that the deviation of delay has positive correlation as Vth variation. It seems reasonable to suppose that the Monte Carlo results correspond to Eq. (3-14) and Eq.

(3-15). In addition, we may note, in passing, that the deviation of delay for N-type TFTs is larger than P-type TFTs due to mobility of N-type TFTs is smaller than P-type TFTs.

3-2-3. Mobility effect

In the same way, the sensitivity of Vth variation relative to delay time can be defined as

$$S_{T_{delay}}^{\mu} = \frac{\partial T_{delay}}{\partial \mu} \cdot \frac{\mu}{T_{delay}} \tag{3-16}$$

The sensitivities, therefore, of the mobility parameters MU0 of N-type and P-type TFTs can be written as

$$S_{T_{delay}}^{\mu_n} \propto \frac{1}{MU0_n} \tag{3-17}$$

$$S_{T_{delay}}^{\mu_p} \propto \frac{1}{MU0_p} \tag{3-18}$$

To compare simulations with above equations, the Monte Carlo results are shown in Fig. 3-2-3 and 3-2-4. From Fig. 3-2-4, the deviations of delay for 100 Monte Carlo runs show a linear dependence with mobility variations, as exception for above sensitivity equations. It is obvious that the mobility variations of N-type TFTs of delay are also larger than P-type TFTs.

3-2-4. Vth and Mobility Effect

After individually discussing the dependence of Vth and mobility variations on the deviation of delay, now we want to know which one is the most important factor in digital circuit. Fig. 3-2-5 shows the dependences of Vth, mobility and both variations on deviation of delay with 100 Monte Carlo runs, respectively. From Fig. 3-3-5, it can be seen that the triple range of Vth and mobility variations relative to

delay deviation are about 4.5 and 1 nsec, respectively. Moreover, we observe that the deviation value of delay is up to 5 nsec while considering both Vth and mobility variations. The results make it clear that the variation of Vth is more important than mobility in digital circuit. Thus, the simulation of Vth variation will play a impact role on front-end design section.
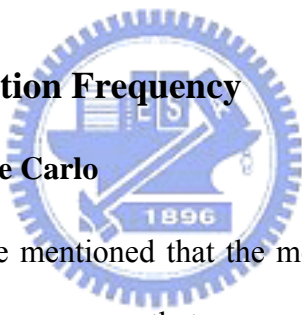
Chapter 4

Simulation Skill

From the chapter above, we have described a method to determine operation frequency from delay time, and it is also demonstrated that the Vth variation of device mainly affects circuit performance in whole parameters. In this chapter, we wil propose a simulation skill to predict operation frequency of an n-stage shift register through simplifying propagation delay from an n-stage one to an 1-stage one. The power dissipation of an n-stage shift register is also estimated in the same way.

4-1. Estimation of Operation Frequency

4-1-1. Worst Case V.S. Monte Carlo

In the chapter 2, we have mentioned that the most frequently used Worst-Case parameters in a practical design are ones that represent "maximum" and "minimum" current of PTFT and NTFT transistors. Because the delay time of cells depend on transistor current, "maximum" and "minimum" parameters correspond to the "fast " and "slow" case, respectively. Although Worst-Case is widely used in a practical design, it does not have enough accuracy while comparing with that of a Monte Carlo analysis. Fig. 4-1-1 shows a distribution of gate delay calculated by the Monte Carlo analysis with 1000 SPICE simulations. Two worst-case values calculated by Worst-Case and Monte Carlo analysis are indicated as "corner" and "MC", respectively. From Fig. 4-1-1, the worst-case rang of the Worst-Case simulation is 19% wider than the range of the Monte Carlo analysis. In order to obtain the high accuracy of Monte Carlo analysis, one has to develop simulation skills to save

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simulation time.

4-1-2. One-Stage Shift Register

Over the past few years, several studies [2,3] have been conducted on future application potential of LTPS TFT LCD display. Some of the most compelling studies have focused on typical simulation of an one-stage shift register. For example, Fig. 4-1-2 shows the operating frequency of a shift register simulated as a function of variations in the field effective electron mobility and channel length. The results show the interesting trends while designing LTPS TFTs digital circuits, e.g. , when a timing controller with a 3V voltage source is integrated into LCD panel whose resolution is VGA (25 MHz dot clock), the electron mobility of an N-type TFT higher than 200 cm2/Vs and channel length shorter than 2um for the TFT characteristics are needed.

However, little attention has been given to the estimation of delay with device variations. Let us begin with the observation of one-stage simulations for Monte Carlo method compared with typical method. The trend of operation frequencies of one-stage shift register with different supply voltages were investigated by means of Monte Carlo and Worst Case simulations using Vth $\pm$ 3σ $_{Vth}$, as shown in Fig. 4-1-3. From Fig. 4-1-3, the typical result obviously over-estimating than Monte Carlo results.

It is said that one-stage simulations have an advantage in predicting operating frequency in LTPS TFTs digital circuits. However, there seems to be no established theory to explain this trend. In digital circuits a path delay is one of the most important performances, so that it is necessary to analyze the variability of the path delay. In next section, we will now discuss the derivation of path delay from one-stage to n-stage shift register more closely.

4-1-3. N-Stage Shift Register

First of all, we will focus our attention on deviation of path delay [1]. The probability distribution function pdf of gate delay can be modeled by an normal distribution function $N(m, \sigma^2)$ fully characterized by its mean value and its variance $\sigma^2 = (\sigma_{delay})^2$ by

$$f(d_{delay}) = \frac{1}{\sqrt{2\pi} \cdot \sigma_{delay}} \cdot e^{-0.5[(d_{delay} - \bar{d}_{delay})^2 / (\sigma_{delay})^2]} \tag{4-1}$$

where σ_{delay} is defined as the deviation of half-stage delay

The average delay of a path comprising n stages corresponds to the linear combination of the n pdfs of the gate delays. The average path delay is given by

$$\bar{d}_{path} = \sum_i^n d_{delay_i} \tag{4-2}$$

With the symmetrical covariance matrix $\underset{\sim}{C}$

$$\underset{\sim}{C} = \begin{bmatrix} c_{11} & \dots & c_{1n} \\ c_{21} & \dots & c_{2n} \\ \dots & \dots & \dots \\ c_{n1} & \dots & c_{nn} \end{bmatrix} \quad \text{and}$$

$$c_{ij} = \sigma_{delaye_i} \cdot \sigma_{delay_j} \cdot \rho_{ij}$$

$$c_{ii} = \sigma^2_{delay_i} \tag{4-3}$$

ρ_{ij} : correlation between two different half-stages

the variance of the path can be expressed as

$$(\sigma_{path})^2 = \sum_i^n \sum_j^n \sigma_{delaye_i} \cdot \sigma_{delay_j} \cdot \rho_{ij} \tag{4-4}$$

$$= \sum_{i}^{n} \sum_{j}^{n} c_{ij} = e^{T} \cdot \underset{\sim}{C} \cdot e \,[4] \tag{4-5}$$

Equation (4-5) can be simplified to

For $\rho_{ij} = \rho$, i.e., the integrate correlation is the same for all half-stages

$$(\sigma_{path})^{2} = \sum_{i}^{n} \sum_{j}^{n} \sigma_{delaye_{i}} \cdot \sigma_{delay_{j}} \cdot \rho + \sum_{i}^{n} (1-\rho) \cdot (\sigma_{delaye_{i}})^{2} \tag{4-6}$$

The distance dependent correlation of the gate delay on the chip is given by the autocorrelation coefficient ρ [5]. As the device variations of each shift register have no relevance to distance, i.e., the device variation is independent to distance. The autocorrelation coefficient ρ can be set to $\rho = 0$. Here, with the variance of a half-stage shift register $\sigma_{delay_{i}}^{2}$, the variance of a path comprising n gates is given as

$$\sigma^{2}_{path} = \sum_{i=1}^{n} \sigma^{2}_{delay_{i}} \tag{4-7}$$
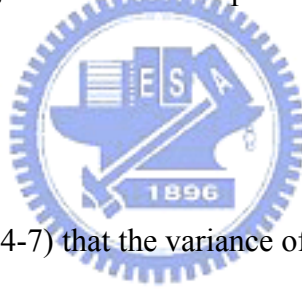
It will be clear from Eq. (4-7) that the variance of a path comprising n half-stages is the linear combination of each half-stage delay. Fig. 4-1-4 shows the average and deviation delays of different nth half-stage on delay time with 30 Monte Carlo simulations. From Fig. 4-1-4, it is seen that the device variations correspond to different deviation of delays $\sigma_{delay_{i}}$ are similar to each other. Thus, Eq. (4-7) can be approximated to

$$\sigma^{2}_{path} = \sum_{i=1}^{n} \sigma^{2}_{delay} \tag{4-8}$$

Finally, as mentioned that the determination of operation frequency determined in chapter 2, operation frequency finally can be written as

$$F = \frac{1}{2 \cdot (m_{delay} + \sigma_{path})} \tag{4-9}$$

where m is described as mean value with Monte Carlo results of an half-stage shift register.

The trend of operation frequencies composed of various n half-stage shift registers with different supply voltages were calculated by Eq. (4-9). The results are shown in Fig. 4-1-5. It was found from the results that operating frequencies showed a reduced ration $\frac{1}{\sqrt{n}}$ while gradually increasing half-stage numbers.

4-2. Estimation of Power Dissipation

The histogram of the power dissipation for the good cases is shown in Fig. 4-1-6, which exhibits normal distribution. This Monte Carlo approach is believed to give better approximation to the actual circuit performance for LTPS TFTs because that it makes no restrictive assumptions on the nature of the relationship between the circuit parameters and the circuit performance.

As for the power consumption, after excluding the failed cases, the linearly product method can be applied, as shown in Table Ⅱ. That is, the power distribution of an *n*-stage shift register circuit (PE*n*) can be estimated by the results of Monte Carlo simulation for 3-stage shift register (PMC3)

Average (PE*n*) = Average (PMC3) $\times\, n\, /\, 3$ (4-10)

and

Deviation (PE*n*) = Deviation (PMC3) $\times \sqrt{n\, /\, 3}$ (4-11)

respectively.

The comparison between PE20 and PMC20 at 10, 11, and 12MHz is listed in Table II. For the frequencies with enough good cases, the errors for the average and deviation are as low as 3% and 8%, respectively.

Chapter 5

Conclusions and Future Work

In this thesis, we investigate the device variation issue in the LTPS TFTs digital circuit. A propagation delay is one of the most important performances, so that it is necessary to analyze the variability of the propagation delay. Firstly we aim at the reason causes the shift register circuit to fail with Monte Carlo simulations. By analyzing the variance of transition characteristic with respect to device variation, we determine the equations of propagation delay corresponds to clock operation frequency. At the same time, we derive the equation derivation of T_{delay} in detail based on the RPI model of HSPICE.

Next we examine the distributions of threshold voltage and mobility variations from different glasses by adopting statistical analysis method with the histogram, the Q-Q plot and the detrend Q-Q plot. It is observe that the distributions of threshold voltage and mobility are the normal and random distributions, respectively. Thus, the Gaussian function of Vth and random function of mobility parameters in the models will be simulated by SPICE. For discussing the sencitivity of Vth and mobility variations on delay compared with Monte Carlo simulation. We start form classical sensitivity function to derive the sensitivity equations of threshold voltage and mobility variations on $T_{delay.}$ The results of the dependences of Vth and mobility variations on average and deviation delay for Monte Carlo simulations are in agreement with the sensitivity equations. Moreover, we also observe the results make it clear that the Vth variations cause the variances of digital circuit are larger than mobility.

For predicting circuit performance, we proposed a simulation skill to save computational time with Monte Carlo simulation. It is founded that the operation frequency of an n-stage shift register can be obtained through simplifying propagation delay from an n-stage one to an 1-stage one. The power dissipation of an n-stage shift register is also estimated in the same way. For the frequencies with enough good cases, the errors for the average and deviation are as low as 3% and 8%, respectively.

From the viewpoints of circuit performance, the variation of device behavior will lead to extra difficulties in prediction. From the scope of statistics, the database of variability can be constructed with different device distance so that one can predict the fluctuation range of device parameter as the device distance is known. In our work, we have classified and quantitatively distinguished macro and micro variation. This would be helpful for designers in predicting the circuit performance and device reliability. We also, furthermore, have to investigate low voltage digital circuit correspond to low field effect before LTPS TFTs can be widely adopted in flat panel display.

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$$f(s_i) = \frac{1}{\sigma_{s_i}\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{s_i - s_i^o}{\sigma_{s_i}}\right)^2\right] \qquad f(s_i) = \begin{cases} \dfrac{1}{b-a}, & a \leq s_i \leq b \\ 0, & otherwise \end{cases}$$

(a)   (b)
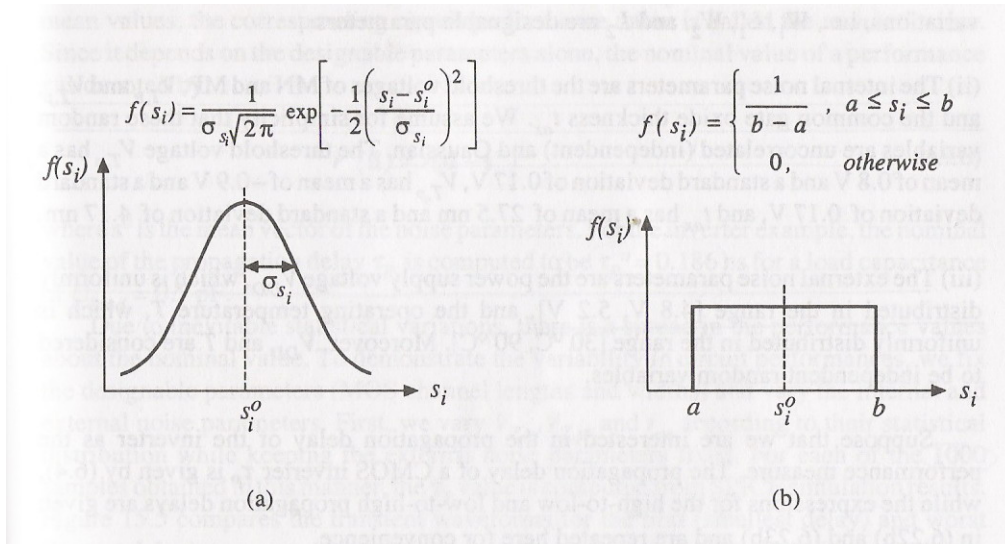
Fig. 2-1-1 Probability density function for (a) a Gaussian and (b) a uniform random variable.
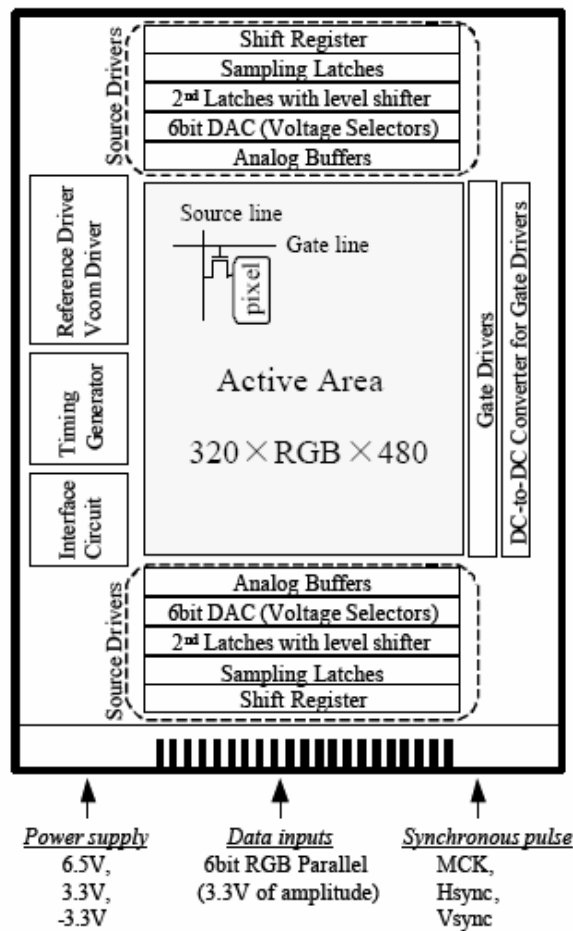
Fig. 2-3-1 System Block Diagram
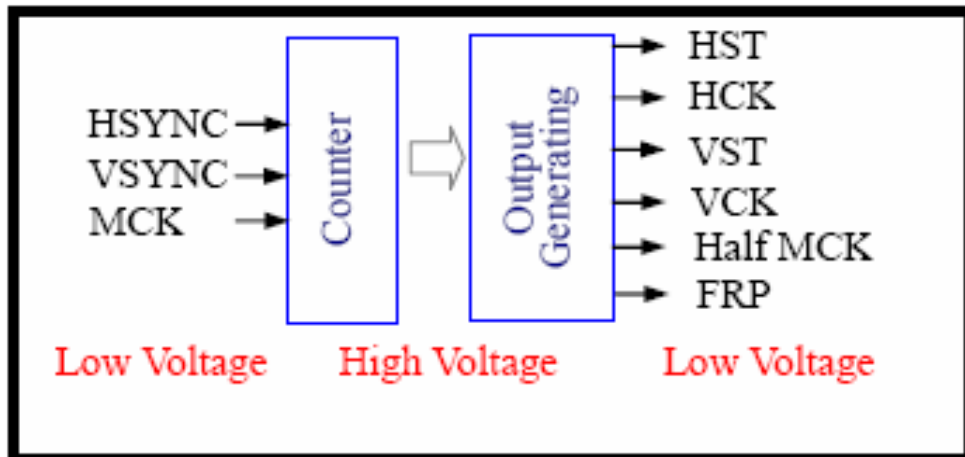
Fig. 2-3-2 Block diagram of Timing Controller
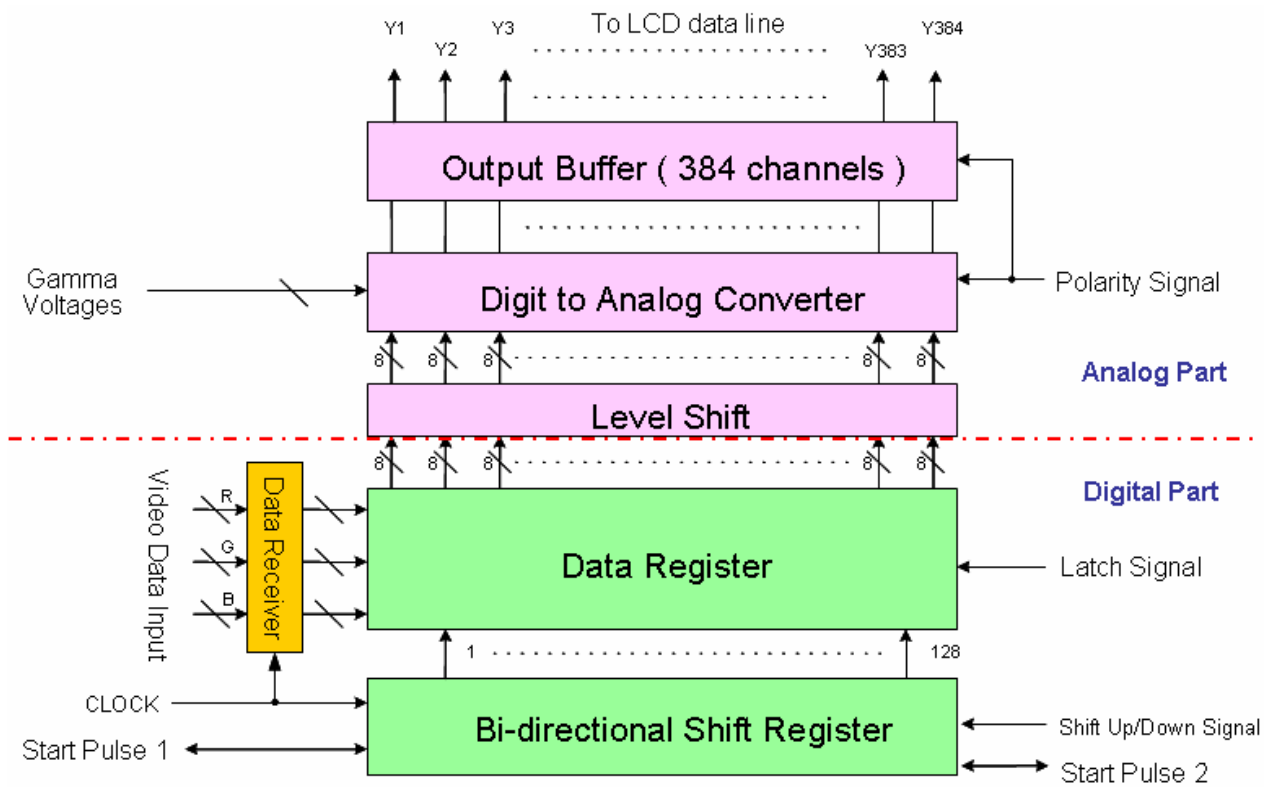
Fig. 2-3-3 Block diagram of Data driver
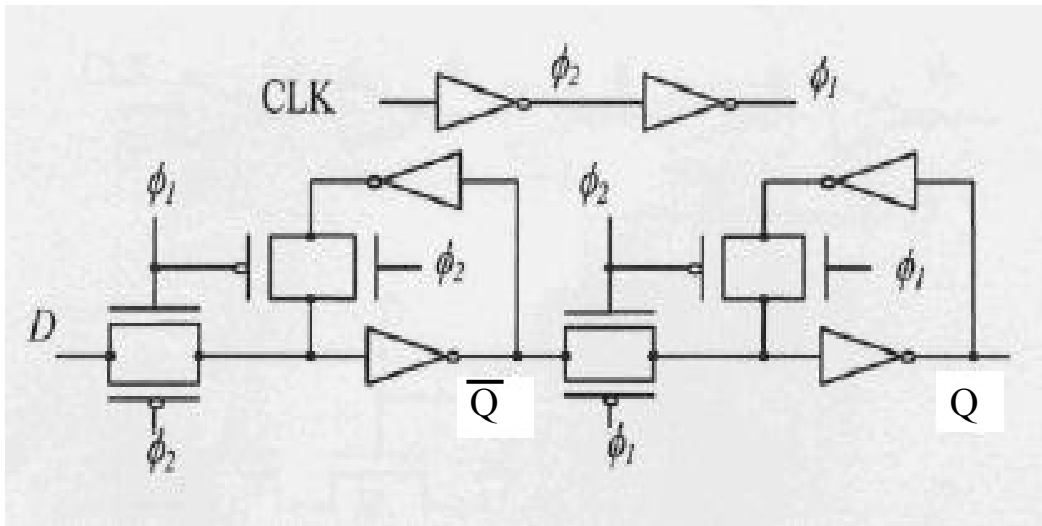
Fig. 2-3-3 The master-slave D flip-flop (version 1)
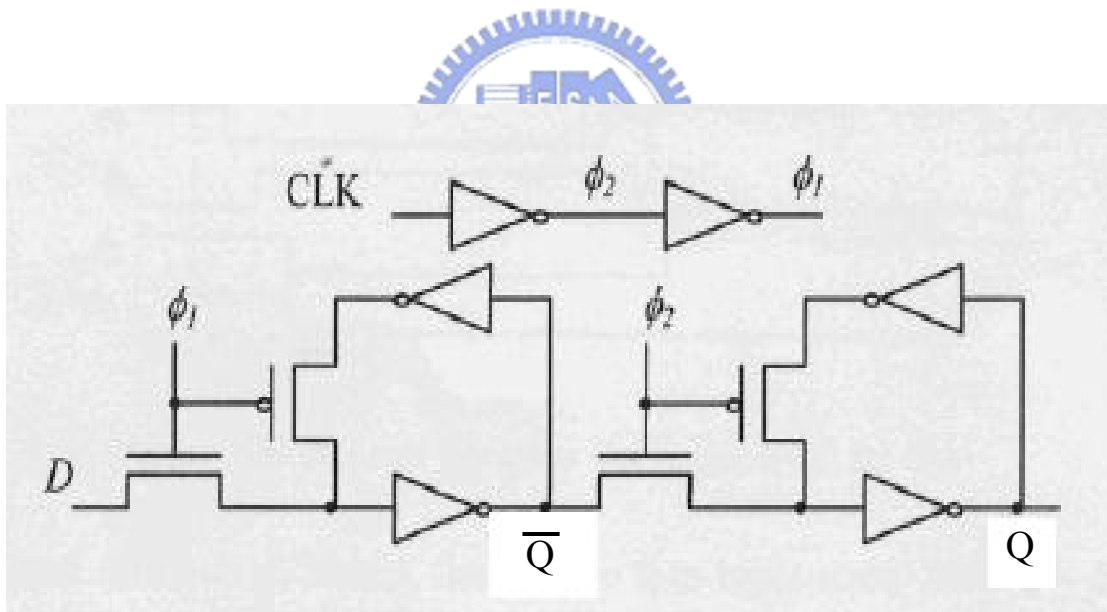
Fig. 2-3-4 The original low-power D flip-flop
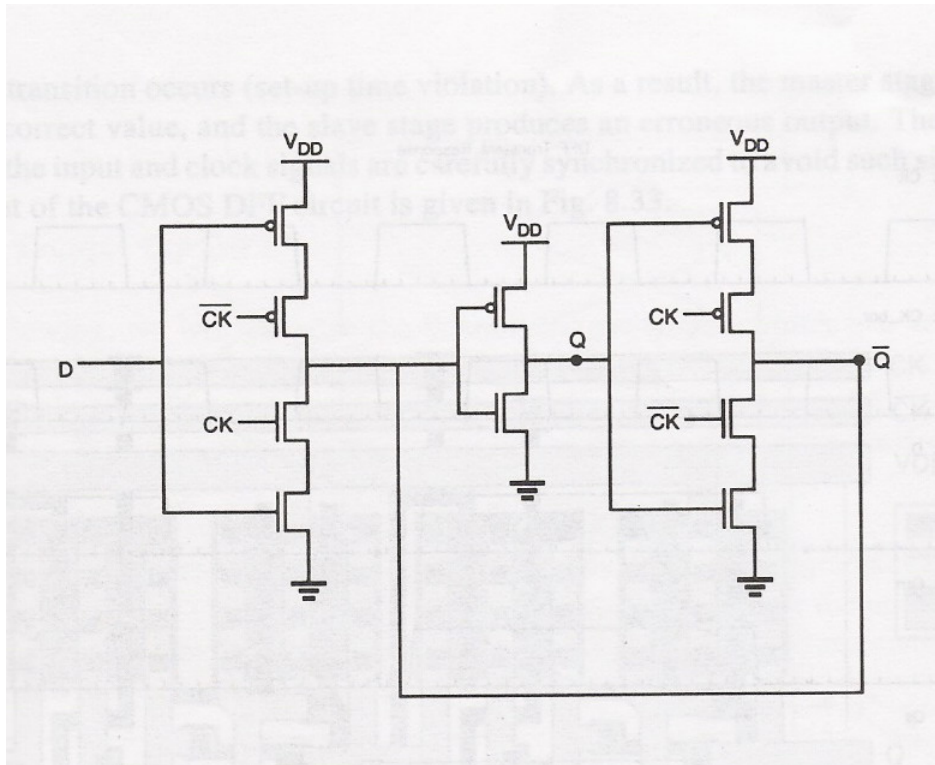
Fig. 2-3-5 CMOS implementation of the D-latch (version 2)
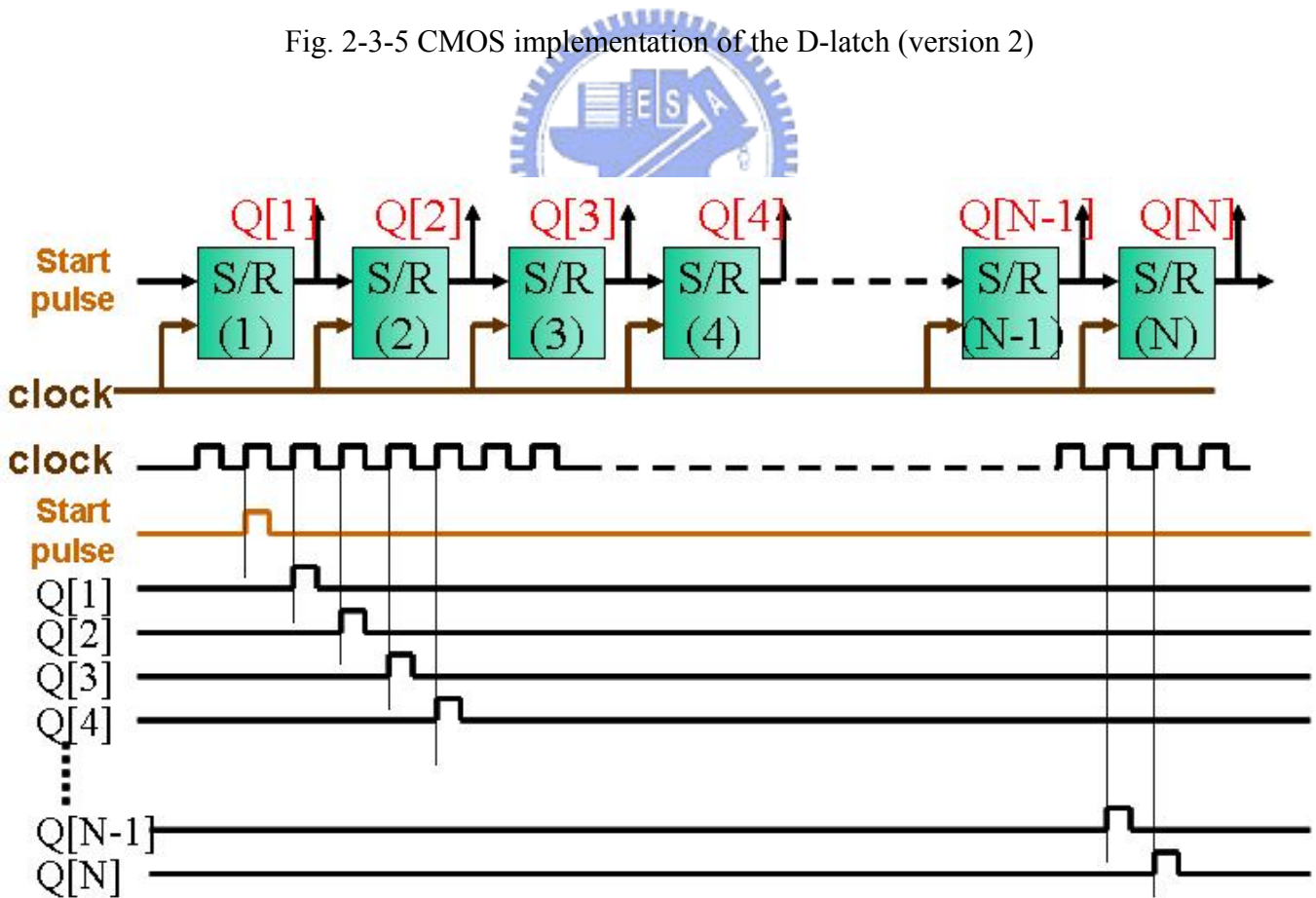
Fig. 2-3-6 Time diagram of shift register
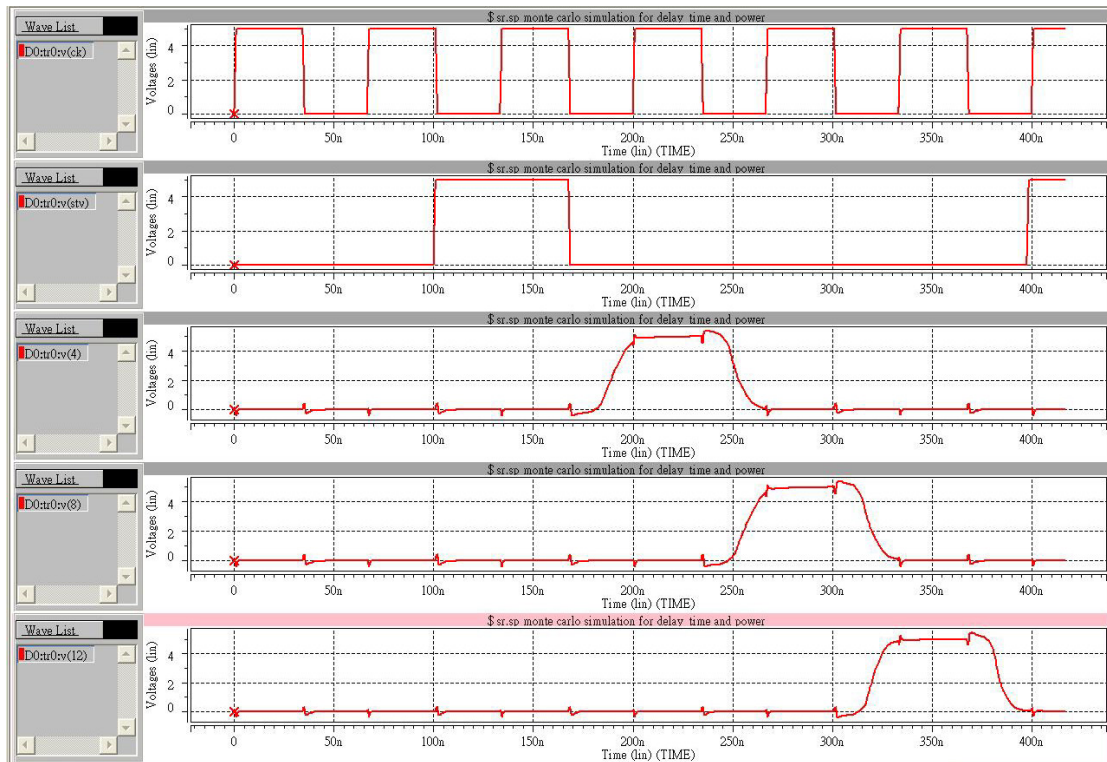
Fig. 2-4-1 Output simulation waveforms of supply voltage 5V, at 15MHz
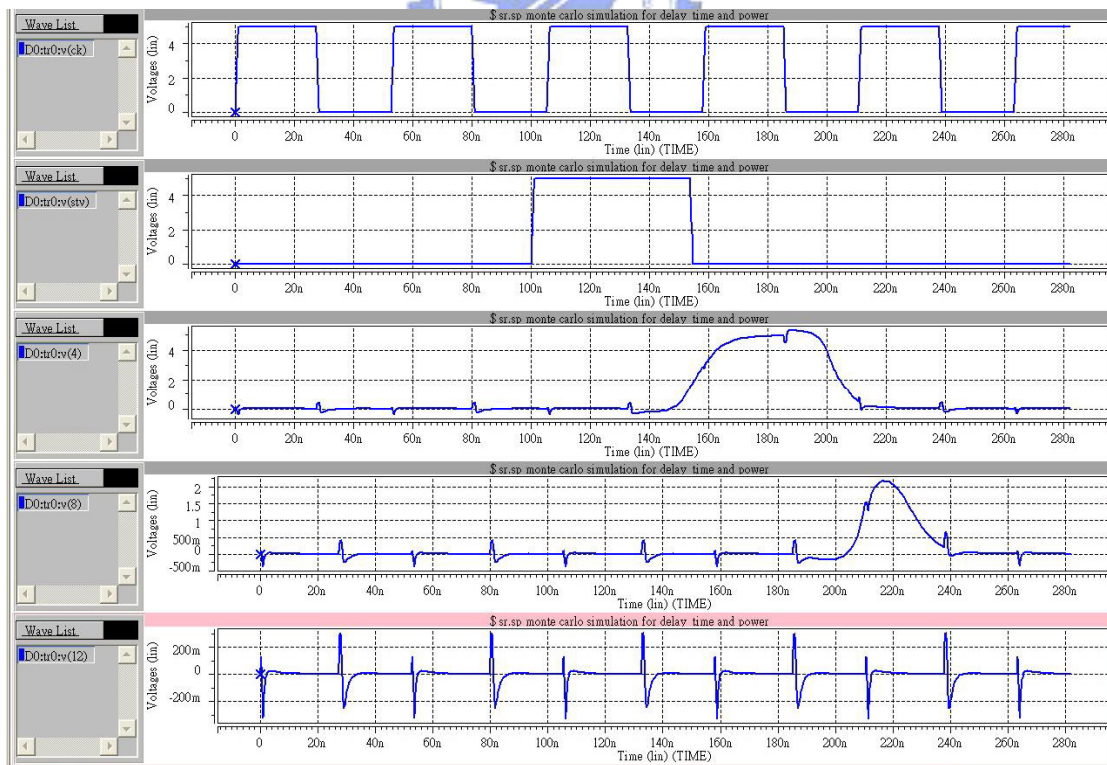
Fig. 2-4-2 Output simulation waveforms of supply voltage 5V, at 19MHz
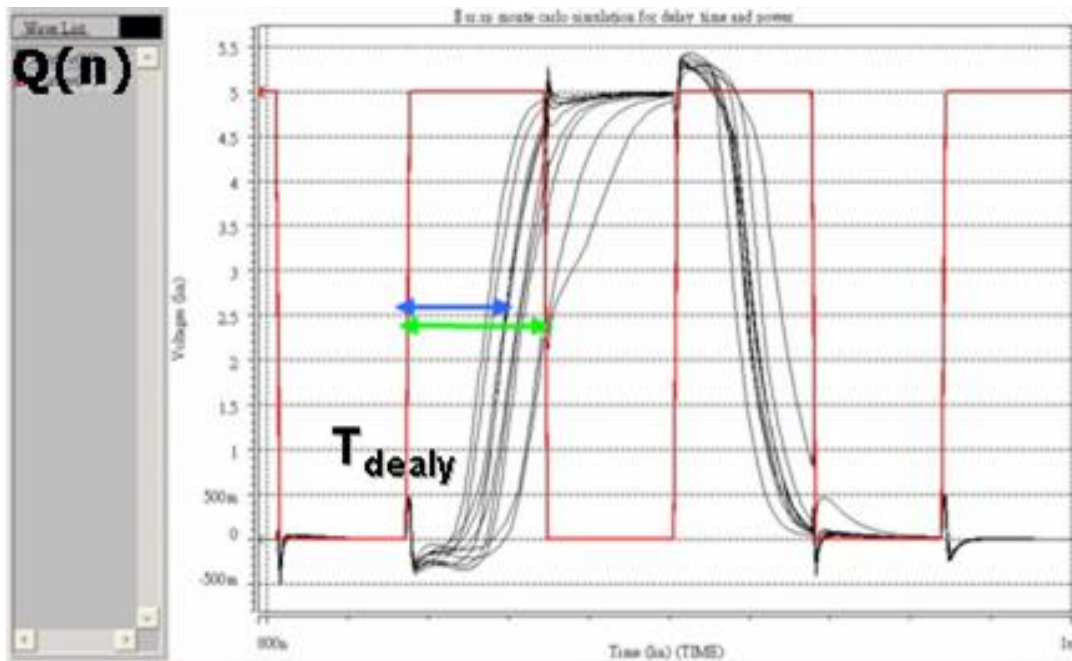
Fig. 2-4-3 Monte Carlo simulation results of n-stage shift register, at 15MHz
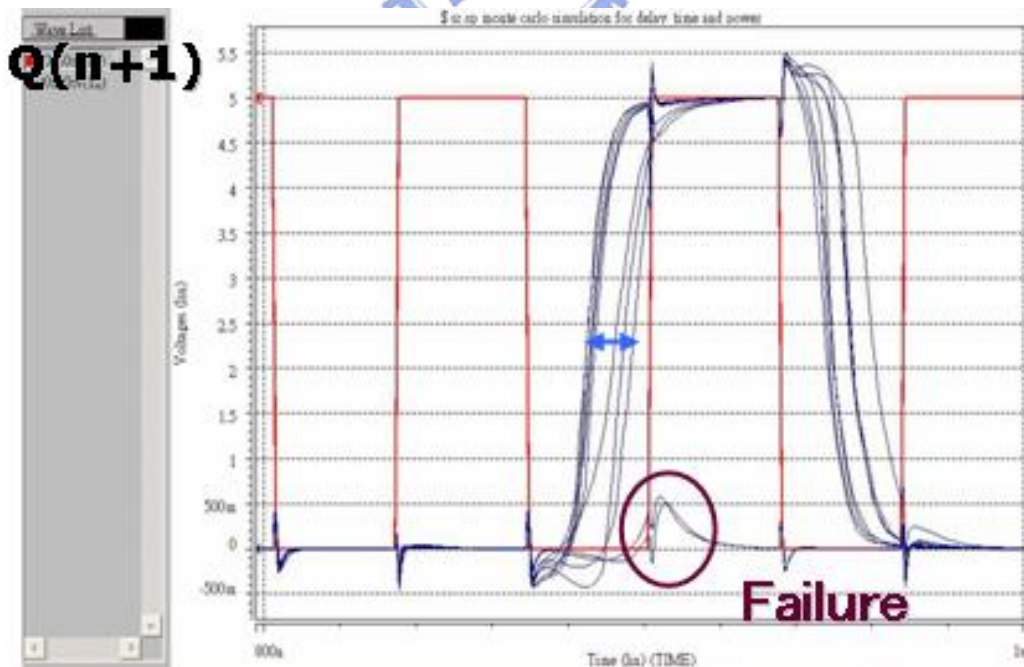
Fig. 2-4-4 Monte Carlo simulation results of n+1-stage shift register, at 15MHz
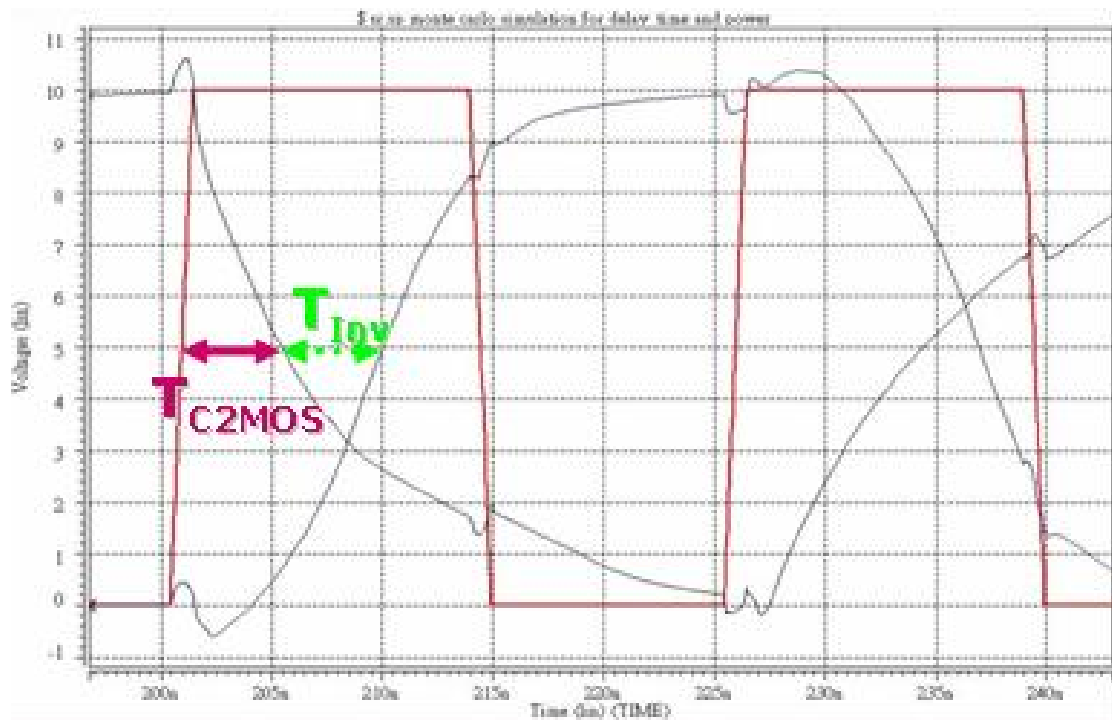
Fig. 2-4-5 T_{dealy} consists of $T_C{}^2{}_{MOS}$ and T_{Inv}
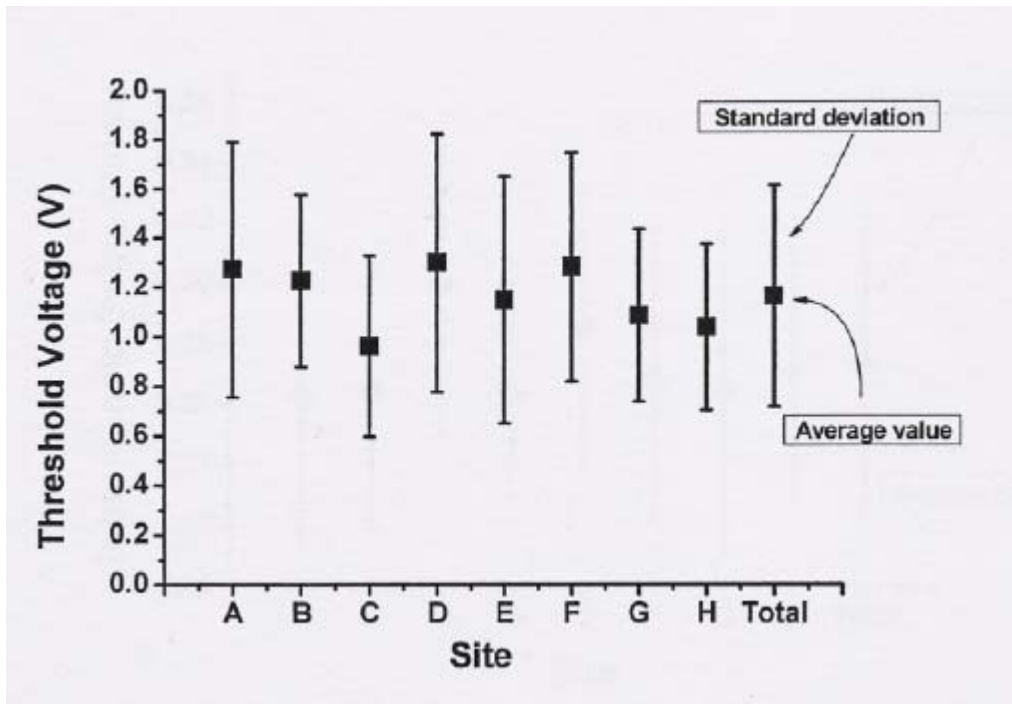
Fig. 3-1-1 The mean value and deviation of threshold voltage of different site.
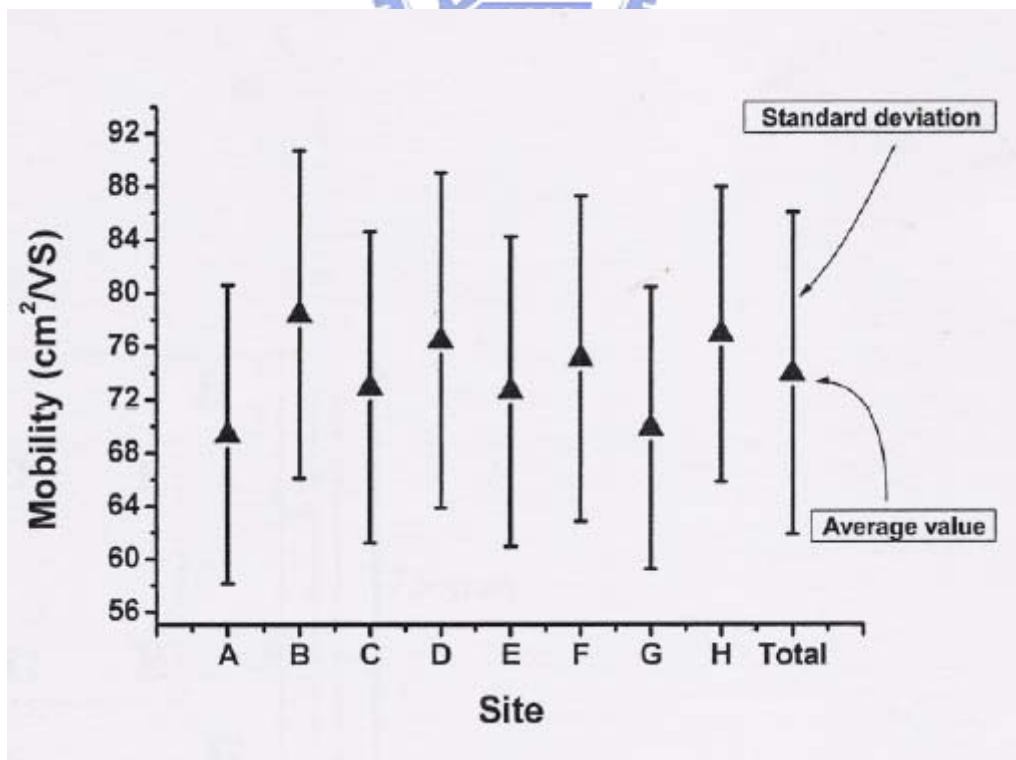
Fig. 3-1-2 The mean value and deviation of mobility of different sites
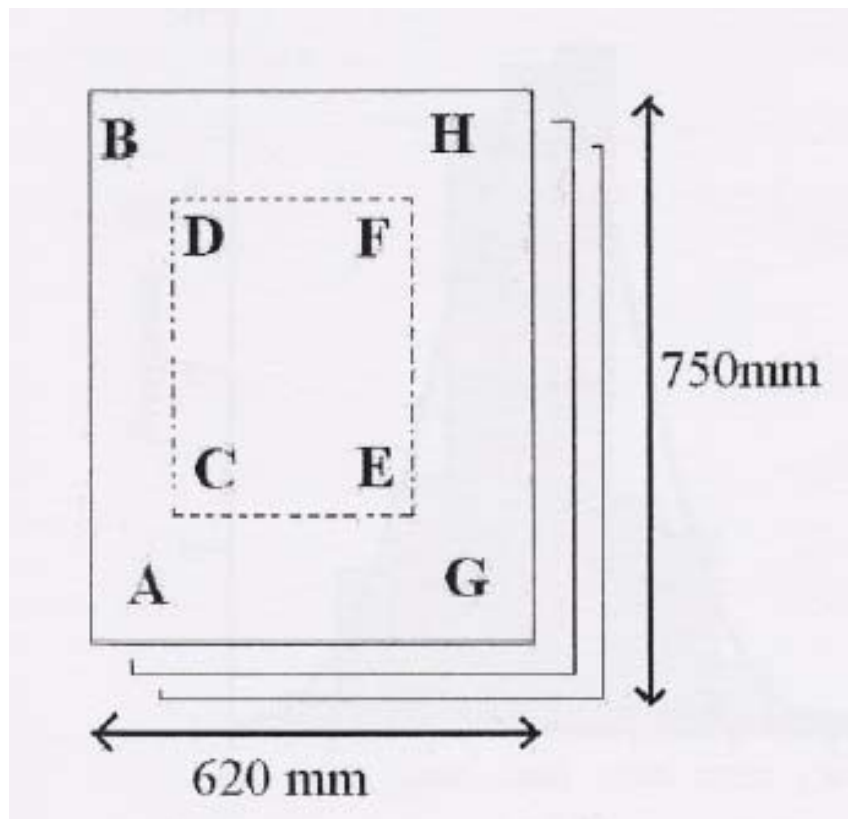
Fig. 3-1-3 The relative position of the eight sites

Horizontal Vth-Histogram

Mean = 1.681583
Std. Dev. = 0.0196779
N = 165
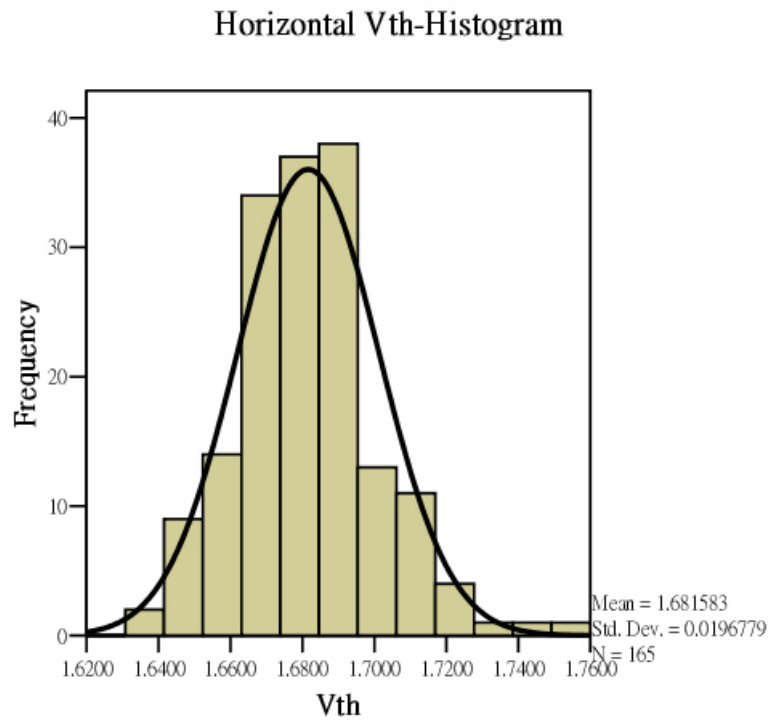
Fig. 3-1-4 The histogram of Vth of horizontal crosstie devices.

Normal Q-Q Plot of Vth of horizontal devices
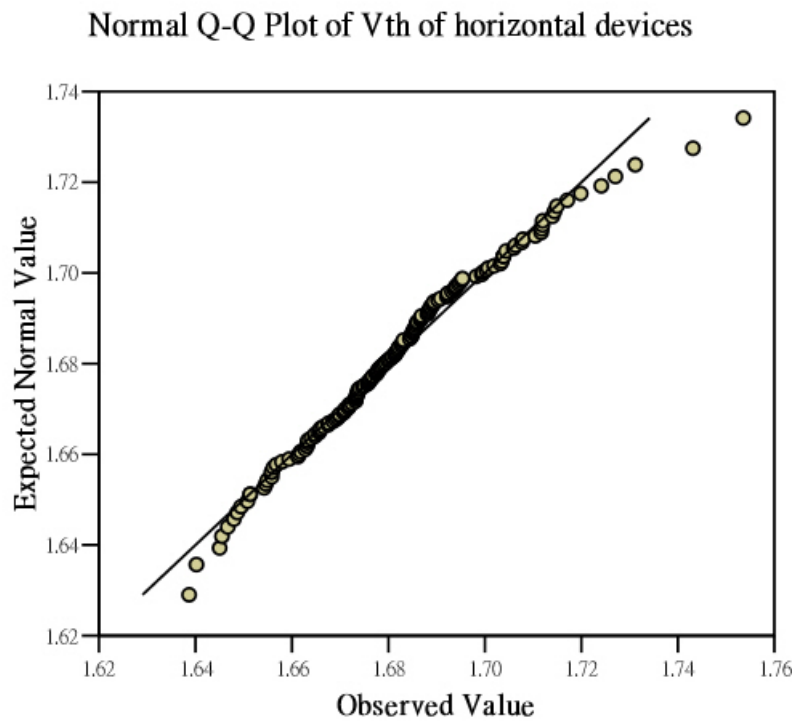
Fig. 3-1-5 The Q-Q plot of Vth of horizontal crosstie devices.

Detrended Normal Q-Q Plot of Vth of horizontal devices
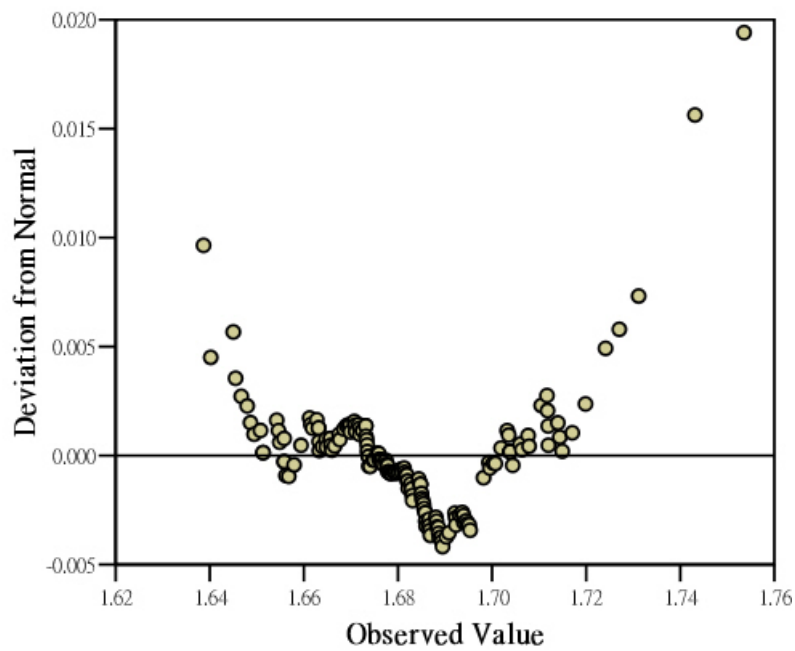
Fig. 3-1-6 The detrended Q-Q plot of Vth of horizontal crosstie devices.

Horizontal Mobility- Histogram
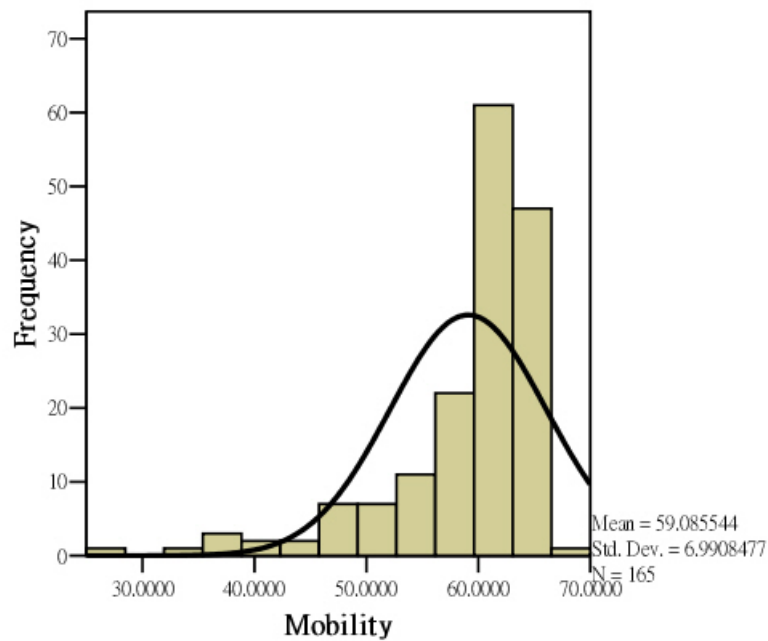
Fig. 3-1-7 The histogram of mobility of horizontal crosstie devices.

Normal Q-Q Plot of Mobility of horizontal devices
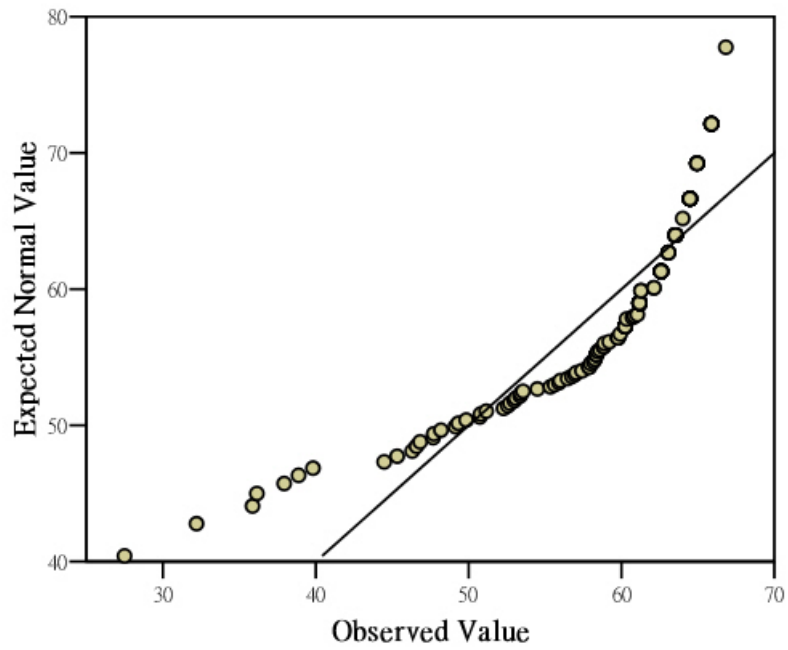
Fig. 3-1-8 The Q-Q plot of mobility of horizontal crosstie devices.

Detrended Normal Q-Q Plot of Mobility of horizontal devices
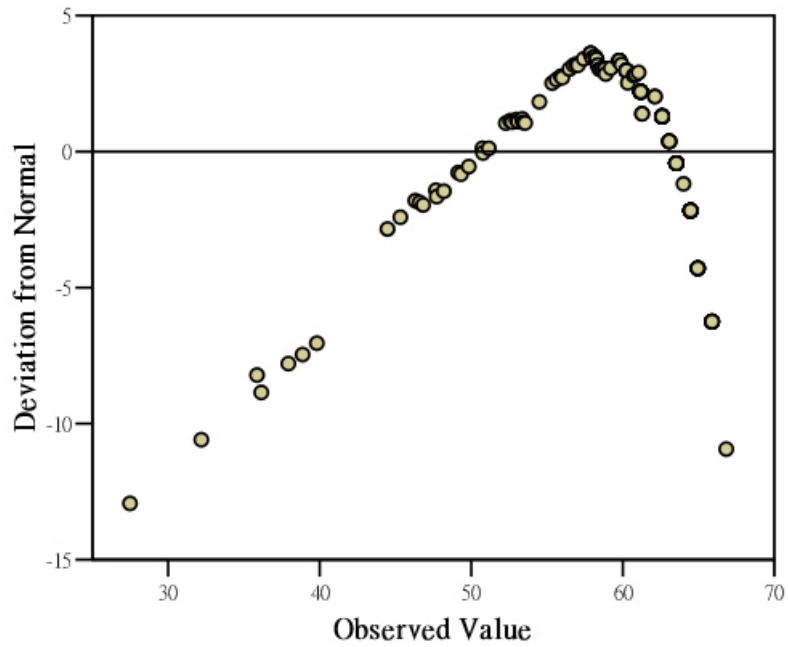
Fig. 3-1-9 The detrended Q-Q plot of mobility of horizontal crosstie devices.

Table I

Parameter values and ±3σ variations

Parameters	NTFT		PTFT	
	value	distribution	value	distribution
Vth (V)	1.5±1.5	Gaussian Normal	-1.5±1.5	Gaussian Normal
Mobility (cm^2/vs)	77.1±21	Random	85±21	Random
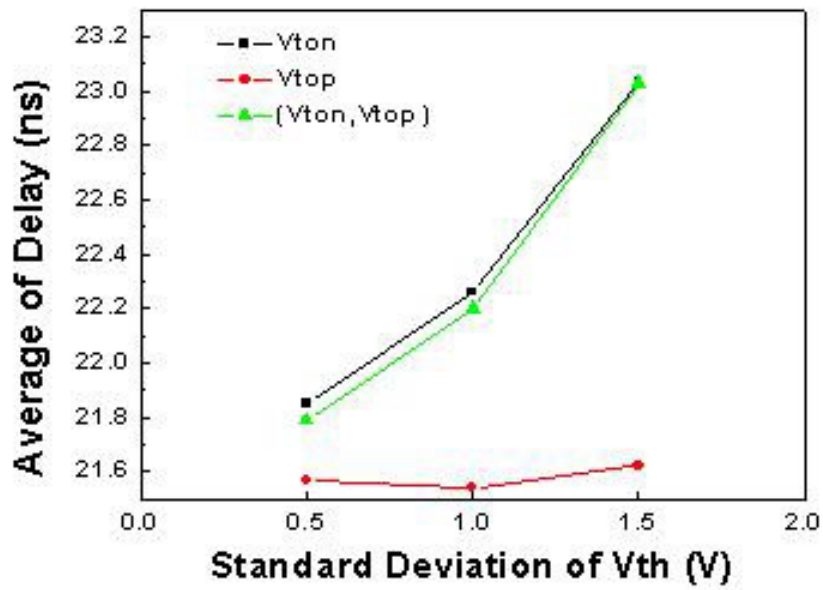
Fig. 3-2-1 Vth variation dependence on the average of delay time
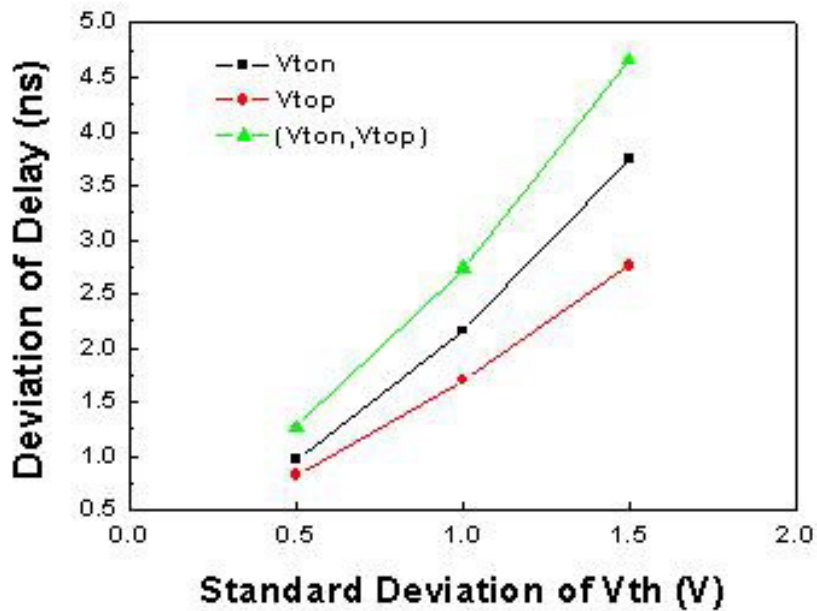
Fig. 3-2-2 Vth variation dependence on the deviation of delay time
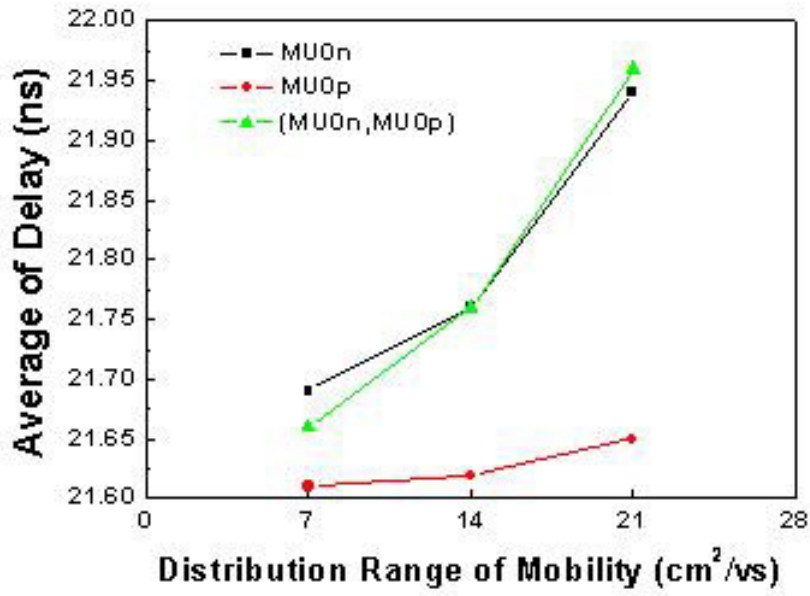
Fig. 3-2-3 Mobility variation dependence on the average of delay time
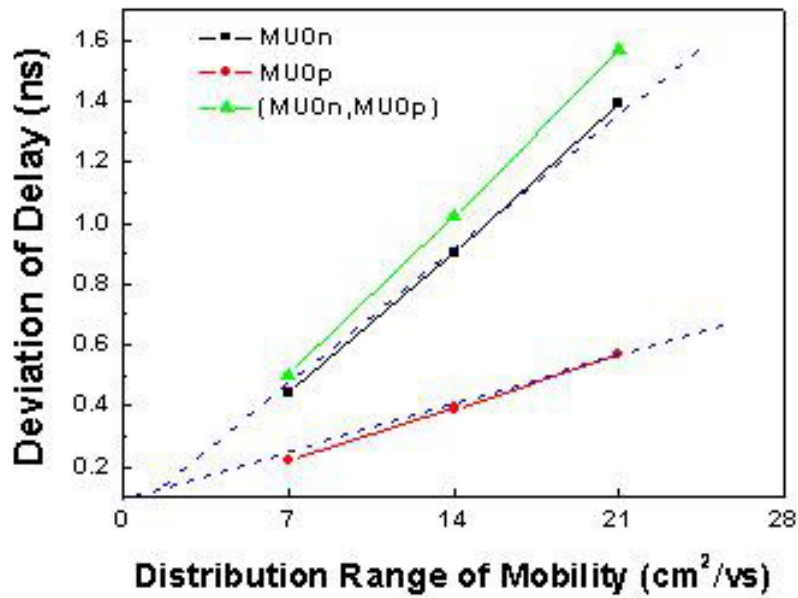
Fig. 3-2-4 Mobility variation dependence on the deviation of delay time
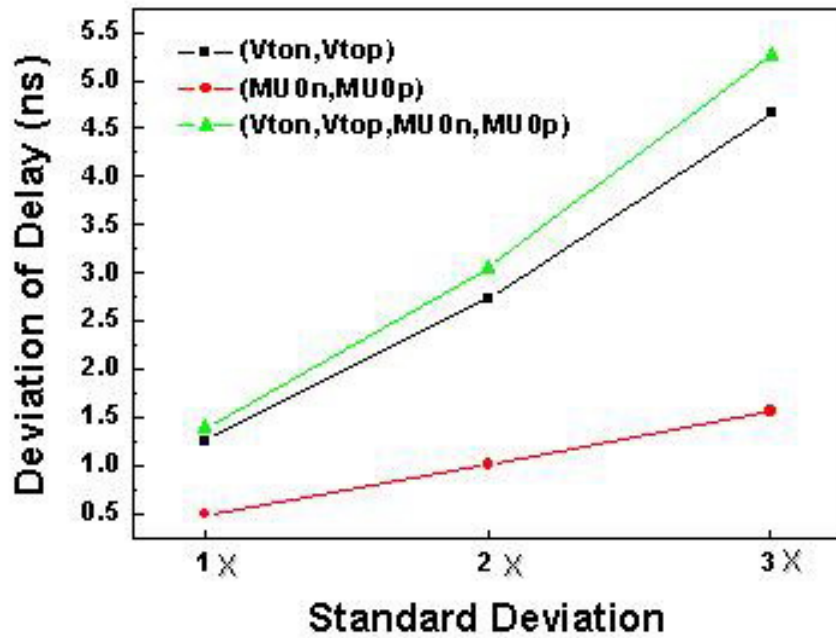
Fig. 3-2-5 Vth and mobility variations dependence on the deviation of delay time

x：0.5 V standard Deviation of Vth

7 cm2/vs distribution range of mobility
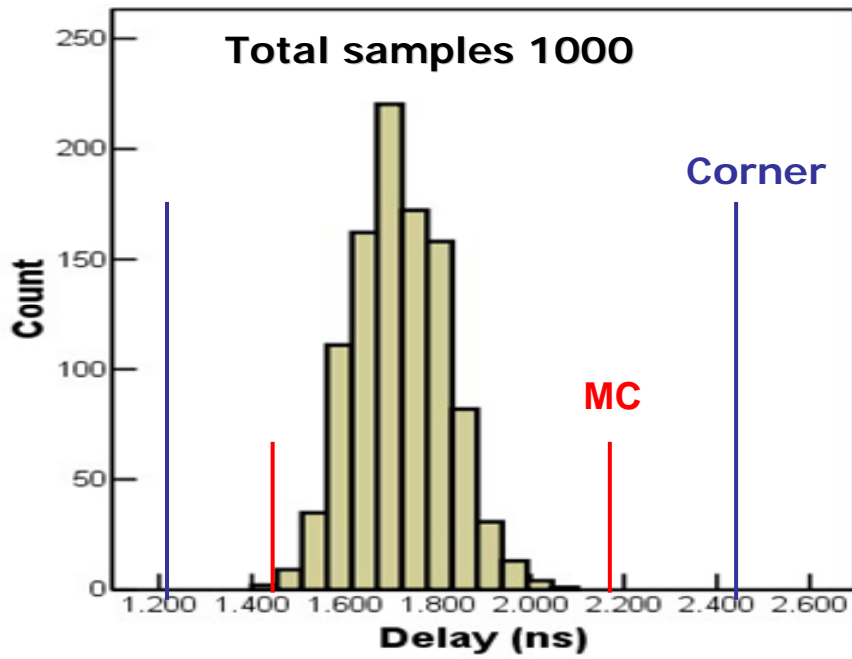
Fig. 4-1-1 Histogram of an inverter circuit carries delay and its worst-case values
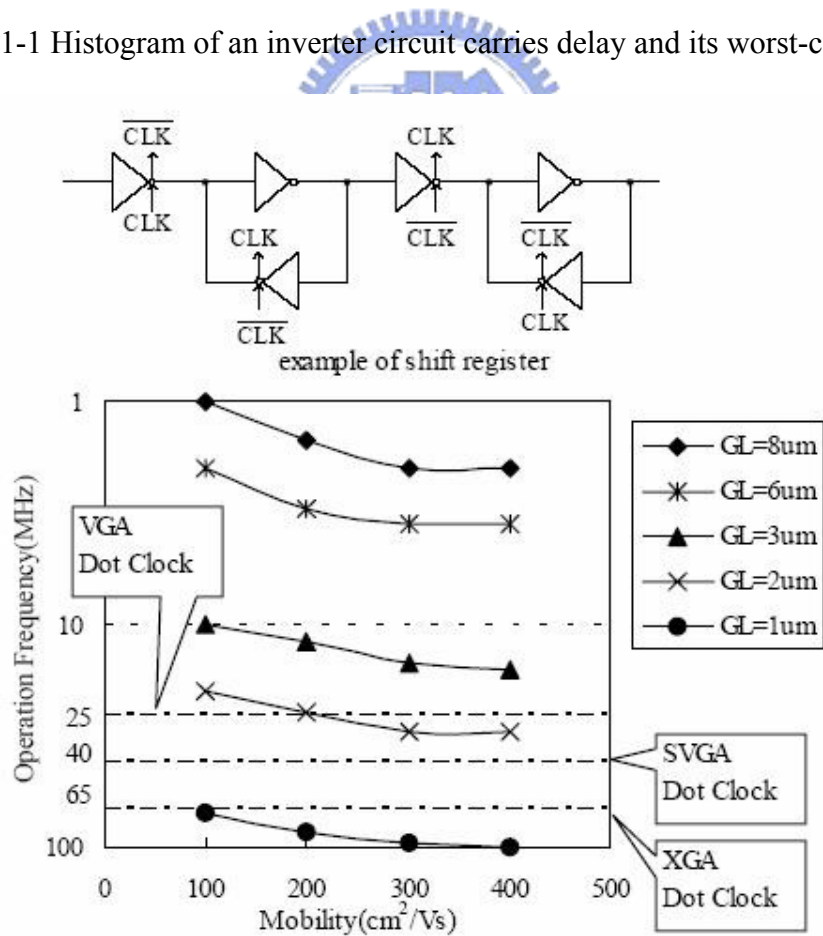
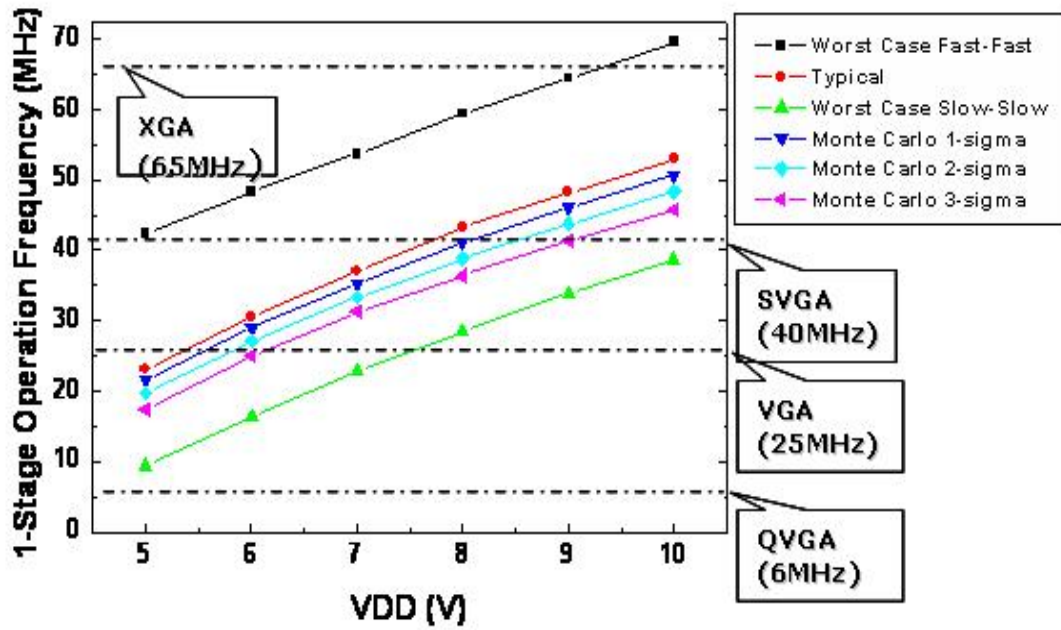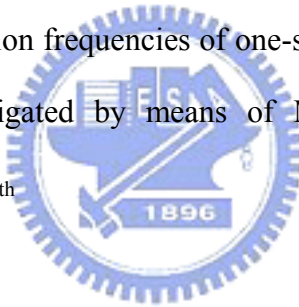Fig. 4-1-2 Result of Shift Register Simulation (VDD=3V)

Fig. 4-1-3 The trend of operation frequencies of one-stage shift register with different supply voltages were investigated by means of Monte Carlo and Worst Case simulations using Vth $\pm$ 3σ Vth
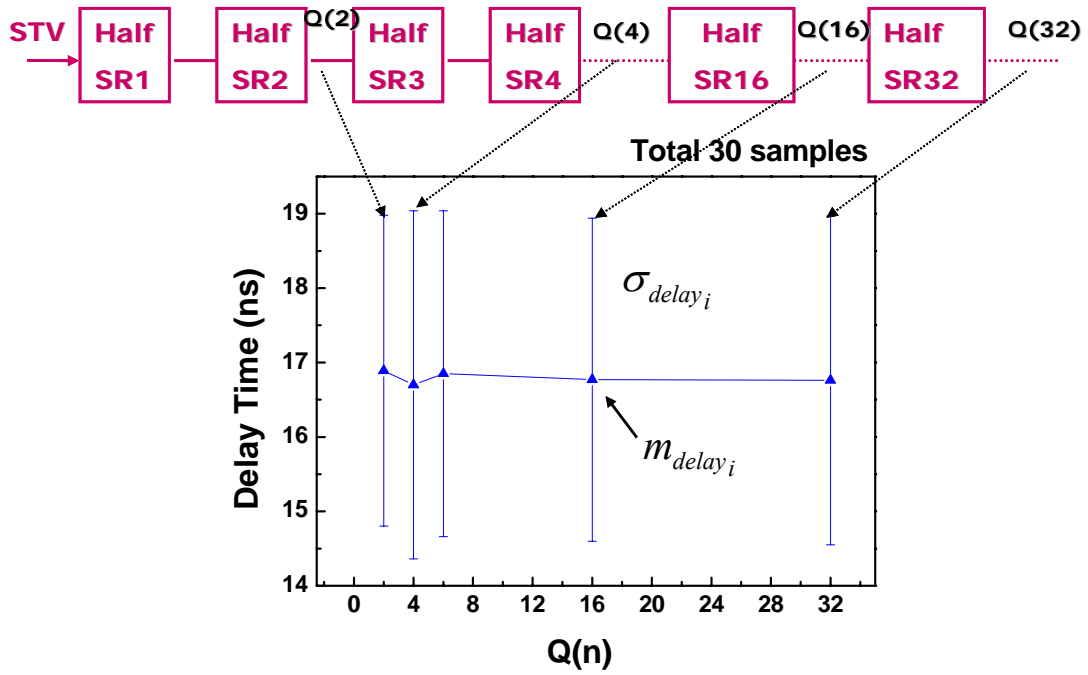
Fig. 4-1-4 The average and deviation delays of different single stages on delay time
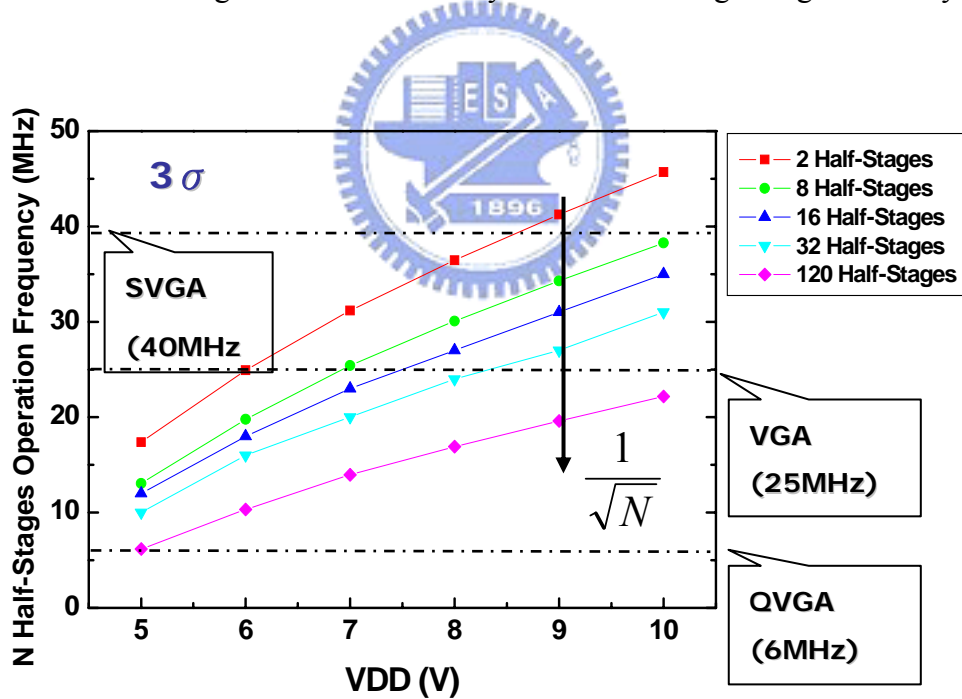

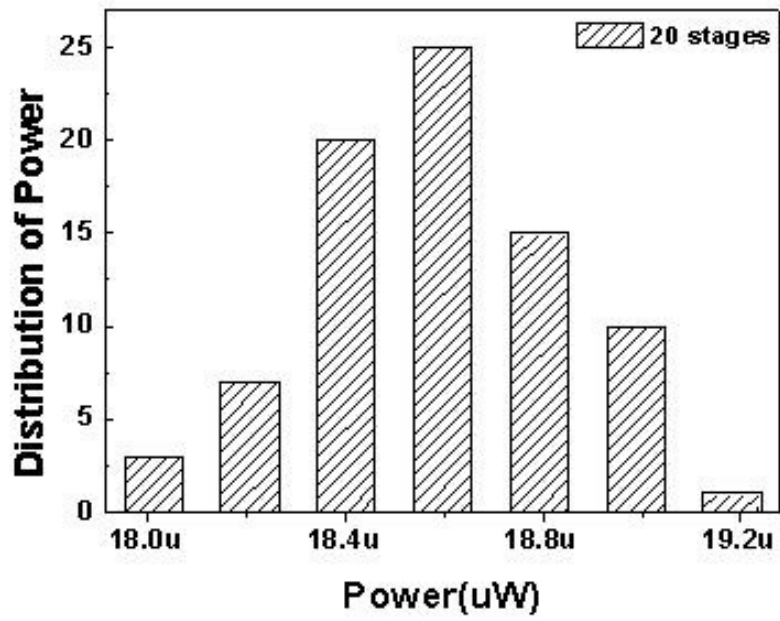Fig. 4-1-5 The trend of operation frequencies of n stage shift registers with different supply voltages

Fig. 4-1-6 The histogram of the power dissipation for the good cases

Table Ⅱ

Power Estimation for 20-stage SR Circuit

Power Distribution for the Good Cases					
	10MHz	11MHz	12MHz		Remark
PMC3	2.73	3.00	3.14	uW	3-stage Monte Carlo
	±0.09	±0.10	±0.345	uW	
Good case #	96	88	76		
PE20	18.17	20.03	20.90	uW	PMC3 x 20 / 3
	±0.23	±0.26	±0.89	uW	PMC3 x $\sqrt{20}$ / 3
PMC20	18.58	20.59	22.52	uW	20-stage Monte Carlo
	±0.25	±0.28	±0.276	uW	
Good case #	80	33	3		
ERRORavg	-2.2%	-2.7%	-7.2%		(PE20-PMC20)/PMC20
ERRORdev	-8.3%	-8.2%	223.8%		