低溫多晶矽薄膜電晶體數位電路變動性 之模擬研究

研究生: 劉宏光 指導教授: 戴亞翔博士

國立交通大學

光電工程學系光電工程研究所

摘要

複晶矽薄膜電晶體(poly-SiTFT)最近幾年在液晶顯示器(AMLCD)應用中之所 以會是眾所注目的焦點,是因為其優異的元件特性。相較於非晶矽薄膜電晶體, 複晶矽薄膜電晶體有較高電流驅動能力及較好的可靠度,因此在複晶矽薄膜電晶 體顯示器裡,它可以被用來整合畫素電路及週邊驅動電路於同一片玻璃基板上, 如此使面板結構簡單化且可以減少週邊半導體零組件的使用數量以及後段模組在 組裝時的接點數目,進而提高工程可靠度,除此之外更可降低驅動 IC 成本,維持 低耗電特性,提供高精細的畫質表現。所以,複晶矽薄膜電晶體被視為實現系統 化面板(System on Panel)的關鍵技術。然而,由於複晶矽層不規則的晶粒邊界分 佈,複晶矽薄膜電晶體有較差的均勻性,同時元件參數呈現大範圍變動。

在本篇論文,我們先描述元件的變動,並進一步研究其對於數位電路的影響以 及如何使用模擬技巧來預估電路效能的課題。本篇論文的目的為開發一個新的模 擬技巧,係利用一級移位暫存器之傳播延遲時間與功率消耗來預測 N 級操作頻率 及功率散失。

Study on the Simulation for the Variation in LTPS TFTs Digital Circuit

Student: Hung-Guang Liu

Advisor: Dr.Ya-Hsiang Tai

Department of Photonics & Institute of Electro-optical Engineering, National Chiao Tung University

Abstract

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) have recently attracted much attention in the application on the integrated peripheral circuits of active matrix liquid crystal displays (AMLCDs). The significant advantages over amorphous silicon (a-Si) TFTs are in the higher current driving capability and the better reliability. In poly-Si TFT-controlled displays, poly-Si TFTs are used to implement pixel circuits and driving circuits on a single glass substrate to reduce system cost and posses compact module. Therefore, the poly-Si TFT is the best candidate to realize system-on-panel (SoP). However, due to the irregularly distributed grain boundary, poly-Si TFTs have poor uniformity and suffer from huge variation.

In this thesis, the device variation is described. Its influences on the digital circuits and circuit simulation techniques to estimate the circuit performance are also discussed. The purpose of this thesis is to develop a new simulation skill that the operation frequency and power consumption of an n-stage shift register can be obtained through simplifying propagation delay from an n-stage one to an one-stage one.

誌 謝

在短暫的兩年研究所生涯中,感謝我能如此幸運,有一個如此完善的研究環境。首先要感謝的,便是我的指導教授戴亞翔博士。由於老師的細心引導與仔細教導,使我能在研究上獲得些成果。除此之外, 也感謝老師在待人處世以及生涯規劃上帶給我的啟發,使我受益良 多,有所成長。在這裡要先對戴老師致上誠摯的謝意。

感謝這一條研究的路上,身邊有無數優秀的研究人才相伴。同時亦 感謝學長們的鼓勵與協助,讓我在實驗上感到迷惑時能順利找到研究 的方向。感謝這兩年來和我一起奮鬥同甘共苦的夥伴們,同實驗室的 士哲、承和、承丘與彥甫,冉老師實驗室的士欽、兆仟、中良、凱傑 等同學,感謝你們花時間教導我元件物理上面的問題。

在此也要感謝實驗室貼心的學弟妹:感謝鈺函、可青、建焜、國烽、 婉萍、彥邦,感謝你們在課餘之後的適時協助。最後,我要感謝我的 家人,總是在背後默默的支持我、給予我高度的肯定並以我為傲,在 此我要向他們送上最真摯的感謝。

僅以此文獻給我的老師、家人與好友。

宏光 2005

iii

Contents

Abstract (Cl	hinese	e)	i
Abstract (Ei	nglish	ı)	ii
Acknowledg	gemen	nts	. iii
Contents			iv
Table caption	ons		. vi
Figure Capt	ions		vii
Chapter 1	Int	roduction	. 1
	1.1	Development of Displays	1
	1.2	LTPS TFTs.	2
	1.3	Integrated Circuits of System on Panel	3
	1.4	Motivation.	4
	1.5	Thesis Organization	5
Chapter 2	Sin	nulation and Analysis Methods	. 7
	2.1	Simulation Methods	7
		2-1-1 Worst-Case Method	7
		2-1-2 Monte Carlo Method	8
	2-2	RPI Model	8
	2-3	Shift Register	9
		2-3-1 Introduction	9
		2-3-2 Selection of Shift Register	10
		2-3-3 Operation of Clocked CMOS (C ² MOS) Shift Register	11

2-4	Determination of the I	Delay Time and	Operating Frequency	12
-----	------------------------	----------------	---------------------	----

Chapter 3	The	Impact	Analysis of Device Parameters	14
	3-1 Model Analysis			
		3-1-1	Derivation of Delay Time	14
		3-1-2	Distribution of Device parameters	17
	3-2	Monte	Carlo Simulation V.S. Sensitivity Analysis	19
		3-2-1	Simulation Condition	19
		3-2-2	Vth effect	20
		3-2-3	Mobility effect	21
		3-2-4	Vth and Mobility Effect	21
Chapter 4	on Skill	23		
		4-1-1	Worst Case V.S. Monte Carlo	23
		4-1-2	One-Stage Shift Register	23
		4-1-3	N-Stage Shift Register	24
	4-2	Estima	ation of Power Dissipation	27
Chapter 5	Со	onclusio	ons and Future Work	29
References				31

Figures

Table captions

Chapter 3

Table I Parameter values and $\pm 3\sigma$ variations

Chapter 4

 Table II
 Power Estimation for 20-stage SR Circuit



Figure captions

Chapter 2

Fig. 2-1-1 Probability density function for (a) a Gaussian and (b) a uniform random variable.

Fig. 2-3-1 System Block Diagram

Fig. 2-3-2 Block diagram of Timing Controller

Fig. 2-3-3 Block diagram of Data driver

Fig. 2-3-3 The master-slave D flip-flop (version 1)

Fig. 2-3-4 The original low-power D flip-flop

Fig. 2-3-5 CMOS implementation of the D-latch (version 2)

Fig. 2-3-6 Time diagram of shift register

Fig. 2-4-1 Output simulation waveforms of supply voltage 5V, at 15MHz

Fig. 2-4-2 Output simulation waveforms of supply voltage 5V, at 19MHz

Fig. 2-4-3 Monte Carlo simulation results of n-stage shift register, at 15MHz

Fig. 2-4-4 Monte Carlo simulation results of n+1-stage shift register, at 15MHz

Fig. 2-4-5 T_{dealy} consists of $T_C^2_{MOS}$ and T_{Inv}

Chapter 3

Fig. 3-1-1 The mean value and deviation of threshold voltage of different site.

Fig. 3-1-2 The mean value and deviation of mobility of different sites

Fig. 3-1-3 The relative position of the eight sites

Fig. 3-1-4 The histogram of Vth of horizontal crosstie devices.

Fig. 3-1-5 The Q-Q plot of Vth of horizontal crosstie devices.

Fig. 3-1-6 The detrended Q-Q plot of Vth of horizontal crosstie devices.

Fig. 3-1-7 The histogram of mobility of horizontal crosstie devices.

- Fig. 3-1-8 The Q-Q plot of mobility of horizontal crosstie devices.
- Fig. 3-1-9 The detrended Q-Q plot of mobility of horizontal crosstie devices.

Fig. 3-1-6 The detrended Q-Q plot of Vth of horizontal crosstie devices.

Fig. 3-1-7 The histogram of mobility of horizontal crosstie devices.

Fig. 3-1-8 The Q-Q plot of mobility of horizontal crosstie devices.

Fig. 3-1-9 The detrended Q-Q plot of mobility of horizontal crosstie devices.

Fig. 3-2-1 Vth variation dependence on the average of delay time

Fig. 3-2-2 Vth variation dependence on the deviation of delay time

Fig. 3-2-3 Mobility variation dependence on the average of delay time

Fig. 3-2-4 Mobility variation dependence on the deviation of delay time

Fig. 3-2-15 Vth and mobility variations dependence on the deviation of delay time

x : 0.5 V standard Deviation of Vth

7 cm2/vs distribution range of mobility

Chapter 4

Fig. 4-1-1 Histogram of an inverter circuit carries delay and its worst-case values

Fig. 4-1-2 Result of Shift Register Simulation (VDD=3V)

Fig. 4-1-3 The trend of operation frequencies of one stage shift register with different supply voltages were investigated by means of Monte Carlo and Worst Case simulations using Vth \pm 3 σ _{Vth}

Fig. 4-1-4 The average and deviation delays of different single stages on delay time Fig. 4-1-5 The trend of operation frequencies of n stage shift registers with different supply voltages

Fig. 4-1-6 The histogram of the power dissipation for the good cases