

# 複晶矽薄膜電晶體在高電場效應下之電性分析與模型建立

研究生：楊 凱 傑

指導教授：冉 曉 雯 教授

國立交通大學光電工程研究所

## 中文摘要

在此論文中，我們研究了多晶矽電晶體中的電流扭結現象並且建立了從漏電區，次臨界區，線性區到飽和區等一系列的模型。首先，從利用不同製程的薄膜條件和操作環境，我們發現倍增率和臨界能量與薄膜品質是強相關。因此，我們考慮缺陷的分佈來修正了臨界能量，並將它導入我們所推導出已經包含了汲極致使能障下降效應的導通區電流。至於缺陷分佈，我們乃是用計算所得與實際量測的活化能比較所得。接著，一個可以正確表達急速導通現象的物理模型被發展出。考慮缺陷相關的表面位能和寄生BJT效應，基板電壓可被正確的模擬。最後，我們將一經驗電場代入SRH產生-復合關係式中，並且考慮缺陷態之分佈，可以得到一新的漏電流模型。此模型可以大量減少人造參數並給予正確的物理概念。

# **Analysis and modeling of the high electric field effect in polycrystalline silicon TFTs**

Student: Kai Chieh Yang

Advisors: Dr. Hsiao Wen Zan

Institute of Electro-Optical Engineering National Chiao Tung University

## **Abstract**

In this thesis, we investigated the current kink phenomenon in polysilicon thin-film transistors and built a series of models from turn-off, subthreshold, linear to the saturation regime. Firstly, through utilizing the samples from different process and operation condition we find that the multiplication factor and threshold energy are strongly related to the film quality (or trap density). Therefore, we modified the threshold energy by the trap state distribution and combined it into our above threshold current model which already includes the drain induced barrier lowering effect. As to the trap state distribution was obtained from a computer minimization method that is based on field-effect conductance measurements. Secondly, a physically based numerical simulation that accurately models the abruptly switch-on behavior of n-type poly-Silicon thin-film transistor (TFT) has been developed. Considering both the trap dependent surface electrostatic potential model and the parasitic BJT effect correlated with floating body potential, the abnormal subthreshold swing at high drain bias in short channel devices can be modeled successfully. Based on this model, body voltage can be raised even by the diffusion current under lower gate bias. Finally, the new leakage current model of Poly-Si thin-film transistor had been proposed. We introduced an empirical electrical field and the defect state distribution in the traditional leakage current model which is based on SRH generation-recombination model. This model could reduce fitting parameters dramatically and enhance the insight of physics.

## Acknowledgment

研究所這二年走下來雖然辛苦，可是當結束畢業口試那一剎那，回想這些日子來所學到的東西與成長，突然心中揚起來一股無以名之的喜悅，這一路走來總覺得自己是幸運的，在人生的路上有兩位開明的父母，允許我自由的做任何我想做的事，也很高興遇到一位很棒的老師，冉曉雯老師讓我了解到，必須將自己的眼光再放遠一點，未來的路才能走得長久，且在我遇到困難的時候能適時的給予幫助，使論文進度不致停頓。同時也遇到一群好伙伴，清大的世青學長在實驗與理論上都給了我很大的啟發與幫助，以及實驗室的國錫學長對研究的熱情與專業令人敬佩，當然還有一群陪我一同奮鬥的同學們兆仟、士欽、中良、銘龍、德章、政偉和士強，有了你們友情的陪伴，使我在研究的路上不是孤獨的一個人;幸運的，因為有了你們大家，我才能在這生命舞台一直盡情地揮灑自己，演出最好的一面。



# Contents

<b>Chinese Abstract</b>	I
<b>English Abstract</b>	II
<b>Acknowledgment</b>	III
<b>Contents</b>	IV
<b>Figure Captions</b>	VI
<b>Table Captions</b>	X
<b>Chapter 1. Introduction</b>	
1.1 Background	1
1.2 Overview of fabrication method for polycrystalline silicon film	2
1.3 Carrier transport mechanisms at high field in poly-Si TFTs	5
1.4 Organization of this thesis	7
<b>Chapter 2. Analysis of Kink Effect in Poly-Si TFT's</b>	
2.1 Some possible kink effect related mechanisms	9
2.2 Device structure and fabrication process	11
2.3 Typical output characteristics	13
2.3.1 Parameters extraction	14
2.3.2 Different re-crystallized methods	14
2.3.3 Different hydrogen-passivation time	15
2.3.4 Operation at different temperatures	16
<b>Chapter 3. Characterization and Modeling of Impact Ionization Effect in Poly-Si TFTs</b>	
3.1 Derivation of DIGBL current model	17
3.2 Determination of density of state in the band gap	21
3.3 The modified threshold energy	23
3.4 Impact ionization model	26
3.5 Result and discussion	29
<b>Chapter 4. A Physically-Based Subthreshold Model of Poly-Silicon Thin-Film</b>	

<b>Transistors with Parasitic BJT Effect</b>		
4.1	Introduction	30
4.2	Model derivation	30
4.2.1	Parasitic BJT model	31
4.2.2	Impact-Ionization factor derivation	33
4.2.3	Surface electrostatic potential model	34
4.3	Result and discussion	35
4.4	Conclusion	36
<b>Chapter 5. A New Empirical Leakage Current Model of Poly-Si Thin-Film Transistors</b>		
5.1	Introduction	38
5.2	Physical model	39
5.3	Result and discussion	42
5.4	Conclusion	44
<b>Chapter 6.</b>	<b>Conclusions</b>	45
<b>References</b>		47
<b>Figures</b>		53~90



# Figure Captions

## Chapter 2

- Fig. 2-1-1. The punch-through effect would become more obvious as the gate length shrinks to  $0.5\mu\text{m}$ .
- Fig. 2-1-2. The drain induced barrier lowering effect with different gate lengths and drain bias.
- Fig. 2-1-3. The charge sharing effect would pronounce only at small device dimension.
- Fig. 2-1-4. The floating body effect in TFTs.
- Fig. 2-2-1. The top-view of the device which is used in our study.
- Fig. 2-2-2. Schematic cross-sectional view of devices with conventional top-gate structure.
- Fig. 2-2-3. The SEM picture of as-deposited poly-silicon film.
- Fig. 2-2-4. The SEM picture of SPC poly-silicon film.
- Fig. 2-3-1. Each saturation voltage at various gate voltages can be defined from the “first” minimum points of the conductance.
- Fig. 2-3-2. The kink current  $I_{\text{KINK}}$  can be evaluated by using the drain current at high drain voltage to minus the saturation current, such that  $I_{\text{KINK}} = I_{\text{DS}} - I_{\text{D,SAT}}$ .
- Fig. 2-3-3.  $I_{\text{D}}-V_{\text{D}}$  characteristics for as-deposit. and two hours  $\text{NH}_3$ -passivation time n-channel poly-Si TFTs with various channel lengths: (a)  $L = 10\mu\text{m}$ , (b)  $L = 5\mu\text{m}$  (c)  $L = 2\mu\text{m}$ . The channel width  $W$  is kept as  $10\mu\text{m}$ .
- Fig. 2-3-4.  $I_{\text{D}}-V_{\text{D}}$  characteristics for SPC and two hours  $\text{NH}_3$ -passivation time n-channel poly-Si TFTs with various channel lengths: (a)  $L = 10\mu\text{m}$ , (b)  $L = 5\mu\text{m}$  (c)  $L = 2\mu\text{m}$ . The channel width  $W$  is kept as  $10\mu\text{m}$ .
- Fig. 2-3-5.  $I_{\text{D}}-V_{\text{D}}$  characteristics for ELA n-channel poly-Si TFTs with various channel lengths: (a)  $L = 13.5\mu\text{m}$  (b)  $L = 4.5\mu\text{m}$  (c)  $L = 3.5\mu\text{m}$ . The channel width  $W$  is kept as  $12\mu\text{m}$ .
- Fig. 2-3-6. (a) The extracted excess kink current versus the gate voltage with different drain voltage. As-deposited, 2hr  $\text{NH}_3$ -passivation time and  $W/L = 10/10$  ( $\mu\text{m}$ ). (b) The multiplication factor versus the gate voltage with different drain voltage. As-deposited, 2hr  $\text{NH}_3$ -passivation time and  $W/L = 10/10$  ( $\mu\text{m}$ ).
- Fig. 2-3-7. (a) The extracted excess kink current versus the gate voltage with different drain voltage. SPC, 2hr  $\text{NH}_3$ -passivation time and  $W/L = 10/10$  ( $\mu\text{m}$ ). (b) The multiplication factor versus the gate voltage with different drain voltage. SPC, 2hr  $\text{NH}_3$ -passivation time and  $W/L = 10/10$  ( $\mu\text{m}$ ).

- Fig. 2-3-8. (a) The extracted excess kink current versus the gate voltage with different drain voltage. ELA, 2hr NH<sub>3</sub>-passivation time and W/L = 13.5/12 (μm). (b) The multiplication factor versus the gate voltage with different drain voltage. ELA, 2hr NH<sub>3</sub>-passivation time and W/L = 13.5/12 (μm).
- Fig. 2-3-9. (a) Threshold energy extracted figure form empirical ionization rate. As-deposited, 2hr NH<sub>3</sub>-passivation time and W/L = 10/10 (μm). (b) Threshold energy extracted figure form empirical ionization rate. SPC, 2hr NH<sub>3</sub>-passivation time and W/L = 10/10 (μm). (c) Threshold energy extracted figure form empirical ionization rate. ELA, 2hr NH<sub>3</sub>-passivation time and W/L = 13.5/12 (μm).
- Fig. 2-3-10. Multiplication factor for n-channel poly-Si TFTs with different film re-crystallized process. The channel length and width are both 5μm.
- Fig. 2-3-11. Threshold energy for n-channel poly-Si TFTs with different film re-crystallized process.
- Fig. 2-3-12. Multiplication factor versus gate voltage with different NH<sub>3</sub>-passivation time. SPC and the channel length is 5μm and width is 10μm.
- Fig. 2-3-13. Threshold energy versus gate voltage with different NH<sub>3</sub>-passivation time. SPC and the channel length is 5μm and width is 10μm.
- Fig. 2-3-14. Multiplication factor vs. gate voltage under different ambient temperature. SPC, 2hr NH<sub>3</sub>-passivation, and channel length and width are both 10μm.
- Fig. 2-3-15. Threshold energy vs. gate voltage under different ambient temperatures. SPC, 2hr NH<sub>3</sub>-passivation, and channel length and width are both 10μm.

## Chapter 3

- Fig. 3-0-1. The model derivation flow.
- Fig. 3-1-1. The relationship between saturation voltage and the square root of saturation current is traced on one straight line means that the saturation point occurs due to the conduction channel collapses.
- Fig. 3-1-2. The saturation voltage  $V_{D,SAT}$  and  $V_G - V_{TH}$  versus the gate voltage  $V_G$ .
- Fig. 3-1-3. The threshold voltage increases with increasing trap density and decreasing grain size.
- Fig. 3-1-4. Calculated potential barrier height which involves the drain induced barrier lowering effect.
- Fig. 3-2-1. The band bending along the x axis at the SiO<sub>2</sub> and polysilicon interface.
- Fig. 3-2-2. The process flow of finding the surface potential.
- Fig. 3-2-3. Dependence of  $IT^{-1}$  on temperature.

Fig. 3-2-4. The solid line is the best fit of the experimental data with the theory for the bulk and interface states distribution parameters.

Fig. 3-2-5. Energy distribution of bulk states of the SPC and 2hr NH<sub>3</sub>-passivation time undoped polysilicon TFT.

Fig. 3-3-1. (a) A high energy entering electron hits the neutral trap which is above the quasi-Fermi level and subsequently generated an electron-hole pair. (b) A high energy entering electron hits the negative charged trap which is under the quasi-Fermi level and subsequently “lift” this electron to the conduction band edge.

Fig. 3-5-1. Comparison between measured and calculated I<sub>D</sub>-V<sub>DS</sub> characteristics for n-channel poly-Si TFT's with W/L=10μm /10μm.

Fig. 3-5-2. Comparison between conventional threshold energy(1.68eV) and our simulated threshold energy for n-channel poly-Si TFT's with W/L=10μm /10μm

## Chapter 4

Fig. 4-2-1. Cross-section of the partially-depleted TFT NMOS device.

Fig. 4-3-1. Plots of (a)I<sub>sub</sub>, I<sub>c</sub>, I<sub>hm</sub>, and M<sub>m</sub> - 1 at V<sub>ds</sub> at 5 V for W/L = 10/6μm and (b)I<sub>sub</sub>, I<sub>c</sub>, I<sub>hm</sub>, and M<sub>m</sub> - 1 at V<sub>ds</sub> at 2.5 V for W/L = 10/1.5μm.

Fig. 4-3-2. Plots of (a)I<sub>c</sub>, I<sub>hb</sub>, and M<sub>b</sub> - 1 at V<sub>ds</sub> at 5 V for W/L = 10/6μm and (b)I<sub>c</sub>, I<sub>hb</sub>, and M<sub>b</sub> - 1 at V<sub>ds</sub> at 2.5 V for W/L = 10/1.5μm.

Fig. 4-3-3. (a)The body potential vs drain voltage on the simulation model for various gate voltage for W/L = 10/6μm (b)The body potential vs drain voltage on the simulation model for various gate voltage for W/L = 10/1.5μm.

Fig. 4-3-4. The relation of transport factor and trap density for various channel length.

## Chapter 5

Fig. 5-2-1. Schematic energy band diagram of the near the drain side.

Fig. 5-2-2. The electrical field in the depletion region.

Fig. 5-3-1. The relationship between the V<sub>DS</sub> and enhance factors, under constant V<sub>G</sub> = -4V, W/L = 6/12(μm).

Fig. 5-3-2. The relationship between the V<sub>G</sub> and enhance factors, under constant V<sub>DS</sub> = 5.1V, W/L = 6/12(μm).

Fig. 5-3-3. Leakage current versus gate voltage (at V<sub>D</sub> = 5V) for different values of parameter  $\alpha$  for our model.



Fig. 5-3-4. Leakage current versus gate voltage (at  $V_{DS} = 5V$ ) for different values of parameter  $\beta$  for our model.

Fig. 5-3-5. The relationship between the trap position of donor-like trap in the energy gap and enhancement factors.

Fig. 5-3-6. The relationship between the trap position of acceptor-like trap in the energy gap and enhancement factors.

Fig. 5-3-7. Fitting result.  $W/L = 6/6$  ( $\mu m$ ) and the drain voltage  $V_{DS}$  is varied from 4 to 5 V.



# Table Captions

Table 3-2-1. Parameters of the bulk state distribution of the SPC and 2hr  $\text{NH}_3$ -passivation polysilicon TFTs.

Table 3-5-1. The parameters set that is used in our numerical model.

