Chapter 1

Introduction

1-1 Background

In 1966, the first polycrystalline silicon thin-film transistors (poly-Si TFT's) were fabricated by Fa et al. [1]. Since then, many research reports have been proposed to study their conduction mechanisms, fabrication processes and device structures to improve the performance, In 1970s, the conduction mechanism and the electrical prosperities of polysilicon films, which are determined by the prosperities of grain-boundaries, were clarified [2], [3]. In 1983, the first practical application of poly-Si TFT's to liquid-crystal displays (LCDs) was announced for full-color pocket TVs [4], and then commercialized in 1984 as the world's first. To date, poly-Si TFT's have been expanding in applications to linear image sensors [5], thermal printer heads [6], liquid-crystal shutter arrays for printers [7], photodetector amplifier [8], high-density static random access memories (SRAMs) [9], [10], nonvolatile memories [11], [12], and active-matrix LCDs (AMLCDs) [13-16], etc.

Recently, poly-Si TFTs have been applied to 16MB SRAMs as load elements and are indispensable in 64MB and higher density SRAMs [17]. One of the reasons for this is that the conventional resistor loads can’t provide adequate performance under the constraints imposed by scaling down devices. Contrast to the drawback of resistor loads on SRAMs, poly-Si TFTs can provide many advantages, such as its small cell area, low standby power dissipation, improved cell stability, and high soft-error immunity [18].

Over the past twenty years, the most interesting application of poly-Si TFTs is

AMLCDs, although the present first generation of AMLCDs relies predominantly upon hydrogenated amorphous silicon (a-Si:H) TFTs for the pixel switching devices. A-Si:H film exhibits high OFF-state resistivity which can reduce the leakage current of TFTs. Unfortunately, the extremely low field-effect mobility (typically below 1 cm^2/V-sec) in a-Si:H TFTs limits the technology from being developed to form integrated drive circuits on the active matrix plate. On the contrary, there are many advantages for using poly-Si TFTs to replace a-Si:H TFTs, such as the superior carrier mobility, CMOS capability, lower photocurrent, and better device reliability [19], [20]. Higher field-effect mobility implies higher drive current. The higher drive current allows small-geometry TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Therefore, the superior field-effect mobility achievable with poly-Si TFTs is seen to be essential for the successful integration of row and column drive circuits on the active panel [21]. At the same time, in order to achieve the System-On-Panel (SOP) and computer-aided circuit design, it is very important to successfully predict the electrical properties of poly-Si TFTs.

1.2 Overview of Fabrication Method for Poly-Silicon Thin Film Transistors

Crystallization of a-Si thin film is the most important process in the fabrication of TFTs. The quality of crystallized poly-Si thin film affects the preference of the TFTs. Enlarge grain size can promote the quality of poly-Si since most defects are generated in the grain boundary.

Various kinds of technology have been proposed for a-Si crystallization. In the

section, we some roughly review on this key process.

1.2.1 As-deposited Method

The low-pressure chemical vapor deposition (LPCVD) is the most conventional method to fabricate poly-Si film. However, this method have some disadvantages such as high deposition temperature (over 600℃), small grain size (< 50nm), poor crystallization, large amount of hydrogen and high grain boundary density states. These properties make it impossible to run the low-temperature processes on a cheap large-area glass substrate. Besides, Plasma enhance chemical vapor deposition (PECVD) can be fabricated poly-silicon film by using $SiF_4/SiH_4/H_2/He$ mixture gas at below 450℃ availably.

1.2.2 Solid Phase Crystallization

SPC has better performance than the as-deposited method in increasing the grain size since enough energy is applied to amorphous silicon atoms by thermal annealing to rearrange silicon atoms regularly. This process start when Si atom with sufficient energy overcome the interfacial free energy associated with the formation of critical sized crystalline nuclei and atomic mobility to the point which the transformation took place at a reasonable rate. The nucleation mechanism is homogeneous. There are many nucleation sites in a-Si film and each site grows individually. This phenomenon limits the grain size. However, SPC method also has some drawbacks. First, the thermal annealing temperature is still high (more than 600℃). Second, the annealing time is more than 24 hours. Third, the poly-silicon film contains many defects. The high processing temperature limits the application of glass substrate. In addition, the defects also affect the characteristics of poly-silicon TFT.

1.2.3 Rapidly Thermal Annealing

The RTA based on the principle of repeatedly exposing a substrate to short heating-cooling cycles. The heating time in each cycle is very short (1 sec) and the cooling time is longer. Turichich et al [1] observed that glass with a strain temperature of 630℃ can be exposed to 740℃ for 1 to 2 second with minimum deformation. Therefore, it is possible to adjust the heating and cooling parameters of a RTA process to minimize glass deformation and expose it to a high temperature for a short period of time at the same time. Poly-Si with small grain and some amorphous phase silicon is obtained with this method.

1.2.4 Metal Induced Crystallization

In 1963, Wagner and Ellis [2] discovered that the addition of small amounts of metallic impurities could drastically decrease the thermal budget for the transformation of a-Si to poly-silicon, namely "metal induced crystallization". Various kinds of metals have been studied and they could be classified to two schemes. One is eutectic-forming metal such as Ag [3], [4], Au [5], Al [6-8]. The other is silicide-forming metals such as Pd [9], [10] and Ni [3~12]. The metal, such as Ni and Pd, on the a-Si film diffuses and forms a crystalline metal silicide which acts as a heterogeneous nucleation site for Si crystallization. Eutectic-forming metal, such as Ag, Au and Al, diffuses and increases Si atomic mobility by forming interstitials which changes the Si-Si bonding nature form covalent to metallic or forming low-temperature eutectic or metal stable silicide compound which undergoes crystallization at low-temperature than a-si. Among the MIC process, a thin metal (such as Ni, Pd, Al) is deposited on the a-Si surface and crystallizes at temperature lower than 600℃. These metal layers are generally deposited with physical vapor deposition (PVD). These methods could regrowth the grain to larger. This technique can also reduce the annealing temperature and time. But the annealing time is still

longer than 8 hours. The long annealing time reduces the throughput of poly-silicon TFT. In addition, the metal contamination was an important problem. The metal contaminations degrade the electrical characteristic.

1.2.5 Excimer Laser annealing

A presently widely used method to crystallize a-Si is laser crystallization. Laser crystallization is faster than SPC or MIC and generates larger grain size with lower dislocation density. The basic principle is the transformation from crystalline silicon by melting the silicon at short time. Poly-Si with large grains results from the subsequent solidification. But laser crystallization isn't a low temperature process as the silicon was heated above 1200oC. However, high temperature sustains for very short time which doesn't damage substrate severely. Laser crystallization of a-Si can be performed with varieties of lasers and different technology. Excimer laser crystallization (ELC) is by far the mostly used method [13]. Generally speaking, there are three kinds of excimer laser using in this area, such as ArF (193 nm), KrF (248nm), XeCl (308nm). The combination of strong optical absorption of the UV light in silicon (α>106cm-1) and small heat diffusion length during the laser pulse (~100nm) imply that high temperature can be produced in the silicon surface region. The high temperature causes melting without huge heat on the substrate. This makes the ELA-process be compatible with glass substrate. However, the excimer laser energy is Gauss distribution. It means that the laser energy density is not uniform.

1.3 Carrier Transport Mechanisms in poly-Si TFTs

In the past the carrier transport through the grain boundaries has investigated extensively. The grain boundary barrier was treated as a Schottky barrier and the thermionic emission of carriers over the barrier was considered which were based on

carrier trapping model. Mandurah regarded this additional barrier as to result from the energy band discontinuity between the grain and grain-boundary material treating the latter as an intrinsic, wider band-gap semiconductor. In the model of Lu, the additional barrier was called scattering potential to represent overall scattering effects in the grain boundaries. The asymmetry of space charge barrier around the grain boundary due to the applied bias was considered in the model of Mandurah while Lu assumed symmetric space charge barrier. Subsequently, the derivation of drain induced grain barrier lowering (DIGBL) has been considered into the I-V characteristics of polysilicon thin film transistors by Lin.

As the poly-Si TFT's are operated at high drain bias the output characteristics show an anomalous drain current increase or an increase of the output conductance, we called this phenomenon the "kink effect". This effect has been investigated extensively in single-crystal MOSFET's or silicon-on-insulator (SOI) devices. In general, the kink effect involves many different physical mechanisms, such as (i) punch-through, (ii) drain induced barrier lowering (DIBL), (iii) charge sharing effect, (iv) channel length modulation, (v) impact ionization or avalanche induced breakdown, (vi) body effect induced threshold voltage roll off, and (vii) parasitic BJT effect. Furthermore, for polycrystalline silicon thin-film transistors, because of the presence of grain boundary, (viii) drain induced grain barrier lowering (DIGBL) are another possible mechanisms in poly-Si TFTs which can increase the output conductance when the device is operating in saturation. Drain induced grain barrier lowering effect is a unique characteristic in polycrystalline silicon films. As a large bias drops across a grain boundary, the asymmetry of potential distribution around the grain boundary will be destroyed. The difference barrier height between two sides of the grain boundary can lead to an additional thermionic emission current. Exact current-voltage model of poly-Si TFTs can not be obtained without taking into

account the DIGBL effect.

1.4 Organization of Thesis

The high driving current as well as the high mobility is the reasons to use the poly-Si TFTs instead of the amorphous TFTs. Furthermore, as the channel length shrink to the size which is comparable to the grain size, the performance of TFTs are improved obviously. Yet, the physical mechanisms pertinent to high electric-field conduction in polycrystalline silicon thin-film transistors are not well understood at present.

In this thesis, we concentrate our effort on predicting the high electric-field of poly-Si TFTs. Here, it should be declared that chapter 4 and 5 were developed before chapter 2 and 3 and had been published The impaction ionization mechanism in chapter 4 and the trap density of state distribution in chapter 5 are not the same as its counterparts used in chapter 3. These non-coincidences must be modified in the future. Chapter 1 describes the background of the motivation on developing polysilicon TFT's, the different useful re-crystallized fabrication of the grain enhanced polycrystalline films, and the development of the model of poly-Si films and thin-film transistors to date.

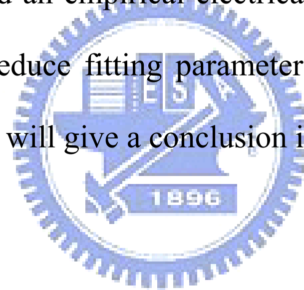
In Chapter 2, kink effect and several relative short channel mechanisms are discussed. And we investigate the kink effect with the condition of samples which split to different re-crystallized process, various hydrogen-passivation time and operating at different temperature and illumination frequency.

In Chapter 3, we propose our semi-empirical numerical drain induced barrier lowering current and the impact ionization model which involves the modified trap

relative threshold energy. A good agreement is found after comparing the simulation results with the experiments. We also describe some factors which could influence the impact ionization induced kink current.

In Chapter 4, a physically based numerical simulation that accurately models the abruptly switch-on behavior of n-type poly-Silicon thin film transistor (TFT) has been developed. Considering both the trap dependent surface electrostatic potential model and the parasitic BJT effect correlated with floating body potential, the abnormal subthreshold swing at high drain bias in short channel devices can be modeled successfully.

In Chapter 5, the new leakage current model of Poly-Si thin film transistor had been proposed. We introduced an empirical electrical field in the traditional leakage current model which could reduce fitting parameters dramatically and enhance the insight of physics. Finally, we will give a conclusion in Chapter 6.



Chapter 2

Analysis of Kink Effect in Poly-Si TFT's

2.1 Some possible kink effect related mechanisms

As the poly-Si TFT's are operated at high drain bias the output characteristics show an anomalous drain current increase or an increase of the output conductance, we called this phenomenon the "kink effect". This effect has been investigated extensively in single-crystal MOSFET's or silicon-on-insulator (SOI) devices. In general, the kink effect involves many different physical mechanisms, such as (i) punch-through [1~5], (ii) drain induced barrier lowering (DIBL) [6~9], (iii) charge sharing effect [10-11], (iv) channel length modulation, (v) impact ionization or avalanche induced breakdown, (vi) body effect induced threshold voltage roll off, and (vii) parasitic BJT effect. Furthermore, for polycrystalline silicon thin-film transistors, because of the presence of grain boundary, (viii) drain induced grain barrier lowering (DIGBL) are another possible mechanisms in poly-Si TFTs which can increase the output conductance when the device is operating in saturation.

We would describe these physical mechanisms briefly as follows. (i) If the device has short channel length and operates at high drain voltage, the sum of the drain and source space charge regions is larger than the channel length. Therefore, the depletion region of the drain junction has punched through to the depletion region of the source junction. Under such a condition, majority carriers in the source region can be injected into the depleted channel region, where they will be swept by the field and collected at the drain. The equipotential lines in the channel spread deep into the bulk semiconductor, indicating a punch-through effect, see Fig. 2-1-1 [12]. (ii) As the channel length is reduced, the surface potential barrier is reduced results from the

serve band bending from the drain side, as illustrated in Fig. 2-1-2 [13]. Thus, the current increases with the barrier decreases by an exponential dependence. This process is so called DIBL effect. (iii) The field lines terminating on the space charges in the depletion region are either from the gate or source and drain. For the long channel device, those field lines originated form the source (or drain) are negligible compared to the field lines from the gate. But in short channel devices, those parallel fields are not negligible and should modify the bulk space charge according as the shape of device. This charge sharing effect is illustrated in Fig. 2-1-3 [13]. (iv) When the MOSFET operates in saturation region, the effective channel length will decrease as a result of the depletion region in the drain side will laterally extend into the channel region. Thus, lead an increase of the output conductance with the drain bias increases. (v) At sufficiently high field, an electron in the conduction band can gain enough energy to lift an electron from the valence band or trap state into the conduction band, thus generating one free electron in the conduction band and one free hole in the valence band. This process is known as impact ionization. If the field is high enough, these secondary electrons and holes can themselves cause further impact ionization, thus beginning a process of carrier multiplication in the high-field region. (vi)(vii) As depicted in Fig. 2-1-4, the floating body region acts as a parasitic BJT to further enhance the kink. Specifically, holes generated by impact ionization effect accumulate at body neutral regions. The body potential is therefore raised and forward biases the body-source junction. When the voltage drop across the body-source junction is large enough, the parasitic BJT will be turned on and a positive feedback latch-up will be formed. (viii) Drain induced grain barrier lowering effect is a unique characteristic in polycrystalline silicon films. As a large bias drops across a grain boundary, the asymmetry of potential distribution around the grain boundary will be destroyed. The difference barrier height between two sides of the

grain boundary can lead to an additional thermionic emission current. Exact current-voltage model of poly-Si TFTs can not be obtained without taking into account the DIGBL effect.

In order to separate these various physical mechanisms, we should first focus our attention on the device with a moderate channel length (L > 4 or 5μm) to avoid the mechanisms that only presents in short channel. The effects (i)~(iv) are believed to dominate the device characteristic only if channel length shrinks to about 1μm [14]. We assumed that the floating body effect can be neglected in polycrystalline silicon thin film transistors if channel length is longer enough [15]. Consequently, we leave the impact ionization effect and the drain induced grain barrier lowering as the only possible mechanisms of the kink effect of poly-Si TFTs. However, attributed to the presence of trap states in poly-Si films, it is so complicate to analyze the impact ionization effect without removing the DIGBL effect. So in the last section of this chapter, we would specifically derivate the reasonable current-voltage model which contains the DIGBL effect. The detailed analysis and modeling of impact ionization had been obtained in the next chapter following by eliminating the DIGBL effect in the excess kink current.

2.2 Device structure and fabrication process

In this experiment, we fabricate the poly-Si TFTs with typical self-aligned structure. The top view of the devices is shown in Fig. 2-2-1 and the schematic cross sectional view of devices with conventional top-gate structure is shown in. Fig. 2-2-2. The fabrication procedure is described as follows.

Step1. Substrate.

100mm p-type single crystal silicon wafers with (100) orientation were used as

the starting materials. After an RCA initial cleaning procedure. Si wafers were coated with 550-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000°C.

Step2. Poly-Si thin film formation.

Undoped poly-Si layers and undoped amorphous-Si with thickness of 100nm were deposited by low pressure chemical vapor deposition (LPCVD) on oxide by pyrolysis of silane (SiH_4) at 620°C and 550°C respectively. The amorphous-Si films were re-crystallized by solid phase crystallization (SPC) method at 600°C for 24hrs in an N_2 ambient. The grain size of as-deposited poly-Si and re-crystallized by solid phase crystallization are about 25~50 nm, as can be gauged in SEM picture after seco-etching in Fig. 2-2-3 and Fig. 2-2-4. These as-deposited poly-Si and re-crystallized poly-Si films were then patterned into islands by transformer couple plasma (TCP) etching using the mixture of Cl_2 and HBr.

Step3. Gate oxide formation.

In order to decrease the roughness of interface between gate-oxide and poly-Si island, thermal oxidation of silicon is excluded. After defining the active region, the wafers were boiled in H_2SO_4 + H_2O_2 to ensure cleanliness of the wafers before deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Soon, the gate insulator was deposited in a horizontal furnace using TEOS and O_2 gases at 700°C. The thickness of the TEOS oxide thin film is 50nm.

Step4. Gate electrode formation.

After deposition of gate insulators, another 350nm poly-Si films were deposited immediately on the gate insulators by in-situ phosphorous doping vertical LPCVD at 620°C. The second poly-Si layers were then patterned by transformer couple plasma (TCP) etching to define the gate regions and to be the mask for self-aligned implantation.

Step5. Source/drain formation.

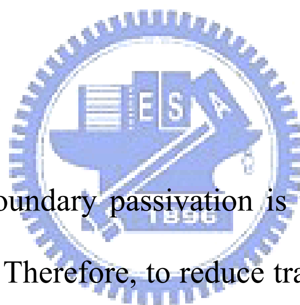
After shielding the body contact region by lithography process, phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted to form the n^+ gate and source/drain regions. Dopants were activated by rapid thermal annealing (RTA) at 750 ºC for 20 sec.

Step7. Passivation layer and contact hole formation.

After activation, a TEOS oxide layer of thickness 550nm was deposited by TEOS and O_2 gas as the passivation layers to protect TFTs. The contact holes were formed by buffer oxide etcher (BOE 7:1) subsequently.

Step8. Metallization.

The aluminum layers were deposited by physical vapor deposition (PVD) for 0.5 μm and then patterned at the gate, source/drain and body contact regions as the metal pads. Finally, the finished devices were sintered at 400°C for 30 minutes in an N_2 ambient.



Step9. Passivation.

It is known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. Therefore, to reduce trap density and improve interface quality, wafers were also immured in an NH_3 plasma generated by plasma enhanced CVD (PECVD) at 300 ºC for 0.5 hr, 1hr, 1.5hr, and 2hr, respectively.

2.3 Typical output characteristics

In this section, we would discuss the characteristics of devices with different re-crystallized methods, different hydrogen-passivation time, operating at different temperatures, and operating under various illumination frequencies. Through studying the kink effect under these various conditions the accurate physical insight could be attained. In the beginning, we showed how to extract the saturation voltage, kink current and multiplication factor from the output characteristics.

2.3.1 Parameter extraction

Because of the absence of the substrate contact in TFT or SOI devices, a simple method to determine the kink current was adopted. This method can allow an easy and reasonable characteristic analysis of the kink effect.

In this study, the saturation voltage was extracted from the output conductance directly. Each saturation voltage at various gate voltages can be defined from the "first" minimum points of the conductance, as illustrated in Fig. 2-3-1. Then, we could obtain the drain current that have not been triggered by multiplication effect from these saturation points. Therefore, the kink current I_{KINK} can be evaluated by using the drain current at high drain voltage to minus the saturation current, such that $I_{KINK} = I_{DS}-I_{D,SAT}$. As showed in Fig. 2-3-2. If we normalized the kink current by the non kink effect triggered current, the total multiplication factor which involves the impact ionization effect and drain induced barrier lowering in the pinch-off region can be obtained, thus $M = I_{KINK}/I_{D,SAT}$.

2.3.2 Different re-crystallized methods

The typical transfer characteristics of devices with different film re-crystallized fabrication are compared in Fig. 2-3-3, Fig. 2-3-4 and Fig. 2-3-5, the nominal channel length are 10μm, 5μm and 2μm and the width is kept as 10μm. It can be seen that the better grain enhanced technology shows more serious kink effect. Fig. 2-3-6(a) and Fig. 2-3-6(b) respectively show the kink current and the multiplication factor of the as-deposited and two hours hydrogen-passivated polysilicon TFT with gate length and width all kept as 10μm. During the gate voltage increases the kink current keeps on increasing because of the increasing of the entering drift-diffusion current. In addition, the multiplication factor decreases monotonously with the gate voltage increasing due to the reduced impact ionization effect. Fig. 2-3-7(a) and Fig. 2-3-7(b) respectively show the kink current and the multiplication factor of the SPC and two hours

hydrogen-passivated polysilicon TFT with gate length and width all kept as 10μm. Fig. 2-3-8(a) and Fig. 2-3-8(b) respectively show the kink current and the multiplication factor of the excimer laser annealed polysilicon TFT with 13.5 μm gate length and 12 μm gate width. In addition to the forward part of the kink current keeps on increasing because of the increasing of the entering drift-diffusion current, afterwards the continuing impact ionization effect may result in the reduction of kink current. In particular, we saw a cell-like shape in the multiplication factor which had not been observed in the single-crystal device. This phenomenon would be discussed in section 2.3.4 as the devices operate at different temperature. From the empirical expression of ionization rate, the threshold energy can be extracted as shown in Fig. 2-3-9(a),(b),(c). Apparently the smaller grain size device exhibit better kink effect suppressing ability than the larger one, as can seen in the multiplication factor for n-channel poly-Si TFTs with different film re-crystallized process (Fig. 2-3-10). The kink effect are less pronounced in as-deposited polycrystalline silicon films as the channel length shrinks to 2μm, it could be attributed to the abundant traps which act as a generation-recombination center and the generated electron-hole pairs may recombined rapidly by these traps. This conclusion is consistent with the result of [1]. The threshold energies for n-channel poly-Si TFTs with different film re-crystallized process are shown in Fig. 2-3-11, it is postulated that the threshold energy may be related to the traps density of state distribution. The full derivation and explanation of the threshold energy would be discussed in detail in the next chapter.

2.3.3 Different hydrogen-passivation time

If the hydrogen-passivation time decreases, the trap density of states may increase. So the multiplication factor may be anticipated to decrease at the low gate bias region with the passivation time increasing, as can be seen in Fig. 2-3-12. Besides, at high gate voltage operation regime the fewer hydrogen-passivation time

sample has larger multiplication factor could be speculated that the retained tail-state traps enhance the ionization rate or make the threshold energy lowering approach to the longer passivation time one (Fig. 2-3-13).

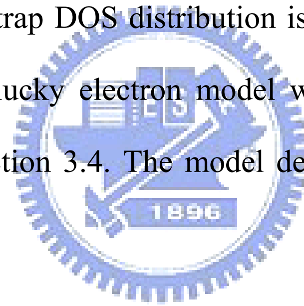
2.3.4 Operation at different temperature

In Fig. 2-3-14, we could see that in the lower gate voltage region the multiplication factor increases with the temperature increases, however at higher gate bias conduction, it shows an opposite phenomenon. It can be postulated that the kink effect are dominated by different mechanisms from low gate voltage to high gate voltage because of its two contrary temperature dependence. It is well known that the barrier height is seen to be lower at higher temperature, thus, in the lower half the multiplication factor may attributed to the drain induced grain barrier lowering effect. On the other words, it seems that the threshold energy lowering (Fig. 2-3-15) is attributed to the DIGBL effect. As for in the higher half, it should be controlled by the conventional impact ionization effect, the decreasing of multiplication factor with the temperature increasing is due to the more pronounced phonon scattering as temperature raise.

Chapter 3

Characterization and Modeling of Impact Ionization Effect in Poly-Si TFTs

In order to obtain the complete output characteristics of the polysilicon TFTs, the drain induced grain boundary lowering effect in the linear region and an exact impact ionization model in the saturation region need to be considered. First, we derived the linear region current model which included the DIGBL effect in section 3.1. Then a novel physical picture of the impact ionization process was proposed in section 3.3. The threshold energy is modified to be trap density of state distribution relative where the extraction method of the trap DOS distribution is derived in section 3.2. Finally, the threshold energy of the lucky electron model was replaced with our modified threshold energy value in section 3.4. The model derivation flow is showed in Fig. 3-0-1.

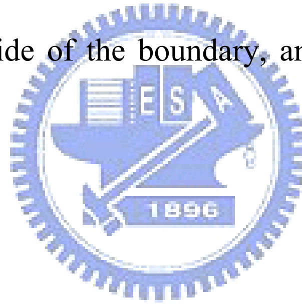


3.1 Derivation of DIGBL current model

In the past the carrier transport through the grain boundaries has investigated extensively. The grain boundary barrier was treated as a Schottky barrier and the thermionic emission of carriers over the barrier was considered [1], [2] which were based on carrier trapping model. Mandurah [3], [4] regarded this additional barriers as to result from the energy band discontinuity between the grain and grain-boundary material treating the latter as an intrinsic, wider band-gap semiconductor. In the model of Lu [5], [6], the additional barrier was called scattering potential to represent overall scattering effects in the grain boundaries. The asymmetry of space charge barrier around the grain boundary due to the applied bias was considered in the model of Mandurah while Lu assumed symmetric space charge barrier. Subsequently, the

derivation of drain induced grain barrier lowering (DIGBL) has been considered into the I-V characteristics of polysilicon thin film transistors by Lin [7].

In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t. The thickness of the grain boundary is thin enough to be neglected. The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When dopant density (or carrier density n_g in the inversion layer) is small, the poly-Si grains will be fully depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the boundary, and the barrier height V_B can be expressed as



$$V_B = \frac{qn_g}{2\varepsilon_{si}} x_d^{\,2} = \frac{qn_g L_g^{\,2}}{8\varepsilon_{si}} \qquad (3\text{-}1\text{-}1)$$

As the dopant (or carrier) concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport through grain boundary become difficult. When the dopant (or carrier) density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to appear inside the grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n_g} \qquad (3\text{-}1\text{-}2)$$

$$V_B = \frac{qn_g}{2\varepsilon_{si}} \left(\frac{N_t}{2n_g}\right)^2 = \frac{qN_t^{\,2}}{8\varepsilon_{si} n_g} \qquad (3\text{-}1\text{-}3)$$

Under this circumstances ($n_g > N^*$), the depletion width and the barrier higher

turn to decrease with increasing dopant (or carrier) density, leading to improved conductivity in carrier transport in poly-Si film.

The carrier transport in partially-depleted poly-Si film can be described by the thermionic emission over the symmetric Schottky barriers [8] and we ignored the thermionic field emission which dominates at extremely high drain bias or low ambient temperature. Its current density can be written as

$$J = qn_g v_c \exp[-\frac{q}{kT}(V_B - V)] \tag{3-1-4}$$

where n_g is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{kT/2\pi m^*}$), V_B is the barrier height without applied bias.

For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_{grain}/2$ which we so called drain induced barrier lowering. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qn_g v_c \exp\left[-\frac{q}{kT}(V_B - \frac{1}{2}V_{grain})\right] \tag{3-1-5}$$

$$J_R = qn_g v_c \exp\left[-\frac{q}{kT}(V_B + \frac{1}{2}V_{grain})\right] \tag{3-1-6}$$

where V_{grain} is the applied bias across the grain boundary region which can be described by

$$V_{grain} = E_i \times 2x_d = \frac{V_{DS} N_t}{L n_g} \tag{3-1-7}$$

where $E_i = V_{DS}/L$ is the average lateral electric field across the ith grain .

the net current density is then given by

$$J = 2qn_g v_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_{grain}}{2kT}) \tag{3-1-8}$$

at high enough applied voltages, the Eq. (3-1-8) can then be simplified as

$$J = qn_g \exp\left[-\frac{q\left(V_B - V_{grain}/2\right)}{kT}\right]\mu_0 E_i \tag{3-1-9}$$

In poly-Si TFTs, the carrier density n_g induced by the gate voltage can be expressed as

$$n_g(V_X) = \frac{C_{OX}(V_G - V_{TH} - V_X)}{qt_{ch}} \tag{3-1-10}$$

where t_{ch} is the thickness of the inversion layer.

If the effective space charge density is defined as N_t/L_g, the threshold voltage (V_{TH}) is given by

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_{si} q (N_t/L_g)(2\phi_B)}}{C_{OX}} \tag{3-1-11}$$

where $\phi_B = \frac{kT}{q}\ln(\frac{N_t/L_g}{n_i})$ and V_{FB} is defined as the minimum point of the transfer characteristic curve.

Therefore, by replacing Eq. (3-1-7), Eq. (3-1-10) and Eq.(3-1-11) into Eq. (3-1-9), the drain current in the ith grain is $I_i = J_i \times W \times t_{ch}$ of poly-Si TFT, then I_{DS} can be obtained by integrating I_i from the source to the drain in the linear output characteristic region:

$$I_{DS} = \frac{W}{L}\mu_0 \int_0^{V_{DS}} \exp\{\frac{q\left[V_B(V_X) - \frac{V_{grain}(V_X)}{2}\right]}{kT}\} \times qt_{ch} n_g(V_X) dV_X \tag{3-1-12}$$

It should be carefully judged that in the drain bias, the saturation voltage is attributed to the channel collapses or the carrier velocity saturates. If the square root of the drain current is varies linearly with the gate voltage, we can assure that the predominant factor is carrier concentration saturation, as seen in Fig. 3-1-1. The saturation voltage can described as $V_{D,SAT} = \eta V_G$, where η is the bulk charge modified term. The relationship between the saturation voltage and gate voltage is illustrated in

Fig. 3-1-2.

As the drain voltage increases close to the saturation voltage, the effective gate induced carrier concentration is approach to zero. We regarded this condition as the fully depleted situation, and the grain boundary barrier height is fixed to its maximum value $V_{Bm} = qL_gN_t/8\varepsilon_{si}$. This voltage V_m is defined as

$$V_m = \eta V_G - \frac{N_t}{L_g} \cdot \frac{qt_{ch}}{C_{OX}} \tag{3-1-13}$$

Therefore, the drain current reach the saturation point can be written as

$$I_{DS} = \frac{W}{L} t_{ch} [\int_0^{V_m} J_i(V_B) dV_X + \int_{V_m}^{V_{DSAT}} Ji(V_{Bm}) dV_X \tag{3-1-14}$$

As shown in Fig. 3-1-3, the threshold voltage increases with increasing trap density and decreasing grain size. Fig. 3-1-4 shows the calculated potential barrier height which involves the drain induced barrier lowering effect. The potential barrier increases as the drain voltage increase because the effective gate induced carrier concentration decreases with the drain voltage increasing. However, the barrier height raising speed is not as fast as the gate voltage increase due to the DIGBL effect.

3.2 Determination of density of state in the band gap

The determination of the gap density of states is one of the key issues for the development of polycrystalline silicon thin-film transistors. Several methods, based on measurements of optical absorption [1], capacitance-voltage [2], activation energy of resistivity as a function of doping concentration [3-6], conductance method measured the frequency dependence of the conductance [7], charge-pumping method [8-10], deep level transient spectroscopy method [11] ,and field-effect conductance activation energy as a function of the gate voltage [12-15], have been proposed to determine the density of states in polysilicon films.

In this section, we use a computer minimization method that is based on field-effect conductance measurements [16], so it can provide exact information on the density of states. Numerical calculations of the field-effect activation energy as a function of the gate voltage are presented for different defect distributions. The activation energy E_a of the source-drain current can be approximated by the energy difference between the conduction band edge and the surface potential ψ_s in the grain boundary, i.e. $E_a = E_{f0}-q\psi_s$, where $E_{f0} = E_c(bulk)-E_f$ and E_f is the equilibrium Fermi-level position (Fig. 3-2-1). The energy distribution $N_{bulk}(E)$ of the bulk traps can be modeled by the sum of a deep-level Gaussian distribution $N_{deep}(E)$ with a maximum at energy E_t near the midgap and an exponential-like $N_{tail}(E)$ band tail near the conduction-band edge, i.e.,

$$N_{bulk}(E) = N_{deep}(E) + N_{tail}(E) = N_{ds}\exp(-\frac{E_c - E}{kT_{ds}}) + N_{ts}\exp(-\frac{E_c - E}{kT_{ts}}) \quad (3\text{-}2\text{-}1)$$

where N_{ds} is the total trap density per unit area, s_d is the standard deviation of the Gaussian trap distribution and N_{ts}, T_{ts} are parameters characteristic of the exponential trap distribution. The deep level Gaussian distribution density of states is due to the dangling bonds and the tail states is due to the silicon-bonds disorder and strain.

The total charge density per unit area Q_{bulk} in the bulk semiconductior is given by

$$Q_{bulk} = -(2\varepsilon_{si}\int_0^{\phi_s}\rho_{bulk}(V)dV)^{1/2} \quad (3\text{-}2\text{-}2)$$

Where

$$\rho_{bulk} = -(\frac{2q}{L_g})\int_{E_{f0}}^{E_{f0}+qV} N_{bulk}(E)dE \quad (3\text{-}2\text{-}3)$$

As increasing the gate voltage, the activation energy will be decreased. The calculation of the surface potential as a function of the gate voltage will allow us to determine the energy distribution of the density of states by fitting the theoretical with the experimental activation energy data.

There are some common assumptions in this method. First one is that the traps at the grain boundaries are uniformly distributed throughout the film. Secondary is that

the conduction band edge E_c and the Fermi level E_f are independent of temperature and the flat band voltage V_{FB} is constant.

The process of finding the surface potential is illustrated as Fig. 3-2-2. We start from $Q_{in} = Q_{bulk} = -C_{ox} (V_G-\psi_s-V_{FB})$. (3-2-4)

Where

Q_{in} is the total induced charge per unit area.

Q_{bulk} is the trapped charge in the bulk

These four kinds charge can be presented as the function of surface potential, gate voltage and activation energy.

Substituting Eq. (3-2-1), Eq. (3-2-2), and Eq. (3-2-3) into Eq. (3-2-4), we can obtain an equation about the surface potential and gate voltage. As we have the relationship of V_G-ψ_s we can obtain V_G-E_a from $E_a = E_{f0}-q\psi_s$. By fitting the calculated activation energy with the activation energy extracted from Arrhenius plot, we can get the parameters of the trap density of state in band gap.

According to the trapping theory, the carrier conduction equation can be given as

$$I = \frac{q^2 L_g N_c \nu_c}{kT}\exp[-\frac{(\frac{E_g}{2} + E_B - E_f)}{kT}] \qquad (3\text{-}2\text{-}5)$$

,where the effective density of states beyond the conduction band edge $N_c \sim T^{3/2}$ and the collection velocity $\nu_c \sim T^{1/2}$

Therefore, the relationship of the current and the temperature holds

$$IT^{-1} \propto \exp\left(-\frac{E_a}{kT}\right) \qquad (3\text{-}2\text{-}6)$$

The activation energy can be obtained from the Arrhenius plot (Fig.3-2-3) and the fitting results and extracted parameters are as shown in Fig. 3-2-4, Fig. 3-2-5 and Table. 3-2-1.

3.3 The modified threshold energy

The general agreement in the literature for the value of the threshold energy for impact ionization is 1.5 times the energy gap (E_g) at room temperature which corresponds to 1.65eV in the case of silicon. The relationship E_{th} = 1.5E_g is obtained from the momentum and energy conservation of a collision event, this energy determine an electron need to acquire at least a kinetic energy.

From the energy conservation: $\frac{1}{2} m_e V_1^{\ 2} = E_g + 3 \times m_e V_2^{\ 2}$ (3-3-1)

From the momentum conservation: $m_e V_1 = 3 m_e V_2$ (3-3-2)

where m_e is the effective electron mass, V_1 is the velocity of the electron before colliding and V_2 is the velocity of the electron and the generated electron-hole pair after the colliding, here we assume these three particles have the same velocity.

Solving the equations (3-1) and (3-2), the threshold energy can be obtained.

Nevertheless, this simple threshold energy presentation is not suitable in the case of polysilicon TFTs due to the presence of the trap density of state distribution in the forbidden band gap. As we have discussed in the second section in this thesis, the threshold energy decreases with different grain size and hydrogen-passivation time and it also varies with the gate voltage applying. Because these density of states may act as a generation center in the impact ionization process, furthermore, a neutral charge trap (first situation) plays a different role to a charged trap states (second situation). In this subsection, the threshold energy will be revised by considering the presence of the trap density of state. Thus, as calculating the new threshold energy, we take into account both the neutral and charged traps in their own trap states. Only the acceptor-like traps are considered in the derivation since our samples are n-type polysilicon thin-film transistors.

In the first situation, the acceptor-like trap that beyond the quasi-Fermi level is

neutral. One high energy electron can initialize an electron-hole pair at this neutral trap state, and the "activation energy" is from the valance band edge to the trap energy level, as shown in Fig.3-3-1(a). Thus, the energy and momentum conservation relation is given as

$$\frac{1}{2}m_eV_1^2 = (E_{T1}) + 3\times\frac{1}{2}m_eV_2^2 \qquad (3\text{-}3\text{-}3)$$

and

$$m_eV_1 = 3m_eV_2 \qquad (3\text{-}3\text{-}4)$$

By solving the above two equations the threshold energy distribution in the band gap can be obtained as

$$E_{th1}(E_{T1}) = 3/2(E_{T1}) \qquad (3\text{-}3\text{-}5)$$

Integrating this threshold energy level multiply the density of states distribution of the neutral trap from the quasi-Fermi level E_f to E_C+E_B and normalized it to the total amount of the neutral traps, the effective threshold energy can be estimated as

$$E_{th1} = \left[\frac{\int_{E_f}^{E_C+E_B} N_{bulk}(E_{T1})\times E_{th1}(E_{T1})dE_{T1}}{\int_{E_f}^{E_C+E_B} N_{bulk}(E_{T1})dE_{T1}}\right] \qquad (3\text{-}3\text{-}6)$$

In the second situation, the acceptor-like trap that under the quasi-Fermi level is negative charged. One high energy electron can knock an electron out at this trap state, and the "activation energy" is from this charged trap energy level to the conduction band edge, as shown in Fig.3-3-1(b). Thus, the energy and momentum conservation relation is given as

$$\frac{1}{2}m_eV_1^2 = (E_g - E_{T2}) + 2\times\frac{1}{2}m_eV_2^2 \qquad (3\text{-}3\text{-}7)$$

and

$$m_eV_1 = 2m_eV_2 \qquad (3\text{-}3\text{-}8)$$

By solving the above two equations the threshold energy distribution in the band

gap can be obtained as

$$E_{th2}(E_{T2}) = 2(E_g - E_{T2}) \tag{3-3-9}$$

Integrating the reciprocal of threshold energy level which multiplies the density of states distribution of the negative charged trap from the barrier height potential E_B to the quasi-Fermi level E_f and normalized it to the total amount of the negative charged traps, the effective threshold energy can be estimated as

$$E_{th2} = \left[\frac{\int_{E_B}^{E_f} N_{bulk}(E_{T2}) E_{th2}(E_{T2}) dE_{T2}}{\int_{E_B}^{E_f} N_{bulk}(E_{T2}) dE_{T2}} \right] \tag{3-3-10}$$

Consequently, the final threshold energy that we adopt into the Shockley's "luck electron model" is the smaller one between E_{th1} and E_{th2}. The conventional threshold energy $1.5E_g$ is replaced by the new threshold energy that is derived by our model. Here the threshold energy model we used in our model is E_{th2} because of its smaller value..

3.4 Impact ionization model

Impact ionization is an important charge generation mechanism. By scaling down the geometrical dimensions while keeping the supply voltage constant, the electrical field increases and therefore impact ionization plays a more important role in device degradation due to hot-carrier effects and bipolar parasitic breakdown.

We first derive the basic ionization integral which determines the breakdown condition. Assume that a current I_{n0} is incident at the left-hand side of the depletion region (x = 0). If the electric field in the depletion region is high enough that electron-hole pairs are generated by the impact ionization process, the electron current I_n will increase with distance through the depletion region and reaches a value M_nI_{n0}

at the drain edge (x = W). Similarly, the hole current I_p will increase from x = W to x = 0. The total current I (= I_n+I_p) is constant at steady state. The incremental electron current at x equals the number of electron-hole pairs generated per second in the distance dx,

$$d(\frac{I_n}{q}) = (\frac{I_n}{q})(\alpha_n dx) + (\frac{I_p}{q})(\alpha_p dx) \quad (3\text{-}4\text{-}1)$$

or

$$\frac{dI_n}{dx} - (\alpha_n - \alpha_p)I_n = \alpha_n I \quad (3\text{-}4\text{-}2)$$

The solution of Eq. (3-4-2) with boundary condition that I = $I_n(W) = M_n I_{n0}$ is given by

$$I_n(x) = I\left[\frac{1}{M_n} + \int_0^x \alpha_p \exp\left(-\int_0^{x'} (\alpha_n - \alpha_p)dx''\right)dx'\right] \times \exp\left(\int_0^x (\alpha_n - \alpha_p)dx'\right) \quad (3\text{-}4\text{-}3)$$

Since we are considering electron-initiated impact ionization, and there is no hole current entering the depletion region at x = W, the current at x = W is simply equal to I. Therefore, Eq. (3-4-3) gives

$$\frac{1}{M_n} = \exp\left(-\int_0^W (\alpha_n - \alpha_p)dx\right) - \int_0^W \alpha_p \exp\left(-\int_x^W (\alpha_n - \alpha_p)dx'\right)dx \quad (3\text{-}4\text{-}4)$$

For the special case of $\alpha_p = 0$, the electron multiplication factor becomes

$$M_n = \exp(\int_0^W \alpha_n dx) \quad (3\text{-}4\text{-}5)$$

Therefore, the excess substrate current (or the excess kink current) can be expressed as $I_{kink} = I_{n0}(M_n\text{-}1)$ (3-4-6)

If the impact ionization rate is much smaller than the unit, the excess kink current before the avalanche breakdown can be described as

$$I_{kink} = I_d \int_0^W \alpha_n dx = I_{DIGBL} \int_0^{\Delta L} \alpha_n dx \quad (3\text{-}4\text{-}7)$$

where I_{DIGBL} is the entering current modified by the drain induced grain barrier lowering effect from the left-side of pinch-off region in the poly-Si TFTs, and ΔL is the length of the saturation region which is derived by a similar step P-N junction

$$\Delta L = \sqrt{\frac{2\varepsilon_{si}}{q(N_t / L_g)}(V_{ds} - V_{dsat})} \qquad (3\text{-}4\text{-}8)$$

Here, we use the lucky electron model to describe the impact ionization rate. It is not the carriers with the average energy that can initialize impact ionization, but only those larger than an energy threshold energy E_{th}. The original of these high-energy carriers is from a "lucky" population of electrons which go without scattering for a distance x, much larger than the mean free path of collision λ. The distance x that an electron has to travel to gain this amount of the kinetic energy from the potential energy is:

$$qEx = qE_{th} \Rightarrow x = \frac{E_{th}}{E} \qquad (3\text{-}4\text{-}9)$$

The concentration n of these lucky electrons is

$$n = n_0 \exp(\frac{-E_{th}}{E\lambda}) \qquad (3\text{-}4\text{-}10)$$

The impact ionization coefficient α is

$$\alpha \propto n = n_0 \exp(\frac{-E_{th}}{E\lambda}) \qquad (3\text{-}4\text{-}11)$$

Thus, the measured ionization rates are often expressed in the empirical form of

$$\alpha = A_i \exp(\frac{-\beta}{E}) \ \ (\#/\text{cm}) \ ; \ \ \beta = \frac{E_{th}}{\lambda} \qquad (3\text{-}4\text{-}12)$$

The excess kink current of polysilicon TFTs can be given by

$$I_{kink} = I_{DIGBL} \int_0^{\Delta L} A_i \exp\left(\frac{-\beta}{E}\right) dx \qquad (3\text{-}4\text{-}13)$$

Replacing dx by $\frac{dx}{dE} dE = -E^2 \frac{dx}{dE} d\left(\frac{1}{E}\right)$ and $\frac{dE}{dx} = \frac{E}{l}$ we have

$$I_{kink} = -I_{DIGBL} \int_{E_{source}}^{E_m} A_i \exp\left(\frac{-\beta}{E}\right) lEd\left(\frac{1}{E}\right) \qquad (3\text{-}4\text{-}14)$$

Since the exp(-β/E) is the most dominate function of E, thus we may replacing E in the other mildly variation terms with E_m. That is replacing lE by lE_m.

The excess kink current becomes

$$I_{kink} = I_{DIGBL} \int_{E_{source}}^{E_m} A_i \exp\left(\frac{-\beta}{E}\right) l E_m d\left(\frac{1}{E}\right) \quad (3\text{-}4\text{-}15)$$

$$\Rightarrow I_{kink} = \frac{A_i}{\beta} l E_m \exp\left(\frac{-\beta}{E_m}\right) \times I_{DIGBL} \quad (3\text{-}4\text{-}16)$$

The maximum electric field can be replaced by

$$E_m = \sqrt{\left(\frac{V_{ds} - V_{dsat}}{l}\right) + E_{sat}^{\ 2}} \cong \frac{V_{ds} - V_{dsat}}{l} \ (\text{ if } \frac{V_{ds} - V_{dsat}}{l} >> E_{sat}) \quad (3\text{-}4\text{-}17)$$

$$\Rightarrow I_{kink} = \frac{A_i}{\beta}(V_{ds} - V_{dsat}) \exp\left(\frac{-\beta l}{V_{ds} - V_{dsat}}\right) \times I_{DIGBL} \quad (3\text{-}4\text{-}18)$$

Using the drain induced grain barrier lowering current and the novel threshold energy expression that we derived in the first and the third sections of this chapter respectively in the Eq. (3-4-18), the entire impact-ionization current model can be obtained.

3.5 Result and discussion

The consequent results compare the modeling results and the experimental data, good agreements are found. The parameter set is shown in Table 3-5-1. Because of the gate induced carrier channel thickness in polycrystalline silicon TFTs is not investigated clearly to date. Hence, we assumed that the conduction channel thickness t_{ch} is empirically expressed as $t_{ch} = A1/(\eta V_G)^{A2}$ which can give the best fitting result. Fig. 3-5-1 shows I_D-V_{DS} characteristics for n-channel TFT's. The model could describe the measured results over wide ranges of gate and drain voltages. Furthermore, we compared the I_D-V_{DS} characteristics with conventional threshold energy (1.68eV) and our simulated threshold energy in Fig. 3-5-2. It can be seen that the conventional threshold energy underestimate the impact ionization effect.

Chapter 4

A Physically-Based Subthreshold Model of Poly-Silicon Thin-Film Transistors with Parasitic BJT Effect

4.1 Introduction

In recent years, polysilicon thin film transistor (poly-Si TFT) have been developed many applications, for example, static random access memories (SRAM), active matrix liquid crystal(AMLCD), and high performance EEPROM. To compare the poly-Si TFT with the classis MOSFET, the major difference is that the body in the poly-Si TFT is usually floating, so it is easily to suffer from the parasitic BJT. This effect will cause the better subthreshold swing [1] and lower threshold voltage [1], and to enhance the lager impact ionization current [2], make the devices to breakdown more early. Because there are similar effects on the silicon on insulator (SOI), we also can find several literatures about parasitic BJT in the SOI, for example [3] ~ [5].

For the polycrystalline silicon, there are many grain boundaries (GBs) in this material, and GBs will form a barrier height, it will retard the carrier transport, and then make the worse subthreshold swing and lower threshold voltage [6] , [7].

In our model, we will consider the similar model with Yu's model [3] about the parasitic BJT and Chen's model [7] about the surface potential to get a accurate subthreshold current. It will present a physical-based numerical model about the subthreshold region in the polysilicon thin film transistors.

4.2 Model derivation

We proposed a model that derived the subthreshold current under large drain bias

and made up with a surface electrostatic potential model that is presented by S.S.Chen et al. [2] and the parasitic BJT model that had been investigated extensively in SOI device [3], [4]. To calculate the accurate impact ionization effect factors, the iterative multiplication process of the initial current flow should be considered [5].

4.2.1 Parasitic BJT model

We based on the Yu's model [3] to model the parasitic BJT, this model use a BJT to calculate the parasitic effect, as shown in Fig. 4-2-1. But the differences between our consideration and Yu's model are that we didn't consider the back gate and back oxide, so we can simplify Yu's model to suit the situation in the polysilicon thin film transistors.

Firstly, we should define some important current components.

$$I_{sub} = W\mu_{eff} \frac{q}{kT} \frac{Q_s - Q_d}{L} \tag{4-2-1}$$

$$Q_s = C_{ox}(V_G - V_{FB} - \phi_s) - \frac{1(N_t / L_g)}{1 + K_m \exp(\frac{-q\phi_s}{kT})} \times t_{ch,s} \tag{4-2-2}$$

$$Q_d = C_{ox}(V_G - V_{FB} - (\phi_s + V_{DS})) - \frac{1(N_t / L_g)}{1 + K_m \exp(\frac{-q(\phi_s + V_{DS})}{kT})} \times t_{ch,d} \tag{4-2-3}$$

I_{sub}: the subthreshold current which is derived from a gradual channel approximation if we have found the relation of surface potential and gate bias.

$$I_{erec} = \frac{qAN_i W_{be}}{2\tau_r}[\exp(\frac{qV_{be}}{2kT}) - 1] \tag{4-2-4}$$

I_{erec}: the electron recombination current in the depletion region of drain side.

$$\mathrm{I}_{\mathrm{edif}} = \frac{q^2 A\mu_{eff} N_i^2}{kTpW_b}[\exp(\frac{qV_{be}}{kT}) - 1] \tag{4-2-5}$$

$$\mathrm{I}_{\mathrm{hdif}} = \frac{q^2 A \frac{1}{3} \mu_{eff} N_i^2}{kTN_d \frac{1}{\sqrt{3}} L_n}[\exp(\frac{qV_{be}}{kT}) - 1] \tag{4-2-6}$$

I_{edif}, I_{hdif}: the electron and hole diffusion current in the pn junction of source side, respectively.

$$I_{hm} = M_m \times (I_{sub} + kI_C) \quad (4\text{-}2\text{-}7)$$

I_{hm}: the impact ionization current comes from subthreshold current I_{sub} and parts of the collect current ($I_C = \alpha_T I_{edif}$).

$$I_{hb} = (M_b - 1)(1 - k)I_C \quad (4\text{-}2\text{-}8)$$

I_{hb}: the impact ionization current comes from parts of collect current $(1-k)*\alpha_T I_{edif}$.

$$I_{hg} = M_b \frac{qAN_i W_{bc}}{2\tau_g} \quad (4\text{-}2\text{-}9)$$

I_{hg}: the impact ionization current comes from the generation current in the depletion region.

Below the front surface, the electronic behavior is similar a BJT, so we consider the diffusion and recombination current in the body and source junction, because the electrical field applied in this junction is forward bias, on the other hand, in the body and drain junction is reversed bias, so there is a generation current.

$$I_E = I_{edif} + I_{erec} + I_{hdif} \quad (4\text{-}2\text{-}10)$$

$$I_B = I_{ht} = I_{hg} + I_{hm} + I_{hb} \quad (4\text{-}2\text{-}11)$$

$$I_C = k\alpha_T \times I_{edif} \quad (4\text{-}2\text{-}12)$$

$$I_E = I_B + I_C \quad (4\text{-}2\text{-}13)$$

From Eq.(4-2-13) we can solve V_{be} using numerical method from the balance among the emitter current, the collect current, and the base current.

No matter what Yu [3], Chen [4], Cheng [5], the carrier lifetime in their models is constant, it is invariable, but when V_{ds} is increasing, V_{be} is also became larger, and the accumulated hole in the body will be increased, so we think the carrier lifetime should not be a constant, it is a variable which vary with the V_{be}. In our developed model, it is a fitting parameter which will change with the V_{be}, later we will discus

this factor.

4.2.2 Impact-Ionization factor derivation

The impact-ionization mechanism must occur in the pinch-off region in which the lateral electric field is greater than the critical electric field ($E_{imp,C}$). For simplicity, we assume that the lateral electric field over the whole saturation region (from the pinch-off point to the drain junction) is the same with the critical electric field ($E_{imp,C}$). It is important to note that the generation rate of the electron-hole pairs by the impact-ionization mechanism will be proportional to the quantity of the initiating electron flow.

$$dI_{em}(y)=\alpha(y)[I_{CH}+I_{em}(y)]dy \qquad (4\text{-}2\text{-}14)$$

where y is in the lateral channel direction, I_{CH} is the initial channel current without considering the impact-ionization effect, the $I_{em}(y)$ is the impact-ionization current initiated by the electrons and $\alpha(y)$ is the impact-ionization rate of the electrons which can be derived from the "Lucky electron model":

$\alpha(\varepsilon)=\frac{q\varepsilon}{E_I}\times\exp\left(\frac{E_I}{q\varepsilon\lambda}\right)$ where E_I is the threshold energy of impact-ionization, λ is the optical-phonon mean free path of carriers in Si.

The drain current is mainly contributed to the impact-ionization electron current component and is expressed by $dI_D(y) = dI_{em}(y)$.

From these above equations, we can obtain

$$\int_{I_{CH}}^{I_D}\frac{dI_D'}{I_D'}=\int_0^{L_{SAT}}\alpha(y)dy=\int_{V_{D,SAT}}^{V_D}\alpha(\varepsilon)\frac{dV}{\varepsilon} \qquad (4\text{-}2\text{-}15)$$

where L_{SAT} is the length of saturation region, ε is the lateral electric field, and it is given as an empirical equation [5]

$$\varepsilon(V)=\varepsilon_{imp,C}\left(\frac{V}{V_{D,SAT}}\right)^{\gamma} \tag{4-2-16}$$

For long channel devices, $\gamma = 0$, because of the weak electric field dependence on the applied voltage. In the other hand, $\gamma = 1$ for short channel devices.

Substituting Eq.(4-2-16) into Eq.(4-2-15), the drain current can be obtained as follows:

$$I_D = I_{CH} \times M_m \tag{4-2-17}$$

where $M_m=\exp\left[\int_{V_{D,SAT}}^{V_D}\alpha(\varepsilon)\frac{dV}{\varepsilon}\right]$ is the impact-ionization factor.

4.2.3 Surface electrostatic potential model

The grain boundaries is assumed perpendicular to the lateral channel and contains N_t (cm^{-2}) of traps located at energy E_T. The total charge density in the Gauss box is the sum of free carrier charges, trapped charges, and ionized doping charges. Based on these assumptions, the one-dimensional Poisson's equation is

$$\frac{\partial^2\phi}{\partial x^2}=\frac{q}{\varepsilon_{Si}}\left(\frac{N_T/L_g}{1+\frac{1}{2}\exp[(\frac{E_t-q\phi+q\phi_f}{kT})}+N_A\exp(\frac{\phi-2\phi_f}{\beta})+N_A\right) \tag{4-2-18}$$

where x is in the substrate direction, q is the electron charge, ε_{Si} is the silicon permittivity, and ϕ is the electrostatic potential. N_A is the doped acceptor density, L_g is the grain size, and ϕ_f is the Fermi potential: $\phi_f = \beta\ln(N_A/n_i)$, where β is kT/q, k is Boltzmann constant, and T is the temperature in Kelvin.

Using the relationship:

$$2\frac{\partial\phi}{\partial x}\left(\frac{\partial^2\phi}{\partial x^2}\right)=\frac{\partial}{\partial x}\left(\frac{\partial\phi}{\partial x}\right)^2$$, and $$E(\phi_S)=\frac{\partial\phi}{\partial x}\bigg|_{\phi=\phi_S}$$

from Eq.(4-2-8), the electric field at poly-Si/oxide interface $E(\phi_S)$ can be obtained.

Applied gate voltage V_G is equal to the sum of the flat band voltage V_{FB}, the voltage drop across oxide V_{OX} and the surface potential ϕ_S, i.e.

$$V_G = V_{FB} + \phi_S + V_{OX}$$

$$= V_{FB} + \phi_S + \varepsilon_{Si} E(\phi_S)/C_{OX} \qquad (4\text{-}2\text{-}19)$$

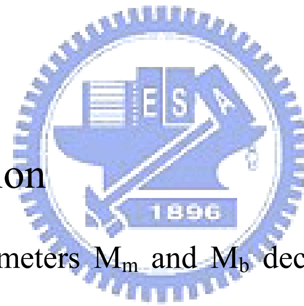
where C_{OX} is the gate capacitance per unit area

By plugging $E(\phi_S)$ into Eq.(4-2-19), the relationship between applied gate bias V_G and surface electrostatic potential can be found from the following equation:

$$V_G = V_{FB} + \phi_S + \frac{\varepsilon_{Si}}{C_{OX}} \sqrt{\frac{2q}{\varepsilon_{Si}} \left[N_A \phi_S + \beta \frac{N_i^2}{N_A} \left(\exp\left(\frac{\phi_S}{\beta}\right) - 1 \right) + \frac{N_t}{L_g} \left(\phi_S + \beta \ln \left(\frac{1+\exp\left(\frac{E_t + q\phi_f - q\phi_S}{kT}\right)}{1+\exp\left(\frac{E_t + q\phi_f}{kT}\right)} \right) \right) \right]}$$

(4-2-20)

From Eq.(4-2-20) the exact surface potential ϕ_S can be obtained by using Newton's approach method.



4.3 Result and discussion

The amount of the parameters M_m and M_b decide how the avalanche-induced parasitic current components affect the whole drain current. In Fig. 4-3-1, the relations among M_m - 1, I_{sub}, Ic, and I_{hm} as a function of V_G is proposed. In Fig. 4-3-1(a), because of the decrease of the multiplication factor Me-1 isn't apparent under such long channel device (L = 6μm), the total generated hole current, I_{ht} still increase to follow the subthreshold current I_{sub}. In the short channel device (L = 1.5μm), the increase in V_G results in more obvious decrease in Mm – 1, because of the increase of V_{dsat}. Therefore, under large gate bias, the avalanche-induced hole current will drop off, as shown in Fig. 4-3-1(b).

Similarly, in Fig. 4-3-2(a), the BJT multiplication factor, M_b – 1 has even less influence on parasitic hole current as gate bias increases. However, in the short channel device (L = 1.5μm), the increase in V_G results in the obvious increase in M_m –

1, as shown in Fig. 4-3-2(b). It is attributed to the increasing of V_{be} with gate bias V_G.

The simulated result of the relationship of body potential and drain voltage, V_{ds} for various gate voltage, V_G, for W/L = 10μm/6μm is shown in Fig. 4-3-4(a). As shown in the figure, for a larger gate bias, the bulk-emitter voltage becomes larger. Due to the increase of the subthreshold current, the bulk-emitter voltage which is obtained from a numerical method of the balance among the emitter current, the collect current, and the base current becomes larger as gate bias increases in the long channel device. As discussed above, the influence of V_{dsat} roll-off isn't apparent on the multiplication factor in the long channel device. In contrast, for a larger gate bias, the bulk-emitter voltage becomes smaller in short channel device, as shown in Fig. 4-3-4(b).

Finally, we analyze the trap density and channel length depended transport factor, α_t. As shown in Fig. 4-3-5, the transport factor is extremely small under long channel device and higher trap density. Because the electron diffusion length is about 1.5μm, the transport factor will decrease rapidly when channel length exceed 1.5μm. The transport factor approach to one as the trap density decreases, it is due to the effective acceptor concentration approximation $p = N_t/L_g$ that we use to calculate the electron life time $\tau_n = 10^{-8}/(1+p/3\times10^{22})$.

4.4 Conclusion

A physical subthreshold model of poly-silicon TFTs with parasitic BJT effect is proposed. This model evaluated body potential by approaching to a balance among various current components in the TFT and parasitic BJT systems. After considering the trap density in the active film, the surface potential can be derived exactly. With a simple gradual channel approximation, we can obtain the subthreshold diffusion

current from this surface potential banding. Further considering a multiplication behavior in the impact ionization effect, those parasitic BJT current components can be obtained more accurately.

Chapter 5

A New Empirical Leakage Current Model of Poly-Si Thin Film Transistors

5.1 Introduction

In recent years, polysilicon thin film transistor (poly-Si TFT) have been developed many applications, for example, static random access memories (SRAM), active matrix liquid crystal (AMLCD), and high performance EEPROM. To implement the integration of the peripheral driving circuitry and to be suitable for the computer-aided circuit design, understanding and predicting the leakage current is very important.

According to Olasupo's research on the activation energy analysis [1], we can know that the phonon-assisted tunneling current near the drain side is the most general leakage current mechanism. Thermionic emission and pure tunneling are two extreme conditions. Traditionally, two kinds of leakage current models were proposed. One is the simulation model, had been proposed by Hurkx [2], Lui [3], and Vincent [4], this kind model is to simulation the phonon-assisted tunneling current. They consider the phonons excite the electron to jump from trap to a virtual state and the electrical field makes the electron to jump from the virtual state to valence band. But as for the electric field in the depletion region, they didn't discuss how Vg and Vd make effects on leakage current. On the other hand, in order to simplify the derived process, Kim [4] proposed another analytic model. When it calculated the thermionic field emission, the phonon excited the electron jump from the valence band to trap, and the electrical field make the electron to jump from trap to conduction band, this kind model has less physical insight than the Hurkx's [4] model.

We introduce the empirical electrical field formulas [6] and the simulation model [3] to construct the new leakage current model. It was not only an insightful physical model, but also reduced the fitting parameters. So, our model was more suitable for the circuit simulation.

5.2 Physical model

In our model, the leakage current is dominated by both phonon-assisted tunneling effect near the drain side and also the Poole-Frenkel effect [3]. The phonons excite the electron to jump from the O level to the P level. Then, the electrical field makes the electron to jump from the P level to the P' level, as illustrated in Fig. 5-2-1.

The general generation rate is expressed as:

$$R_t = N_t \frac{c_n c_p np - e_n e_p}{c_n n + c_p p + e_n + e_p} \qquad (5\text{-}2\text{-}1)$$

The Poole-Frenkel effect described that if we applied an electric field on the semiconductor, a Coulombic well is lowered while the Dirac well remains unchanged.

The Coulombic potential barrier lowing is

$$\Delta E_t = \left(\frac{q^3 E}{\pi \varepsilon_{si}}\right) \qquad (5\text{-}2\text{-}2)$$

According to the Vincent's and Lui's model, we can get the field enhanced thermal emission rate, electron and hole concentration for the Coulombic well:

$$\chi = \exp\left(\frac{\Delta E_t}{kT}\right) \quad \Gamma = \int_{\frac{\Delta E_t}{kT}}^{\frac{\Delta E_p}{kT}} \exp\left\{z - z^{\frac{3}{2}}\left(\frac{4}{3}\frac{\sqrt{2m^*(kT)^3}}{q\hbar \mathrm{E}}\right)\left[1-\left(\frac{\Delta E_t}{zkT}\right)\right]\right\} dz) \qquad (5\text{-}2\text{-}3)$$

where ΔE_p is the difference between the trap state and conduction band

χ is the factor contributed from Poole Frenkel effect

Γ is the factor contributed from tunneling effect

$$e_n^c = e_n(\chi + \Gamma^{Coul}) \quad e_p^c = e_p(\chi + \Gamma^{Coul}) \tag{5-2-4}$$

$$n^c = n(\chi + \Gamma^{Coul}) \quad p^c = p(\chi + \Gamma^{Coul}) \tag{5-2-5}$$

e_n^c , e_p^c and n^c , p^c are the modified electron , hole emission rate and concentration for Coulombic well.

For the Dirac well $\Delta E_t = 0$,

$$\chi = 0 \quad \Gamma = \int_0^{\frac{\Delta E_p}{kT}} \exp\{z - z^{\frac{3}{2}}(\frac{4}{3}\frac{\sqrt{2m^*(kT)^3}}{q\hbar \mathrm{E}})\}dz) \tag{5-2-6}$$

,so the field enhanced thermal emission rate, electron and hole concentration for the Dirac well is

$$e_n^d = e_n(1 + \Gamma^{Dirac}) \quad e_p^d = e_p(1 + \Gamma^{Dirac}) \tag{5-2-7}$$

$$n^d = n(1 + \Gamma^{Dirac}) \quad p^d = p(1 + \Gamma^{Dirac}) \tag{5-2-8}$$

e_n^d , e_p^d and n^d , p^d are the modified electron , hole emission rate and concentration for Dirac well.

And the density of state of trap distribution is

$$N_a = gt_t \times \exp(\frac{E - Ec}{KT_t}) + gt_d \times \exp(\frac{E - Ec}{KT_d})$$
$$N_d = gt_t \times \exp(\frac{Ev - E}{KT_t}) + gt_d \times \exp(\frac{Ev - E}{KT_d}) \tag{5-2-9}$$

N_a , N_d : the concentration of the accepter-like, donor-like trap.

gt_d, gt_a : the concentration parameters of the deep state and tail state.

T_t and T_a : the characteristic temperatures of the tail state and deep state.

The donor-like traps act as a Dirac well for electron emission and as a Coulombic well for hole emission. The opposite holds true for the acceptor-like traps.

So, we can get a modified SRH generation equation

$$\mathrm{U} = U_A + U_D \tag{5-2-10}$$

$$U_A = N_A \frac{n_i^2 - n^d p^c}{\dfrac{n^d + n_1}{c_p^c} + \dfrac{p^c + p_1}{c_n^d}} \tag{5-2-11}$$

$$U_D = N_D \frac{n_i^2 - n^c p^d}{\dfrac{n^c + n_1}{c_p^d} + \dfrac{p^d + p_1}{c_n^c}} \tag{5-2-12}$$

$$I = q \int_{\substack{\text{depletion} \\ \text{region}}} U(y)dy \tag{5-2-13}$$

Based on the above equations, we can know that how to get the electric filed in the depletion region is the key point.

In our model, we also introduce empirical electrical field formulas [6]:

$$E = E_1 + E_2 + E_3 \tag{5-2-14}$$

E_1 is the p-n junction electrical field:

$$E_1 = \sqrt{\frac{2qp_{ch}\Phi_D}{\varepsilon_{Si}}} \quad [7] \tag{5-2-15}$$

Φ_D : potential difference in the depletion region.

p_{ch} : accumulation carrier concentration

E_2 and E_3 are the transverse fringing electrical field due to drain to gate potential drop and potential difference between gate and the end of the inversion layer, respectively, as illustrated in Fig. 5-2-1.

$$E_2 = \alpha \times \frac{C_{ox}}{\varepsilon_{si}}(V_d - V_g - V_{fb})$$

$$E_3 = \beta \times \frac{C_{ox}}{\varepsilon_{Si}}(V_g - V_{fb} - \frac{E_g}{q})$$

(5-2-16),(5-2-17)

α and β are fitting parameters.

5.3 Result and discussion

In Lui's model [3], the enhanced factors χ_f, Γ^{Dirac}, and Γ^{Coul}. χ_f is the factors related to the contribution of the Poole-Frenkel effect enhancing pure thermal emission. Γ^{Dirac} and Γ^{Coul} are the factors related to the tunneling probability of electron and hole are trapped in the Dirac well and Coulmbic well.

In previous proposed models, they didn't indicate that how V_{DS}, V_G make effects on the enhanced factor [2], [3]. From our new model, we can observe how the three enhanced factors change when the V_{DS} and V_G are varied. In Fig. 5-3-1, when V_{DS} is varied between 1~10V, Γ^{Coul} is the dominated factor. Under low V_{DS} condition, the χ_f is lager than Γ^{Dirac}, however under high V_{DS} condition, the χ_f is lower than Γ^{Dirac}.

In Fig. 5-3-2, under low Vg condition, the dominated factor is Γ^{Coul}. When the gate bias V_G increased, the Γ^{Coul} and Γ^{Dirac} decreased rapidly, so in higher Vg condition, the χ_f will be the dominated factor. Via the enhanced factors, we may directly predict which mechanism will dominate the leakage current.

The parameters α and β are the only two artificial factors in our model. By modulating these two parameters, we can pursue the electric field values approach to the real electric field system. Parameter α is related to the drain to gate potential

drop, so the V_{DS} and V_G dependence of the electric field will be influenced when changing the value of α . In the other hand, the parameter β is only related to the potential difference between gate and the end of the inversion layer. Therefore, only the V_G dependence of the electric field will be influenced when changing the value of β. By adjusting this two parameters, we can calibrate our model to the real measured electrical characteristics. In fig. 5-3-3, the leakage current versus gate voltage for different values of parameter α is presented. We can see that the leakage current apparently rise when α increases. In fig. 5-3-4, the Leakage current versus gate voltage (at $V_{DS} = 5V$) for different values of the parameter β is presented. Only little V_G dependence of the leakage current is observed when the parameter β is adjusted.

Form Fig. 5-3-5, we can know that for donor-like trap, when E_t is near the E_c, the χ_f is dominated, Γ_n^{coul} will be vanished, and Γ_p^{dirac} is lower than χ_f. It is because the barrier lowing resulting from the Poole Frenkel effect cause the electron can directly thermal generate from the trap state. So, near the tail state, the Γ_n^{coul} will be vanished, and χ_f is important. But for acceptor-like trap when near the E_v, because the electron effective mass is smaller, thus, from Fig. 5-3-6 we can see that Γ_n^{dirac} is lager than χ_f.

With the aid of our new model, we may predict the leakage current with only two fitting parameters. We also compare the model with the measured data. We found that the model was good agreed with the result. The fitting result is shown in Fig. 5-3-7 and the parameter set used in our model is listed in Table 5-3-1.

5.4 Conclusion

A new leakage current model with fewer fitting parameters has been presented. We build up a leakage current model which is composed of Lui's generation-recombination model, determination of the density of state in the band gap and using the pseudo-two dimension method to solve the electrical field near the drain side and the depletion region width. The physical-based electric field model is composed of three parts. We only have to adjust α and β then can get the accurate the leakage current and obtain how the drain voltage V_{DS} and gate voltage V_G influencing the leakage current.

Chapter 6

Conclusions

In this work, the high electric field effect has been studied in whole operation regime. Some kinds of kink effect and short channel mechanisms were separately investigated in chapter 2. The condition of samples which split to different re-crystallized process, various hydrogen-passivation time and operating at different temperature. Through the first two conditions we find that the smaller grain size and shorter hydrogen-passivation time devices exhibit better kink effect suppressing ability than the larger ones. And through different temperature we can postulate that in low gate voltage regime the DIGBL effect dominates the multiplication factor and in high gate voltage regime the impact ionization is predominant.

In chapter 3, we propose our semi-empirical numerical drain induced barrier lowering current and the impact ionization model which involves the modified trap relative threshold energy. The carrier transport in partially-depleted poly-Si film can be described by the thermionic emission over the symmetric Schottky barriers and includes the drain induced barrier lowering (DIGBL) effect. Furthermore, the threshold energy was modified by considering the trap state distribution and the DIGBL effect.

In chapter 4, a physical subthreshold model of poly-silicon TFTs with parasitic BJT effect is proposed. This model evaluated body potential by approaching to a balance among various current components in the TFT and parasitic BJT systems. After considering the trap density in the active film, the surface potential can be derived exactly. With a simple gradual channel approximation, we can obtain the subthreshold diffusion current from this surface potential banding. Further

considering a multiplication behavior in the impact ionization effect, those parasitic BJT current components can be obtained more accurately.

In chapter 5, a new leakage current model with fewer fitting parameters has been presented. We build up a leakage current model which is composed of Lui's generation-recombination model, determination of the density of state in the band gap and using the pseudo-two dimension method to solve the electrical field near the drain side and the depletion region width. The physical-based electric field model is composed of three parts. We only have to adjust α and β then can get the accurate the leakage current and obtain how the drain voltage V_{DS} and gate voltage V_G influencing the leakage current.

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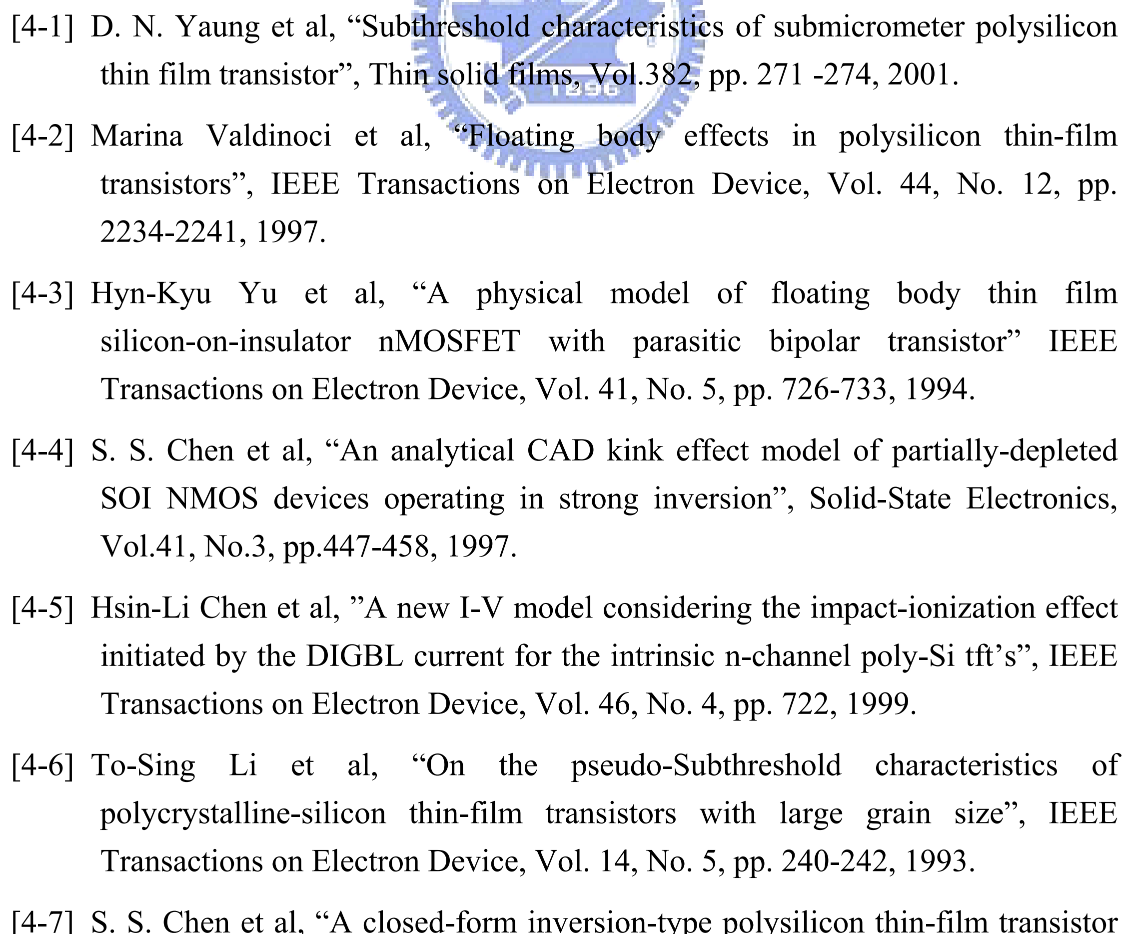

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