Chapter 2

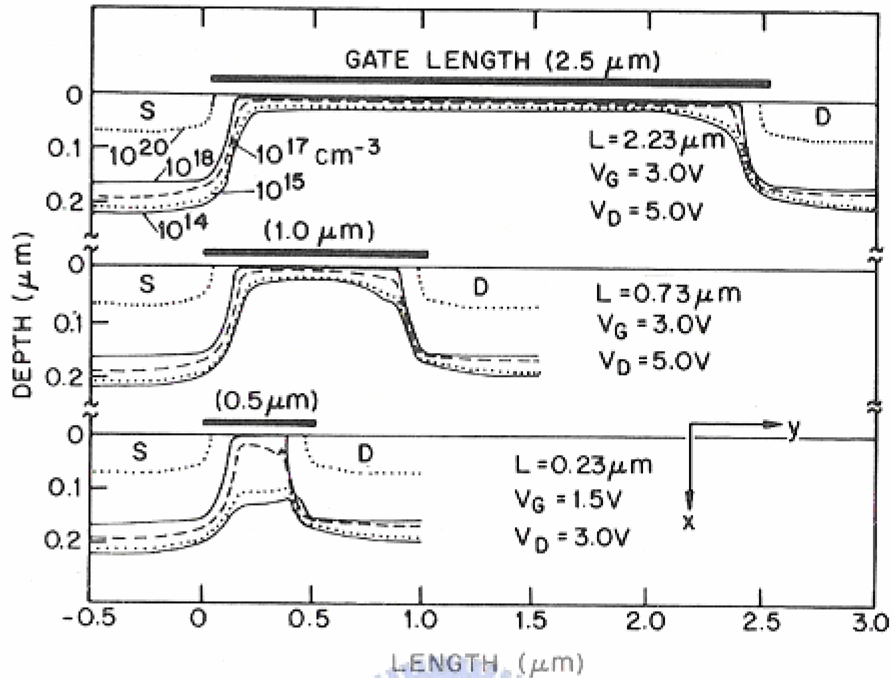


Fig. 2-1-1 The punch-through effect would become more obvious as the gate length shrinks to 0.5μm [12].

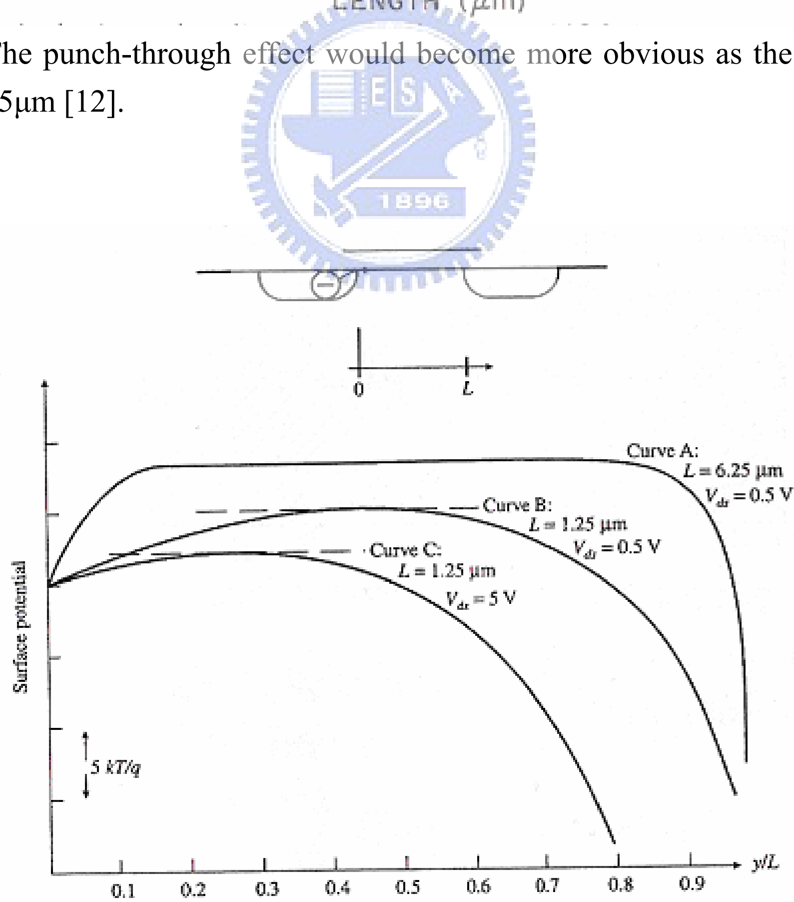


Fig. 2-1-2 The drain induced barrier lowering effect with different gate lengths and drain bias [13].

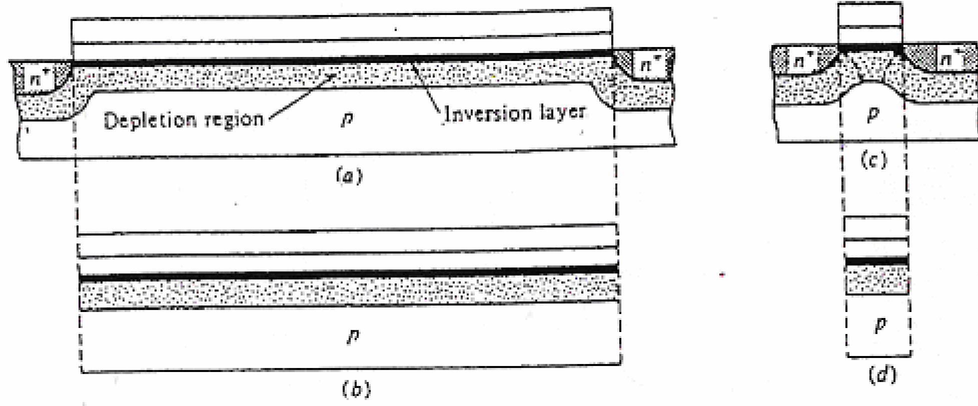


Fig. 2-1-3 The charge sharing effect would pronounce only at small device dimension [13].

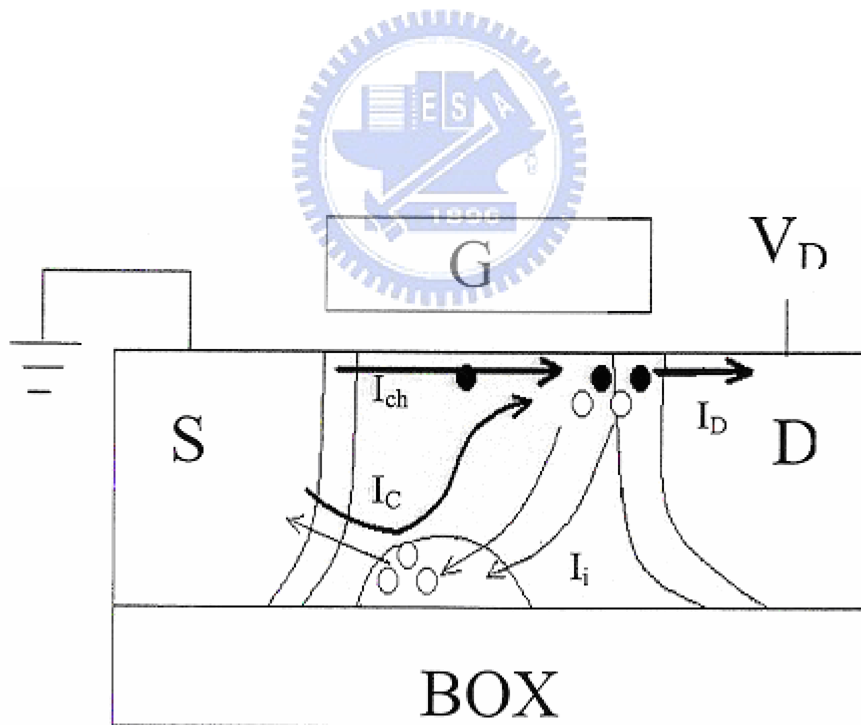


Fig. 2-1-4 The floating body effect in TFTs.

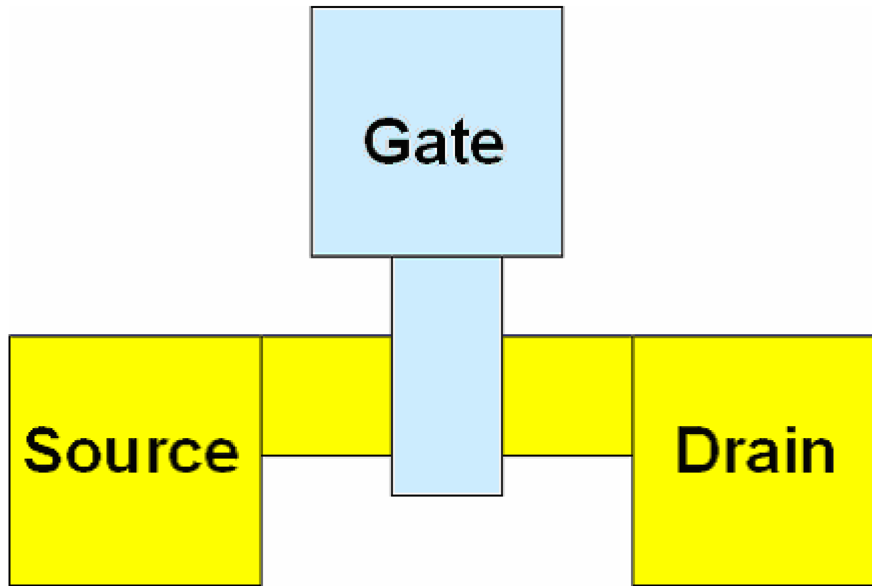


Fig. 2-2-1 The top-view of the device which is used in our study.

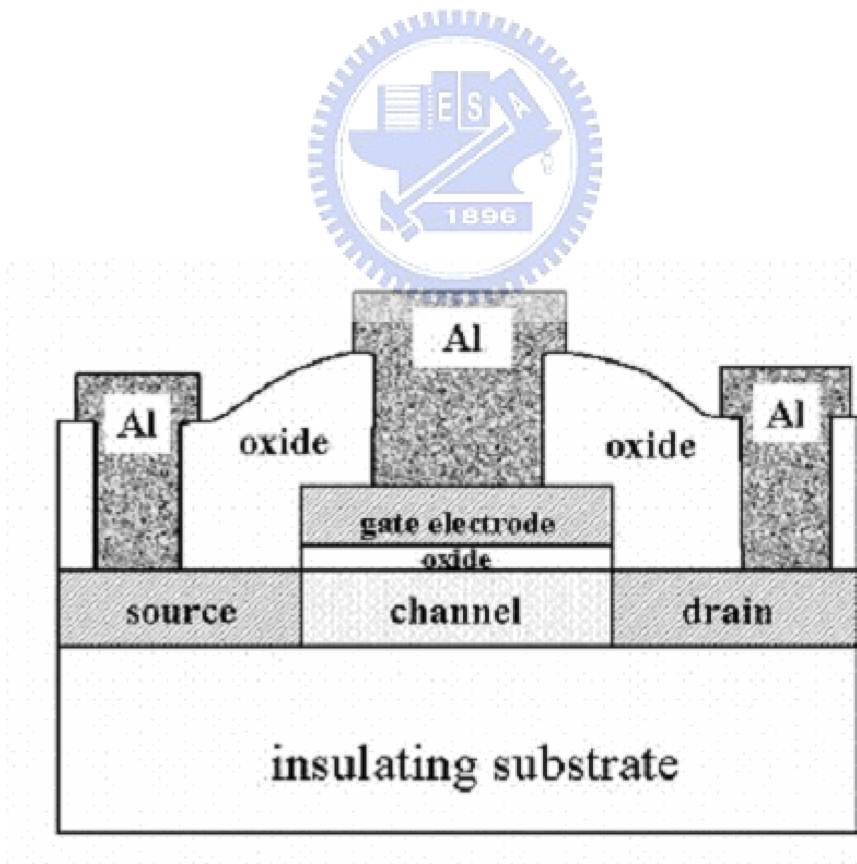


Fig. 2-2-2 Schematic cross-sectional view of devices with conventional top-gate structure.

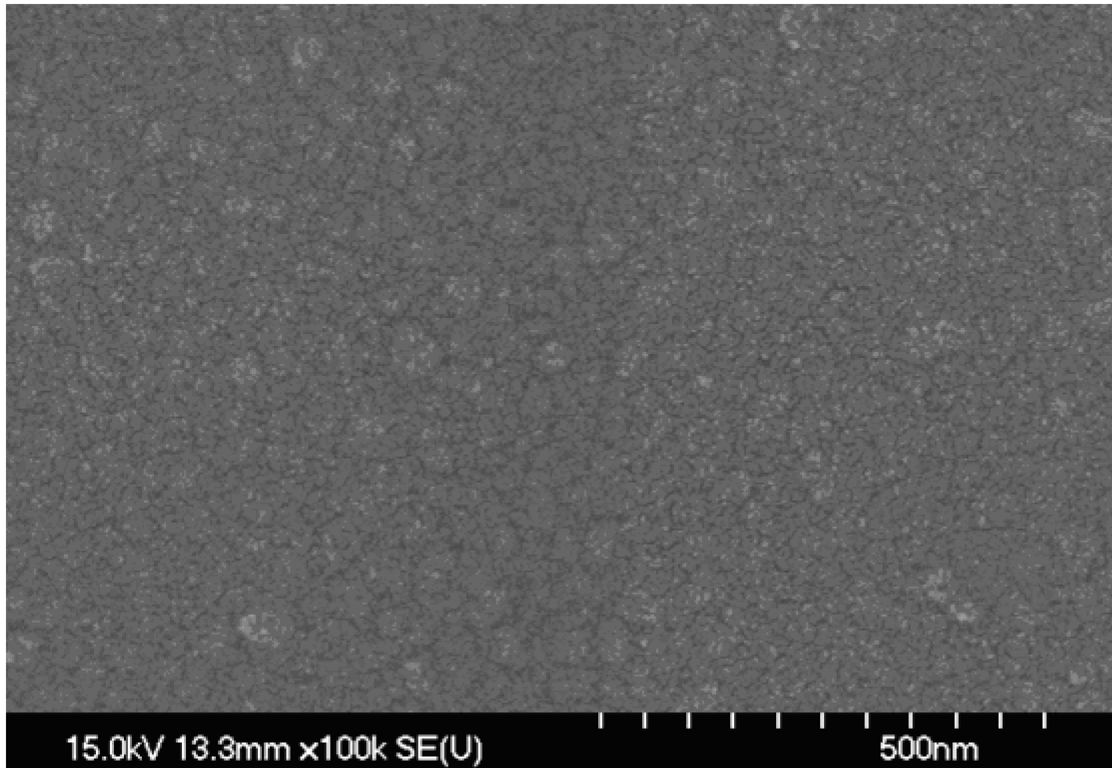


Fig. 2-2-3 The SEM picture of as-deposited poly-silicon film.

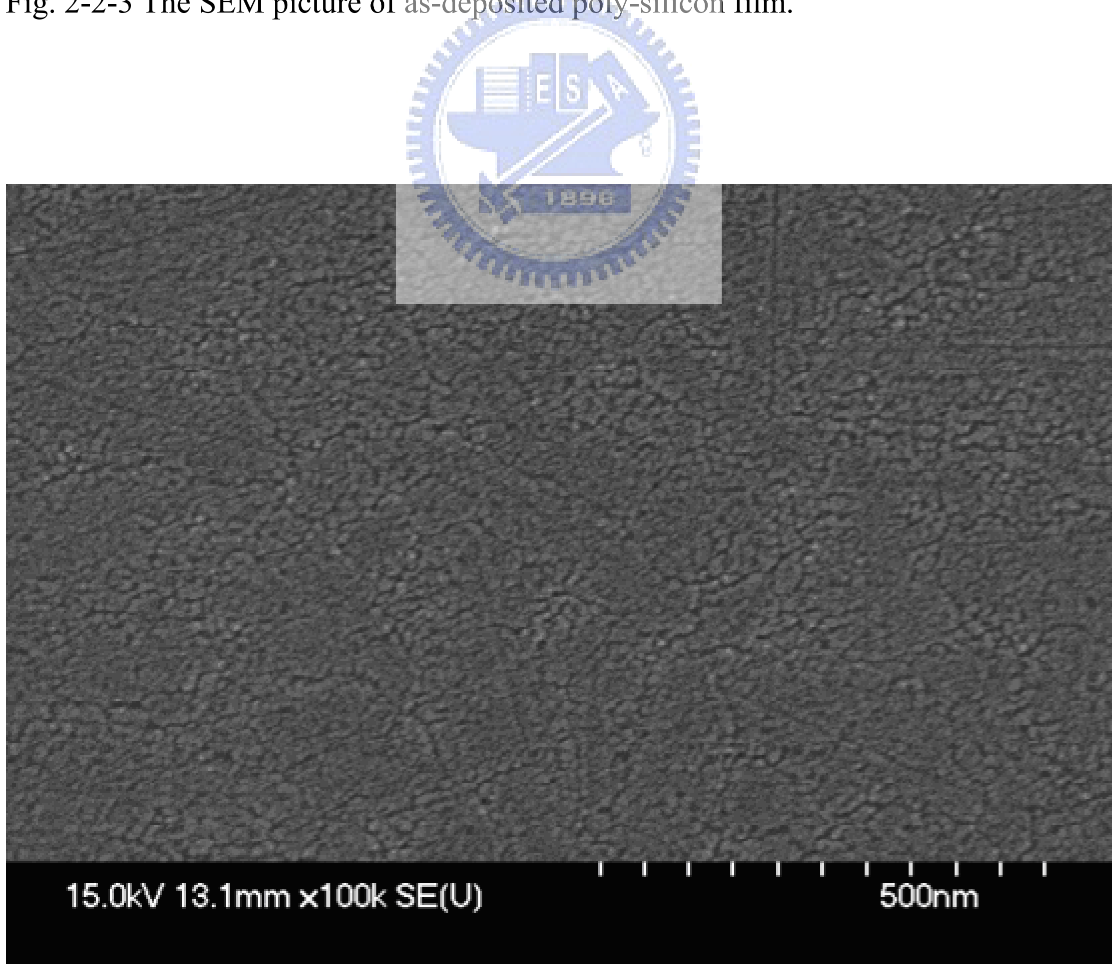


Fig. 2-2-4 The SEM picture of SPC poly-silicon film.

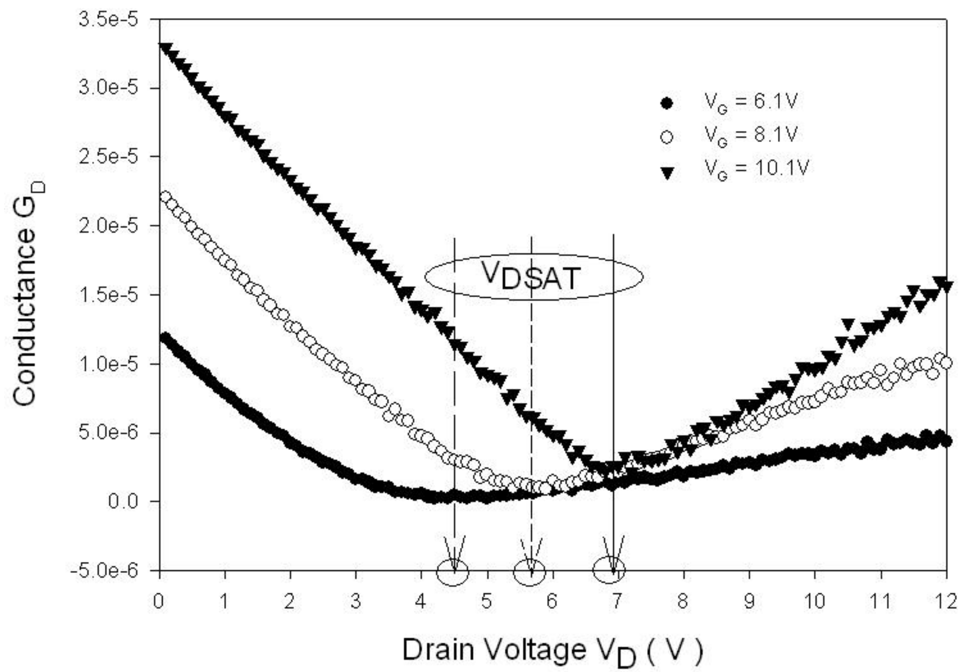


Fig. 2-3-1 Each saturation voltage at various gate voltages can be defined from the "first" minimum points of the conductance.

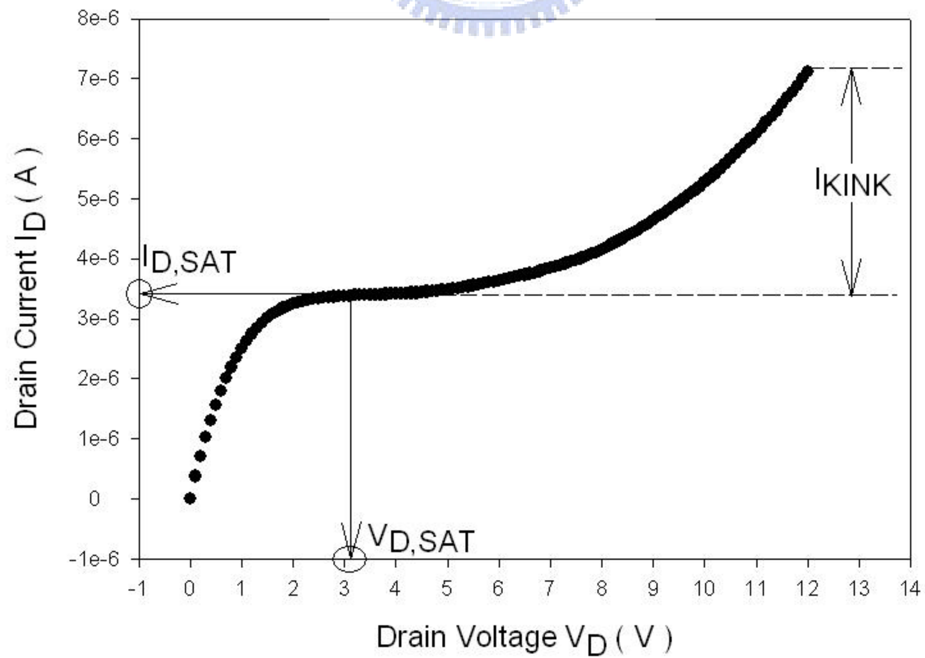
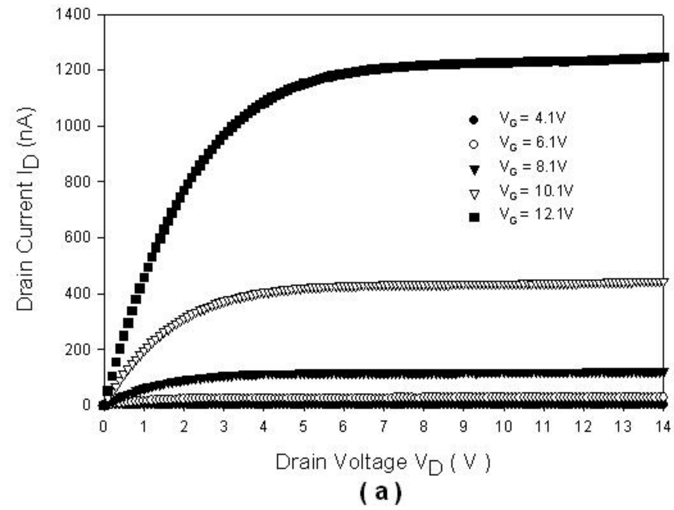
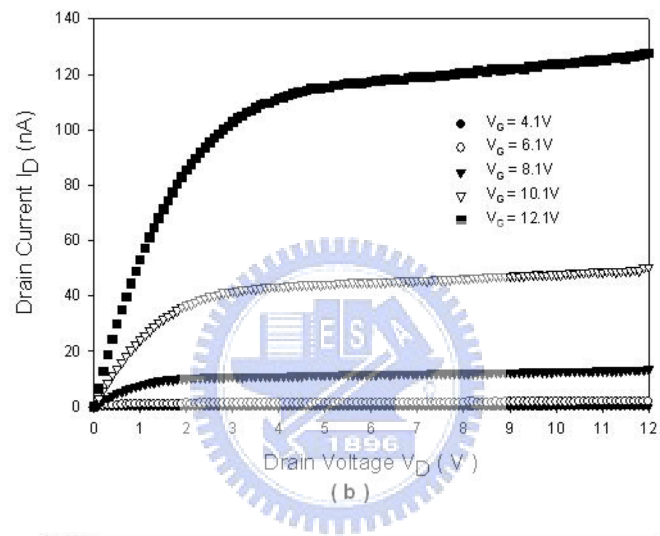


Fig. 2-3-2 The kink current I_{KINK} can be evaluated by using the drain current at high drain voltage to minus the saturation current, such that $I_{KINK} = I_{DS}\text{-}I_{D,SAT}$.





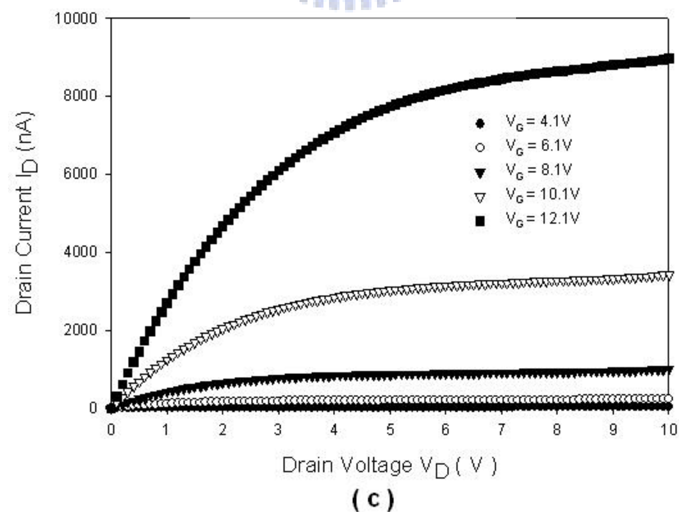
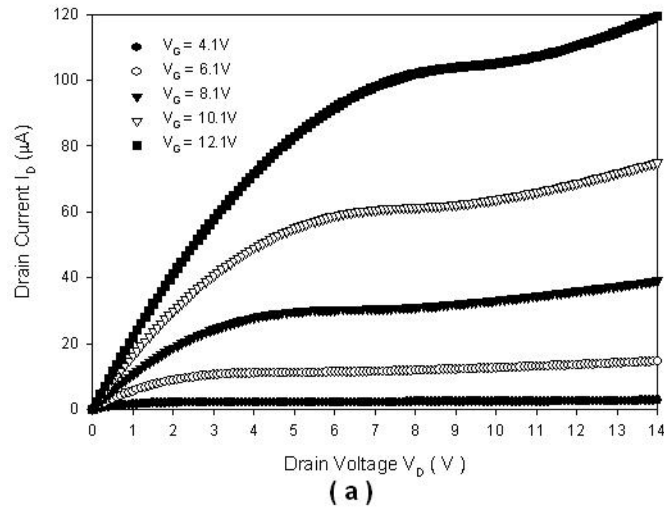
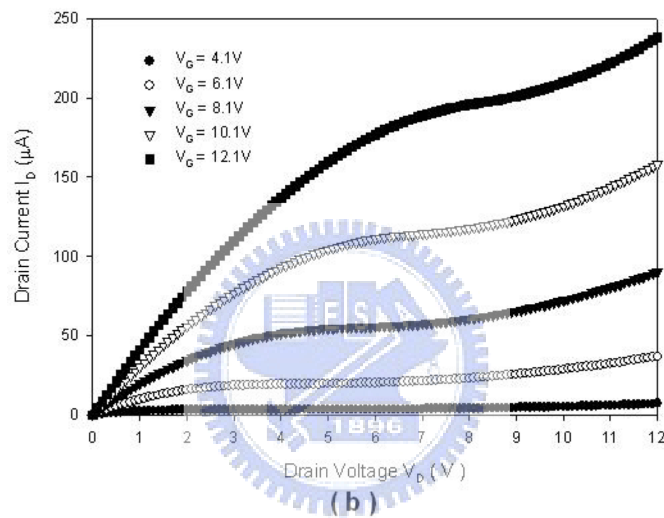


Fig. 2-3-3 I_D-V_D characteristics for as-deposit. and two hours NH_3-passivation time n-channel poly-Si TFTs with various channel lengths: (a) L = 10μm, (b) L = 5μm (c) L = 2μm. The channel width W is kept as 10μm.





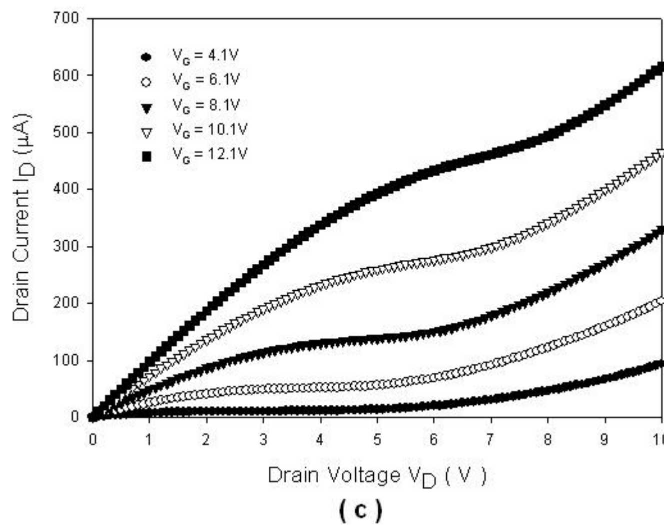
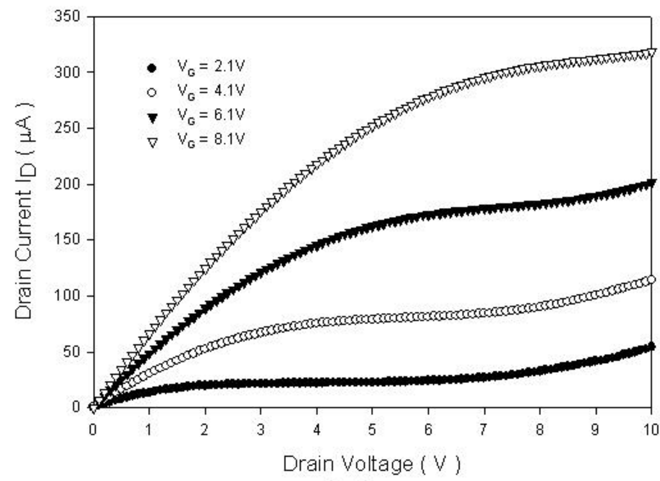
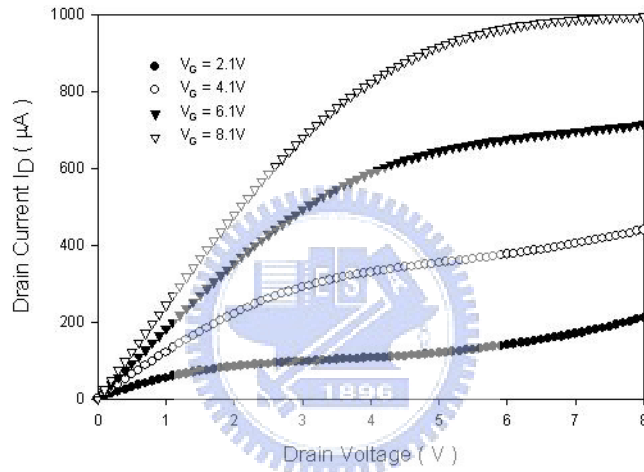


Fig. 2-3-4 I_D-V_D characteristics for SPC and two hours NH_3-passivation time n-channel poly-Si TFTs with various channel lengths: (a) L = 10μm, (b) L = 5μm (c) L = 2μm. The channel width W is kept as 10μm.





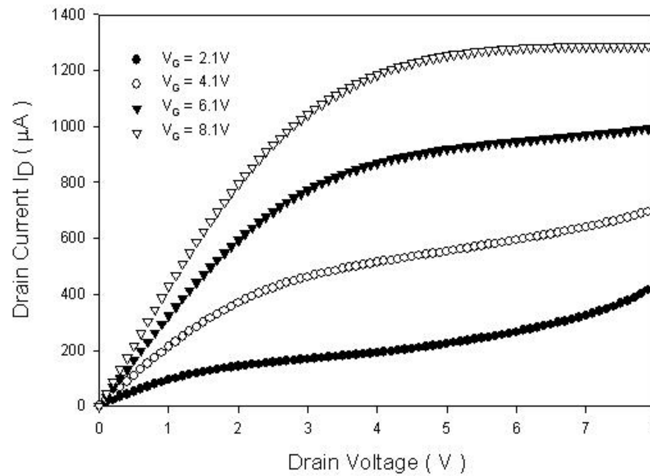


Fig. 2-3-5 I_D-V_D characteristics for ELA n-channel poly-Si TFTs with various channel lengths: (a) L = 13.5μm (b) L = 4.5μm (c) L = 3.5μm. The channel width W is kept as 12μm.

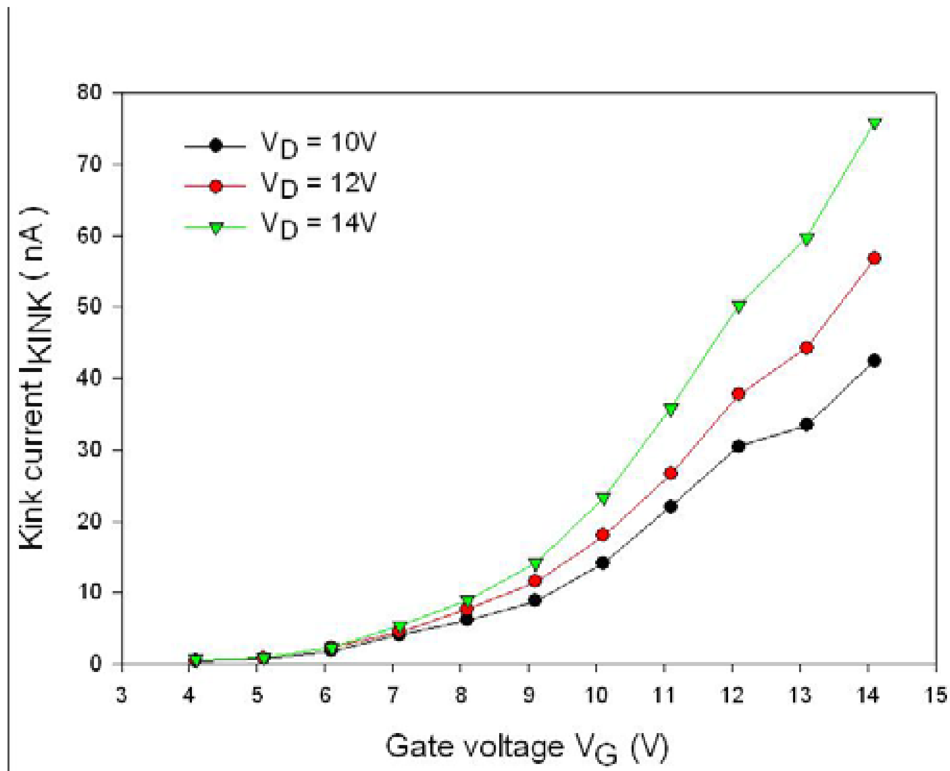


Fig. 2-3-6(a) The extracted excess kink current versus the gate voltage with different drain voltage. As-deposited, 2hr NH_3-passivation time and W/L = 10/10 (μm).

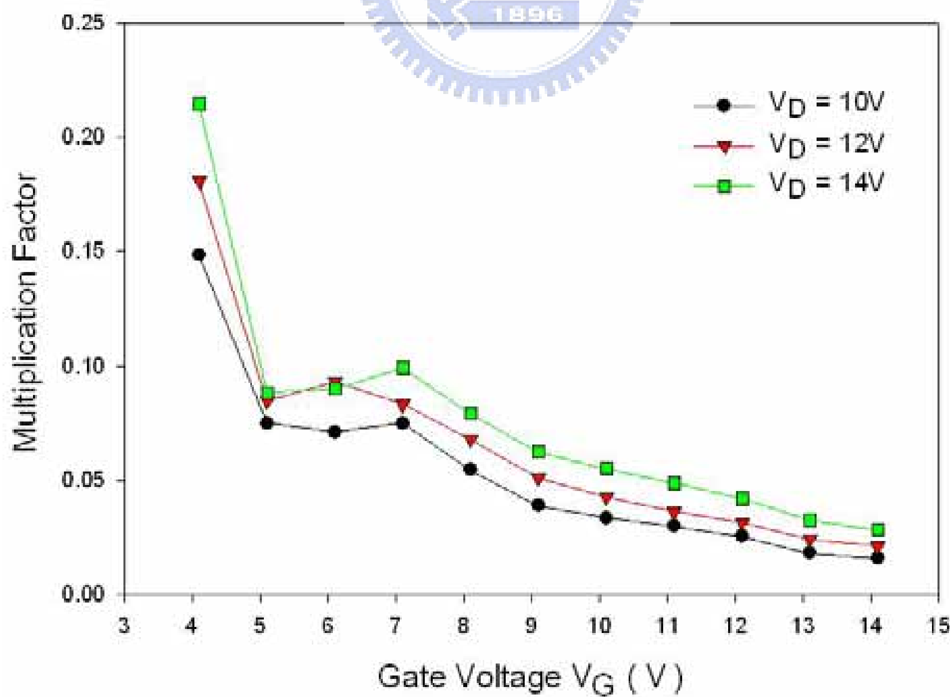


Fig. 2-3-6(b) The multiplication factor versus the gate voltage with different drain voltage. As-deposited, 2hr NH_3-passivation time and W/L = 10/10 (μm).

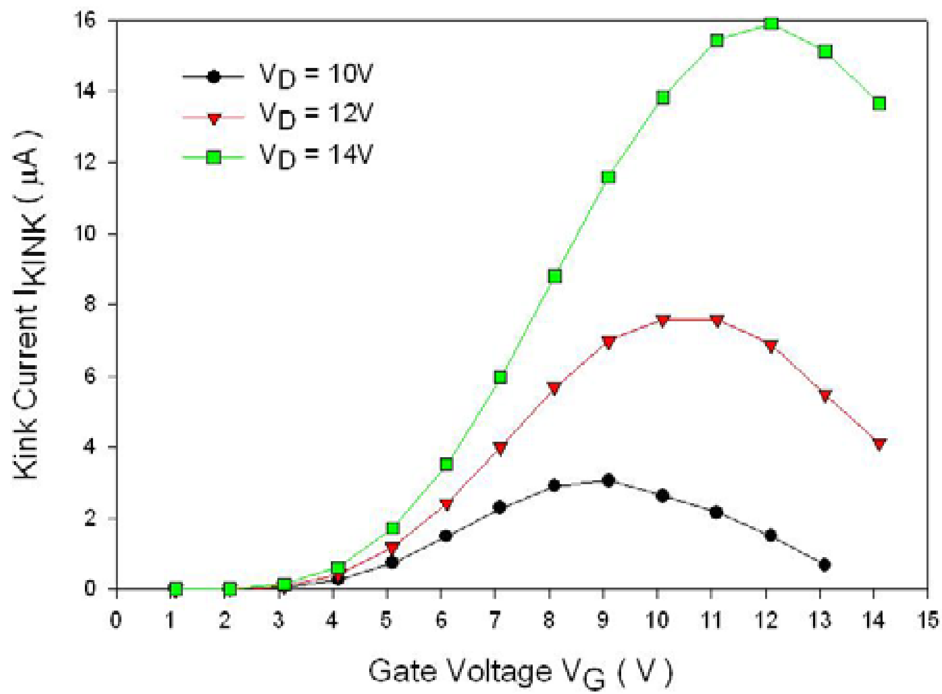


Fig. 2-3-7(a) The extracted excess kink current versus the gate voltage with different drain voltage. SPC, 2hr NH_3-passivation time and W/L = 10/10(μm).

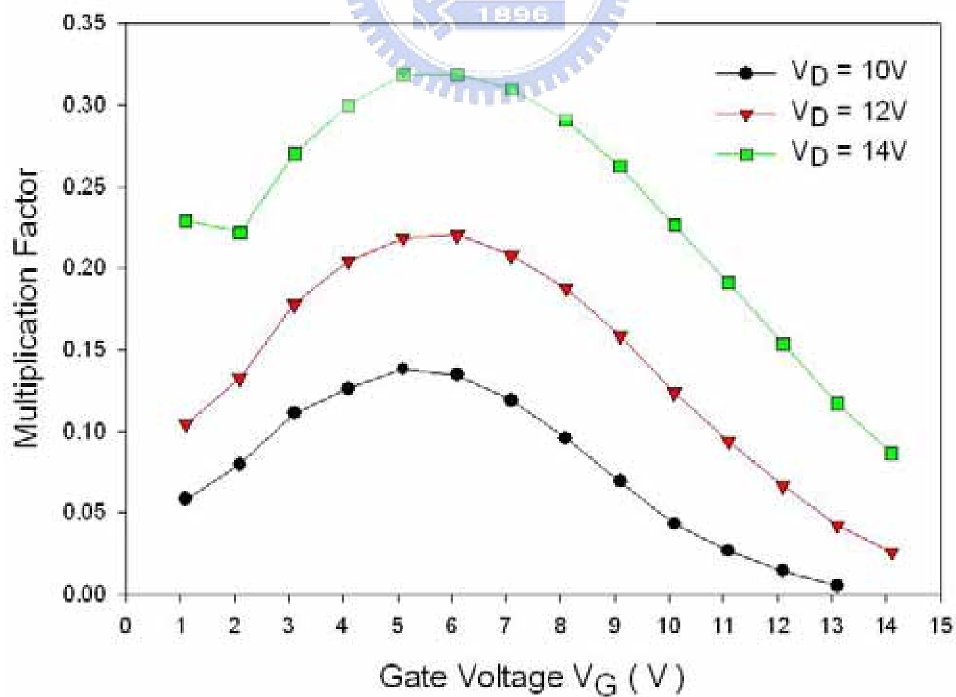


Fig. 2-3-7(b) The multiplication factor versus the gate voltage with different drain voltage. SPC, 2hr NH_3-passivation time and W/L = 10/10 (μm).

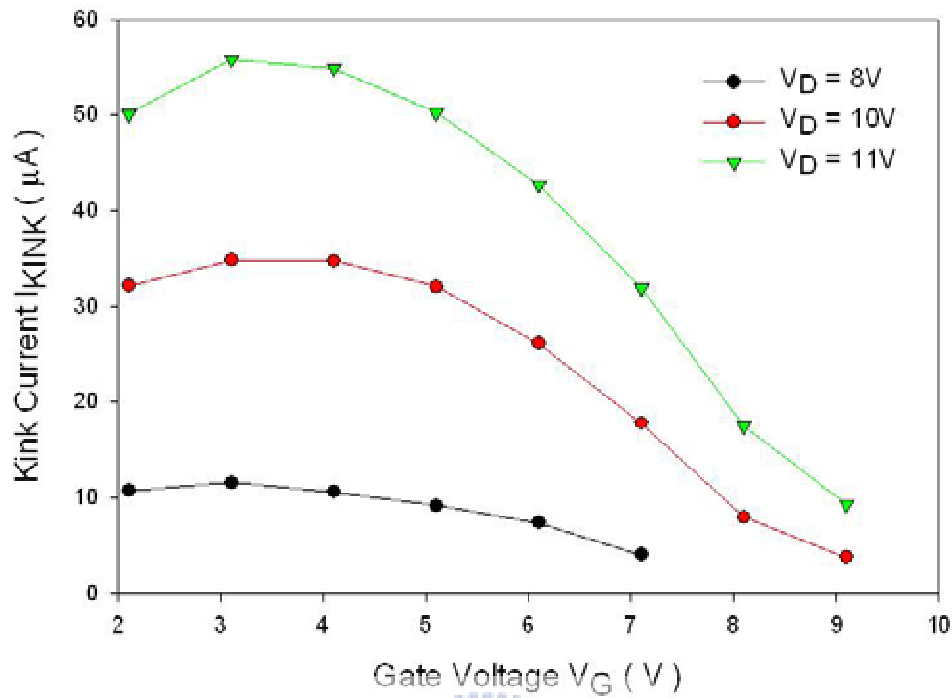


Fig.2-3-8(a) The extracted excess kink current versus the gate voltage with different drain voltage. ELA, 2hr NH_3-passivation time and W/L = 13.5/12 (μm).

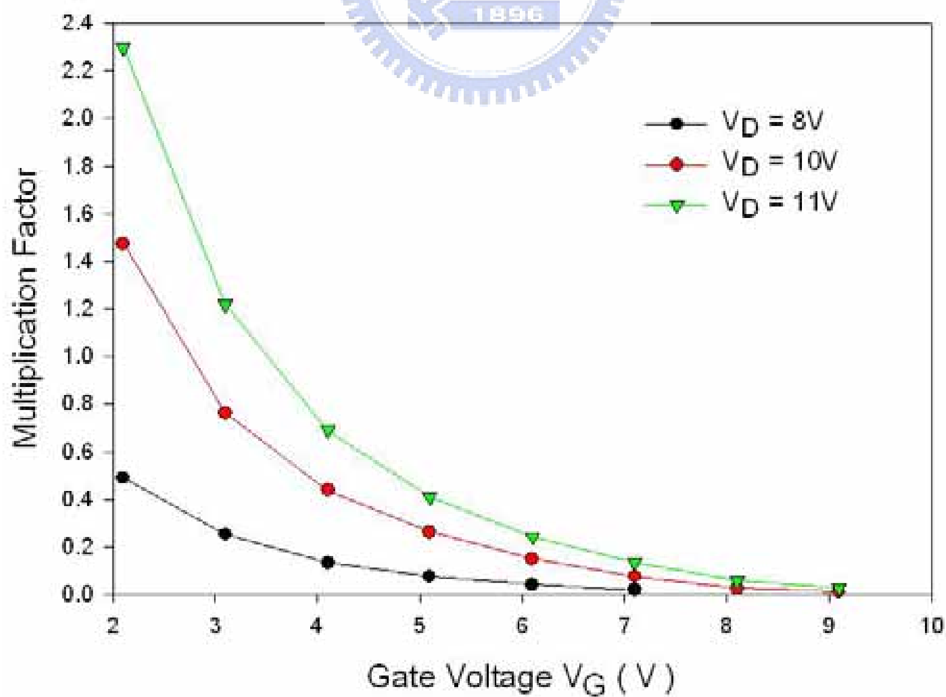


Fig.2-3-8(b) The multiplication factor versus the gate voltage with different drain voltage. ELA, 2hr NH_3-passivation time and W/L = 13.5/12 (μm).

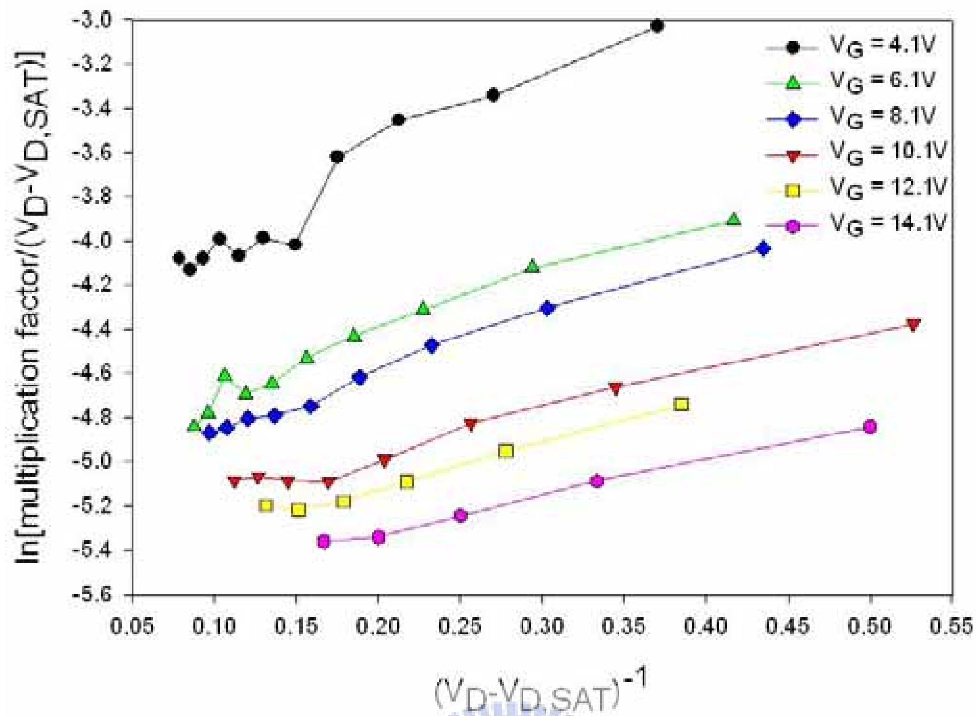


Fig. 2-3-9(a) Threshold energy extracted figure form empirical ionization rate. As-deposited, 2hr NH_3-passivation time and W/L = 10/10 (μm).

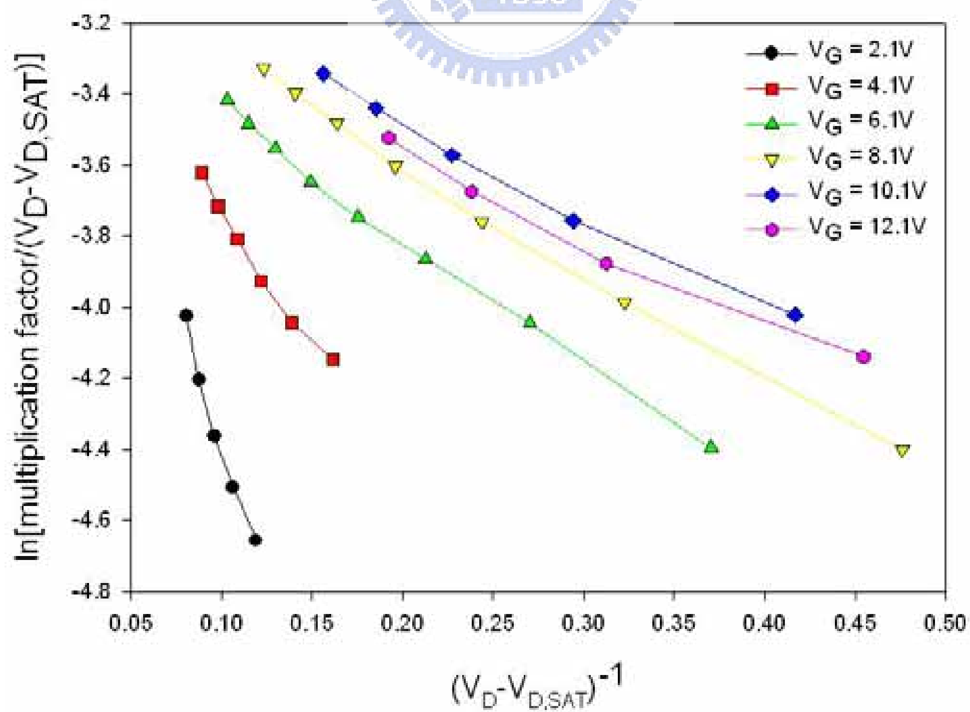


Fig. 2-3-9(b) Threshold energy extracted figure form empirical ionization rate. SPC, 2hr NH_3-passivation time and W/L = 10/10 (μm).

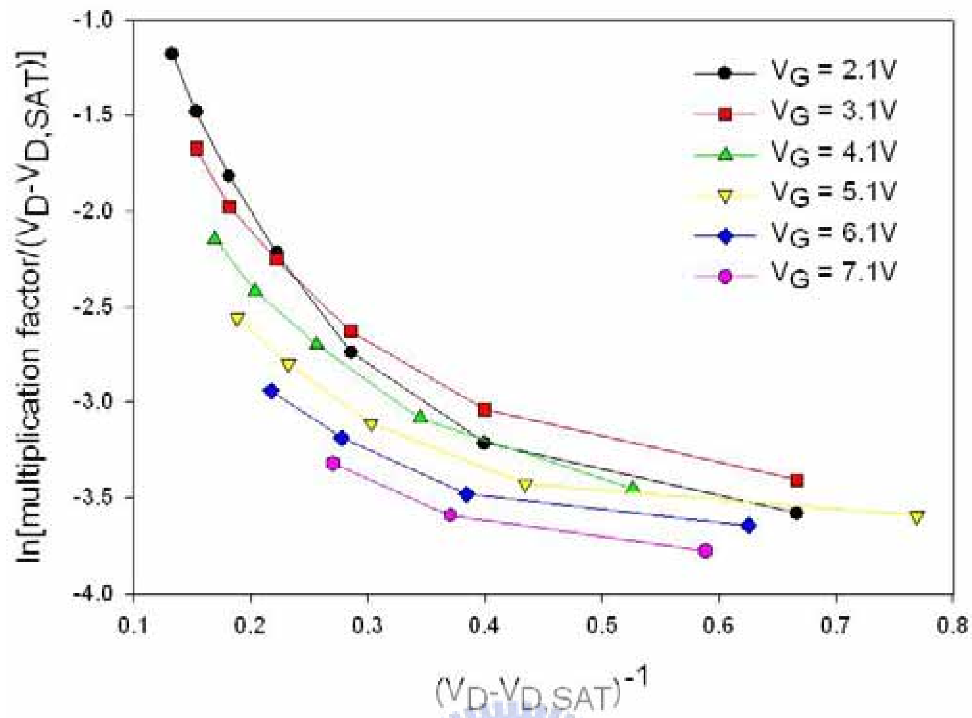


Fig. 2-3-9(c) Threshold energy extracted figure form empirical ionization rate. ELA, 2hr NH_3-passivation time and W/L = 13.5/12 (μm).

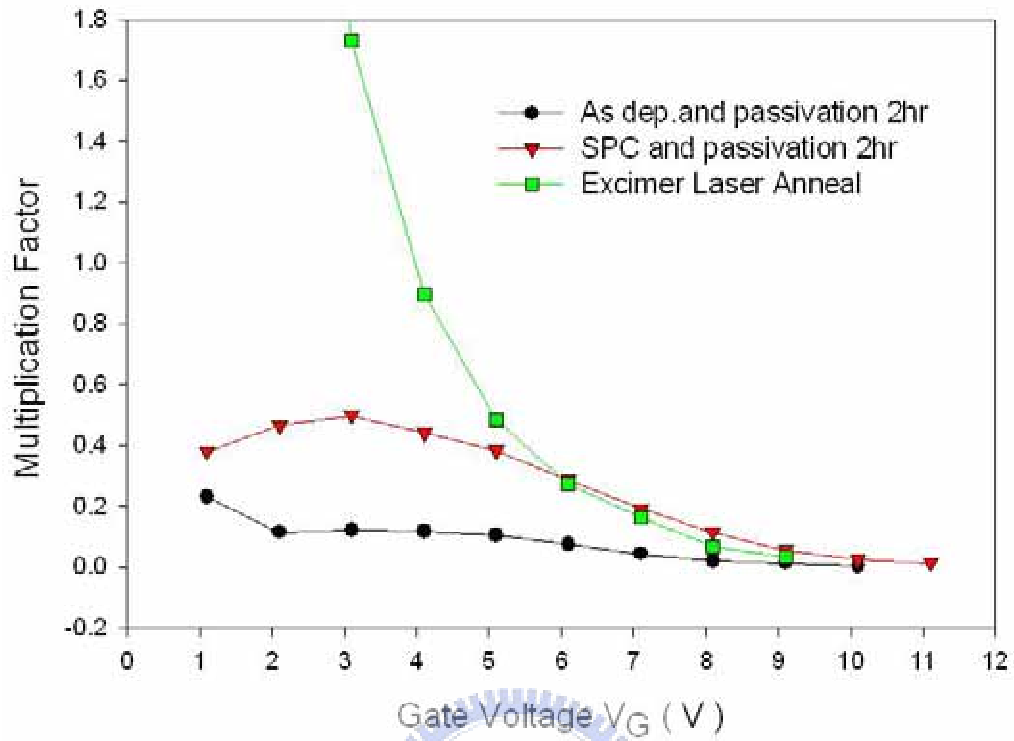


Fig. 2-3-10 Multiplication factor for n-channel poly-Si TFTs with different film re-crystallized process. The channel length and width are both 5μm.

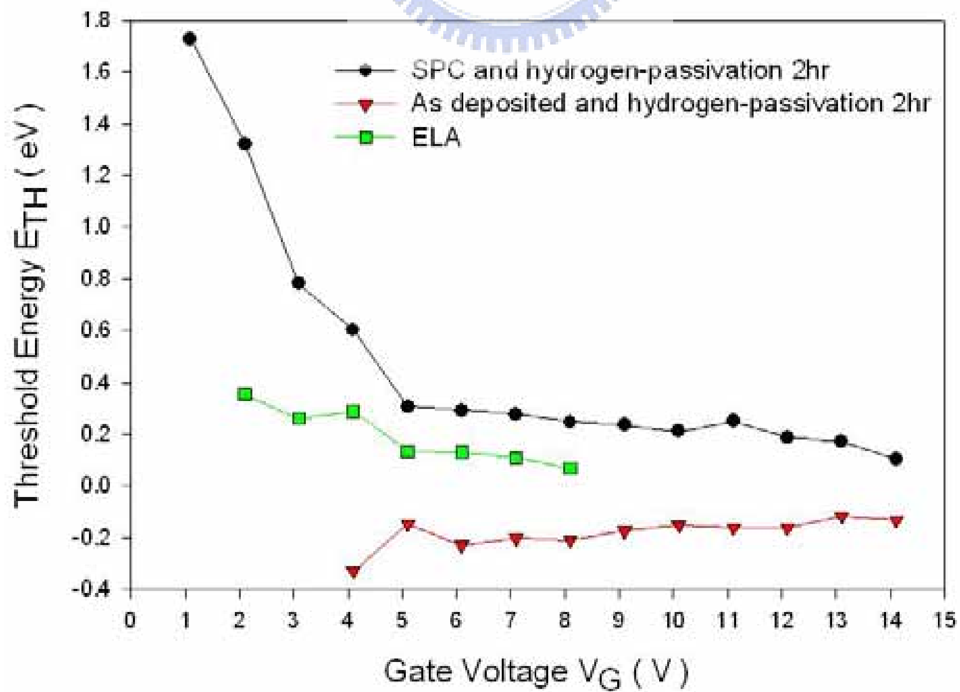


Fig. 2-3-11 Threshold energy for n-channel poly-Si TFTs with different film re-crystallized process.

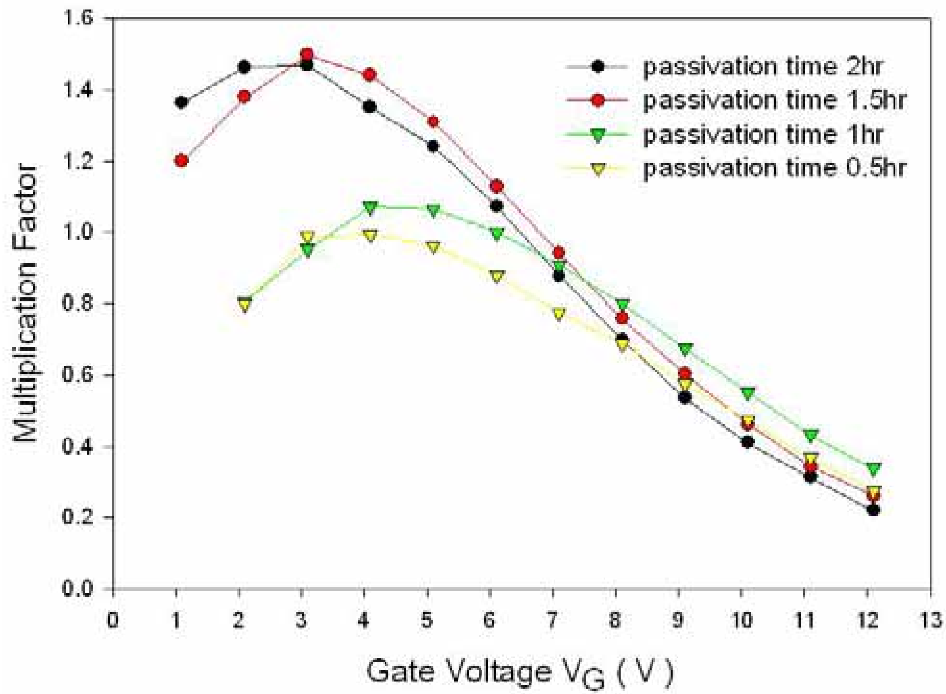


Fig. 2-3-12 Multiplication factor versus gate voltage with different NH_3-passivation time. SPC and the channel length is 5μm and width is 10μm.

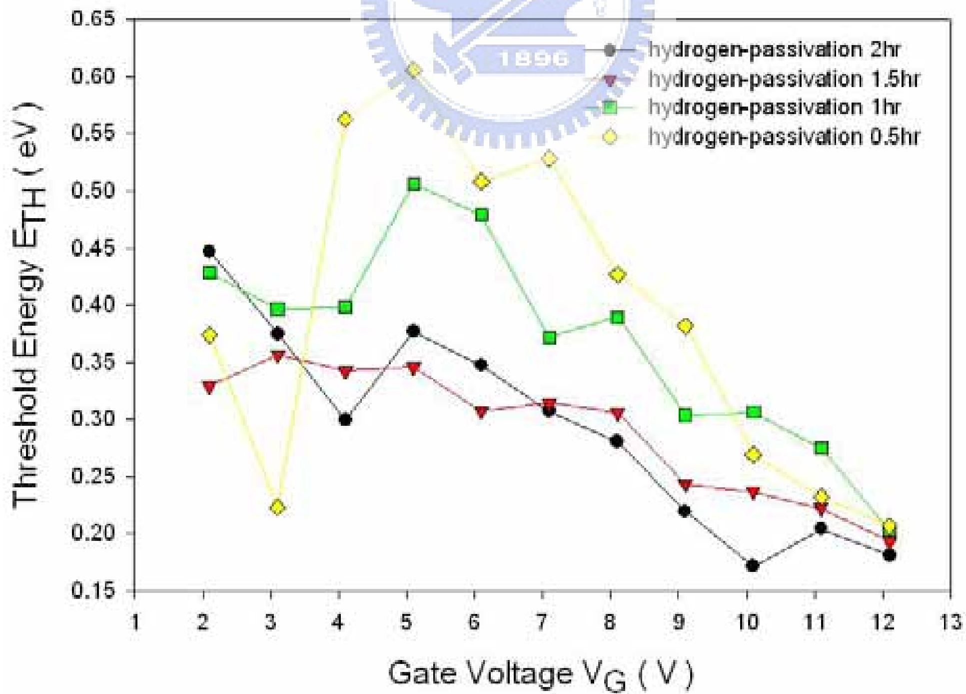


Fig. 2-3-13 Threshold energy versus gate voltage with different NH_3-passivation time. SPC and the channel length is 5μm and width is 10μm.

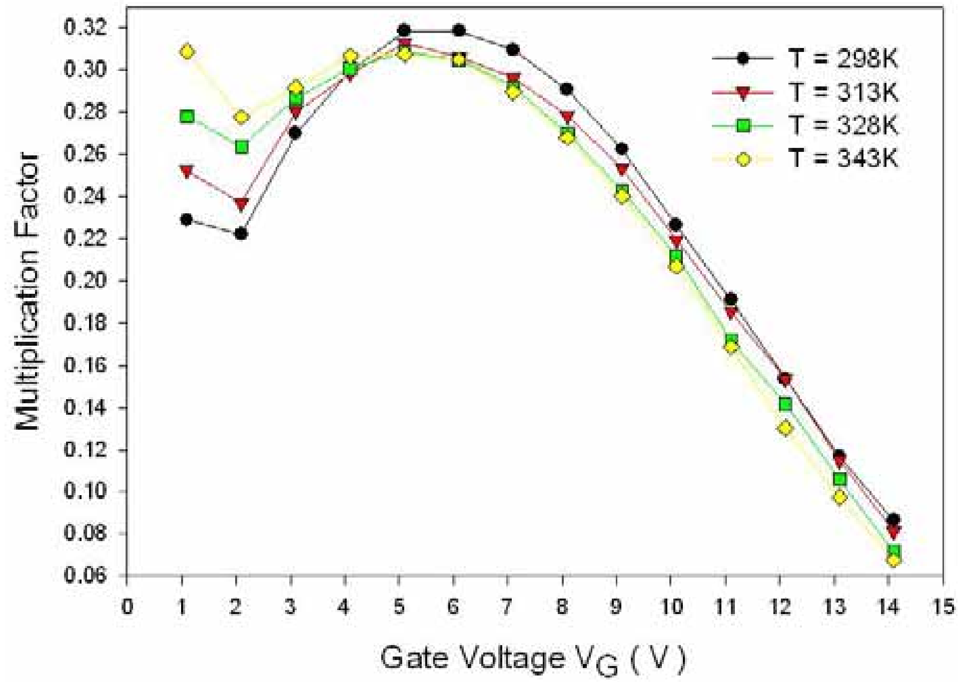


Fig. 2-3-14 Multiplication factor vs. gate voltage under different ambient temperature. SPC, 2hr NH_3-passivation, and channel length and width are both 10μm.

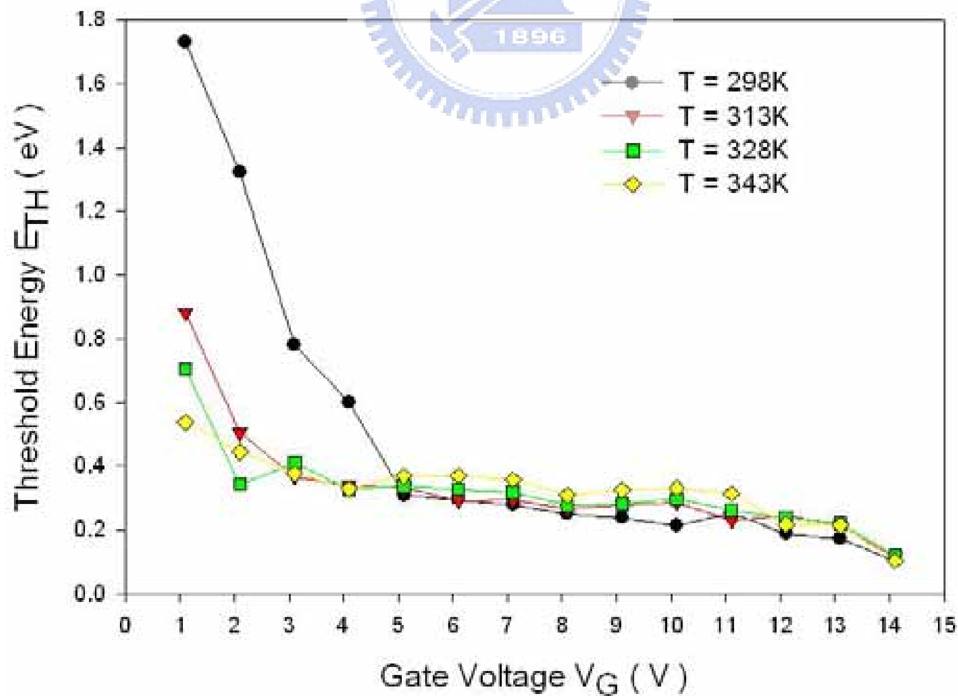


Fig. 2-3-15 Threshold energy vs. gate voltage under different ambient temperature. SPC, 2hr NH_3-passivation, and channel length and width are both 10μm.

Chapter 3

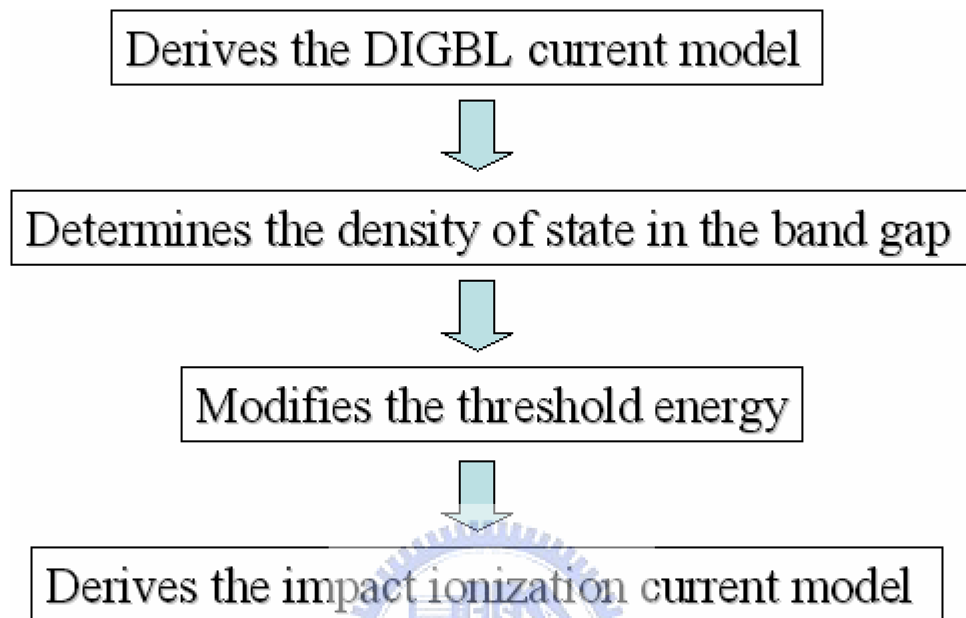


Fig. 3-0-1 The model derivation flow.

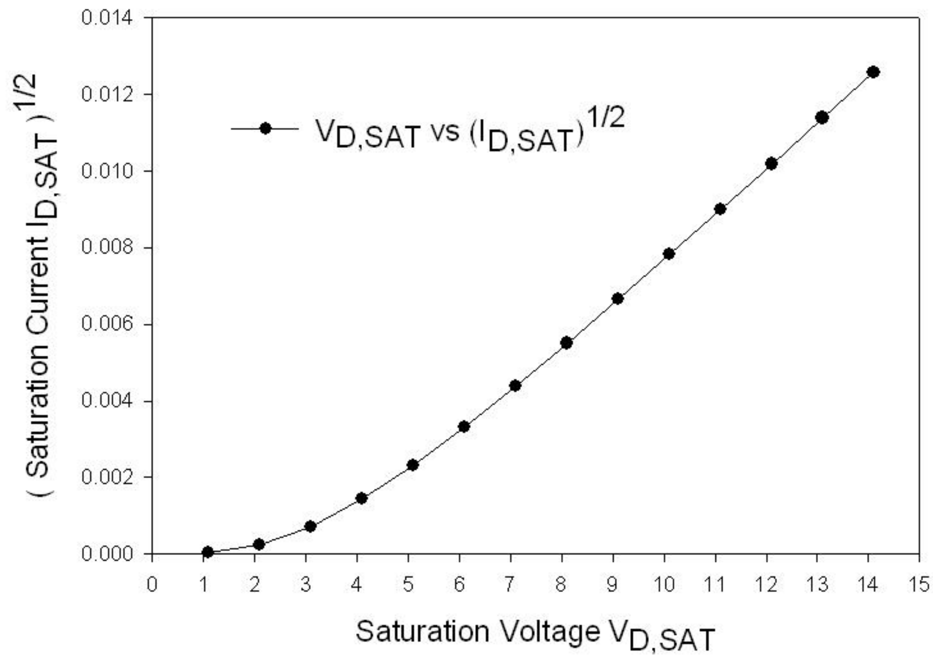


Fig. 3-1-1 The relationship between saturation voltage and the square root of saturation current is traced on one straight line means that the saturation point occurs due to the conduction channel collapses.

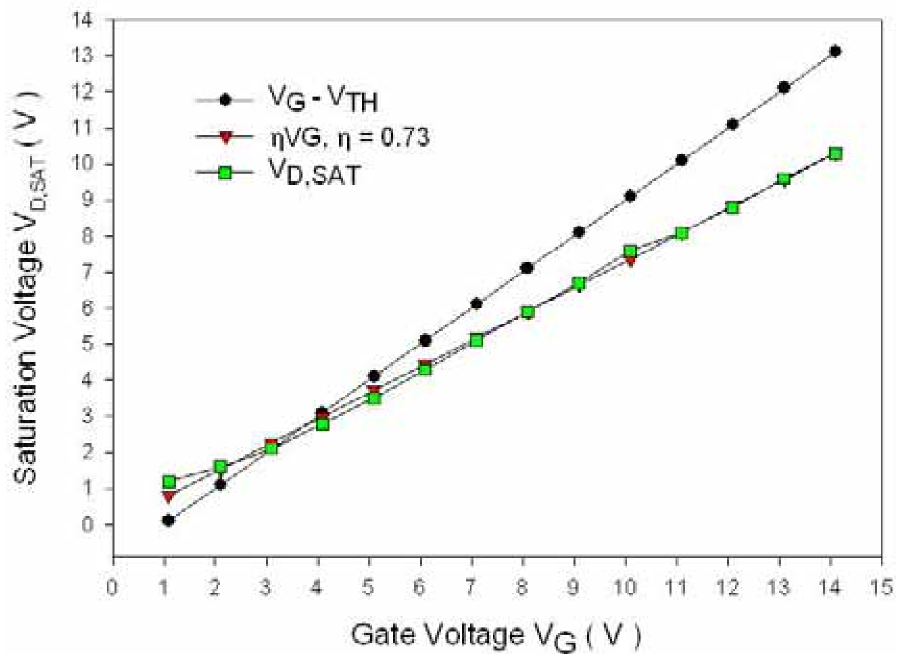


Fig. 3-1-2 The saturation voltage $V_{D,SAT}$ and V_G-V_{TH} versus the gate voltage V_G.

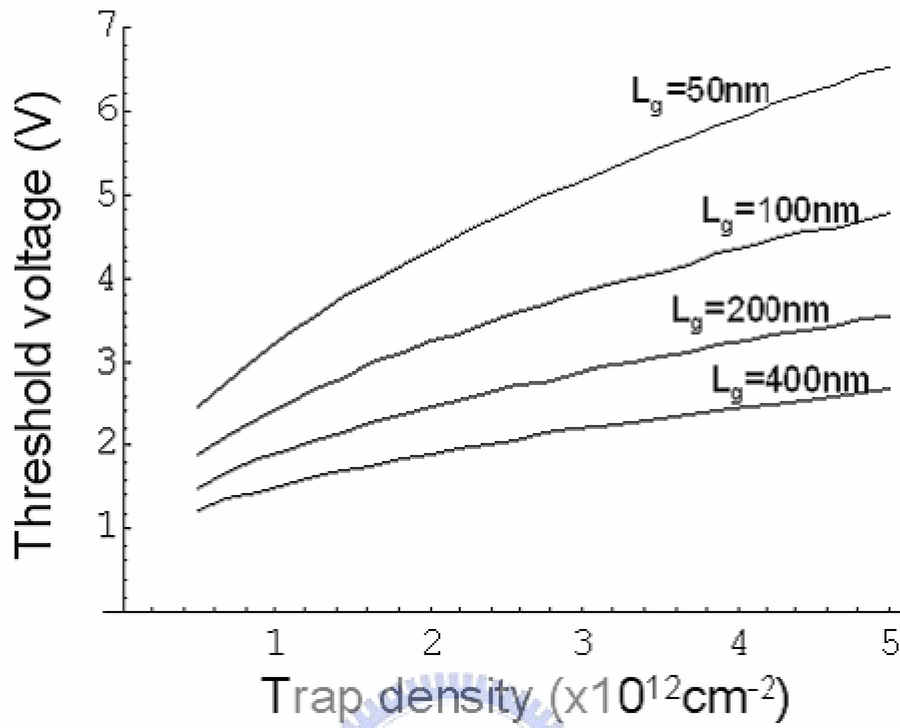


Fig. 3-1-3 The threshold voltage increases with increasing trap density and decreasing grain size.

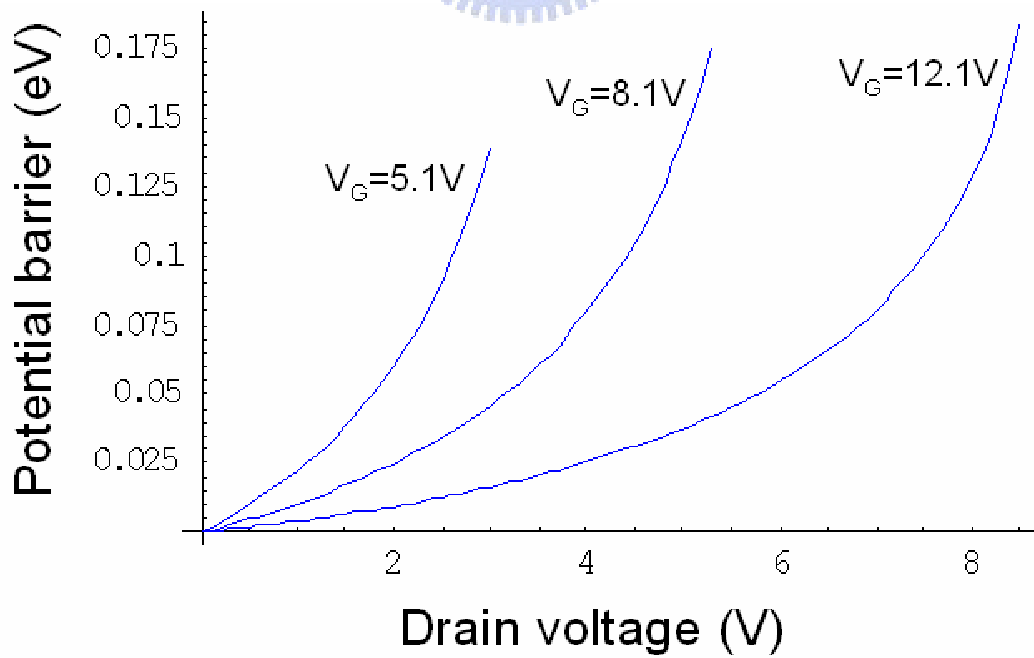


Fig. 3-1-4 Calculated potential barrier height which involves the drain induced barrier lowering effect.

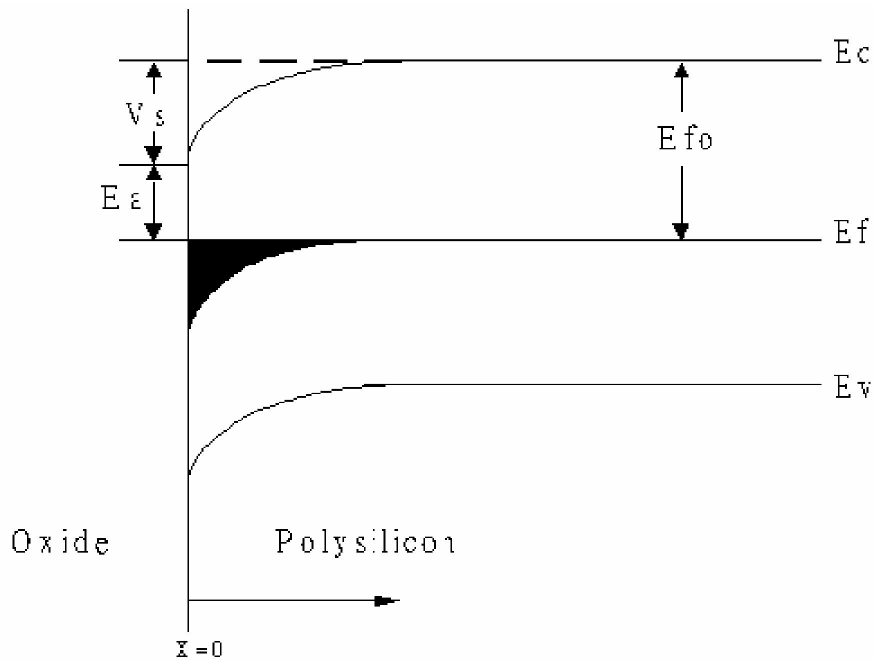


Fig. 3-2-1 The band bending along the x axis at the SiO_2 and polysilicon interface.

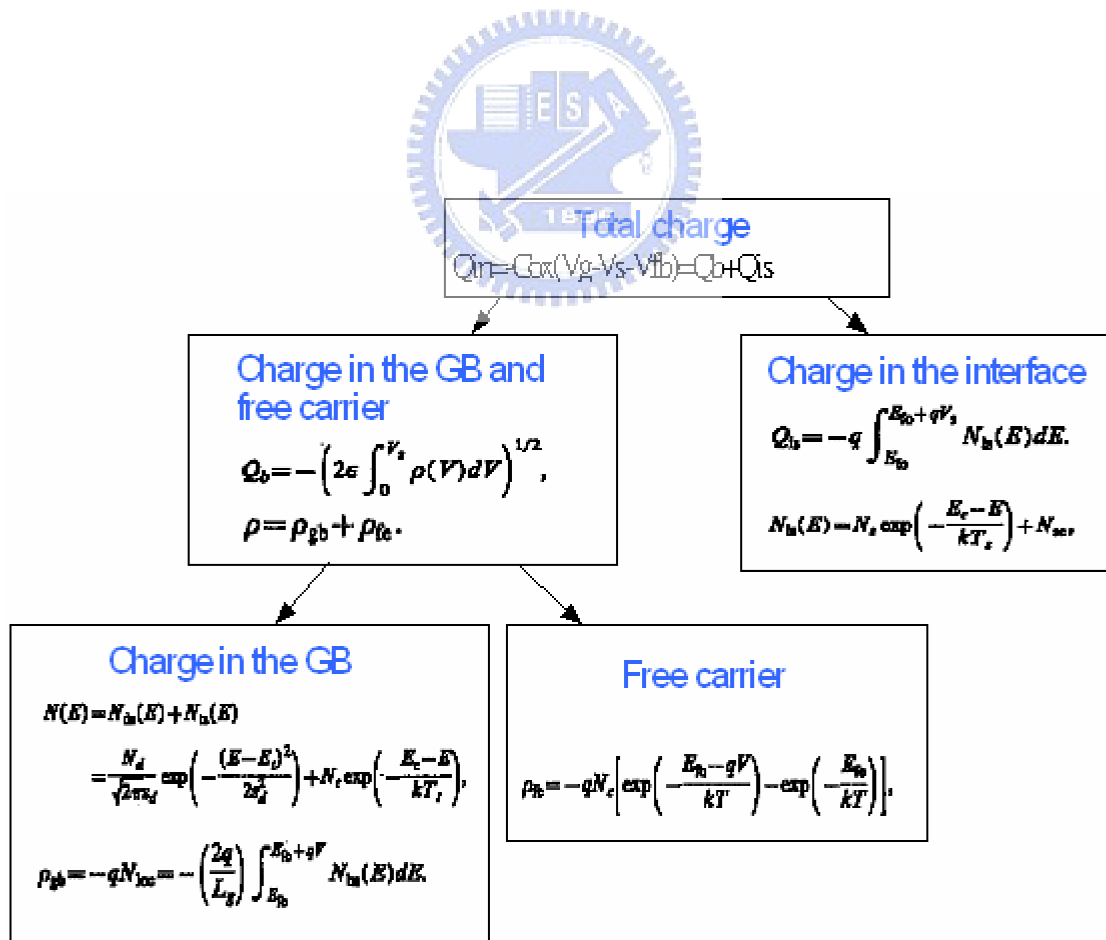


Fig. 3-2-2 The process flow of finding the surface potential

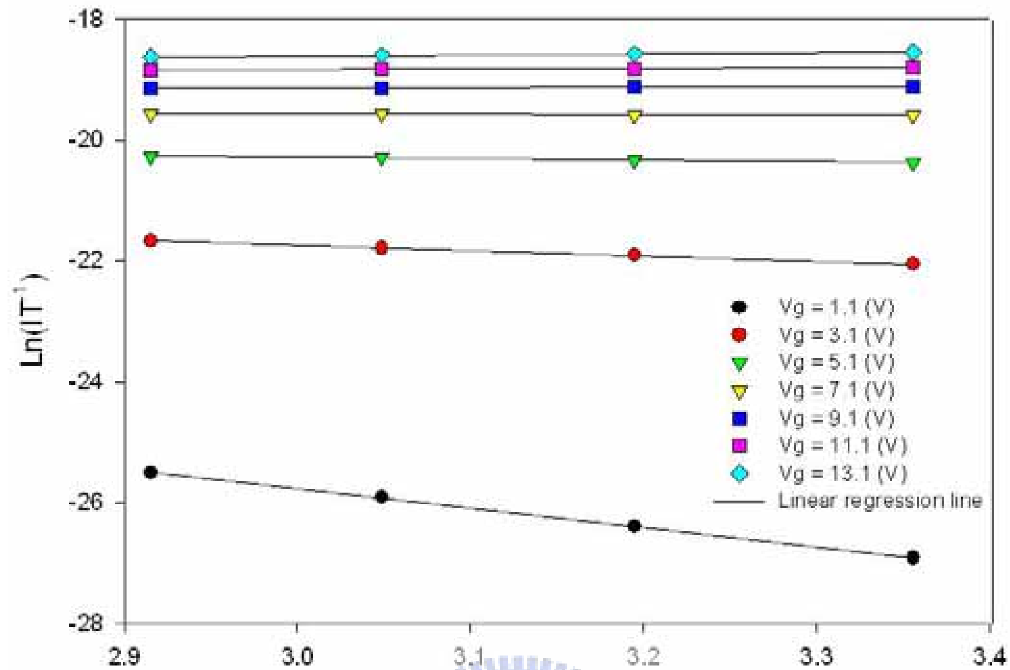


Fig. 3-2-3 Dependence of IT^{-1} on temperature.

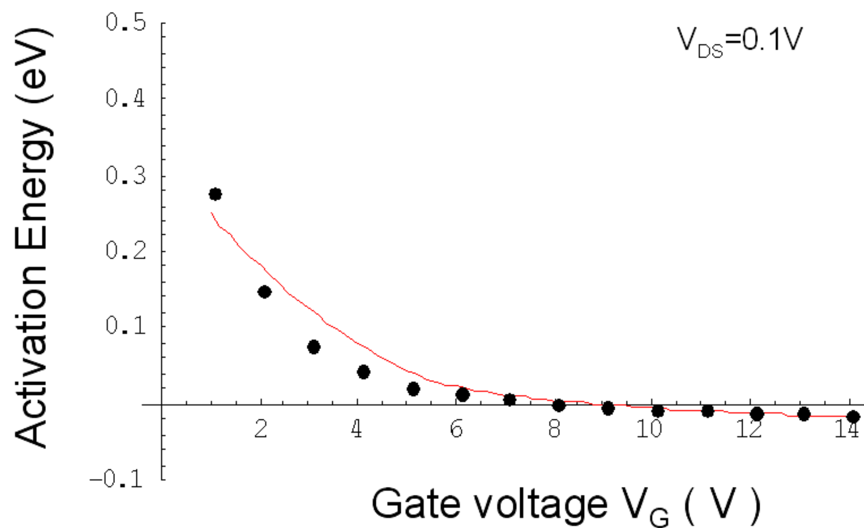


Fig. 3-2-4 The solid line is the best fit of the experimental data with the theory for the bulk and interface states distribution parameters.

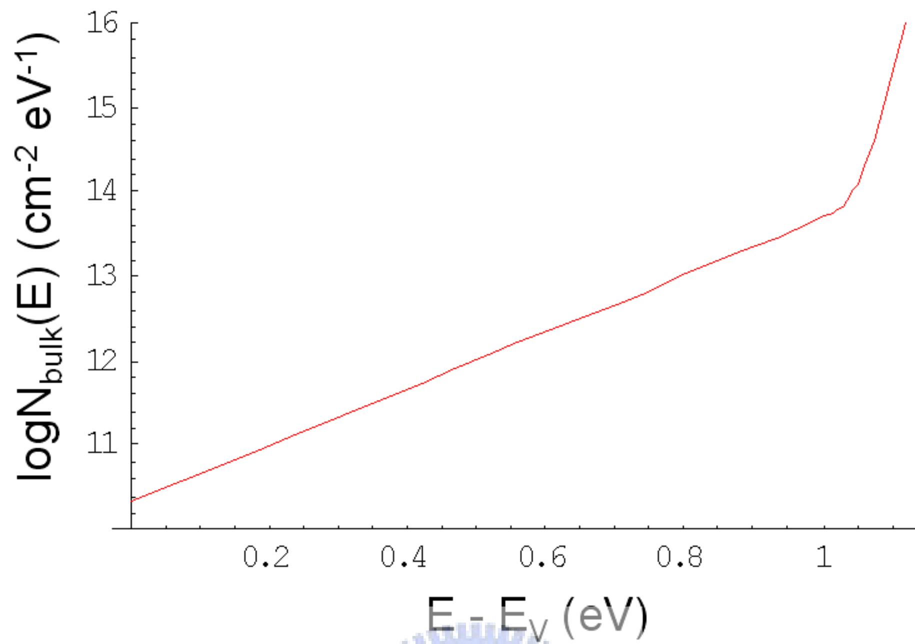


Fig. 3-2-5 Energy distribution of bulk states of the SPC and 2hr NH_3-passivation time undoped polysilicon TFT.

flat band voltage, V_{FB}	-1.7 (V)
total deep-state density per unit area, N_{ds}	1.2×10^{14} (cm^{-2})
characteristic of the exponential trap distribution, kT_{ds}	0.013 (eV)
total tail-state density per unit area, N_{ts}	1.0×10^{16} (cm^{-2})
characteristic of the exponential trap distribution, kT_{ts}	0.013 (eV)

Table. 3-2-1 Parameters of the bulk state distribution of the SPC and 2hr NH_3-passivation polysilicon TFTs.

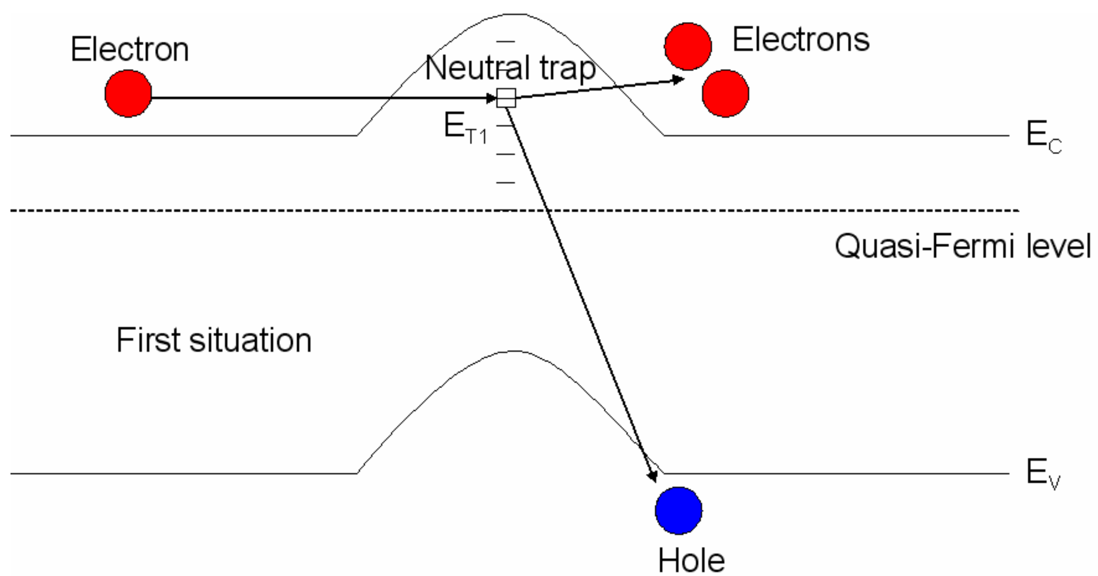
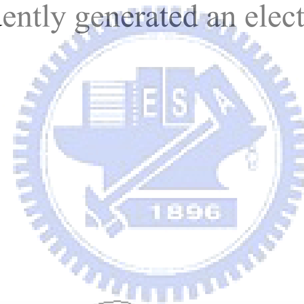


Fig. 3-3-1(a) A high energy entering electron hits the neutral trap which is above the quasi-Fermi level and subsequently generated an electron-hole pair.



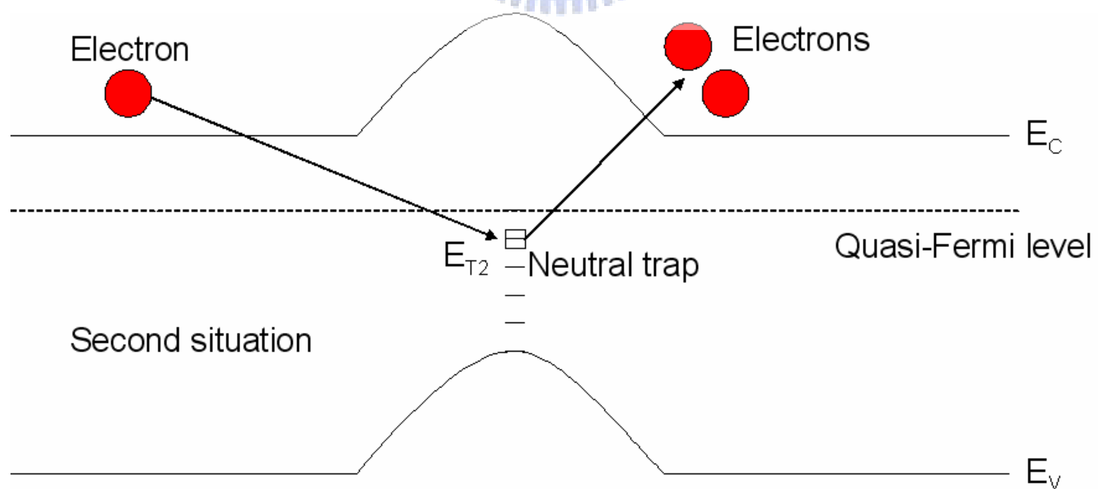


Fig. 3-3-1(b) A high energy entering electron hits the negative charged trap which is under the quasi-Fermi level and subsequently "lift" this electron to the conduction band edge.

Channel width W	10 (μ m)
Channel length L	10 (μ m)
Grain size L_g	50 (nm)
Trap density N_T	$0.64x10^{-12}$ (cm^{-2})
Polysilicon film thickness t_{Si}	100 (nm)
Gate oxide thickness t_{ox}	50 (nm)
Flat band voltage V_{FB}	-1.7 (V)
Bulk charge modified term η	0.73
Channel thickness empirical parameter A_1	2341
Channel thickness empirical parameter A_2	0.983
Saturation region barrier lowering modified term Γ	0.1
A_i/β	0.1

Table. 3-5-1 The parameters set that is used in our numerical model.

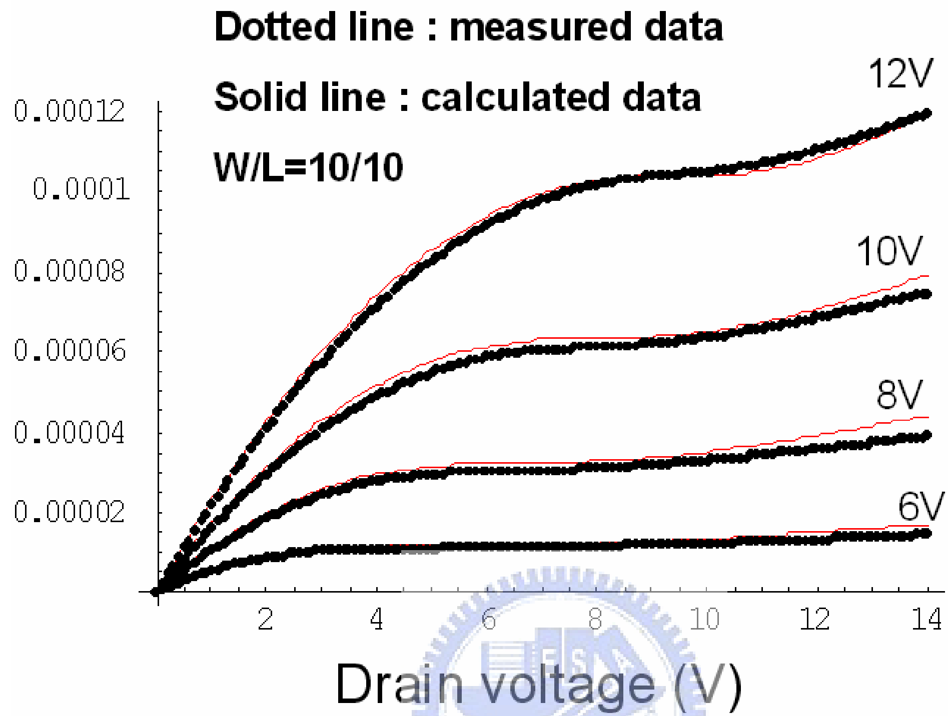


Fig. 3-5-1 Comparison between measured and calculated I_D-V_{DS} characteristics for n-channel poly-Si TFT's with W/L=10μm /10μm.

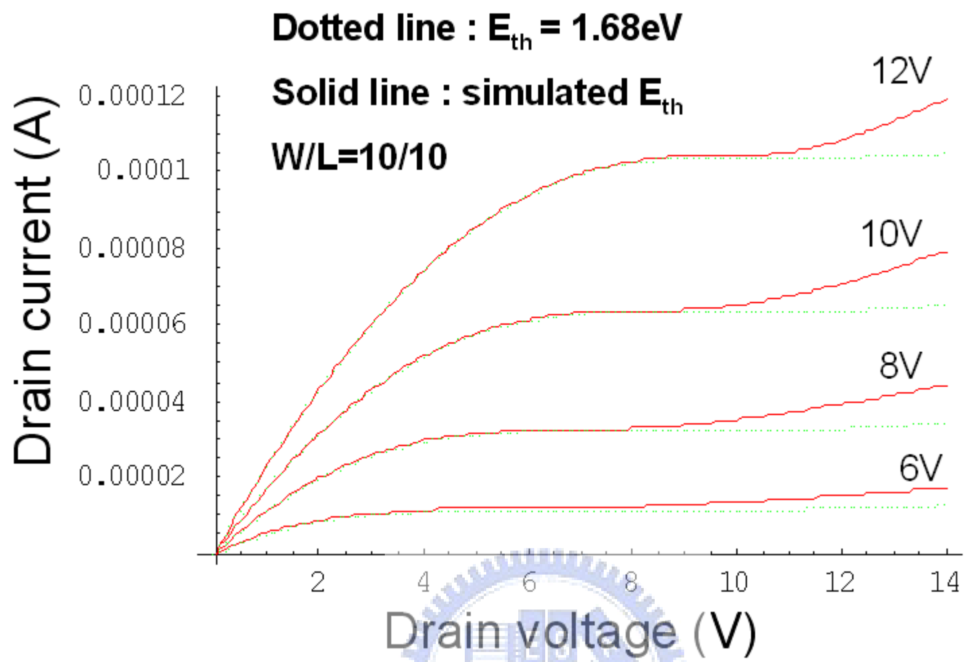


Fig. 3-5-2 Comparison between conventional threshold energy(1.68eV) and our simulated threshold energy for n-channel poly-Si TFT's with W/L=10μm /10μm.

Chapter 4

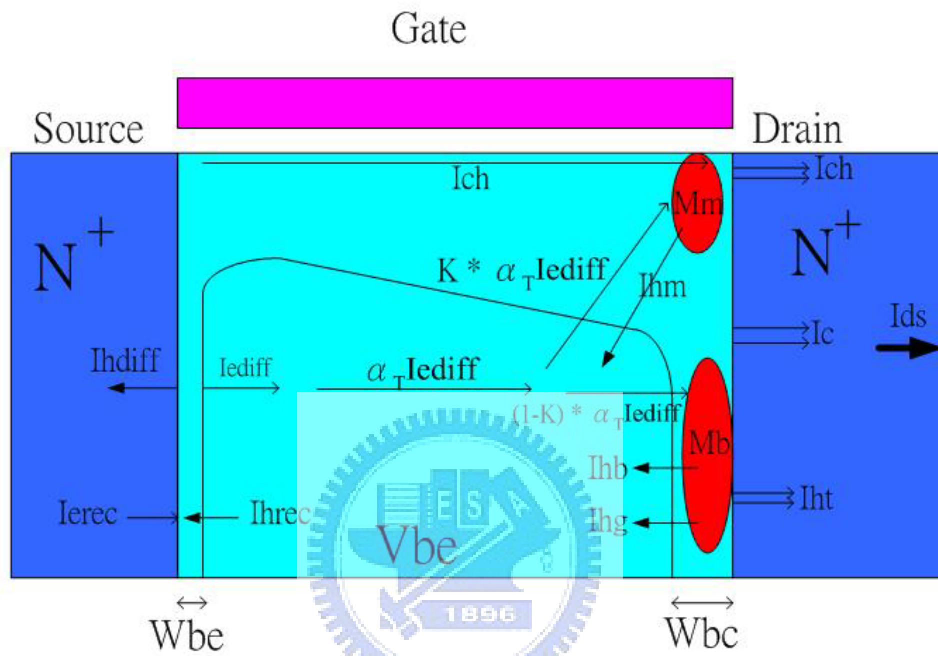
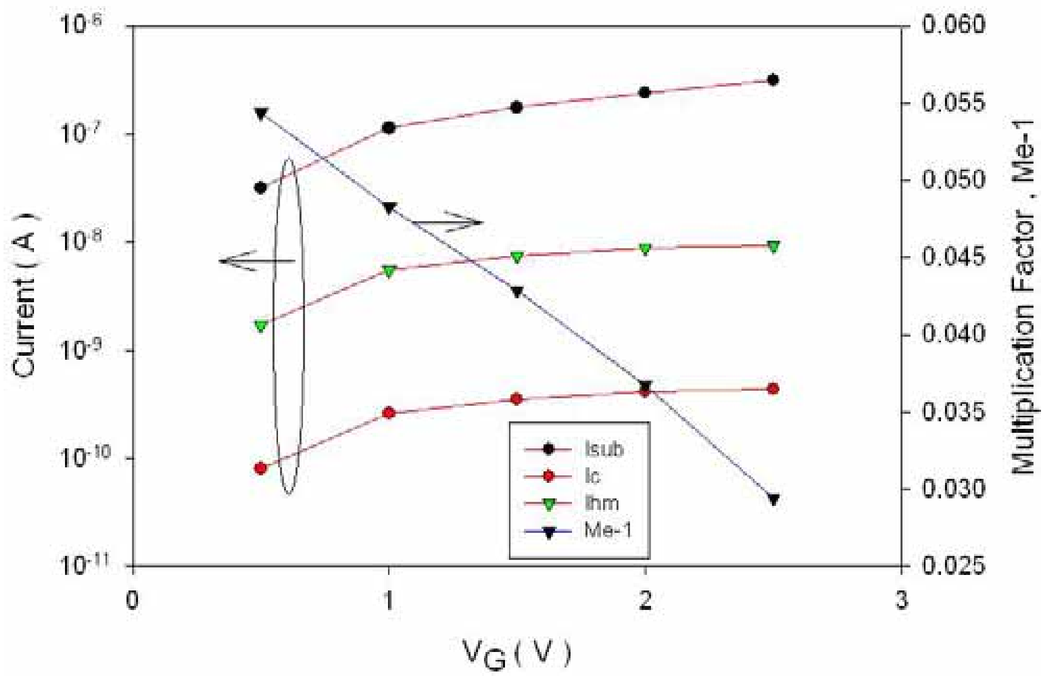
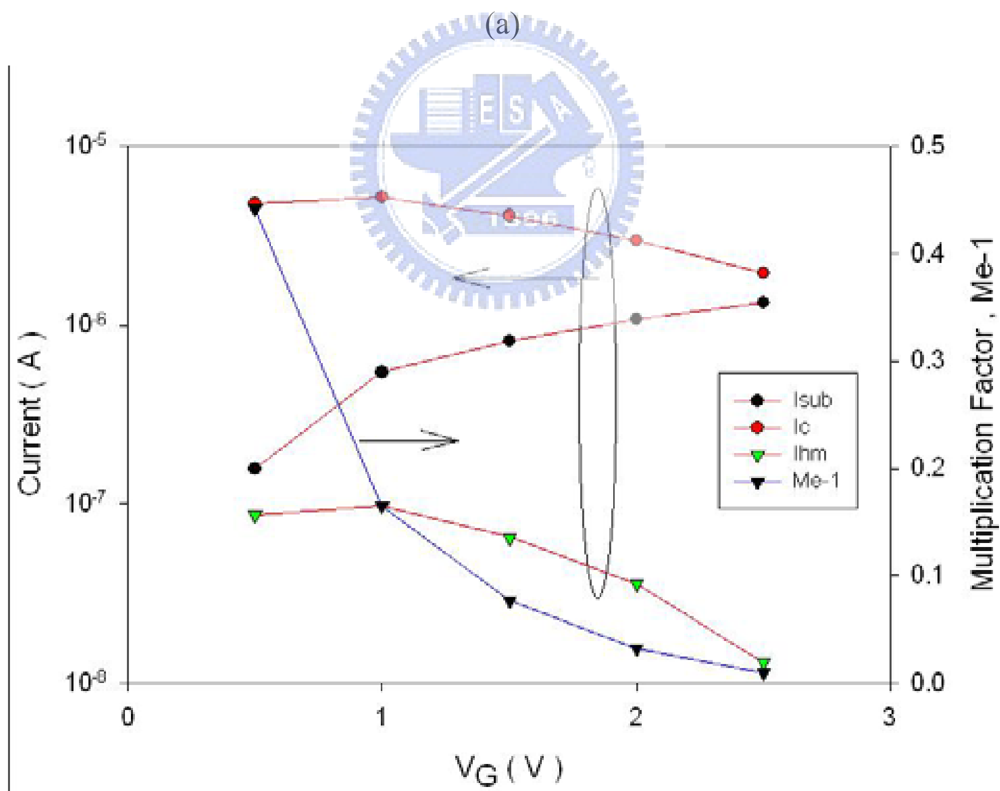


Fig. 4-2-1 Cross-section of the partially-depleted TFT NMOS device.

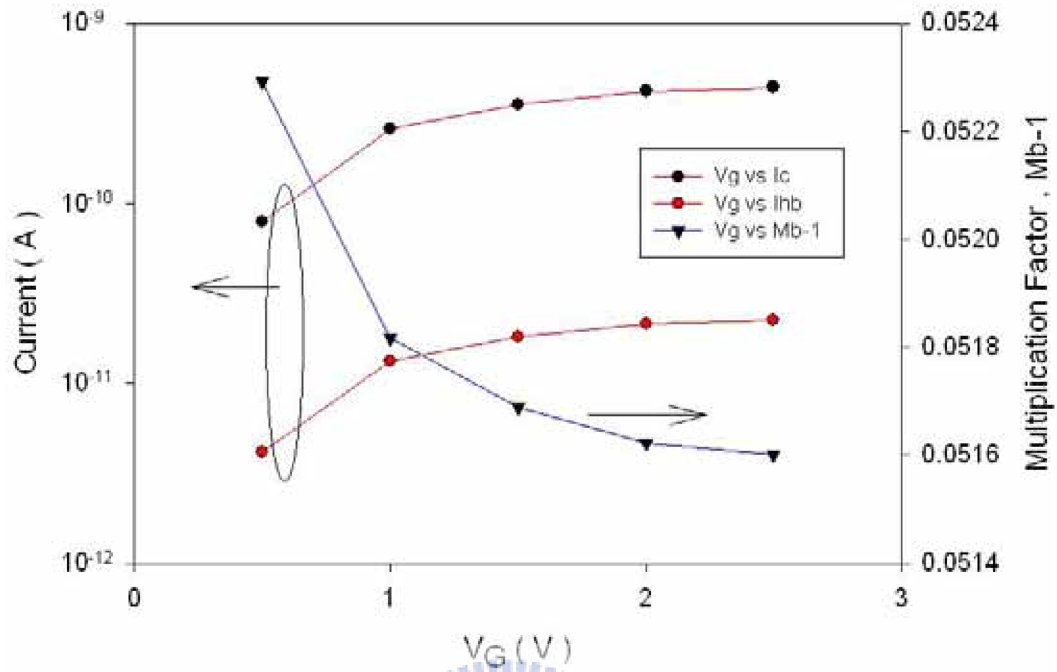


(a)

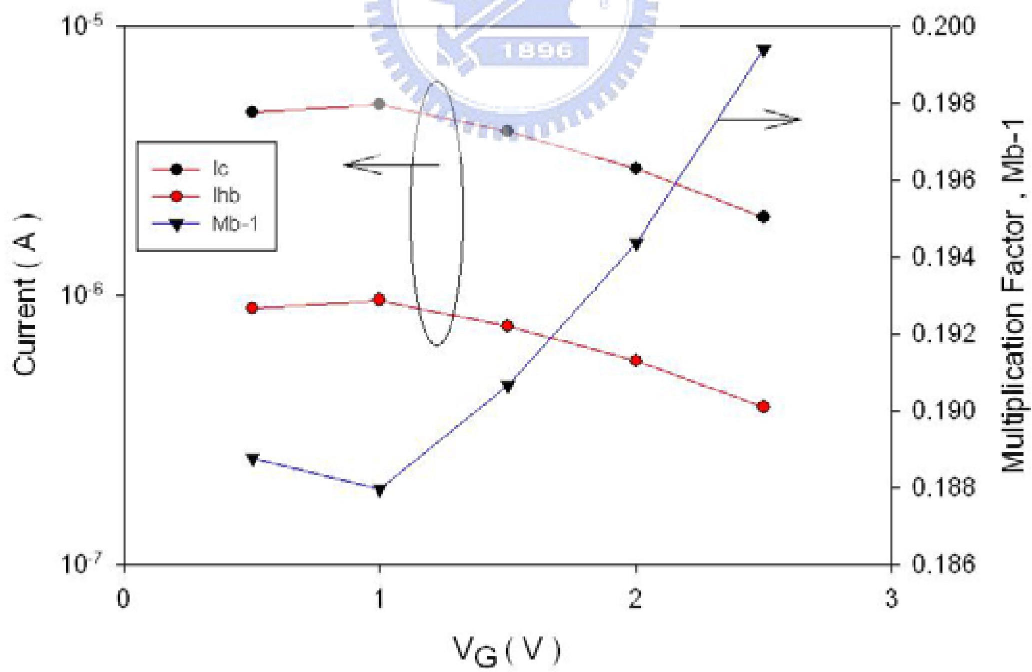


(b)

Fig. 4-3-1 Plots of (a)I_{sub}, Ic, I_{hm}, and $M_m - 1$ at V_{ds} at 5 V for W/L = 10/6μm and (b)I_{sub}, Ic, I_{hm}, and $M_m - 1$ at V_{ds} at 2.5 V for W/L = 10/1.5μm.

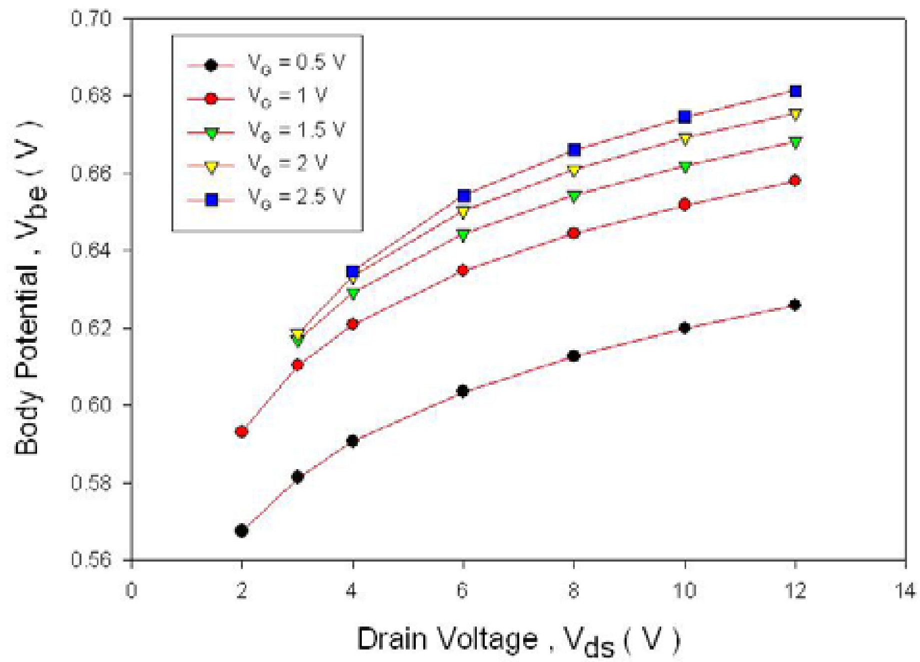


(a)

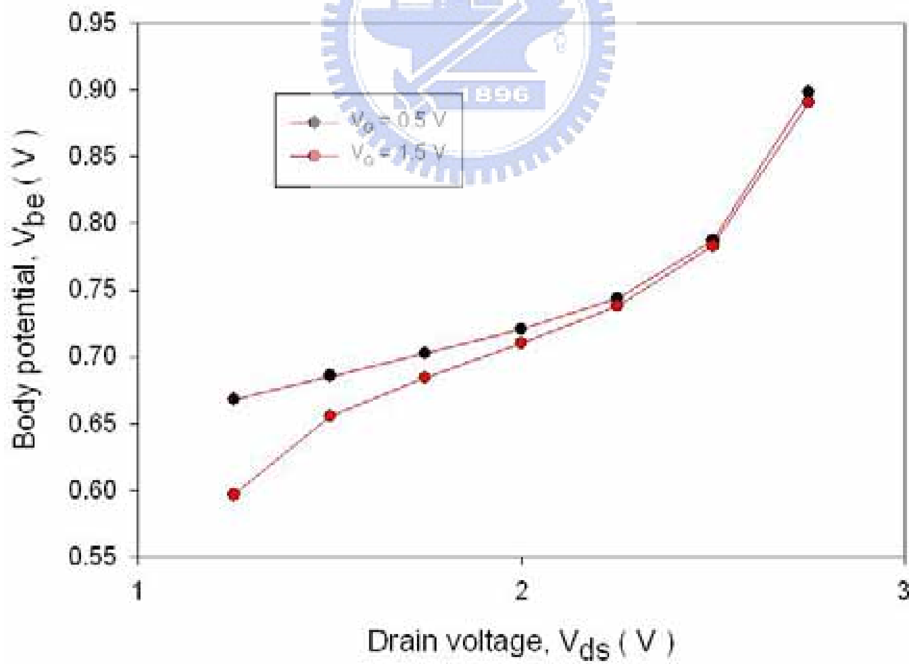


(b)

Fig. 4-3-2 Plots of (a)Ic, I_{hb}, and $M_b - 1$ at V_{ds} at 5 V for W/L = 10/6μm and (b)Ic, I_{hb}, and $M_b - 1$ at V_{ds} at 2.5 V for W/L = 10/1.5μm.



(a)



(b)

Fig. 4-3-3 (a)The body potential vs drain voltage on the simulation model for various gate voltage for W/L = 10/6μm (b)The body potential vs drain voltage on the simulation model for various gate voltage for W/L = 10/1.5μm.

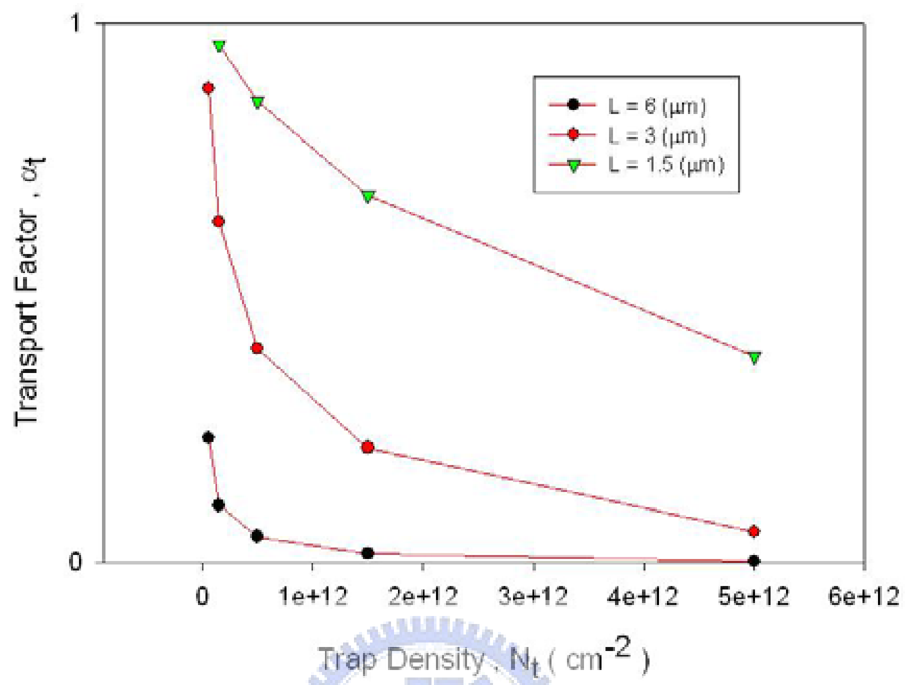
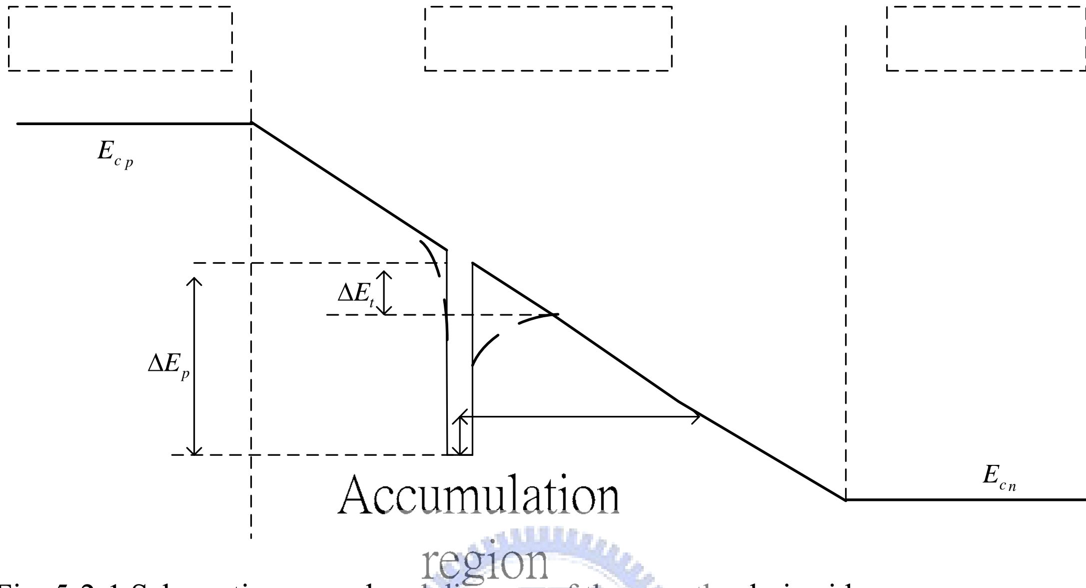


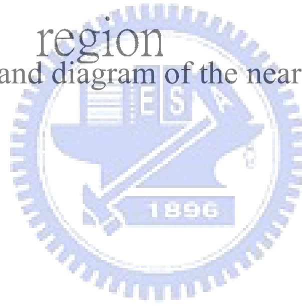
Fig. 4-3-4 The relation of transport factor and trap density for various channel length.

Chapter 5



Depletio

Fig. 5-2-1 Schematic energy band diagram of the near the drain side.



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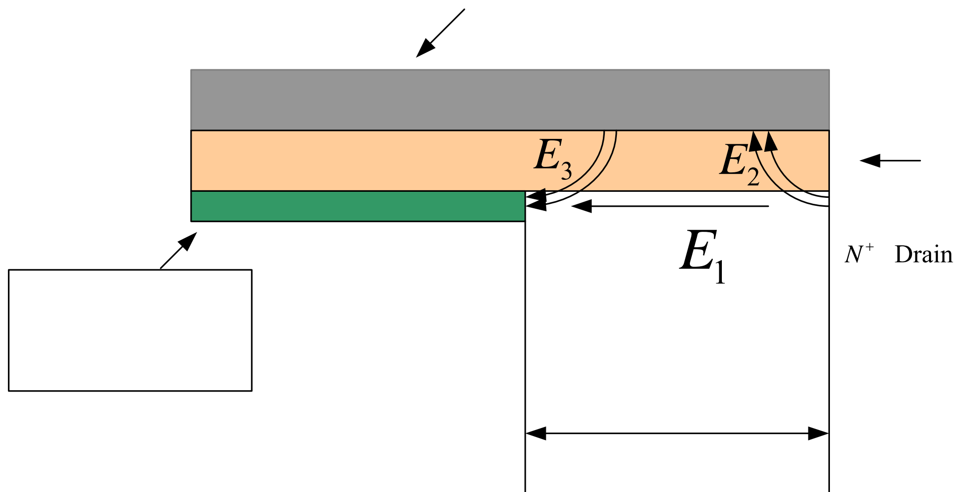

Fig. 5-2-2 The electrical field in the depletion region.

Accumulation
region

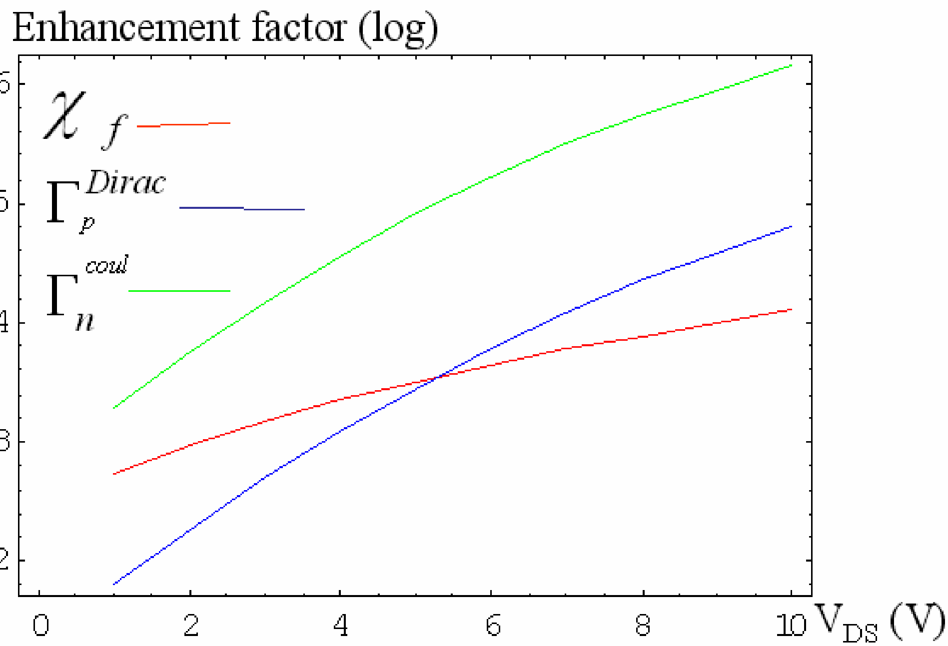

Fig. 5-3-1 The relationship between the V_{DS} and enhance factors, under constant V_G = -4V, W/L = 6/12(μm).

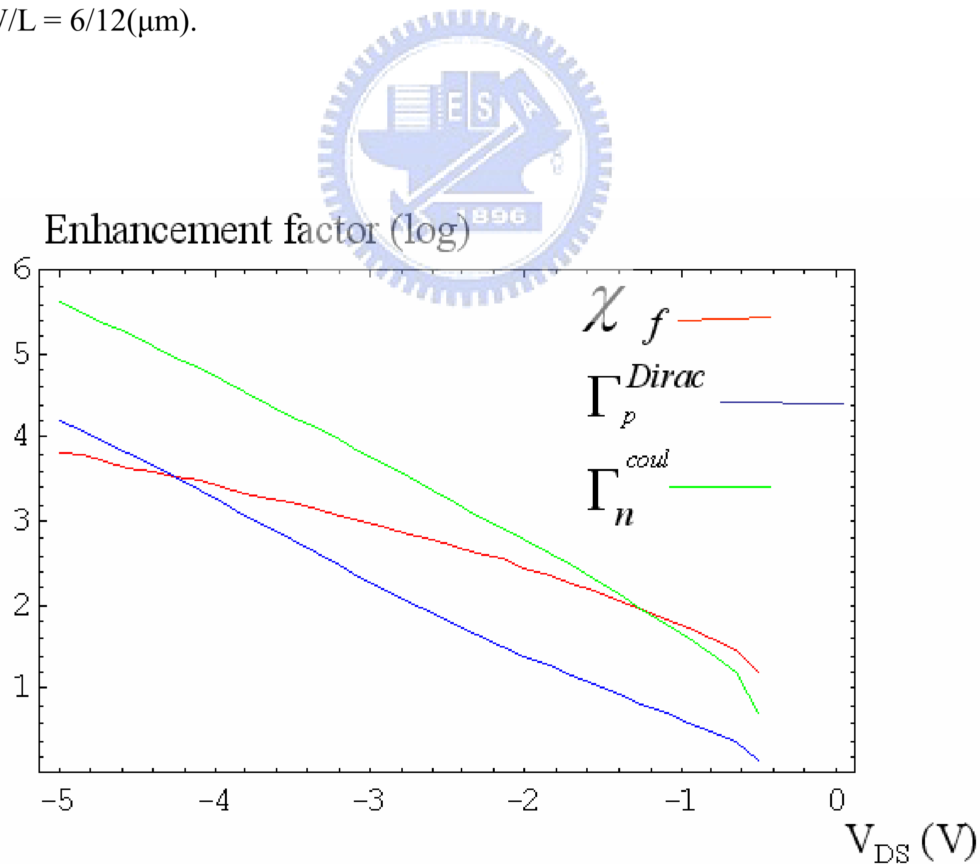

Fig. 5-3-2 The relationship between the V_G and enhance factors, under constant V_{DS} = 5.1V, W/L = 6/12(μm).

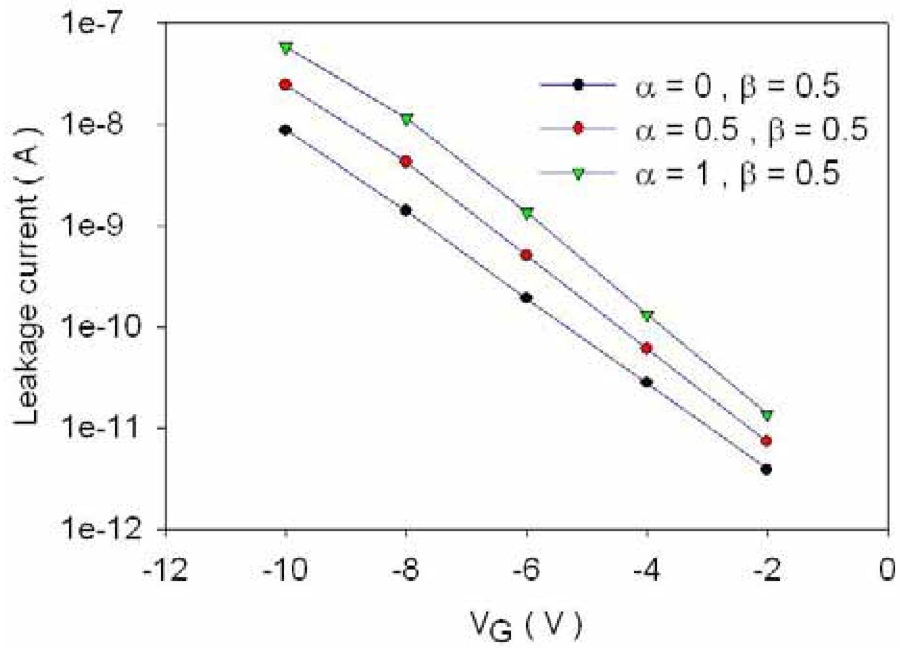

Fig. 5-3-3 Leakage current versus gate voltage (at $V_D = 5V$) for different values of parameter α for our model.

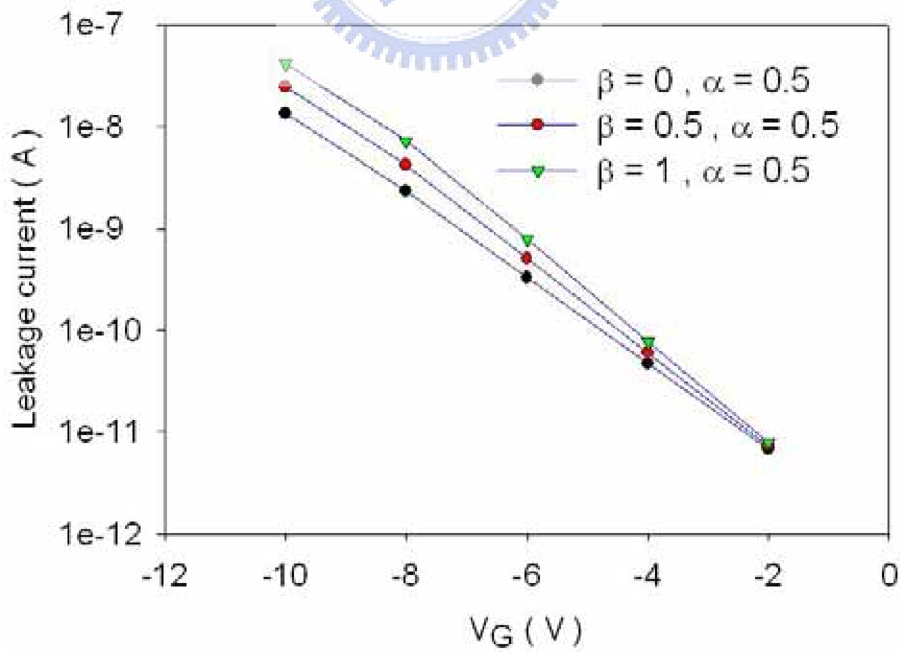

Fig. 5-3-4 Leakage current versus gate voltage (at $V_{DS} = 5V$) for different values of parameter β for our model.

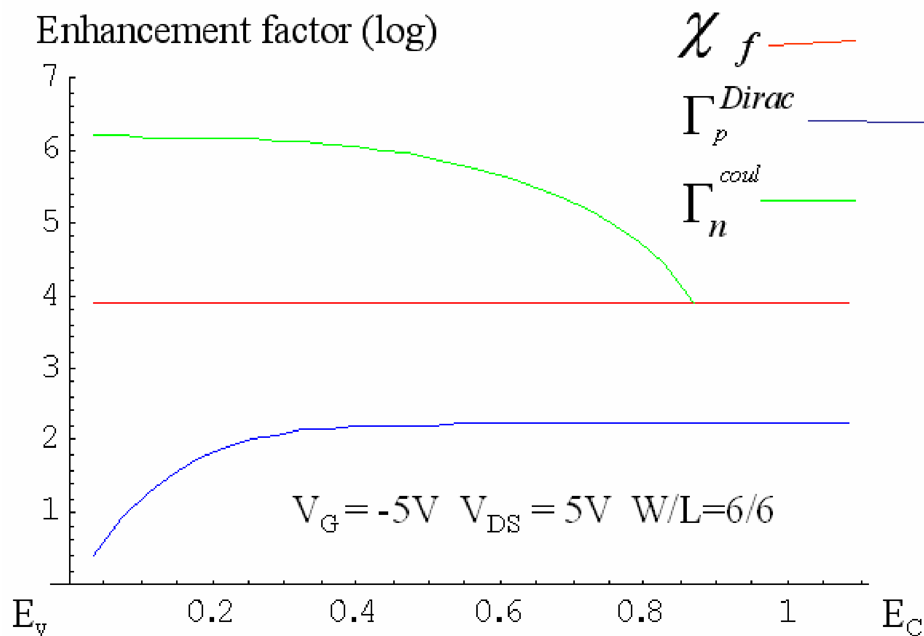

Fig. 5-3-5 The relationship between the trap position of donor-like trap in the energy gap and enhancement factors.

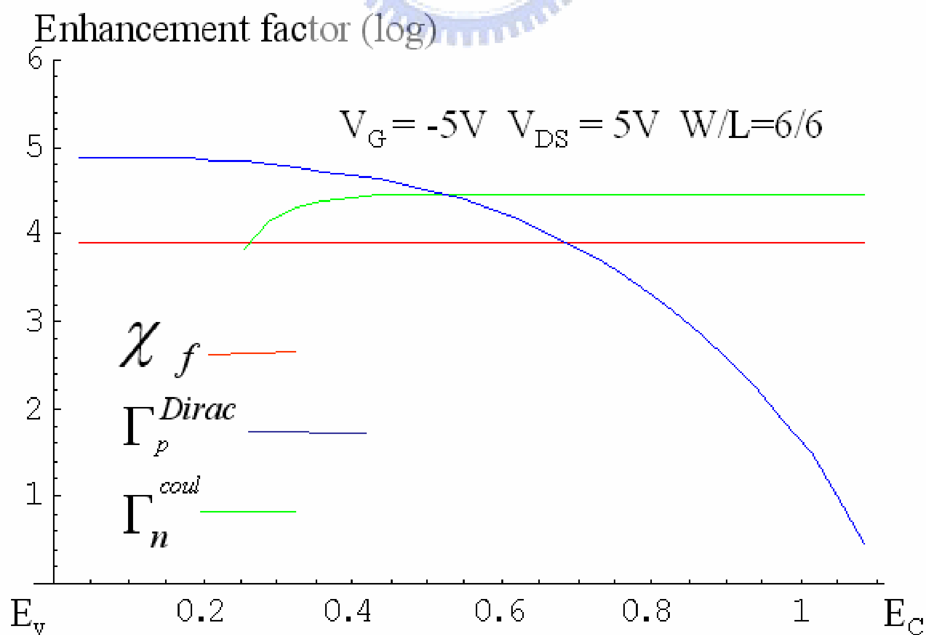

Fig. 5-3-6 The relationship between the trap position of acceptor-like trap in the energy gap and enhancement factors.

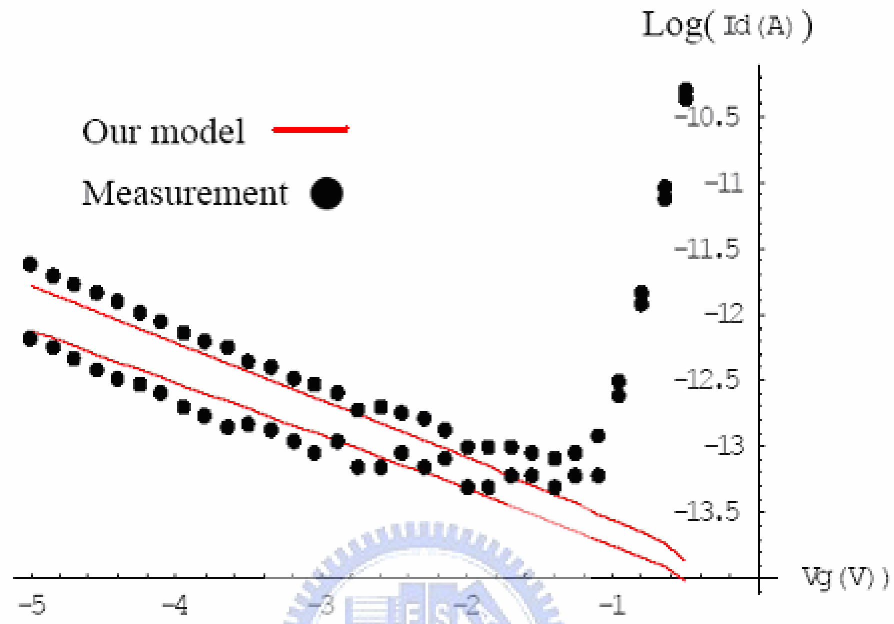

Fig. 5-3-7 Fitting result. W/L = 6/6 (μm) and the drain voltage V_{DS} is varied from 4 to 5 V.

Parameter	Notation	Value
Electron effective mass	me	0.26×m0
Hole effective mass	mp	0.78×m0
Thermal velocity	Θn =Θp	10^{7} (cm)
Capture cross section area	σnd =σna =σpd =σpa	10^{-15} (cm^{2})
	a	0.9
	b	0.2
Deep state trap concentration	gtd	0.5×10^{16} (cm^{3})
Characteristic temperature of deep state	Ttd	2700 (K)
Tail state trap concentration	gtt	10^{19} (cm^{3})
Characteristic temperature of tail state	Ttt	450 (K)

Table 5-3-1 Parameters employed for out model.