國立交通大學

光電工程研究所

碩士論文

可調變電流畫素電路應用在非晶矽薄膜電晶體主動式矩陣有機發光二極體顯示器

Adaptive Current Scaling Pixel Circuit for a-Si:H TFT AMOLED Displays

研 究 生 ： 黃建智

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A Thesis

Submitted to Institute of Electro-Optical Engineering

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

In

Electro-Optical Engineering

January 2006

Hsin-Chu, Taiwan, Republic of China

中華民國九十五年三月

可調變電流畫素電路應用在非晶矽薄膜電晶體主動式矩陣有機發光二極體顯示器

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摘要

主動式矩陣有機發光二極體電流源畫素電路之瓶頸，在於顯示低灰階畫面時充電時間過長導致驅動資料的錯誤。本論文提出一種創新可調變電流畫素電路設計，利用儲存電容串接結構，來達到電流可調變的功效以縮短充電時間，同時不減少畫素的開口率。

根據數值分析與實驗的結果，若與傳統的電流源驅動畫素電路做比較，當顯示亮度為 100 和 20 cd/m^2 時，充電時間可分別縮短 10.7 和 13.7 倍。此外，當輸入電流範圍為 0.2 和 10 μ 情況之下，此一可調變電流畫素電路設計可達最大驅動電流範圍 2 nA 和 5 μA。另一方面，此畫素電路設計中，當驅動電晶體的截止電壓變化為 4.5 V 時，輸出電流變化可壓縮至 3.8 %。這些實驗結果，皆證實此一可調變電流畫素電路設計可縮短充電時間及補償元件特性變化，以達到主動式有機發光二極體顯示器高解析、大尺寸之需求。

Adaptive Current Scaling Pixel Circuit for a-Si:H TFT AMOLED Displays

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Abstract

The difficulty that current-driven pixel circuit of active matrix organic light emitting diode devices encounters lies in long charging time resulted in data programming error while displaying low gray level images. This thesis proposes an adaptive current scaling pixel circuit design, which utilizes the cascade structure of storage capacitors to achieve current scaling function without sacrificing aperture ratio so as to shorten the charging time.

By the analytical and experimental results, at display luminance of 100 and 20 cd/m^2, the charging time can be shortened by a factor of 10.7 and 13.7, respectively; moreover, the driving current ranging from 2 nA to 5 μA can be obtained at programming current ranging from 0.2 to 10 μA. Besides, the variation of driving current can be suppressed to 3.8% while the threshold voltage variation of driving TFT is 4.5 V which evidently demonstrated shortening charging time and compensating the characteristic variations to fulfill the requirement of high resolution and large size AMOLED displays.

致　　謝

回憶著過去兩年的日子，有歡笑有汗水，這一路走來，受到眾人的扶持與關懷，讓我能夠順利地劃下句點。在此，謹以此論文來表達對你們誠摯的謝意。

首先要感謝的是我的指導教授鄭惟中老師和謝漢萍老師，不僅提供很好的學習環境，各方面的資源也給予莫大的協助；此外，平日的教導、表達能力的訓練以及研究精神與態度的培養，讓我了解到不論在學術或是人生的任何事上，都要以嚴謹認真的態度來面對。

在求學的日子裡，感謝研究所學長姐彥仲、Vicowa、裕國、均合、喬舜、榮安、安琪、予潔，同學奕智、正宇、龍材、彥行、立仁、文生、佳峰、健富、枝福等，在課業上、研究上、生活上的幫助與分享，因為有你們使我的研究生活變得十分有趣，可能尚有一些未提及的朋友們，在此均一併致謝。

此外，我也感謝廣輝電子面板技術開發部提供儀器設備來完成畫素電路的製作與克勤經理、培銘、燕玲在實驗上的討論。

最後，是我最敬愛的父母、哥哥、嫂嫂與妹妹，感謝你們多年來的栽培與鼓勵，並在生活上細心照顧與關懷，使我能夠全心研究與學習，若沒有你們不可能有我今天的小小成果。我將與幫助過我的人一同分享這份喜悅。

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Chapter 1

Introduction

Organic Light Emitting Diode (OLED) displays have great potential to replace Liquid Crystal Display (LCD) thanks to its merits such as high brightness, high contrast ratio, light weight, thin structure, short response time and low-power consumption [1-5]. Owing to the vastly different properties of OLED from LC, the conventional driving methods for LCD may be inapplicable for OLED displays. In this chapter, the choke point of the exited driving method for OLED displays will be discussed and the objective of this thesis will be resolved accordingly.

1.1 Thin Film Transistor For Active Matrix Addressing

Initially LCD and OLED were driven by passive matrix (PM) addressing mode to achieve maximum performance. Although the PM addressing mode is simple, it would limit the display size and resolution because the duration of pulsed signal decreases as the display resolution and gray level increase. Therefore, PM addressing has been replaced by active matrix (AM) addressing for mass information content and large area flat panel displays (FPDs). In AM addressing scheme, field-effect transistors (FETs), such as thin-film transistors (TFTs) are widely adopted because TFTs can be easily fabricated for large size substrate by either amorphous or polycrystalline silicon technologies.

In the realization of AMOLED, low temperature poly-silicon (LTPS) TFTs utilized as a backplane for OLED are commonly adopted in AMOLED development because LTPS TFTs can provide much higher current due to its higher mobility than that of hydrogenated amorphous-silicon (a-Si:H) TFTs. However, during LTPS TFT fabrication process, the poly-Si is crystallized by excimer laser annealing (ELA),

where the uniformity control is difficult. Consequently, the crystallization of poly-Si is probably varied to affect the threshold voltage, mobility and sub-threshold. Thus, the uniformity of TFT will be deteriorated to result in non-uniform brightness from pixel to pixel [6]. Besides, complex fabrication process and high cost are extra considerations for display industries to develop LTPS TFT as well.

Compared to LTPS TFT, using a-Si:H TFTs as the backplane to realize AMOLED needs fewer manufacturing costs and lower equipment investment because the a-Si:H can be deposited in chemical vapor deposition (CVD) and no extra process steps are required. The uniformity of brightness throughout the whole display is satisfactory [7-8]. There, a-Si:H TFTs is therefore to LTPS TFTs in large size OLED displays.

1.2 Driving Mode

The active matrix pixel circuits can be classified into two categories based on the type of input data. The first one is the voltage-driven pixel circuit and the other is current-driven pixel circuit.

1.2.1 Voltage-Driven Pixel Circuit

TFT-based electrical circuit is the main stream of LCD driving circuit, and exhibits good performance. Hence, it is straight-forward to implement the same structure, two-TFT voltage-driven circuit, in OLED panel as shown in Fig. 1-1, [2]. The gate of switching TFT (T1) is connected to V_{SCAN} line, and the V_{DATA} driver supply data to the source of T1 in each pixel circuit. After V_{DATA} has been written to the pixel, the V_{SCAN} is switched to low and the voltage stored in C_{ST}. However, the two-TFTs circuit in OLED panel causes serious problems: threshold voltage (V_{TH}) and mobility (μ_{FE}) variations due to the process- and aging-induced the variation of the TFT characteristics. The direct influences of the increasing V_{TH} and decreasing μ_{FE} are a decreasing OLED driver current for the same input data voltage leading to

the non-uniformity in brightness of the whole display area shown in Fig. 1-2(a) [9]. Hence, the compensating circuits should be inserted to maintain a constant current passing through the OLED.

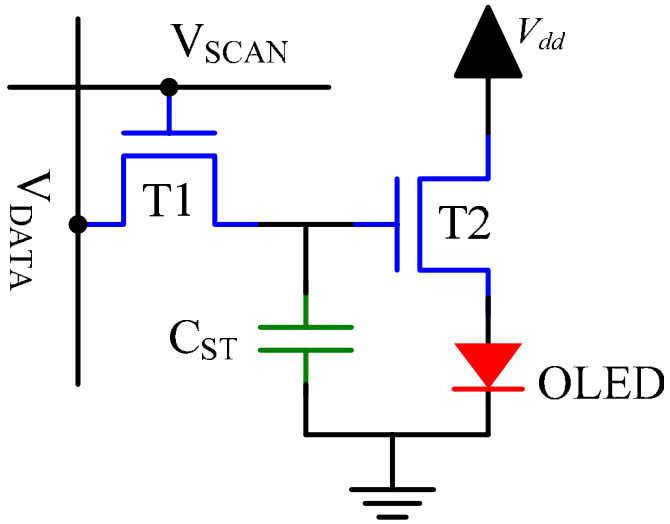


Fig. 1-1. Conventional voltage-driven pixel circuit for AMOLED display.

(a) **(b)**

Fig. 1-2. Comparison of luminance uniformity of (a) voltage programming with (b) current programming.

1.2.2 Current-Driven Pixel Circuit

Current driving schemes with four-TFT a-Si AMOLED pixel circuit with three control lines shown in Fig. 1-3, was proposed by He et al. [10-11]. A current programmed pixel circuit with self-adjusted voltage source not only provides a continuous excitation to OLED, but also compensates ΔV_{TH} to improve the brightness uniformity as shown in Fig. 1-2(b). However, a large timing delay is observed at a low

programming data current inasmuch as the interaction between the high OLED efficiency and charging of a large interconnect parasitic capacitance. For example, a current of 70 nA is sufficient to achieve luminance of 100 cd/m^2 when the efficiency of OLED is 20 cd/A or higher, but charging the interconnect parasitic capacitance of about 10 pF to the sufficient voltage level needs more than 150 μs. This charging time is much longer than the typical frame time (30 μs) for a display with VGA (640*RGB*80) resolution operated at 60 Hz. Thus, the current driving method causes serious data programming error and still has much room to improve.

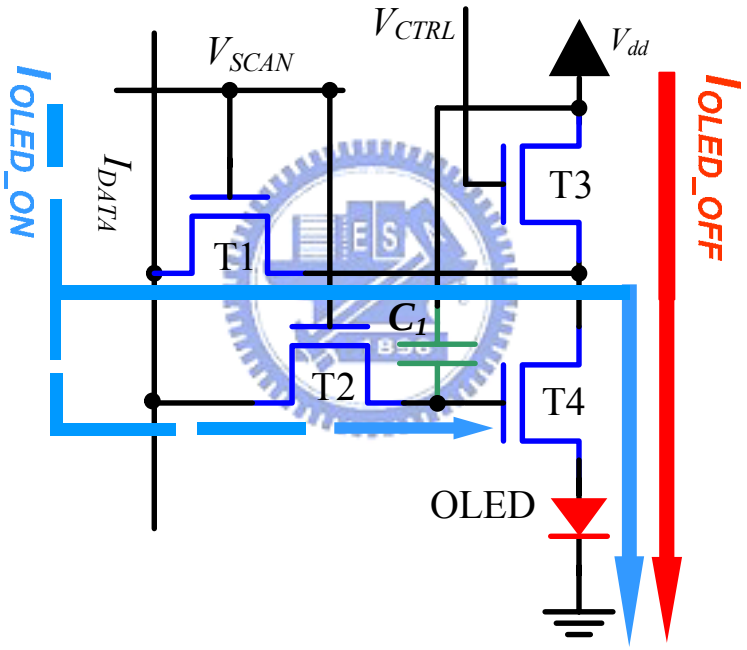


Fig. 1-3. Schematic diagram of conventional current-driven pixel circuit for AMOLED display.

1.3 Motivation and Objective of This Thesis

As the abovementioned discussion on active matrix pixel circuits, since the OLED is a current driven device, the pixel circuit needs not only to ensure the matching of current during addressing and non-addressing state but also to compensate the variations in OLED and TFT characteristics such as threshold voltage variations, aging effects, and etc.

Although a-Si:H TFT technology can reduce manufacturing cost, equipment investment and posses TFT uniformity, poor carrier mobility and larger threshold voltage shift are the main issues. To resolve these problems, various techniques have been proposed in both voltage and current driven pixel circuits [12-16] using a-Si:H TFTs. In these cases, the current-driven scheme can effectively achieve uniform brightness so that it is suitable for high resolution and large size AMOLED displays. However, in the current-driven mode, low programming data current will induce serious data programming error for high resolution and large sizes displays. Therefore, in this thesis an adjustable current scaling pixel circuit for the a-Si:H TFT is proposed and demonstrated to improve programming time delay.

1.4 Organization of This Thesis

This thesis is organized as follows. The principles and the features of adaptive current scaling pixel circuit will be presented in Chapter 2. In Chapter 3, the simulation results including TFT parameter extraction, the variation of current scaling ratio with different the ratio of storage capacitance and evaluation of programming time will be discussed. In Chapter 4, the inversed-staggered back-channel-etch a-Si:H TFT and OLED device fabrication process will be introduced, respectively. Besides, the measurement equipments used to evaluate electrical properties of adaptive current scaling pixel circuit and visual performance of active matrix OLED device are illustrated. In Chapter 5, according to the experimental results, several parameters in fabrication process are discussed, and then the designed structure will be realized and modified. The conclusion of the dissertation and the future work are given in Chapter 6.

Chapter 2

Principle

Due to the technical challenge for the current-driven pixel circuit for AMOLED displays, the current-mirror type based on current-driven pixel circuit with current scaling function [17-18] that rudimentarily solves programming time delay by using high programming data current to display low gray level images will be described. However, to achieve a large current scaling ratio, the TFT geometric sizes are necessary enlarging resulted in low aperture ratio. Hence, a modified current-driven pixel circuit based on a-Si:H TFT technology with current scaling function which can enhance the data programming speed is proposed. The operation of the proposed pixel circuit and the method of current scaled down will be presented in details as well.

2.1 Why Current Scaling Function

The main issue of current-driven pixel circuit in applications for matrix array in pixels display is the long resistance-capacitance (RC) delay, which is proportional to the size and resolution of display panel. A large RC delay will cause cross-talk, flicker effects, and even more serious data programming error due to the insufficient pixel charging across the large display area. The total programming time (T_{PROG}) [19] is defined as the sum of the RC delay time of scan line ($T_{RC\text{-}SCAN}$) and data programming time of data line (T_{DATA}) in the following equation :

$$T_{PROG} = T_{RC-SCAN} + T_{DATA}, \qquad (2\text{-}1)$$

where $T_{RC\text{-}SCAN}$ and T_{DATA} can be estimated by the following equation:

$$T_{RC-SCAN} = (N_H R_{PIXEL})(N_H C_{PIXEL}) = \frac{R_{\square} C_{\square} H^2}{Z} + N_H C_{OV} R_{\square} H, \qquad (2\text{-}2)$$

where R_{PIXEL}, C_{PIXEL}, H, N_H, $C_{\square}$, $R_{\square}$, Z and C_{OV} denote the pixel resistance of bus line, pixel capacitance of bus line, display width, horizontal resolution, capacitance per meter square, sheet resistance, pixel pitch to bus line width ratio, and TFT gate-to-drain/source overlap capacitance.

$$T_{DATA} = \frac{V_{DATA}(C_{DATA} + C_{ST})}{I_{DATA}}, \tag{2-3}$$

where I_{DATA}, C_{DATA}, C_{ST}, and V_{DATA} denote the programming data current, data line capacitance, storage capacitance and the voltage of C_{ST}. Due to the C_{ST} was much smaller than C_{DATA}, it could be neglected to simplify the calculation. Hence, T_{DATA} was rewritten as:

$$T_{DATA} \cong \frac{V_{DATA} \cdot N_V \cdot C_{\square}}{R_{SCALE} \cdot J_{OLED} \cdot Z^2}, \tag{2-4}$$

$$R_{SCALE} = \frac{I_{DATA}}{I_{OLED}}, \tag{2-5}$$

$$J_{OLED} = \frac{C_n C_E \pi L}{C_V \eta}, \tag{2-6}$$

where N_V, R_{SCALE} and J_{OLED} denote the vertical resolution of display, current scaling ratio and the current density of OLED device. I_{OLED} is the OLED driving current. The C_n, C_E, and C_V depend on the refractive index and the emission spectrum of the OLED material. L is the OLED luminance and η is device quantum efficiency. Based on Eq. 2-1 to 2-6, the total programming time can be effectively shortened by large R_{SCALE} in the condition of the same materials, panel size and resolution. Hence, the combination of current-driven pixel circuit and current scaling function is expected to be widely adopted by the applications in high resolution and large size AMOLED display.

2.2 Current-Mirror Pixel Circuit

The current-mirror pixel circuit can achieve current scaling function by enlarging the geometric size of TFTs. The architecture and driving method can be described as follows.

The current-mirror pixel circuit consists of a driving TFT (T4), three switching TFTs (T1, T2, and T3), and one capacitor (C_1) shown in Fig. 2-1. The operation of the pixel circuit is controlled by the three external terminals (V_{SCAN}, I_{DATA}, and V_{dd}) and the ground. The signals of V_{SCAN} and I_{DATA} are supplied by external drivers while the cathode of OLED is connected to the drain electrode of T4. There are two states for the pixel circuit: addressing state and non-addressing state, which will be described as follows.

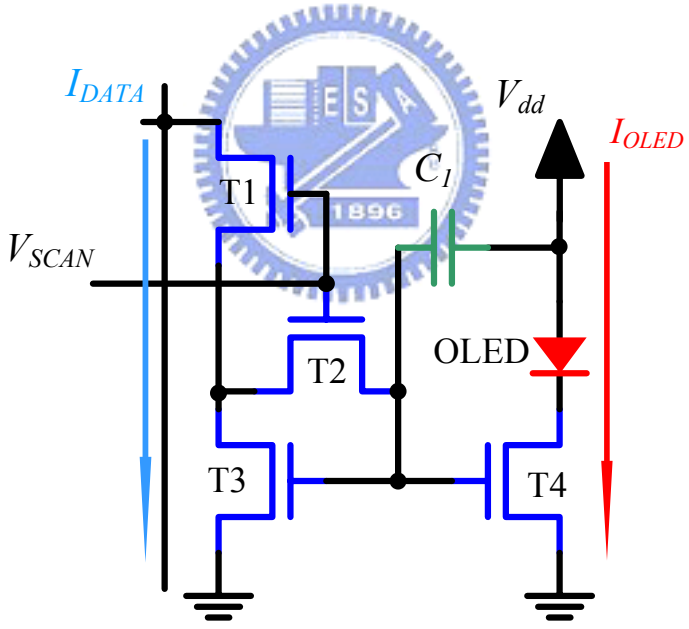


Fig. 2-1. Schematic diagram of conventional current-mirror pixel circuit.

2.2.1 Addressing State

During the period of the addressing state, T1 and T2 are turned on by the V_{SCAN}. Then, the programming data current (I_{DATA}) passing through T1 and T3 to the ground determines the gate voltage of T3 by the following equation:

$$I_{DATA} = \frac{1}{2}\mu_{FE}C_{OX}\frac{W_3}{L_3}(V_{GS3} - V_{TH3})^2, \quad (2\text{-}7)$$

where μ_{FE}, C_{OX}, W_3, L_3, V_{GS4} and V_{TH3} denote the field-effect mobility, oxide capacitance, channel width, length, the gate-source voltage and threshold voltage of T3, respectively. T3's drain voltage is equal to its gate voltage in the deep saturation operation ($V_{DS} > V_{GS}$-V_{TH}) to sustain the current. In addition, the gate electrode of T4 is connected to the gate electrode of T3, and the gate voltage of T4 is equal to that of T3. Once the gate voltage of T4 becomes higher than the threshold voltage of T4, T4 will be turned on. In other words, the gate voltage of T3 determines T4 to turn on or turn off. Moreover, V_{dd} is larger than the gate voltage of T4 so that T4 is also operated in the deep saturation region. The driving current (I_{OLED}) passing through V_{dd}, OLED, and T4 to the ground is determined by:

$$I_{OLED} = \frac{1}{2}\mu_{FE}C_{OX}\frac{W_4}{L_4}(V_{GS4} - V_{TH4})^2, \quad (2\text{-}8)$$

where W_4, L_4, V_{GS4} and V_{TH4} denote the channel width, length, the gate-source voltage and threshold voltage of T4, respectively. The voltage difference between V_{dd} and V_{GS4} is stored in the storage capacitor (C_1) at the same time.

2.2.2 Non-Addressing State

When the operation switches from the addressing state to the non-addressing state, the T1 and T2 will be turned off due to V_{SCAN} changing from high voltage to ground. The storage capacitor will be discharged to maintain the same I_{OLED} passing through OLED and T4 during the non-addressing state.

Since the threshold voltage of T3 is still equal to that of T4, and the V_{GS3} and V_{GS4} are the same, the relation between I_{DATA} and I_{OLED} can be written as:

$$I_{OLED} = \frac{W_4}{W_3}I_{DATA}. \quad (2\text{-}9)$$

From Eq. 2-9, when W_4 is fixed, I_{OLED} can be scaled down by increasing W_3. The *scaled down ratio*, R_{SCALE}, is defined as:

$$R_{SCALE} = \frac{I_{DATA}}{I_{OLED}} = \frac{W_3}{W_4}. \quad (2\text{-}10)$$

Since the R_{SCALE} and W_3/W_4 are identical, both low I_{OLED} and large R_{SCALE} can be obtained by increasing the ratio of W_3/W_4 as the I_{DATA} is fixed. Hence, the large programming data current is utilized to display low gray level pixel so as to shorten the charging time. To improve the charging time effectively, the large geometric ratio of W_3 to W_4 is needed so that the geometric ratio will decrease the pixel aperture ratio while leaving the current scaling ratio fixed. Consequently, the current scaling ratio of current-mirror pixel circuit can not be effectively used when the display resolution increases.

2.3 Design of Adaptive Current Scaling Pixel Circuit

From the above discussions, we can conclude that although current-mirror pixel circuit is capable of improving the charging time, the large geometric size of TFTs causes low aperture ratio. In order to resolve this problem, this section introduces the architecture and driving methods of a novel current-driven pixel circuit based on the a-Si:H TFT technology.

The adaptive current scaling circuit consists of a driving TFT (T3), three switching TFTs (T1, T2, and T4) and two storage capacitors (C_1 and C_2), connected between a scan line and ground with a cascaded structure, as shown in Fig. 2-2. The operation of the circuit is controlled by the ground and four external terminals: V_{SCAN1} V_{SCAN2}, I_{DATA}, and V_{dd}. The signals of V_{SCAN1}, V_{SCAN2}, and I_{DATA} are supplied by external drivers while the cathode of OLED is connected to the ground. The operation of this pixel circuit is divided into two states: addressing and non-addressing states which are described as follows.

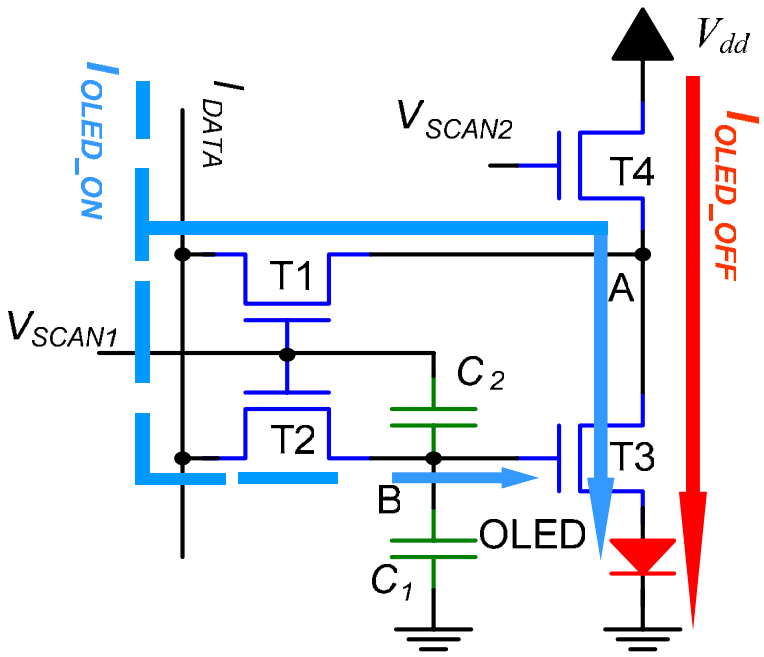


Fig. 2-2. Schematic diagram of adaptive current scaling pixel circuit for AMOLED display.

2.3.1 The Operation of Addressing State

During the period of the addressing state, T1 and T2 are turned on by V_{SCAN1} and T4 is turned off by V_{SCAN2}. After that, I_{DATA} will pass through T1 and T3 to the OLED device, while a small portion of I_{DATA} also passed through T2 to node B. Then, the drain voltage of T3 (node A) and node B are determined. The equivalent circuit diagram of the addressing state is shown in Fig. 2-3, where T1 and T2 are modeled by the turn-on resistance R_{T1} and R_{T2}, respectively. Since the R_{T1} is almost equal to R_{T2}, node A and node B are at the same potential, and T3 operates in the saturation region, accordingly. Meanwhile, the current passing through the OLED device in the addressing state, I_{OLED_ON}, is equal to I_{DATA}, which also determines the voltages of node A and B. If the variation of threshold voltage of T3 is smaller than the amplitude of V_{SCAN1}, the gate voltage of T3, $V_{B\text{-}ON}$, can be adjusted accordingly to ensure constant I_{DATA} in the addressing state. In other words, $V_{B\text{-}ON}$ is self-adjustable to

maintain the same stable value of I_{DATA} regardless of threshold voltage variation resulted from the a-Si:H TFT process.

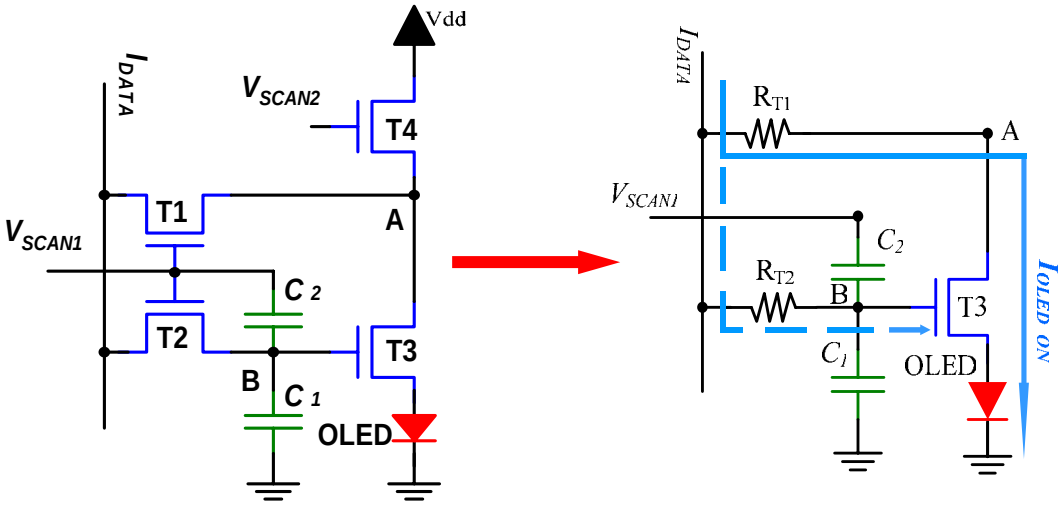


Fig. 2-3. The equivalent circuit diagram of the addressing state.

2.3.2 The Operation of Non-Addressing State

During the transition from addressing state to non-addressing state, V_{SCAN1} changes from high to low and then turns off T1 and T2. At the same time, T4 is turned on by V_{SCAN2} and then the drain electrode of T3 is connected to V_{dd} to ensure that T3 operates in the saturation region. After that, the current, I_{OLED_OFF}, will pass through T4 and T3 to the OLED device. The equivalent circuit diagram of the non-addressing state is shown in Fig. 2-4, where R_{T4} represents the turn-on resistance of T4. The voltage at node B drops because of the feed-through effect on the cascaded structure of C_1 and C_2. The dropped voltage is derived from the charged conversation theory and given by Eq. 2-11. The lower gate voltage of T3 ($V_{B\text{-}OFF}$) is kept on C_1 and C_2 to maintain T3 turned-on during this period.

$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN1} \frac{(C_2 \parallel C_{OV-T2})}{C_1 + (C_2 \parallel C_{OV-T2})}. \quad (2\text{-}11)$$

In Eq. 2-11, ΔV_{SCAN1} is the voltage difference of V_{SCAN1} between addressing-state and non-addressing-state, and $C_{OV\text{-}T2}$ is the gate-to-source/drain overlap capacitance of T2.

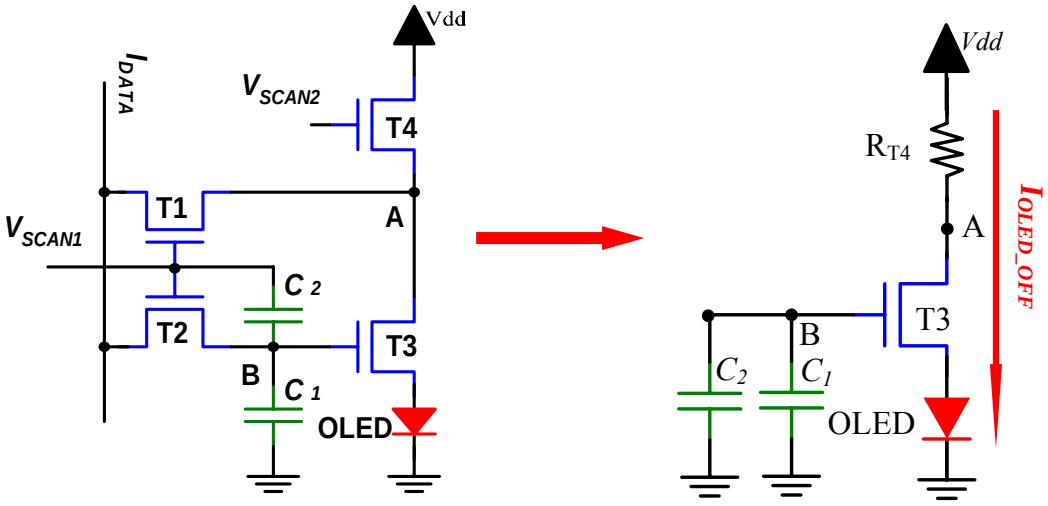


Fig. 2-4. The equivalent circuit diagram of the non-addressing state.

Since the gate voltage of T3 decreases from $V_{B\text{-}ON}$ to $V_{B\text{-}OFF}$, the driving current (I_{OLED_OFF}) is scaled down, which can be represented by the current scaling ratio, R_{SCALE}, defined as:

$$R_{SCALE} = \frac{I_{DATA\_ON}}{I_{OLED\_OFF}}. \quad (2\text{-}12)$$

The quantity of voltage drop shown in Eq. 2-11 is proportional to $\Delta V_{SCAN1}(C_2||C_{OV\text{-}T2})/[C_1+(C_2||C_{OV\text{-}T2})]$ and leads to a small I_{OLED_OFF}. Namely, R_{SCALE} is related to the size of C_1, C_2, $C_{OV\text{-}T2}$ and ΔV_{SCAN1}. Since the small geometric size is adequate for T2, a small $C_{OV\text{-}T2}$ which is connected to the C_2 in parallel can be regarded as a portion of C_2. Therefore the adaptive R_{SCALE} can be achieved by tuning the ratio of the two cascaded capacitors. Consequently, when a very large programming data current I_{DATA} is used to charge the pixel electrode and to shorten the pixel programming time, a small driving current I_{OLED_OFF} can be achieved for low gray scales at the same time.

2.4 Summary

Compared with the current-mirror pixel circuit, the proposed adaptive current scaling pixel circuit has a distinguished capability of shortening programming time delay especially in the low gray levels condition. The current scaling ratio can be achieved by inserting a small storage capacitor to form a cascaded capacitors structure instead of increasing the geometric size of TFTs. The R_{SCALE} is adjusted by tuning the ratio of the two cascaded capacitors without sacrificing the pixel aperture ratio. In the following chapter, software simulation will be utilized to evaluate the performance so that the adaptive current scaling pixel circuit can be realized in the AMOLED applications.

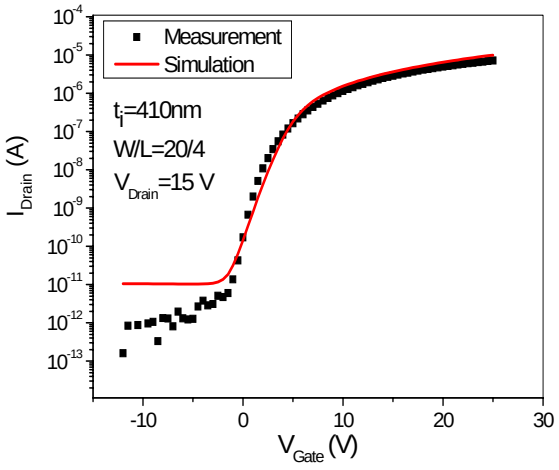
Chapter 3

Simulated Results and Discussions

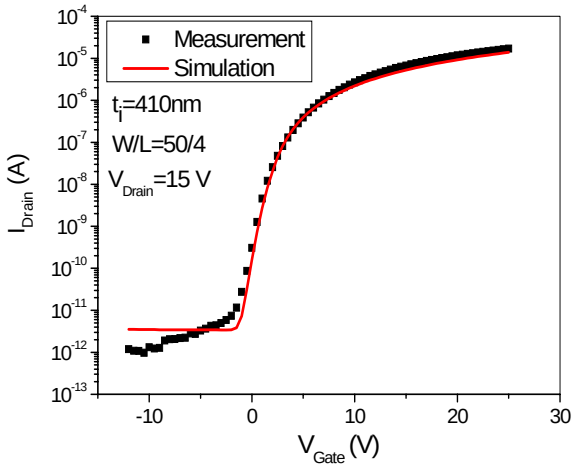
Based on the principle described in Chapter 2, simulation was performed to rudimentarily confirm the features of the adaptive current scaling pixel circuit in the first place as a guide to fabrication.

3.1 Simulation Premise

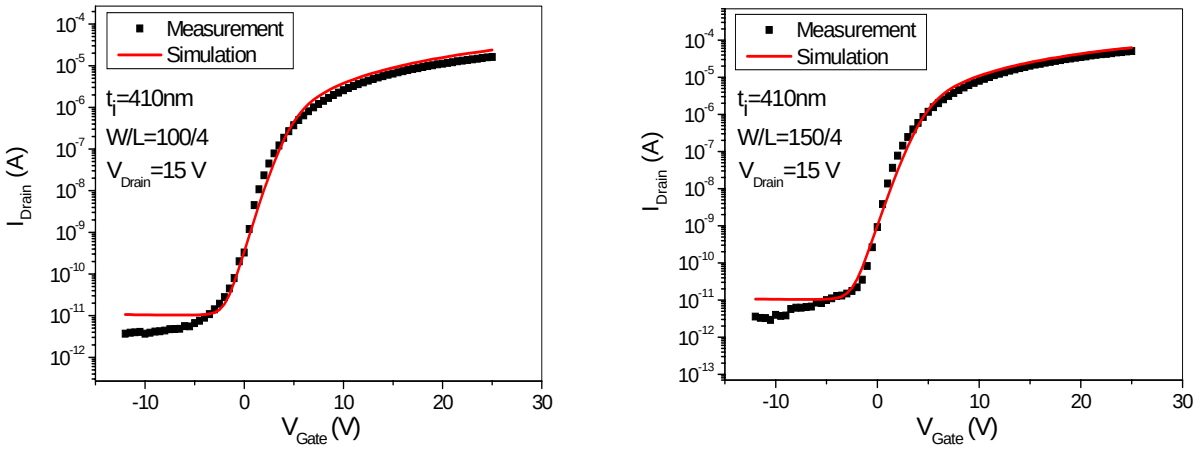
The a-Si:H TFT model was constructed to simulate the current scaling ratio of an adaptive pixel circuit by Synopsis H-SPICE, Rensselaer Polytechnic Institute (RPI). In the beginning, several parameters shown in Fig. 3-1 should be tuned to make this simulated I-V curve in agreement with the measured one of the fabricated sample. According to the results, while the simulated parameters are set as Table 3-1, the simulated I-V curve fits the experimental data shown in Fig. 3-2. Hence, the following simulations on current scaling ratio and programming time delay will be performed in accordance to these parameters.



(a)



(b)



(c) (d)

Fig. 3-1. Comparison of I_{Drain} as a function of V_{Gate} among measurement and simulation results for a-Si:H TFT devices at various channel width (W) (a) 20, (b) 50, (c) 100 and (d) 150 μm while channel length (L), dielectric thickness (t_i) and V_{Drain} were 4 μm, 410 nm and 15 V, respectively.

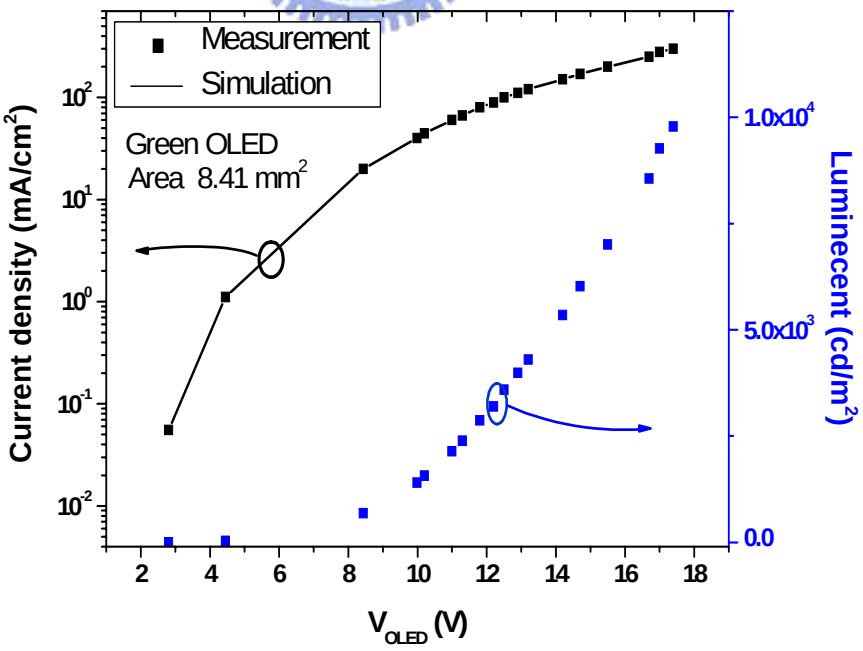


Fig. 3-2. OLED current density and brightness variation with supplied voltages.

Table 3-1. The parameters used in proposed pixel circuit simulation.

Device parameters		
W^a/L^b (T_1, T_3)	(μm)	50/4
W/L (T_2)	(μm)	30/4
W/L (T_4)	(μm)	40/4
V_{TH}	(V)	1.65
μ_{FE}	(cm^2/V-sec)	0.52
C_1	(pF)	2.5
C_2	(fF)	208 ~ 625
Supplied signals		
V_{SCAN1}	(V)	0~30
V_{SCAN2}	(V)	0~30
V_{dd}	(V)	30
I_{DATA}	(μA)	0.2 ~ 10
Time		
t_{ON}	(ms)	0.33
t_{OFF}	(ms)	33

[a] channel width of TFT

[b] channel length of TFT

3.2 Simulation Results and Discussion

3.2.1 Current Scaling Ratio

The proposed current scaling pixel circuit in accordance with the parameters in Table 3-1 is evaluated by the H-SPICE simulation tool and results are shown in Fig. 3-3. In the case of C_2/C_1 = 1/6, the simulation results are listed in the Table 3-2. It is worth noticing that the appropriate voltages are applied on nodes A and B to ensure I_{DATA} of 1 μA through the OLED device. In ideal case, V_A is equal to V_B; however, in practice, V_B is larger than V_A because I_{DATA} through T1 causes a voltage drop between drain and source electrodes of T1. In addition, the voltage drop of V_B results in the decreased I_{OLED} from 1 (= I_{OLED_ON}) to 0.07 μA (= I_{ONED_OFF}). Therefore, the current scaling function is achieved and the current scaling ratio, $R_{SCALE} = I_{OLED\_ON}/I_{ONED\_OFF}$,

is equal to 14.2 so that the programming time can be shortened to 1/14 times than conventional current-driven pixel circuit.

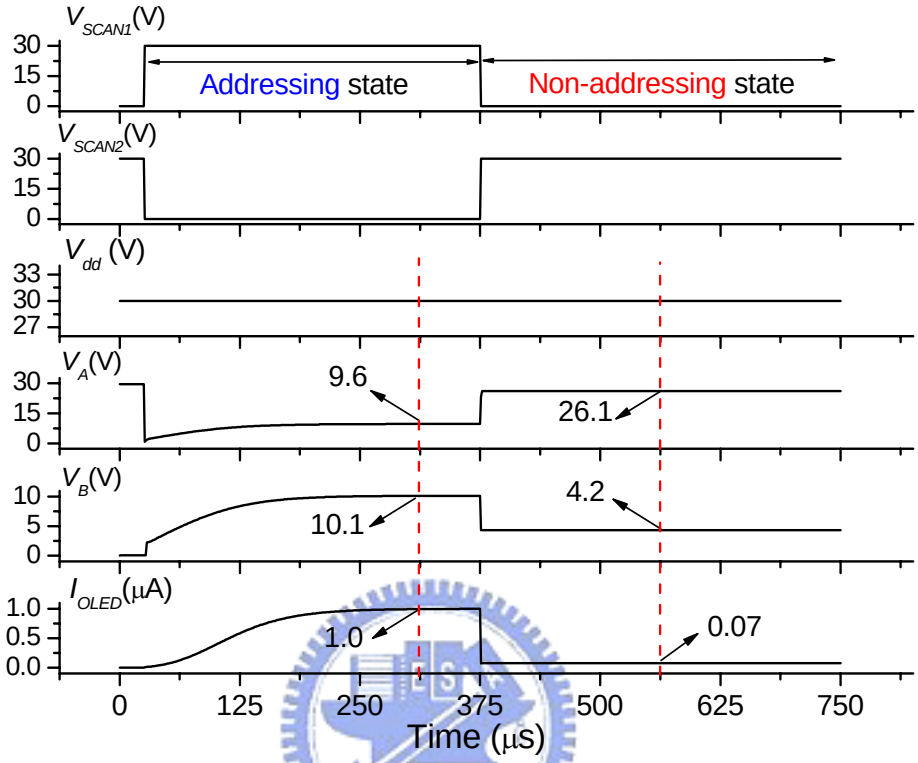


Fig. 3-3. The simulation waveform of proposed pixel circuit.

Table 3-2. Simulation results of proposed pixel circuit in the Fig. 3-3

		Addressing State	Non-Addressing State
V_{SCAN1}	(V)	30	0
V_{SCAN2}	(V)	0	30
V_{dd}	(V)	30	30
V_A	(V)	9.6	26.1
V_B	(V)	10.1	4.2
I_{DATA}	(μA)	1.0	0.07

From Fig. 3-3, the current scaling function has been obtained; however, the variation of R_{SCALE} with I_{DATA} and C_2/C_1 shall be taken into consideration owing to its critical impact on the performance of a proposed pixel circuit. The dependence of R_{SCALE} on the data current as shown in Fig. 3-4 reveals that R_{SCALE} increases as I_{DATA} decreases and R_{SCALE} is adjustable. R_{SCALE} is larger at lower I_{DATA} because larger data current through T3 leads to the larger $V_{B\text{-}ON}$. The voltage drop

$$\Delta V_{SCAN1} \frac{(C_2 \parallel C_{OV-T2})}{C_1 + (C_2 \parallel C_{OV-T2})}$$

is relatively smaller than $V_{B\text{-}ON}$ so that the OLED driving current drop is also slight. In other words, the lower I_{DATA} at lower gray level, the larger OLED driving current drop can be attained. On the other hand, according to Eq. 2-11, the larger ratio of C_2/C_1 yields the larger voltage drop of V_B from addressing state to non-addressing state. Signifying the lower $V_{B\text{-}OFF}$ can bring out the possibly lower I_{OLED_OFF} and the higher R_{SCALE}. By fitting the simulation result, the function of fitting curves in the different ratio of C_2/C_1 can be described as follows:

(1) $C_2/C_1 = 1/4$

$$Y = 8.7524X^{-3.7118} \quad \text{,between in} \quad 0.2 \le X \le 0.5 \qquad (3\text{-}1.1)$$

$$Y = 15.957X^{-2.6356} \quad \text{,between in} \quad 0.5 < X \le 1.0 \qquad (3\text{-}1.2)$$

$$Y = 7.6333X^{-0.6779} \quad \text{,between in} \quad 1.0 < X \le 10.0 \qquad (3\text{-}1.3)$$

(2) $C_2/C_1 = 1/8$

$$Y = 1.3779X^{-1.7890} \quad \text{,between in} \quad 0.2 \le X \le 0.5 \qquad (3\text{-}2.1)$$

$$Y = 2.6612X^{-0.8277} \quad \text{,between in} \quad 0.5 < X \le 1.0 \qquad (3\text{-}2.2)$$

$$Y = 2.1509X^{-0.2177} \quad \text{,between in} \quad 1.0 < X \le 10.0 \qquad (3\text{-}2.3)$$

(3) $C_2/C_1 = 1/12$

$$Y = 1.0657X^{-1.1202} \quad \text{,between in} \quad 0.2 \le X \le 0.5 \qquad (3\text{-}3.1)$$

$$Y = 1.7154X^{-0.4491} \quad \text{,between in} \quad 0.5 < X \leq 1.0 \qquad (3\text{-}3.2)$$

$$Y = 1.4934X^{-0.0899} \quad \text{,between in} \quad 1.0 < X \leq 10.0 \qquad (3\text{-}3.3)$$

where X and Y denote the programming data current and current scaling ratio. Since R_{SCALE} increases greatly with decreasing I_{DATA}, the function of fitting curve is divided into three regions to match simulation accurately. According to these functions at different ratio of C_2/C_1, the adaptive current scaling can be evaluated to meet the display requirements. Moreover, when I_{DATA} is fixed, the increasing rate of R_{SCALE} increases as C_2/C_1 increases from 1/12 to 1/4. In addition, when the sum of all storage capacitor sizes in the proposed pixel circuit is the same as that in a traditional current-driven pixel circuit, the aperture ratio is identical while tuning the ratio of C_2/C_1. In brief, large R_{SCALE} is achieved at low gray levels and low R_{SCALE} is obtained at high gray levels. Hence, an adaptive current scaling ratio is achieved by tuning the ratio of C_2/C_1 without sacrificing aperture ratio.

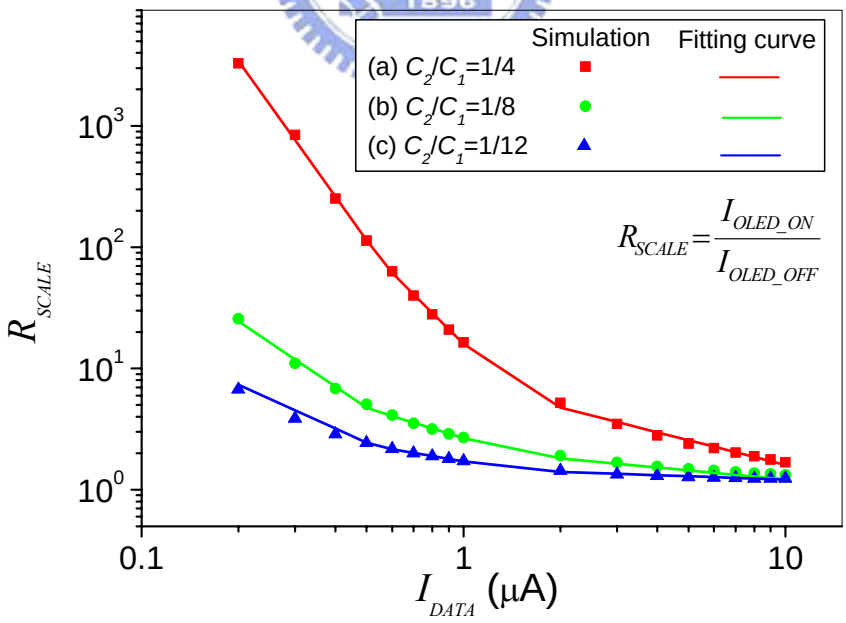


Fig. 3-4. Comparison of R_{SCALE} as function of I_{DATA} among simulation and fitting cutting curve at various C_2/C_1 (a) 1/4, (b) 1/8 and (c) 1/12 in the proposed

pixel circuit shown in Fig. 2-2.

The current scaling function is implemented to reduce the programmed current from addressing state to non-addressing state. Since I_{OLED_ON} (=I_{DATA}) is larger than I_{OLED_OFF} by a factor of R_{SCALE}, the average OLED current (I_{AVG}) for the pixel circuit is

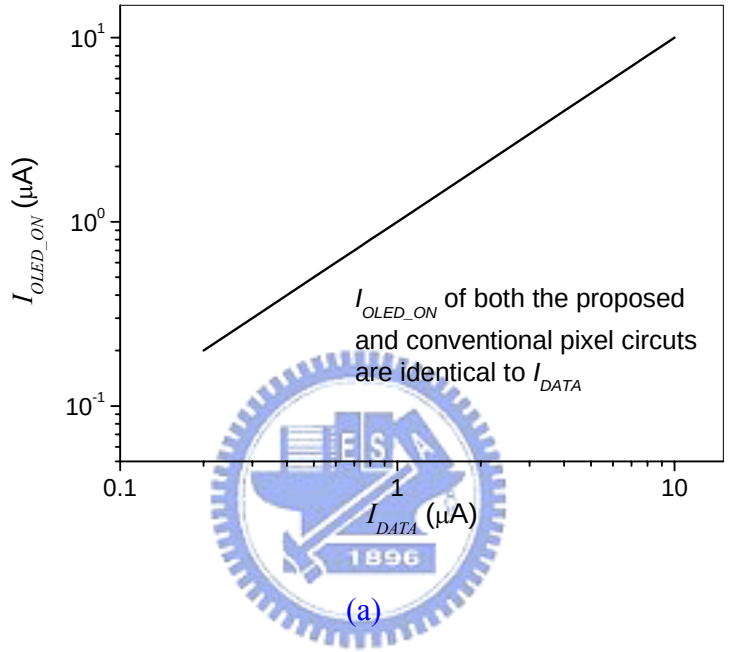
$$I_{AVG} = \frac{I_{OLED\_ON} t_{ON} + I_{OLED\_OFF} t_{OFF}}{t_{ON} + t_{OFF}}, \quad (3\text{-}4)$$

where t_{ON} and t_{OFF} denote the addressing and non-addressing state periods during the frame time, respectively. Meanwhile, the I_{AVE} can also be rewritten by Eq. 2-12 as :

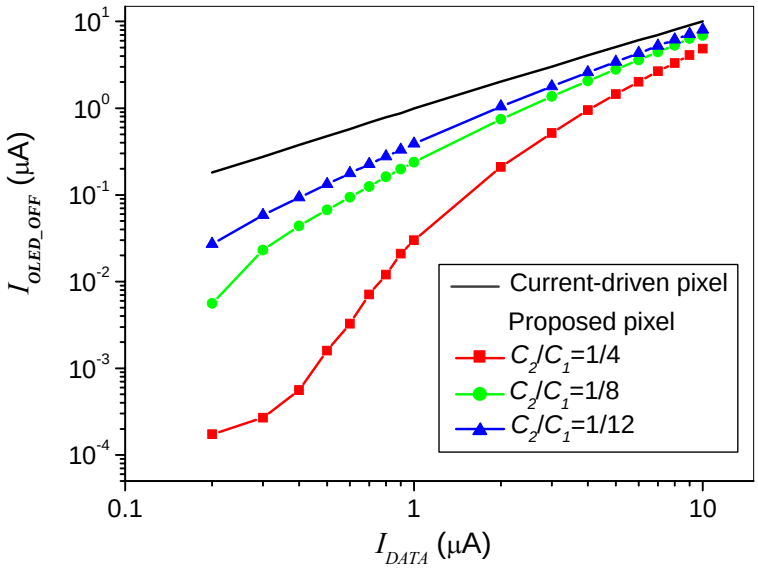
$$I_{AVG} = I_{OLED\_OFF}\left[\frac{R_{SCALE} t_{ON} + t_{OFF}}{t_{ON} + t_{OFF}}\right]. \quad (3\text{-}5)$$

Evidently adjusting I_{OLED_OFF} and R_{SCALE} controls I_{AVE} to achieve different gray levels for display. Subsequently, t_{ON} of 0.33 ms and t_{OFF} of 33 ms are adopted to calculate the variation of OLED current during a frame time as shown in Fig. 3-5. For the addressing state, both conventional current-driven pixel circuit and proposed one provide the I_{OLED_ON} identical to I_{DATA} because the current is directly supplied by external driver shown in Fig. 3-5(a). However, for the non-addressing state, the proposed pixel circuit reveals the lower current than the conventional one does whose I_{OLED_OFF} is equivalent to I_{OLED_ON} as shown in Fig. 3-5(b). In addition, the larger ratio of C_2/C_1 always yields more rapid decrease in I_{OLED_OFF}. Moreover, t_{ON} is much longer than t_{OFF}, the small I_{OLED_OFF} in the non-addressing state can further reduce the I_{AVG} even if the I_{OLED_ON} is large. According to Eq. 3-4, the I_{AVG} is dependent on I_{DATA} with different ratio of C_2/C_1 in one frame period as shown in Fig. 3-5(c). At the ratio of C_2/C_1 =1/4, the proposed pixel circuit can generate the I_{AVG} ranging from 2 nA to 5 μA while I_{DATA} is changed between 0.2 and 10 μA. By contrast, the I_{AVG} of the conventional pixel circuit is almost equal to I_{DATA}, implying that there is no current scaling function. From applying these abovementioned results, it is evident that

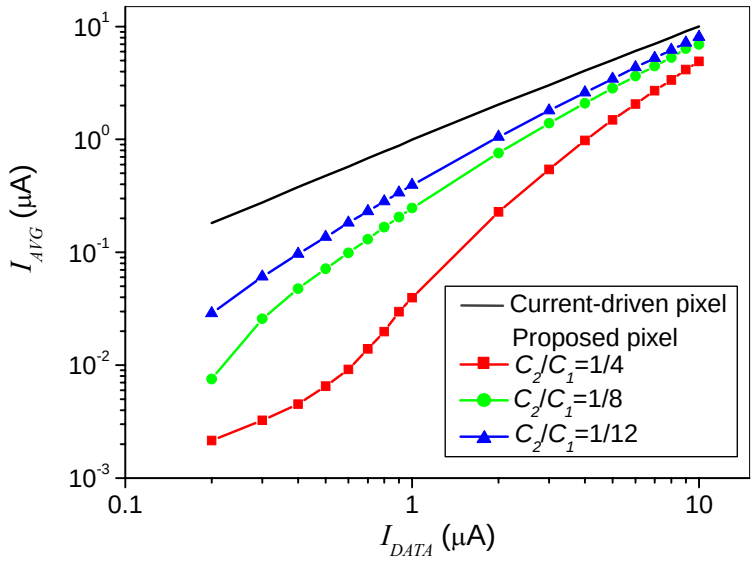
proposed pixel circuit in address state can provide larger I_{DATA} than I_{AVE} without increasing the a-Si:H TFTs geometric size. Hence, a large R_{SCALE} can be achieved by inserting a small storage capacitor (C_2) to form a cascaded structure of storage capacitors and a high I_{DATA} can be used to accelerate the programming time in the addressing state accordingly.



(a)



(b)



(c)

Fig. 3-5. Comparison of (a) I_{OLED_ON}, (b) I_{OLED_OFF} and (c) I_{AVG} as a function of I_{DATA} among current-driven pixel shown in Fig. 1-1 and proposed pixel shown in Fig. 2-2 at various C_2/C_1 ratio during one frame period while t_{ON} = 0.33 ms and t_{OFF} = 33 ms.

Going a step further, compared to the current-mirror circuit which can only provide a constant R_{SCALE}, the proposed pixel circuit is obviously more outstanding because of the adjustable R_{SCALE} and large aperture ratio. The I_{AVG} as a function of I_{DATA} is shown in Fig. 3-6. The proposed pixel circuit achieves the wider range of I_{AVG} from 2 nA to 5 μA compared with the current-mirror pixel (0.05 to 2.8 μA). Meanwhile, the R_{SCALE} is adjusted by the I_{DATA}. However, the current–mirror pixel circuit is able to scale down I_{DATA}, R_{SCALE} is constant in the whole range of I_{DATA}. In addition, to achieve larger R_{SCALE} requires a larger driving TFT in current-mirror pixel circuit and results in lower aperture ratio. Hence, not only high I_{DATA} and large R_{SCALE} for the low gray levels that can shorten programming time but also reasonable I_{DATA} for high gray levels that can avoid large display power consumption can be obtained

concomitantly in proposed pixel circuit without sacrificing aperture ratio.

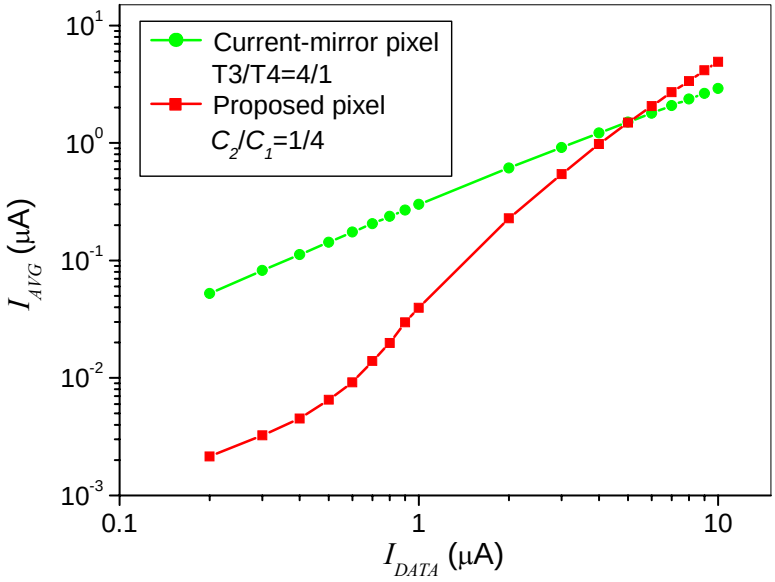


Fig. 3-6. Comparison of I_{AVG} as a function of I_{DATA} among current-mirror pixel shown in Fig. 2-1 and proposed pixel shown in Fig. 2-2 at t_{ON} = 0.33 ms and t_{OFF} = 33 ms.

3.2.2 Programming Time

As discussed in chapter 2, the current scaling function can effectively shorten programming time. In the section, the total programming time (T_{PROG}) is calculated based on Eq. 2-1 to Eq. 2-6 and the parameters are listed in the Table 3-3. The T_{PROG} as a function of display size is shown in Fig. 3-7. Without current scaling function (R_{SCALE} = 1), a XGA display requires T_{PROG} of 89 ~ 90 μs to charge up the conventional current-driven pixel circuit which is four times longer than the scan pulse width (T_{SCAN}) of 21.7 μs at 60 Hz frame rate. Therefore, conventional current-driven pixel circuit is inapplicable for a large size and a high resolution display. In contrast, the current-driven pixel circuit with current scaling function (R_{SCALE} = 20) can reduce the T_{PROG} effectively. Furthermore, as display resolution

increases to UXGA, the T_{PROG} is 7 ~ 8 μs which is lower than T_{SCAN} of 10 μs even for display diagonal of 40 inch. Hence, the proposed pixel circuit with cascaded structure of storage capacitors and build-in current scaling capability can allow the realization of a high resolution and large size current-driven AMOLED display.

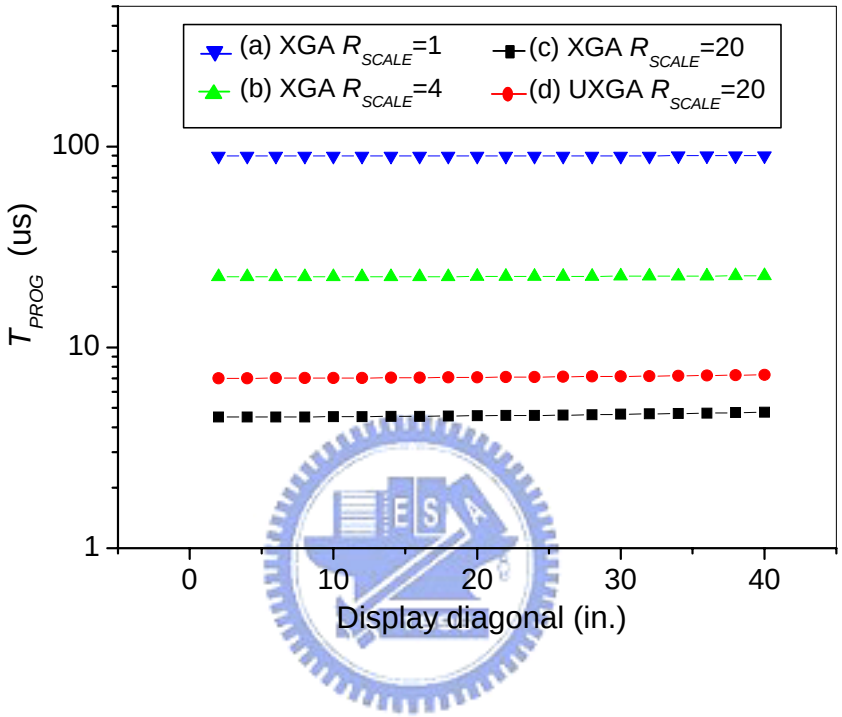


Fig. 3-7. T_{PROG} as a function of display diagonal with a scan line made from Cu at (a) XGA R_{SCALE} = 1, (b) XGA R_{SCALE} = 4, (c) XGA R_{SCALE} = 20 and (d) UXGA R_{SCALE} = 20.

Table 3-3. The parameters including TFT materials and OLED device for calculating total programming time.

OLED device			TFT material		
V_{DATA}	(V)	5	$C\square$	($\mu F/m^2$)	150
C_E	(V^{-1})	0.44	$R\square$	(Ω/sqr)	0.075
C_V	(lm/W)	427	C_{OV}	(nF/m)	0.2
L	(cd/m^2)	100			
C_n		1.1			
η	(%)	5			

ps : Z = 30

3.3 Summary

We have designed an adaptive current scaling pixel circuit with a-Si:H TFT technology for shortening programming time delay without sacrificing aperture ratio. From the calculation of the total programming time, we can infer that the proposed pixel circuit has an outstanding ability to improve programming time delay even though the resolution and display size are more than 1600*1200 and 40 inch, respectively. In addition, the adaptation rate of R_{SCALE} can be adjusted by tuning the ratio of the two cascaded capacitors without sacrificing pixel aperture ratio. In comparison with conventional current-driven and the current-mirror pixel circuits, the widest range of I_{AVG} from 2 nA to 5 μA for I_{DATA} ranging from 0.1 to 10 μA can be achieved by the proposed adaptive current scaling pixel circuit. As a result, both the current scaling function and the reasonable power consumption can be easily accomplished.

Chapter 4

Fabrication and Measurement Instruments

4.1 a-Si:H TFT Fabrication Process

In this section, a prototype to characterize the features of the current scaling pixel structure is fabricated by the standard processes of a conventional inversed-staggered back-channel-etch a-Si:H TFT technologies.

Typical process flow for inversed-staggered back-channel-etch a-Si:H TFT [Fig. 4-1]

1. Gate metal deposition on the glass substrate by sputtering method.
2. **Mask #1** : TFT gate electrodes formation, Fig. 4-1(a).
3. Deposition of gate dielectric layer, Fig. 4-1(b).
4. Sequential deposition of a-Si:H and n+ a-Si:H layers are formed by Plasma Enhanced Chemical Vapor Deposition (PECVD), Fig. 4-1(c).
5. **Mask #2** : active island definition, Fig. 4-1(d).
6. Source/Drain metal deposition by sputtering method.
7. **Mask #3** : Source/Drain electrodes definition, Fig. 4-1(e).
8. n+ a-Si:H back-channel-etch by the dry etching process, Fig. 4-1(f).
9. Deposition of SiN_x layer.
10. **Mask #4**: Indium-tin-oxide (ITO) electrode contact hole definition, Fig. 4-1(g).
11. Deposition of ITO layer.
12. **Mask #5**: ITO electrode definition, Fig. 4-1(h).

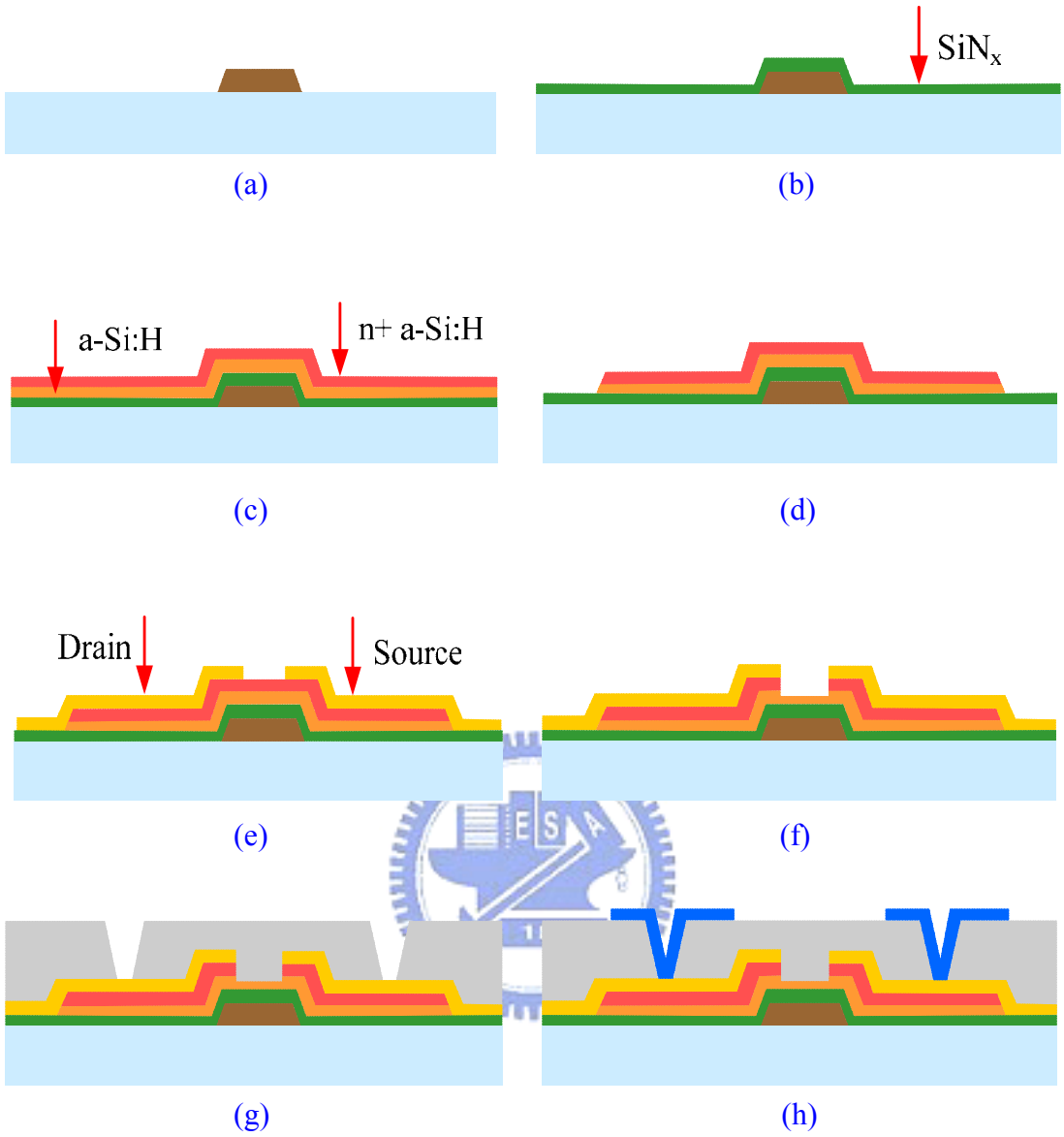


Fig. 4-1. Process flow for inversed-staggered back-channel-etch a-Si:H TFT.

4.2 Organic Light Emitting Diode Fabrication Process

After the fabrication of the current scaling pixel circuit, an OLED device is deposited onto the TFT backplane to demonstrate the unique performance of the current scaling pixel circuit. The well-known structure of bottom-emission OLED device, ITO / CuPc / NPB / Alq_3 / LiF / Al, is chosen because of its advantages such as high efficiency and stability. All of the device architectures and material structures are shown in Fig. 4-2. These small molecule layers are deposited sequentially by a vacuum evaporation process in a chamber to form several parallel thin films which

are important for the lifetime of the device as shown in Fig. 4-3.

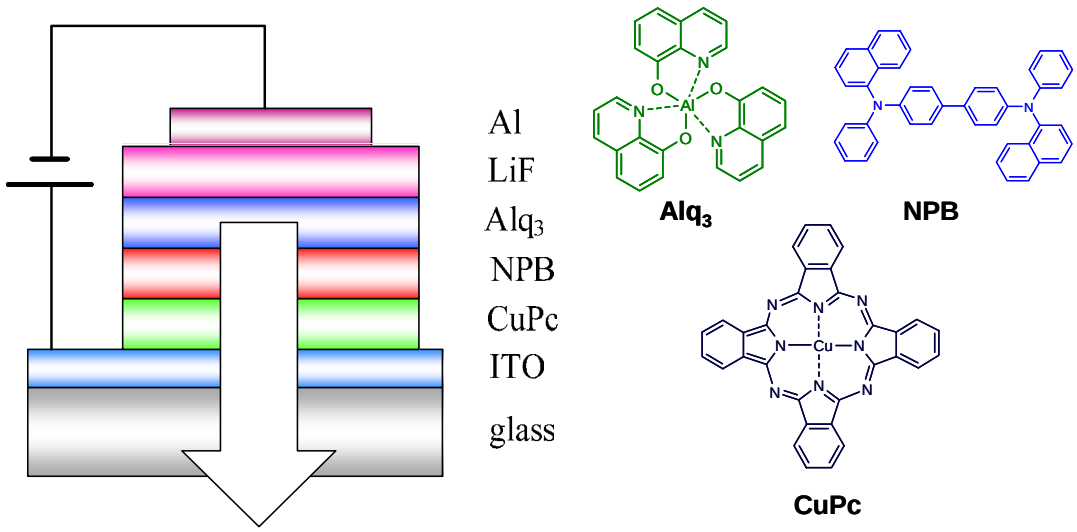


Fig. 4-2. The schematic architecture and molecular structures of bottom-emission OLED device.

Fig. 4-3. Thermal coater system for OLED fabrication.

4.3 Measurement System

After fabricating the current scaling pixel circuit and an OLED device, the

experiments were conducted to confirm that the fabricated sample performs in agreement with the original design. The instruments including electrical properties analysis system, testing circuitry system and ConoScope will be introduced in the following subsections.

4.3.1 Electrical Properties Analysis System

The electrical property analysis system mainly consists of Agilent 4156A semiconductor analyzer and 41501B pulse generator as shown in Fig. 4-4. An Agilent 4156A semiconductor analyzer with a probe station is used to analyze the electrical properties of a circuit such as I-V measurement or bias-temperature-stress (BTS). The ground probe station is furnished with an electrically isolated, water-cooled thermal plate within an optical shielding box. The plate can be controlled by Temptronic TPO315A thermal controller between 25°C and 300°C. The source measurement units (SMUs) are used to control voltage sources where current flowing through can be measured. The voltage or current sources supplied by Agilent 4156A semiconductor analyzer can be transmitted through SMU to the pixel circuit and the output voltage or current will be detected concomitantly.

In addition, the 41501B pulse generator is employed to create wave function signals which Agilent 4156A semiconductor analyzer cannot provide. Consequently, combining Agilent 4156A semiconductor analyzer with 41501B pulse generator can advance the application for electrical property analysis.

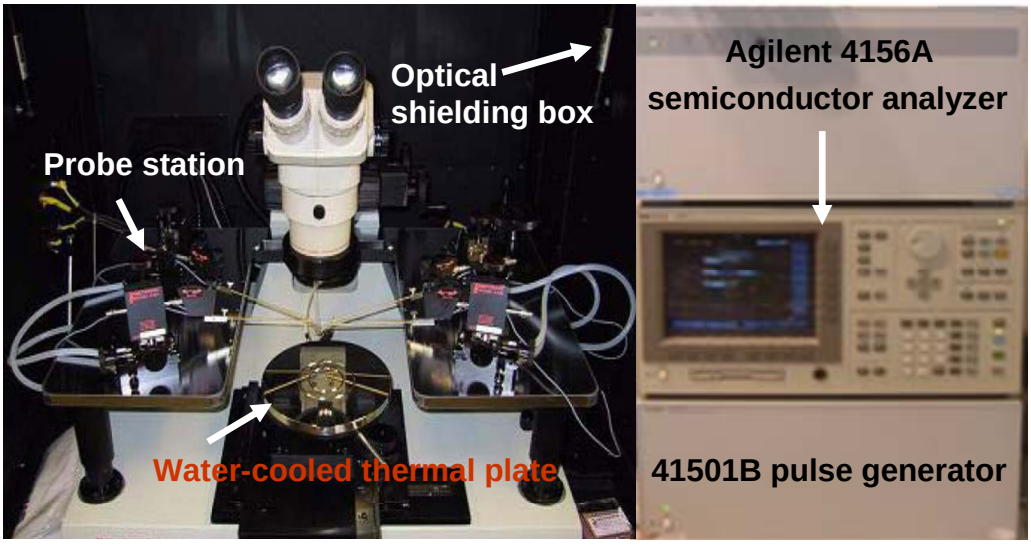


Fig. 4-4. Electrical property analysis system with Agilent 4156A semiconductor analyzer, 41501B pulse generator, and probe station.

4.3.2 Testing Circuitry Systems

The testing circuitry system is composed by a function generator and a micro-ampere (μA) level power supply to drive the adaptive current scaling pixel AMOLED device. The function generator can generate rectangular, triangular and sine waves with frequency limitation of 2 MHz as shown in Fig. 4-5. Due to the amplitude of signal wave is not high enough to turn on the switching TFT, the adjustable amplifier circuit is necessary to amplify the amplitude to a proper voltage level. After amplifying, the signal passing through buffer and inverse circuits can synchronously produce the non-inverse and inverse signals for the operation of adaptive current scaling pixel AMOLED device.

On the other hand, in the μA level power supply there are 24 channels and the resolution of 100 nano-ampere (nA) can be achieved shown in Fig. 4-6. By using the variable resistor, the output current can be adjusted from 1 uA to 1 milli-ampere (mA).

Fig. 4-5. The GFG-8020H function generator.

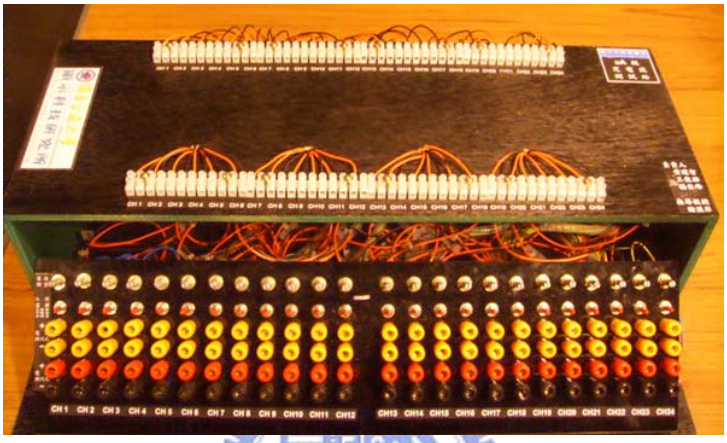


Fig. 4-6. The micro-ampere level power supply.

4.3.3 ConoScope

The ConoScope is used for visual performance evaluation such as luminance, contrast ratio, color shift, gray scale and so on shown in Fig. 4-7. In principle, the light from the test area will be focused by a set of lenses so that all beams emerging from the sample in the same direction will meet in one spot in the so called focal plane. Hence, all parallel beams can be projected on one spot in the focal plane by the ConoScope lens. The resulting figure is called the "conoscopic figure". It represents that each spot on the focal plane corresponds to one specific direction of the viewing cone. The conoscopic figure directly shows color and luminance as they would have been plotted in a polar coordinate system shown in Fig. 4-8.

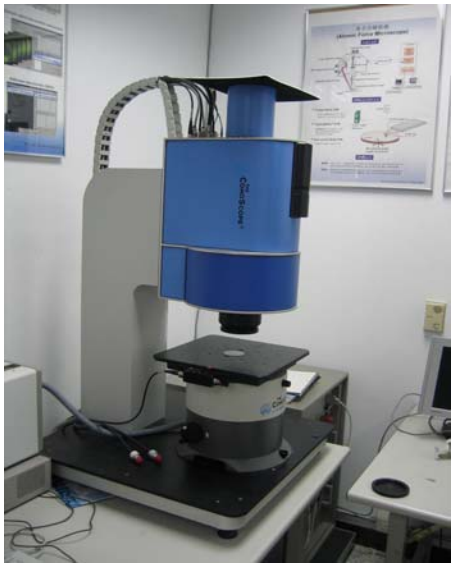


Fig. 4-7. The visual performance evaluation system of ConoScope instrument.

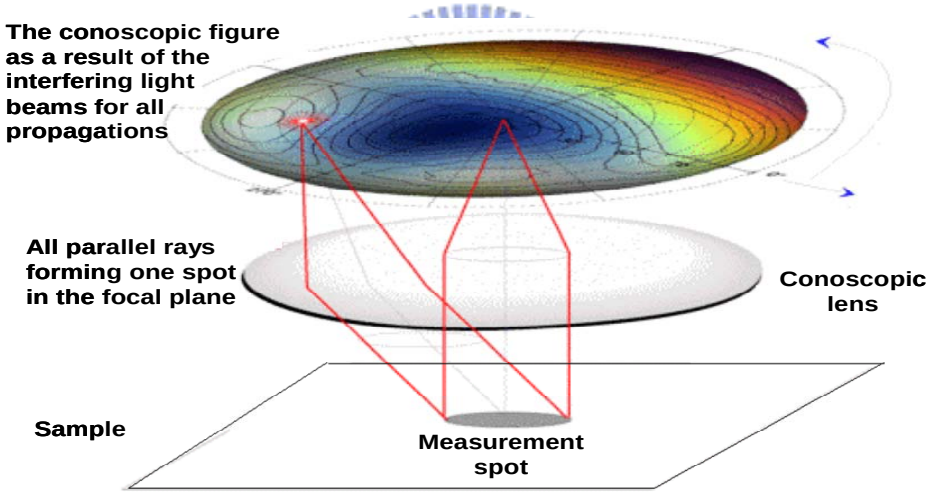
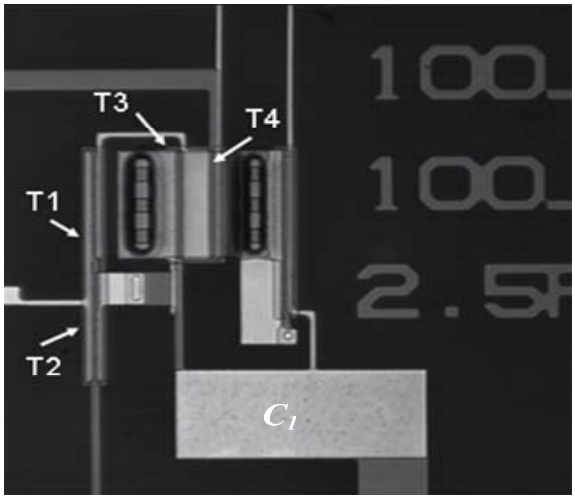


Fig. 4-8. Illustrations of ConoScope detector.

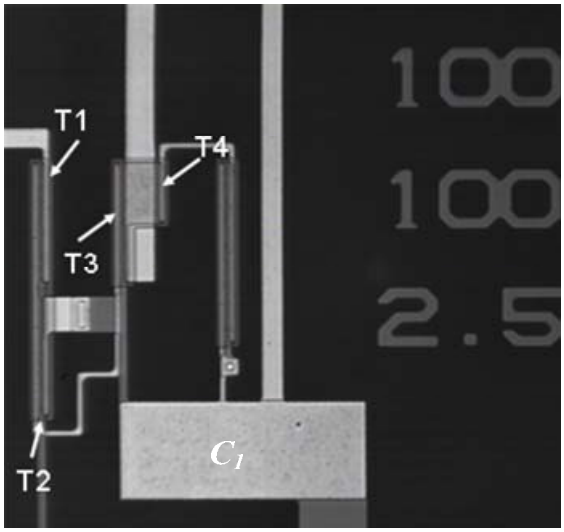
Chapter 5

Experimental Results and Discussions

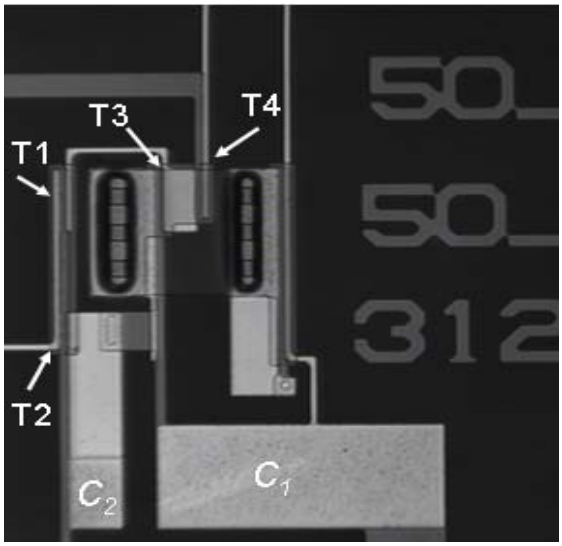
After simulation and fabrication, the experiments were implemented to examine the calculation. In this chapter, the electrical characteristics and reliability among conventional current-driven, current-mirror and adaptive current scaling pixel circuits were compared and the feature was characterized by optical microscope shown in Fig. 5-1. Besides, OLED materials were deposited onto the a:Si:H TFT panel to form single pixel AMOLED devices so as to analyze the visual performance.



(a)



(b)



(c)

Fig. 5-1. A photograph of (a) current-driven, (b) current-mirror and (c) adaptive current scaling pixel circuits fabricated by a-Si:H TFT technologies.

5.1 Electrical Characteristics

5.1.1 Current Scaling Ratio

As the discussed simulation results in Chapter 3, the proposed adaptive current scaling pixel circuit revealed the outstanding current scaling function in comparison with conventional current-driven and current-mirror pixel circuits. Next, we would

measure the pixel circuits with different ratios of cascaded storage capacitors and geometric sizes of TFT to observe the variation of current scaling ratio.

First, in the proposed pixel circuit, the device parameters and measurement conditions were listed in Table 5-1 and Table 5-2. The R_{SCALE} as a function of I_{DATA} at various ratio of C_2/C_1 was shown in Fig. 5-2. From the measurement results, when the ratio of C_2/C_1 was equal to 1/4, the R_{SCALE} increased from 1.8 to 950 as I_{DATA} decreased from 10 to 0.2 μA shown as the dot line in Fig. 5-2. It was clearly indicated that not only the large R_{SCALE} at low gray levels but also low R_{SCALE} at high gray levels were achieved so that the R_{SCALE} was adjusted by input data current. On the other hand, when I_{DATA} was fixed, the larger ratio of C_2/C_1 yielded larger the increasing rate of R_{SCALE}. The results were also identical to the above simulation. Hence, an adaptive current scaling pixel circuit was successfully demonstrated.

Table 5-1. The parameters of fabricated device for proposed pixel circuit.

		Device parameter
W[a]/L[b] (T_1)	(μm)	50/4
W/L (T_2)	(μm)	30/4
W/L (T_3)	(μm)	50/4
W/L (T_4)	(μm)	40/4
C_1	(pF)	2.5
C_2	(fF)	208 ~ 625

[a] channel width of TFT
[b] channel length of TFT

Table 5-2. The parameters used in the condition of measurement.

Supplied signals		
V_{SCAN1}	(V)	0~30
V_{SCAN2}	(V)	0~30
V_{dd}	(V)	30
I_{DATA}	(μA)	0.2 ~ 10
Frame time		
t_{ON}	(ms)	0.33
t_{OFF}	(ms)	33

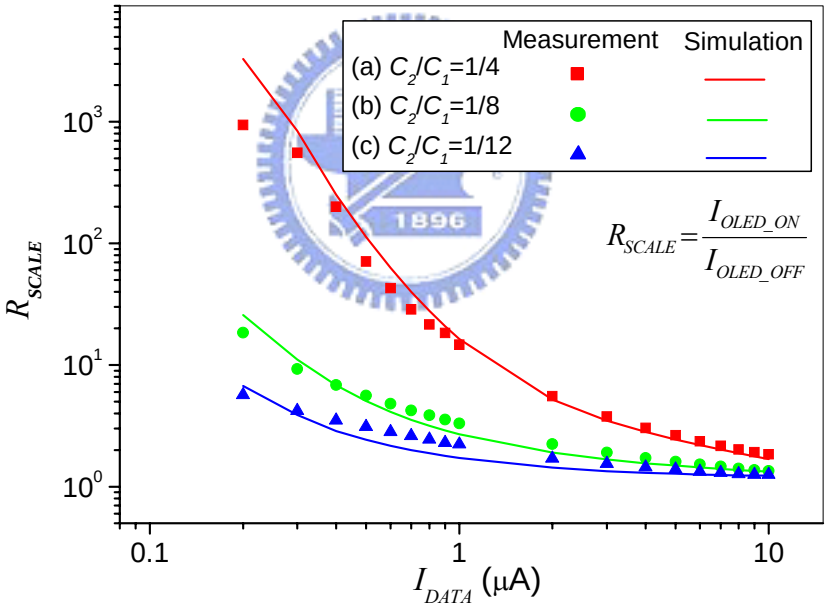


Fig. 5-2. Comparison of R_{SCALE} as a function of I_{DATA} among measurement and simulation results at various C_2/C_1 (a) 1/4, (b) 1/8 and (c) 1/12 in proposed pixel circuit shown in Fig. 2-2.

As mentioned before, the current scaling ratio was adjusted by tuning the ratio of C_2/C_1. To investigate the variation of current scaling ratio with different geometric

size of TFTs, we would focus on different channel width of T1, T3 and T4 to evaluate R_{SCALE} variation while T2 was ignored due to the less current passing through T2. In the following case, the channel length of all TFTs, channel width of T2, the capacitance of C_1 and C_2 were fixed in 4 μm, 30 μm, 2.5 pF and 312 fF, respectively.

(1) In the case of T1:

The R_{SCAL} was dependent on I_{DATA} with different channel width of T1 shown in Fig. 5-3 (a). With increasing the channel width of T1, the R_{SCALE} was increased as the channel width of T3 and T4 were 50 and 40 μm. Since the turn-on resistance of T1 (R_{T1}) was decreased with increasing the channel width of T1, $V_{B\text{-}ON}$ was close to V_A resulted in the lower $V_{B\text{-}ON}$ was. Based on Eq. 2-11, the lower $V_{B\text{-}ON}$ would cause significant decrease of $V_{B\text{-}OFF}$. Therefore, the lower I_{OLED_OFF} was achieved by increasing the channel width of T1. In other words, the larger R_{SCALE} was obtained in the longer channel width of T1.

(2) In the case of T3:

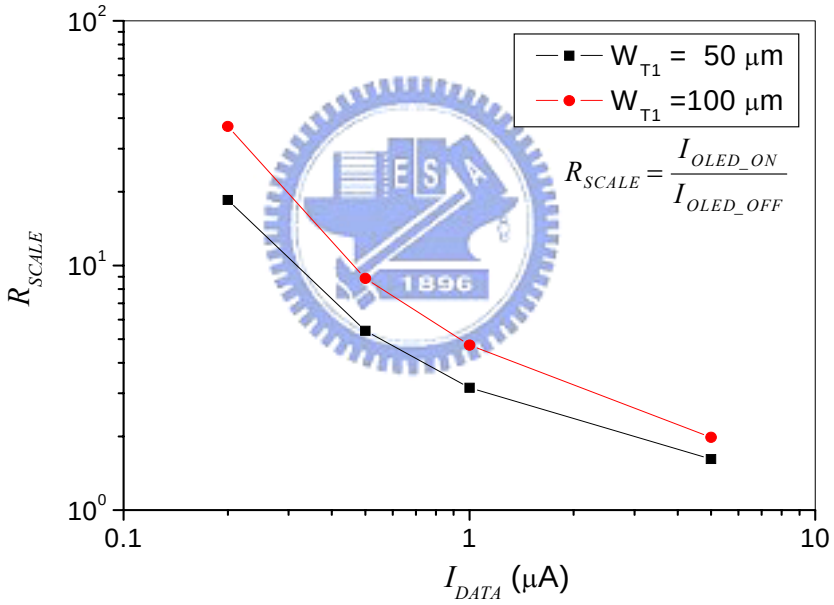
According to Eq. 2-7, in the constant current passing through driving TFT (T3), the longer channel width of T3 caused the lower $V_{B\text{-}ON}$. As mentioned of the above case, the lower $V_{B\text{-}ON}$ would result in larger R_{SCALE}. Hence, in the experimental result, the larger R_{SCALE} was accompanied with the longer channel width of T3 as shown in Fig. 5-3 (b).

(3) In the case of T4:

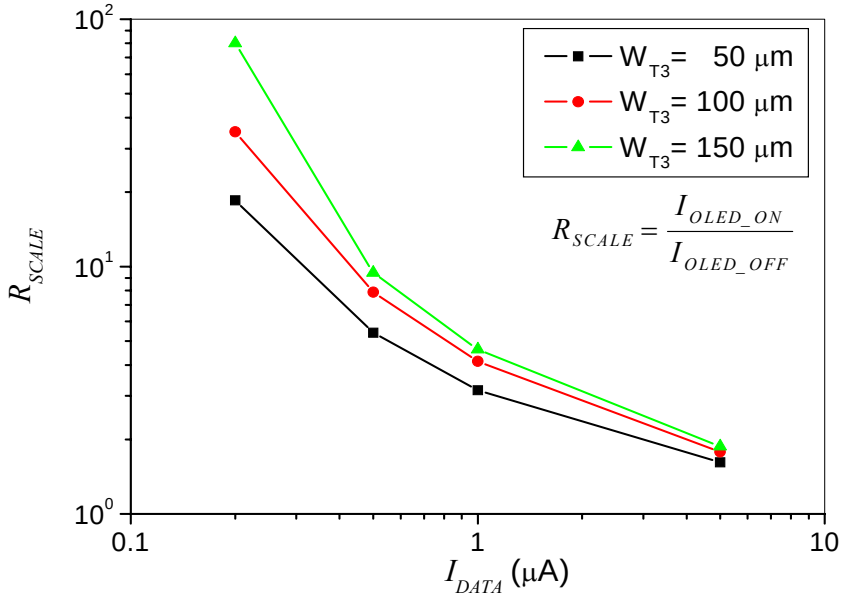
When the channel width of T4 increased, the turn-on resistance of T4 (R_{T4}) would decrease. In the non-addressing state, the current passing through T4 caused the voltage drop (V_{T4}) across the T4. When the channel width of T4 was decreased, the low R_{T4} was obtained so that low V_{T4} was achieved. Hence, the V_A in the non-addressing state was equal to $Vdd - V_{T4}$. Since T3 operated in the saturation region, if the drain voltage of T3 (V_A) was gradually increasing, the I_{OLED_OFF} was

also simultaneously increased due to the kink effect. It would be derived that the influence of kink effect on the longer channel width of T4 was more significant resulted in the larger I_{OLED_OFF} and the measurement result was shown in Fig. 5-3 (c).

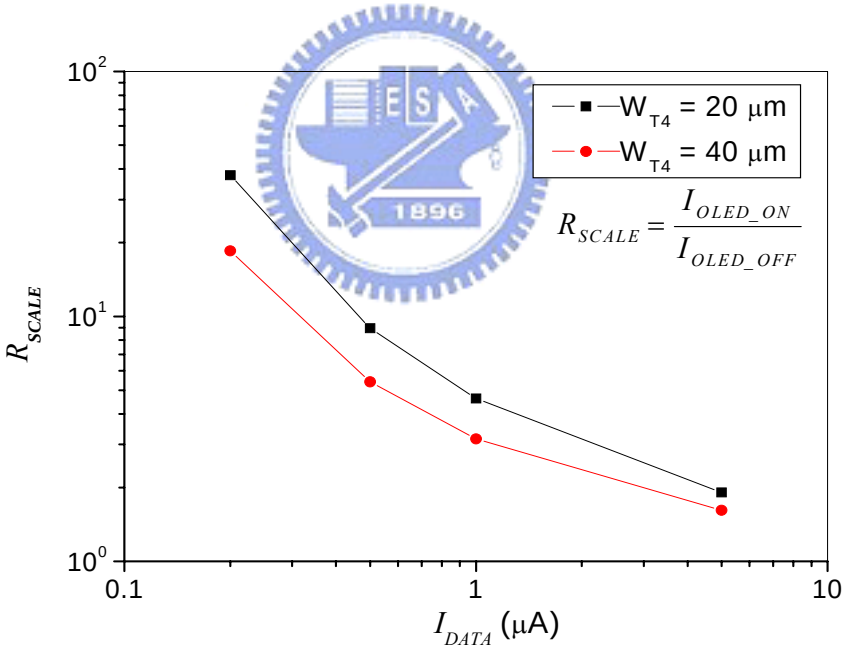
With the analysis of the above, we could conclude that the current scaling ratio would be adjusted by not only the cascaded storage capacitors but also the channel width of T1, T3 and T4. The longer channel width of T1 and T3 and the shorter channel with of T4 would cause the larger current scaling ratio. Hence, to be optimum current scaling ratio, we should consider both the ratio of cascaded capacitance and the channel width of TFTs.



(a)



(b)



(c)

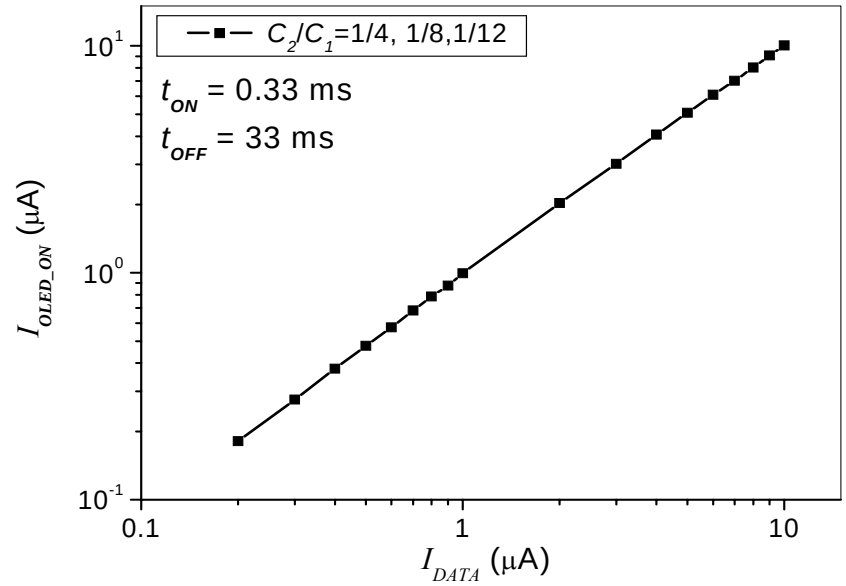
Fig. 5-3. The R_{SCALE} as a function of I_{DATA} at various channel width of (a) T1, (b) T3 and (c) T4 in proposed pixel circuit shown in Fig. 2-2.

The purpose of current scaling function was to shorten programming time with

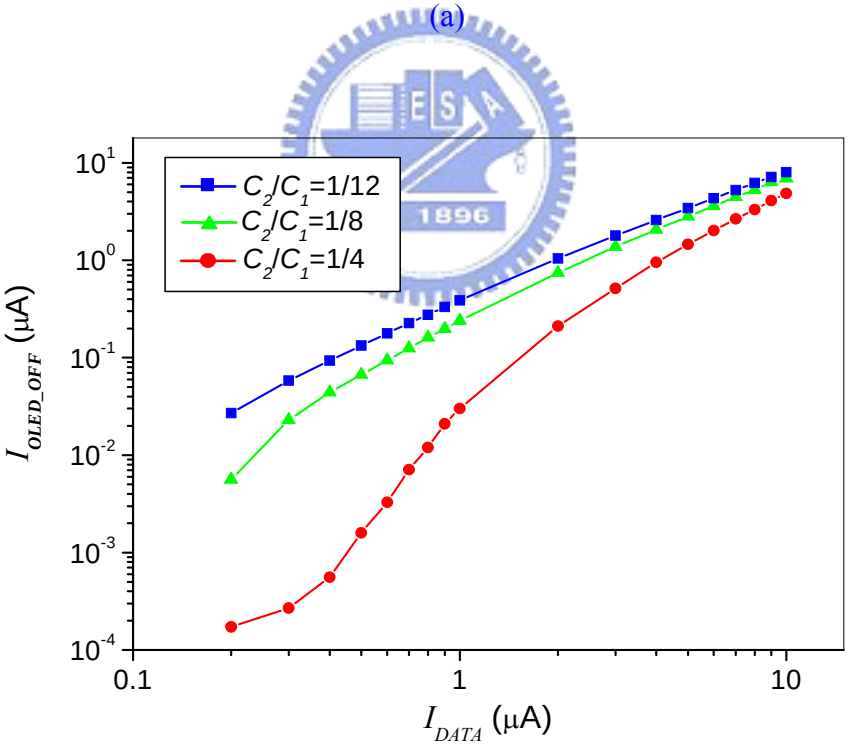
high programming data current charged the parasitic capacitor and storage capacitor at the low gray levels. The dependence of OLED current with different the ratio of C_2/C_1 on I_{DATA} during a frame period was shown in Fig. 5-4 and ensure that t_{ON} and t_{OFF} were 0.33 and 33 ms in one frame period, respectively. In the addressing state, the I_{OLED_ON} was equal to I_{DATA} no matter the C_2/C_1 ratio changed from 1/4 to 1/12. During the transition from addressing state to non-addressing state, at I_{DATA} of 0.2 μA, the OLED driving current in the non-addressing state, I_{OLED_OFF}, was scaled down to 0.17, 5 and 20 nA while the ratio of C_2/C_1 was equal to 1/4, 1/8 and 1/12, respectively. It revealed that the larger ratio of C_2/C_1 caused significant decrease of I_{OLED_OFF} so that the result corresponded to Eq. 2-9. On the other hand, at I_{DATA} of 10 μA, the I_{OLED_OFF} was scaled down to 4.8, 6.9 and 8.0 μA while the ratio of C_2/C_1 was equal to 1/4, 1/8 and 1/12, respectively. It meant that the amount of current drop at lower I_{DATA} was more than that at higher I_{DATA} due to the lower I_{DATA} passed through T3, the lower $V_{B\text{-}ON}$ was. Hence, the voltage drop of

$$\Delta V_{SCAN1} : \frac{C_2 \parallel C_{OV-T2}}{C_1 + C_2 \parallel C_{OV-T2}}$$

was relatively larger than $V_{B\text{-}ON}$ resulted in the larger current drop of I_{DATA} so that the larger R_{SCALE} was obtained at lower gray levels.



(a)



(b)

Fig. 5-4. The (a) I_{OLED_ON} and (b) I_{OLED_OFF} as a function of I_{DATA} at various C_2/C_1 during a frame period in proposed pixel circuit shown in Fig. 2-2.

As described in Chapter 3, the conventional current-driven pixel circuit does not have the capability of current scaled down no matter the geometric size of TFTs changed or not. In the experimental results, the parameters of conventional current-driven pixel circuit and measurement condition were listed in Table 5-3 and Table 5-2, respectively. The OLED current of conventional current-driven pixel circuit in the addressing state was the same with Fig. 5-4 (a). When pixel circuit worked in the non-addressing state, the I_{OLED_OFF} was still identical to I_{DATA} regardless of the channel width of driving TFT (T4) increased from 50 to 150 μm shown in Fig. 5-5.

Table 5-3. The parameters of fabricated device for conventional current-driven pixel circuit.

		Device parameter	
W[a]/L[b]	(T_1)	(μm)	100/4
W/L	(T_2)	(μm)	100/4
W/L	(T_3)	(μm)	100/4
W/L	(T_4)	(μm)	50/4~150/4
C_1		(pF)	2.5

[a] channel width of TFT
[b] channel length of TFT

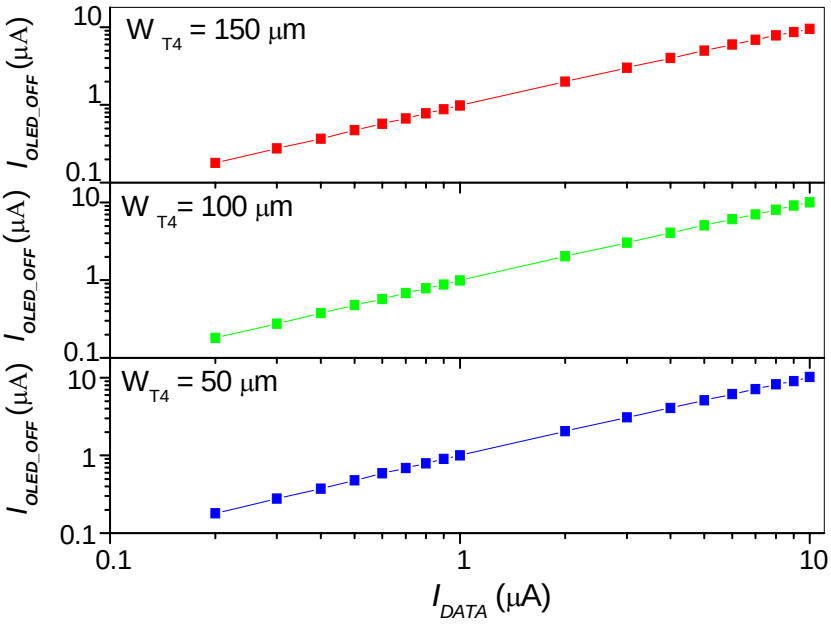


Fig. 5-5. The I_{OLED_OFF} as a function of I_{DATA} during a frame period at various channel width of T4 = 150, 100 and 50 μm in the current-driven pixel circuit shown in Fig. 1-3.

As to conventional current-mirror pixel circuit, the OLED current was dependent on the I_{DATA} with different geometric sizes of T3 during a frame period as shown in Fig. 5-6 and the parameters and measurement condition of current-mirror pixel circuit were listed in Table 5-4 and Table 5-2. In the addressing state, the I_{OLED} as a function of I_{DATA} was shown in Fig. 5-6 (a). Clearly, the ratio of I_{DATA}/I_{OLED} was direct proportion to geometric size ratio of T3/T4. In the case of T3/T4 = 1/2, I_{OLED} enlarged from 0.15 to 5.7 μA while the I_{DATA} increased from 0.2 to 10 μA. In ideal condition, the ratio of I_{DATA}/I_{OLED} was equal to the ratio of T3/T4. However, in this case, the I_{OLED} was larger than that of ideal condition due to the high V_{dd} induced kink effect resulted in the increase of I_{OLED}. In the non-addressing state, although the I_{OLED} still kept linear relationship with I_{DATA}, the I_{OLED} in the addressing state was lower than

that in the non-addressing state because of the discharging of storage capacitor resulted in the decreasing of T4 gate voltage.

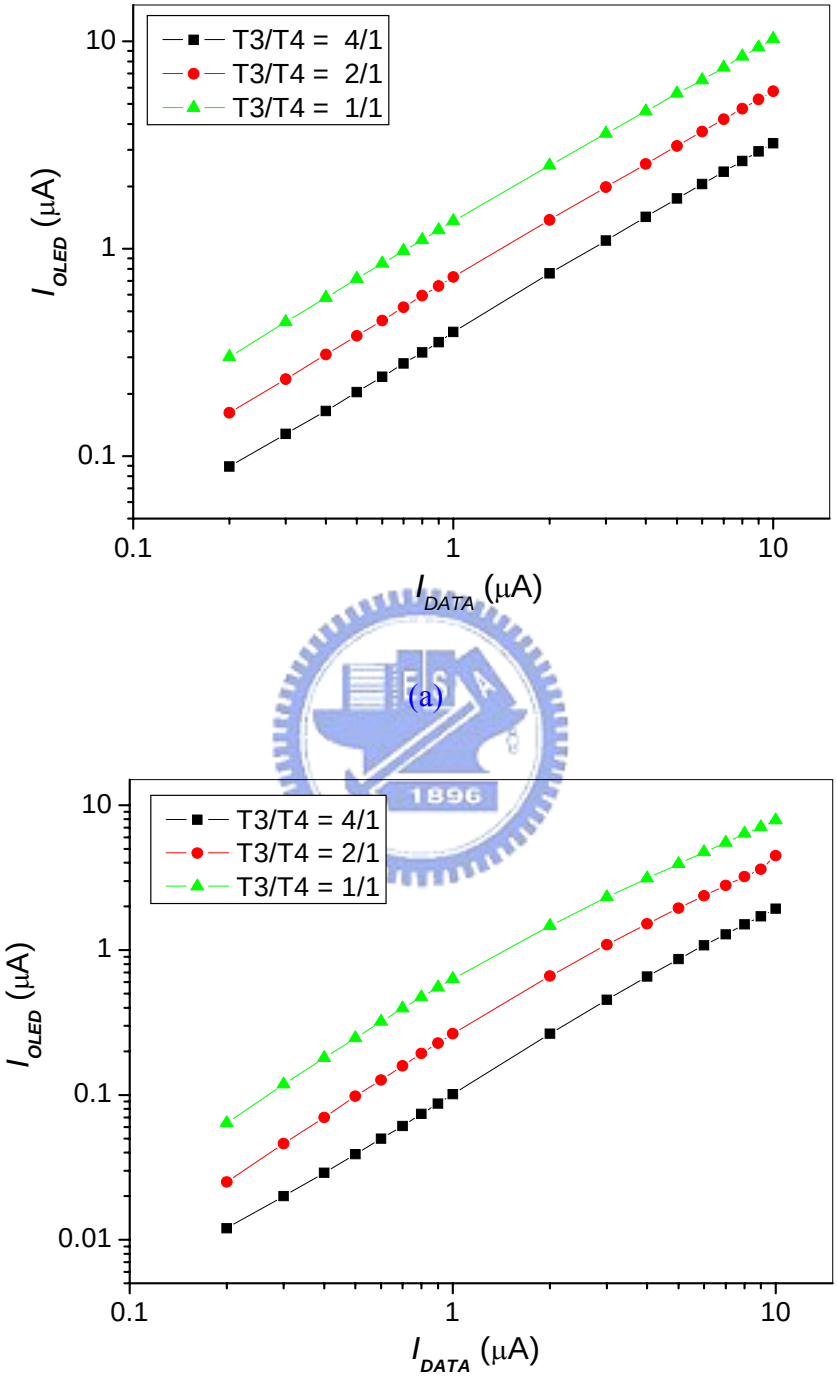


Fig. 5-6. The I_{OLED} as a function of I_{DATA} in the (a) addressing state and (b) non-addressing state at various T3/T4 = 4/1, 2/1 and 1/1 in a conventional

current-mirror pixel circuit shown in Fig. 2-1.

Table 5-4. The parameters of fabricated device for current-mirror pixel circuit.

Device parameter		
W[a]/L[b] (T_1)	(μm)	100/4
W/L (T_2)	(μm)	100/4
W/L (T_3)	(μm)	50/4~200/4
W/L (T_4)	(μm)	50/4
C_1	(pF)	2.5

[a] channel width of TFT

[b] channel length of TFT

According to Eq. 2-1 to 2-4 and Table 3-3, the comparison of the total programming time among current-driven, current-mirror and proposed pixel circuit was listed in the Table 5-5. Clearly, proposed pixel circuit could be effectively suppressed to 8.4 μs at luminance of 100 cd/m^2 XGA display while the conventional current-driven and current-mirror pixel circuits were 90 and 14.6 μs as scan pulse width was 21.7 μs at 60 Hz frame rate. On the other hand, at low gray level such as luminance of 20 cd/m^2, the total programming time of proposed pixel circuit was 16.4 μs which was shorter than the scan pulse width of 21.7 μs. Hence, the proposed pixel circuit had a capacity for shortening the programming time.

Table 5-5. Comparison of total programming time among current-driven, current-mirror and proposed pixel circuit at various luminance.

Luminance	Current-driven pixel		[1] Current-mirror pixel		[2] Proposed pixel	
20 cd/m^2	225	(μs)	22.0	(μs)	16.4	(μs)
100 cd/m^2	90	(μs)	14.6	(μs)	8.4	(μs)

[1] W_{T3}/W_{T4} = 4/1 (W: channel width of TFT)

[2] C_2/C_1 =1/4

To highlight the advantages of our proposed pixel circuit in comparison with both the conventional current-driven and current-mirror pixels, the OLED average current (I_{AVE}) as a function of data current in the proposed pixel circuit as well as the conventional current-driven and current-mirror pixel circuits was shown in Fig. 5-7. In a frame period (t_{ON} + t_{OFF}), the I_{AVG} of the current driven pixel circuit was almost equal to I_{DATA}, implying no current scaling function existed in the current driven pixel. As to the current mirror pixel, the circuit was able to scale down I_{DATA}, but the scale-down ratio was constant in the whole range of I_{DATA}. In addition, in order to achieve higher current scaling function, the TFT size should be larger but the aperture ratio would be reduced. In comparison, I_{AVE} of the proposed pixel circuit was achieved the widest range of driving current from 2 nA to 5 μA compared with current-driven pixel (0.2 to 10 μA) and current-mirror pixel (0.01 to 2 μA) in the range of I_{DATA} from 0.2 to 10 μA. Hence, at the same programming data current, the lowest gray levels would be displayed by the proposed circuit. In other words, the proposed circuit could be driven by a larger I_{DATA} to shorten the programming time.

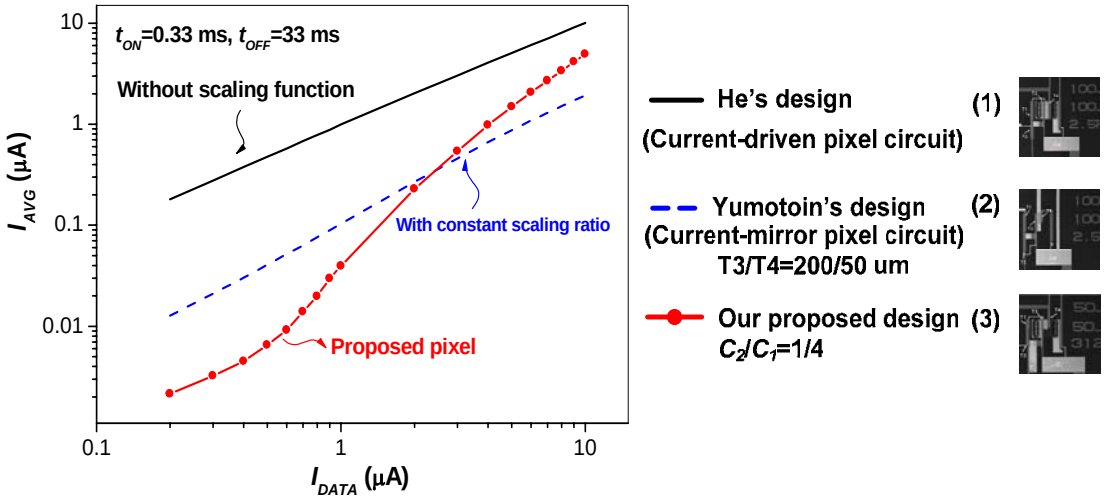


Fig. 5-7. Comparison of I_{AVG} as a function of I_{DATA} among conventional current-driven, current-mirror, and proposed pixels.

5.2 Reliability

The function of the current-driven AMOLED pixel circuit was to provide a constant current for the OLED regardless of threshold voltage (V_{TH}) and mobility (μ_{FE}) variation due to device aging or fabrication processes. To investigate the influence of V_{TH} and μ_{FE} variations, a bias-temperature-stress (BTS) experiment was performed for TFT device, current-driven and proposed pixel circuits to accelerate the aging process by using an Agilent 4156A with a probe station.

5.2.1 BTS for TFT Device

In the experiment, the channel width and length of TFT device were set to 50 and 4 μm while the gate and drain electrodes were supplied 30 V and 5 μA during the stress time. The threshold voltage deviation, ΔV_{TH}, was defined as follows:

$$\Delta V_{TH} = V_{TH\_AS} - V_{TH\_BS}, \quad (5\text{-}1)$$

where V_{TH_AS} and V_{TH_BS} denote the after and before stress of TFT threshold voltage. The ΔV_{TH} of TFT device was dependant on stress time as shown in Fig. 5-8. At 25 °C,

ΔV_{TH} varied from 0 to 1.9 V as the stress time increased from 0 to 20000 seconds as shown by the black line in Fig. 5-8. On the other hand, when the temperature was increased to 85 °C, the ΔV_{TH} enlarged from 0 to 13.4 V while stress time increased from 0 to 20000 seconds shown by the red line in Fig. 5-8. The substantial deviation was obtained because hot carrier was trapped at the interface of a-Si and the dielectric layer resulted in the increase of ΔV_{TH}.

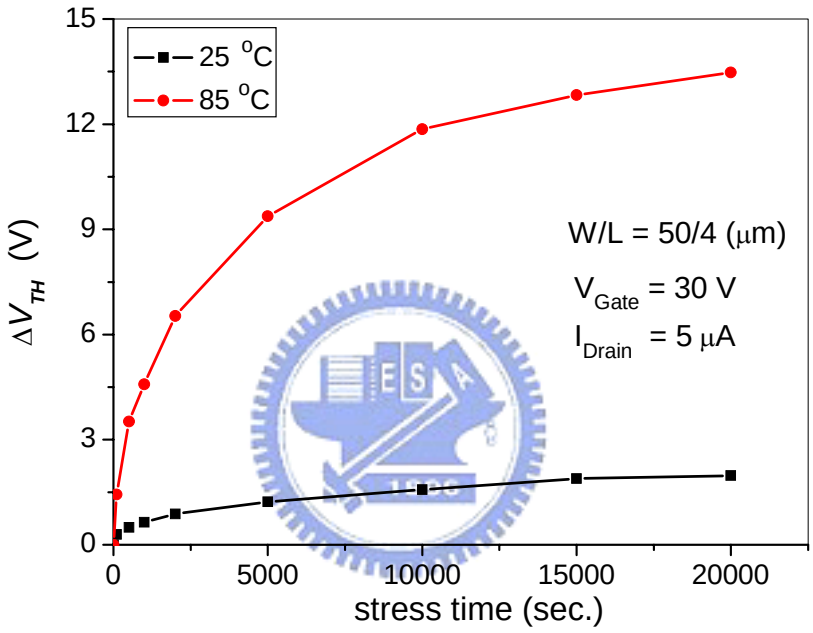


Fig. 5-8. The ΔV_{TH} as function of stress time at V_{Gate} = 30 V, I_{Drain} = 5 μA in the single TFT device which channel width (W) and length (L) are 50 and 4 μm, respectively.

5.2.2 BTS for Current Scaling Pixel Circuit

To research the influence of ΔV_{TH} of driving TFT (T3) on pixel circuit performance, a bias-temperature-stress (BTS) experiment was performed to accelerate the aging speed. Meanwhile, to avoid any OLED-related degradation issues, a diode-connected TFT was connected to source electrode of T3 instead of the OLED

device in the experiment. Based on the Fig. 5-8 results, in the condition of high temperature stress, the aging process was fast. Hence, the operation temperature was set to 85°C and V_{SCAN1} was kept on 30 V when an I_{OLED_ON} of 5 μA was applied. Moreover, the channel width and length of driving TFT and capacitance of C_1 were fixed on 50 μm, 4 μm and 2.5 pF, respectively. The variation of the I_{OLED_OFF} (ΔI_{OLED_OFF}) was defined as:

$$\Delta I_{OLED\_OFF} = \frac{I_{OLED\_OFF}(\Delta V_{TH}) - I_{OLED\_OFF}(\Delta V_{TH} = 0)}{I_{OLED\_OFF}(\Delta V_{TH} = 0)}. \quad (5\text{-}2)$$

The ΔI_{OLED_OFF} as a function of stress time was shown in Fig. 5-9. In the case of C_2/C_1 = 1/8, when stress time was lower than 1000 seconds, the amount of ΔV_{TH} was equal to 4.5 V. In this condition, the amount of ΔI_{OLED_OFF} was only 23 % and 6.7 % while the I_{OLED_ON} was 0.5 and 5 μA, respectively. Besides, the amount of ΔI_{OLED_OFF} was gradually increased with reducing I_{OLED_ON} due to the influence of charge injection of T2 on $V_{B\text{-}ON}$. Since a small $V_{B\text{-}ON}$ would result from a low I_{OLED_ON} at low gray scales, the charge carrier released from T2 could reduce the $V_{B\text{-}ON}$ when T2 was turn-off. In other words, a high I_{OLED_ON} could result in high $V_{B\text{-}ON}$ and consequently made $V_{B\text{-}ON}$ immune to the influence of charge injection. In the other hand, at C_2/C_1=1/4, the amount of ΔI_{OLED_OFF} was suppressed to 21 % and 3.8 % as the I_{OLED_ON} was 0.5 and 5 μA, respectively. Hence, the large storage capacitor had ability to eliminate the influence of T2 charge injection.

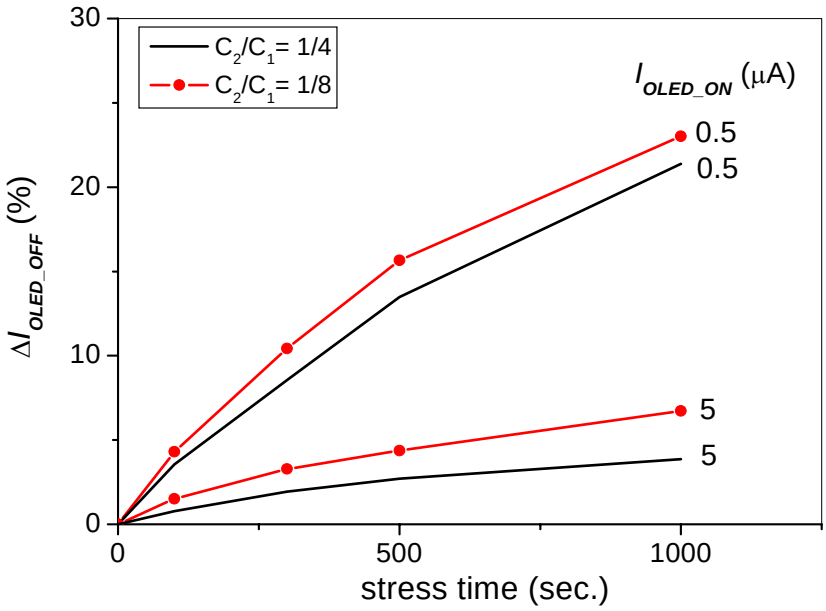


Fig. 5-9. Comparison of ΔI_{OLED_OFF} as function of stress time among C_2/C_1 = 1/8 and 1/4 at various I_{OLED_ON} current in the proposed pixel circuit shown in Fig.2-2.

Going a step further, the ΔI_{OLED_OFF} as a function of stress time was compared in the conventional current-driven and proposed pixel circuits shown in Fig. 5-10. In the stress time of 1000 seconds, the amount of ΔI_{OLED_OFF} in current-driven pixel circuit was 15 % and 3 % while the I_{DATA} was 0.5 and 5 μA, respectively. Although the ΔI_{OLED_OFF} of proposed pixel circuit was larger than that of current-driven pixel circuit at I_{DATA} of 0.5 μA, ΔI_{OLED_OFF} of proposed pixel circuit could be suppressed to 3.8 % at I_{DATA} of 5 μA. These results indicated that proposed pixel circuit was able to compensate for the TFT ΔV_{TH} variation to ensure a stable, constant output current level. This would achieve both a good control of the display gray levels and a uniform luminance distribution over the whole AM-OLEDs.

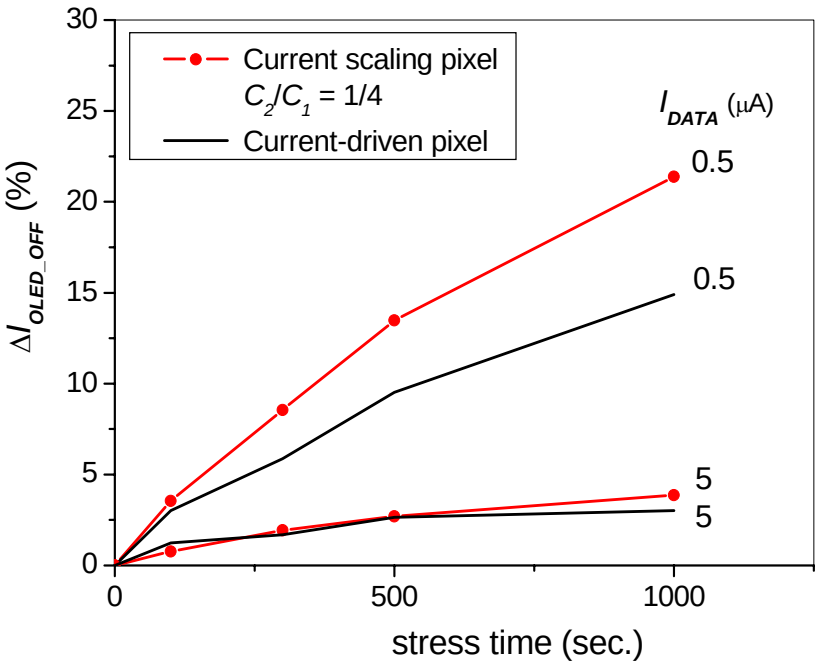


Fig. 5-10. Comparison of ΔI_{OLED_OFF} as a function of stress time among conventional current-driven pixel circuit shown in Fig. 1-3 and proposed pixel circuit shown in Fig. 2-2 at various I_{DATA} current.

5.3 Single Pixel AMOLED Device

Based on our analyses, the performances of proposed pixel circuit were more excellent than conventional current-driven and current-mirror pixel circuits. In this section, organic layers were deposited onto the panel to form the single pixel AMOLED device.

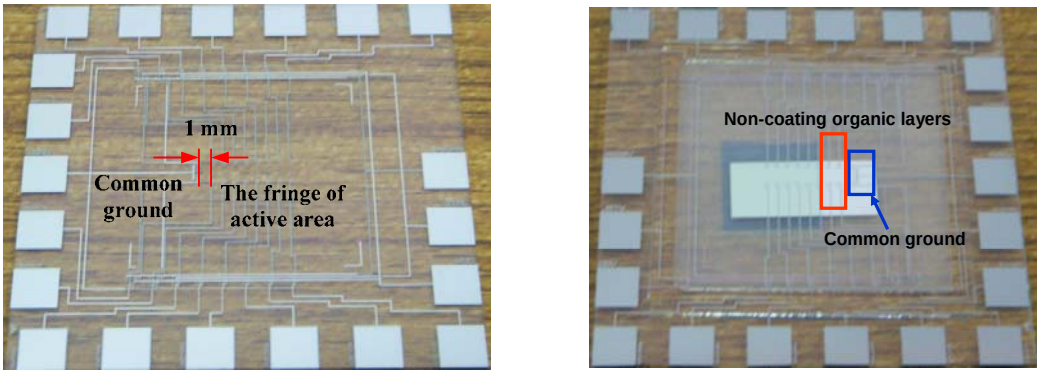
In the a:Si:H TFT panel, the different ratios of C_2/C_1 were designed in the individual pixel circuit to comparison the visual performance with each condition and the device parameters were shown in Table 5-6. Meanwhile, all of the individual signal lines including V_{SCAN1}, V_{SCAN2} and Vdd were connected to the relative pad to simplify the circuit. After fabrication of TFT components and relative signal pads, the

organic layers were deposited on the active area of the panel shown in Fig. 5-11. Due to the distance from the fringe of active area to common ground was only 1 mm, it was difficult to deposit the organic layers without covering the common ground. Hence, the active areas of current-mirror pixel circuit were not depositing organic layers to ensure the cathode of OLED device connected to the common ground. The parameters of organic layers were shown in Table 5-7. In the process of turning on AMOLED devices, the signals such as V_{SCAN1} and V_{SCAN2} were rectangular wave which pick-to-pick value were 0 to 30 V and 30 to 0 V at 60 Hz, respectively. As to I_{DATA} of ranging from 1 to 15 μA, *Vdd* of 30 V and ground were supplied to the relative signal pad. When the current was supplied to one of I_{DATA} pads, the one of AMOLED devices was lighted in normally operational condition. However, the adjacent active areas were also lighted as shown in Fig. 5-12.

Table 5-6. The parameters used in single pixel AMOLED device including current-driven, current-mirror and proposed pixel circuits.

		Device parameter
W[a]/L[b] (T_1)	(μm)	100/4
W/L (T_2)	(μm)	100/4
W/L (T_3)	(μm)	50/4~200/4
W/L (T_4)	(μm)	50/4
C_1	(pF)	1.5
C_2	(fF)	100~167
Active area	(mm^2)	0.16

[a] channel width of TFT
[b] channel length of TFT



(a) (b)

Fig. 5-11. (a) Before and (b) after depositing organic layers on the a:Si:H panel.

Table 5-7. The parameters of each organic layer were used for bottom-emission organic device.

Organic layer		
CuPc	(nm)	15
NPB	(nm)	60
Alq_3	(nm)	75
LiF	(nm)	0.5
Al	(nm)	150

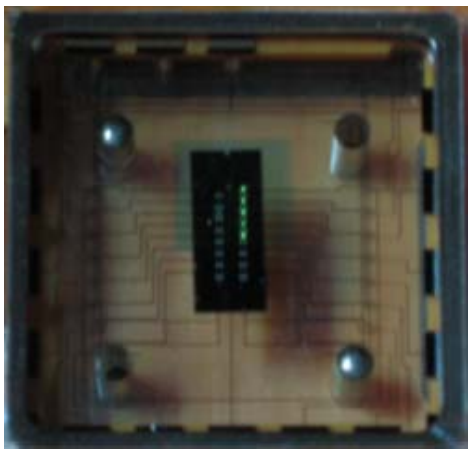


Fig. 5-12. Extraordinary lighting of active areas in the normally operational condition.

According to our investigation, there were two reasons resulted in the extraordinary lighting of AMOLED devices.

(1) The surrounded signal pad was connected to adjacent pad

In order to reduce the influence of static electricity in the fabricated process, the surrounded pad was connected to each other by a metallic line so as to remove the static electricity easily shown in Fig.5-13. However, after the fabrication of TFT components, the connected line between signal pad and metallic line was not cutting resulted in the surrounded signal pad was still connected to each other. Thus, the programming data current could pass through the other OLED device resulted in the extraordinary lighting of AMOLED devices.

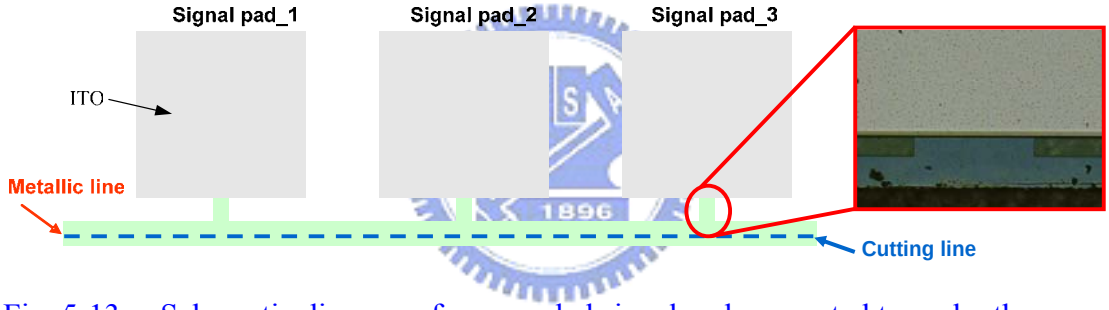


Fig. 5-13. Schematic diagram of surrounded signal pad connected to each other.

(2) The mistake of current-mirror pixel circuit design

In the current-mirror pixel circuit, organic layers were not deposited onto the active area because the distance from the fringe of active area to common ground was not long enough so that organic layers could be covered on the entire common ground resulted in the cathode of OLED devices and common ground was isolated by organic layers. Moreover, in ideal case, the cathode of OLED devices was connected to the drain electrode of driving TFT (T4); in practice, the cathode of OLED devices was connected to the common ground. However, V_{dd} pad in the all pixel circuits was directly connected to common ground by the V_{dd} signal line of current-mirror pixel

circuit resulted in the current in the non-addressing state passing through V_{dd} to common ground, not to OLED devices shown in Fig. 5-14. Hence, in the non-addressing state, single pixel AMOLED device could not be lighted.

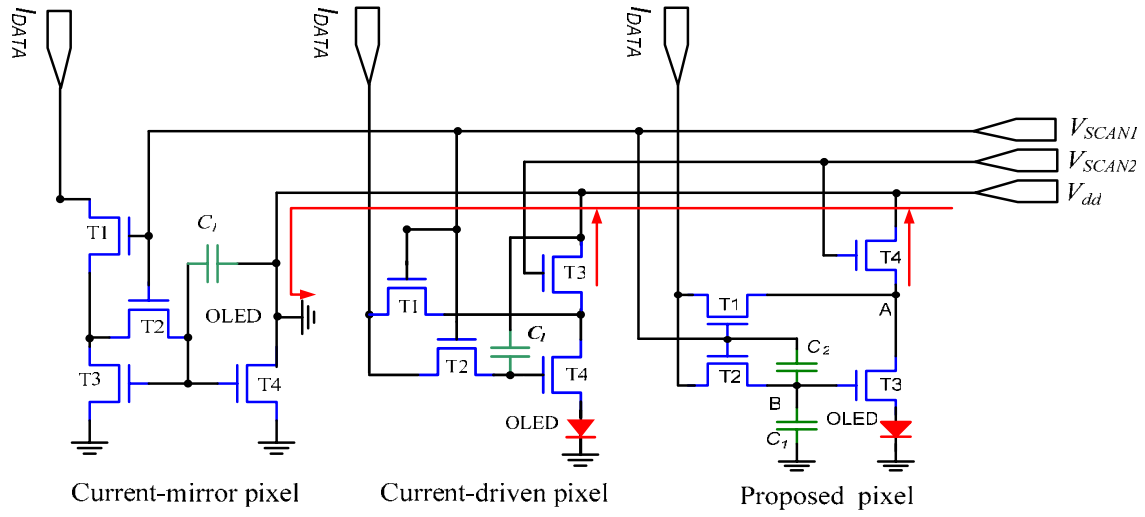


Fig. 5-14. Analysis of non-optimum pixel circuit in the single pixel AMOLED panel.

For the both reasons, the extraordinary lighting of single pixel AMOLED devices was obtained. Then, several methods were proposed to solve these problems in the following subsections.

5.3.1 Solution of Glass Cutting by Laser

The laser cutting technology can be used to cut the connected line between surrounded pad and metallic line accurately. Then, the input signal can only be transmitted to relative pixel circuit.

5.3.2 Solution of Short Circuit Problem

The bottom-emission structure of OLED device in the single pixel AMOLED device is adopted to simplify the OLED process. Hence, in order to implement current-mirror pixel circuit with bottom-emitting OLED device, the mask can be designed as shown in Fig. 5-15. In the current-mirror pixel circuit, the cathode line is

covered with metal layer so that the cathode line can be connected to the drain electrode of driving TFT rather than the common ground. Hence, this method can solve the short circuit problem.

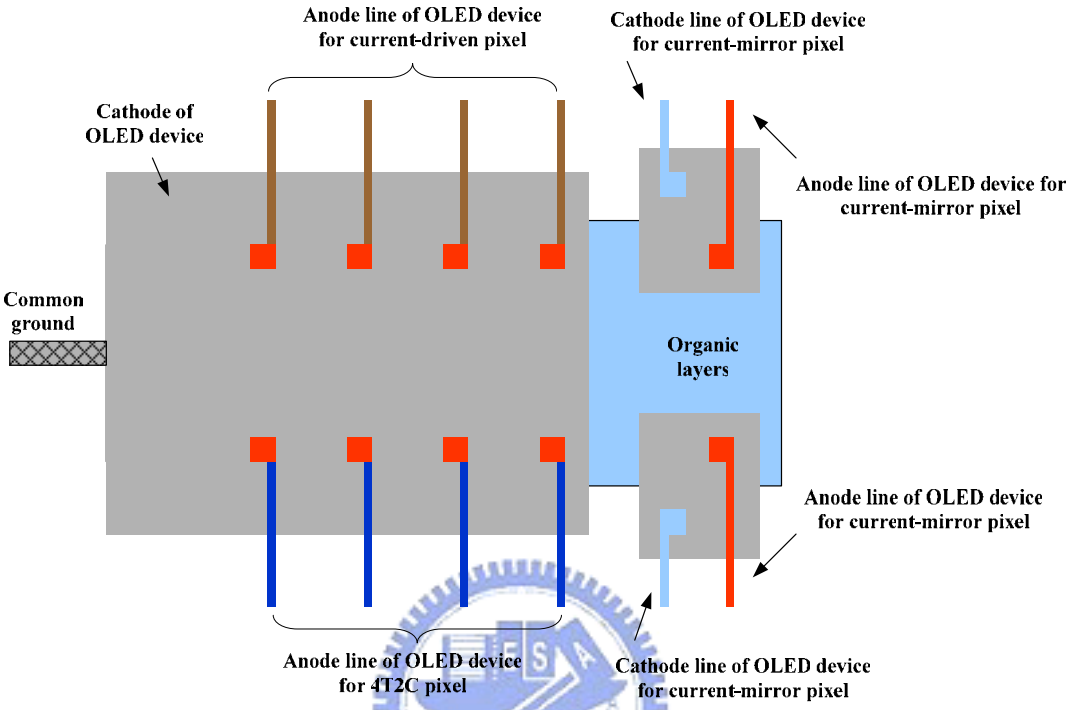


Fig. 5-15. The improved layout for single pixel AMOLED device.

5.4 Summary

By using standard fabrication process for a:Si:H TFT technologies, testing pixel circuit including current-driven, current-mirror and proposed pixel circuits are successfully fabricated and measured. In the analysis of measurement results, the programming time of proposed pixel circuit at luminance of 20 and 100 cd/m^2 can be suppressed to 8.4 and 16.4 μs, respectively while the scan pulse with is 21.7μs. In addition, at the ranging of data current from 0.2 to 10 μA, proposed pixel circuit can drive the widest OLED current range from 2 nA to 5 μA. By contrast, the current-driven and current-mirror can only drive OLED current range from 0.2 to 10 μA and 0.01 to 2 μA, respectively. On the other hand, the proposed pixel circuit also has the compensation function for the process- and aging-induced threshold voltage

variation so that the uniform images can be achieved. In the process of turning-on AMOLED devices, the extraordinary lighting of single pixel AMOLED devices is observed due to the glass cutting and current-mirror pixel circuit design, which also can be further improved by the proper fabrication.

Chapter 6

Conclusion and Future Direction

6.1 Conclusion

The OLED display technology has been a very active research area for its merits such as high brightness, high contrast ratio, light weight, thin structure, fast response time and low power consumption. Although several pixel circuit designs of AMOLED display were proposed for the applications in the electronic devices, the long programming time and low aperture ratio are critical issues. Therefore, an adaptive current scaling pixel circuit consists of cascaded storage capacitors was proposed to resolve the issues of programming time delay and low aperture ratio. The OLED driving current of proposed pixel circuit can be scaled down by the feed-through effect in the cascaded structure to achieve current scaling function, which can further reduce programming time. By tuning the ratio of the two cascaded capacitors, both adaptive current scaling ratio and the maximum range of OLED average driving current can be obtained without reducing aperture ratio. As a result, shorter programming time can be achieved while maintaining aperture ratio.

By software simulation, the device model was established to characterize the features of the pixel circuit. Initially, in the proposed circuit, the addressing state programming current of a factor of 10 larger than OLED current in non-addressing state was achieved. Furthermore, the current scaling ratio was adaptive to the input data current so that both large current scaling ratio at low gray levels to shorten programming time and low current scaling ratio at high gray levels to reduce power consumption could be obtained.

In the experiments, proposed pixel circuit was fabricated based on conventional

standard process for a:Si:H TFT technology. In the part of electrical characteristics, the programming time of proposed pixel circuit at luminance of 20 and 100 cd/m^2 could be suppressed to 16.4 and 8.4 μs, respectively. In contrast to the conventional current-driven and the current-mirror pixel circuits, proposed pixel circuit could drive the widest OLED average current range from 2 nA to 5 μA at the ranging of programming current from 0.2 to 10 μA. On the other hand, in the reliability, the bias temperature stress experiment was performed to accelerate the TFT device aging. The results showed that with the threshold voltage variation of TFT ranging from 0 to 4.5 V, the OLED current variation was only 3.8 and 21 % while the programming data current was 5 and 0.5 μA, respectively. The reason caused the OLED current variation up to 21 % was the influence of charge injection on switching TFT. The charge injection could be effectively eliminated by enlarging the ratio of cascade storage capacitors. Therefore, the proposed pixel circuit was capability of compensating the threshold voltage variation of driving TFT to ensure a stable, constant output current level so as to achieve both a good control of the display gray levels and a uniform luminance distribution over the whole AM-OLEDs. Although the visual performance of single pixel AMOLED devices was extraordinary results, the fabrication problems and layout design could be resolved by the proper fabrications. Hence, the combination of the outstanding current scaling and compensation functions stands for a dual applicability in the electronic displays and micro-electronic. Such an adaptive current scaling design transcends over the conventional concept and extends its feasibility to another applied technology.

6.2 Future Direction

The core in the future direction is the integrated case. The simulation will proceed to 50*50 AMOLED display with adaptive current scaling pixel circuit based on a:Si:H TFT technology. The field-programmable gate arrays (FPGA) demo board

is utilized to supply the digital signals for the programming and controlling signals shown in Fig. 6-1. Here, the operational amplifier circuitry is necessary to amplify the voltage to appropriate level to turn on the switching TFT and drive the constant current source. By integrating driving circuitry system and TFT panel, the adaptive current scaling pixel circuit of AMOLED display will be developed in the future.

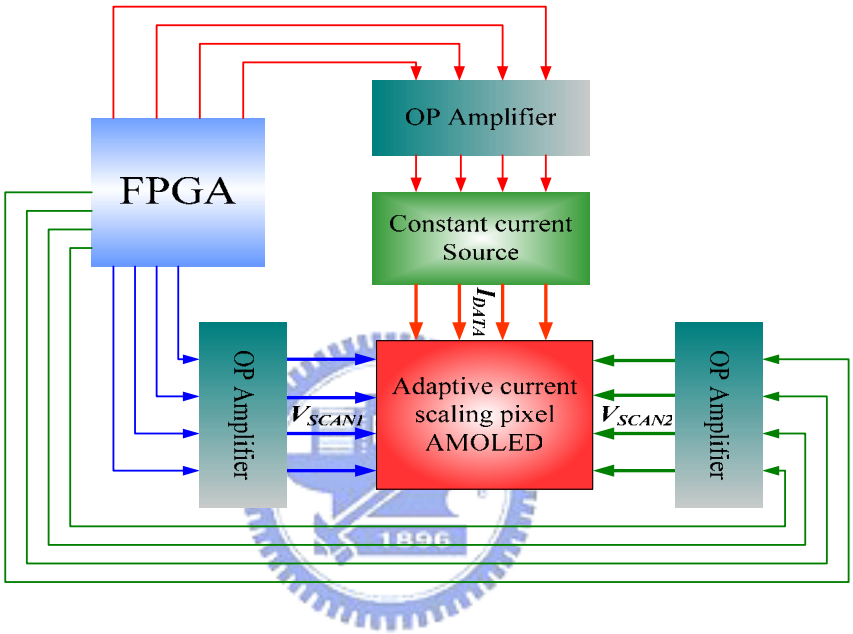


Fig. 6-1. The schematic diagram of driving circuitry system for adaptive current scaling pixel AMOLED display.

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