Small-Subthreshold-Swing and Low-Voltage Flexible Organic Thin-Film Transistors Which Use HfLaO as the Gate Dielectric

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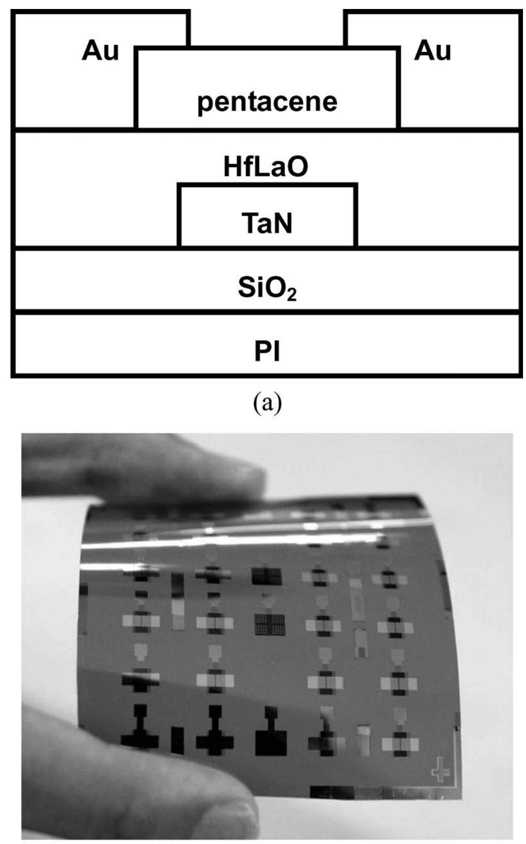
***Abstract*—Pentacene organic thin-film transistors (OTFTs) with a high-κ HfLaO dielectric were integrated onto flexible polyimide substrates. The pentacene OTFTs exhibited good performance, such as a low subthreshold swing of 0.13 V/decade and a threshold voltage of -1.25 V. The field-effect mobility was 0.13 $cm^2/V \cdot s$ at an operating voltage as low as only 2.5 V. These characteristics are attractive for high-switching-speed and low-power applications.**

***Index Terms*—Flexible, HfLaO, high-κ, organic thin-film transistors (OTFTs), pentacene.**

I. Introduction

PENTACENE-BASED organic thin-film transistors (OTFTs) have been intensely investigated due to their low cost and lightweight for potential use in applications such as flexible displays and low-cost flexible integrated circuits (ICs) [1]–[3]. The low thermal budget and rapid processing have strong merits of energy savings and environment friendliness, which are in sharp contrast to the extended 600-°C annealing times in conventional solid-phase-crystallized (SPC) poly-Si TFTs. Although low-thermal-budget poly-Si TFTs can also be formed on plastic substrate using excimer laser annealing [4], the uniformity is a concern. Alternatively, poly-Si TFTs [5] or even single-crystal submicrometer MOSFETs [6] can be realized on plastic substrate by fabrication first, separation next and transfer, but these methods still require high thermal budget for device fabrication. However, conventional OTFTs require a high operating voltage and show a poor subthreshold swing (SS), which detracts from their suitability in IC operations [7], [8]. To address these issues, high-κ gate dielectrics have been applied in OTFTs for low-voltage operation [1], [3], [9]–[13]. We have previously reported pentacene OTFTs on SiO_2/Si substrates using high-κ HfLaO as the gate dielectric [13]. Although the performance is comparable with that of SPC poly-Si TFTs, the process temperature of 350 °C is still not suitable for flexible electronics. In this letter, we further decrease the process temperature to 200 °C and demonstrate HfLaO/pentacene OTFTs, fabricated on low-cost flexible polyimide (PI) (Kapton HPP-ST, Dupont) substrates. These substrates are much more economical than other PI (Kapton E-type, Dupont) substrates [1], [9] and those which use polyethylene naphthalate (Teonex Q65 PEN, Dupont) [2]. Our HfLaO/pentacene OTFTs showed a low SS of only 0.13 V/decade, a high gate capacitance density of 450 nF/cm^2,



(a)

(b)

Fig. 1. Schematic diagram (a) and image (b) of the high-κ flexible HfLaO/pentacene OTFTs.

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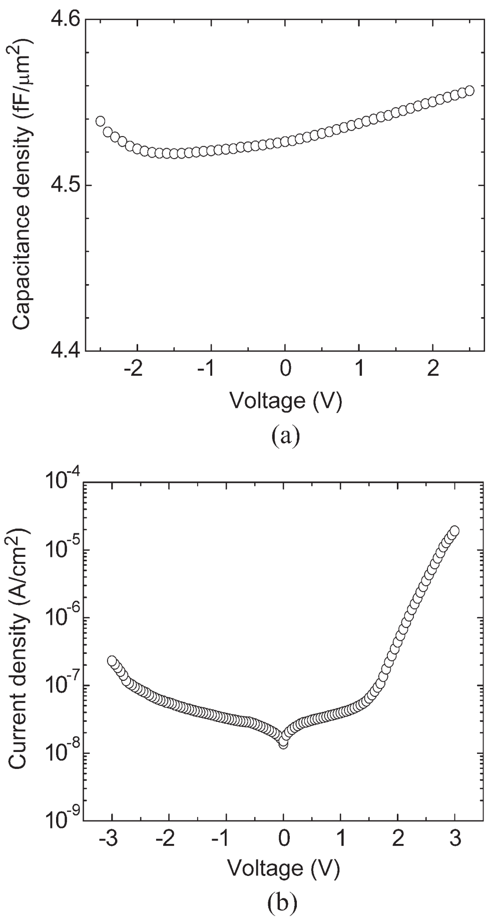

Fig. 2. (a) C–V and (b) J–V characteristics of Au/HfLaO/TaN capacitors.

a low threshold voltage (V_T) of -1.25 V, a good mobility $(\mu_{\rm FE})$ of 0.13 $\text{cm}^2/\text{V}\cdot\text{s}$, and an ON–OFF-state drive current ratio $(I_{\rm on}/I_{\rm off})$ of 1.2×10^4. This superior performance permits the devices to be operated at 2.5 V, which could be useful in flexible electronics.

II. Experimental Details

All the devices were fabricated on 125-μm-thick PI substrates (Kapton HPP-ST, Dupont). Prior to the device fabrication process, the PI substrates were annealed in vacuum at 200 °C [2]. A 100-nm SiO_2 thin film was deposited on the PI substrate [3]. Then, a 50-nm TaN gate electrode was deposited by reactive sputtering through a shadow mask. The surface of the TaN gate was treated in a NH_3 plasma to reduce the gate leakage current [14], [15]. A 30-nm-thick HfLaO gate dielectric was then deposited. A 200-°C 30-min furnace O_2 treatment was then used to improve the gate oxide quality. Next, the pentacene active layer (Aldrich Chemical Company), 70 nm in thickness, was deposited through the shadow mask under vacuum and 70 °C. Finally, 50 nm of Au was deposited for the source/drain electrodes. The channel width and channel length were 2000 and 100 μm, respectively. Metal–insulator–metal Au/HfLaO/TaN capacitors, 200×200 μm^2 in size, were also fabricated to analyze the leakage current and the dielectric properties.

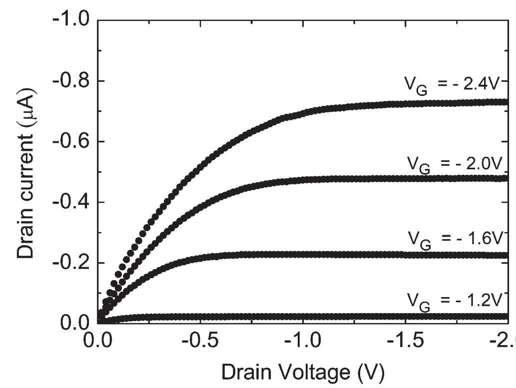

Fig. 3. I_D–V_D curve for a HfLaO gate dielectric OTFT.

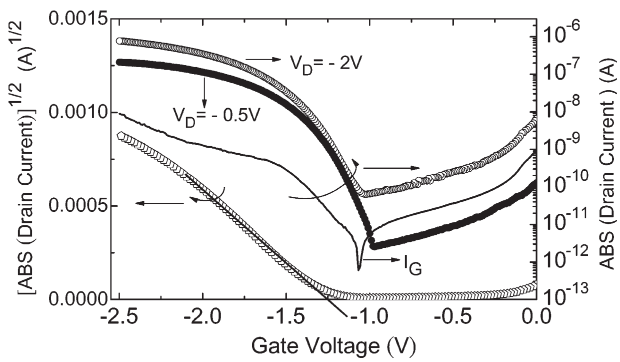

Fig. 4. I_D–V_G and $-I_D^{1/2}V_G$ of a HfLaO gate dielectric OTFT.

III. Results and Discussion

We show a schematic diagram and an image of the OTFTs in Fig. 1(a) and (b), respectively. The C–V and J–V characteristics of the Au/HfLaO/TaN capacitors are shown in Fig. 2(a) and (b), respectively. A low leakage current of 3.5×10^{-6} A/cm^2 at 2.5 V was measured, along with a capacitance density of 450 nF/cm^2. This density yields an equivalent oxide thickness (EOT) of 7.7 nm and a high-κ value of 15.3.

The output characteristics $(I_D$–$V_D)$ of a high-κ HfLaO OTFT are shown in Fig. 3. Good drain saturation behaviors were observed and suggest possible operation at 2.5 V. Fig. 4 shows the I_D–V_G characteristics of a representative OTFT, and $\mu_{\rm FE}$ and V_T were determined from the $-I_D^{1/2}$ versus V_G plot. The resulting values are -1.25 V for V_T, 0.13 cm^2/Vs for $\mu_{\rm FE}$, and an SS of 0.13 V/decade. The $I_{\rm on}/I_{\rm off}$ ratio was 1.2×10^4. The SS of our device is better than the values observed for other flexible pentacene OTFTs [1]–[3], [9], [10], arising from the high gate capacitance density and small EOT [13]. The relatively smaller mobility and $I_{\rm on}/I_{\rm off}$ were due to both lower operation voltage and poor surface roughness. An rms surface roughness of 4.3 nm was measured by atomic force microscopy on HfLaO and worse than the 2.0-nm value of BZN [3], which originates from the poor 9.0-nm roughness of very low cost PI substrate (Kapton HPP-ST, Dupont).

In Table I, we summarize some important device parameters, including other data of low-voltage flexible pentacene OTFTs using $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN), polyvinylphenol, Ta_2O_5, $TiSiO_2$, and Mn-doped $Ba_{0.6}Sr_{0.4}TiO_3$ (Mn-doped BST) as

TABLE I
COMPARISON OF LOW-VOLTAGE OTFTS WITH VARIOUS GATE DIELECTRICS

OTFTs with various gate dielectrics	HfLaO [This work]	BZN [1]	PVP [2]	Ta_2O_5 [3]	Mn-doped BST [9]	$TiSiO_2$ [10]	π-σ-PA1 /AlOx [11]	OPDA/ AlO_x [12]	HfLaO [13]
substrate	PI Kapton HPP-ST	PI Kapton E-type	PEN	PEN	PI Kapton E-type	PEN	Si	glass	SiO_2/Si
Dielectric thickness (nm)	30	200	50	150	200	136.4	-	-	20
Operating voltage (V)	2.5	2	8	12	10	5	3	2	2
C_i (nF/cm^2)	450	221	63.7	141.6	110	142.1	760	600~800	950
V_T (V)	-1.25	0.1	-	0.8	-1	-0.88	-1.3	0.35	-1.3
μ_{FE} (cm^2/Vs)	0.13	0.5	0.1	0.25	0.32	0.67	0.18	0.04	0.71
SS (V/decade)	0.13	0.3	0.6	-	-	0.315	0.085	0.11	0.078
$\mu_{FE}C_i$ (nF/cm^2)	58.5	110.5	6.37	35.4	35.2	95.21	136.8	24~32	674.5
I_{on}/I_{off}	1.2×10^4	3.5×10^5	1×10^4	-	$<1\times10^3$	1×10^4	1×10^5	1×10^4	1×10^5

gate dielectrics, and fabricated on high-quality PI (Kapton E-type) and PEN substrates [1]–[3], [9], [10]. The low-voltage OTFTs using (2-anthryl)undecoxycarbonyldecylphosphonic acid (π-σ-PA1)/AlO_x, octadecylphosphonic acid (OPDA)/ AlO_x, and HfLaO as gate dielectrics, fabricated on Si, glass, and SiO_2/Si substrate, are also listed in Table I for comparison [9]–[13]. The value of the $\mu_{\rm FE}C_i$ term is directly proportional to I_D $(W/2L_G \times \mu_{\rm FE}C_i(V_G - V_T)^2)$, normalized to the channel length L_G, channel width W, and overdrive voltage of $V_G - V_T$. The performance of our HfLaO OTFTs is comparable with that of other low-voltage flexible pentacene OTFTs for low-power applications, but with the additional merit of a good SS and the use of economical PI substrates.

IV. CONCLUSION

A high-κ HfLaO dielectric was successfully integrated into pentacene OTFTs fabricated on low-cost flexible substrates. The HfLaO/pentacene OTFTs showed a low SS, a small V_T, a large $\mu_{\rm FE}C_i$, and a low operating voltage.

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