Characteristics of Gate-All-Around Twin Poly-Si Nanowire Thin-Film Transistors

Jeng-Tzong Sheu, Po-Chun Huang, Tzu-Shiun Sheu, Chen-Chia Chen, and Lu-An Chen

***Abstract*—We have investigated the characteristics of gate-all-around (GAA) twin polycrystalline-silicon nanowire (NW) thin-film transistors (TFTs). The NW channel and surrounding gate imparted the GAA twin NW TFT with superior channel controllability. Moreover, the combination of the high surface-to-volume ratio of the NW and the split channel structure led to highly efficient NH_3 plasma treatment, which reduced the effective grain-boundary trap-state density. The GAA twin NW TFT exhibited greatly improved electrical performance, including a lower threshold voltage, a steeper subthreshold swing (114 mV/dec), a higher on/off current ratio ($>10^8$), and a virtual absence of drain-induced barrier lowering (13 mV/V).**

***Index Terms*—Gate-all-around (GAA), nanowire (NW), plasma treatment, short-channel effects (SCEs), thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) are attracting much attention for their use in active-matrix liquid crystal displays [1]. Increasing the performance of poly-Si TFTs has become one of the key challenges for system-on-chip applications. Unfortunately, traditional poly-Si TFTs suffer from serious short-channel effects (SCEs) when the device feature size is scaled down, due to the field-emission leakage current near the high-electric-field drain side and grain-boundary trap states in the channel [2]–[4]. Many crystallization techniques, including excimer-laser annealing (ELA), [5], [6] metal-induced lateral crystallization (MILC), [7], [8], and solid-phase crystallization (SPC) [9], have been used to improve the quality of poly-Si films, reduce the leakage current, enhance the carrier mobility, and suppress SCEs. Although ELA and MILC both result in poly-Si films exhibiting larger grain size, they add complexity to the fabrication process. Poly-Si films formed through SPC exhibit poorer performance because of the presence of a large number of randomly oriented grain boundaries [10]. A multiple-gated device has been proposed to enhance the gate controllability over the channel and thereby improve the device performance [6], [9], [11]. Although the gate-all-around (GAA) structure provides superior channel controllability, however, performance of the poly-Si TFT with the GAA structure still suffers from intrinsic defects in the poly-Si channel. In this letter, the performance of the GAA TFT was further improved by employing NH_3 plasma treatment for the reduction of trap-state density. Only few research works discussed these considerations [6], [12], [13]. Furthermore, the spacer patterning technique was adopted for linewidth uniformity and controllability without using expensive advance lithographic tools [7], [9].

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II. Device Fabrication

The 3-μm-long twin poly-Si nanowire (NW) was fabricated using the spacer patterning technique [14]. Wafers (p-type, ca. $10^{15}/\text{cm}^3$) were subjected to thermal oxidation to form a 400-nm SiO_2 that served as the starting substrate. A 50-nm-thick undoped amorphous-Si (α-Si) layer was deposited at 550 °C using low-pressure chemical vapor deposition (LPCVD). SPC was performed at 600 °C for 24 h in a nitrogen ambient to turn the α-Si into a polycrystalline-silicon structure. Next, a 100-nm-thick tetraethylorthosilicate (TEOS) oxide was deposited through LPCVD to serve as the dummy oxide layer. After patterning the dummy oxide layer using optical lithography, a 100-nm SiN_x film was deposited; subsequent reactive ion etching (RIE) formed the sidewall spacers that served as a hard mask in the following poly-Si etching process. By controlling the RIE conditions and the thickness of the SiN_x film, the feature size of the SiN_x units could be scaled down to the nanoscale without using any advanced photolithography techniques. Next, the TEOS dummy block was stripped off, and then, anisotropic RIE of poly-Si layer led to the formation of the twin poly-Si NW in which the wire width was predefined by the size of the SiN_x features. The poly-Si NW was then released from the thermal oxide through wet etching in 1 : 100 diluted HF solution by removing 70–80 nm of thermal SiO_2, followed by sequential conformal deposition of 20-nm TEOS and 200-nm *in situ* N^+ polysilicon using LPCVD. The channel was surrounded by TEOS and N^+ polysilicon. After transferring the 2-μm poly gate, self-aligned phosphorous ion implantation was performed at a dose of 5×10^{15} cm^{-2}, and then, the samples were activated through thermal annealing at 600 °C for 12 h. A 300-nm-thick TEOS layer was deposited as the passivation layer using LPCVD. Finally, the contact hole was defined, and Al metallization was performed. All devices were sintered at 400 °C in a nitrogen ambient for 30 min. To study the impact of grain-boundary defects, the samples were subjected to NH_3

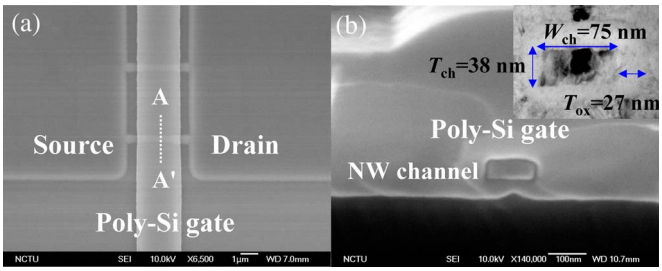

Fig. 1. (a) Top-view SEM photograph of the GAA twin poly-Si NW TFT. (b) SEM image of the cross-sectional view of the poly-Si NW which is surrounded by poly-Si gate electrode along the AA′ shown in (a). The inset of (b) shows a TEM photograph of the suspended NW ($W_{\rm ch} = 75$ nm and $T_{\rm ch} = 38$ nm) channel surrounded by 27-nm-thick TEOS and poly-Si gate.

TABLE I
DEVICE KEY PARAMETERS OF GAA TWIN POLY-SI NW TFTS WITH $W_{\rm eff}/L = 0.452\ \mu{\rm m}/2\ \mu{\rm m}$ AND PLANAR TFTS WITH $W/L = 0.5\ \mu{\rm m}/2\ \mu{\rm m}$. ALL PARAMETERS WERE EXTRACTED AT $V_{\rm ds} = 0.5$ V, EXCEPT FOR THE ON/OFF CURRENT RATIO, WHICH WAS EXTRACTED AT $V_{\rm ds} = 3.0$ V

Structure (W_{eff}/L)	V_{th} (V)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)
GAA (0.452 μm/2 μm, NH_3 1h)	-0.38 ± 0.177	1.2×10^8	114	13
GAA (0.452 μm/2 μm, NH_3 30 min)	0.73 ± 0.317	2.9×10^7	125	14
GAA (0.452 μm/2 μm, as fabricated)	2.2 ± 0.361	2.5×10^6	466	24
Planar (0.5 μm/2 μm, NH_3 1h)	0.9	2.1×10^7	402	15
Planar (0.5 μm/2 μm, as fabricated)	1.12	3.3×10^6	611	96

plasma treatment in a parallel-plate plasma reactor at a power density of 0.7 W/cm^2 at 300 °C for either 30 min or 1 h.

III. RESULTS AND DISCUSION

Fig. 1(a) shows a top-view scanning electron microscopy (SEM) image of the proposed GAA twin poly-Si NW TFT. Fig. 1(b) shows a cross-sectional SEM image viewed along the AA′ direction in Fig. 1(a). The poly-Si NW channel was surrounded by the N^+ poly-Si gate. The inset of Fig. 1(b) shows a transmission electron microscopy (TEM) image of the NW channel possessing the GAA structure. The proposed devices have a nominal channel length (L) of 2 μm, a channel width $(W_{\rm ch})$ of 75 nm, and an effective channel width $(W_{\rm eff})$ of 452 nm $[4 \times (W_{\rm ch} + T_{\rm ch})]$. Because the aspect ratio $(T_{\rm ch}/W_{\rm ch} = 0.5)$ is higher than that of a conventional planar TFT $(T_{\rm ch}/W_{\rm ch} \ll 0.1)$, we expected to observe improved device characteristics as a result of corner effects [15]. The additional electric field at the bottom corners and bottom of the channel in the GAA TFT enhances the performance so that the device exhibits a faster turn-on speed, a lower threshold voltage, and a smaller leakage current. Table I presents the key device parameters measured in GAA poly-Si NW TFTs and conventional planar gate poly-Si TFTs. GAA poly-Si NW TFTs exhibit a better device performance over conventional planar

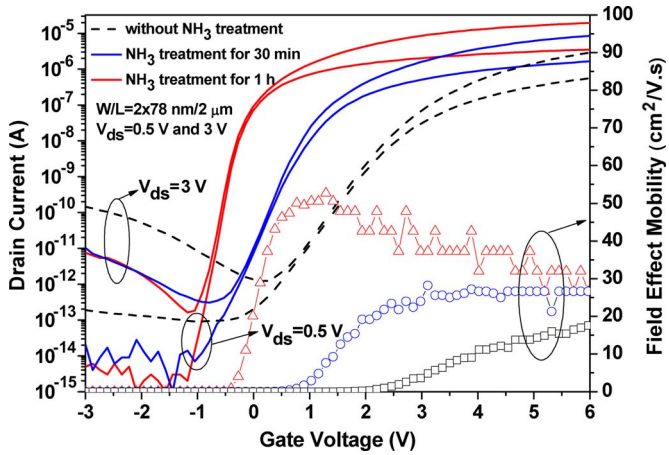

Fig. 2. Comparison of $I_{\rm ds}$–$V_{\rm gs}$ transfer characteristics and field-effect mobility of GAA twin poly-Si NW TFTs $(W/L = 75\ {\rm nm}/2\ \mu{\rm m} \times 2)$ after passivation with NH_3 plasma treatment for different periods.

poly-Si TFTs. In addition, after NH_3 plasma treatment, the variations of the threshold voltage were minimized. Fig. 2 shows the normalized transfer characteristics of a typical GAA twin poly-Si NW TFT before and after NH_3 plasma treatment at values of $V_{\rm ds}$ of 0.5 and 3 V. The threshold voltage $(V_{\rm th})$ is defined as the gate voltage required to achieve a normalized drain current of $I_d = (W_{\rm eff}/L) \times 10^{-8}$ A at a value of $V_{\rm ds}$ of 0.5 V. The subthreshold swing and field-effect mobility were extracted at a value of $V_{\rm ds}$ of 0.5 V, whereas the on/off current ratio $(I_{\rm on}/I_{\rm off})$ was extracted when $V_{\rm ds}$ was 3 V, where $I_{\rm off}$ is the minimum OFF-state current and $I_{\rm on}$ is the maximum ON-state current. Drain-induced barrier lowering (DIBL) is defined as $\Delta V_{\rm gs}/\Delta V_{\rm ds}$, where I_d is 10^{-10} A.

DIBL was well controlled to values less than 24 mV/V, and it is improved further to 13 mV when the devices were subjected to NH_3 plasma treatment for 1 h. SCEs were suppressed due to the channel being tightly controlled by the surrounding gate and because the grain-boundary-defect density was reduced after NH_3 plasma treatment [13]. Additionally, NH_3 plasma treatment reduced the leakage current significantly and provided the GAA twin poly-Si NW TFTs with a higher on-current. As a result, the GAA twin poly-Si NW TFTs exhibited a higher on/off current ratio $(>10^8)$ than that of the untreated samples $(>10^6)$. Similarly, the threshold voltage and subthreshold swing (−0.38 V and 114 mV/dec, respectively) were superior to those (2.2 V and 466 mV/dec) of the untreated device. Moreover, the maximum field-effect mobility of the GAA twin poly-Si NW TFTs increased dramatically from 23.4 to 52.7 cm^2/V · s. No channel doping process during self-aligned N^+ S/D implantation resulted in negative value of the threshold voltage. This problem can be solved by employing metal or metal silicide gates that have an appropriate work function [16].

To verify the reduction of grain-boundary defects in the GAA twin poly-Si NW TFTs after NH_3 plasma treatment, we extracted the effective trap-state density (N_t) from the slope of the plot of $\ln(I_d/V_{\rm gs})$ versus $(1/V_g)$ [3]. The GAA twin poly-Si NW TFTs had been subjected to 1 h of NH_3 plasma treatment, revealing a reduction in the effective trap-state density $(N_t =$ ca. $4.4 \times 10^{11})$ relative to that of the untreated GAA twin

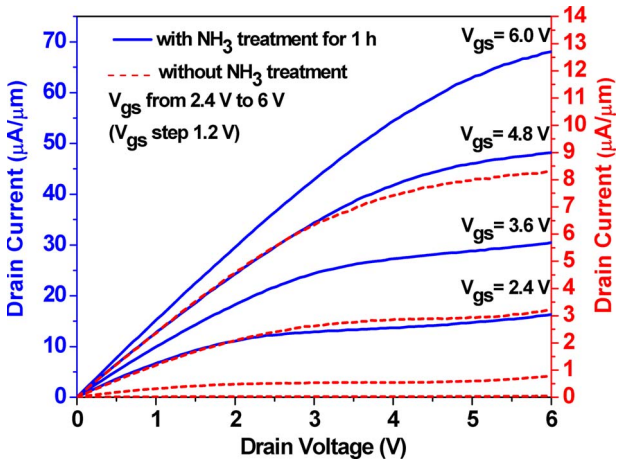

Fig. 3. Output $I_{\rm ds}$–$V_{\rm ds}$ characteristics of a GAA twin poly-Si NW TFT subjected to NH_3 plasma treatment for 1 h. Kink effect is suppressed by both GAA structure and NH_3 plasma treatment.

poly-Si NW TFTs ($N_t =$ ca. 3.15×10^{12}). We suspect that radicals diffused mainly through the gate oxide passivated the trap states in the channel during the NH_3 plasma treatment process, and hence, the grain-boundary barrier potentials were further reduced [17]. Moreover, the high surface-to-volume ratio of the NWs and the split channel structure led to the higher efficiency of NH_3-plasma-treated devices relative to that of conventional TFT devices (as shown in Table I for devices that had been subjected to 1-h plasma treatment).

Fig. 3 shows output characteristics typical for a GAA twin poly-Si NW TFT after NH_3 plasma treatment for 1 h. The drain saturation current was 12.2 μA/μm at values of $V_{\rm ds}$ and $V_{\rm gs}$ of 2.4 V (0.024 μA/μm for a device without plasma treatment). We suspect that performance characteristics could be improved further by optimizing the contact resistance through plug implantation or by using a metal silicide as source/drain regions. In the absence of a lightly doped drain, our proposed device structure features a steeper subthreshold slope, a greater on/off current ratio, and suppression of SCEs. As more and more functions are integrated on a flat-panel system, SCEs will make the power consumption problem for TFT applications like driving circuits in the active-matrix liquid crystal display more challenging. The proposed device exhibiting a low turn-on voltage, a very low leakage current, and a high switching speed is highly promising for future applications.

IV. Conclusion

In summary, we have characterized high-performance GAA twin poly-Si NW TFTs subjected to NH^3 plasma treatment for 1 h. The combination of the excellent gate controllability of the GAA structure and the NH_3 plasma treatment process resulted in TFTs that were immune to both grain-boundary effects and SCEs. GAA twin poly-Si NW TFTs subjected to NH_3 plasma treatment for 1 h exhibit a low threshold voltage ($V_{\rm th} = -0.38$ V), a small subthreshold swing (114 mV/dec), a high on/off current ratio ($>10^8$), and a virtual absence of DIBL. From the point of view of device integration, the wet etching process is the only process added in the fabrication of GAA NW poly-Si TFTs. We suspect that our proposed GAA twin poly-Si NW TFTs will be suitable for applications in low-voltage (< 3.5 V) circuit operations, high-performance driver circuits, and switching devices.

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