國　立　交　通　大　學

電子工程學系　電子研究所

博 士 論 文

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摘　要

本論文針對完全空乏型之單晶矽/二氧化矽金氧半場效電晶體建立了臨界電壓、汲極電流之解析模型。此外，並對於結合大傾角佈植（*Halo or Pocket Implantation*）製程之短通道完全空乏型單晶矽/二氧化矽金氧半場效電晶體，依序建立其電位分佈、臨界電壓以及次臨界電流之解析模式。另外，本文亦推導一適用於高頻積體電路之金氧半場效電晶體小信號模型及一正確的參數萃取方法。在二維數值分析以及相關實驗之測試下，所提出的解析模式之有效性已經成功地被驗證。

第一章包含有關於我們研究動機的概括論述及介紹本論文的組織架構。在第二章中，我們利用三區域格林函數解法（*Three–Zone Green's Function Solution Method*）於二維帕松方程式（*Poisson's Equation*），且根據適當的邊界條件選取合適的格林函數，精確地解出位於前/後閘二氧化矽以及單晶矽內的二維電位分佈。我們藉由在前閘二氧化矽與單晶矽介面間應用高斯定律（*Gauss's Law*）來定義臨界電壓。在推導出的二維電位分佈函數之基礎下，我們提出了一新方法用以避免傳統欲求得最小表面電場位置時，可能需要的重複運算以及時間耗費。我們將使用垂直平均電場來替代前二氧化矽/單晶矽介面間最小表面電場，並由此來定義臨界電壓。但是，這將會忽略了來自源極及汲極接面的側向電場侵入。因此，我們將引入一

具有物理意義之修正因子以彌補此一可能產生的錯誤，並且提升此解析模型之準確性。經由二維數值分析比較之後，證實此模式可準確地預測完全空乏型之單晶矽/二氧化矽金氧半場效電晶體在各種不同結構及外加偏壓下之臨界電壓。

在第三章中，我們將前一章所得之臨界電壓模式對於汲極電壓加以線性化，置入線性區域之電流－電壓解析模式中，以考慮汲極導引位障降低（*Drain–Induced Barrier Lowering*, DIBL）效應。此外，並將溫度提昇模型一併考慮在內。接著，在飽和區域之電流－電壓解析模式中包含了汲極飽和電壓模式以及通道長度調變模式（*Channel Length Modulation*, CLM）。再者，次臨界區域電流－電壓解析模式也涵蓋在內。其中，寄生電阻、溫度、撞擊離子化及寄生雙載子電晶體等效應皆內含於所提出之電流－電壓解析模式中。經由實驗結果分析比較之後，發現所得到的解析模式可以準確地估算完全空乏型之單晶矽/二氧化矽金氧半場效電晶體在各種不同外加偏壓下電流－電壓關係。

在第四章中，我們將探討具有大傾角佈植結構之短通道完全空乏型單晶矽/二氧化矽金氧半場效電晶體，並建立其電位分佈、臨界電壓以及次臨界電流之解析模式。首先，我們應用三階連續函數於二維帕松方程式，配合適當的邊界條件，解出單晶矽內部的二維電位分佈，並進而推得前閘二氧化矽與單晶矽介面處之電位分佈。接著，藉由求出最低表面電位，進而導出臨界電壓解析模式。此外，配合漂移－擴散電流方程式，我們推導出次臨界電流之解析模型。所提出的解析模式經由與二維數值模擬比較結果顯示，我們發現： 當通道長度縮減到 0.06 微米時，解析模式也能獲得令人滿意的結果。

第五章提出了一個適用於高頻電路方面應用之金氧半場效電晶體小信號模型及其相關參數之萃取方法。此小信號模型考慮了閘極區域內呈現連續分佈之閘極電阻、基板電阻網路及不可互逆的電容。在適當的假設及邊界條件之下，配合閘極區域之傳輸線方程式，即可求得位於閘極區域之電流及電壓關係式。接著，配合二埠電路模型，我們求得等效電路之 Y 參數。此外，以所求得之 Y 參數與頻率之關係為基礎，我們發展出一套準確的電路參數萃取方法。此參數萃取方法已成功地應用在實驗數據的參數取得上，我們發現其所萃取出的參數仍具有相當的物理意義。此外，將所萃取得之參數置入小信號模型中，經由計算結果與實驗數據比較分析後，我們得知： 即使當操作頻率提昇至 10 G 赫茲時，此小信號模型仍可準確預測電

晶體之高頻特性。

第六章中，在為了能夠同時萃取得金氧半場效電晶體交流及直流參數的動機之下，我們提出了一個參數萃取方法： 除了萃取得交流參數之外，藉由使用 S 參數量測方法來萃取金氧半場效電晶體之元件參數。所萃取的參數包含了臨界電壓、寄生串聯電阻、有效之載子遷移率以及元件尺寸相關參數。此參數萃取方法已成功地應用於實驗數據上，經由實驗數據以及模擬計算結果的分析比較之後，我們得知此一參數萃取方法提供了極佳的準確性。

第七章將本論文的重要貢獻做一整理回顧，並展望值得延伸探討的研究方向。

2–D Analysis and New Analytical Models for Fully–Depleted SOI Short–Channel MOSFETs

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ABSTRACT

The analytical models for the threshold voltage and drain current of short–channel fully–depleted SOI MOSFETs have been developed in this thesis. Additionally, new analytical models of potential distribution, threshold voltage and subthreshold current of short–channel fully–depleted SOI MOSFETs with halo and pocket implants have also been proposed. Moreover, a new small–signal model of MOSFETs and the relevant parameter extraction method are presented for high frequency applications. Based on the numerical analysis and experimental results, the validities of the developed analytical models are successfully verified.

This thesis is consisted of seven chapters. In Chapter 1, the potential advantages of SOI MOSFETs are globally discussed and the organization of the thesis is given. In Chapter 2, a three–zone Green's function solution method is proposed to analytically model the potential distributions in the front/bottom oxide and silicon regions of the fully–depleted SOI MOSFETs. The exact solution of 2–D Poisson's equation is obtained by means of the Green's theorem, in which the Green's function solutions are determined according to the appropriate boundary conditions. The threshold voltage is defined by applying the Gauss's Law to the surface of the silicon film. Based on the derived 2–D potential distribution, a new approach of approximating the normal electric field at the location of minimum surface potential with the average electric filed is proposed to avoid the

iterations in solving the position of the minimum surface potential. In the development of the analytical threshold voltage model, a modified factor accounting for the lateral electric encroachment from the drain junction is further introduced to compensate the error resulted from the above approximation. Comparisons between the developed analytical threshold voltage model and the 2D numerical analysis are presented. It is shown that good agreements are achieved for wide range of device structure parameters and applied biases.

In Chapter 3, a new analytical model for I–V characteristics of fully–depleted SOI MOSFETs is proposed, in which an analytical threshold voltage model considering the drain–induced barrier–lowering (DIBL) effect and a temperature raise model are incorporated. The DIBL factor, which is obtained by linearizing the threshold voltage model derived in the Chapter 2, is then incorporated into the I–V model in the linear region. In the saturation region of the I–V model, a quasi–2D saturation model, which includes a source–drain saturation voltage model and a channel length modulation model is presented. Furthermore, the effects of the parasitic series resistances, temperature raise, impact ionization and parasitic bipolar junction transistor are included in the developed I–V model. It is shown that good agreements are obtained between the experimental data and the simulation results.

In Chapter 4, new analytical models of subthreshold surface potential, threshold voltage and subthreshold current for the fully–depleted SOI MOSFETs with halo or pocket implants are developed. By using the cubic series function method, the 2–D Poisson's equation for the fully–depleted SOI MOSFETs with halo implants is solved with the proper boundary conditions. Then, the subthreshold surface potential model is consequentially derived. Further, the threshold voltage model is defined by the minimum surface potential. Moreover, with the aids of the drift–diffusion current equation, the analytical subthreshold current model is derived. These derived analytical models have been compared with the 2–D numerical analysis and excellent agreements are obtained, which validates the accuracy of the models.

In Chapter 5, a new small–signal MOSFET model and a relevant parameter extraction method

are proposed for RF IC applications. The small–signal model considers the distributed gate resistances, substrate network and the nonreciprocal capacitance. With the suitable assumptions and boundary conditions, the transmission line equation along the gate region is solved. Then, by applying the two–port circuit model, the *Y*–parameters of the small signal circuit are obtained. An extraction method for the relevant parameters of the small signal model is presented in detail. The extraction method has been applied to the experimental data and the extracted parameters show good physical meanings. Furthermore, with the extracted parameters, the derived *Y*–parameters are in a good agreement with the experimental data for the frequency up to 10 GHz, which shows the validity of the developed small signal MOSFET model and the parameter extraction method.

In Chapter 6, an efficient method using *S*–parameters measurement is proposed for the extractions of the threshold voltage, parasitic series resistances, effective mobility and geometric dimensions of the MOSFETs. The proposed method provides the simultaneous extractions of the AC– and DC–related parameters. The method has been applied to the experimental data for a wide range of geometries, and a good agreement is obtained between the experimental data and the simulation results.

Chapter 7 summarizes the conclusions of this thesis, in which the major contributions as well as the suggested future researches are given.

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

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Fig. 6–6 The plots of $F_1(V_{gs})$ versus $1/(V_{gs}–V_T)^2$ for n–MOSFETs with different drawn gate lengths. The symbols represent the experimental data and the solid lines are the best–fit straight line to the experimental data. The intercept on the $F_1(V_{gs})$ axis yields θ_2/β_0.

Fig. 6–7 The plots of the extracted results of V_T obtained by the proposed method and linear extrapolation method [90]. The filled circles represent the V_T obtained by the proposed method, and the open circles represent the results obtained by linear extrapolation method. Error bars show the 97%–confidence interval of V_T obtained by the proposed method.

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Fig. 6–11 The plots of the comparisons of the simulated results obtained by proposed method with the experimental data I_{ds} of n–MOSFETs with different drawn gate lengths.

Nomenclature

$\varepsilon_{si}[\varepsilon_{ox}]$	The dielectric permittivity of Si [SiO_2].
q	The elementary charge.
$\rho(x,y)$	The two-dimensional charge density.
t_{si}	The thickness of silicon film.
$t_{fox}[t_{box}]$	The thickness of front [back]-gate oxide.
n_i	The intrinsic carrier concentration of Si semiconductor.
$L[W]$	The effective channel length [width].
$C_{fox}[C_{box}]$	The capacitance per unit area of the front [back] gate oxide.
C_{si}	The capacitance per unit area of the silicon film.
$V_{GS}[V_{gs}]$	The external [intrinsic] gate-source voltage.
$V_{DS}[V_{ds}]$	The external [intrinsic] drain-source voltage.
$V_{BS}[V_{bs}]$	The external [intrinsic] back gate-source voltage.
$V_{FB}^{f}[V_{FB}^{b}]$	The flat band voltage of the front [back] gate.
$V_{gs}^{'}[V_{bs}^{'}]$	$V_{gs}^{'} = V_{gs} - V_{FB}^{f}[V_{bs}^{'} = V_{bs} - V_{FB}^{b}]$
$V_{bi}(y)$	The built-in potential of the source [drain]/ body junctions in Zone II.
$N_B f(y)$	The doping profile in the Zone II, where $f(y)$ is a doping profile function.
N_D	The doping concentration in the source/drain region.
k_n^i	The eigenvalue of Zone i $(i = I, II, III)$. $k_n^I = ((n-1/2)\pi)/t_{fox}$ for Zone I, $k_n^{II} = n\pi/t_{si}$ for Zone II and $k_n^{III} = ((n-1/2)\pi)/t_{box}$ for Zone III.
k_m	The eigenvalue in all Zones. $k_m = m\pi/L$.
$D_{sf}(x)[D_{sb}(x)]$	The electric displacement at the front [back] Si-SiO_2 interface.
$\phi^i(x,y)$	The 2-D potential distribution in Zone i $(i = I, II, III)$.
$E_y^i(x,y)$	The 2-D vertical electric field distribution in Zone i $(i = I, II, III)$.

$\phi_{sf}^{II}(x)\left[\phi_{sb}^{II}(x)\right]$ The front [back] surface potential in Zone II.

$Q_B^n\left[Q_B^0\right]$ The Fourier coefficient of the bulk charge density with the integer n $[n=0]$ in Zone II.

$$Q_B^n = \frac{2}{t_{si}}\int_0^{t_{si}}\left(-qN_B f(y)\right)\cos k_n^{II} y \cdot dy$$

$$Q_B^0 = \frac{1}{t_{si}}\int_0^{t_{si}}\left(-qN_B f(y)\right)\cdot dy$$

$D_{sf}^m\left[D_{sb}^m\right]$ The Fourier coefficient of the electric displacement at the front [back] surface.

$$D_{sf}^m = \frac{2}{L}\int_0^L D_{sf}(x)\sin(k_m x)\cdot dx$$

$$D_{sb}^m = \frac{2}{L}\int_0^L D_{sb}(x)\sin(k_m x)\cdot dx$$

$A_n^S\left[A_n^D\right]$ The Fourier coefficient of the boundary potential at the source [drain] side in Zone I.

$$A_n^S = \frac{2}{t_{fox}}\int_0^{t_{fox}}\phi^I(0,y)\cos k_n^I y\cdot dy$$

$$A_n^D = \frac{2}{t_{fox}}\int_0^{t_{fox}}\phi^I(L,y)\cos k_n^I y\cdot dy$$

$B_n^S\left[B_0^S\right]$ The Fourier coefficient of the source boundary potential with the integer n $[n=0]$ in Zone II.

$$B_n^S = \frac{2}{t_{si}}\int_0^{t_{si}}V_{bi}(y)\cos k_n^{II} y\cdot dy$$

$$B_0^S = \frac{1}{t_{si}}\int_0^{t_{si}}V_{bi}(y)\cdot dy$$

$B_n^D\left[B_0^D\right]$ The Fourier coefficient of the drain boundary potential with the integer n $[n=0]$ n Zone II.

$$B_n^D = \frac{2}{t_{si}}\int_0^{t_{si}}\left[V_{bi}(y)+V_{ds}\right]\cos k_n^{II} y\cdot dy$$

$$B_0^D = \frac{1}{t_{si}}\int_0^{t_{si}}\left[V_{bi}(y)+V_{ds}\right]\cdot dy$$

$C_n^S \left[C_n^D\right]$ The Fourier coefficient of the boundary potential at the source [drain] side in Zone III.

$$C_n^S = \frac{2}{t_{box}} \int_0^{t_{box}} \phi^{III}(0, y) \cos k_n^{III} y \cdot dy$$

$$C_n^D = \frac{2}{t_{box}} \int_0^{t_{box}} \phi^{III}(L, y) \cos k_n^{III} y \cdot dy$$

$\phi_{f,inv}$ The front surface potential at the onset of strong inversion.

$$\phi_{f,inv} = 2\phi_{fp} = 2\left(k_B T / q\right) \ln\left(N_B / n_i\right)$$


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Chapter 1
Introduction

1–1 General Introduction

Since mid–1960s, the Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) has been treated as the most important electronic device, superseding the Bipolar Junction Transistor (BJT) and initiating a revolution in the Integrated Circuit (IC) industry. According to the statistics, more than 95% of the available microelectronic products are fabricated by the silicon–based technology, among which the bulk–MOS device stands for the most pronounced branch. Nowadays, it has invaded our daily lives by the magic power derived from its simple structure and low fabrication cost. For these reasons, the MOS technologies, especially the Complementary Metal–Oxide–Semiconductor (CMOS), are taken as the major trend for Ultra–Large–Scale–Integration (ULSI) circuit and mass–production product. Other than the compact density, the figures of merit for IC performance also include high speed and low power consumption. In order to increase the packing density and to improve the circuit performance, the geometries of the bulk–MOS device have been continually scaled down [1]–[5]. However, as the bulk–MOS devices shrink to deep–submicrometer regime, several problems such as gate oxide reliability, shallow junction, parasitic capacitance, device isolation and radiation/plasma damage occur, and those limit the further scaling of the bulk–MOS devices [6]–[8]. Therefore, many manufacture techniques have been found to reduce the effects of these problems such as making shallow junction with raised source/drain regions, using deep trench isolation or epitaxial substrate to prevent the occurrence of the latchup, reduce the junction capacitance with Silicon–On–Insulator (SOI) technique, etc [9]–[11]. Among these techniques, the SOI CMOS technique is the most attractive one because it involves less processing steps than the bulk CMOS technique, and suppresses some yield hazard factors present in bulk CMOS.

Recently, the SOI MOSFETs have drawn much attention for its advantages over bulk MOSFETs such as elimination of latch–up problem, excellent device isolation, reduced junction capacitances and improved radiation hardness. The advantages of the SOI MOSFETs are discussed and described as follows.

a) Elimination of latch–up effect

In the bulk CMOS technique, the latch–up effect is originated from the parasitic PNP (NPN) structure residing in the CMOS circuit. The latch–up path can be represented by two bipolar transistors (Q_1 and Q_2) and parasitic resistances (R_s and R_w), as shown in Fig. 1–1(a) and (b). The latch–up can be triggered by several different mechanisms, such as junction avalanche, voltage overshoot and displacement current [10]. The necessary condition for the occurrence of latch–up is that the current gain of the loop formed by these two bipolar transistors is larger than unity. However, in the SOI CMOS circuit, e.g., inverter, due to the existence of the high dielectric isolation between the active regions and substrate, the latch–up path is ruled out because no current path to the substrate exists, as shown in Fig. 1–1(c).

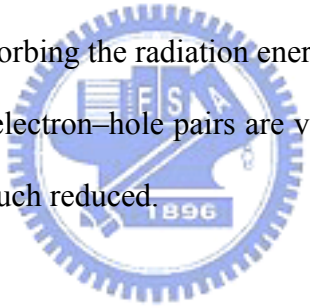
b) Reduced parasitic capacitances

In the bulk MOSFETs, the parasitic junction capacitances, i.e., source–to–substrate and drain–to–substrate capacitances, which consist of two components: the capacitance between the source/drain and the substrate regions in the vertical direction, and the capacitance between the source/drain and the channel regions in the lateral direction, as shown in Fig. 1–2(a). These capacitances may increase with the substrate doping concentrations as the devices are shrunk to smaller geometries. However, in SOI MOSFETs, the junction capacitance in the vertical direction is replaced by the capacitance of buried oxide that is typically lower than the junction capacitance in bulk MOSFETs, as shown in Fig. 1–2(b). The reduced parasitic capacitance properties of the SOI MOSFETs make them very suitable for high–speed applications such as RF IC's and

telecommunication.

c) Excellent radiation hardness

Figure 1–3 shows the radiation effects on bulk and SOI MOSFET. From the figure, it is seen that the radiation effects are different for bulk and SOI MOSFETs. In general, when the MOSFETs are exposed in the radiation environment, the silicon volume would absorb the energy of radiation and subsequently the electron–hole pairs would be generated [12]. The radiation–induced electron–hole pairs may be collected by the source/drain junctions and contribute to the leakage current, and consequently soft–error may occurs. For SOI MOS devices, due to that the active region is isolated from the substrate, the radiation–induced electron–hole pairs generated in the substrate would not influence the device performance. Besides, due to that the volume of the active region above the buried oxide for absorbing the radiation energy, and the source/drain junction areas for collecting the radiation–induced electron–hole pairs are very small, the probability of occurring the soft–error for the SOI circuit is much reduced.



d) Simple IC processing

Although the process techniques for the fabrication of CMOS circuit in bulk silicon wafer and in SOI wafer are very similar, the SOI fabrication process is simpler than bulk one. Firstly, there is no need to do the essential well implantation (even twin well), which is a necessary in the bulk CMOS process, in the SOI CMOS process. Besides, the guard–ring structure in the bulk CMOS circuit to suppress the latch–up problem is also unnecessary in SOI CMOS process. Secondly, due to the presence of the buried oxide film underneath the active region, the SOI isolation process is more effective in the isolating the active islands from one another. Thirdly, the source/drain shallow junctions are essential in the deep–submicrometer regime to ensure the less short–channel effects, but it is a difficult task for the bulk CMOS process. In the shallow junction processing, a harmful spiking effect may take place between the silicon substrate and metal conductor through the

source/drain junctions, as shown in Fig. 1–4. Such a junction punch–through may give rise to the uncontrolled leakage current. However, the source/drain junctions can be extended to the buried oxide in the SOI CMOS process, and hence the shallow junctions could be obtained.

e) High integration density

Generally speaking, the SOI CMOS circuit can offer a higher integration density than bulk CMOS circuit. This can be observed from the layouts of the bulk CMOS inverter and SOI COMOS inverter shown in Fig. 1–5. It is seen that the area of the SOI CMOS inverter is smaller than that of the bulk CMOS inverter. This happens due to the following reasons. The major reason is the absence of the well in SOI CMOS, and consequently the number of the well contact is decreased. The second reason is that the possibility of having a direct contact between the P^+ and N^+ junctions, such as the drain regions of the *p*–channel and *n*–channel devices shown in Fig. 1–5. Moreover, the removal of the guard–ring structure could also increase the integration density.

Depending on the relation of the thickness of silicon film to the maximum depletion width while the SOI MOSFET is turned on, two types of SOI MOS devices can be distinguished. One is the Fully–Depleted (FD) SOI MOSFET, where the silicon film is completely depleted, and the other one is the Partially–Depleted (PD) SOI MOSFET, where a neutral region exists other than the depleted region. Except for the advantages of the SOI CMOS technique mentioned above, there are two unique features of SOI MOSFETs needed to be considered and described in the following.

1) Floating–body effect: The most prominent electrical property of the PD–SOI device is that the body is floating, and subsequently the body voltage would vary during switching. The variation of the floating body potential may cause the threshold voltage vary, and consequently the I–V characteristics of the PD–SOI devices are no longer constant. The voltage of the floating body is dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body, and the distribution of the charge are determined by the p–n junction leakage currents, the impact ionization current, and the capacitive coupling from the external

terminals during operation transitions. The variation of the threshold voltage resulting from the content of the charge in the body may cause a “kink effect” in the I–V characteristics of the devices [13]. However, the kink effect is undesirable for analog circuit because of the lower output resistance. Furthermore, due to the parasitic bipolar transistor presented in the SOI MOSFETs, the floating body effect may cause the reduction of the drain–source breakdown voltage. The classical remedy to the floating body problem is the use of a body contact. On the other hand, for the FD–SOI MOSFETs, due to the completely depleted region in the silicon film, the charge storage in not observe. Therefore, to understand, characterize and model the floating–body effect is essential in SOI CMOS technique.

2) Self–heating effect: Due to the presence of the buried oxide film beneath the device active region, SOI CMOS technique owns several advantages over the bulk CMOS one as mentioned in previous subsections. However, the low thermal conductivity of the buried oxide reduces the efficiency in removing the generated heat. In bulk technologies, heat generated by the charge transfer in the device can be readily removed out of the chip backside through the crystalline silicon substrate. The removal of the heat is quick enough that the local device performance change due to the self–heating is negligible. On the other hand, in SOI technique, it seems that the MOS device is encased in a perfect insulated region of its own, with inter–layer dielectric above, shallow trench isolation dielectric to the left and right sides, and buried oxide film underneath. As a result, the heat generated by the charge transfer is hard to be removed out through these dielectric films, and consequently an elevated device temperature is observed [14]. This phenomena is so–called Self–Heating Effect (SHE). The temperature increase induced by the SHE may give rise to some parameter variations such as carrier mobility and threshold voltage, and the further influence on the device performance. It must be emphasized that these effects would take place as the heat is dissipated into the device. In reality, in an operating digital CMOS circuit, there is almost zero current flowing through the devices in the standby mode. Therefore, the self–heating effects are greatly reduced.

From the above discussion, we believe that the SOI technology is a preferable choice for the deep–submicrometer generation in the applications of low power, high speed and high reliable integrated circuits.

1–2 Organization of the Thesis

In Chapter 2, the 2–D Poisson's equation is solved for a SOI MOSFET by using the three–zone Green's function technique with the appropriate boundary conditions. In Section 2–2, the exact solution of the 2–D potential distribution in the silicon film is obtained and a 2–D analytical threshold–voltage model is derived based on the concept of the average electric field. Comparisons between the 2–D numerical analysis, experimental data and the proposed analytical threshold voltage model are shown in Section 2–3. Finally, the conclusions are summarized in Section 2–4.

Based on the threshold–voltage model developed in Chapter 2, a new analytical I–V model is derived for fully–depleted SOI MOSFETs in Chapter 3. In Section 3–2, the derived threshold voltage is linearized with respect to the drain voltage to obtain the DIBL factor, which is subsequently incorporated into the I–V model derivation. The new I–V model accounts for the effects of the parasitic series resistances, self–heating effect, channel length modulation, impact ionization and parasitic bipolar junction transistor. The comparisons with the measured data and 2–D numerical simulation results are presented in Section 3–3. Conclusions are given in the final Section 3–4.

In Chapter 4, the 2–D Poisson's equation is solved for a fully–depleted SOI MOSFET with halo or pocket implants by assuming a power series potential distribution in the silicon film with the proper boundary conditions. The derivations of the surface potential model are given in Section 4–2. The derived surface potential model is further implemented to obtain an analytical threshold voltage model in Section 4–3. Moreover, with the derived surface potential model, an analytical subthreshold current is developed in Section 4–4. The calculated results of the subthreshold surface potential distribution, threshold voltage and subthreshold current are compared with the 2–D

numerical analysis in Section 4–5. Conclusions are summarized in Section 4–6.

In Chapter 5, a high frequency analytical MOSFETs model is proposed to account for the distributed effects of the gate region, substrate parasitics and nonreciprocal capacitance. Besides, a direct parameter extraction method for the proposed model is also presented. The derivations of the small signal MOSFET model is described in Section 5–2. The details of the extraction method are shown in Section 5–3. The verifications of the small signal MOSFET model and extraction method are presented in Section 5–4. Eventually, the conclusions are given in the section 5–5.

In Chapter 6, a simple method based on the small–signal conductance extracted by *S*–parameters measurements is proposed to accurately extract the threshold voltage, the parasitic series resistance, gain factor, and mobility degradation parameters. In Section 6–2, the parameter extraction method is described in detail. Subsequently, the present extraction method is performed for the parameters of the test devices with different geometries. The comparisons of the results obtained by the proposed method with the experimental data are presented and discussed in Section 6–3. The conclusions are summarized in Section 6–4.

In the concluding chapter, the major contribution of the thesis is given is Section 7–1. Future researches deserved further efforts are proposed in Section 7–2.

Chapter 2

A Simple 2–D Analytical Threshold Voltage Model for Fully–Depleted Short–Channel SOI MOSFETs

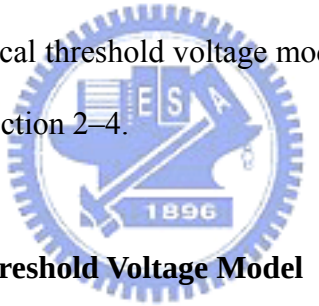
2–1 Introduction

The fully depleted (FD) silicon–on–insulator (SOI) CMOS technology has been becoming another major technology for the next generation of VLSI [15–17]. This is because that the FD SOI CMOS transistors provide superior electrical characteristics over bulk CMOS devices [18–20] such as reduced source/drain junction capacitances [21], increased carrier mobility [22], suppressed short channel effect [23], improved subthreshold slope [24], improved latchup immunity [25] and better radiation hardness [26]. However, the coupling effect between the front gate and back gate becomes complicated, especially for short channel devices. Therefore, it is difficult to develop a simple and accurate analytical model for circuit design and device characterization.

In general, the threshold voltage of a MOS transistor is a very important physical parameter in the device design. On the other hand, the accuracy of the threshold voltage model plays a more important role in the device optimization and circuit design. The analytical modeling of the threshold voltage of the FD SOI MOS transistor has already been proposed by numerous authors [27–30]. In a paper by Young [27], the potential distribution in the Si film was approximated by a simple parabolic function. This simplified assumption underestimates the coupling effect of the source/drain region and may cause a significant error in the prediction of the threshold voltage when the channel length continues to scale down. In a paper by Veeraraghavan and Fossum [28], the threshold voltage model was developed based on the conventional charge–sharing scheme and it predicted a $1/L_{eff}$ dependent threshold voltage shift. In the range of submicrometer channel length, the assumption of the constant surface potential of the charge–sharing model is invalid. In a paper

by Woo *et al*. [29], the work was done by the decomposition of the 2–D Poisson's equation into a 1–D Poisson's equation and a 2–D Laplace equation. In a paper by Guo and Wu [30], an accurate 2–D analytical threshold voltage model was developed by means of a three–zone Green's function solution technique. Although a closed form of the threshold voltage is derived, the calculation is too complicated to be further implemented in the derivation of the I–V model for a simulator like SPICE. Therefore, to consider an efficient computation, the simplified and explicit expression of the threshold voltage of the FD SOI MOS transistor is necessary.

In this chapter, in order to derive the threshold voltage model, the three–zone Green's function technique [30] is used to solve the 2–D Poisson's equation. Based on the concept of the average vertical electric field, a simple and closed expression of the threshold voltage is obtained and described in Section 2–2. Comparisons between the 2–D numerical analysis (Medici program), experiments and the proposed analytical threshold voltage model are shown in Section 2–3. Finally, the conclusions are summarized in Section 2–4.



2–2 Derivation of the Analytical Threshold Voltage Model

2–2.1 Basic Analysis

The conventional structure of a FD SOI MOS transistor for 2–D numerical simulation is presented in Figure 2–1. A simplified domain has been used for solving the 2–D Poisson's equation and indicated by the bolded lines in Figure 2–1. The domain for solving 2–D Poisson's equation is further divided into three sub–domains (Zones I, II and III) to avoid the complexity of calculating the equivalent charge density between the regions with different dielectrics. Zone I is the front gate oxide, zone II represents the Si film and zone III is the buried oxide. The boundary conditions used for each zone are enumerated in Table 1. It should be noted that the boundary potential in the y direction in the zones I and III are assumed to vary linearly [29].

Based on the assumption that the front gate oxide and buried oxide well grown and there is no

charge reside. The 2–D Poisson's equations in the zones I and III can be reduced to two 2–D Laplace equations. Substituting the Green's function solutions, listed in Table 2, into the Green's theorem [31], which is given as

$$\phi(x,y)=\iint\frac{\rho(x',y')}{\varepsilon}\cdot G(x,y:x',y')\cdot dx'dy' + \int G(x,y:x',y')\frac{\partial\phi}{\partial n'}ds' - \int\phi(x',y')\frac{\partial G}{\partial n'}ds' \tag{2–1}$$

where $G(x,y:x',y')$ is the Green's function satisfying $\nabla^2 G=-\delta(x-x')\delta(y-y')$; n' is the outward normal direction on the boundary surface, and neglecting the free carriers, the general form of the 2–D potential distribution in each zone can be obtained as follows [30]:

$$\phi^{I}(x,y)=\sum_{m=odd}^{\infty}\frac{4V_{gs}'}{m\pi}\frac{\cosh k_m y}{\cosh k_m t_{fox}}\sin k_m x-\sum_{m=1}^{\infty}\frac{D_{sf}^{m}}{\varepsilon_{ox}}\frac{\sinh k_m(t_{fox}+y)}{k_m\cosh k_m t_{fox}}\sin k_m x + \sum_{n=1}^{\infty}\frac{\cos k_n^{I} y}{\sin k_n^{I} L}\cdot\left[A_n^{s}\sinh k_n^{I}(L-x)+A_n^{D}\sinh k_n^{I} x\right] \tag{2–2}$$

$$\phi^{II}(x,y)=\frac{Q_B^0}{2\varepsilon_{si}}x(L-x)+\sum_{n=1}^{\infty}\frac{Q_B^n}{\varepsilon_{si}}\frac{\cos k_n^{II} y}{(k_n^{II})^2}\cdot\left[1-\frac{\sinh k_n^{II} x+\sinh k_n^{II}(L-x)}{\sinh k_n^{II} L}\right] + B_0^{S}\left(1-\frac{x}{L}\right)+B_0^{D}\frac{x}{L}+\sum_{n=1}^{\infty}\frac{\cos k_n^{II} y}{\sinh k_n^{II} L}\cdot\left[B_n^{S}\sinh k_n^{II}(L-x)+B_n^{D}\sinh k_n^{II} x\right] + \sum_{m=1}^{\infty}\frac{\sin k_m x}{\varepsilon_{si}k_m\sinh k_m t_{si}}\cdot\left[D_{sf}^{m}\cosh k_m(t_{si}-y)-D_{sb}^{m}\cosh k_m y\right] \tag{2–3}$$

$$\phi^{III}(x,y)=\sum_{m=odd}^{\infty}\frac{4V_{bs}'}{m\pi}\frac{\cosh k_m(y-t_{si})}{\cosh k_m t_{box}}\sin k_m x+\sum_{m=1}^{\infty}\frac{D_{sb}^{m}}{\varepsilon_{ox}}\frac{\sinh k_m(t_{box}+t_{si}-y)}{k_m\cosh k_m t_{box}}\sin k_m x + \sum_{n=1}^{\infty}\frac{\cos k_n^{III}(y-t_{si})}{\sin k_n^{III} L}\cdot\left[C_n^{S}\sinh k_n^{III}(L-x)+C_n^{D}\sinh k_n^{III} x\right] \tag{2–4}$$

where the definitions of the Fourier coefficients A_n^s, A_n^d, B_0^S, B_0^D, B_n^S, B_n^D, C_n^S, C_n^D, D_{sf}^m, D_{sb}^m, Q_B^0 and Q_B^n are given in the Nomenclature. In order to obtain the 2–D analytical solution of the potential distribution at the zone II, D_{sf}^m and D_{sb}^m have to be solved first. D_{sf}^m and D_{sb}^m can

be obtained by equating equations (2–2) and (2–3) at $y = 0$ and equations (2–3) and (2–4) at $y = t_{si}$, respectively. The related expressions are given in Table 3 for details. It should be noted that the above equations are exact in the sense that any arbitrary doping profile in the Si film can be treated. In the following analysis, the uniformly doped Si film is assumed for simplicity. Therefore, the 2–D potential distribution at the zone II can be further repressed as follows [30]:

$$\phi^{II}(x,y) = -\frac{qN_B}{2\varepsilon_{si}}x(L-x) + \sum_{m=1}^{\infty}\frac{\sin k_m x}{\varepsilon_{si}k_m \sinh k_m t_{si}}\cdot\left[D_{sf}^m \cosh k_m(t_{si}-y) - D_{sb}^m \cosh k_m y\right] + V_{bi} + \frac{x}{L}\cdot V_{ds}. \tag{2–5}$$

2–2.2 A New Approach for the Development of the Threshold Voltage Model

Since the FD SOI MOS transistor under consideration is normally–off type (enhancement mode), the front surface potential distribution of the Si film is usually used to monitor the turn–on status of FD–SOI MOSFETs. From equation (2–5), the potential distribution along the front surface of the Si film can be derived as:

$$\phi^{II}(x,0) = -\frac{qN_B}{2\varepsilon_{si}}x(L-x) + \sum_{m=1}^{\infty}\frac{\sin k_m x}{\varepsilon_{si}k_m \sinh k_m t_{si}}\cdot\left[D_{sf}^m \cosh k_m t_{si} - D_{sb}^m\right] + V_{bi} + \frac{x}{L}\cdot V_{ds}. \tag{2–6}$$

The accuracy of the derived front surface potential distribution in the Si film has been verified by the 2–D numerical analysis as shown in [30]. In the paper by Guo [30], to develop an analytical threshold voltage model, the minimum potential along the front surface of the Si film has to be calculated first. By differentiating the equation (2–6), the position of the minimum potential along the front surface of the Si film can be calculated.

$$\left.\frac{\partial\phi^{II}(x,0)}{\partial x}\right|_{x=x_{mim}} = \left.\frac{\partial\phi_{sf}^{II}(x)}{\partial x}\right|_{x=x_{mim}} = 0, \tag{2–7}$$

where $x_{\min}$ is the position of the minimum surface potential and $\phi_{sf}^{II}(x)$ represents the potential

distribution along the front surface of the Si film. By introducing the value of $x_{\min}$ into equation (2–6), the minimum surface potential $\phi_{sf,\min}^{II}$ can be obtained. However, the position of the minimum surface potential $x_{\min}$ can be only solved iteratively and no explicit form of $x_{\min}$ can be obtained. Therefore, the calculation of the minimum front surface potential is too complicated to be further implemented in the derivations of the analytical I–V model for a circuit simulator like SPICE.

The new approach for the development of the threshold voltage model is described in the following. Firstly, by differentiating equation (2–3) with respect to *y*, the normal electric field along the front Si film surface can be obtained and expressed as:

$$E_{sf}(x) = -\left.\frac{\partial \phi^{II}(x,y)}{\partial y}\right|_{y=0} = \sum_{m=1}^{\infty} \frac{D_{sf}^{m}}{\varepsilon_{si}} \sin k_m x. \tag{2–8}$$

Then, by integrating equation (2–8) with respect to *x* from *x = 0* to *x = L*, the total charge density controlled by the front gate can be obtained and expressed as:

$$Q_{fg} = -\int_0^L \varepsilon_{si} E_{sf}(x) \cdot dx = -\sum_{m=1}^{\infty} \frac{D_{sf}^{m}}{k_m} \left[1 - (-1)^m\right] \tag{2–9}$$

By applying Gauss's law at the front SiO_2–Si interface, we obtain

$$E_{sf}(x) = \frac{C_{fox}\left(V_{gs} - V_{FB}^{f} - \phi_{sf}^{II}(x)\right)}{\varepsilon_{si}}. \tag{2–10}$$

From equation (2–10), the threshold voltage can be obtained as:

$$V_{TH} = V_{FB}^{f} + \phi_{f,inv} + \frac{\varepsilon_{si} E_{sf}(x_{\min})}{C_{fox}}, \tag{2–11}$$

where the threshold voltage is defined as the value of gate voltage V_{gs} for which $\phi_{sf,\min}^{II} = \phi_{f,inv} = 2\phi_{fp}$. However, the derivation of the equation (2–11) is still complicated and computationally inefficient due to the calculation of $x_{\min}$. Therefore, in this work, the average

normal electric field along the front surface of the Si film $\overline{E_{sf}}$ is used to substitute the $E_{sf}(x_{\min})$. From equation (2–9), $\overline{E_{sf}}$ can be obtained and expressed as:

$$\overline{E_{sf}} = \sum_{m=1}^{\infty} \frac{D_{sf}^{m}}{\varepsilon_{si} k_m L} \left[1-(-1)^m\right] \tag{2–12}$$

Then, the threshold voltage can be redefined as:

$$V_{TH} = V_{FB}^{f} + \phi_{f,inv} + \frac{\varepsilon_{si}\overline{E_{sf}}}{C_{fox}}. \tag{2–13}$$

Due to the effect of the lateral electric field originating from the source/drain junctions, the average normal electric filed along the front surface of the Si film is expected to be smaller than the normal electric filed at the position of minimum potential. Therefore, in order to compensate the error results from the charge–sharing effect, a modification to the equation (2–13) is necessary.

Figure 2–2 shows the normal electric field along the front SiO_2–Si interface of the FD SOI MOSFETs, where the case of the average surface normal electric field is shown in (a) and the case of the surface normal electric field accounting for the charge–sharing effect is shown in (b). In Figure 2–2(a), the total depletion charges $Q_{depl,1}$ in the Si film that terminate the average surface normal electric field originating from the gate can be expressed as:

$$Q_{depl,1} = \varepsilon_{si}\overline{E_{sf}} \cdot W \cdot L \cdot t_{si}. \tag{2–14}$$

The charge–sharing effect is due to the loss of the control ability of the gate to the depletion charge under it. In other words, the depletion charge controlled by the gate is no longer equal to $Q_{depl,bulk}$ ($Q_{depl,bulk} = qN_B y_{d\max}$, for bulk MOSFETs, where $y_{d\max}$ is the maximum depletion width of the depletion region under the gate), but to a fraction of it. The reduction of the depletion charge is due to the presences of the source/drain junctions and the surface normal electric field is disturbed by the lateral electric field originating from the source/drain junctions, as shown in Figure 2–2(b). According to the charge–sharing scheme shown in Figure 2–2(b), the effective depletion charge controlled by the gate can be obtained as:

$$Q_{depl,2} = W \cdot \left(\int_0^L \varepsilon_{si} E_{sf}(x) \cdot dx \right) \cdot \frac{t_{si}}{2} (2L - \Delta L_1 - \Delta L_2)$$
$$= W \cdot Q_{fg} \cdot \frac{t_{si}}{2} (2L - \Delta L_1 - \Delta L_2) \quad (2\text{–}15)$$

where

$$\Delta L_1 \approx W_s = \left[\frac{2\varepsilon_{si} (V_{bi} - \phi_{f,inv})}{qN_B} \right]^{1/2},$$
$$\Delta L_2 \approx W_d = \left[\frac{2\varepsilon_{si} (V_{bi} + V_{ds} - \phi_{f,inv})}{qN_B} \right]^{1/2}.$$

where W_s and W_d are the depletion widths of the source– and drain–substrate junctions at the surface.

By equating equations (2–14) and (2–15), the relationship between Q_{fg} and $\overline{E_{sf}}$ can be obtained as

$$Q_{fg} = \varepsilon_{si} \overline{E_{sf}} \cdot \beta, \quad (2\text{–}16)$$

where

$$\beta = \frac{2L}{2L - \Delta L_1 - \Delta L_2} = \left\{ 1 - \frac{\Delta L_1 + \Delta L_2}{2L} \right\}^{-1}.$$

Therefore, in order to compensate the errors caused by the charge–sharing effect, we add the modified factor β into equation (2–13) and obtain the final expression of the analytical threshold voltage model:

$$V_{TH} = V_{FB}^f + \phi_{f,inv} + \frac{\varepsilon_{si} \overline{E_{sf}}}{C_{fox}} \cdot \beta. \quad (2\text{–}17)$$

After some mathematical manipulations, the equation (2–17) can be further expressed in terms of the terminal voltage as:

$$V_{TH} = V_{FB}^f + X \cdot \left\{ \phi_{f,inv} + \frac{\varepsilon_{si} \beta}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} \left[1 - (-1)^m \right] \left(G^m + F_b^m V_{bs}^{'} + \gamma F_d^m V_{ds} \right) \right\},$$
$$X = \left\{ 1 - \frac{\varepsilon_{si} \beta}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} F_g^m \left[1 - (-1)^m \right] \right\}^{-1}.$$

(2–18)

where the coefficients G^m, F_b^m, F_d^m and F_g^m are listed in Table 4 for details and γ is an empirical constant assumed to account for the errors resulting from the drain–induced barrier lowering effect.

2–3 Verifications and Discussion

In order to verify the accuracy of the derived equations, the analytical model of the V_{TH}, given in the equation (2–18), has been compared with the results obtained by the 2–D numerical device simulator Medici [32] and experimental data [33]. The threshold voltages of the results obtained by the 2–D numerical simulator are defined by the relationship between the drain current and external gate–source voltage as follows. In general, the drain current in the non–saturation region can be expressed as

$$I_{DS} = \frac{W_{eff} C_{fox} \mu_{eff}}{L_{eff}} \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS} \right) \cdot V_{DS} . \tag{2–19}$$

For the long channel length devices operating at low V_{DS} (e.g., $V_{DS} = 50$ mV), using the extrapolation method on the $I_{DS} - V_{GS}$ curve at V_{GS} equal to the voltage at which the maximum dI_{DS}/dV_{GS} occurs, the threshold voltage can be obtained by the intercept on the V_{GS}–axis.

$$V_{TH} = V_{GS,\mathrm{int}ercept} - \frac{1}{2} V_{DS} . \tag{2–20}$$

Additionally, when $V_{GS} = V_{TH}$, the normalized drain current is defined as a reference current.

$$I_{reference} = I_{DS,normalized} = \frac{L_{eff}}{W_{eff}} I_{DS,longL} \tag{2–21}$$

where $I_{reference}$ is the reference current, $I_{DS,normalized}$ is the normalized drain current and $I_{DS,longL}$ is the drain current of the long channel device. When the channel length is very short, the maximum transconductance extrapolation method would fail due to the significant short channel effect. Thus, the threshold voltage of the short channel device is extracted by equating the normalized drain current to the reference current, which is determined by the long channel device. For high V_{DS}

operation, V_{TH} is extracted from the parallel shift of $\ln(I_{DS})$ versus V_{GS} in the subthreshold region, as mentioned in [33].

The comparisons of the threshold voltage versus effective channel length of the fully depleted SOI MOSFET's with 11 nm front gate oxide, 330 nm buried oxide and $1\times10^{17}cm^{-3}$ bulk doping concentration for different Si film thicknesses are shown in Figure 2–3 when $V_{DS}=0.05V$ and $V_{BS}=0V$. In this figure, it is expected to see that the roll–off of the threshold voltage is severer in the case of thicker Si film due to the short channel effect. In other words, the V_{TH} roll–off starts to occur at larger gate lengths in the MOS transistors with thicker Si film thicknesses. Additionally, it is clearly seen that the calculated results using the present model agree very well with the 2–D numerical analysis.

Figure 2–4 shows the comparisons of the threshold voltage versus effective channel length for the devices of 70 nm Si film, 330 nm buried oxide and $1\times10^{17}cm^{-3}$ bulk doping concentration with front gate oxide as the parameter. From this figure, it is seen that the devices with thinner front gate oxides can significantly retard the roll–off of the V_{TH} as the channel length getting shorter. This is because that with thinner front gate oxide, the ability of control of the gate to the depletion region under it becomes better. It is also seen that a good agreement is obtained between the simulated results and 2–D numerical analysis.

Figures 2–5 and 2–6 compare the roll–off of the threshold voltages for different back gate voltages with 2–D numerical analysis and experimental data. As can be seen, the present model correctly predicts the V_{TH} roll–off for different back gate biases. Figure 2–7 shows the effect of the drain voltage on the roll–off of the threshold voltage of the devices with 1.6 nm front gate oxide, 400 nm buried oxide, 21 nm Si film and $1.5\times10^{18}cm^{-3}$ bulk doping concentration. It is expected to see that at larger drain bias, the encroachment field from the drain becomes more significant, especially at small channel length. From this figure, the accurate predictions of the severe threshold voltage roll–off by the proposed model are obtained, even for the devices with 0.07 μm channel length. Figure 2–8 shows the comparisons of the threshold voltages obtained by

the present model with the experimental data for the devices biased at different drain voltages. In this figure, it is seen that a good agreement is obtained between the simulated results and the experimental data. Eventually, the present model is compared with the numerical data used in [30] (Figs. 5–7) and the compared results are shown in Figure 2–9. From the figure, it is seen that a good agreement is obtained and evaluates the validity of the modified model.

2–4 Conclusions

In this chapter, we propose an analytical threshold voltage model for deep–submicrometer FD SOI MOSFET's using three–zone Green's function technique to solve the 2–D Poisson's equation and adopting a new concept of the average electric field to avoid the iterations in solving the position of the minimum surface potential. Firstly, we obtain the 2–D potential distribution in the Si film region by using Green's function technique to solve the 2–D Poisson's equation. By applying Gauss's law at the Si–SiO_2 interface, the initial expression of the threshold voltage is obtained. Then, we introduce a modified factor to compensate the errors resulting from the charge–sharing effect in the derivations of the final threshold voltage model. The proposed model is validated against the data obtained from 2–D numerical analysis and experimental data and excellent agreements are obtained. From the above discussion, it can be seen that the present model predicts the threshold voltage well and has no iteration problem in the calculation that exists in the previous work [30].

Chapter 3

A New Analytical I–V Model for Fully–Depleted Short–Channel SOI MOSFETs

3–1 Introduction

Fully–depleted silicon–on–insulator (FD SOI) MOSFET's are considered as the possible successors for the bulk MOSFET's in the applications of low power and high speed circuit designs, as they offer various attractive characteristics such as suppressed short channel effects, reduced junction capacitance, excellent latchup immunity and improved subthreshold swing [15, 17, 19 and 20]]. As a consequence, the SOI circuit design and device simulation are getting increasingly important in the deep submicrometer range of the VLSI technology. Therefore, for the reliable analysis and design of the SOI circuits, accurate and physically based I–V models are needed.

As the channel length of the SOI MOS transistor scales down, the effect of the threshold voltage roll–off due to the charge sharing and drain–induced barrier–lowering effects (DIBL) should be taken into account. Besides, due to the low thermal conductivity of the buried oxide, which inhibits the efficient cooling of the active devices, a significant self–heating effect (SHE) of the silicon film [34] arose and should be also considered. The increasing lattice temperature may cause a reduced drain current and even a negative differential conductance at high power inputs [35]. Additionally, as the devices biased at high current level, the parasitic source/drain resistances and impact ionization effect are noticeable and should be accounted for, especially in the saturation region and small gate voltage.

Several analytical I–V models for thin–film SOI MOSFETs had been developed in [29, 36–38]. The 2–D analysis of the conduction channel by Woo *et al.* [29] calculated the channel current by assuming a linearly varied channel surface potential. This assumption would cause a significant error in the prediction of the threshold voltage, especially when the drain bias is large. In a paper by

Hsiao *et al*. [36], the source/drain series resistances and the effect of the drain induced conductivity enhancement were considered. However, this model may have error in the prediction of the high current level due to the exclusion of the effects of the impact ionization effect and self–heating. In the paper by Hu *et al.* [37], the above effects mentioned were included in the I–V model derivation, but an additional smooth function was needed to make a smooth transition for V_{DS} between linear and saturation regions. In a paper by Iniguez *et al.* [38], they improved the continuity through the transition regions based on the charge sheet model, but lacked the effects of self–heating and parasitic series resistances.

In this chapter, the model derivations are described in Section 3–2. The simplified analytical threshold voltage model developed in the previous chapter is utilized and it is linearized to obtain the DIBL factor in Section 3–2.1 that is incorporated in the derivations of the analytical I–V model. Then, a complete analytical drain current model for the deep submicrometer SOI MOSFETs is presented in Section 3–2.2 to account for the effects of the parasitic series resistances, drain–induced barrier–lowering, channel length modulation, impact ionization and parasitic bipolar junction transistor. The temperature rise model and temperature dependent parameters are described in Section 3–2.3. The comparisons with the measured data and 2–D numerical simulations for devices with a wide range of parameters in all regions of device operation are presented in Section 3–3. Conclusions are given in the final section.

3–2 Model Derivations

3–2.1 Analytical Threshold Voltage Model

It is known that the drain–induced barrier–lowering effect has great influences on the I–V characteristics of MOSFETs in both the below– and above–threshold operation regions when the channel lengths of MOS devices become very short. It is beneficial for the designers to predict the device I–V characteristic accurately and efficiently if these short channel effects are well described

and modelled as a simple analytical expression. To simply the derivation of an analytical I–V model, a DIBL factor is introduced to account for the drain bias effect by a linearization of the threshold voltage with respect to the drain bias at very small drain voltage. The DIBL factor can also be incorporated into the electron mobility model.

Based on the simplified 2–D threshold voltage model developed in Chapter 2, an analytical I–V model is derived for fully–depleted SOI MOSFETs. The threshold voltage model can be rewritten as:

$$V_{TH} = V_{FB}^{f} + \frac{\phi_{f,inv} + \frac{\varepsilon_{si}\beta_0}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} \left[1-(-1)^m\right] \left(G^m + F_b^m V_{bs}^{'} + \gamma F_d^m V_{ds}\right)}{1 - \frac{\varepsilon_{si}\beta}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} F_g^m \left[1-(-1)^m\right]}, \tag{3–1}$$

Differentiating eq. (3–1) with respect to drain bias at very low drain voltage, the DIBL factor K can be obtained by taking the negative derivative:

$$K = -\left(\frac{dV_{TH}}{dV_{ds}}\right)_{V_{ds}=0} = (-1)\cdot \frac{\frac{\varepsilon_{si}\beta_0^{'}}{C_{fox}} M_2 \cdot \left(1 - \frac{\varepsilon_{si}\beta_0^{'}}{C_{fox}} \cdot M_3\right) + \frac{\varepsilon_{si}}{C_{fox}} M_0 \cdot \left(M_1 + \phi_{f,inv} \cdot M_3\right)}{\left(1 - \frac{\varepsilon_{si}\beta_0^{'}}{C_{fox}} M_3\right)^2},$$

$$M_0 = \frac{\varepsilon_{si}}{2qN_B W_s L}\left(1 - \frac{\Delta L_1}{L}\right)^{-2} \cdot \left(1 + \frac{2W_s}{t_{si}}\right)^{-1/2}$$

$$M_1 = \sum_{m=0}^{\infty} \frac{1}{d_0^m} \left(G^m + F_b^m V_{bs}^{'}\right)\left[1-(-1)^m\right]$$

$$M_2 = \sum_{m=0}^{\infty} \frac{1}{d_0^m} \gamma F_d^m \left[1-(-1)^m\right]$$

$$M_3 = \sum_{m=0}^{\infty} \frac{1}{d_0^m} F_g^m \left[1-(-1)^m\right]$$

$$\beta_0^{'} = \left(1 - \frac{\Delta L_1}{L}\right)^{-1} \tag{3–2}$$

Then the threshold voltage of a fully depleted thin film SOI MOSFET can be rewritten as:

$$V_{TH} = V_{TH0} - K \cdot V_{ds}, \tag{3–3}$$

where V_{TH0} is the threshold voltage of the SOI MOSFET at zero drain bias and is expressed as:

$$V_{TH0} = V_{FB}^{f} + \frac{\phi_{f,inv} + \frac{\varepsilon_{si}\beta_0}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} \left[1-(-1)^m\right] \left(G^m + F_b^m V_{bs}^{'}\right)}{1 - \frac{\varepsilon_{si}\beta_0}{C_{fox}} \sum_{m=1}^{\infty} \frac{1}{d_0^m} F_g^m \left[1-(-1)^m\right]}. \quad (3\text{–}4)$$

3–2.2 Analytical I–V model

3–2.2.1 I–V Characteristics in Linear Region ($V_{gs} > V_{TH}$, $V_{DS} < V_{DSAT}$)

It is known that the conduction current in the above–threshold region is contributed by the drift motion of the inversion carriers. When the drain voltage is smaller than the drain saturation voltage, the MOS transistor is operated in the linear region and the drive current can be expressed as [39]:

$$I_{DS} = \frac{W}{L}\mu_{eff} C_{fox}\left(V_{gs} - V_{TH} - \frac{1}{2}V_{ds}\right)\cdot V_{ds} = \frac{W}{L}\mu_{eff} C_{fox}\left[V_{gs} - \left(V_{TH0} + KV_{ds}\right) - \frac{1}{2}V_{ds}\right]\cdot V_{ds} \quad (3\text{–}5)$$

where V_{TH} is the threshold voltage derived in the previous section and is a function of the drain bias, and μ_{eff} is the effective mobility and expressed as [40]:

$$\mu_{eff} = \frac{\mu_n}{1 + \frac{\alpha C_{fox}}{2\varepsilon_{si}}\left[V_{gs} + V_{TH} - 2\left(V_{FB}^{f} + \phi_{f,inv}\right) - \frac{1}{2}V_{ds}\right] + \left(\eta + \frac{\beta}{L}\right)\cdot V_{ds}} \quad (3\text{–}6)$$

where μ_n is the maximum low filed mobility in the inversion layer, and the constant α (β, η) is the transverse (longitudinal) electric field degradation factor in the mobility model. Considering the parasitic source and drain resistances R_S and R_D, the intrinsic gate– and drain–to–source voltages V_{gs} and V_{ds} can be written in terms of the terminal voltages:

$$\begin{aligned} V_{gs} &= V_{GS} - I_{DS}\cdot R_S \\ V_{ds} &= V_{DS} - I_{DS}\cdot\left(R_S + R_D\right) \end{aligned} \quad (3\text{–}7)$$

where V_{GS} and V_{DS} are the terminal voltages. Substituting equations (3–6) and (3–7) into equation (3–5), we may obtain the following equation:

$$AI_{DS}^2 + BI_{DS} + C = 0 \tag{3–8}$$

where

$$A = \frac{\alpha C_{fox}}{2\varepsilon_{si}}\left[(0.5+K)(R_D+R_S)-R_S\right]-\left(\eta+\frac{\beta}{L}\right)(R_D+R_S)$$
$$+\frac{R_D+R_S}{L}\mu_n C_{fox} W\left[(0.5-K)(R_D+R_S)-R_S\right]$$

$$B = 1+\frac{\alpha C_{fox}}{2\varepsilon_{si}}\left[V_{GS}+V_{TH0}-2\left(V_{FB}^f+\phi_{f,inv}\right)-(0.5+K)V_{DS}\right]+\left(\eta+\frac{\beta}{L}\right)V_{DS}$$
$$+\frac{R_D+R_S}{L}\mu_n C_{fox} W\left(V_{GS}-V_{TH0}\right)-\frac{V_{DS}}{L}\mu_n C_{fox} W\left[2(0.5-K)(R_D+R_S)-R_S\right]$$

$$C = \frac{-\mu_n C_{fox} W}{L}\left[V_{GS}-V_{TH0}-(0.5-K)V_{DS}\right]\cdot V_{DS}$$

Solving equation (3–8), the drain current in the linear region can be expressed as:

$$I_{DS} = \frac{-B+\sqrt{B^2-4AC}}{2A} \tag{3–9}$$

It is noted that the drain current in the linear region is expressed in terms of the terminal voltages explicitly and can be obtained without any iteration.

3–2.2.2 I–V Characteristics in Saturation Region ($V_{gs} > V_{TH}$, $V_{DS} > V_{DSAT}$)

(a) Saturation Voltage V_{DSAT} and Saturation Current I_{DSAT}

As the drain voltage is increased, the longitudinal electric field in the channel region near the drain junction may reach the critical field E_c ($E_c = 1/\beta$) and the drift velocity of the carriers becomes saturated. Therefore, the saturation current at the saturation voltage can be expressed as:

$$I_{DSAT} = W\mu_{eff}C_{fox}\left[V_{gs} - V_{TH0} - (1-K)V_{dsat}\right]\cdot E_c \tag{3–10}$$

where V_{dsat} is the intrinsic saturation voltage. From equation (3–5), the drain current can be also expressed as:

$$I_{DSAT} = W\mu_{eff}C_{fox}\left[V_{gs} - V_{TH0} - \left(\frac{1}{2} - K\right)V_{dsat}\right]\cdot\frac{V_{dsat}}{L} \tag{3–11}$$

Equating equations (3–10) and (3–11), we can obtain the following equation:

$$A_1V_{dsat}^2 + B_1V_{dsat} + C_1 = 0 \tag{3–12}$$

where

$$A_1 = K - \frac{1}{2}$$
$$B_1 = (1-K)E_cL + V_{gs} - V_{TH0}$$
$$C_1 = -(V_{gs} - V_{TH0})E_cL$$

By solving equation (3–12), the intrinsic saturation voltage V_{dsat} can be obtained as:

$$V_{dsat} = \frac{-B_1 + \sqrt{B_1^2 - 4A_1C_1}}{2A_1}. \tag{3–13}$$

Substituting equation (3–13) into equation (3–11), the saturation current I_{DSAT} can be obtained. Then, the extrinsic saturation voltage V_{DSAT} can be also determined by putting I_{DSAT} into equation (3–7).

(b) Channel Length Modulation Effect

As the drain bias is increased beyond the saturation voltage, the pinch–off point of the inversion layer will move toward to the source junction and result in the shortening of the effective conducting path of inversion carriers in the channel region. This channel length modulation effect would cause the drain current to increase with respect to the drain voltage in the saturation region,

especially for short channel devices. The drain current in the saturation region can be expressed as:

$$I_{DS}=\frac{WC_{fox}\mu_n\left[V_{gs}-\left(V_{TH0}+KV_{dsat}\right)-\frac{1}{2}V_{dsat}\right]V_{dsat}}{\left(L-\Delta L_3\right)\cdot\left\{1+\frac{\alpha C_{fox}}{2\varepsilon_{si}}\left[V_{gs}+V_{TH}-2\left(V_{FB}^{f}+\phi_{f,inv}\right)-\frac{1}{2}V_{dsat}\right]+\left(\eta+\frac{\beta}{L-\Delta L_3}\right)\cdot V_{dsat}\right\}} \tag{3–14}$$

where ΔL_3 is the channel length modulation factor in the channel region, which can be calculated by using a pseudo–two–dimensional approximation method [39] and given as below. As shown in Figure 3–1, it is assumed that the channel current is uniformly distributed within the depths of d and t_{si} for the channel and drain edges, respectively. By applying the Gauss's law to the rectangular boxes indicated in the dashed lines (1)–(4) for both the channel and drain edges, and differentiating the integrals with respect to x, we obtain the following equations for the channel and drain regions:

$$\begin{aligned}
&-\frac{C_{fox}}{\varepsilon_{si}}\left[V_{gs}^{'}-\phi_{f,inv}-V(x)\right]-t_{si}\frac{d^2V(x)}{d^2x}-\frac{C_{box}}{\varepsilon_{si}}\left[V_{bs}^{'}-V^{'}(x)\right]=-\frac{\left[qN_Bt_{si}+Q_m\right]}{\varepsilon_{si}}\\
&-\frac{C_{fox}}{\varepsilon_{si}}\left[V_{gs}^{'}-\phi_{f,inv}-V(x)\right]-t_{si}\frac{d^2V(x)}{d^2x}-\frac{C_{box}}{\varepsilon_{si}}\left[V_{bs}^{'}-V_{bi}-V_{ds}\right]=\frac{\left[qN_Dt_{si}-Q_m\right]}{\varepsilon_{si}}
\end{aligned} \tag{3–15}$$

where $V(x)$ ($V'(x)$) is the surface potential along the front (back) channel in the pinch–off region, $V_{gs}^{'}=V_{gs}-V_{FB}^{f}$, C_{box} is the back gate capacitance per– unit area, N_D is the doping concentration in the drain region, and Q_m is the mobility charge density, which can be approximated by $2I_{DSAT}/W\mu_nE_c$. Then, by assuming

$$\frac{C_{box}}{\varepsilon_{si}}\left[V_{bs}^{'}-V^{'}(x)\right]\cong\frac{1}{2}\left[\frac{qN_B\left(t_{si}-d\right)}{\varepsilon_{si}}-\frac{C_{box}}{\varepsilon_{si}}\left(V_{bs}^{'}-V_{bi}-V_{ds}\right)\right], \tag{3–16}$$

and using several mathematical manipulations, equation (3–15) can be further simplified as:

$$\frac{d^2V(x)}{dx^2}-\theta^2V(x)=-\theta^2(G_1+V_{dsat}),\qquad -\Delta L_3<x<0$$
$$\frac{d^2V(x)}{dx^2}-\theta^2V(x)=-\theta^2(G_2+V_{ds}),\qquad 0<x<\Delta L_4 \tag{3–17}$$

where $\theta^2=C_{fox}/(\varepsilon_{si}t_{si})$, d is the thickness of the channel inversion layer and can be obtained by $d=k_BT\varepsilon_{si}/(q|Q_B|)$, the bulk depletion charge density Q_B can be expressed by $Q_B=qN_Bt_{si}$, and

$$G_1=V_{gs}^{'}-\phi_{f.inv}-\frac{qN_Bt_{si}}{C_{fox}}-\frac{Q_m}{C_{fox}}+\frac{1}{2}\left[\frac{qN_B(t_{si}-d)}{C_{fox}}-\frac{C_{box}}{C_{fox}}\left(V_{bs}^{'}-V_{bi}-V_{ds}\right)\right]-V_{dsat},$$
$$G_2=V_{gs}^{'}-\phi_{f.inv}-\frac{qN_Dt_{si}}{C_{fox}}-\frac{Q_m}{C_{fox}}+\frac{C_{box}}{C_{fox}}\left(V_{bs}^{'}-V_{bi}-V_{ds}\right)-V_{ds}.$$

By applying the following boundary conditions:

$$V(-\Delta L_3)=V_{dsat},\quad \left(\frac{dV}{dx}\right)_{x=-\Delta L_3}=E_c,$$
$$V(0^-)=V(0^+),\quad \left(\frac{dV}{dx}\right)_{x=-\Delta L_3}=\left(\frac{dV}{dx}\right)_{x=\Delta L_4},$$
$$V(\Delta L_4)=V_{ds},\quad \left(\frac{dV}{dx}\right)_{x=\Delta L_4}=E_c,$$

we can obtain the solutions of equation (3–17) and expressed as:

$$V(x)=E_1\exp(\theta\cdot x)+F_1\exp(-\theta\cdot x)+G_1+V_{dsat},\qquad -\Delta L_3<x<0$$
$$V(x)=E_2\exp(\theta\cdot x)+F_2\exp(-\theta\cdot x)+G_2+V_{ds},\qquad 0<x<\Delta L_4 \tag{3–18}$$

where

$$E_1=Q_{a1}\exp(\theta\Delta L_3),\quad Q_{a1}=\frac{1}{2}\left(-G_1+\frac{E_c}{\theta}\right),$$
$$F_1=Q_{b1}\exp(-\theta\Delta L_3),\quad Q_{b1}=\frac{1}{2}\left(-G_1-\frac{E_c}{\theta}\right),$$
$$E_2=Q_{a2}\exp(-\theta\Delta L_4),\quad Q_{a2}=\frac{1}{2}\left(-G_2+\frac{E_c}{\theta}\right),$$
$$F_2=Q_{b2}\exp(\theta\Delta L_4),\quad Q_{b2}=\frac{1}{2}\left(-G_2-\frac{E_c}{\theta}\right).$$

Using several mathematical manipulations, the following relation can be obtained:

$$A_{n0} = E_1 + F_1 = Q_{a1}\exp(\theta \cdot \Delta L_3) + Q_{b1}\exp(-\theta \cdot \Delta L_3)$$
$$= \frac{2}{Q_b}(Q_{a1}Q_{b1} - Q_{a2}Q_{b2}) + \frac{Q_b}{2} \tag{3–19}$$

where $Q_b = G_2 + V_{ds} - G_1 - V_{dsat}$. From equation (3–19), the channel length modulation factor can be expressed as explicitly:

$$\Delta L_3 = \frac{1}{\theta}\ln\left[\frac{A_{n0} + \sqrt{A_{n0}^2 - 4Q_{a1}Q_{b1}}}{2Q_{a1}}\right]. \tag{3–20}$$

It is noted that ΔL_3 can be obtained analytically without any iteration and is equal to zero at the onset of the saturation condition.

(c) Drain Current in Saturation Region

By applying equations (3–20) and (3–7) into equation (3–14), the drain current in the saturation region can be expressed as:

$$I_{DS} = \frac{-B_2 + \sqrt{B_2^2 - 4A_2C_2}}{2A_2} \tag{3–21}$$

where

$$A_2 = -\frac{\alpha C_{fox}}{2\varepsilon_{si}}R_S$$

$$B_2 = 1 + \frac{\alpha C_{fox}}{2\varepsilon_{si}}\left[V_{GS} + V_{TH0} - 2\left(V_{FB}^f + \phi_{f,inv}\right) - \left(K + \frac{1}{2}\right)V_{dsat}\right] + \left(\eta + \frac{\beta}{L - \Delta L_3}\right)V_{dsat}$$
$$+ \frac{\mu_n C_{fox} W}{L - \Delta L_3}R_S V_{dsat}$$

$$C_2 = -\frac{\mu_n C_{fox} W}{L - \Delta L_3}\left[V_{GS} - V_{TH0} - \left(\frac{1}{2} - K\right)V_{dsat}\right]V_{dsat}$$

It is noted that the drain current is continuous at the transition between the linear and saturation regions without adding additional smooth function to improve the continuity.

3–2.2.3 I–V Characteristics in Subthreshold Region ($V_{gs} < V_{TH}$)

Since the injection minority carrier concentration from the source region is smaller than the doping concentration in the Si film, the subthreshold current of the SOI MOS transistor is mainly contributed by the diffusion of the minority carriers injected from the source edge. Due to the fact that the diffusion length of the minority carriers in the surface channel is much longer than the channel length, the I–V characteristics in the subthreshold region can be expressed as:

$$I_{subth} = \frac{W}{L} I_0(\phi_{sf}) \left[1 - \exp\left(-\frac{qV_{ds}}{k_B T} \right) \right] \tag{3–22}$$

where

$$I_0(\phi_{sf}) = qD_n \frac{k_B T}{q} \frac{\varepsilon_{si}}{C_{fox}\left(V_{gs} - V_{FB}^f - \phi_{sf}\right)} \frac{n_i^2}{N_B} \exp\left(\frac{q\phi_{sf}}{k_B T} \right),$$

D_n is the carrier diffusivity and ϕ_{sf} is the surface band–bending with respect to the source potential. The surface potential ϕ_{sf} can be analytically expressed in terms of external biases as shown in ref. [30]. However, the solution is not explicit to V_{gs}. For the purpose of efficient circuit analysis, it would be preferable that the current equation can be expressed in terms of external voltage as well as the surface potential ϕ_{sf} expressed in terms of V_{gs}. Therefore, the Taylor's series expansion method is utilized around the central bias of the weak inversion to meet this purpose. If the surface band–bending is equal to $0.8\phi_{f,inv}$, denoted as ϕ_{sf0}, the first order expression of V_{gs} can be obtained as

$$V_{gs} = V_{gs0} + (\phi_{sf} - \phi_{sf0}) \cdot n \tag{3–23}$$

where

$$V_{gs0} = V_{gs}\big|_{\phi_{sf}=\phi_{sf0}},$$

$$n = \frac{\partial}{\partial \phi_{sf}} \left(V_{gs}\big|_{\phi_{sf}=\phi_{sf0}} \right) = 1 + \frac{1}{C_{fox}} \left(\frac{1}{C_{si}} + \frac{1}{C_{box}} \right)^{-1}.$$

From equations (3–22) and (3–23), we obtain:

$$I_{subth} = \frac{W}{L} I_0(\phi_{sf0}) \exp\left(\frac{q(V_{gs} - V_{gs0})}{nk_BT}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_BT}\right)\right]. \tag{3–24}$$

It is obvious that the above formula of the subthreshold current would be inaccurate when the gate bias is increased near or beyond the threshold voltage, since the minority carrier density has exceeded the channel doping concentration. Therefore, the following approximation is taken for the channel inversion carrier concentration n_{ch} [41]:

$$n_{ch} = \left(\frac{1}{n_{sf}} + \frac{1}{n_x}\right)^{-1}, \tag{3–25}$$

$$n_{sf} = n_{gs0} \exp\left[\frac{q(V_{gs} - V_{gs0})}{nk_BT}\right] \tag{3–26}$$

where n_{gs0} is the inversion carrier concentration at $V_{gs} = V_{gs0}$, and n_x is the inversion carrier concentration for $V_{gs} > V_{gs0}$. Substituting equation (3–26) into equation (3–25), the channel inversion carrier concentration can be expressed as:

$$n_{ch} = n_{gs0} \exp\left[\frac{q(V_{gs} - V_{gs0})}{nk_BT}\right]\left(\frac{1}{1 + \delta \exp\left(\frac{q(V_{gs} - V_{gs0})}{nk_BT}\right)}\right), \tag{3–27}$$

where $\delta = n_{gs0}/n_x << 1$.

Then, the diffusion current in the subthreshold region can be obtained as:

$$I_{subth} = \frac{W}{L} I_0(\phi_{sf0}) \exp\left(\frac{q(V_{gs} - V_{gs0} - KV_{ds})}{nk_BT}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_BT}\right)\right]\left(\frac{1}{1 + \delta \exp\left(\frac{q(V_{gs} - V_{gs0})}{nk_BT}\right)}\right). \tag{3–28}$$

Since the channel conduction current is contributed by the diffusion current I_{subth} and the drift current I_{DS}, the total current is therefore simply expressed as:

$$I_{DS,T} = I_{DS} + I_{subth}. \tag{3–29}$$

It is noted that the channel resistance is much larger than the parasitic source/drain resistances. So, the intrinsic gate– and drain–to–source voltages V_{gs} and V_{ds}, respectively, are almost equal to the external voltages V_{GS} and V_{DS}. Therefore, equation (3–28) can be expressed in terms of terminal voltages.

3–2.2.4 Impact–Ionization Effect and Parasitic Bipolar Junction Transistor (BJT)

As the MOS devices operated in the saturation region, the longitudinal electric field in the pinch–off region near the drain junction is increased significantly with the drain voltage. The channel conducting carriers drifting into the pinch–off region collide with the lattice, resulting in the generations of the electron and hole pairs. The generated electrons and holes move in the opposite directions as a result of the electric field. The electrons move toward the drain region and the holes move toward the source junction. Thus, it results in the extra electron and hole currents, the impact ionization current. Additionally, for a SOI MOS transistor with the very short channel, the current conduction within the parasitic BJT with its emitter at the source and its collector at the drain above the buried oxide cannot be overlooked. This is because that a portion of the hole current due to the impact ionization effect is directed vertically toward the buried oxide owing to the transverse electric field. As a result, in the area above the buried oxide in the Si film, an accumulation of the holes exists, which may lead to an activation of the parasitic bipolar junction transistor above the buried oxide.

Thus, in the drain current model, the effects of the impact ionization and parasitic BJT should

be included [42]

$$I_D = G \cdot I_{DS,T} + H \cdot I_{CBO}, \tag{3–30}$$

where

$$G = 1 + \frac{(M-1)\left(1-(1-K_1)\alpha_0\right)}{1-\left(1+K_1 \cdot K_1^{'}(M-1)\right)\alpha_0}$$
$$H = \frac{1+K_1^{'}(M-1)}{1-\left(1+K_1 \cdot K_1^{'}(M-1)\right)\alpha_0} \quad ,$$
$$M = \alpha_i E_{\max} \exp\left(-\frac{\beta_i}{E_{\max}}\right) + 1$$

I_{CBO} is the collector–base leakage current in the parasitic BJT with the emitter–base open in the FD SOI MOS device, K_1 and $K_1^{'}$ are used to account for the mechanism of the impact ionization hole current and the collector current in the parasitic BJT, M is the impact ionization factor, α_i and β_i are the ionization parameters, and E_{max} is the maximum longitudinal electric field and can be determined from equation (3–18). By setting x equal to zero, the maximum longitudinal electric field E_{max} that is the derivative of equation (3–18) with respect to x, can be expressed as

$$E_{\max} = \theta \cdot (E_1 - F_1). \tag{3–31}$$

3–2.3 Temperature Rise Model and Temperature Dependent Parameters

The relationship of the power dissipation in the channel and the difference between the operating temperature and ambient temperature can be described by the following equation [34]:

$$T_l - T_0 = R_{th} \cdot P = R_{th} \cdot I_D \cdot V_{DS}, \tag{3–32}$$

where T_l and T_0 are the new operating temperature and ambient (room) temperature, respectively, P is the device power dissipation and expressed as $P = I_D V_{DS}$, and R_{th} is the thermal resistance. Here, the thermal resistance R_{th} is given by

$$R_{th} = \frac{1}{2W}\left(\frac{t_{box}}{k_{ox}k_{si}t_{si}}\right)^{\frac{1}{2}}, \tag{3–33}$$

where W is the channel width of the device, t_{box} and t_{si} are the thicknesses of the buried oxide and Si film, respectively, and k_{ox} and k_{si} are the thermal conductivities of the oxide and silicon, respectively. Similar to the ref [37], by using the Taylor's series expansion, we can obtain

$$I_D \approx I_D^0 + A_W\left(T_l - T_0\right), \tag{3–34}$$

where I_D^0 is the drain current without including the lattice temperature, and

$$A_W = \left.\frac{\partial I_D}{\partial\left(T_l - T_0\right)}\right|_{(T_l = T_0)}.$$

From equations (3–32) and (3–34), the following equation can be obtained:

$$T_l = T_0 + \frac{I_D^0}{1/\left(R_{th}V_{DS}\right) - A_W}. \tag{3–35}$$

To determine the influence of the SHE on the characteristics of SOI MOS devices, the temperature dependencies of the physical parameters are needed to be considered. These important parameters included in the present analysis are the threshold voltage V_{TH}, the mobility μ_n, and the impact ionization parameter β_i. The dependence on the temperature of these parameters is well known in the refs. [43–45].

The variation of the threshold voltage with temperature can be described reasonably well by the following empirical linear relationship [43]:

$$V_{TH}\left(T_l\right) = V_{TH}\left(T_0\right) - K_2\left(T_l - T_0\right), \tag{3–36}$$

where $V_{TH}(T_l)$ and $V_{TH}(T_0)$ are the threshold voltages at temperatures T_l and T_0, respectively, and K_2 is the empirical temperature constant of the threshold voltage.

The temperature dependence of the maximum low field mobility μ_n can be modelled by [44]:

$$\mu_n(T_l) = \mu_n(T_0) \cdot \left(\frac{T_0}{T_l} \right)^{K_3}, \tag{3–37}$$

where $\mu_n(T_l)$ and $\mu_n(T_0)$ are the low filed mobility at temperatures T_l and T_0, respectively, and K_3 is the empirical temperature constant of the low filed mobility.

Since several authors have shown that the temperature dependence of the impact ionization factor M is dominated by that of β_i, we consider α_i to be independent of temperature and use the following expression for β_i [45]:

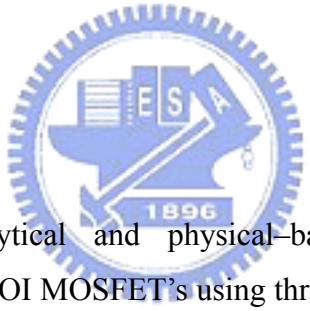
$$\beta_i(T_l) = \beta_i(T_0) + K_4(T_l - T_0), \tag{3–38}$$

where $\beta_i(T_l)$ and $\beta_i(T_0)$ are the impact ionization parameters at temperatures T_l and T_0, respectively, and K_4 is the empirical temperature constant of the impact ionization parameter. It is noted that K_2, K_3 and K_4 are the temperature relevant constants and can be extracted from the experiments. In the simulation, the drain current without the rise of the lattice temperature is calculated first, and then the lattice temperature T_l is obtained by using equation (3–35). Finally, the determined T_l is substituted to equations (3–36)–(3–38) to obtain the temperature–dependent parameters, and then the drain current can be calculated.

3–3 Verifications and Discussion

In this section, the present drain current model is verified with the 2–D numerical device simulator Medici [32] and experimental data for the SOI devices with different front gate oxide thicknesses, silicon film thicknesses, buried oxide thicknesses and geometries. Figure 3–2 shows the comparisons of the calculated drain currents with the experimental data as a function of gate voltage for SOI MOS devices with different channel lengths, back gate biases and drain biases. It is clearly seen that a close agreement is obtained between the results obtained by the present I–V

model and experimental data in the above–threshold regions of devices operation. Figure 3–3 emphasizes the subthreshold regime of operation for the devices with different channel lengths, back gate biases and drain biases. It shows a good agreement between the measured data and simulation results. Figure 3–4 shows the comparisons of the experimental dc output characteristics obtained from several fully depleted SOI MOSFET devices with the results obtained by the present model. It is seen that with the SHE in the model, an excellent agreement is found for all devices. On the other hand, the results predicted by the model excluding SHE show the significant deviations from the experimental data at large drain current and bias level. The large deviations of the drain current may result in significant error in the prediction of the drain conductance that plays an important role in the circuit design, especially in the analog circuit design. Therefore, the negative differential resistance in saturation region resulting from the SHE should be carefully considered. The fitting parameters of a SOI MOS transistor with L = 0.28 μm are given in Table 5. Likewise, in Figs. 3–5 and 3–6, we demonstrate a satisfying correspondence between the experimental data and modelled results in cases where SHE significantly influences the output characteristics of the SOI MOS devices.



3–4 Conclusions

We have proposed an analytical and physical–based threshold voltage model for deep–submicrometer fully depleted SOI MOSFET's using three–zone Green's function technique to solve the 2–D Poisson's equation and adopting a new concept of the average electric field to avoid the iterations in solving the position of the minimum surface potential and to obtain a closed expression of the threshold voltage. The derived threshold voltage model is further linearized to obtain the drain–induced barrier–lowering factor with respect to the drain bias and incorporated into the derivation of the analytical I–V model. A complete analytical drain current model for the deep submicrometer SOI MOSFETs is presented to account for the effects of the parasitic series resistances, drain–induced barrier–lowering, channel length modulation, self–heating, impact ionization and parasitic bipolar junction transistor. Good agreements among the measured data, 2–D numerical analysis and the calculated results have demonstrated that the present threshold voltage model is accurate and reliable. Additionally, the calculated I–V characteristics in the below– and above–threshold regions are compared with the experimental data and excellent agreements are obtained. These verify the applicability of the developed threshold voltage model and I–V model in the device design and computer–aided circuit simulation for SOI MOSFETs in VLSI integrated circuits.

Chapter 4

New 2–D Models for Threshold Voltage and Subthreshold Current of Fully–Depleted Short–Channel SOI MOSFETs With Halo or Pocket Implants

4–1 Introduction

Thin film, fully depleted silicon–on–insulator (FD SOI) CMOS has been becoming another major technology for the next generation of VLSI [50–52]. This is because that the FD–SOI CMOS transistors provide superior electrical characteristics over the bulk MOS devices such as reduced source/drain junction capacitances, increased carrier mobility, suppressed short channel effect, improved subthreshold slope and improved latchup immunity [53]. To keep with the progress in the process technology, the SOI MOS devices have been continuously scaled down, pushing the CMOS technology into the deep–submicrometer regime. However, as the gate lengths of MOSFETs keep shrinking, we observe the short–channel effects such as the serious threshold voltage roll–off due to the increased charge–sharing between the source/drain regions and channel, the increased off–state leakage current due to the higher sensitivity of the source/channel barrier to the drain bias or drain–induced barrier lowering (DIBL), and lower bulk punchthrough voltage. Therefore, the study of the short–channel effects has become a significant role for the down–scaling of the CMOS technology. Recently, lateral channel engineering utilizing halo or pocket implants [54–57] surrounding the drain and source regions in short–channel MOSFETs are proposed to suppress such short–channel effects.

In order to correctly predict the short–channel effects, solving the two–dimensional (2–D) Poisson's equation for the surface potential in the channel depletion region of SOI MOSFETs is a very important step. The analytical modeling of the threshold voltage of FD–SOI MOSFETs has

already been performed by numerous authors [27–30, 58 and 59]. Veeraraghavan and Fossum [28] used a conventional charge–sharing scheme to develop the threshold–voltage model for the I–V characteristics. Young [27] and Pidin [58] utilized a parabolic–like potential distribution for the 2–D Poisson's equation and developed an analytical model for the drain–induced barrier lowering. In a work by Woo [29], the 2–D Poisson's equation was separated into a 1–D Poisson's equation and a 2–D Laplace equation. In a paper by Guo [30], a full 2–D analytical solution of the 2–D Poisson's equation by means of the Green's function technique was reported. However, these analytical models are not able to take into account the effect of halo or pocket implants for SOI MOSFETs. In the paper by Meer [59], an analytical threshold voltage model of SOI MOSFETs accounting for the halo implants was developed based on the three–zones Green's function solution technique. Although a closed form of the threshold voltage is derived, it involves the infinite Fourier series terms and the calculation is too complicated to be further implemented in the derivation of the I–V model for a simulator like SPICE.

In this Chapter, we present an analytical model for characterizing the DIBL, the threshold voltage and subthreshold current of the short–channel FD–SOI MOSFETs with halo or pocket implants in the thin silicon film. The potential distribution function is approximated by a cubic function and consequently the front/bottom potential functions at the active/oxide layer interfaces have been obtained by solving the 2–D Poisson's equation with the appropriate boundary conditions and described in Section 4–2. The subthreshold surface potential model is suitable for FD–SOI MOSFETs with halo implants or uniformly doped profile in the silicon film. The front surface potential is used to monitor the DIBL in the short–channel SOI MOSFETs. Analytical expressions for the threshold voltage and subthreshold current of the MOS device including the short channel effects have been derived considering a wide range of device parameters and presented in Sections 4–3 and 4–4, respectively. The calculated results of the subthreshold surface potential distribution, threshold voltage and subthreshold current for both deep–submicrometer and long–channel halo MOSFETs have been compared with the simulation ones obtained by using the Medici device

simulation software [32] and shown in Section 4–5. Conclusions are summarized in the final section.

4–2 Two–Dimensional Subthreshold Surface Potential Model

The schematic cross–sectional view of a fully depleted SOI MOSFET under consideration is shown in Fig. 4–1, where L is the length of the channel region, L_1 is the length of the halo region, and t_f, t_{si} and t_b are the thicknesses of the front gate oxide, silicon film and bottom oxide, respectively, and the gate, source and drain regions are made of n^+–type polycrystalline silicon. The potential distribution function for the short–channel device may be obtained by solving the 2–D Poisson's equation in the silicon film. Assuming that the impurity density in the channel region is uniform, and the influence of charge carriers and fixed oxide charges on the electrostatics of the channel region can be neglected, the 2–D potential distribution $\Psi(x, y)$ in the silicon film can be obtained by solving the following Poisson's equation, before the onset of strong inversion:

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=-\frac{\rho(x,y)}{\varepsilon_{si}} \qquad 0\le x\le L,\ \ 0\le y\le t_{si} \tag{4–1}$$

where $\rho(x, y)$ is the 2–D charge density in the silicon film and ε_{si} is the permittivity of the silicon film. In the following analysis, the uniformly doped channel and halo are assumed for simplicity. Consequently, the 2–D doping profile $N_{si}(x, y)$ in the silicon film for long channel FD–SOI MOSFETs with halos, where the halo length L_1 is smaller than $L/2$, can be defined as follows:

$$N_{si}(x,y)=\begin{cases} N_A & 0\le x\le L_1 \\ N_B & L_1\le x\le L_2 \\ N_A & L_2\le x\le L \end{cases} \tag{4–2}$$

while for short–channel devices, where the halo length L_1 is greater than $L/2$ and less than L, the 2–D doping profile can be defined as:

$$N_{si}(x,y)=\begin{cases} N_A & 0 \le x \le L-L_1 \\ 2N_A - N_B & L-L_1 \le x \le L_1 \\ N_A & L_1 \le x \le L \end{cases} \tag{4–3}$$

where L_1 is the length of the halo region, and N_A and N_B are the doping concentration in the halo and channel regions, respectively. Figure 4–2 shows the schematic diagrams and the doping profiles of FD–SOI MOS transistors with halo as function of gate length. From this figure, it is seen that based on the definitions in eqs. (4–2) and (4–3), there are four different 2–D doping distributions present in the silicon film. Besides, it is also seen that the doping concentration in the channel region increases as the gate length decreases due to overlapping the halo regions [60], [61].

In the silicon film, the potential profile in the vertical direction, i.e., the y–dependence of $\Psi(x, y)$ can be approximated by a simple parabolic function as considered in [27] and [58] for the FD–SOI MOSFETs and may be given as:

$$\Psi(x,y)=\Psi_s(x)+c_1(x)y+c_2(x)y^2+c_3(x)y^3 \tag{4–4}$$

where $\Psi_s(x)$ is the surface potential and the arbitrary coefficients $c_1(x)$, $c_2(x)$ and $c_3(x)$ are the functions of x. In the MOS devices with halo implants, since the doping distribution in the silicon film is divided into three parts, i.e., for the case in Fig. 4–2(a), the potential functions in the channel and halo regions can be written as:

$$\Psi_i(x,y)=\Psi_{s,i}(x)+c_{i1}(x)y+c_{i2}(x)y^2+c_{i3}(x)y^3, \quad \begin{cases} i=1, & 0 \le x \le L_1, & 0 \le y \le t_{si} \\ i=2, & L_1 \le x \le L_2, & 0 \le y \le t_{si} \\ i=3, & L_2 \le x \le L, & 0 \le y \le t_{si} \end{cases} \tag{4–5}$$

where $\Psi_i(x, y)$ and $\Psi_{s,i}(x, y)$ indicate the potential function and the surface potential in the region i,

respectively. From the energy band diagram in Fig. 4–3 of the SOI MOS structure in Fig. 4–1, the surface potential is $\Psi_s \equiv [E_i(0) - E_f]/(-q)$ and the band bending at the silicon surface is $\phi_s \equiv [E_i(0) - E_i(\infty)]/(-q)$, where E_f is the extrinsic Fermi level of the silicon, and $E_i(0)$ and $E_i(\infty)$ are the intrinsic Fermi levels at the surface of the silicon and in the silicon bulk, respectively. Then, we have the relation $\Psi_s(x) = \phi_s(x) - \Psi_{FP}(x)$ between $\Psi_s(x)$ and $\phi_s(x)$ at the front surface of the silicon film, where $\Psi_{FP}(x) = V_T \ln[N(x)/n_i]$, $V_T = kT/q$ is the thermal voltage, and $N(x)$ and n_i are the doping concentration in the silicon film and intrinsic carrier concentration of silicon, respectively.

The Poisson's equation is solved separately in the channel and halo regions using the following boundary conditions.

1) The electric flux at the front gate oxide/silicon film interface is continuous for each region i and can be given as:

$$\left.\frac{\partial \Psi_i(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Psi_{fs,i}(x) - V'_{GS,i}}{t_f} \tag{4–6}$$

where $\Psi_{fs,i}(x) = \Psi_{s,i}(x, 0)$ is the front surface potential along the channel length in the region i, ε_{ox} is the permittivity of the oxide, t_f is the thickness of the front gate oxide, and

$$V'_{GS,i} = V_{GS} - V_{fbf,i} - \Psi_{FP,i}$$

where V_{GS} is the gate–to–source bias voltage, $V_{fbf,i}$ is the front–channel flatband voltage in the region i, and $\Psi_{FP,i}$ is the difference between the extrinsic Fermi level and the intrinsic Fermi level in the region i and can be expressed as

$$\begin{aligned} \Psi_{FP,1} &= \Psi_{FP,3} = V_T \ln(N_A/n_i) \\ \Psi_{FP,2} &= V_T \ln(N_B/n_i). \end{aligned} \tag{4–7}$$

2) The electric flux at the bottom oxide/silicon film interface is continuous for each region i and can be given as:

$$\left.\frac{\partial \Psi_i(x,y)}{\partial y}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{SUB,i} - \Psi_{bs,i}(x)}{t_b} \tag{4–8}$$

where $\Psi_{bs,i}(x) = \Psi_{s,i}(x, t_{si})$ is the back surface potential along the channel length in the region i, t_b is the thickness of the bottom oxide, and

$$V'_{SUB,i} = V_{SUB} - V_{fbb,i} - \Psi_{FP,i}$$

where V_{SUB} is the substrate–to–source bias voltage, and $V_{fbb,i}$ is the back–channel flatband voltage in the region i.

3) The surface potential at the interface of the different regions is continuous

$$\begin{aligned} \Psi_1(L_1, y) &= \Psi_2(L_1, y) \\ \Psi_2(L_2, y) &= \Psi_3(L_2, y) \end{aligned} \tag{4–9}$$

4) The Electric flux at the interface of the different regions is continuous

$$\begin{aligned} \left.\frac{\partial \Psi_1(x,y)}{\partial x}\right|_{x=L_1} &= \left.\frac{\partial \Psi_2(x,y)}{\partial x}\right|_{x=L_1} \\ \left.\frac{\partial \Psi_2(x,y)}{\partial x}\right|_{x=L_2} &= \left.\frac{\partial \Psi_3(x,y)}{\partial x}\right|_{x=L_2} \end{aligned} \tag{4–10}$$

5) The potential at the source end is

$$\Psi_1(0,0) = \Psi_{fs,1}(0) = V_{bi}. \tag{4–11}$$

6) The potential at the drain end is

$$\Psi_1(L,0) = \Psi_{fs,3}(L) = V_{bi} + V_{DS}. \tag{4–12}$$

where $V_{bi} = \Psi_{\text{npoly}} \approx E_g/(2q)$ is the built–in potential across the body–source junction, and V_{DS} is the drain–to–source bias voltage.

The constants $c_{i1}(x)$, $c_{i2}(x)$ and $c_{i3}(x)$ in eq. (4–5) can be deduced from the boundary conditions (4–6)–(4–8) and are given as:

$$\begin{aligned} c_{i1}(x) &= \frac{C_f}{\varepsilon_{si}} \cdot \left(\Psi_{fs,i} - V'_{GS,i}\right), \\ c_{i2}(x) &= \frac{1}{t_{si}^2} \cdot \left[-\left(3 + \frac{2C_f}{C_{si}}\right) \cdot \Psi_{fs,i} + \left(3 + \frac{C_b}{C_{si}}\right) \cdot \Psi_{bs,i} - \frac{C_b}{C_{si}} \cdot V'_{SUB,i} + \frac{2C_f}{C_{si}} \cdot V'_{GS,i} \right], \\ c_{i3}(x) &= \frac{1}{t_{si}^3} \cdot \left[\left(2 + \frac{C_f}{C_{si}}\right) \cdot \Psi_{fs,i} - \left(2 + \frac{C_b}{C_{si}}\right) \cdot \Psi_{bs,i} + \frac{C_b}{C_{si}} \cdot V'_{SUB,i} - \frac{C_f}{C_{si}} \cdot V'_{GS,i} \right]. \end{aligned}$$

(4–13)

where $C_{si} = \varepsilon_{si}/t_{si}$, $C_f = \varepsilon_{ox}/t_f$ and $C_b = \varepsilon_{ox}/t_b$ are the silicon film, front gate oxide, and bottom oxide capacitances, respectively. Substituting $\Psi_i(x, y)$ from eq. (4–5) in eq. (4–1), and using the expressions of $c_{i1}(x)$, $c_{i2}(x)$ and $c_{i3}(x)$ in eq. (4–13), the front surface and bottom surface potentials in the region i, $\Psi_{fs,i}(x)$ and $\Psi_{bs,i}(x)$ can be expressed in terms of second–order nonhomogenous differential equations given by

$$\begin{aligned}
&\frac{\partial^2 \Psi_{fs,i}(x)}{\partial x^2} + A_i \Psi_{fs,i}(x) + B_i \Psi_{bs,i}(x) = C_i \\
&\frac{\partial^2 \Psi_{bs,i}(x)}{\partial x^2} + F_i \Psi_{fs,i}(x) + G_i \Psi_{bs,i}(x) = H_i .
\end{aligned} \tag{4–14}$$

where the expressions of the coefficients A_i, B_i, C_i, F_i, G_i, and H_i are given in Appendix A. According to [62], the analytical solution of the above differential equations can be obtained in the form

$$\begin{aligned}
\Psi_{fs,i}(x) &= \Psi_{fsp,i} + a_{i1} \cdot g_1 \cdot e^{d_1 x} + a_{i2} \cdot g_1 \cdot e^{-d_1 x} + a_{i3} \cdot g_2 \cdot e^{d_2 x} + a_{i4} \cdot g_2 \cdot e^{-d_2 x}, \\
\Psi_{bs,i}(x) &= \Psi_{bsp,i} + a_{i1} \cdot e^{d_1 x} + a_{i2} \cdot e^{-d_1 x} + a_{i3} \cdot e^{d_2 x} + a_{i4} \cdot e^{-d_2 x}.
\end{aligned} \tag{4–15}$$

where the particular solutions $\Psi_{fsp,i}(x)$ and $\Psi_{bsp,i}(x)$, and the constants g_1, g_2, d_1 and d_2 are given in the Appendix B. By using the boundary conditions (4–9)–(4–12), we can obtain the expressions of the coefficients a_{i1}, a_{i2}, a_{i3} and a_{i4} as shown in the Appendix C.

4–3 Two–Dimensional Threshold Voltage Model

In general, for MOS devices with uniform channel doping concentration, the threshold voltage is defined as the gate–to–source voltage at which the minimum surface potential is Ψ_{FP} and expressed as

$$V_{TH} = V_{GS} \quad @ \quad \Psi(x_{\min}, 0) = \Psi_{FP} \tag{4–16}$$

i.e.

$$V_{TH} = V_{GS} \quad @ \quad \phi(x_{\min},0) = 2\Psi_{FP}. \tag{4–17}$$

where x_{min} is the lateral position along the channel region with minimum front surface potential $\Psi_{fs}(x_{min})$ in the channel. In the SOI MOS devices with halo or pocket implants, since the doping concentration is different in the channel and halo regions, the value of the Fermi potential depends on the lateral location within the silicon film. Consequently, the threshold voltages in the halo and channel regions, $V_{TH,1}$ and $V_{TH,2}$, respectively, are defined as:

$$\begin{aligned} V_{TH,1} &= V_{GS} \quad @ \quad \Psi_{fs,1}(x_{\min,1}) = \Psi_{FP,1} \\ V_{TH,2} &= V_{GS} \quad @ \quad \Psi_{fs,2}(x_{\min,2}) = \Psi_{FP,2}. \end{aligned} \tag{4–18}$$

where $x_{min,1}$ and $x_{min,2}$ are the lateral positions of the minimum surface potentials in the halo and channel regions, respectively. Then, the threshold voltage of the FD–SOI MOSFET is defined by the maximum of these two voltages

$$V_{TH} = \max\{V_{TH,1}, V_{TH,2}\} \tag{4–19}$$

Equation (4–19) ensures the 2–D analytical model to calculate a threshold voltage for which the front gate/silicon interface of FD–SOI MOS transistor is just inverted.

Next, the positions of the minimum surface potentials $x_{min,1}$ and $x_{min,2}$ can be obtained by differentiating eq. (4–5) with respect to x at $y = 0$, and solved by

$$\left.\frac{\partial\Psi(x,y)}{\partial x}\right|_{y=0} = 0. \tag{4–20}$$

Note that due to three regions of the device, i.e., for the case in Fig. 4–2(a), there are three values of x_{min} in the solutions of eq. (4–20). However, since the drain–to–source bias voltage V_{DS} is positive for an n–MOS device, the lateral position of the minimum potential $x_{min,1}$ will always be located near by the source region. Therefore, only the channel and halo region near by the source side needed to be considered.

It may be observed that the closed form solution of the lateral position of the minimum surface potential x_{min} is not possible in this case. However, for different values of V_{GS} and V_{DS}, x_{min} may be obtained by solving eq. (4–20) numerically. Consequently, it is clear that explicit expressions for both the threshold voltages $V_{TH,1}$ and $V_{TH,2}$ can be deduced from eq. (4–15) by replacing V_{GS} and $\Psi_{fs,i}$ by $V_{TH,i}$ and $\Psi_{FP,i}$, respectively, where i = 1 or 2, and expressed as:

$$V_{TH,1} = \frac{\Psi_{FP,1} - \gamma_2 \cdot V_{SUB} - \gamma_3}{\gamma_1} \tag{4–21}$$

$$V_{TH,2} = \frac{\Psi_{FP,2} - \beta_2 \cdot V_{SUB} - \beta_3}{\beta_1} \tag{4–22}$$

where

$$\gamma_1 = g_1\alpha_1 e^{d_1 x_{\min,1}} + g_1\alpha_4 e^{-d_1 x_{\min,1}} + g_2\alpha_7 e^{d_2 x_{\min,1}} + g_2\alpha_{10} e^{-d_2 x_{\min,1}} + \lambda_1$$
$$\gamma_2 = g_1\alpha_2 e^{d_1 x_{\min,1}} + g_1\alpha_5 e^{-d_1 x_{\min,1}} + g_2\alpha_8 e^{d_2 x_{\min,1}} + g_2\alpha_{11} e^{-d_2 x_{\min,1}} + \lambda_2$$
$$\gamma_3 = g_1\alpha_3 e^{d_1 x_{\min,1}} + g_1\alpha_6 e^{-d_1 x_{\min,1}} + g_2\alpha_9 e^{d_2 x_{\min,1}} + g_2\alpha_{12} e^{-d_2 x_{\min,1}} + \lambda_3$$
$$\beta_1 = g_1\delta_1 e^{d_1 x_{\min,2}} + g_1\delta_4 e^{-d_1 x_{\min,2}} + g_2\delta_7 e^{d_2 x_{\min,2}} + g_2\delta_{10} e^{-d_2 x_{\min,2}} + \lambda_1$$
$$\beta_2 = g_1\delta_2 e^{d_1 x_{\min,2}} + g_1\delta_5 e^{-d_1 x_{\min,2}} + g_2\delta_8 e^{d_2 x_{\min,2}} + g_2\delta_{11} e^{-d_2 x_{\min,2}} + \lambda_2$$
$$\beta_3 = g_1\delta_3 e^{d_1 x_{\min,2}} + g_1\delta_6 e^{-d_1 x_{\min,2}} + g_2\delta_9 e^{d_2 x_{\min,2}} + g_2\delta_{12} e^{-d_2 x_{\min,2}} + \lambda_4.$$

Then, the threshold voltage of the FD–SOI MOS transistor is obtained by taking the maximum of eqs. (4–21) and (4–22).

4–4 Subthreshold Current Model

In the subthreshold region of SOI MOSFET operation, the depletion charge is much larger than the inversion carrier, thus the diffusion current component is expected to be dominant. However, since the potential distribution in the silicon film varies along the channel, the drift current component may contribute to the subthreshold current flow. Based on the drift–diffusion current theory, the electron current density in the *n*–MOSFET can be expressed as

$$J_n = -q\mu_n n\frac{\partial \phi_{fs}(x)}{\partial x} + qD_n\frac{\partial n(x)}{\partial x} \tag{4–23}$$

where $n(x)$ is the electron density along the channel length, and D_n is the electron diffusion coefficient, which can be related to the thermal voltage V_T and electron mobility μ_n through Einstein relation as $D_n = \mu_n \cdot V_T$. Multiplying eq. (4–23) by an integrating factor of $\exp(-\phi_{fs}(x)/V_T)$, the right hand side of the equation can be transformed into an exact derivative. With the boundary conditions in eqs. (4–11) and (4–12), we can obtain

$$J_n = -qD_n N_A \cdot \exp\left(-\frac{V_{bi}}{V_T}\right) \cdot \frac{\left[1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right]}{\int_0^L \exp\left(-\frac{\phi_{fs}(x)}{V_T}\right)\cdot dx} \tag{4–24}$$

The subthreshold current can be obtained by integrating the current density over the cross section of the conducting channel, yielding

$$I_{SUB} = J_n \cdot W \cdot d \tag{4–25}$$

where W is the device channel width and d is the effective channel thickness, which can be estimated as the distance from the surface to the position where the electrostatic potential has changed by V_T [63]. According to the Gauss' Law, the vertical component of the electric field at the surface, V_T/d, is equal to Q_{dep}/ε_{si}, where Q_{dep} is the depletion charge. Thus, the effective channel thickness d can be obtained as

$$d = V_T \cdot \left[\frac{\varepsilon_{si}}{2qN_{AV}\cdot\left(\phi_{fs,inv} + V_{GT}/\theta\right)}\right] \tag{4–26}$$

where N_{AV} is the effective doping density within the channel, $\phi_{fs,inv}$ is the surface potential at the onset of strong inversion, $\phi_{fs,inv} = 2\Psi_{FP}$, $V_{GT} = V_{GS} - V_{TH}$, and θ is the subthreshold ideality factor reflecting the gate voltage division between the insulator capacitances and the silicon depletion

layer capacitance. Note that the effective channel thickness given in eq. (4–26) is only valid for the case of $-\phi_{fs.inv} < V_{GT}/\theta < 0$, i.e., the weak inversion and depletion operations. The effective doping profile within the channel can be approximated by an effective channel concentration N_{AV} developed based on the voltage–doping transformation [64]:

$$N_{AV} = N_B + 2\cdot(N_A - N_B)\cdot(L_1/L) - (2\varepsilon_{si}/q)\cdot(V_{DS} + v\cdot V_{bi})/L^2. \qquad (4\text{–}27)$$

where v is a fitting parameter. Substituting eqs. (4–24), (4–26) and (4–27) into eq. (4–25), the subthreshold current can be obtained.

4–5 Results and Discussion

To verify the proposed analytical model, the 2–D device simulation software Medici [32] was used to simulate the surface potential distribution within the silicon film. A set of fully depleted *n*–channel SOI MOS transistors is implemented in Medici having uniformly doped channel, halo and drain/source regions. In this section, we have presented some numerical results to demonstrate the DIBL in short–channel SOI MOS transistors with halo implants and its effect on the threshold voltage variation considering a wide range of parameters of the devices.

In Fig. 4–4, the variation of the front surface potential $\Psi_{fs}(x) = \Psi(x, 0)$ as a function of normalized position (x/L) along the channel has been shown for different gate lengths and drain voltages. The doping profiles of the halo and channel regions of the MOS devices in Figs. 4–4(a) and 4–4(b) belong to the case in Fig. 4–2(c), where halo implants overlap the channel region and make the channel doping concentration increase. From Figs. 4–4(a) and 4–4(b), it is observed that for a fixed gate length, as the drain–source voltage V_{DS} is increased, the minimum front surface potential is elevated which results in the considerable reduction of the channel barrier. Further, for a

fixed value of V_{DS}, the minimum front surface potential is also increased with the decrease in L. Although the lateral position of the minimum front surface potential shifts toward the source side with the increase in V_{DS} as well as with the decrease in L, it remains almost at the middle of the channel region for small values of the drain voltages. The increase in the surface potential at the drain side due to the increased V_{DS} lowers the channel barrier height, i.e., the potential difference between the channel and source regions, of the device that is well known as the DIBL in the short channel MOS transistor. From the figure, it is also observed that DIBL for L = 0.06 μm is more than that for L = 0.09 μm indicating that the effect is more significant if the gate length reduces to deep submicrometer region. In Fig. 4–4(c), (d) and (e), the doping profile of the halo and channel regions of the devices belongs to the case in Fig. 4–2(a). From these figure, it is seen that due to the presence of the halo region with doping concentration higher than the channel region, the barrier height remains unchanged as V_{DS} is increased, where the barrier is the potential difference between the source side halo and source regions. Hence, the halo region near the source side is "screened" from the changes in the drain potential, i.e., the drain voltage is not absorbed in source side halo, but in drain side halo. Furthermore, it is clearly seen that the shift in the position of the minimum front surface potential is almost zero irrespective of the applied drain bias. This is a clear indication that the DIBL effect is considerably reduced for the FD–SOI MOSFET with halo implants. A good agreement is achieved between the numerical simulations and model predictions, that shows the validity of the proposed analytical model.

The surface potential profiles $\Psi_{fs}(x)$ against the lateral position in channel x for the halo devices with gate length as the parameter are shown in Fig. 4–5. It is seen that the barrier lowering effect due to the scaling down of the gate length of the halo devices is small. From the figure, it is also seen that as the doping concentration in the halo region is increased, double–hump appears in the deep–submicrometer devices as well as long channel halo devices. Further, it is clearly seen that at the fixed gate length and drain bias voltage, the drain side surface potential of the devices with lower halo doping concentration elevated more due to the more serious electric field encroachment

from the drain side. On the other hand, the surface potential near by the source side is lower in the devices with higher halo doping profile and this may increase the threshold voltage consequently. Comparisons between the surface potentials of halo SOI MOS devices obtained by the present model and Medici simulator are also shown in Fig. 4–5, and a good agreement is obtained.

The surface potential profiles $\Psi_{fs}(x)$ as a function of normalized position (x/L) along the channel length for the halo MOSFETs of L = 0.09 μm with the length of the halo region L_1 as a parameter is shown in Fig. 4–6. From the figure, it is seen that the position of the minimum surface potential, locating in the source side halo region is shifted toward the source side as the length of the halo region is reduced. Moreover, it is observed that the surface potential minima for the three cases are not the same. The minimum surface potential is shifted to a higher value as the length of the halo region is reduced. This happens because the average doping concentration in the silicon film controlled by the gate is increased as the length of the halo region L_1 is increased. For the fixed channel length and halo doping profile, as the length of the halo region is decreased from 0.035 μm to 0.015 μm, the off–state current I_{off} is increased from 1.84 pA/μm to 59.6 nA/μm, obtained from the 2–D numerical analysis.

The threshold voltage against the gate length L has been plotted in Fig. 4–7 for different silicon film thicknesses t_{si}. It is observed from the figure that the dependence of the threshold voltage on the gate length can be considerably reduced by reducing the thickness of the silicon film. Further, with thinner silicon film, the depleted charge in the silicon film controlled by the gate at the onset of the inversion is reduced and this makes the threshold voltage decrease. Therefore, FD–SOI MOSFETs with thinner silicon film may be used for designing the low–power digital circuits for which devices with lower threshold voltage are needed.

The threshold voltage against the gate length L has been plotted in Fig. 4–8 for different front gate oxide thicknesses t_f. From the figure, it is observed that the threshold voltage of the MOS transistor is lower with thinner gate oxide. This happens because that a MOS transistor with a smaller thickness of gate oxide has a larger value of gate oxide drive capacitance. The effect of the

halo doping concentration N_A on the threshold voltage has been plotted against the gate length and shown in Fig. 4–9. In this figure, it is seen that the threshold voltage is increased as the doping concentration in the halo region is increased. Figures 4–10(a) and 4–10(b) show the surface potentials of the devices with non–overlap and overlap halo regions, respectively. For the halo devices with non–overlap halo regions, i.e., the case in Figs. 4–2(a) and 4–2(b), the threshold voltage is determined by the minimum surface potential in the source side halo region. From Fig. 4–10(a), it is seen that increasing the halo doping concentration will increase the doping profiles and decrease the minimum surface potential in the source side halo region. This would increase the threshold voltage of the devices with non–overlap halo regions. Similarly, from Fig. 4–10(b), it is observed that due to the threshold voltage is determined by the minimum surface potential in the channel region for the halo devices with overlap halo regions, i.e., the case in Figs. 4–2(c) and (d), increasing the halo doping concentration will increase the doping profiles and decrease the minimum surface potential in the channel region, and consequently increase the threshold voltage.

The threshold voltage against the gate length L has been plotted in Fig. 4–11 for the MOS devices with different channel doping concentrations N_B. From the figure, it is observed that for the devices with gate length $L \geq 2L_1$, the variation of the threshold voltage with respect to the change of the channel doping profile is very less. This happens because the lateral position of the minimum surface potential is located in the source side halo region and related to the halo doping concentration. However, for the gate length $L < 2L_1$, the increase of the channel doping concentration would decrease the minimum surface potential in the channel region and increase the threshold voltage as shown in the figure.

Beside the device parameters, the bias voltage may be also used to control the threshold voltage of the MOS device. Figure 4–12 shows the effect of the substrate bias V_{SUB} on the threshold voltage plotted against the gate length. It is seen that for the long–channel halo devices ($L > 2L_1$), a more negative substrate voltage biased results in the increase of the threshold voltage. However, for the short–channel halo devices ($L < 2L_1$), the effect of the substrate bias V_{SUB} on the threshold

voltage is less due to the high doping concentration in the channel region. Therefore, it may be observed that biasing at a negative substrate voltage may be a better choice to reduce the DIBL effect which may substantially improve the threshold voltage degradation. The effects of the drain–source bias voltage V_{DS} on the threshold voltage of the MOSFETs against the gate length L are shown in Fig. 4–13. From the figure, it is observed that the threshold voltage of the device may be shifted to a lower value if V_{DS} is changed from V_{DS} = 0.05 V to V_{DS} = 2.5 V. In other words, for a fixed value of the gate–source voltage, the normally–off device may be turned into normally–on by increasing the drain–source bias voltage V_{DS}. The above results have been compared with the simulation results obtained by the Medici device simulators and a closed agreement is achieved between the two.

Figure 4–14 shows the plot of subthreshold current I_{SUB} against the gate–source voltage V_{GS} with V_{DS} as a parameter. It is observed that although the MOS transistor is with halo regions, the subthreshold current is increased with the increase in V_{DS} due to the increased electric encroachment from the drain region and small value of channel length. The calculated results have been compared with the Medici software and a good agreement is achieved for the gate length down to 0.06 μm that shows the validity of the proposed analytical model.

Figure 4–15 shows the comparison of the surface potentials obtained by the present model and Medici as a function of normalized position along the channel with halo doping concentration N_A as a parameter. It is observed that at the fixed V_{GS}, the surface potential of halo MOS device with higher halo doping concentration is shifted to lower level and results in an increase in the channel barrier height. The effect of the halo doping concentration on the subthreshold current is show in the plot of I_{SUB} vs. V_{GS} in Fig. 4–16. It is seen that the subthreshold current of the MOSFETs with higher halo doping concentration is lower due to the increased barrier height. Figure 4–17 shows the off–state current I_{off} against the channel length L with halo doping concentration N_A as a parameter, where $I_{off} = I_{SUB}$ at V_{GS} = 0 V. It is seen that with the fixed N_A, the I_{off} is increased with the decrease in L due to the short–channel effect. Further, it is observed that for the fixed channel length L, I_{off} is

decreased with the increase in N_A due to the lower minimum surface potential and higher channel barrier height.

Figure 4–18 shows the effect of the channel doping concentration N_B on the surface potential as a function of normalized position (x/L) along the channel length. It is seen that the location of the minimum surface potential remains almost the same and only a small variation of the surface potential occurs in the channel region ($L_1 < x < L_2$) as N_B is varied due to high doping concentration in the halo regions. Owing to the high halo doping concentration, the effect of the channel doping concentration N_B on the subthreshold current I_{SUB} is very small and can be observed from Fig. 4–19. In this figure, it is seen that only a small increase in the subthreshold current as N_B is increased from 5×10^{17} cm^{-3} to 7×10^{17} cm^{-3}. The above results have been compared with the 2–D numerical simulation and a closed agreement is obtained between the two.

4–6 Conclusions

New 2–D analytical models for the 2–D potential distribution, threshold voltage and subthreshold current for short–channel FD–SOI MOSFETs with halo or pocket implants have been presented in this paper. Analytical expressions have been obtained for both the surface potential, and threshold voltage by solving the Poisson's equation with the appropriate boundary conditions. Subsequently, together with the conventional drift–diffusion current theory, an analytical model of subthreshold current is also developed for halo–implanted SOI MOSFET devices. Numerical results for the surface potential, threshold voltage and subthreshold current have been presented for both overlap halo and non–overlap halo cases. The proposed surface potential and threshold voltage model are also appropriate for the conventional MOSFETs without halo implants. The effects of the different device structure parameters such as the gate length, silicon film thickness, front gate oxide thickness, halo doping concentration and channel doping concentration, and different bias conditions such as substrate and drain voltages on the threshold voltage of the device are also

demonstrated. The calculated results of the presented analytical models have been compared with the simulation results obtained by the Medici device simulation software and a good agreement obtained between them shows the validity of the present analytical models of the surface potential, threshold voltage and subthreshold current. To the best of our knowledge, these are the first 2–D models for the FD–SOI MOSFETs with halo or pocket implants, considering subthreshold surface potential, threshold voltage and subthreshold current at the same time.

Chapter 5

A New Small–Signal MOSFET Model and Parameter Extraction Method for RF IC's Applications

5–1 Introduction

The majority of the radio–frequency integrated circuits (RFICs) are typically implemented by GaAs or silicon bipolar technologies [65], [66]. Due to their high unity–gain cutoff frequency (f_t), GaAs devices and BJTs have been generally used in high frequency applications. However, continuously scaling down of the minimum channel length and the consequent increase of f_t have made CMOS technology become an attractive one in applications for analog and RFICs [67]. With another advantages (i.e., high integration level and low cost budget, etc.) over GaAs and silicon bipolar technologies, CMOS technology is a good candidate to meet the demand of wireless telecommunication system in the future.

As circuitry operates at higher frequency (GHz frequency range) and lower voltages, a major requirement for RF circuit design is the availability of RF MOS transistor model to describe the circuit behavior accurately. Besides, the establishment of an accurate parameters extraction method relevant to the RF model is essential.

In order to meet the requirement for an accurate RF model, several fundamental analyses on MOSFETs high frequency characteristics have been developed, as described in [68]–[70]. As MOSFETs operation frequency approaches VHF and beyond, the parasitic components geometry–related (e.g., inductance, capacitance and resistance) play important roles in their high frequency performance. Therefore, the nature of gate region – RLC distributed network and substrate parasitics should be considered in the development of RF MOS model. Some conventional models [71]–[73] replaced the gate region with a single resistance, and this would cause inaccuracy in predicting the gate related noise at high frequency [73]. Besides, in several models [74]–[76], the

substrate parasitics were not taken into account, and this would hurt their accuracy in the prediction of output characteristics (i.e., output impedance [77]). In addition, several conventional models [77]–[79] excluded the nonreciprocal capacitance considering the charge conservation [80], and this would result in a significant error in predicting the imaginary parts of Y_{12} and Y_{21}.

Except for the development of an accurate RF model, a related parameters extraction methodology is indispensable. Several methods of extracting small–signal equivalent circuit parameters from the *S*–parameter measurement data have been reported [78], [81] and [82]. However, most of them require complex curve fitting and optimization steps.

In this chapter, we propose a high frequency analytical MOSFETs model well describing the distributed effects of the gate region and including substrate parasitics and nonreciprocal capacitance. Besides, a direct and accurate parameter extraction method for the proposed model including gate–related parameters, substrate–related parameters and nonreciprocal capacitor is also proposed. This study focuses on the development of a physics–based small signal MOSFETs model and an accurate parameter extraction approach by *Y*-parameter analysis from measured *S*-parameters.

This chapter is organized in the following manners. In Section 5–2, a new and accurate high frequency MOS transistor model is briefly described. This section begins with the assumptions and definitions, which are useful for the model development, and follows by describing the closed–form modeling equations. In Section 5–3, an accurate and direct method for the extractions of the parameters of small signal equivalent circuit is presented and explained in detail. In Section 5–4, both the proposed model and related extraction method are verified by the experimental data. Finally, the conclusions are summarized in Section 5–5.

5–2 Small Signal RF MOSFET Model

In this section, a new and analytical small signal RF MOSFET model including distributed

gate network, substrate parasitics and nonreciprocal capacitance is proposed. At first, the relative approaches and assumptions are briefly described and defined, respectively. Then, the derivation details of model equations will be described.

5–2.1 Approaches and Assumptions

To accurately describe the fact that the signal travels across the gate in the form of incident and reflected EM waves [74], we use the concept of transmission line theorem to model the distributed nature of the gate region and the delay it causes in charging the gate capacitance. In addition, for the sake of simplicity and calculation efficiency, we add a lumped resistance to the bulk terminal to account for the substrate coupling effect. We also use the nonreciprocal capacitance to take into account the different effects of the gate and drain on each other in terms of charging currents [80]. In order to describe the distributed nature of the gate region, a MOS transistor is viewed as an array of discrete transistors connected in parallel via gate resistances along the gate region, as illustrated in Fig. 5–1. The related small signal equivalent circuit is shown in Fig. 5–2 which is based on the three–terminal configuration. In a three–terminal configuration, the substrate is tied to the source, as in most high frequency applications [73] and [83]. This model is suitable for the case of zero source–substrate bias in circuit. Before developing expressions for the *Y*–parameters of the MOS transistors, the following assumptions have to be made:

1) Assumption 1: It is assumed that the DC bias condition remains the same along the gate width. This means that only AC small signals applied at the gate region needed to be considered. With this assumption, the discrete MOS transistors illustrated in Fig. 5–1 have the same small signal parameters (e.g., transconductance g_m; drain–bulk transconductance g_{mb}, etc.). To make the model equations clearly, we use the prime–notation to stand for the parameters per width (i.e., X' is used to represent the variable X per unit width).

$$R_g' = R_g / W \tag{5–1}$$

$$C'_{gd} = C_{gd}/W \tag{5–2}$$

$$C'_{gs} = C_{gs}/W \tag{5–3}$$

$$g'_m = g_m/W \tag{5–4}$$

where W is the channel width, R_g is the gate resistance, C_{gd} and C_{gs} are the gate–to–drain capacitance and gate–to–source capacitance, respectively, and g_{mb} is the transconductance of substrate.

2) Assumption 2: This assumption states that the electric field along the width of the device is significantly less than the fields existing along the channel length. Note that this condition is valid in most devices used for RF applications where the gate width *W* is normally larger with respect to the gate length *L*.

3) Assumption 3: In order to develop an analytical model easily, the average voltage at the gate region is expressed as:

$$\bar{v} = \frac{1}{W}\int_0^W v(x)\cdot dx. \tag{5–5}$$

where $\bar{v}$ is the average voltage at the gate region, and $v(x)$ is the voltage at the location *x* along the gate region. Thus, the total current flowing in the channel can be expressed as:

$$\overline{g_m v} = \int_0^W g'_m \cdot v(x)\cdot dx. \tag{5–6}$$

5–2.2 Analysis for New RF MOSFET Model

In the primary step, we will decouple the feedback loops and find the loadings caused by the feedback networks at the input and output terminals. Then, the derivation of *Y*–parameters of MOSFETs will be expressed in the secondary step.

1) Step 1: The circuit configuration shown in Fig. 5–2 is too complicated to be analyzed directly.

Nevertheless, if the circuit is viewed as a dual–feedback circuit in which ΔC_{gd} is the local shunt–shunt feedback element forms the first feedback loop (i.e., loop A), where $\Delta C_{gd} = C_{gd}^{'} \cdot \Delta x$ represents the gate–drain capacitance of the section Δx at the gate region, and C_{db}, C_{sb}, R_{sub} and $C_{gb}^{'} \cdot \Delta x$ are the local shunt–shunt feedback elements form the second feedback loop (i.e., loop B), where $\Delta C_{gb} = C_{gb}^{'} \cdot \Delta x$ represents the gate–substrate capacitance of the section Δx at the gate region, then the circuit becomes much easier to solve. The feedback loops A and B are illustrated in Fig. 5–3, where V_1 and V_2 represent the output voltage relative to ground (e.g., V_{ds}) and the voltage along the gate width shown in Fig. 5–2, respectively. By local shunt–shunt feedback theory [84], the loading effects at the input and output terminals caused by the feedback networks shown in Fig. 5–3 can be expressed in the *Y*–parameter representation as follows.

$$Y_{11,loopA} = sC_{gd} \tag{5–7}$$

$$Y_{12,loopA} = Y_{21,loopA} = -sC_{gd}^{'} \cdot \Delta x \tag{5–8}$$

$$Y_{22,loopA} = sC_{gd}^{'} \cdot \Delta x \tag{5–9}$$

$$Y_{11,loopB} = \frac{sC_{db}\left(1 + sR_{sub}\left(C_{sb} + C_{gb}\right)\right)}{1 + sR_{sub}C_b} \tag{5–10}$$

$$Y_{12,loopB} = Y_{21,loopB} = -\frac{s^2 R_{sub} C_{db} C_{gb}^{'} \cdot \Delta x}{1 + sR_{sub}C_b} \tag{5–11}$$

$$Y_{22,loopB} = \frac{sC_{gb}^{'} \cdot \Delta x\left(1 + sR_{sub}\left(C_{sb} + C_{db} + C_{gb} - C_{gb}^{'} \cdot \Delta x\right)\right)}{1 + sR_{sub}C_b} \tag{5–12}$$

where, C_{db}, C_{sb} and C_{gb} are the drain–to–substrate capacitance, source–to–substrate capacitance and gate–to–substrate capacitance, respectively, $C_{gd}^{'}$ and $C_{gb}^{'}$ are the gate–to–drain capacitance per unit width and gate–to–substrate capacitance per unit width, R_{sub} is the substrate resistance, and C_b is the sum of C_{gb}, C_{db} and C_{sb}.

Then, with the local shunt–shunt feedback theory mentioned above, the circuit in Fig. 5–2 can

be transformed into the one in Fig. 5–4. In Fig. 5–4, some components (i.e., $Y'_{12,loopA}$, $Y'_{21,loopA}$, $Y'_{22,loopA}$, $Y'_{12,loopB}$, $Y'_{21,loopB}$ and $Y'_{22,loopB}$) in the Blocks A and B are referred to as the per–unit width components and expressed as:

$$Y'_{12,loopA} = Y'_{21,loopA} = -sC'_{gd} \tag{5–13}$$

$$Y'_{22,loopA} = sC'_{gd} \tag{5–14}$$

$$Y'_{12,loopB} = Y'_{21,loopB} = -\frac{s^2 R_{sub} C_{db} C'_{gb}}{1 + sR_{sub} C_b} \tag{5–15}$$

$$\begin{aligned} Y'_{22,loopB} &= \frac{sC'_{gb}\left(1 + sR_{sub}\left(C_{sb} + C_{db} + C_{gb} - C'_{gb} \cdot \Delta x\right)\right)}{1 + sR_{sub} C_b} \\ &\approx \frac{sC'_{gb}\left(1 + sR_{sub}\left(C_{sb} + C_{db} + C_{gb}\right)\right)}{1 + sR_{sub} C_b} = sC'_{gb} \end{aligned} \tag{5–16}$$

where Δx is an infinitesimal section of the gate width.

3) *Step 2*: In the derivation procedure of *Y*–parameters, the complete small–signal equivalent circuit of Fig. 5–4 is analyzed as a two–port circuit with input at the gate and output at the drain and both the source and substrate terminals are grounded. Then, due to the distributed RC network along the gate region, the equivalent circuit can be analyzed by transmission line theory. Along the gate width, we have the transmission line equations in frequency domain as follows:

$$-\frac{\partial v(x)}{\partial x} = R'_g \cdot i(x) \tag{5–17}$$

$$\begin{aligned} -\frac{\partial i(x)}{\partial x} &= \left(sC'_{gs} + Y'_{22,loopA} + Y'_{22,loopB}\right) \cdot v(x) + \left(Y'_{21,loopA} + Y'_{21,loopB}\right) \cdot vout \\ &= \left(sC'_{gs} + sC'_{gd} + sC'_{gb}\right) \cdot v(x) + \left(-sC'_{gd} + -\frac{s^2 R_{sub} C_{db} C'_{gb}}{1 + sR_{sub} C_b}\right) \cdot vout \end{aligned} \tag{5–18}$$

which are subject to the boundary conditions $i(W) = 0$ and $v(0) = v_{gs}$. Solving these equations for $v(x)$ and $i(x)$ yields

$$v(x)=\left(v_{gs}-\frac{B}{A}\right)\frac{\cosh\left(\sqrt{A}\cdot(W-x)\right)}{\cosh\left(\sqrt{A}\cdot W\right)}+\frac{B}{A} \tag{5–19}$$

$$i(x)=\left(v_{gs}-\frac{B}{A}\right)\cdot\frac{\sqrt{A}}{R_g^{'}}\cdot\frac{\sinh\left(\sqrt{A}\cdot(W-x)\right)}{\cosh\left(\sqrt{A}\cdot W\right)} \tag{5–20}$$

where

$$A=R_g^{'}\left(sC_{gs}^{'}+Y_{22,loopA}^{'}+Y_{22,loopB}^{'}\right)=R_g^{'}\left(sC_{gs}^{'}+sC_{gd}^{'}+sC_{gb}^{'}\right)=sR_g^{'}C_g^{'} \tag{5–21}$$

$$B=-R_g^{'}\left(Y_{21,loopA}^{'}+Y_{21,loopB}^{'}\right)\cdot vout=R_g^{'}\left(sC_{gd}^{'}+\frac{s^2R_{sub}C_{db}C_{gb}^{'}}{1+sR_{sub}C_b}\right)\cdot vout \tag{5–22}$$

where $R_g^{'}$ is the gate resistance per unit width and $C_g^{'}=C_{gs}^{'}+C_{gd}^{'}+C_{gb}^{'}$. With the assumption (3), the average voltage at the gate region and total current in the channel can be expressed as:

$$\bar{v}=\left(v_{gs}-\frac{B}{A}\right)\cdot\frac{\tanh\left(\sqrt{AW}\right)}{\sqrt{AW}}+\frac{B}{A} \tag{5–23}$$

$$\overline{g_m v}=g_m\cdot\bar{v}=g_m\cdot\left[\left(v_{gs}-\frac{B}{A}\right)\cdot\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W}+\frac{B}{A}\right]. \tag{5–24}$$

Then, according to the two–port circuit model, the *Y*–parameters of the equivalent small signal circuit can be solved as follows:

$$Y_{11}=\left[\frac{i_g}{v_{gs}}\right]_{vout=0}=W\left[sC_{gs}^{'}+Y_{22,loopA}^{'}+Y_{22,loopB}^{'}\right]\cdot\frac{\tanh\left(\sqrt{AW}\right)}{\sqrt{AW}}=sC_g\cdot\frac{\tanh\left(\sqrt{AW}\right)}{\sqrt{AW}} \tag{5–25}$$

where i_g is expressed as the current at location $x = 0$ and C_g is the sum of C_{gb}, C_{gs} and C_{gd}. The above result clearly indicates that three coupling paths influence the input admittance Y_{11}. They are the ways from gate to source, gate to drain and gate to substrate through C_{gs}, C_{gd} and C_{gb}, respectively. Then, the parameter Y_{12} can be expressed as:

$$Y_{12}=\left[\frac{i_g}{v_{out}}\right]_{v_{gs}=0}=W\left(\underbrace{Y'_{21,loopA}}_{TermM}+\underbrace{Y'_{21,loopB}}_{TermN}\right)\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W}$$
$$=-\left(sC_{gd}+\frac{s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W} \quad (5\text{–}26)$$

Equation (5–26) provides useful insight on the coupling paths of drain voltage to gate current. Two terms (term M and term N) in equation (5–26) describe the paths. Term M: the voltage applied to the drain couples to the distributed gate region through C_{gd}. Term N: the drain voltage couples to the distributed substrate region and makes current flow through C_{gb} into gate region. In addition, the parameter Y_{21} can be expressed as:

$$Y_{21}=\left[\frac{i_d}{v_{gs}}\right]_{vout=0}=\left[\underbrace{\left(g_m+WY'_{12,loopA}-sC_m\right)}_{TermO}+\underbrace{g_{mb}\cdot\frac{sR_{sub}C_{gb}}{1+sR_{sub}C_b}}_{TermP}+W\underbrace{Y'_{12,.loopB}}_{TermQ}\right]\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W}$$
$$=\left(g_m-sC_{dg}+\frac{sg_{mb}R_{sub}C_{gb}-s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W} \quad (5\text{–}27)$$

where C_m is the transcapacitance (i.e., $C_m=C_{dg}-C_{gd}$) and C_{dg} is the drain–to–gate capacitance. Similarly, the signal coupling paths are described by three terms expressed in equation (5–27). Term O: the voltage applied to the gate makes the current flowing in the channel, but due to the existence of C_{gd}, the current flowing from the drain end must subtract the current flowing through C_{gd} from gate region. Term P: the gate voltage makes current flow through C_{gb} and voltage drop across R_{sub}, v_{bs}, which is multiplied by g_{mb} to make current flowing into the channel. Term Q: the gate voltage makes the current flow through C_{gb} and voltage drop on R_{sub}, v_{bs}, which makes current flowing through C_{db} into the drain end in the opposite direction of i_d. Finally, the parameter Y_{22} can be expressed as:

$$Y_{22}=\left[\frac{i_d}{v_{out}}\right]_{v_{gs}=0}=\left(\underbrace{g_m+W\left(Y'_{12,loopA}+Y'_{12,loopB}\right)-sC_m}_{TermR}\right)\left(1-\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W}\right)\frac{(-1)R'_g\left(Y'_{21,loopA}+Y'_{21,loopB}\right)}{A}$$
$$+g_{ds}+\underbrace{Y_{11,loopA}}_{TermS}+\underbrace{Y_{11,loopB}}_{TermT}+\underbrace{g_{mb}\cdot\frac{sR_{sub}C_{db}}{1+sR_{sub}C_b}}_{TermU}$$
$$=\left(g_m-sC_{dg}-\frac{s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\left(1-\frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W}\right)\left(\frac{sC'_{gd}+\frac{s^2R_{sub}C_{db}C'_{gb}}{1+sR_{sub}C_b}}{sC'_g}\right)$$
$$+g_{ds}+sC_{gd}+\frac{sC_{db}\left[1+g_{mb}R_{sub}+sR_{sub}\left(C_{sb}+C_{gb}\right)\right]}{1+sR_{sub}C_b} \qquad (5\text{–}28)$$

where g_{ds} is the conductance of drain–to–source. In equation (5–28), four terms describe the signal coupling paths. Term R: the voltage applied to the drain makes current flow into the distributed gate region through loops A and B, and voltage drop on the gate region, v_{gs}, which makes current flow out of the drain end through feedback loops A and B. Term S: the drain voltage makes current flow through loop A. Term T: the drain voltage makes current flow through C_{db} and voltage drop across R_{sub}, C_{sb} and C_{gb}, v_{bs}, which makes current flow out of the drain end. Term U: the voltage drop v_{bs} due to the coupling effect as described in Term T is multiplied by g_{mb} to make current flow into the channel. From the expressions of *Y*–parameters derived, how signal–coupling occurring through capacitive and resistive elements contained in Fig. 5–2 has been clearly explained.

5–3 Parameter–Extraction Method

In this section, a direct extraction method for RF equivalent circuit parameters of MOS transistors is presented. The method is based on the linear regression approach and the *Y*–parameters obtained from *S*–parameters analysis. All components in the equivalent circuit are extracted by the *Y*–parameters analysis and the relative analytical equations are derived from the

real and imaginary parts of *Y*–parameter expressions mentioned in section 5–2. The details of the equivalent circuit parameters extraction are described as follows.

Due to the fact that g_m and g_{ds} are DC parameters, they can be obtained from the *y*–intercept of $\mathrm{Re}[Y_{21}]$ versus w^2 and *y*–intercept of $\mathrm{Re}[Y_{22}]$ versus w^2 at low frequency, respectively and shown as:

$$g_m = \mathrm{Re}[Y_{21}]_{w^2=0} \tag{5–29}$$

$$g_{ds} = \mathrm{Re}[Y_{22}]_{w^2=0} \tag{5–30}$$

Then, at low frequency, with the assumption that the first term in the parentheses of equation (5–26) dominates, Y_{12} can be approximated as follows:

$$Y_{12} = -\left(sC_{gd} + \frac{s^2 R_{sub} C_{db} C_{gb}}{1 + sR_{sub} C_b} \right) \frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W} \approx -sC_{gd} \frac{\tanh\left(\sqrt{A}\cdot W\right)}{\sqrt{A}\cdot W} \tag{5–31}$$

Similarly, with the assumption that the first two terms in the parentheses of equation (5–27) dominate, Y_{21} can be approximated as follows:

$$Y_{21} = \left(g_m - sC_{dg} + \frac{sg_{mb} R_{sub} C_{gb} - s^2 R_{sub} C_{db} C_{gb}}{1 + sR_{sub} C_b} \right) \frac{\tanh\left(\sqrt{A}W\right)}{\sqrt{A}W} \approx \left(g_m - sC_{dg}\right) \frac{\tanh\left(\sqrt{A}\cdot W\right)}{\sqrt{A}\cdot W} \tag{5–32}$$

Then, due to the fact that the real part of term $\tanh\left(\sqrt{A}\cdot W\right)/\left(\sqrt{A}\cdot W\right)$ is almost equal to 1 at low frequency, as shown in Fig. 5–5, C_{gd} can be obtained as:

$$C_{gd} = -\mathrm{Im}[Y_{12}] / \left(\mathrm{Re}[\frac{\tanh\left(\sqrt{A}\cdot W\right)}{\sqrt{A}\cdot W}] \cdot w \right) = \mathrm{Im}[Y_{12}] / w. \tag{5–33}$$

In addition, C_g can be obtained from Y_{11} at low frequency and shown as follows:

$$C_g = \mathrm{Im}[Y_{11}]/\left(\mathrm{Re}[\frac{\tanh\left(\sqrt{A}\cdot W\right)}{\sqrt{A}\cdot W}]\cdot w \right) = \mathrm{Im}[Y_{11}]/w \tag{5–34}$$

With the extracted parameters C_g, we can obtain R_g by optimization to fit equation (5–25) to the experimental data Y_{11}. Then, in order to extract the transcapacitance C_m, C_{dg} has to be extracted first. At low frequency, from equation (5–32), C_{dg} can be obtained as:

$$C_{dg} = \mathrm{Im}[Y_{21}]/\left(\mathrm{Re}[\frac{\tanh\left(\sqrt{A}\cdot W\right)}{\sqrt{A}\cdot W}]\cdot w \right) = \mathrm{Im}[Y_{21}]/w. \tag{5–35}$$

Besides, based on the assumption that the term $s^2 R_{sub} C_{db} C_{gb} / \left(1 + sR_{sub} C_b\right)$ is extremely small for frequency up to 10 GHz, equation (5–28) can be re–expressed as:

$$\begin{aligned} Y_{22} &\approx \left(g_m - sC_{dg}\right)\left(1 - \frac{\tanh\left(\sqrt{AW}\right)}{\sqrt{AW}}\right)\left(\frac{C'_{gd}}{C'_g}\right) + g_{ds} + sC_{gd} + \frac{sC_{db}\left[1 + g_{mb}R_{sub} + sR_{sub}\left(C_{sb} + C_{gb}\right)\right]}{1 + sR_{sub}C_b} \\ &= Y_A + \frac{sC_{db}\left[1 + g_{mb}R_{sub} + sR_{sub}\left(C_{sb} + C_{gb}\right)\right]}{1 + sR_{sub}C_b} \end{aligned} \tag{5–36}$$

where

$$Y_A = \left(g_m - sC_{dg}\right)\left(1 - \frac{\tanh\left(\sqrt{AW}\right)}{\sqrt{AW}}\right)\left(\frac{C'_{gd}}{C'_g}\right) + g_{ds} + sC_{gd}$$

Additionally, at low frequency, with the assumption $w^2 R_{sub}^2 C_b^2 << 1$, equation (5–36) can be approximated as [86]:

$$\begin{aligned} Y_{22} &\approx Y_A + w^2 R_{sub}\left[C_b\left(C_{db} + g_{mb}R_{sub}C_{db}\right) - C_{db}\left(C_{sb} + C_{gb}\right)\right] \\ &\quad + jw\left[\left(C_{db} + g_{mb}R_{sub}C_{db}\right) + w^2 R_{sub}^2 C_b C_{db}\left(C_{sb} + C_{gb}\right)\right] \\ &\approx Y_A + w^2 R_{sub} C_{db}^2 + jwC_{db} \end{aligned} \tag{5–37}$$

In the equation (5–37), in order to obtain initial values of C_{db} and R_{sub}, we assume that

$g_{mb}R_{sub} << 1$. This assumption may slightly overestimate the values of C_{db} and R_{sub}, so they have to be corrected by optimization after substrate–related components (i.e., C_{gb}, C_b and g_{mb}) extracted. At first, we determine the initial values of C_{db} and R_{sub} from the imaginary and real parts of Y_{22} in (5–37) at low frequency, respectively, and shown as follows:

$$C_{db} = \left(\mathrm{Im}[Y_{22}] - \mathrm{Im}[Y_A]\right)/w \tag{5–38}$$

$$R_{sub} = \left(\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_A]\right)/\left(w^2 \cdot C_{db}^2\right). \tag{5–39}$$

For the extraction of substrate–related components, C_{gb}, C_b and g_{mb}, Y_{sub} is first defined as follows:

$$Y_{sub} = Y_{22} - Y_A \approx jw\frac{C_{db}\left(1+g_{mb}R_{sub}\right)}{1+w^2R_{sub}^2C_b^2} + w^2\frac{R_{sub}C_{db}\left(g_{mb}R_{sub}C_b + C_{db}\right)}{1+w^2R_{sub}^2C_b^2} \tag{5–40}$$

where w^3–terms are negligible compared with the w–terms for operation frequency up to 10 GHz. The parameter g_{mb} can be obtained from the intercept of the relationship for $w/\mathrm{Im}[Y_{sub}]$ versus w^2 by equation (5–41) as follows:

$$\frac{w}{\mathrm{Im}[Y_{sub}]} = \frac{1}{C_{db}(1+g_{mb}R_{sub})} + w^2\frac{R_{sub}^2C_b^2}{C_{db}(1+g_{mb}R_{sub})} \tag{5–41}$$

Then, C_b is obtained from the slope of the relationship for $w^2/\mathrm{Re}[Y_{sub}]$ versus w^2 and shown as:

$$\frac{w^2}{\mathrm{Re}[Y_{sub}]} = \frac{1}{R_{sub}C_{db}\left(R_{sub}g_{mb}C_b + C_{db}\right)} + w^2\frac{R_{sub}^2C_b^2}{R_{sub}C_{db}\left(R_{sub}g_{mb}C_b + C_{db}\right)} \tag{5–42}$$

The remaining parameter C_{gb} is determined by optimization to fit equation (5–36) to the experimental data Y_{22}. The validity of the assumptions mentioned above (i.e. $w^2R_{sub}^2C_b^2 << 1$ at low frequency; $s^2R_{sub}C_{db}C_{gb}/\left(1+sR_{sub}C_b\right)$ is extremely small for frequency up to 10 GHz) will be

checked after all parameters are extracted.

5–4 Verification with Experiments and Result Discussion

In this section, the proposed direct extraction approach was applied to determine the parameters of the test device, which were *n*–MOSFETs fabricated by 0.18–μm technology. To obtain the *Y*–parameters of RF MOSFETs, *S*–parameters were measured in the common–source configuration using an Agilent 8510C vector network analyzer and an on–wafer RF probe station. Before starting the measuring procedure, the calibration was performed on a ceramic calibration substrate using a SOLT calibration method. Besides, the measured data had to be corrected for parasitic capacitance of input/output pads and the resistances and inductances of connection lines using two–step de–embedding technique [85]. The parameter extraction approach had been performed on the *n*–MOSFETs with 0.18–μm length and 105–μm width.

Figure 5–6 shows the extraction results of transconductance g_m and channel conductance g_{ds} for an *n*–MOSFET device *W*/*L* = 105–μm/0.18–μm biased at $V_{gs}=1\ V$ and $V_{ds}=1.4\ V$. The transconductance g_m was obtained from the *y*–intercept of $\mathrm{Re}[Y_{21}]$ versus w^2 at low frequency, as shown in Fig. 5–6(a). In similarity, the channel conductance g_{ds} was obtained from the *y*–intercept of $\mathrm{Re}[Y_{22}]$ versus w^2 at low frequency, as shown in Fig. 5–6(b). In Fig. 5–7(a), g_{mb} can be obtained from the *y*–intercept of linear fit straight line of $w/\mathrm{Im}[Y_{sub}]$ versus w^2. In Fig. 5–7(b), C_b can be obtained from the slope of linear fit straight line of $w^2/\mathrm{Re}[Y_{sub}]$ versus w^2. Figures. 5–8 and 5–9 show the extracted parameters C_{gb}, C_b, C_{sb}, C_{db}, C_{gd}, C_{dg}, C_{gs}, R_g and R_{sub} as a function of frequency. They show that the extracted resistances and capacitances are frequency–independent and this result verifies that the proposed extraction approach is accurate and

reliable. Furthermore, due to the charge–conservation and non–reciprocity, C_{dg} is larger than C_{gd}, as shown in Fig. 5–8. The extracted values of all parameters are summarized in Table 6. From the extracted parameters, the value of $w^2R_{sub}^2C_b^2$ is calculated to be 0.012 at 1 GHz, and the real and imaginary parts of $s^2R_{sub}C_{db}C_{gb}/(1+sR_{sub}C_b)$ are calculated to be 8×10^{-5} and -8.6×10^{-5} at 10 GHz, respectively, which are much smaller than the ones of $g_m - jwC_{dg}$ and jwC_{gd}. Besides, for the extracted parameters listed in Table 6, the assumptions used in the approximations of Y_{12} and Y_{21} in the equations (5–31) and (5–32) are valid for frequency up to 10 GHz. These results verify the validity of the assumptions made in the extraction approach.

In Fig. 5–10, the *Y*–parameters calculated with the extracted parameters are compared with measured data for two bias conditions: 1) $V_{gs}=1\ V$, $V_{ds}=1.4\ V$; and 2) $V_{gs}=0.6\ V$, $V_{ds}=1.4\ V$. It is shown that a good agreement was obtained between the simulation results and measured data. From equation (5–27), it is known that nonreciprocal capacitance C_{dg} contributes the accuracy in $\mathrm{Im}[Y_{21}]$ prediction. In Fig. 5–10(c), excluding the nonreciprocal capacitance C_{dg} resulting in a significant error in matching $\mathrm{Im}[Y_{21}]$ is observed, especially for larger V_{gs}. This is because C_{dg} increases with V_{gs}, being discussed latter.

Figure 5–11(a) shows the gate bias dependence of the extracted capacitances for an *n*–MOSFET biased at $V_{ds}=1.4\ V$. As gate bias increases for constant V_{ds}, C_{gb} decreases due to the fact that the inversion status is getting stronger as V_{gs} increases. In other words, the ability of the inversion layer to protect the gate from the influence of the substrate is increasing as V_{gs} increases. In saturation region, C_{db} is dominated by junction capacitance and almost constant at fixed V_{ds}. C_{gd} and C_{gs} are composed of intrinsic capacitances C_{gdi}, C_{gsi} and overlap

capacitances C_{gdo}, C_{gso}. C_{gd} is dominated by the overlap capacitance C_{gdo} in the saturation region because the communication from the drain to the rest of the device is cut off owing to the pinch–off region. Furthermore, C_{dg} and C_m increase with V_{gs} due to the increase of intrinsic capacitance. Figure 5–11(b) shows the gate bias dependence of the extracted resistances for an *n*–MOSFET biased at $V_{ds} = 1.4$ V. From the figure, it is shown that R_g and R_{sub} remain almost constant as V_{gs} increases.

The drain bias dependence of the extracted capacitances for an *n*–MOSFET biased at $V_{gs} = 1$ V is shown in Fig. 5–12(a). As V_{ds} increases, C_{gb} increases because the influence of the substrate bias on the gate charge is increasing. Due to the increasing reverse bias between drain and substrate, C_{db} decreases as V_{ds} increases. In the saturation, C_{gs} and C_{gd} are dominated by the overlap capacitances C_{gdo}, C_{gso} and remain constant. Figure 5–12(b) shows the drain bias dependence of the extracted resistances for an *n*–MOSFET biased at $V_{gs} = 1$ V. The extracted resistances R_g and R_{sub} are almost constant as V_{ds} increases. The bias dependence of transconductance g_m obtained from *Y*–parameters measurement and conventional DC measurement for an *n*–MOSFET is shown in Fig. 5–13. It can be seen that there is a good agreement between these two measurements. The results demonstrate that the DC–related and AC–related parameters can be extracted by the proposed method in the HF analysis simultaneously. This extraction method avoids the possible error occurring in the conventional DC extraction method for transconductance g_m. This is because that conventional DC extraction method extracts g_m by differentiation of the I–V curves and this may cause a significant error.

5–5 Conclusions

In this chapter, a new and accurate small signal model including distributed gate network, substrate network and nonreciprocal capacitance has been developed. Meanwhile, a direct extraction method for the parameters of the new model is also proposed. This model uses transmission line theorem to describe the distributed gate region, a single substrate resistance and relative capacitances to model the distributed substrate network and accounts for the nonreciprocal capacitance. In addition, an examination has done by using the measured data to verify the model and parameter extraction method. The extracted parameters are physical meaning and good agreements have been obtained between the simulation results and measured data. Furthermore, the extraction method was used to extract the transconductance g_m by *Y*–parameters analysis and verified by DC measurement data. The results demonstrated that the proposed extraction method is accurate and reliable.

Chapter 6

An Efficient Method for Determining Threshold Voltage, Effective Inversion Layer Mobility, Series resistance, and Effective Geometries of MOSFETs by *S*–parameter Measurement

6–1 Introduction

Effective channel length and width, threshold voltage, inversion layer mobility and source/drain resistances are the essential parameters of the SPICE–based submicron MOSFET model. The extraction methods related to these parameters stand as a critical issue for technology characterization, device design and circuit level simulation.

Due to the fact that the SPICE–based MOSFET model is developed from the analytical model for the drain current as a function of terminal voltages which is based on the well–known gradual channel analysis of inversion layer conduction [87], the most common parameters extraction techniques are developed based on the DC current–voltage measurements [88–90]. More recently, several capacitance–voltage techniques [91–93], small signal channel conductance technique [94], and *S*–parameters measurements [95, 96] have been also developed for the parameters extraction.

In the development of submicron MOSFET models, such as BSIM4 [97], the parameters required are classified to several categories: DC–related parameters, AC–related parameters and geometry–related parameters, etc. The DC–related parameters include threshold voltage, mobility degradation coefficients, series resistances, etc. The AC–related parameters include junction model parameters, and overlap capacitance coefficients. The geometry–related parameters include channel length shortening and width narrowing parameters.

Although using DC current–voltage measurements [88]–[90] is the most popular way to

extract the DC–related parameters, the AC–related parameters cannot be obtained at the same time. Besides, the C–V measurement can be used to extract the AC–related parameters and several DC–related parameters (e.g., threshold voltage [91] and effective channel length [98]), but it cannot determine the series resistance [90]. Up to present, the methods using *S*–parameters measurements are aimed at the extraction of parameters of RF small–signal model [99–101] or single parameter of MOSFETs (i.e., effective mobility [96]). However, there is no method published to extract DC–related and AC–related parameters simultaneously by *S*–parameters measurements. Therefore, to develop an extraction method, by using *S*–parameters measurements, accompanying the extraction of AC–related parameters with DC–related parameters is essential.

In this Chapter, a novel and simple method for accurately extracting the threshold voltage V_T, sum of drain and source series resistance R_T, gain factor β_{eff}, and mobility degradation parameters θ_1 and θ_2 [102], [103] utilizing small–signal conductance g_{dsm} between source and drain, as a function of gate bias, extracted from *S*–parameters measurements is proposed. The *S*–parameters measurements of test devices are performed with zero drain bias to eliminate the influences from the drain–bias related effects such as channel length modulation (CLM), drain induced barrier lowering (DIBL), and carrier velocity saturation. In addition, by carrying out the same procedure for devices with different geometries, the effective channel length L_{eff} and inversion layer mobility μ_0 can be also extracted.

This Chapter is organized in the following manners. In Section 6–2, the theory of the proposed parameter extraction method will be described in detail. In Section 6–3, the proposed extraction method is performed on the extraction of threshold voltage, effective channel length, source/drain series resistances, and inversion layer mobility for test devices with different geometries by *S*–parameters measurements. The comparisons of the results obtained by the proposed method and the other one with the experimental data are presented and discussed. The conclusions are summarized in Section 6–4**.**

6–2 Theory of the Extraction Method

In this section, the extraction of small–signal source–drain conductance g_{dsm} by using *S*–parameters measurements is described first. Then, both the MOSFET model adopted by this work, and the parameters extraction method will be presented.

A. Extraction of g_{dsm} from *S*–parameters measurements

Figure 6–1 shows the small–signal equivalent circuit of a MOSFET [107], where R_g, R_s and R_d are series resistances; L_g, L_s and L_d represent the interconnection parasitics. Besides, the parasitics of the pads are modeled by the capacitors C_{pg} and C_{pd} in series with the resistors R_{pg} and R_{pd}, respectively. With the small–signal equivalent circuit shown in Fig. 6–1, g_{dsm}, as a function of gate bias, can be derived directly from the *Z*–parameter data. In this work, the *Z*–parameters of test MOSFETs are obtained from *S*–parameters measurements, after de–embedding the influence of pad parasitics and interconnections, performed at various gate voltages while keeping the drain bias to be zero. Fig. 6–2 shows the equivalent circuit, which is valid for a gate voltage above pinchoff and at zero drain voltage [104–106], where a distributed channel resistance R'_{ch} and a distributed gate capacitance C'_g are used to model the intrinsic device. As mentioned in [104] and [105], the small–signal source–drain conductance determined from the real part of the Z_{22}^{d} (without pads and interconnections parasitics) at low frequency is regarded as the measured data g_{dsm} and expressed as:

$$g_{dsm} = \frac{1}{\mathrm{Re}\left[Z_{22}^{d}\right]_{low\ \ frequency}} = \frac{1}{R_d + 1/g_{ds} + R_s} \qquad (6\text{–}1)$$

where the superscript *d* refers to the *Z*–parameters after de–embedding the influences of pad parasitics and interconnections.

B. Descriptions Of MOSFET Model and Extraction Method

Figure 6–3 shows the schematic circuit model of a MOS transistor, where *g*, *d* and *s* denote the external nodes, while *d'* and *s'* denote the internal nodes. The DC drain current and the small–signal source–drain conductance g_{dsm} (including source/drain series resistance) of a MOS transistor in the linear region can be expressed as follows [89]:

$$\begin{aligned} I_{ds} &= \frac{W_{eff} C_{ox} \mu_{eff}}{L_{eff}} \left[\left(V_{gs} - \frac{1}{2} R_T I_{ds} \right) - V_T - \frac{1}{2} \left(V_{ds} - I_{ds} R_T \right) \right] \cdot \left(V_{ds} - I_{ds} R_T \right) \\ &= \frac{W_{eff} C_{ox} \mu_{eff}}{L_{eff}} \left(V_{gs'} - V_T - \frac{V_{d's'}}{2} \right) \cdot V_{d's'} = \beta_{eff} \left(V_{gs'} - V_T - \frac{V_{d's'}}{2} \right) \cdot V_{d's'}. \end{aligned} \tag{6–2}$$

$$g_{dsm} = \left[\frac{\partial I_{ds}}{\partial V_{ds}} \right]_{fixed\ V_{gs}} = \left[\frac{\partial}{\partial V_{ds}} \left(\frac{W_{eff} C_{ox} \mu_{eff}}{L_{eff}} \left(V_{gs'} - V_T - \frac{V_{d's'}}{2} \right) \cdot V_{d's'} \right) \right]_{fixed\ V_{gs}} \tag{6–3}$$

where W_{eff} and L_{eff} are the effective channel width and length, respectively, C_{ox} is the gate capacitance per unit area, μ_{eff} is the effective inversion layer mobility, β_{eff} is the gain factor, R_T is the sum of source and drain series resistance, V_T is the device threshold voltage, V_{ds} and V_{gs} are external drain–source voltage and gate–source voltage, respectively ($V_{ds} = V_{d's'} + R_T I_{ds}$, $V_{gs} = V_{gs'} + R_T I_{ds}/2$).

In the following extraction procedure, in order to avoid the drain–bias effects mentioned in Section 6–1, zero drain bias is set in the *S*–parameters measurement. This makes the intrinsic channel conductance g_{ds} expressed as:

$$g_{ds} = \left(\frac{W_{eff} C_{ox} \mu_{eff}}{L_{eff}} \left(V_{gs} - V_T \right) \right) = \beta_{eff} \left(V_{gs} - V_T \right). \tag{6–4}$$

In actual small–signal conductance g_{dsm} measurement, the inverse of the measured conductance between source and drain terminals consists of the source/drain series resistances and the inverse of intrinsic channel conductance. Hence, the measured small–signal source–drain

conductance g_{dsm} can be expressed as

$$g_{dsm} = \frac{1}{R_T + \frac{1}{g_{ds}}} = \frac{1}{R_T + \frac{1}{\beta_{eff}\left(V_{gs} - V_T\right)}}. \tag{6–5}$$

In SPICE–based model, the gate–voltage dependent curve of inversion layer mobility μ_{eff} is expressed as follows [102], [103]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1\left(V_{gs} - V_T\right) + \theta_2\left(V_{gs} - V_T\right)^2}. \tag{6–6}$$

where μ_0 is the low field mobility, θ_1 and θ_2 are the mobility degradation parameters [102], [103]. Conventional extraction methods were developed in the past for the case $\theta_2 = 0$ [94]. The approximation $\theta_2 = 0$ implies that the current is always an increasing function of gate voltage. However, in a situation that for a MOSFET with thin oxide thickness, this assumption is incorrect, and the current can decrease at high gate voltages resulting in a negative transconductance [107], [108]. The reason for this effect is attributed to the strong dependence of the carrier mobility on the oxide surface roughness scattering. This mechanism is taken into account by the quadratic mobility dependence of gate voltage via the coefficient θ_2.

By introducing equation (6–6) into equation (6–5), we have the following expression:

$$g_{dsm} = \frac{\beta_0\left(V_{gs} - V_T\right)}{1 + \left(\theta_1 + R_T\beta_0\right)\left(V_{gs} - V_T\right) + \theta_2\left(V_{gs} - V_T\right)^2}. \tag{6–7}$$

where

$$\beta_0 = \frac{W_{eff} C_{ox} \mu_0}{L_{eff}}.$$

Then, inverting equation (6–7) and differentiating once and twice results in the first and second order derivatives, which can be expressed as:

$$\frac{\partial}{\partial V_{gs}}\left(\frac{1}{g_{dsm}}\right)=F_1\left(V_{gs}\right)=\frac{\theta_2}{\beta_0}-\frac{1}{\beta_0}\frac{1}{\left(V_{gs}-V_T\right)^2}. \tag{6–8}$$

$$\frac{\partial^2}{\partial V_{gs}^2}\left(\frac{1}{g_{dsm}}\right)=\frac{2}{\beta_0\cdot\left(V_{gs}-V_T\right)^3}. \tag{6–9}$$

From equation (6–9), the function $F_2(V_{gs})$ can be defined as follows:

$$F_2\left(V_{gs}\right)=\left[\frac{\partial^2}{\partial V_{gs}^2}\left(\frac{1}{g_{dsm}}\right)\right]^{-\frac{1}{3}}=\left(\frac{\beta_0}{2}\right)^{\frac{1}{3}}\cdot\left(V_{gs}-V_T\right). \tag{6–10}$$

From equation (6–10), the fact that the function $F_2(V_{gs})$ is a linear function of V_{gs} which the three parameters θ_1, θ_2 and R_T are eliminated can be used to determine the threshold voltage V_T and parameter β_0. For a given device, by the use of a simple straight–line fit to the numerically derived experimental quantity $(\beta_0/2)^{1/3}(V_{gs}–V_T)$ in the plot of function $F_2(V_{gs})$ versus V_{gs}, the threshold voltage V_T and parameter β_0 can be obtained from the x–axis intercept and slope, respectively.

According to equation (6–8), the threshold voltage V_T and parameter β_0 determined above serves to generate a plot of the function $F_1(V_{gs})$ versus $1/(V_{gs}–V_T)^2$ which can be used to extract the mobility degradation parameter θ_2. The parameter θ_2 can be determined from the y–axis intercept of a best curve–fit of experimental data $F_1(V_{gs})$.

After having threshold voltage V_T, parameters β_0 and θ_2, the two remaining parameters R_T and θ_1 can be determined by optimization to fit equation (6–7) to the measured data g_{dsm}.

By performing the above extraction procedure for devices with several different geometries (i.e., drawn gate width W_{drawn} and drawn gate length L_{drawn}) fabricated by the same technology, the relationship between parameters β_0 and W_{drawn}, and the relationship between parameters $1/\beta_0$ and L_{drawn} can be also obtained [109]. With the standard relationship between drawn gate length and effective gate length: $L_{eff}=(L_{drawn}–\Delta L)$, and the one between drawn gate width and effective gate width: $W_{eff}=(W_{drawn}–\Delta W)$ [90], where ΔL and ΔW are taken as constant in the same technology, the

parameter β_0 can be expressed as:

$$\beta_0 = \frac{(W_{drawn} - \Delta W)}{(L_{drawn} - \Delta L)} \cdot C_{ox} \cdot \mu_0 \qquad (6\text{–}11)$$

From equation (6–11), the plots of parameter β_0 versus W_{drawn} and parameter $1/\beta_0$ versus L_{drawn} can be used to determine the effective values of W and L by linear extrapolation, respectively. From the plot of parameter β_0 versus W_{drawn}, the parameters ΔW can be obtained (with known value of C_{ox}) from the x–axis intercept of the best–fit linear line for the experimental data. With the determined parameter ΔW, the parameters ΔL and μ_0 can be obtained (with known value of C_{ox}) from the x–axis intercept and slope of the best–fit linear line for the experimental data, respectively, from the plot of parameter $1/\beta_0$ versus L_{drawn}.

6–3 Experimental Results and Discussion

The proposed extraction method is applied to determine the parameters of the test devices using S–parameters measurement. S–parameters are measured in the common source–substrate configuration using on–wafer RF probes and an HP 8510C vector network analyzer. The initial calibration is performed on a separate ceramic calibration substrate using a SOLT calibration method. Before the extraction procedure, the parasitic components of input and output pads and interconnections have to be removed. To remove on–wafer pad parasitics, a two–steps de–embedding technique is carried out by subtracting S–parameters of the open pad structure from S–parameters of the measured devices.

The S–parameters measurements for test devices are performed at different gate voltages for zero drain voltage. The small–signal source–drain conductance g_{dsm} is determined from the real part of parameter Z_{22}^{d}, which excludes the parasitics of pads and interconnections by de–embedding technique.

The test devices are *n*–MOSFETs with drawn gate length ranging from 0.35 to 20 μm, drawn gate width ranging from 0.35 to 2 μm, and oxide thickness of 109 Å. All the parameters of the MOSFETs mentioned above are extracted by using equations (6–7)–(6–11).

Figure 6–4 shows the measured data g_{dsm} as a function of gate voltage for different drawn gate lengths. Fig. 6–5 shows the linear plots of $F_2(V_{gs})$ versus V_{gs} for *n*–MOSFETs with several drawn gate lengths. From this figure, the threshold voltage V_T and parameter β_0 can be obtained from the *x*–axis intercept and slope, respectively, of the best–fit straight line of the measured data for each device according to equation (6–10).

Figure 6–6 shows the linear plots of $F_1(V_{gs})$ versus $1/(V_{gs}–V_T)^2$ for devices with different drawn gate lengths. According to equation (6–8), the parameter θ_2 can be determined from the *y*–axis intercept of the best straight–line fit of the measured data for each device.

Figure 6–7 shows the comparison of the threshold voltage, as a function of drawn gate length, obtained by the proposed method, and the one extracted from DC I_d–V_{gs} measurement using linear extrapolation method [90]. In this figure, the error bars show the 97%–confidence intervals of V_T obtained by the present extraction method. The small difference between the values of V_T obtained by these two methods makes the present method become the alternative of determining V_T of MOSFETs in RF applications.

With the extracted threshold voltage V_T, parameters β_0 and θ_2, we determine the two remaining parameters R_T and θ_1 by optimization to fit equation (6–7) to the experimental data g_{dsm} shown in Fig. 6–4.

Next, we make use of the extracted values β_0 of devices with different drawn gate lengths and widths to determine the parameters ΔL, ΔW and μ_0. Figs. 6–8(a) and 6–8(b) show the plots of parameter β_0 versus W_{drawn}, and parameter $1/\beta_0$ versus L_{drawn}, respectively. In Fig. 6–8(a), we determine the parameter ΔW from the *x*–axis intercept of the best–fit straight line for the experimental data β_0. In Fig. 6–8(b), the parameters ΔL and μ_0 are extracted from the *x*–axis intercept and slope of the best–fit straight line for the experimental data $1/\beta_0$.

The extracted values of parameters V_T, R_T, μ_0, θ_1, θ_2, ΔL, ΔW and β_0 for test devices with different drawn lengths are summarized in Table 7. Theoretically, the parameters R_T, θ_1 and θ_2 are independent of gate length. In this work, it is seen to be the case for parameters R_T and θ_1 obtained by the independent parameter optimization on the measured data for different gate lengths, where even if the parameter θ_2 is determined from the measured data, rather than optimization on the measured data.

Figure 6–9 shows the plot of effective inversion layer mobility μ_{eff} versus gate bias V_{gs} for a MOS transistor with W_{drawn}/L_{drawn} = 10 μm/ 0.5 μm. The inset in Fig. 6–9 shows the intrinsic channel conductance g_{ds} as a function of V_{gs} obtained from equation (6–5) with the extracted parameter R_T. Due to the fact that effective inversion layer mobility μ_{eff} is usually extracted from the intrinsic channel conductance g_{ds} directly [90], with the relationship between g_{ds} and gate bias, extracted parameters V_T, R_T, ΔL, ΔW and the known C_{ox}, μ_{eff} is determined through equation (6–4). In Fig. 6–9, it is seen that the extracted μ_{eff} by equation (6–4) has a significant raise with reducing V_{gs} just above V_T. This is attributed to the failure of the approximation of inversion layer charges Q_n using equation: $Q_n = C_{ox}(V_{gs}–V_T)$ while V_{gs} approaches V_T [90]. Besides, according to the SPICE–based mobility model expressed in equation (6–6), μ_{eff} can be also obtained and shown in Fig. 6–9. Since the difference between the two sets of μ_{eff} obtained by equations (6–4) and (6–6) is within 2% in the strong inversion region, the μ_{eff} calculated by equation (6–6) using extracted parameters θ_1 and θ_2 should be a good prediction of actual mobility in this region.

Additionally, the curves of experimental data g_{dsm} as a function of gate voltage V_{gs} is compared to those calculated using equation (6–7) and the extracted parameters. These curves are shown as the solid lines in Fig. 6–10 and a good agreement is obtained over the range of V_{gs} where the experimental g_{dsm} are used in the extraction procedure. In addition, simulated results I_{ds} as a function of gate bias obtained from equation (6–2) with the extracted parameters are compared with the experimental data. The comparison results are shown in Fig. 6–11 for devices with different drawn gate lengths biased at V_{ds} = 0.1 V. In these figures, a good agreement is obtained between the

experimental data and simulated results.

6–4 Conclusions

In summary, a simple and novel method using *S*–parameters measurement has been proposed for the simultaneous extraction of threshold voltage V_T, sum of drain and source series resistance R_T, gain factor β_{eff}, and mobility degradation parameters θ_1 and θ_2 of MOSFETs. In addition, by carrying out the extraction method for devices with different geometries, the effective channel length L_{eff} and width W_{eff} can be also obtained. The proposed method, based on the relationship between small–signal source–drain conductance and gate bias, is shown to provide good agreements to the experimental data. The advantages of this method are the accuracy and simplicity as well as a number of parameters can be obtained by a single measurement, and by using *S*–parameters measurement and avoiding DC drain bias, the influence of drain bias on the extraction of the parameters has been eliminated.

Chapter 7

Conclusions

7–1 Major Contributions of the Thesis

In this thesis, the detailed investigations of fully–depleted SOI MOSFETs are presented. We focus the attention on the development for SOI MOSFET analytical models and the extraction method for the basic device parameters of MOSFETs. In device modeling, the threshold voltage and current–voltage equation in all operation regions for conventional fully–depleted SOI MOSFETs are analyzed. Furthermore, the analytical models of the threshold voltage and subthreshold current for the SOI MOSFETs with halo implants are also developed. In addition, a small–signal MOSFET model and a relevant parameter extraction method are presented for RF applications. These studies are verified by 2–D numerical analysis or demonstrated with the experimental data. The major contributions of the thesis are summarized as follow:

1. With the aid of the Green function technique and the appropriate boundary conditions, the general solutions for the 2–D Poisson equation of the fully–depleted SOI MOSFETs with arbitrarily doped profile has been derived. By using the concept of the average electric filed, the derivation of the analytical threshold voltage model is further simplified. Moreover, a modified factor is introduced to describe the DIBL effect from the source/drain junctions. The analytical threshold voltage model is shown to be in good agreements with the 2–D numerical analysis.
2. To incorporate the DIBL effects into the development of I–V model, a DIBL factor is obtained from the previous analytical threshold voltage model. A complete analytical I–V model of the fully–depleted SOI MOSFETs in all operation regions is presented. Furthermore, the temperature raise model is also incorporated for the temperature related

parameters.

3. For the first time, an analytical 2–D threshold voltage model and a subthreshold current model for the fully–depleted SOI MOSFETs with halo or pocket implants are presented. By the approximation of the potential distribution with parabolic functions and the use of proper boundary conditions, the subthreshold surface potential distribution along the interface of gate oxide and silicon film is obtained. Furthermore, a simple quasi–2D threshold voltage model is developed. Then, with the drift–diffusion current equation, an analytical subthreshold current model is also derived. These derived analytical models have been verified with the numerical analysis and excellent agreements are obtained.
4. A small–signal MOSFET model accounting for the distributed gate resistance, substrate network and nonreciprocal capacitance is presented. By using the feedback theory, the transmission line equation along the gate region is solved with the proper boundary conditions. Then, with the help of the two–port circuit model, the *Y*–parameters of the equivalent small signal circuit are obtained. Moreover, an extraction method is also developed for the relevant parameters of the small signal model. The developed small signal model and parameter extraction method are confirmed by the experimental data with the frequency up to 10 GHz.
5. For the purpose of extracting DC and AC parameters of the MOSFETs at the same time, a device parameter extraction method is developed by using the *S*–parameters measurement at zero drain bias voltage to avoid the drain bias effect. This method includes the extractions of the threshold voltage, effective mobility, series resistance and the geometries of the MOSFETs. In addition, the method has been applied to the experimental data and a good agreement is obtained.

7–2 Proposed Future Researches

1. In the development of the threshold voltage model for advanced fully–depleted SOI MOSFETs, the quantum effect and poly gate depletion effect should be considered. As the thickness of the silicon film decreases, the density of states becomes a staircase function of the energy, making the threshold voltage increase. Therefore, the quantum mechanical effect needs to be taken into account.
2. Although the analytical models of threshold voltage and subthreshold current for the fully–depleted SOI MOSFETs with halo or pocket implants have been proposed, the analytical compact model for the I–V characteristics with the reverse short–channel effect appropriate for all operation regions is lacked. As mentioned in Chapter 4, the process of the halo implantation has some benefits for the device design. Therefore, it is worth to develop an analytical I–V model to account for this effect, and the analytical model can be incorporated into the circuit simulator to obtain the more accurate simulation results.
3. The developed parameter extraction method adopting *S*–parameter measurement is only suited for the devices with gate oxide thickness above 2 nm. As devices are scaled down toward ultra–thin gate oxide thickness, the gate–related leakage current is significant and needed to be considered in the parameter extractions. The extraction error from the simple theory of the perfect gate insulator may underestimate the charge density in the inversion layer and consequently obtain the inaccurate effective mobility. Therefore, it is essential to extend the device parameter extraction method for the devices down to deep submicrometer regimes. Furthermore, it is also essential to obtain the bias dependence of the DC–related parameters, i.e., series resistance, effective geometry.
4. Recently, the long–term reliability of the deep–submicrometer SOI MOS transistors has drawn considerable attention, and it is becoming an important issue as the density of VLSI/ULSI chips increases with the shrinking design rules. With the exception of the threshold voltage shift, the hot–carrier induced interface traps and oxide–trapped charge greatly degrade the I–V characteristics. The future researches include (a) methodology for

modeling the electrical behavior of the transistors with hot–carrier induced damage, (b) analytical models developed for predicting the hot–carrier induced characteristics degradation, i.e., threshold voltage model, mobility model and I–V models.

5. After the small–signal model and relevant parameter extraction method for the MOSFETs are developed, the applications of the small–signal model to the design of the high frequency circuit is essential to prove its feasibility. Furthermore, before implementing into the circuit simulator, we must check the comparison of the model calculation results with the simulation by the current circuit simulator as the SPICE program. Once the prediction achieves the desired accuracy in the near future, the small–signal model may be introduced in a circuit simulator to aid the circuit design.

Appendices

Appendix A: The coefficients of the second–order nonhomogenous differential equations.

The expressions of the coefficients A_i, B_i, C_i, F_i, G_i, and H_i in eq. (4–14) are given as:

$$A_1 = A_2 = A_3 = (-1)\left(\frac{2}{t_{si}^2}\right)\left(3 + \frac{2C_f}{C_{si}}\right)$$

$$B_1 = B_2 = B_3 = \left(\frac{2}{t_{si}^2}\right)\left(3 + \frac{C_b}{C_{si}}\right)$$

$$F_1 = F_2 = F_3 = \left(\frac{2}{t_{si}^2}\right)\left(3 + \frac{C_f}{C_{si}}\right)$$

$$G_1 = G_2 = G_3 = (-1)\left(\frac{2}{t_{si}^2}\right)\left(3 + \frac{2C_b}{C_{si}}\right)$$

$$C_1 = C_3 = \frac{qN_A}{\varepsilon_{si}} + \frac{2}{t_{si}^2}\left(\frac{C_b V'_{SUB,1} - 2C_f V'_{GS,1}}{C_{si}}\right)$$

$$H_1 = H_3 = \frac{qN_A}{\varepsilon_{si}} - \frac{2}{t_{si}^2}\left(\frac{2C_b V'_{SUB,1} - C_f V'_{GS,1}}{C_{si}}\right)$$

$$C_2 = \frac{qN_B}{\varepsilon_{si}} + \frac{2}{t_{si}^2}\left(\frac{C_b V'_{SUB,2} - 2C_f V'_{GS,2}}{C_{si}}\right)$$

$$H_2 = \frac{qN_B}{\varepsilon_{si}} - \frac{2}{t_{si}^2}\left(\frac{2C_b V'_{SUB,1} - C_f V'_{GS,1}}{C_{si}}\right) \qquad \text{(A–1)}$$

Appendix B: Particular solutions $\Psi_{fsp,i}(x)$ and $\Psi_{bsp,i}(x)$, and the constants g_1, g_2, d_1 and d_2 of the general solution.

The expressions of the particular solutions $\Psi_{fsp,i}(x)$ and $\Psi_{bsp,i}(x)$, and the constants g_1, g_2, d_1 and d_2 given in eq. (4–15) are expressed as:

$$\Psi_{fsp,1} = \lambda_1 \cdot V_{GS} + \lambda_2 \cdot V_{SUB} + \lambda_3 = \Psi_{fsp,3}$$

$$\Psi_{fsp,2} = \lambda_1 \cdot V_{GS} + \lambda_2 \cdot V_{SUB} + \lambda_4$$

$$\Psi_{bsp,1} = \lambda_5 \cdot V_{SUB} + \lambda_6 \cdot V_{GS} + \lambda_7 = \Psi_{bsp,3}$$

$$\Psi_{bsp,2} = \lambda_5 \cdot V_{SUB} + \lambda_6 \cdot V_{GS} + \lambda_8$$

$$C_T = \left(\frac{1}{C_{si}} + \frac{1}{C_f} + \frac{1}{C_b}\right)^{-1}$$

$$\lambda_1 = C_T \cdot \left(\frac{1}{C_b} + \frac{1}{C_{si}} \right)$$

$$\lambda_2 = \frac{C_T}{C_f}$$

$$\lambda_3 = \frac{C_T}{C_f} \cdot \left(\frac{1}{C_b} + \frac{1}{2C_{si}} \right) \cdot \left(-qN_A t_{si} \right) - \lambda_1 \cdot \left(V_{fbf,1} + \Psi_{FP,1} \right) - \lambda_2 \cdot \left(V_{fbb,1} + \Psi_{FP,1} \right)$$

$$\lambda_4 = \frac{C_T}{C_f} \cdot \left(\frac{1}{C_b} + \frac{1}{2C_{si}} \right) \cdot \left(-qN_B t_{si} \right) - \lambda_1 \cdot \left(V_{fbf,2} + \Psi_{FP,2} \right) - \lambda_2 \cdot \left(V_{fbb,2} + \Psi_{FP,2} \right)$$

$$\lambda_5 = C_T \cdot \left(\frac{1}{C_f} + \frac{1}{C_{si}} \right)$$

$$\lambda_6 = \frac{C_T}{C_b}$$

$$\lambda_7 = \frac{C_T}{C_b} \cdot \left(\frac{1}{C_f} + \frac{1}{2C_{si}} \right) \cdot \left(-qN_A t_{si} \right) - \lambda_5 \cdot \left(V_{fbb,1} + \Psi_{FP,1} \right) - \lambda_6 \cdot \left(V_{fbf,1} + \Psi_{FP,1} \right)$$

$$\lambda_8 = \frac{C_T}{C_b} \cdot \left(\frac{1}{C_b} + \frac{1}{2C_{si}} \right) \cdot \left(-qN_B t_{si} \right) - \lambda_5 \cdot \left(V_{fbb,2} + \Psi_{FP,2} \right) - \lambda_6 \cdot \left(V_{fbf,2} + \Psi_{FP,2} \right)$$

$$\lambda_9 = d_2 \cdot \left\{ (g_1 - 1) \cdot V_{bi} + \left[g_1 (\lambda_7 - \lambda_8) + (\lambda_4 - \lambda_3) \right] \cdot \cosh(d_2 L_1) + (\lambda_3 - g_1 \lambda_7) \right\}$$

$$\lambda_{10} = d_1 \cdot \left\{ (g_2 - 1) \cdot V_{bi} + \left[g_2 (\lambda_7 - \lambda_8) + (\lambda_4 - \lambda_3) \right] \cdot \cosh(d_1 L_1) + (\lambda_3 - g_2 \lambda_7) \right\}$$

$$\lambda_{11} = d_2 \cdot \left\{ -(g_1 - 1) \cdot (V_{bi} + V_{DS}) + \left[g_1 (\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4) \right] \cdot \cosh(d_2 (L_2 - L)) + (g_1 \lambda_7 - \lambda_3) \right\}$$

$$\lambda_{12} = d_1 \cdot \left\{ -(g_2 - 1) \cdot (V_{bi} + V_{DS}) + \left[g_2 (\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4) \right] \cdot \cosh(d_1 (L_2 - L)) + (g_2 \lambda_7 - \lambda_3) \right\}$$

$$g_1 = (-1) \frac{\frac{\varepsilon_{ox}}{\varepsilon_{si}} \left(\frac{1}{t_f} - \frac{1}{t_b} \right) + \sqrt{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \left(\frac{1}{t_f} - \frac{1}{t_b} \right)^2 + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \frac{1}{t_f t_b} + \frac{9}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{3}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right)}}{\frac{3}{t_{si}} + \frac{C_f}{\varepsilon_{si}}}$$

$$g_2 = (-1) \frac{\frac{\varepsilon_{ox}}{\varepsilon_{si}} \left(\frac{1}{t_f} - \frac{1}{t_b} \right) - \sqrt{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \left(\frac{1}{t_f} - \frac{1}{t_b} \right)^2 + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \frac{1}{t_f t_b} + \frac{9}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{3}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right)}}{\frac{3}{t_{si}} + \frac{C_f}{\varepsilon_{si}}}$$

$$d_1 = \left[\frac{6}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{2}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right) + \frac{2}{t_{si}} \sqrt{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \left(\frac{1}{t_f} - \frac{1}{t_b} \right)^2 + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \frac{1}{t_f t_b} + \frac{9}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{3}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right)} \right]^{1/2}$$

$$d_2 = \left[\frac{6}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{2}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right) - \frac{2}{t_{si}} \sqrt{\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \left(\frac{1}{t_f} - \frac{1}{t_b} \right)^2 + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \right)^2 \frac{1}{t_f t_b} + \frac{9}{t_{si}^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \cdot \frac{3}{t_{si}} \left(\frac{1}{t_f} + \frac{1}{t_b} \right)} \right]^{1/2}$$

(B–1)

Appendix C: The coefficients of the analytical solution of the surface potential.

The expressions of the coefficients a_{i1}, a_{i2}, a_{i3} and a_{i4} of the surface potential solution in the region i given in eq. (4–15) are presented as:

$$a_{11} = \alpha_1 \cdot V_{GS} + \alpha_2 \cdot V_{SUB} + \alpha_3$$
$$a_{12} = \alpha_4 \cdot V_{GS} + \alpha_5 \cdot V_{SUB} + \alpha_6$$
$$a_{13} = \alpha_7 \cdot V_{GS} + \alpha_8 \cdot V_{SUB} + \alpha_9$$
$$a_{14} = \alpha_{10} \cdot V_{GS} + \alpha_{11} \cdot V_{SUB} + \alpha_{12}$$
$$\alpha_1 = \frac{(g_2\lambda_6 - \lambda_1)\cdot\left(e^{-d_1 L} - 1\right)}{2\cdot(g_2 - g_1)\cdot\sinh(d_1 L)}$$
$$\alpha_2 = \frac{(g_2\lambda_5 - \lambda_2)\cdot\left(e^{-d_1 L} - 1\right)}{2\cdot(g_2 - g_1)\cdot\sinh(d_1 L)}$$
$$\alpha_3 = \frac{1}{2(g_2 - g_1)\cdot\sinh(d_1 L_1)}\cdot\left\{e^{-d_1 L_1}\cdot\left[g_2\lambda_7 - \lambda_3 - (g_2 - 1)\cdot V_{bi}\right] + g_2(\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4)\right.$$
$$\left. + (-1)\cdot\frac{\left[\lambda_{10}\cdot\sinh(d_1\cdot(L_1 - L)) + \lambda_{12}\cdot\sinh(d_1 L_1)\right]}{d_1\sinh(d_1 L)}\right\}$$
$$\alpha_4 = \frac{(\lambda_1 - g_2\lambda_6)\cdot\left(e^{d_1 L} - 1\right)}{2\cdot(g_2 - g_1)\cdot\sinh(d_1 L)}$$
$$\alpha_5 = \frac{(\lambda_2 - g_2\lambda_5)\cdot\left(e^{d_1 L} - 1\right)}{2\cdot(g_2 - g_1)\cdot\sinh(d_1 L)}$$
$$\alpha_6 = \frac{(-1)}{2(g_2 - g_1)\cdot\sinh(d_1 L_1)}\cdot\left\{e^{d_1 L_1}\cdot\left[g_2\lambda_7 - \lambda_3 - (g_2 - 1)\cdot V_{bi}\right] + g_2(\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4)\right.$$
$$\left. + (-1)\cdot\frac{\left[\lambda_{10}\cdot\sinh(d_1\cdot(L_1 - L)) + \lambda_{12}\cdot\sinh(d_1 L_1)\right]}{d_1\sinh(d_1 L)}\right\}$$
$$\alpha_7 = \frac{(g_1\lambda_6 - \lambda_1)\cdot\left(e^{-d_2 L} - 1\right)}{2\cdot(g_1 - g_2)\cdot\sinh(d_2 L)}$$
$$\alpha_8 = \frac{(g_1\lambda_5 - \lambda_2)\cdot\left(e^{-d_2 L} - 1\right)}{2\cdot(g_1 - g_2)\cdot\sinh(d_2 L)}$$
$$\alpha_9 = \frac{1}{2(g_1 - g_2)\cdot\sinh(d_2 L_1)}\cdot\left\{e^{-d_2 L_1}\cdot\left[g_1\lambda_7 - \lambda_3 - (g_1 - 1)\cdot V_{bi}\right] + g_1(\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4)\right.$$
$$\left. + (-1)\cdot\frac{\left[\lambda_9\cdot\sinh(d_2\cdot(L_1 - L)) + \lambda_{11}\cdot\sinh(d_2 L_1)\right]}{d_2\sinh(d_2 L)}\right\}$$
$$\alpha_{10} = \frac{(\lambda_1 - g_1\lambda_6)\cdot\left(e^{d_2 L} - 1\right)}{2\cdot(g_1 - g_2)\cdot\sinh(d_2 L)}$$
$$\alpha_{11} = \frac{(\lambda_2 - g_1\lambda_5)\cdot\left(e^{d_2 L} - 1\right)}{2\cdot(g_1 - g_2)\cdot\sinh(d_2 L)}$$

$$\alpha_{12} = \frac{(-1)}{2(g_1 - g_2)\cdot\sinh(d_2 L_1)}\cdot\left\{e^{d_2 L_1}\cdot\left[g_1\lambda_7 - \lambda_3 - (g_1 - 1)\cdot V_{bi}\right] + g_1(\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4)\right.$$
$$\left. + (-1)\cdot\frac{\left[\lambda_9\cdot\sinh(d_2\cdot(L_1 - L)) + \lambda_{11}\cdot\sinh(d_2 L_1)\right]}{d_2\sinh(d_2 L)}\right\}$$

$$a_{21} = \delta_1\cdot V_{GS} + \delta_2\cdot V_{SUB} + \delta_3$$
$$a_{22} = \delta_4\cdot V_{GS} + \delta_5\cdot V_{SUB} + \delta_6$$
$$a_{23} = \delta_7\cdot V_{GS} + \delta_8\cdot V_{SUB} + \delta_9$$
$$a_{24} = \delta_{10}\cdot V_{GS} + \delta_{11}\cdot V_{SUB} + \delta_{12}$$

$$\delta_1 = \frac{(g_2\lambda_6 - \lambda_1)\cdot(1 - e^{-d_1 L})}{2(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_2 = \frac{(g_2\lambda_5 - \lambda_2)\cdot(1 - e^{-d_1 L})}{2(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_3 = \frac{\lambda_{12} + \lambda_{10}\cdot e^{-d_1 L}}{2d_1(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_4 = -\frac{(g_2\lambda_6 - \lambda_1)\cdot(1 - e^{d_1 L})}{2(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_5 = -\frac{(g_2\lambda_5 - \lambda_2)\cdot(1 - e^{d_1 L})}{2(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_6 = \frac{\lambda_{12} + \lambda_{10}\cdot e^{d_1 L}}{2d_1(g_1 - g_2)\cdot\sinh(d_1 L)}$$
$$\delta_7 = \frac{(g_1\lambda_6 - \lambda_1)\cdot(1 - e^{-d_2 L})}{2(g_2 - g_1)\cdot\sinh(d_2 L)}$$
$$\delta_8 = \frac{(g_1\lambda_5 - \lambda_2)\cdot(1 - e^{-d_2 L})}{2(g_2 - g_1)\cdot\sinh(d_2 L)}$$
$$\delta_9 = \frac{\lambda_{11} + \lambda_9\cdot e^{-d_2 L}}{2d_2(g_2 - g_1)\cdot\sinh(d_2 L)}$$
$$\delta_{10} = -\frac{(g_1\lambda_6 - \lambda_1)\cdot(1 - e^{d_2 L})}{2(g_2 - g_1)\cdot\sinh(d_2 L)}$$
$$\delta_{11} = -\frac{(g_1\lambda_5 - \lambda_2)\cdot(1 - e^{d_2 L})}{2(g_2 - g_1)\cdot\sinh(d_2 L)}$$
$$\delta_{12} = \frac{\lambda_{11} + \lambda_9\cdot e^{d_2 L}}{2d_2(g_2 - g_1)\cdot\sinh(d_2 L)}$$

$$a_{31} = \frac{1}{(g_2 - g_1)\cdot\left(e^{d_1(L_2 - 2L)} - e^{-d_1 L_2}\right)}\cdot\left\{(-1)\cdot\left[(g_2 - 1)(V_{bi} + V_{DS}) - g_2\Psi_{bsp,3} + \Psi_{fsp,2}\right]\cdot e^{-d_1(L_2 + L)}\right.$$
$$\left. + (g_2 - g_1)\cdot e^{-2d_1 L}\left(b_1 e^{d_1 L_2} + b_2 e^{-d_1 L_2}\right) + \left[g_2(\lambda_8 - \lambda_7) + (\lambda_3 - \lambda_4)\right]\cdot e^{-2d_1 L}\right\}$$

$$a_{32}=\frac{1}{(g_2-g_1)\cdot\left(e^{d_1(L_2-2L)}-e^{-d_1L_2}\right)}\cdot\left\{\left[(g_2-1)(V_{bi}+V_{DS})-g_2\Psi_{bsp,3}+\Psi_{fsp,2}\right]\cdot e^{d_1(L_2-L)}\right.$$
$$\left.-(g_2-g_1)\cdot\left(b_1e^{d_1L_2}+b_2e^{-d_1L_2}\right)+\left[g_2(\lambda_7-\lambda_8)+(\lambda_4-\lambda_3)\right]\right\}$$
$$a_{33}=\frac{1}{(g_1-g_2)\cdot\left(e^{d_2(L_2-2L)}-e^{-d_2L_2}\right)}\cdot\left\{(-1)\cdot\left[(g_1-1)(V_{bi}+V_{DS})-g_1\Psi_{bsp,3}+\Psi_{fsp,2}\right]\cdot e^{-d_2(L_2+L)}\right.$$
$$\left.+(g_1-g_2)\cdot e^{-2d_2L}\left(b_3e^{d_2L_2}+b_4e^{-d_2L_2}\right)+\left[g_1(\lambda_8-\lambda_7)+(\lambda_3-\lambda_4)\right]\cdot e^{-2d_2L}\right\}$$
$$a_{34}=\frac{1}{(g_1-g_2)\cdot\left(e^{d_2(L_2-2L)}-e^{-d_2L_2}\right)}\cdot\left\{\left[(g_1-1)(V_{bi}+V_{DS})-g_1\Psi_{bsp,3}+\Psi_{fsp,2}\right]\cdot e^{d_2(L_2-L)}\right.$$
$$\left.-(g_1-g_2)\cdot\left(b_3e^{d_2L_2}+b_4e^{-d_2L_2}\right)+\left[g_1(\lambda_7-\lambda_8)+(\lambda_4-\lambda_3)\right]\right\}$$

(C–1)

REFERENCES

[1] J. R. Brews, W. Fichtner, E. H. Nicolllian and S. M. Sze, “Generalized guide to MOSFET miniaturization,” *IEEE Electron Device Lett.*, vol. EDL–1, no. 1, p.2, Jan. 1980.

[2] K. K. Ng, S. A. Eshraghi and T. D. Stanik, “An improved generalized guide for MOSFET scaling,” *IEEE Trans. Electron Devices*, vol. ED–40, no. 10, p. 1895. Oct. 1993.

[3] T. Yuan and E. J. Nowak, “CMOS devices below 0.1 μm: how high will performance go?,” *Proceedings of IEEE International Electron Devices Meeting*, 1997, p. 215. Dec. 1997.

[4] T. H. Ning, “Silicon VLSI trends – what else besides scaling CMOS to its limit?,” in *Physical and Failure Analysis of Integrated Circuits, 2003. Proceedings of the 10th International Symposium.*, p. 7. July. 2003.

[5] T. H. Ning, “Future silicon technology trends from a system application perspective,” in *VLSI Technology, Systems, and Applications, 2003 International Symposium.*, p. 121. Oct. 2003.

[6] F. Monsieur, E. Vincent and D. Roy, “A thorough investigation of progressive breakdown in ultra–thin oxide. Physical understanding and application for industry reliability assessment,” in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, p. 0_3, April. 2004.

[7] C. Claeys, “Technological challenges of advanced CMOS processing and their impact on design aspects,” in *VLSI Design, 2004. Proceedings. 17th International Conference.*, p. 275. Jan. 2004.

[8] A. Agarwal and H. Gossmann, “Ultra–shallow junctions for novel device architectures beyond 65 nm node,” in *Junction Technology, 2004. IWJT '04. The Fourth International Workshop*., p. 335. Mar. 2004.

[9] O. Wang, Z. Zhang, K Li, L. Guo, X. Wu and Z. Wang, “A deep trench isolation for silicon,” in *Solid–State and Integrated Circuit Technology, 1998. Proceedings. 1998 5th International*

Conference., p. 172. Oct. 1998.

[10] R. R. Troutman, *Latchup in CMOS Technology*, Kluwer Academic Publishers: Boston, 1998.

[11] B. Davari, R. H. Dennard and G. G. Shahidi, "CMOS scaling for high performance and low power–the next ten years," in *Proceedings of the IEEE*, vol. 83, no. 4, p. 595, Apr. 1995.

[12] S. T. Liu, J. Yue and J. Schrankler, "Screening SOI substrates for radiation resistant space electronics application," in *SOI Conference, 1997. Proceedings., 1997 IEEE International.*, p. 7, Oct. 1997.

[13] G. Shahidi, A. Aimera, F. Assaderaghi, R. J. Bolam, E. Leobandung, W. Rausch, D. Sankus, D. Schepis, L. F. Wagner, K. Wu and B. Davari, "Partially–depleted SOI technology for digital logic," in *Solid–State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International.*, p. 426, Feb. 1999.

[14] J. S. Brodsky, R. M. Fox, D. T. Zweidinger and S. Veeraraghavan, "A physics–based, dynamic thermal impedance model for SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. ED–44, no. 6, p. 957, Jun. 1997.

[15] V. P. Trivedi and J. G. Fossum, "Scaling fully depleted SOI CMOS," *IEEE Trans. Electron Devices*, vol. ED–50, no. 10, p. 2095, Oct. 2003.

[16] A. Vandooren, D. Jovanovic, S. Egley, M. Sadd, B. Y. Nguyen, B. White, M. Orlowski and J. Mogab, "Scaling assessment of fully–depleted SOI technology at the 30 nm gate length generation," in *SOI Conference, 2002. Proceedings., 2002 IEEE International.*, p. 25, Oct. 2002.

[17] R. Zhang and K. Roy, "Low–power high–performance double–gate fully depleted SOI circuit design," *IEEE Trans. Electron Devices*, vol. ED–49, no. 10, p. 852, May. 2002.

[18] T. Ohno, Y. Kado, M. Harada and T. Tsuchiya, "Experimental 0.25–μm–gate fully depleted CMOS/SIMOX process using a new two–step LOCOS isolation technique," *IEEE Trans. Electron Devices*, vol. ED–42, no. 8, p. 1481, Aug. 1995.

[19] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R.

Rios and R. Chau, “High performance fully–depleted tri–gate CMOS transistors,” *IEEE Electron Device Lett.*, vol. EDL–24, no. 4, p.263, Apr. 2004.

[20] R. J. Luyken, M. Stadele, W. Rosner, T. Schulz, J. Hartwich, L. Dreeskornfeld and L. Risch, “Perspectives of fully–depleted SOI transistors down to 20nm gate length,” in *SOI Conference, 2002. Proceedings., 2002 IEEE International.*, p. 137, Oct. 2002.

[21] A. J. Auberton-Herve, J. M. Lamure, T. Berrge, M. Bruel, B. Aspar and J. L. Pelloie, “SOI materials for ULSI applications,” *Semiconductor International*, p. 97, Oct. 1995.

[22] M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada and H. Tango, “Two–dimensional simulation and measurement of high–performance MOSFETs made on a very thin SOI film,” *IEEE Trans. Electron Devices*, vol. ED–36, no. 3, p. 493, Mar. 1989.

[23] J. P. Colinge, “Thin-film SOI technology: the solution to many submicron CMOS problems,” in *Electron Devices Meeting, 1989. IEDM Technical Digest. International*, p. 817, Dec. 1989.

[24] H. O. Joachim, Y. Yamaguchi, K. Ishikawa, Y. Inoue and T. Nishimura, “Simulation and two–dimensional analytical modeling of subthreshold slope in ultrathin–film SOI MOSFETs down to 0.1 μm gate length,” *IEEE Trans. Electron Devices*, vol. ED–40, no. 10, p. 1812, Oct. 1993.

[25] J. P. Colinge, *Silicon‐on‐Insulator Technology: Materials to VLSI*, Kluwer Academic Publishers: Boston, 1996.

[26] T. Ohno, “Total-dose effects of gamma-ray irradiation on CMOS/SIMOX devices,” *IEEE Circuit and Device Magazine*, vol. 3, p. 21, Nov. 1987.

[27] K. K. Young, “Short–channel effect in fully depleted SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. ED–36, no. 2, p. 399, Feb. 1989.

[28] S. Veeraraghavan and J. G. Fossum, “Short–channel effects in SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. ED–36, no. 3, p. 522, Mar. 1989.

[29] J. C. S. Woo, K. W. Terrill and P. K. Vasudev, “Two–dimensional analytic modeling of very thin SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. ED–37, no. 9, p. 1999, Sep. 1990.

[30] J. Y. Guo and C. Y. Wu, “A new 2–D analytic threshold–voltage model for fully depleted short–channel SOI MOSFET's,” *IEEE Trans. Electron Devices*, vol. ED–40, no. 9, p. 1653, Sep. 1993.

[31] J. D. Jackson, *Classical Electrodynamics*, McGraw‐Hill Publisher: New York, 1998.

[32] *MEDICI*, V4.0, 1998 Tech. Rep., Technology Modeling Associates, Inc., Palo Alto, CA.

[33] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen and M. Chan, “Threshold voltage model for deep–submicrometer fully depleted SOI MOSFET's,” *IEEE Trans. Electron Devices*, vol. ED–42, no. 11, p. 1949, Nov. 1995.

[34] K. E. Goodson and M. I. Flik, “Effect of microscale thermal conduction on the packing limit of silicon–on–insulator electronic devices,” *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol. 15, no. 5, p. 715, Oct. 1992.

[35] L. J. McDaid, S. Hall, P. H. Mellor, W. Eccleston and J. C. Alderman, “Physical origin of negative differential resistance in SOI transistors,” *Electronics Letters*, vol. 25, no. 13, p. 827, Jun. 1989.

[36] T. C. Hsiao, N. A. Kistler and J. C. S. Woo, “Modeling the I–V characteristics of fully depleted submicrometer SOI MOSFET's,” *IEEE Electron Device Lett.*, vol. EDL–15, no. 2, p.45, Feb. 1994.

[37] M. C. Hu, S. L. Jang, Y. S. Chen, S. S. Liu and J. M. Lin, “An analytical fully‐depleted silicon‐on‐insulator metal‐oxide‐semiconductor field‐effect‐transistor model considering the effects of self‐heating, source/drain resistance, impact‐ionization, and parasitic bipolar junction transistor,” *Japanese Journal of Applied Physics*, vol. 36, no. 5A, p. 2606, May. 1997.

[38] B. Iniguez, L. F. Ferreira, B. Gentinne and D. Flandre, “A physically–based C∞–continuous fully–depleted SOI MOSFET model for analog applications,” *IEEE Trans. Electron Devices*, vol. ED–43, no. 4, p. 568, Apr. 1996.

[39] G. S. Huang and C. Y. Wu**,** “An analytic saturation model for drain and substrate currents of

conventional and LDD MOSFETs," *IEEE Trans. Electron Devices*, vol. ED–37, no. 7, p. 1667, Jul. 1990.

[40] C. Y. Wu and Y. W. Daih, "An accurate mobility model for the I-V characteristics of n-channel enhancement-mode mosfets with single-channel boron implantation," *Solid-State Electrons*, vol. 28, p.1271, Dec. 1985.

[41] P. Antognetti, D. D. Caviglia and E. Profumo**,** "CAD model for threshold and subthreshold conduction in MOSFETs," *IEEE J. Solid – State Circuits*, vol. 17, no. 3, p. 454, Jun. 1982.

[42] Y. G. Chen, J. B. Kuo, Z. Yu, and R. W. Dutton, "An analytical drain current mdel for short-channel fully-depleted ultra-thin silicon-on-insulator nmos devices," *Solid-State Electrons*, vol. 38, p. 2051, Dec. 1995.

[43] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons: New York, 1981.

[44] D. Sharma, J. Gautier and G. Merckel, "A high–voltage circuit for driving liquid–crystal displays," *IEEE J. Solid – State Circuits*, vol. 13, no. 3, p. 378, Jun. 1978.

[45] R. Howes, W. R. White, K. G. Nichlos, P. J. Mole, M. J. Robinson and S. Bird, "An SOS MOSFET model based on calculation of the surface potential," *IEEE Trans. Computer – Aided Design*, vol. 13, no. 4, p. 494, Apr. 1994.

[46] S. R. Banna, P. C. H. Chan, M. Chan and P. K. Ko, **"**A physically based compact device model for fully depleted and nearly fully depleted SOI MOSFET," *IEEE Trans. Electron Devices*, vol. ED–43, no. 11, p. 1914, Nov. 1996.

[47] Y. Cheng and T. A. Fjeldly, "Unified physical I-V model of fully-depleted SOI/MOSFETs for analog/digital circuit simulation," *Solid-State Electrons*, vol. 39, p. 721, May. 1996.

[48] J. R. Davis, G. A. Armstrong, N. J. Thomas and A. Doyel, **"**Thin–film SOI CMOS transistors with p^+–polysilicon gates," *IEEE Trans. Electron Devices*, vol. ED–38, no. 1, p. 32, Jan. 1991.

[49] Y. G. Chen, S Y. Ma, J. B. Kuo, Z. Yu and R. W. Dutton, "An analytical drain current model considering both electron and lattice temperatures simultaneously for deep submicron ultrathin SOI NMOS devices with self–heating," *IEEE Trans. Electron Devices*, vol. ED–42,

no. 5, p. 899, May. 1995.

[50] C. Min, T. Kamins, P. V. Voorde, C. Diaz and W. Greene, "0.18–μm fully–depleted silicon–on–insulator MOSFETs," *IEEE Electron Device Lett.*, EDL–18, no. 6, p. 251, Jun. 1997.

[51] K. Imai, H. Onishi, K. Yamaguchi, K. Inoue, Y. Matsubara, A. Ono and T. Horiuchi, "A 0.18 μm fully–depleted CMOS on 30 nm thick SOI for sub–1.0 V operation," in *VLSI Technology, 1998. Digest of Technical Papers. 1998 Symposium on.*, p. 116, June. 1998.

[52] J. Chen, B. Maiti, D. Connelly, M. Mendicino. F. Huang, O. Adetutu, Y. Yu, D. Weddington, W. Wu, J. Candelaria, D. Dow, P. Tobin and J. Mogab, "0.18 μm metal gate fully–depleted SOI MOSFETs for advanced CMOS applications," in *VLSI Technology, 1999. Digest of Technical Papers. 1999 Symposium on.*, p. 25, June. 1999.

[53] J. –P. Coling, "Thin–film SOI technology: The solution to many submicron CMOS problems," in *Electron Devices Meeting, 1989. IEDM Technical Digest. International*, p. 817, Dec. 1989.

[54] T. Hori, "A 0.1–μm CMOS technology with tilt–implanted punchthrough stopper (TIPS)," in *Electron Devices Meeting, 1994. IEDM Technical Digest. International*, p. 75, Dec. 1994.

[55] B. Yu, H. Wang, O. Milic, Q. Xiang, W. Wang, J. X. An and M. R. Lin, "50 nm gate–length CMOS transistor with super–halo: design, process, and reliability," in *Electron Devices Meeting, 1999. IEDM Technical Digest. International*, p. 653, Dec. 1999.

[56] K. M. Cao, W. Liu, X. Jin, K. Vashanth, K. Greek, J. Krick, T. Vrotsos and C. Hu, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," in *Electron Devices Meeting, 1999. IEDM Technical Digest. International*, p. 171, Dec. 1999.

[57] A. Chatterjee, K. Vasanth, D. T. Grider, M. Nandakumar, G. Pollack, R. Aggarwal, M. Rodder and H. Shichijo, "Transistor design issues in integrating analog functions with high performance digital CMOS," in *VLSI Technology, 1999. Digest of Technical Papers. 1999 Symposium on.*, p. 147, June. 1999.

[58] S. Pidin and M. Koyanagi, “Two–dimensional analytical subthreshold model and optimal scaling of fully–depleted SOI MOSFET down to 0.1 μm channel length,” *Japanese Journal of Applied Physics*, vol. 36, no. 3B, p. 1497, Mar. 1997.

[59] V. H. Meer and K. D. Meyer, “A 2–D analytical threshold voltage model for fully–depleted SOI MOSFETs with Halos or pockets,” *IEEE Trans. Electron Devices*, vol. ED–48, no. 10, p. 2292, Oct. 2001.

[60] P. S. Lin and C. Y. Wu, “A new approach to analytically solving the 2 – D Poisson’s equation and its application in short channel MOSFET modeling,” *IEEE Trans. Electron Devices*, vol. ED–34, no. 9, p. 1947, Sep. 1987.

[61] S. P. Chin and C. Y. Wu, “A new two–dimensional model for the potential distribution of short gate–length MESFETs and its applications,” *IEEE Trans. Electron Devices*, vol. ED–39, no. 8, p. 1928, Aug. 1992.

[62] E. Kreyszig, *Advanced Engineering Mathematics*, John Wiley & Sons: New York, 1983.

[63] T. A. Fjeldly and M. Shur, “Threshold voltage modeling and the subthreshold regime of operation of short–channel MOSFETs,” *IEEE Trans. Electron Devices*, vol. ED–40, no. 1, p. 137, Jan. 1993.

[64] R. Gwoziecki, T. Skotnicki, P. Bouillon and P. Gentil, “Optimization of V_{th} roll–off in MOSFET's with advanced channel architecture–retrograde doping and pockets,” *IEEE Trans. Electron Devices*, vol. ED–46, no. 7, p. 1551, Jul. 1999.

[65] L. E. Larson, “Integrated circuit technology options for RFIC’s – Present status and future directions,” *IEEE J. Solid – State Circuits*, vol. 33, no. 3, p. 387, Mar. 1998.

[66] A. A. Abidi, “Low–power radio–frequency ICs for portable communications,” in *Proceedings of the IEEE*, vol. 83, no. 4, p. 544, Apr. 1995.

[67] C. Enz, “An MOS transistor model for RF IC design valid in all region of operation,” *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 1, p. 342, Jan. 2002.

[68] R. Vanoppen, J. Geelen and D. Klaassen, “The high – frequency analogue performance of

MOSFET's," in *Electron Devices Meeting, 1994. IEDM Technical Digest. International*, p. 173, Dec. 1994.

[69] G. Dambrine, A. Cappy, F. Heliodore and E. Playez, "A new method for determining the FET small‐signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 7, p. 1151, Jul. 1988.

[70] P. Vandeloo and W. Sansen, "Modeling of the MOS transistor for high frequency analog designs," *IEEE Trans. Computer‐Aided Design*, vol. 8, no. 7, p. 713, Jul. 1989.

[71] J.‐J. Ou, X. Jin, I. Ma, C. Hu and P. Gray, "CMOS RF modeling for GHz communication IC's," in *VLSI Technology, 1998. Digest of Technical Papers. 1999 Symposium on.*, p. 94, June. 1998.

[72] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal and J. P. Matta, "RF MOSFET modeling accounting for distributed substrate and channel resistances with emphasis on the BSIM3v3 SPICE model," in *Electron Devices Meeting, 1997. IEDM Technical Digest. International*, p. 309, Dec. 1997.

[73] S. F. Tin, A. A. Osman, K. Mayaram and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design," *IEEE J. Solid‐State Circuits*, vol. 35, no. 4, p. 612, Apr. 2000.

[74] E. Abou‐Allam and T. Manku, "A small‐signal MOSFET model for radio frequency IC applications," *IEEE Trans. Computer‐Aided Design*, vol. 16, no. 5, p. 437, May. 1997.

[75] A. Pascht, M. Grozing, D. Wiegne and M. Berroth, "Small‐signal and temperature noise model for MOSFETs," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 8, p. 1927, Aug. 2002.

[76] T. Manku, "Microwave CMOS‐device physics and designs," *IEEE J. Solid‐State Circuits*, vol. 34, no.5, p. 277, May. 1999.

[77] C. H. Kim, C. S. Kim, H. Y. Yu and K. S. Nam, "Unique extraction of substrate parameters of common‐source MOSFETs," *IEEE Microwave Guided Wave Lett.,* vol. 9, no. 3, p. 108, Mar.

1999.

[78] R. Sung, P. Bendix and M. B. Das, “Extraction of high‐frequency equivalent circuit parameters of submicron gate‐length MOSFET’s,” *IEEE Trans. Electron Devices*, vol. ED–45, no.8, p. 1769, Aug. 1998.

[79] M. Berroth and R. Bosch, “Broad‐Band determination of the FET small‐signal equivalent circuit,” *IEEE Trans. Microwave Theory Tech.*, vol. 38, no. 7, p. 891, Jul. 1990.

[80] Y. Tsividis, *The Operation and Modeling of the MOS Transistor*, McGraw‐Hill: New York, 1999.

[81] S. Lee, H. K. Yu, C. S. Kim, J. G. Koo and K. S. Nam, “A novel approach to extracting small–signal model parameters of silicon MOSFET's” *IEEE Microwave Guided Wave Lett.,* vol. 7, no. 3, p. 75, Mar. 1997.

[82] D. Lovelace, J. Costa and N. Camilleri, “Extracting small–signal model parameters of silicon MOSFET transistors,” in *1994 IEEE MTT‐S International Microwave Symposium Digest*, vol. 2, no. 6, p. 865, 1994.

[83] M. Je and H. Shin, “Gate bias dependence of the substrate signal coupling effect in RF MOSFETs,” *IEEE Electron Device Lett.*, vol. EDL–24, no. 3, p.183, Mar. 2003.

[84] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons: New York, 1993.

[85] M. Koolen, J. Geelen and M. Versleijen, “An improved de‐embedding technique for on‐wafer high‐frequency characterization,” In: *1991 IEEE Bipolar Circuit and Technology Meeting*, p. 188, 1991. .

[86] Y. Cheng and M. Matloubian, “On the high–frequency characteristics of substrate resistance in RF MOSFETs,” *IEEE Electron Device Lett.*, vol. EDL–21, no. 12, p.604, Dec. 2000.

[87] H. C. Pao and C. T. Sah, “Effects of diffusion current on characteristics of metal‐oxide (insulator)‐semiconductor transistors,” *Solid‐State Electron*., vol. 9, p. 927, Oct. 1966.

[88] K. K. Ng and J. R. Brews, “Measuring the effective channel length of MOSFETs,” *IEEE*

Circuit Device Mag., vol. 6, p. 33, Nov. 1990.

[89] C. C. McAndrew and P. A. Layman, "MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization," *IEEE Trans. Electron Devices*, vol. ED–39, no. 10, p. 2298, Oct. 1992.

[90] D. K. Schroder, *Semiconductor Material and Device Characterization*, Wiley: New York, 1998.

[91] M. M. Lau, C. Y. T. Chiang, Y. T. Yeow, and Z. Q. Yao, "A new method of threshold voltage extraction via MOSFET gate‐to‐substrate capacitance measurement," *IEEE Trans. Electron Devices*, vol. ED–48, no. 8, p. 1742, Aug. 2001.

[92] S. W. Lee, "A capacitance‐based method for experimental determination of metallurgical channel length of submicron LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED–41, no. 3, p. 403, Mar. 1994.

[93] B. J. Sheu and P. K. Ko, "A capacitance method to determine the channel lengths for conventional and LDD MOSFETs," *IEEE Electron Device Lett.*, vol. EDL–5, no. 11, p. 491, Nov. 1984.

[94] F. C. J. Kong, Y. T. Yeow, Z. Q. Yao, "Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small‐signal channel conductance measurement," *IEEE Trans. Electron Devices*, vol. ED–48, no. 12, p. 2870, Dec. 2001.

[95] S. Lee and H. K. Yu, "A semianalytical parameter extraction of a SPICE BSIM3v3 for RF MOSFET's using S‐parameters," *IEEE Trans. Microwave Theory Tech*, vol. 48, no. 3, p. 412, Mar. 2000.

[96] S. Lee and H. K. Yu, "A new method to determine channel mobility model parameters in submicron MOSFET's using measured S‐parameters," in *IEEE Conf. Simulation of Semiconductor Processes and Devices*., p. 253, Sept. 2000.

[97] *BSIM4 Version 3.0 Manual*, Department of Electrical Engineering and Computer Sciences,

University of California, Berkeley, CA. 2003.

[98] J. C. Guo, S. S. Chung, and C. H. Hsu, "A new approach to determine the effective channel length and the drain – and – source series resistance of miniaturized MOSFET's," *IEEE Trans. Electron Devices*, vol. ED–41, no. 10, p. 1811, Oct. 1994.

[99] R. Sung, P. Bendix, and M. B. Das, "Extraction of high – frequency equivalent circuit parameters of submicron gate – length MOSFET's," *IEEE Trans. Electron Devices*, vol. ED–45, no. 8, p. 1769, Aug. 1998.

[100] J. Han, M. Je, and H. Shin, "A simple and accurate method for extracting substrate resistance of RF MOSFETs," *IEEE Electron Device Lett.*, vol. EDL–23, no. 7, p. 434, July. 2002.

[101] Y. Cheng and M. Matloubian, "Parameter extraction of accurate and scaleable substrate resistance components in RF MOSFETs," *IEEE Electron Device Lett.*, vol. EDL–23, no. 4, p. 221, Apr. 2002.

[102] T. C. Ong, P. K. Ko, and C. Hu, "50 – Å gate oxide MOSFET's at 77 K," *IEEE Trans. Electron Devices*, vol. ED–34, p. 2129, 1987.

[103] J. I. Lee, M. B. Lee and K, N, Kang, "Simple extraction method for mobility parameters in Si – MOSFET's at 77 K," *Electronic Lett.*, vol. 26, p. 852, June. 1990.

[104] E. P. Vandamme, D. Schreurs, C. van Dinther, G. Badenes, L. Deferm, "Development of a RF large signal MOSFET model, based on an equivalent circuit, and comparison with the BSIM3v3 compact model," *Solid – State Electron.*, vol. 46, p. 353, June. 2002.

[105] A. Pascht, M. Grozing, D. Wiegner, and M. Berroth, "Small – signal and temperature noise model for MOSFETs," *IEEE Trans. Microwave Theory Tech.*, vol. 50, p. 1927, Aug. 2002.

[106] U. L. Rohde and D. P. Newkirk, *RF/Microwave Circuit Design for Wireless Applications*, Wiley: New York, 2000.

[107] R. Versari and B. Ricco, "MOSFET's negative transconductance at room temperature," *IEEE Trans. Electron Devices*, vol. ED–46, no. 6, p. 1189, June. 1999.

[108] B. Chihming and J. Y. Lee, " The observation of negative transconductance effect caused by

real–space–transfer of electrons in metal oxide semiconductor field effect transistors fabricated with Ta_2O_5 gate dielectric," *IEEE Electron Device Lett.*, vol. EDL–22, no. 3, p. 142, Mar. 2001.

[109] P. R. Karlsson and K. O. Jeppson, "An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors," *IEEE Trans. Semic. Manufact.*, vol. 9, p. 215, May. 1996.

$$
\begin{aligned}
&\text{Zone } I: \begin{cases}
\phi^{I}(L,y) = V_{bi}(0) + V_{ds} + \dfrac{V_{bi}(0) + V_{ds} - V_{gs}^{'}}{t_{fox}}\, y \\
\phi^{I}(0,y) = V_{bi}(0) + \dfrac{V_{bi}(0) - V_{gs}^{'}}{t_{fox}}\, y \\
\phi^{I}(x,-t_{fox}) = V_{gs} - V_{fb,f} = V_{gs}^{'} \\
D_{sf}(x,0) = \varepsilon_{ox} E_{y}^{I}(x,0)
\end{cases} \\
&\text{Zone } II: \begin{cases}
\phi^{II}(L,y) = V_{bi}(y) + V_{ds} \\
\phi^{II}(0,y) = V_{bi}(y) \\
D_{sf}(x,0) = \varepsilon_{si} E_{y}^{II}(x,0) \\
D_{sb}(x,t_{si}) = \varepsilon_{si} E_{y}^{II}(x,t_{si})
\end{cases} \\
&\text{Zone } III: \begin{cases}
\phi^{III}(L,y) = V_{bi}(t_{si}) + V_{ds} - \dfrac{V_{bi}(t_{si}) + V_{ds} - V_{bs}^{'}}{t_{box}}(y - t_{si}) \\
\phi^{III}(0,y) = V_{bi}(t_{si}) - \dfrac{V_{bi}(t_{si}) - V_{bs}^{'}}{t_{box}}(y - t_{si}) \\
\phi^{III}(x,t_{si} + t_{box}) = V_{bs} - V_{fb,b} = V_{bs}^{'} \\
D_{sb}(x,t_{si}) = \varepsilon_{ox} E_{y}^{III}(x,t_{si})
\end{cases}
\end{aligned}
$$

Table 1

$$
\text{Zone } I:\begin{cases}
G_x^I(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m y\sinh k_m\left(t_{fox}+y'\right)}{k_m\cosh k_m t_{fox}}, & y'<y\\
G_x^I(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m y'\sinh k_m\left(t_{fox}+y\right)}{k_m\cosh k_m t_{fox}}, & y<y'\\
G_y^I(x,y;x',y')=\dfrac{2}{t_{fox}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^I y\cos k_n^I y'\,\dfrac{\sinh k_n^I x\sinh k_n^I\left(L-x'\right)}{k_n^I\sinh k_n^I L}, & x<x'\\
G_y^I(x,y;x',y')=\dfrac{2}{t_{fox}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^I y\cos k_n^I y'\,\dfrac{\sinh k_n^I x'\sinh k_n^I\left(L-x\right)}{k_n^I\sinh k_n^I L}, & x'<x
\end{cases}
$$

$$
\text{Zone } II:\begin{cases}
G_x^{II}(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m y\cosh k_m\left(t_{si}-y'\right)}{k_m\sinh k_m t_{si}}, & y'<y\\
G_x^{II}(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m y'\cosh k_m\left(t_{si}-y\right)}{k_m\cosh k_m t_{fox}}, & y<y'\\
G_y^{II}(x,y;x',y')=\dfrac{c}{t_{si}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^{II} y\cos k_n^{II} y'\,\dfrac{\sinh k_n^{II} x\sinh k_n^{II}\left(L-x'\right)}{k_n^{II}\sinh k_n^{II} L}, & x<x'\\
G_y^{II}(x,y;x',y')=\dfrac{c}{t_{si}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^{II} y\cos k_n^{II} y'\,\dfrac{\sinh k_n^{II} x'\sinh k_n^{II}\left(L-x\right)}{k_n^{II}\sinh k_n^{II} L}, & x'<x
\end{cases}
$$

$c=1\,for\quad n=0;c=2\,for\quad n>0.$

$$
\text{Zone } III:\begin{cases}
G_x^{III}(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m\left(y-t_{si}\right)\sinh k_m\left(t_{box}+t_{si}-y'\right)}{k_m\cosh k_m t_{box}}, & y'<y\\
G_x^{III}(x,y;x',y')=\dfrac{2}{L}\displaystyle\sum_{m=1}^{\infty}\sin k_m x\sin k_m x'\,\dfrac{\cos k_m\left(y'-t_{si}\right)\sinh k_m\left(t_{box}+t_{si}-y\right)}{k_m\cosh k_m t_{box}}, & y<y'\\
G_y^{III}(x,y;x',y')=\dfrac{2}{t_{box}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^{III}\left(y-t_{si}\right)\cos k_n^{III}\left(y'-t_{si}\right)\dfrac{\sinh k_n^{III} x\sinh k_n^{III}\left(L-x'\right)}{k_n^{III}\sinh k_n^{III} L}, & x<x'\\
G_y^{III}(x,y;x',y')=\dfrac{2}{t_{box}}\displaystyle\sum_{n=1}^{\infty}\cos k_n^{III}\left(y-t_{si}\right)\cos k_n^{III}\left(y'-t_{si}\right)\dfrac{\sinh k_n^{III} x'\sinh k_n^{III}\left(L-x\right)}{k_n^{III}\sinh k_n^{III} L}, & x'<x
\end{cases}
$$

Table 2

$$D_{sf}^{m}=\frac{\varepsilon_{si}k_{m}}{d_{0}^{m}}\left[\frac{d_{2}^{m}}{\sinh\left(k_{m}t_{si}\right)}-d_{1}^{m}\left(\frac{1}{\tanh\left(k_{m}t_{si}\right)}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}\tanh\left(k_{m}t_{box}\right)\right)\right]$$

$$D_{sb}^{m}=\frac{\varepsilon_{si}k_{m}}{d_{0}^{m}}\left[-\frac{d_{1}^{m}}{\sinh\left(k_{m}t_{si}\right)}+d_{2}^{m}\left(\frac{1}{\tanh\left(k_{m}t_{si}\right)}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}\tanh\left(k_{m}t_{fox}\right)\right)\right]$$

$$d_{0}^{m}=\frac{1}{\left[\sinh\left(k_{m}t_{si}\right)\right]^{2}}-\left(\frac{1}{\tanh\left(k_{m}t_{si}\right)}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}\tanh\left(k_{m}t_{fox}\right)\right)\left(\frac{1}{\tanh\left(k_{m}t_{si}\right)}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}\tanh\left(k_{m}t_{box}\right)\right)$$

$$d_{1}^{m}=-\phi_{q}^{m}+\left(\frac{2V_{gs}^{'}}{m\pi}\right)\cdot\left(\frac{1-\left(-1\right)^{m}}{\cosh\left(k_{m}t_{fox}\right)}\right)+h_{m}^{I}$$

$$d_{2}^{m}=-\phi_{q}^{m}+\left(\frac{2V_{bs}^{'}}{m\pi}\right)\cdot\left(\frac{1-\left(-1\right)^{m}}{\cosh\left(k_{m}t_{box}\right)}\right)+h_{m}^{III}$$

$$h_{m}^{I}=\sum_{n=1}^{\infty}\frac{1}{2}t_{mn}^{I}\left[A_{n}^{S}+\left(-1\right)^{m+1}A_{n}^{D}\right]$$

$$h_{m}^{III}=\sum_{n=1}^{\infty}\frac{1}{2}t_{mn}^{III}\left[C_{n}^{S}+\left(-1\right)^{m+1}C_{n}^{D}\right]$$

$$t_{mn}^{I}=\frac{4}{m\pi}\left[1+\frac{L^{2}\left(n-0.5\right)^{2}}{t_{fox}^{2}m^{2}}\right]^{-1}$$

$$t_{mn}^{III}=\frac{4}{m\pi}\left[1+\frac{L^{2}\left(n-0.5\right)^{2}}{t_{box}^{2}m^{2}}\right]^{-1}$$

$$\phi_{q}^{m}=\frac{2}{m\pi}\left[\left(1-\left(-1\right)^{m}\right)\left(-\frac{qN_{B}}{\varepsilon_{si}}\cdot\frac{L^{2}}{\left(m\pi\right)^{2}}\right)+\left(1-\left(-1\right)^{m}\right)\cdot V_{bi}+\left(-1\right)^{m+1}\cdot V_{ds}\right]$$

Table 3

$$G^m = \left[\frac{P_2^m}{\sinh(k_m t_{si})} - P_1^m \left(\frac{1}{\tanh(k_m t_{si})} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tanh(k_m t_{box}) \right) \right]$$

$$F_g^m = -\left[\frac{1}{\tanh(k_m t_{si})} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tanh(k_m t_{box}) \right] \left[P_3^m + \frac{2}{m\pi} \cdot \frac{1-(-1)^m}{\cosh(k_m t_{fox})} \right]$$

$$F_b^m = \frac{1}{\sinh(k_m t_{si})} \left[P_4^m + \frac{2}{m\pi} \cdot \frac{1-(-1)^m}{\cosh(k_m t_{box})} \right]$$

$$F_d^m = \left[\frac{P_5^m}{\sinh(k_m t_{si})} - P_6^m \left(\frac{1}{\tanh(k_m t_{si})} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} \tanh(k_m t_{box}) \right) \right]$$

$$P_1^m = -\frac{2}{m\pi}\left[1-(-1)^m\right] \cdot \left(V_{bi} - \frac{qN_B}{\varepsilon_{si}} \frac{L^2}{(m\pi)^2} \right)$$
$$+ \sum_{n=1}^{\infty} \frac{t_{mn}^I}{t_{fox} k_{mn}^I} \left[1-(-1)^{m+1}\right] \cdot \left[V_{bi} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{V_{bi}}{t_{fox}} \left(t_{fox} \cdot \sin\left(n-\frac{1}{2}\right)\pi \right) - \frac{1}{k_n^I} \right]$$

$$P_2^m = -\frac{2}{m\pi}\left[1-(-1)^m\right] \cdot \left(V_{bi} - \frac{qN_B}{\varepsilon_{si}} \frac{L^2}{(m\pi)^2} \right)$$
$$+ \sum_{n=1}^{\infty} \frac{t_{mn}^{III}}{t_{box} k_{mn}^{III}} \left[1-(-1)^{m+1}\right] \cdot \left[V_{bi} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{V_{bi}}{t_{box}} \left(t_{box} \cdot \sin\left(n-\frac{1}{2}\right)\pi \right) - \frac{1}{k_n^{III}} \right]$$

$$P_3^m = \sum_{n=1}^{\infty} \frac{t_{mn}^I}{t_{fox}^2 k_n^I} \left[1-(-1)^{m+1}\right] \cdot \left(t_{fox} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{k_n^I} \right)$$

$$P_4^m = \sum_{n=1}^{\infty} \frac{t_{mn}^{III}}{t_{box}^2 k_n^{III}} \left[1-(-1)^{m+1}\right] \cdot \left(t_{box} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{k_n^{III}} \right)$$

$$P_5^m = \sum_{n=1}^{\infty} \frac{t_{mn}^{III}}{t_{box} k_n^{III}} (-1)^{m+1} \cdot \left[\sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{t_{box}} \left(t_{box} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{k_n^{III}} \right) \right] - \frac{2}{m\pi}(-1)^{m+1}$$

$$P_6^m = \sum_{n=1}^{\infty} \frac{t_{mn}^I}{t_{fox} k_n^I} (-1)^{m+1} \cdot \left[\sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{t_{fox}} \left(t_{fox} \cdot \sin\left(n-\frac{1}{2}\right)\pi - \frac{1}{k_n^I} \right) \right] - \frac{2}{m\pi}(-1)^{m+1}$$

Table 4

Parameters	Value	Unit
$\boldsymbol{L}$	0.28	μm
$\boldsymbol{W}$	7.83	μm
t_{fox}	10	nm
t_{box}	347	nm
t_{si}	94	nm
μ_n	600	$cm^2/V{\cdot}s$
α	2.5×10^{-7}	cm/V
β	4×10^{-5}	cm/V
η	0.046	1/V
K_1	0.85	
K_1'	0.85	
K_2	2×10^{-3}	V/K
K_3	1.15	
K_4	4800	V/cm·K
α_0	0.995	
R_{th}	1.953×10^{4}	C/W
T_0	300	K
α_i	1.2×10^{-7}	cm/V
β_{i0}	2.3×10^{6}	V/cm

Table 5

V_{gs} (V)	0.6	1
C_{gs} (fF)	102	118.9
C_{gd} (fF)	58.5	60.45
R_g (Ω)	6.5	6.4
g_m (mS)	26.626	51.238
C_{dg} (fF)	85	140.3
R_{sub} (Ω)	59	60.7
C_{gb} (fF)	8.3	8
g_{mb} (mS)	3.543	3.92
C_{db} (fF)	80.1	90
C_{sb} (fF)	185	188
g_{ds} (mS)	1.3433	3.608

Table 6

W_{drawn} (μm)	L_{drawn} (μm)	μ_0 ($cm^2V^{-1}s^{-1}$)	θ_1 (V^{-1})	θ_2 (V^{-2})	V_T (V)	R_T (Ω)	β_0 (AV^{-2})	T_{ox} (Å)	L_{eff} (μm)	W_{eff} (μm)
10	0.35	395	0.17	-0.017	0.6585	60	4.43E-03	106	0.29	9.94
10	0.4	395	0.165	-0.015	0.791	60	3.72E-03	107.9	0.34	9.94
10	0.5	395	0.165	-0.015	0.861	60.1	2.84E-03	109.3	0.44	9.94
10	0.6	395	0.165	-0.015	0.88	60.1	2.32E-03	109	0.54	9.94
10	0.8	395	0.165	-0.016	0.842	60.1	1.69E-03	109	0.74	9.94
10	1	395	0.165	-0.017	0.82	59	1.33E-03	109	0.94	9.94
10	2	395	0.16	-0.019	0.7916	59	6.72E-04	104.6	1.94	9.94
10	5	395	0.16	-0.023	0.7429	59	2.60E-04	106.3	4.94	9.94
10	10	395	0.165	-0.021	0.7367	59	1.31E-04	104.6	9.94	9.94
10	20	395	0.165	-0.021	0.738	59.5	6.28E-05	109	19.94	9.94

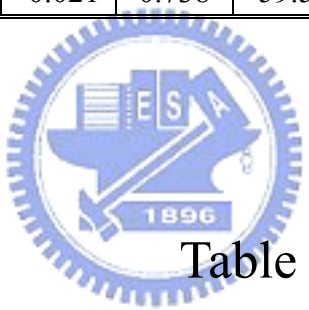
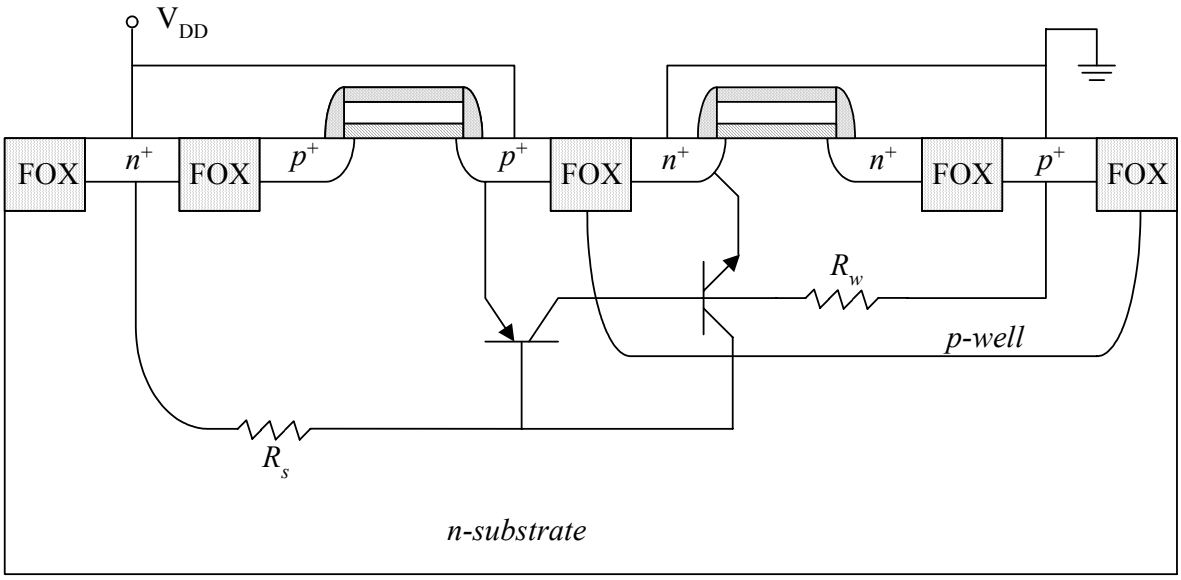
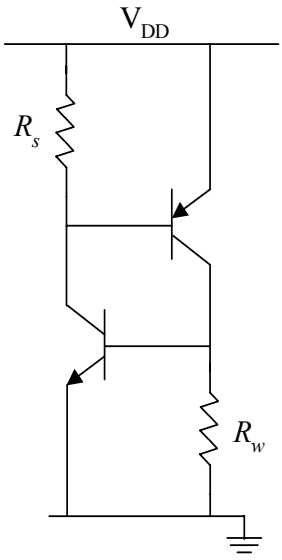


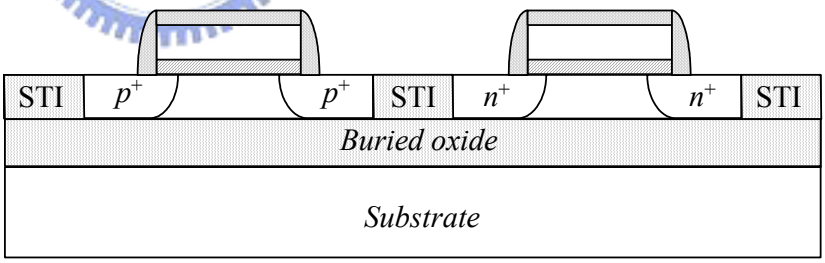
Table 7


V DD
FOX
n+
FOX
p+
p+
FOX
n+
n+
FOX
p+
FOX
Rw
p-well
Rs
n-substrate

(a)

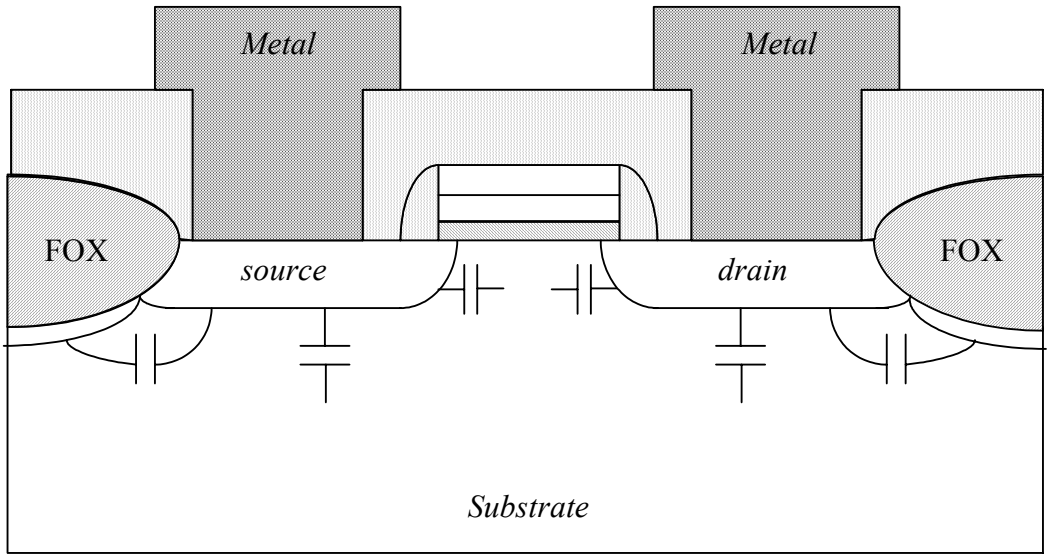

V DD
Rs
Rw

(b)

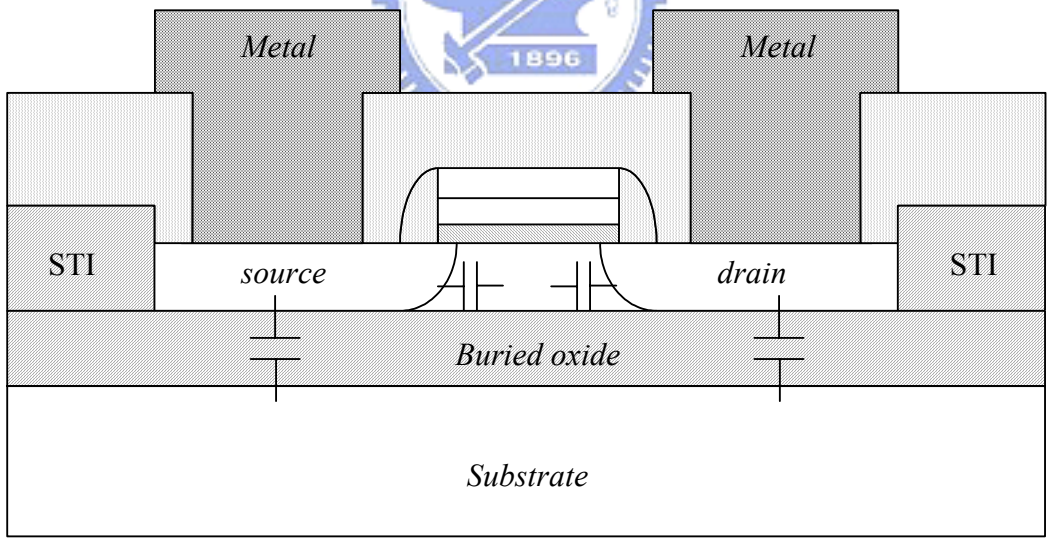

STI
p+
p+
STI
n+
n+
STI
Buried oxide
Substrate

(c)

Fig. 1–1

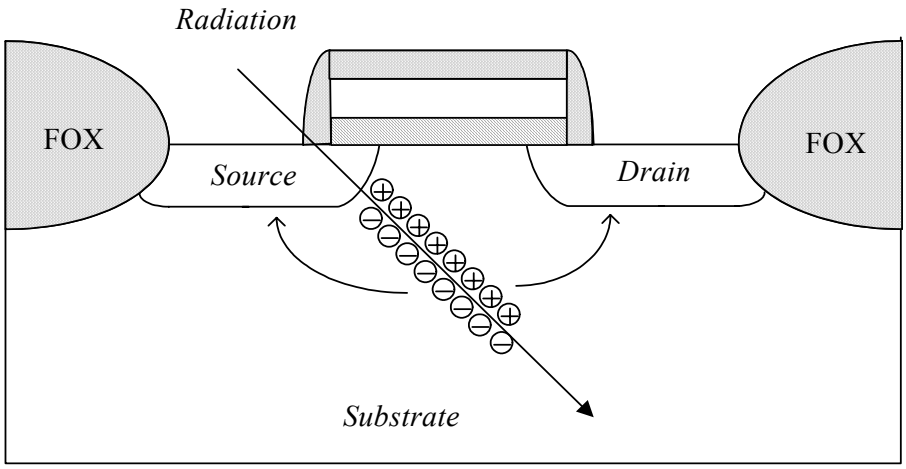

Metal
Metal
FOX
source
drain
FOX
Substrate

(a)

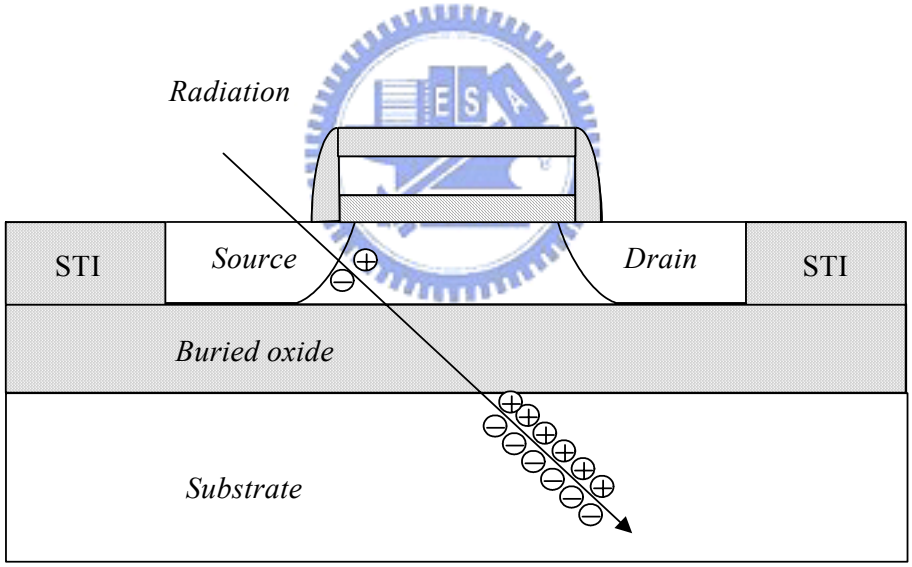

Metal
Metal
STI
source
drain
STI
Buried oxide
Substrate

(b)

Fig. 1–2

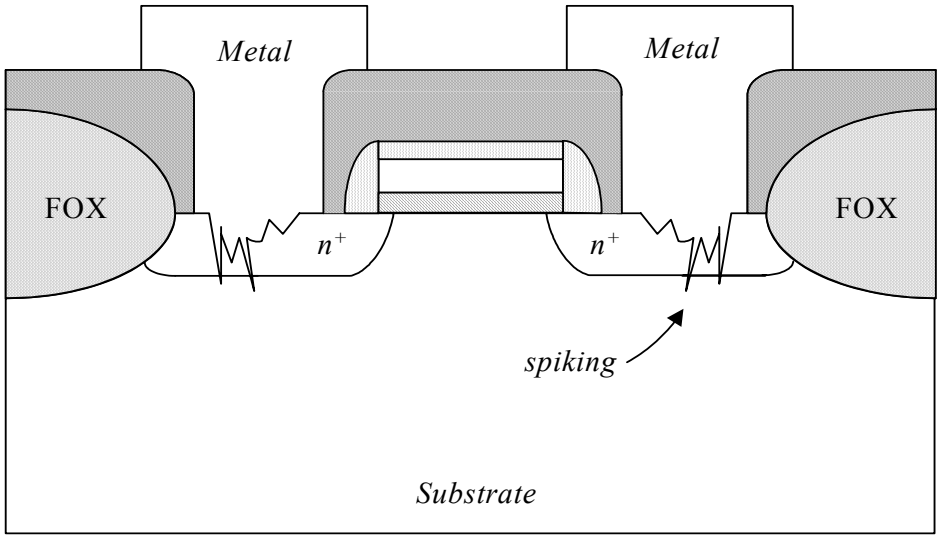

Radiation
FOX
Source
Drain
FOX
Substrate

(a)

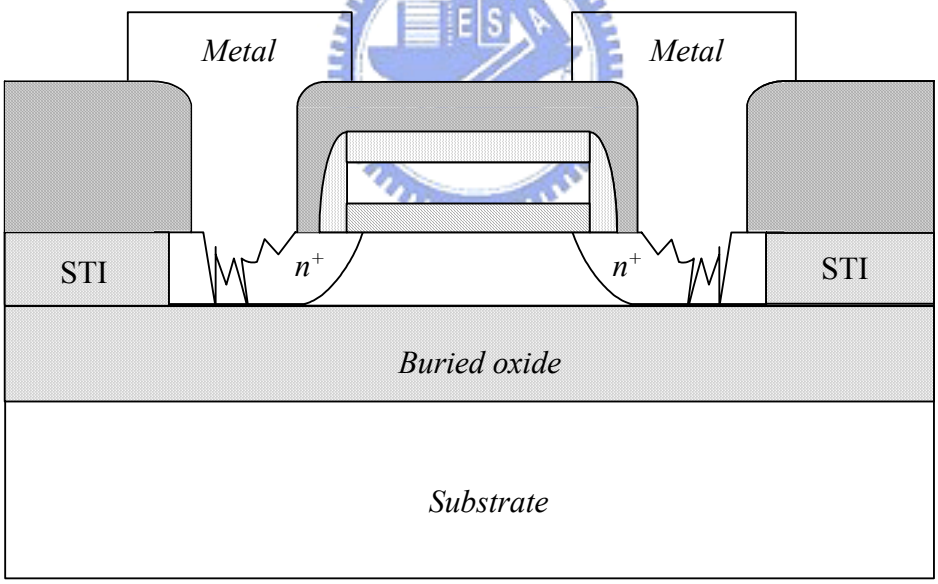

Radiation
STI
Source
Drain
STI
Buried oxide
Substrate

(b)

Fig. 1–3


Metal
Metal
FOX
FOX
n^+
n^+
spiking
Substrate

(a)


Metal
Metal
STI
STI
n^+
n^+
Buried oxide
Substrate

(b)

Fig. 1–4

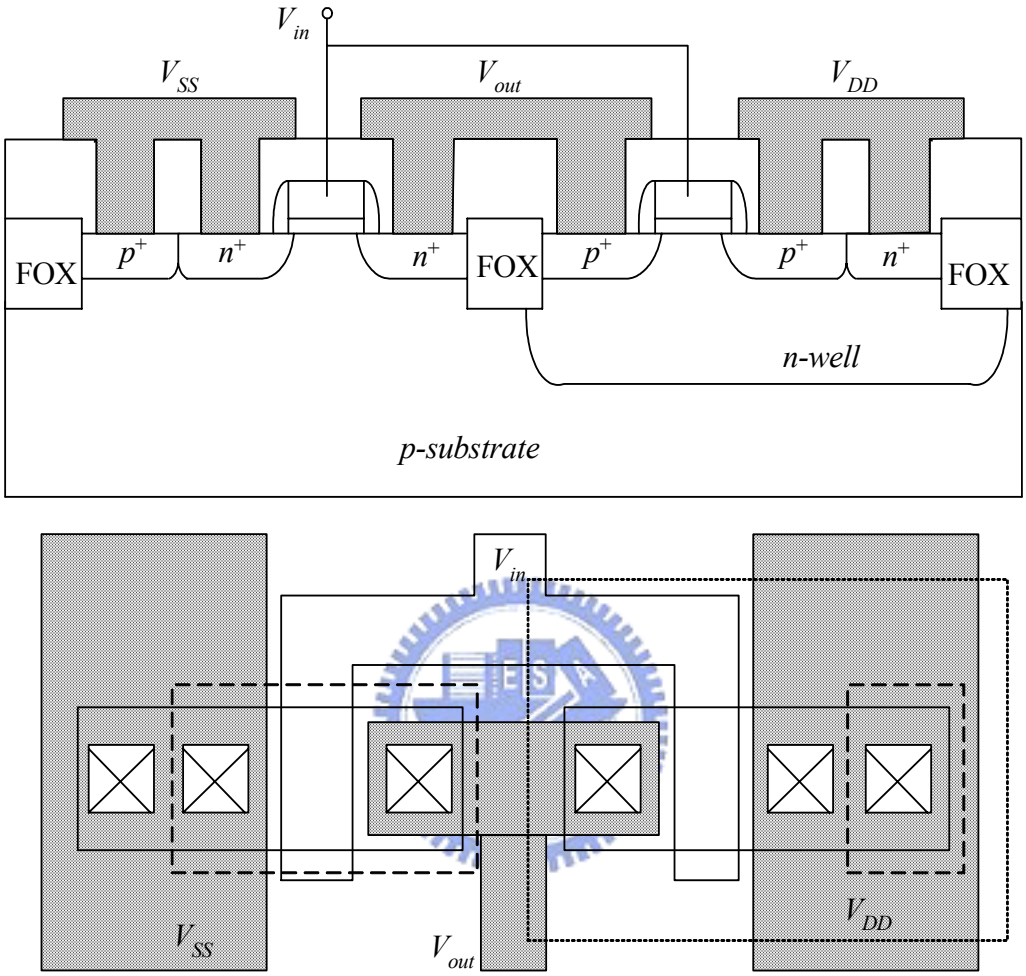

V_{in}
V_{SS}
V_{out}
V_{DD}
FOX
p^+
n^+
n^+
FOX
p^+
p^+
n^+
FOX
n-well
p-substrate
V_{in}
V_{SS}
V_{out}
V_{DD}

Fig. 1–5(a)

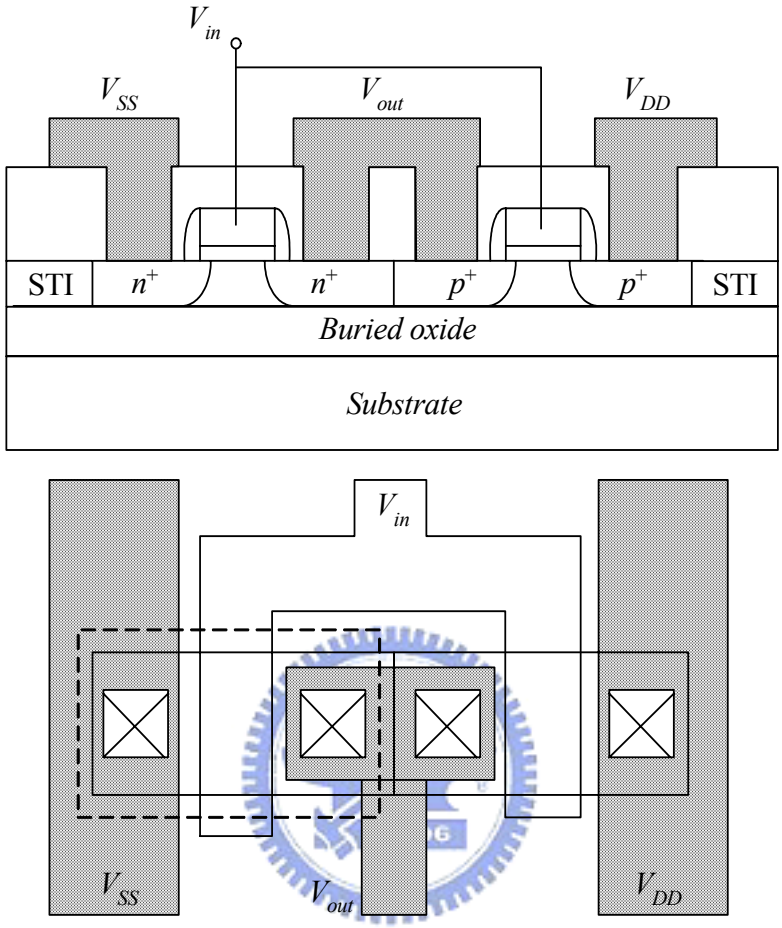

V_{in}
V_{SS}
V_{out}
V_{DD}
STI
n^+
n^+
p^+
p^+
STI
Buried oxide
Substrate
V_{in}
V_{SS}
V_{out}
V_{DD}

Fig. 1–5(b)

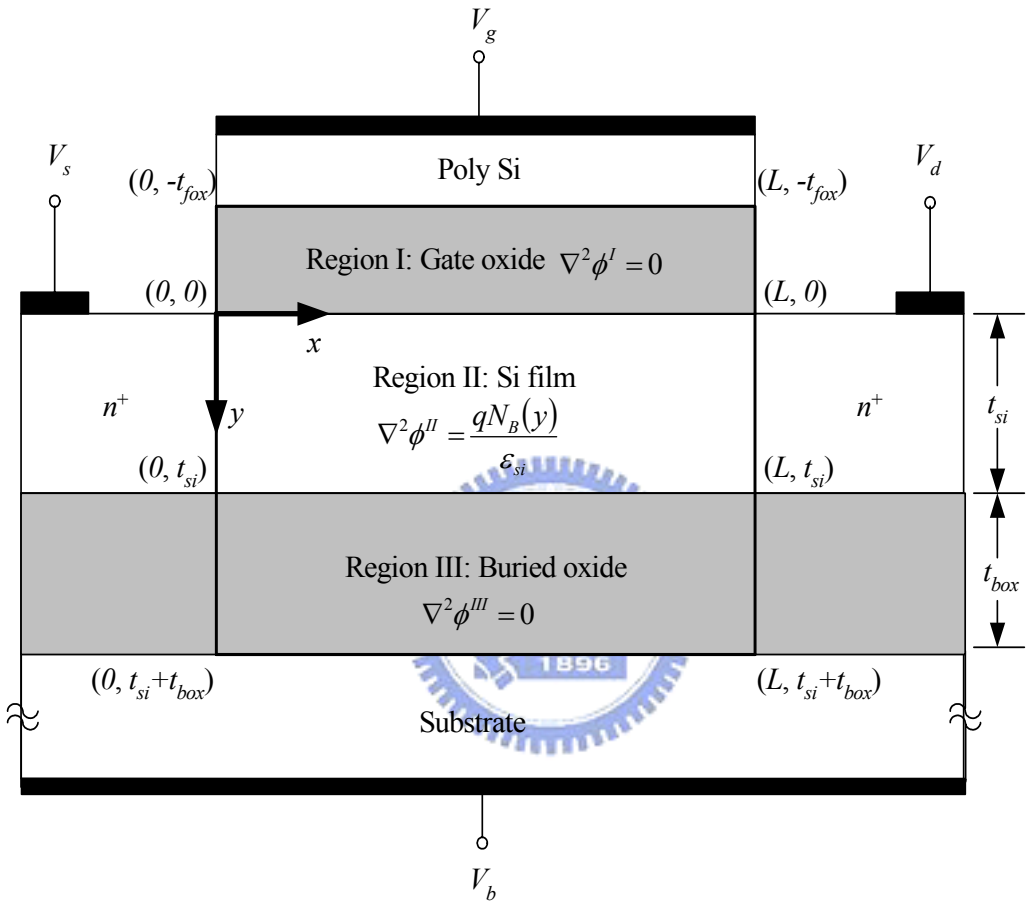

V_g
V_s
V_d
$(0, -t_{fox})$
Poly Si
$(L, -t_{fox})$
Region I: Gate oxide $\nabla^2\phi^I = 0$
$(0, 0)$
$(L, 0)$
x
y
Region II: Si film
$\nabla^2\phi^{II} = \frac{qN_B(y)}{\varepsilon_{si}}$
n^+
n^+
t_{si}
$(0, t_{si})$
(L, t_{si})
Region III: Buried oxide
$\nabla^2\phi^{III} = 0$
t_{box}
$(0, t_{si}+t_{box})$
$(L, t_{si}+t_{box})$
Substrate
V_b

Fig. 2–1

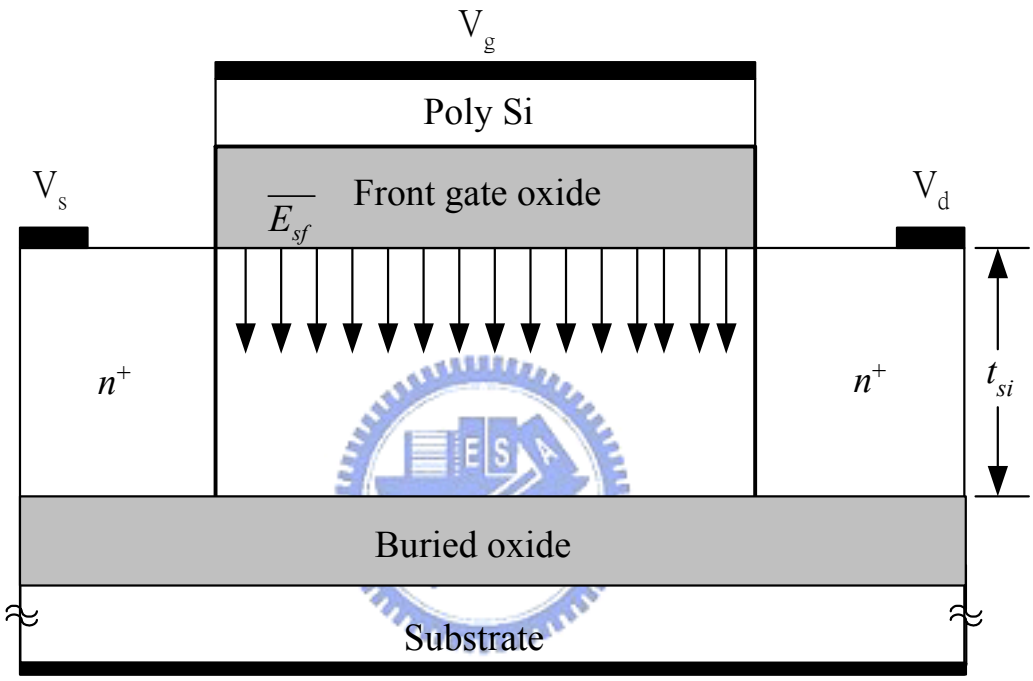

V g
Poly Si
V s
Front gate oxide
V d
$\overline{E_{sf}}$
n^+
n^+
t_{si}
Buried oxide
Substrate

Fig. 2–2(a)

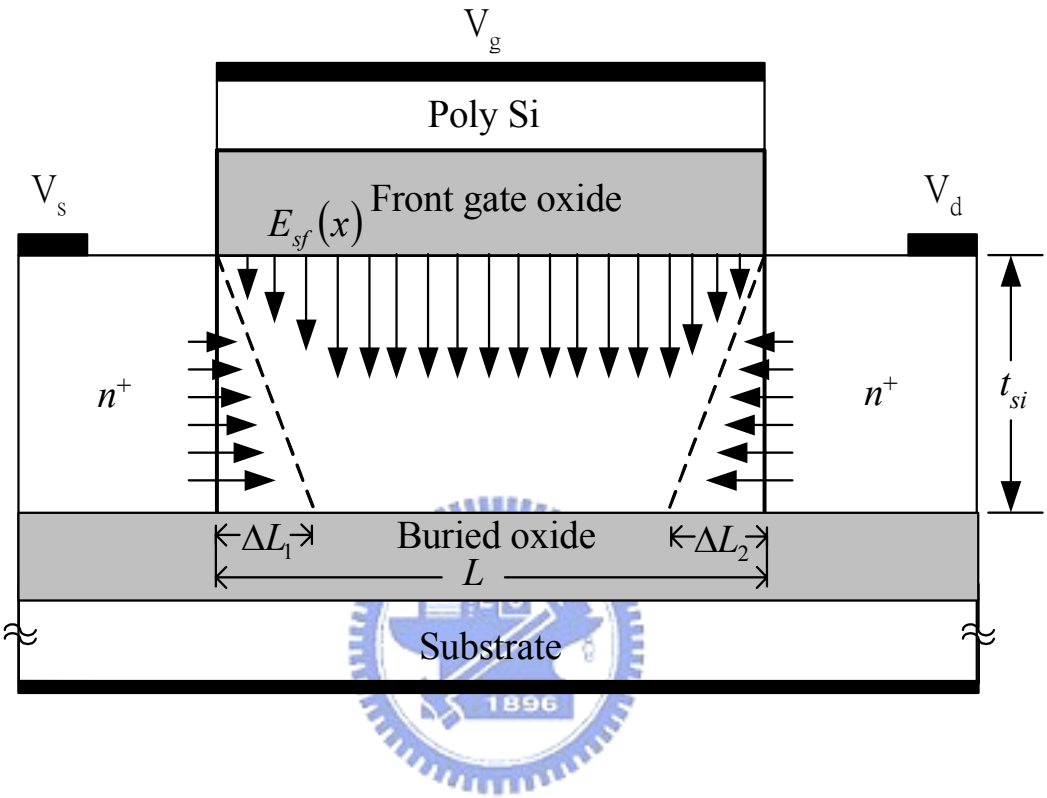

V_g
Poly Si
V_s
E_sf(x)
Front gate oxide
V_d
n+
n+
t_si
ΔL_1
Buried oxide
ΔL_2
L
Substrate

Fig. 2–2(b)

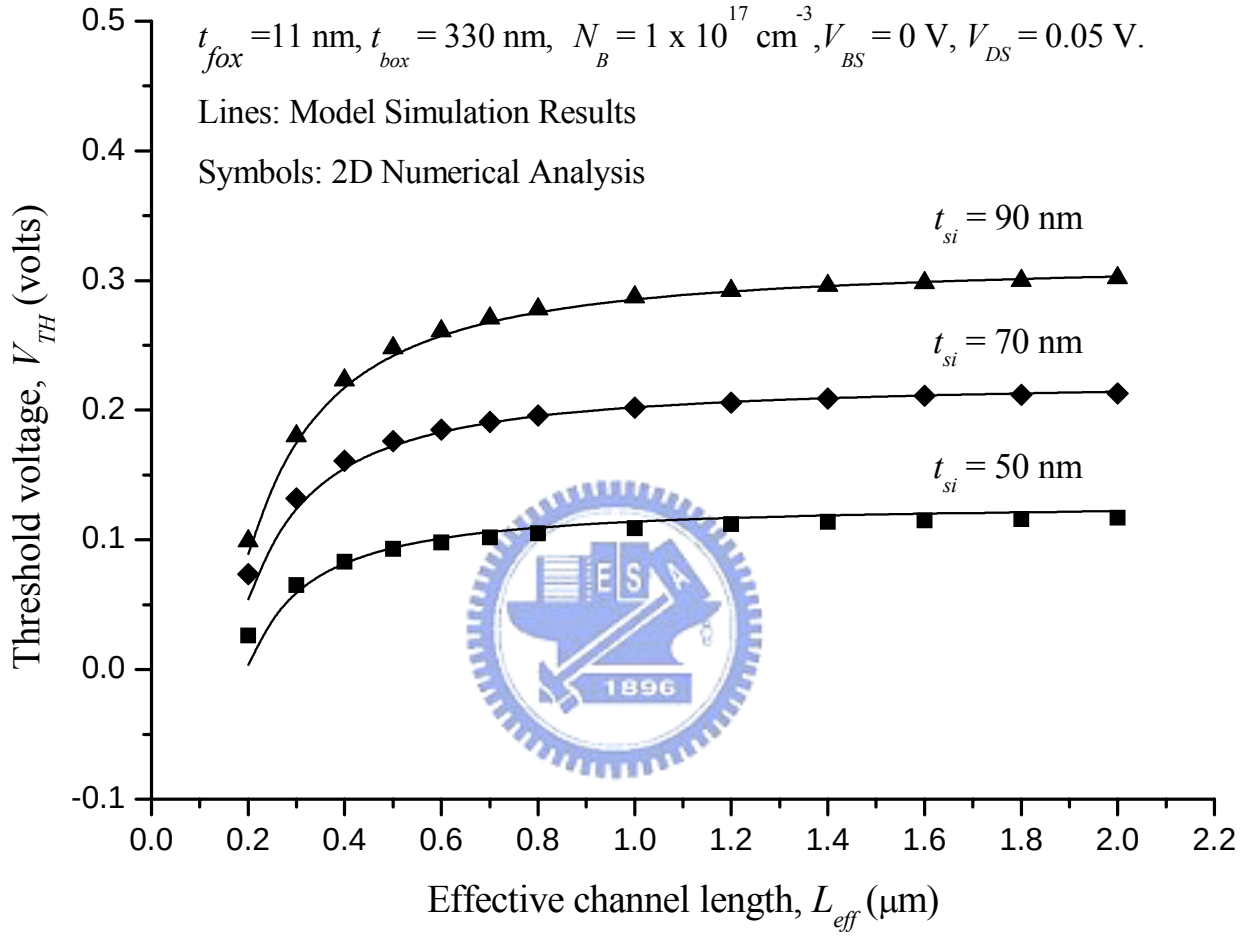

t_{fox} =11 nm, t_{box} = 330 nm, N_B = 1 x 10^{17} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
t_{si} = 90 nm
t_{si} = 70 nm
t_{si} = 50 nm
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2

Fig. 2–3

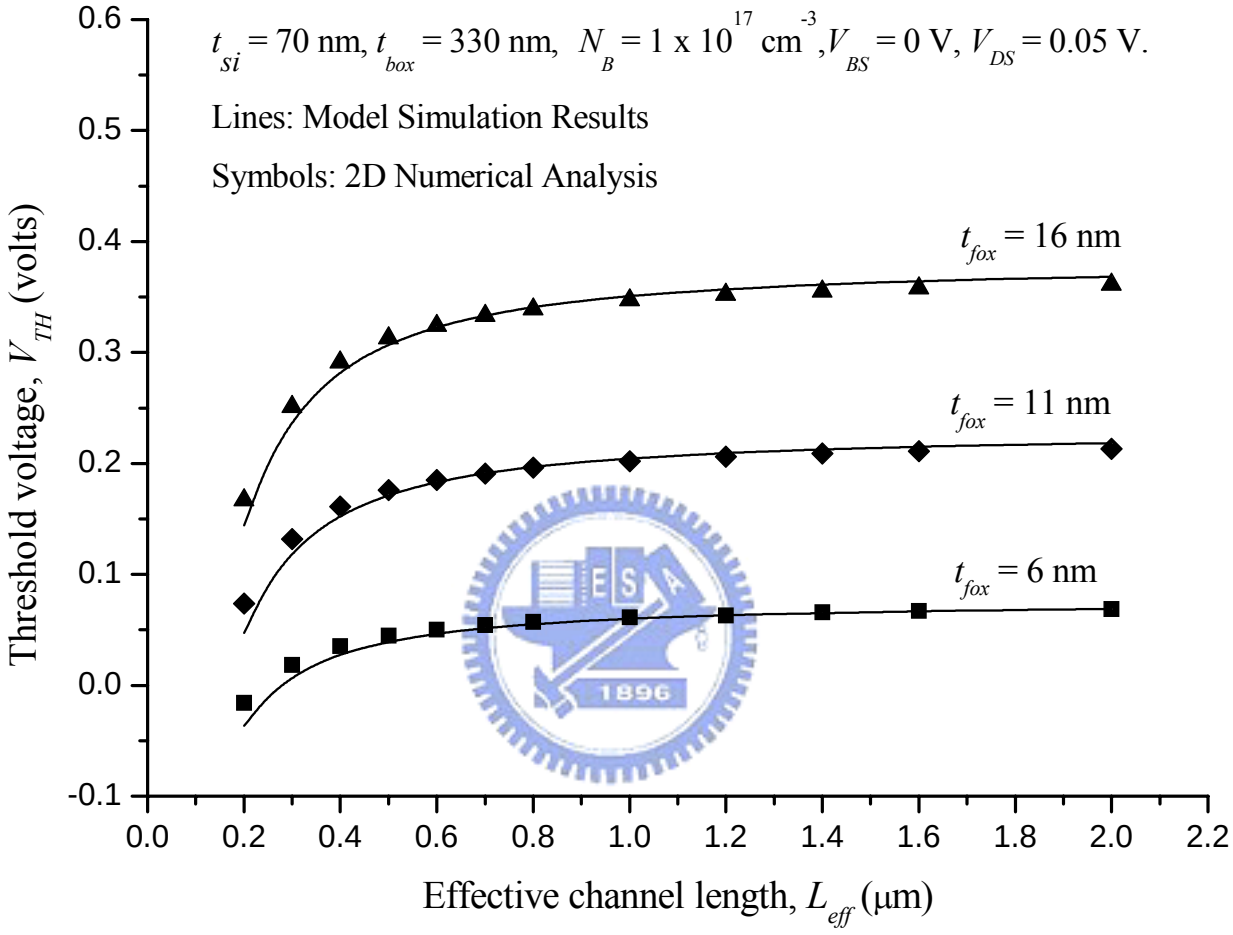

t_{si} = 70 nm, t_{box} = 330 nm, N_B = 1 x 10^{17} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
t_{fox} = 16 nm
t_{fox} = 11 nm
t_{fox} = 6 nm
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2

Fig. 2–4

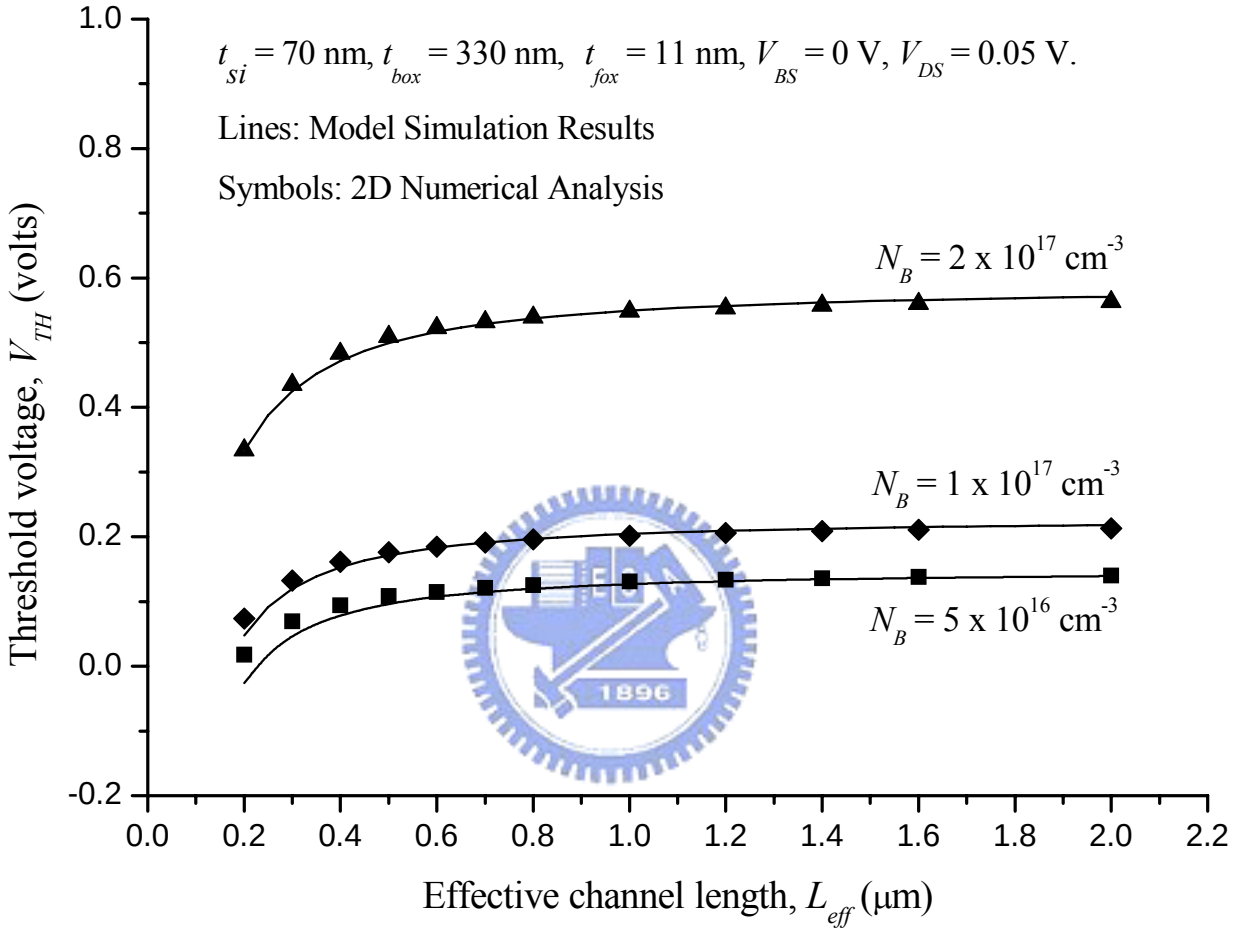

t_{si} = 70 nm, t_{box} = 330 nm, t_{fox} = 11 nm, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 2 x 10^{17} cm^{-3}
N_B = 1 x 10^{17} cm^{-3}
N_B = 5 x 10^{16} cm^{-3}
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2

Fig. 2–5

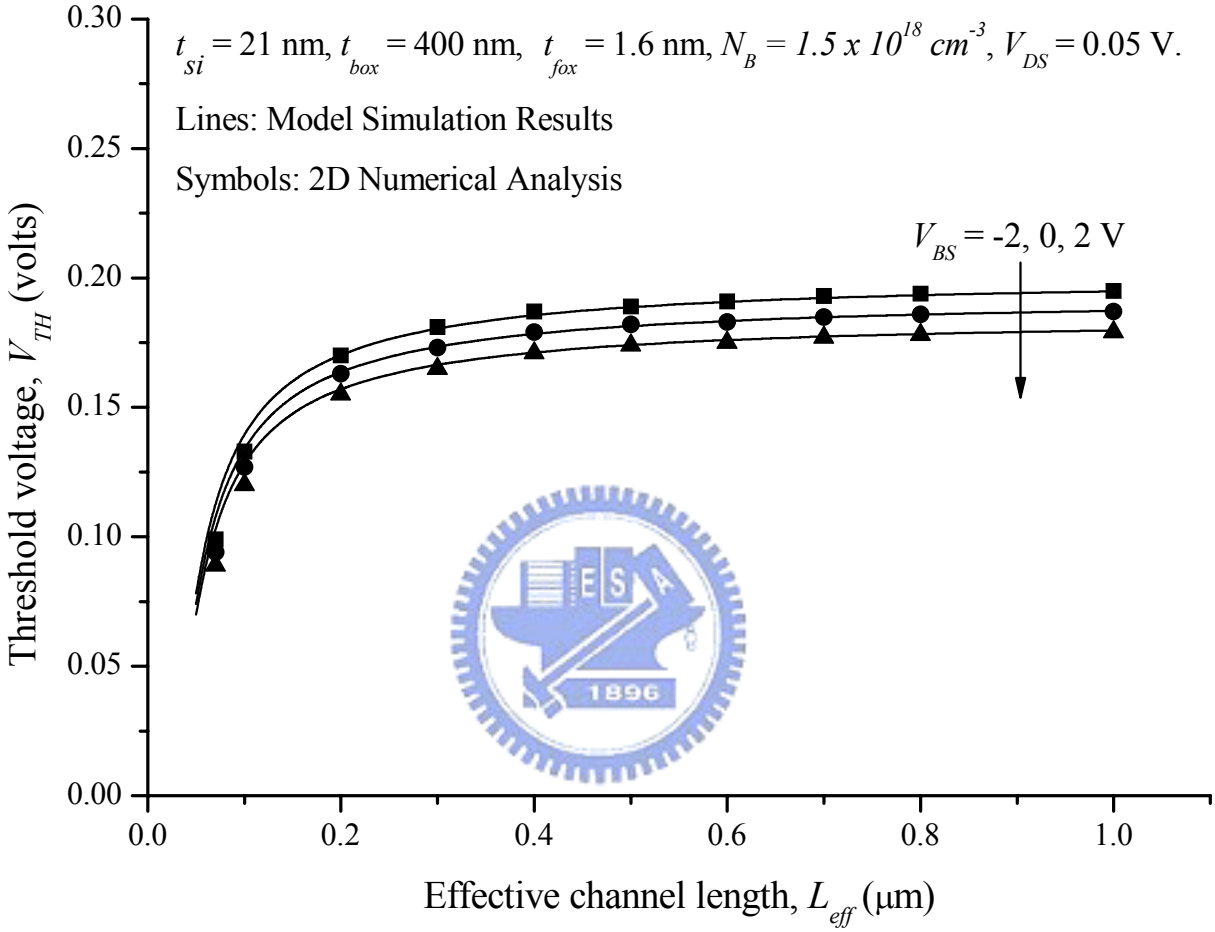

t_{si} = 21 nm, t_{box} = 400 nm, t_{fox} = 1.6 nm, N_B = 1.5 x 10^{18} cm^{-3}, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{BS} = -2, 0, 2 V
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
0.00
0.05
0.10
0.15
0.20
0.25
0.30
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 2–6

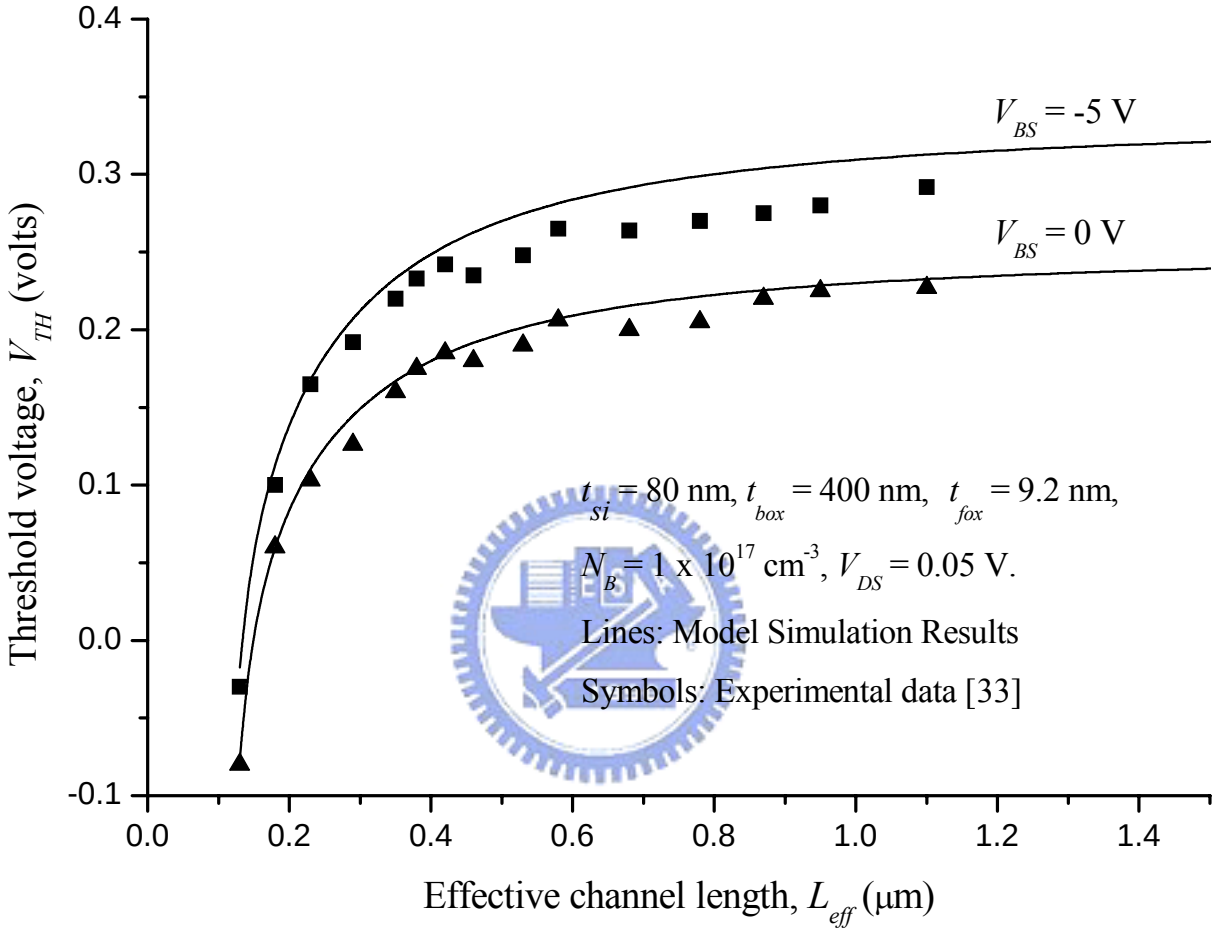

0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
V_{BS} = -5 V
V_{BS} = 0 V
t_{si} = 80 nm, t_{box} = 400 nm, t_{fox} = 9.2 nm,
N_B = 1 x 10^{17} cm^{-3}, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: Experimental data [33]

Fig. 2–7

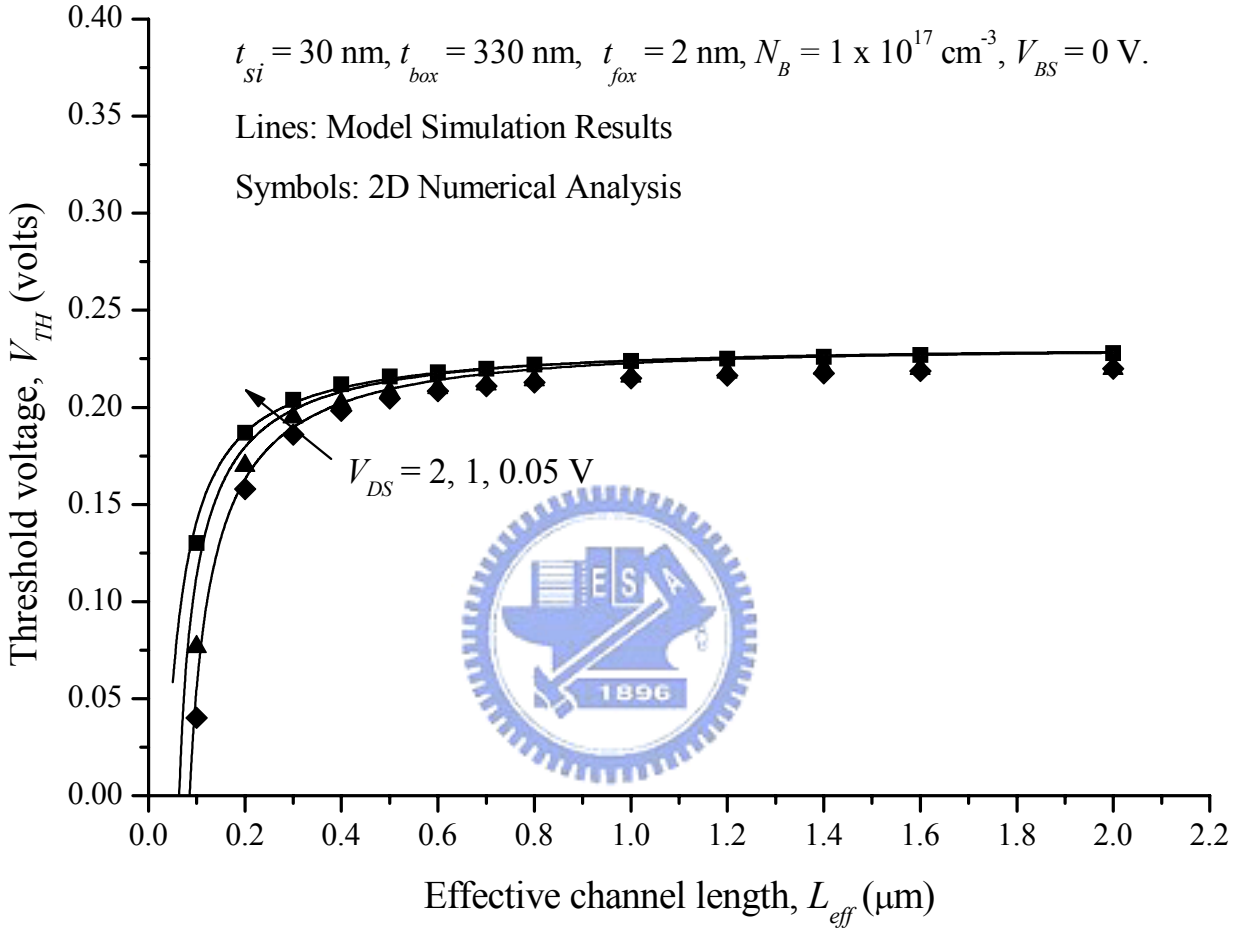

t_{si} = 30 nm, t_{box} = 330 nm, t_{fox} = 2 nm, N_B = 1 x 10^{17} cm^{-3}, V_{BS} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{DS} = 2, 1, 0.05 V
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
0.00
0.05
0.10
0.15
0.20
0.25
0.30
0.35
0.40
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2

Fig. 2–8

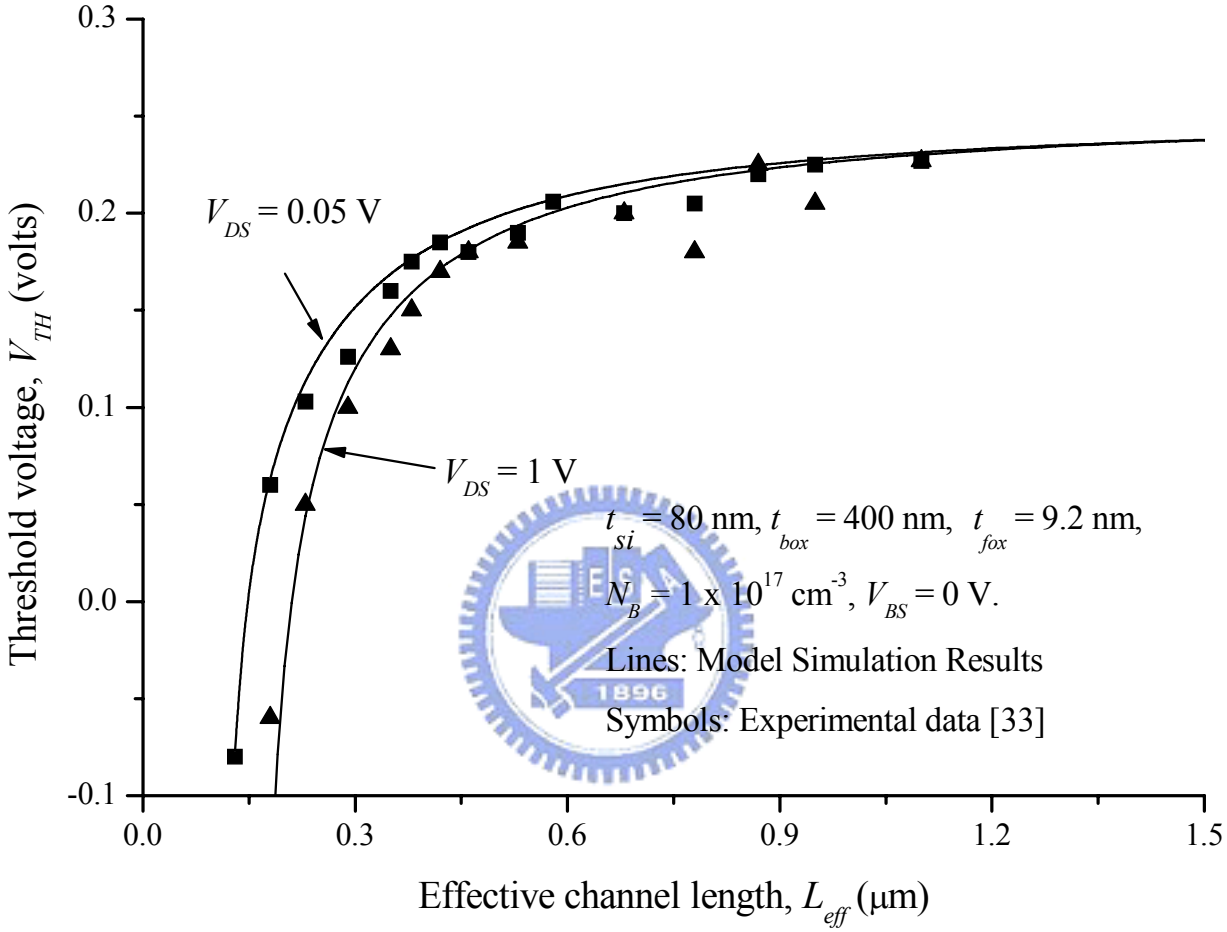

0.3
0.2
0.1
0.0
-0.1
0.0
0.3
0.6
0.9
1.2
1.5
Threshold voltage, V_{TH} (volts)
Effective channel length, L_{eff} (μm)
V_{DS} = 0.05 V
V_{DS} = 1 V
t_{si} = 80 nm, t_{box} = 400 nm, t_{fox} = 9.2 nm,
N_B = 1 x 10^{17} cm^{-3}, V_{BS} = 0 V.
Lines: Model Simulation Results
Symbols: Experimental data [33]

Fig. 2–9

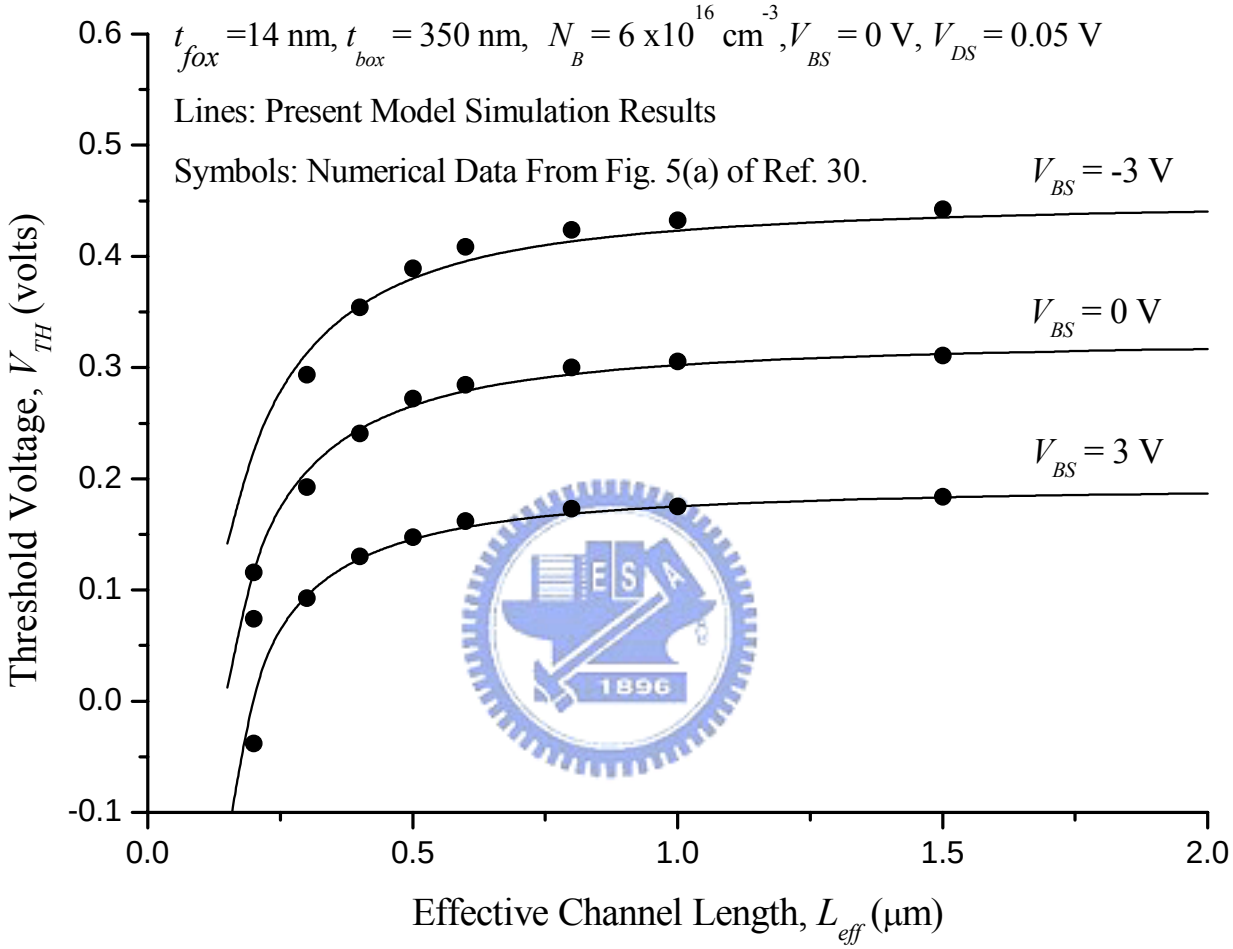

t_{fox} =14 nm, t_{box} = 350 nm, N_B = 6 x10^{16} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V
Lines: Present Model Simulation Results
Symbols: Numerical Data From Fig. 5(a) of Ref. 30.
V_{BS} = -3 V
V_{BS} = 0 V
V_{BS} = 3 V
Threshold Voltage, V_{TH} (volts)
Effective Channel Length, L_{eff} (μm)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.5
1.0
1.5
2.0

Fig. 2–10(a)

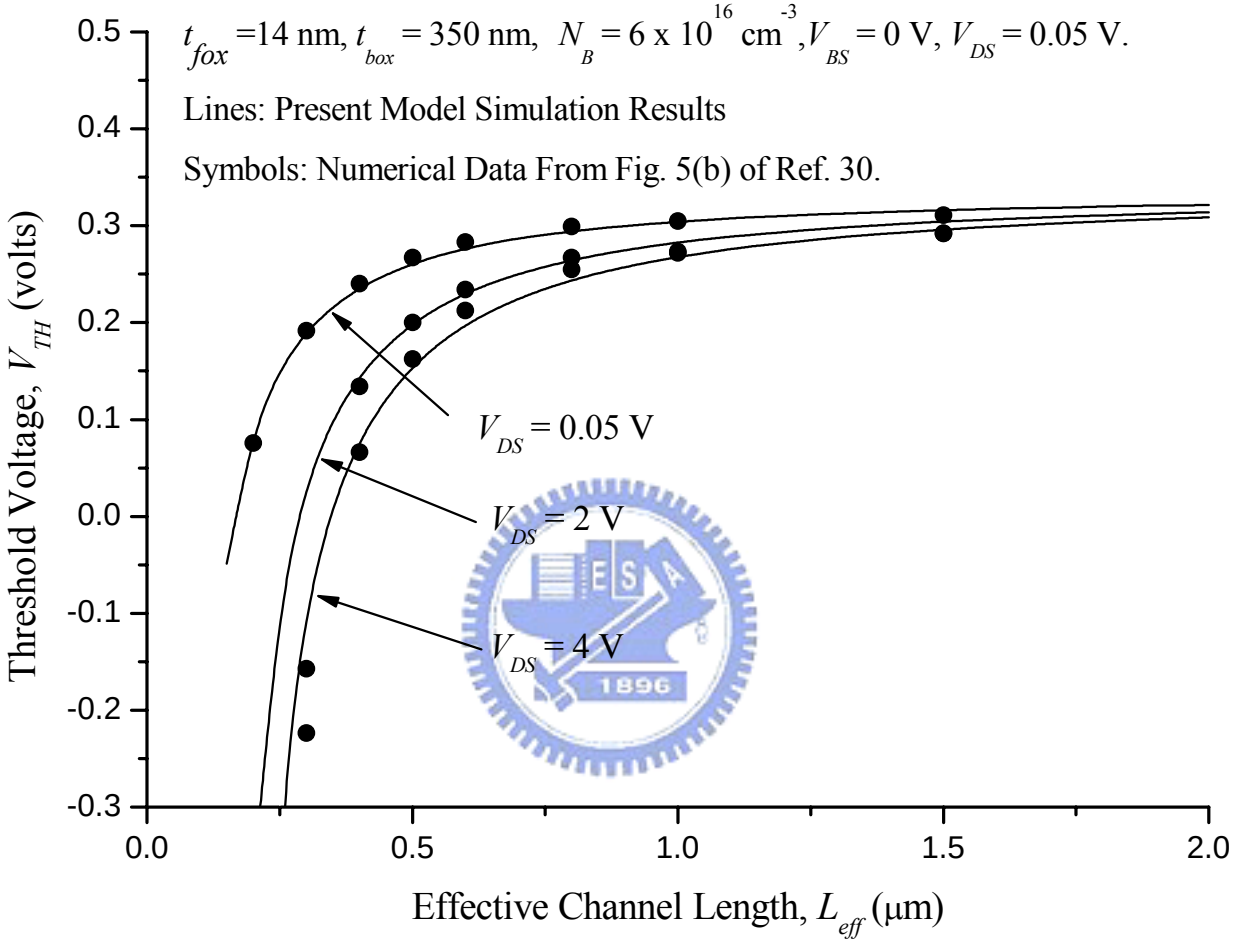

t_{fox} =14 nm, t_{box} = 350 nm, N_B = 6 x 10^{16} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Present Model Simulation Results
Symbols: Numerical Data From Fig. 5(b) of Ref. 30.
V_{DS} = 0.05 V
V_{DS} = 2 V
V_{DS} = 4 V
Threshold Voltage, V_{TH} (volts)
Effective Channel Length, L_{eff} (μm)
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
0.0
0.5
1.0
1.5
2.0

Fig. 2–10(b)

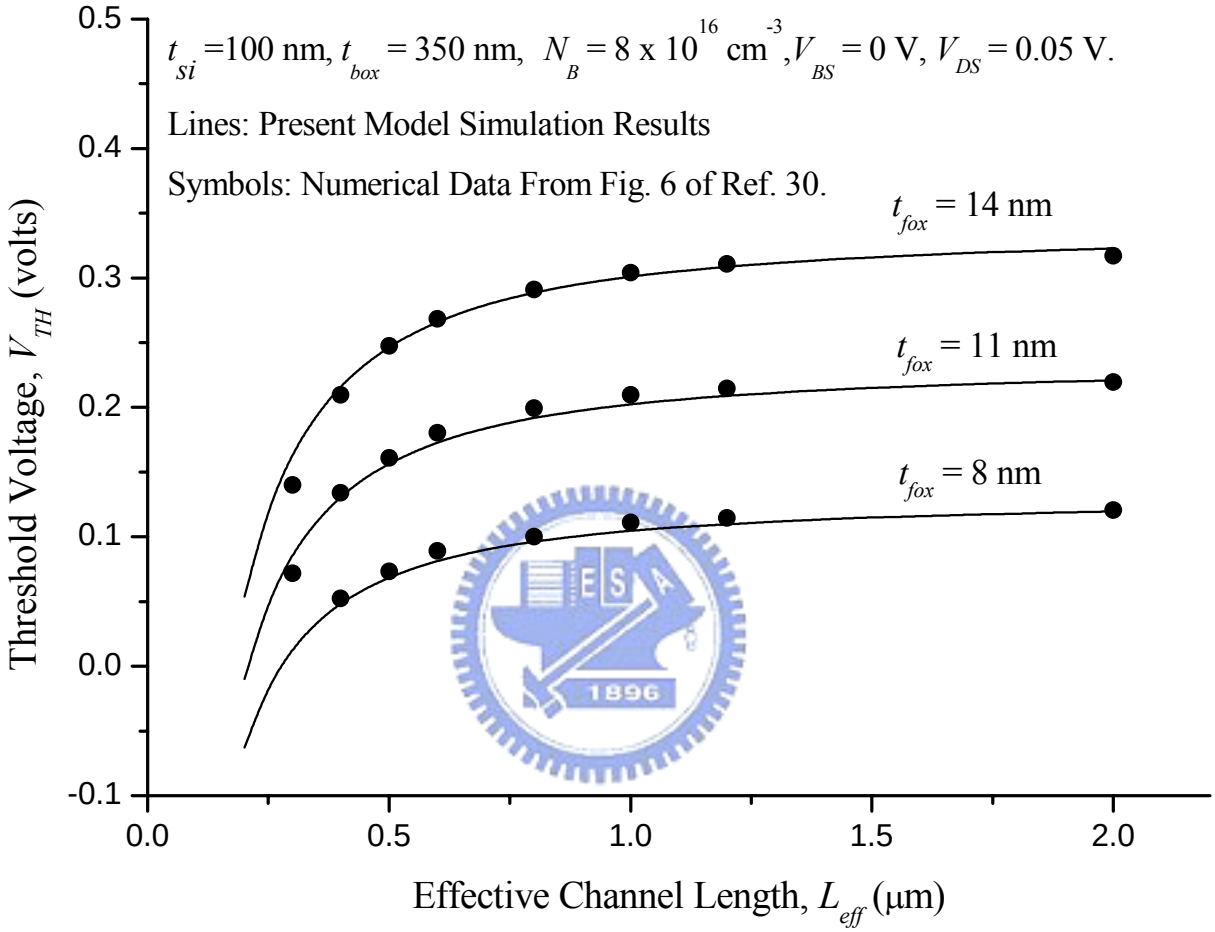

t_{si} =100 nm, t_{box} = 350 nm, N_B = 8 x 10^{16} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Present Model Simulation Results
Symbols: Numerical Data From Fig. 6 of Ref. 30.
t_{fox} = 14 nm
t_{fox} = 11 nm
t_{fox} = 8 nm
Threshold Voltage, V_{TH} (volts)
Effective Channel Length, L_{eff} (μm)
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.5
1.0
1.5
2.0

Fig. 2–10(c)

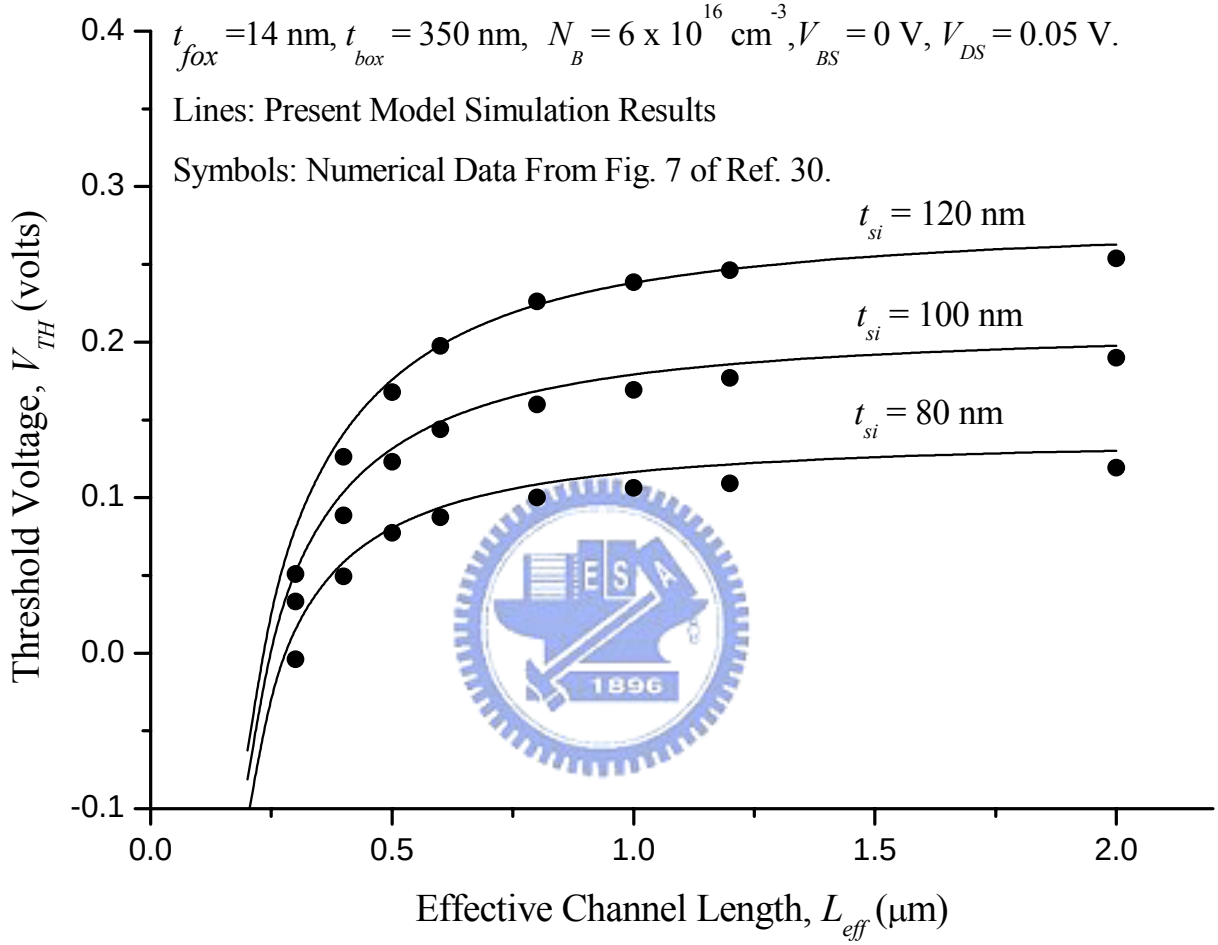

t_{fox} =14 nm, t_{box} = 350 nm, N_B = 6 x 10^{16} cm^{-3}, V_{BS} = 0 V, V_{DS} = 0.05 V.
Lines: Present Model Simulation Results
Symbols: Numerical Data From Fig. 7 of Ref. 30.
t_{si} = 120 nm
t_{si} = 100 nm
t_{si} = 80 nm
Threshold Voltage, V_{TH} (volts)
Effective Channel Length, L_{eff} (μm)
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
0.5
1.0
1.5
2.0

Fig. 2–10(d)

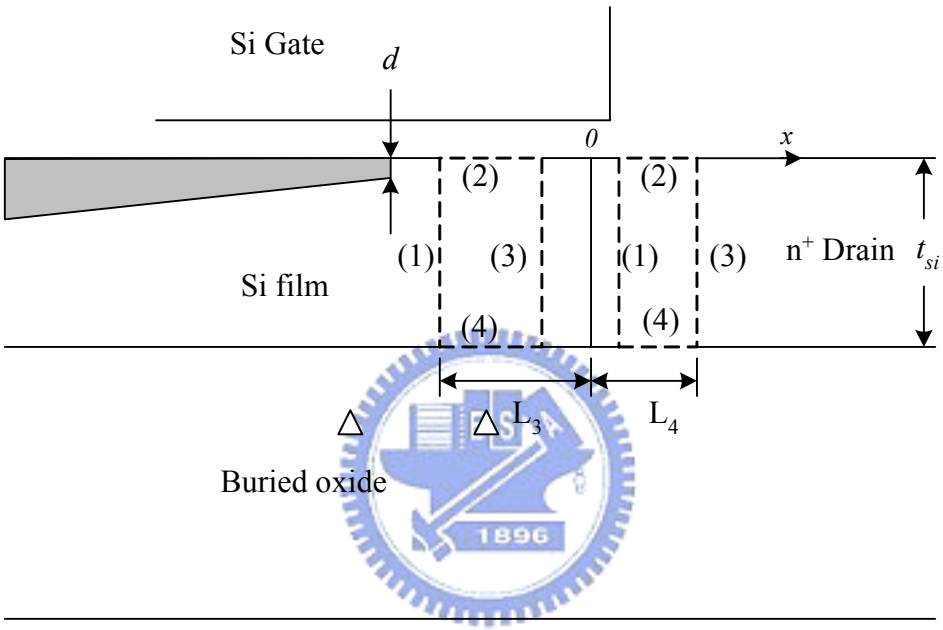


Fig. 3–1

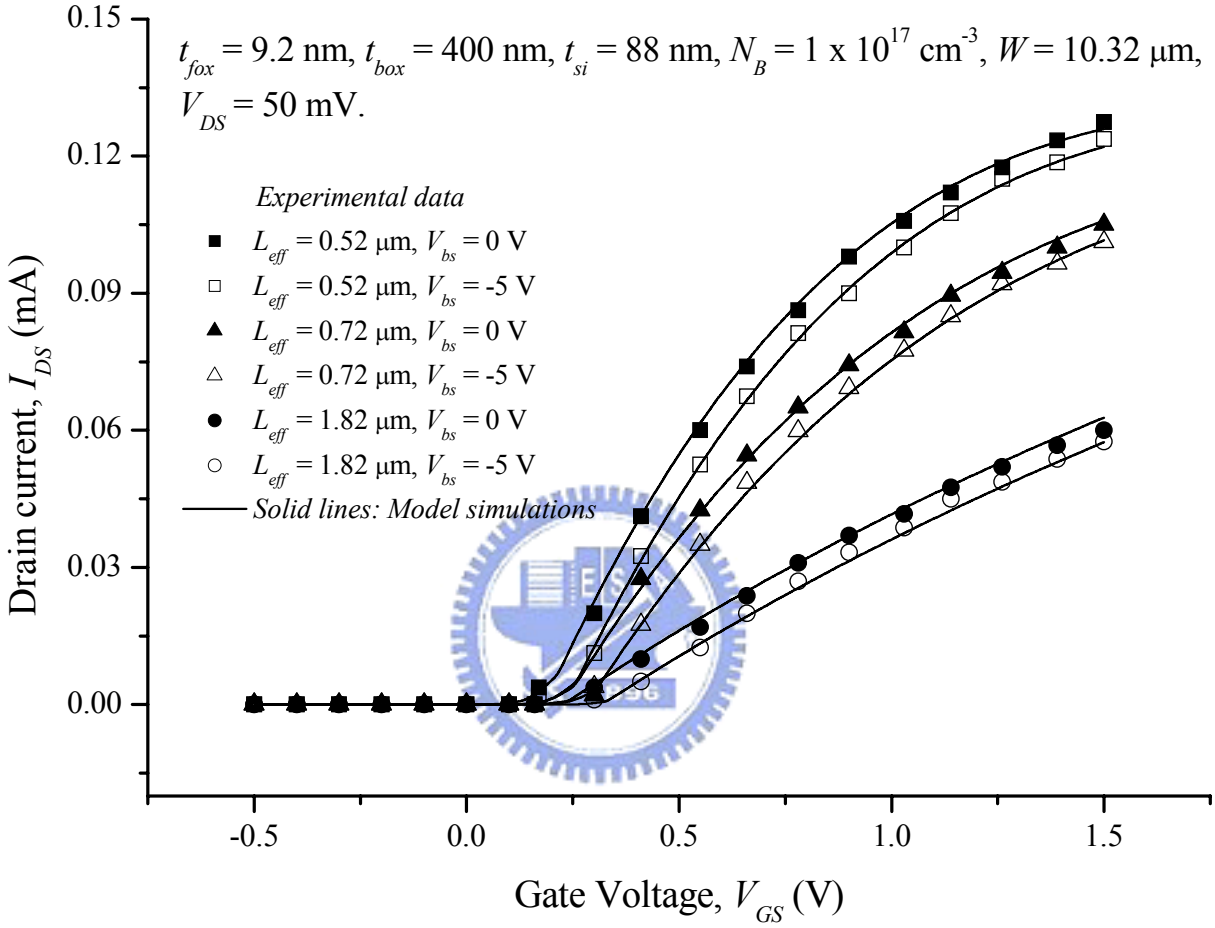

t_{fox} = 9.2 nm, t_{box} = 400 nm, t_{si} = 88 nm, N_B = 1 x 10^{17} cm^{-3}, W = 10.32 μm,
V_{DS} = 50 mV.
Experimental data
L_{eff} = 0.52 μm, V_{bs} = 0 V
L_{eff} = 0.52 μm, V_{bs} = -5 V
L_{eff} = 0.72 μm, V_{bs} = 0 V
L_{eff} = 0.72 μm, V_{bs} = -5 V
L_{eff} = 1.82 μm, V_{bs} = 0 V
L_{eff} = 1.82 μm, V_{bs} = -5 V
Solid lines: Model simulations
Drain current, I_{DS} (mA)
0.15
0.12
0.09
0.06
0.03
0.00
-0.5
0.0
0.5
1.0
1.5
Gate Voltage, V_{GS} (V)

Fig. 3–2(a)

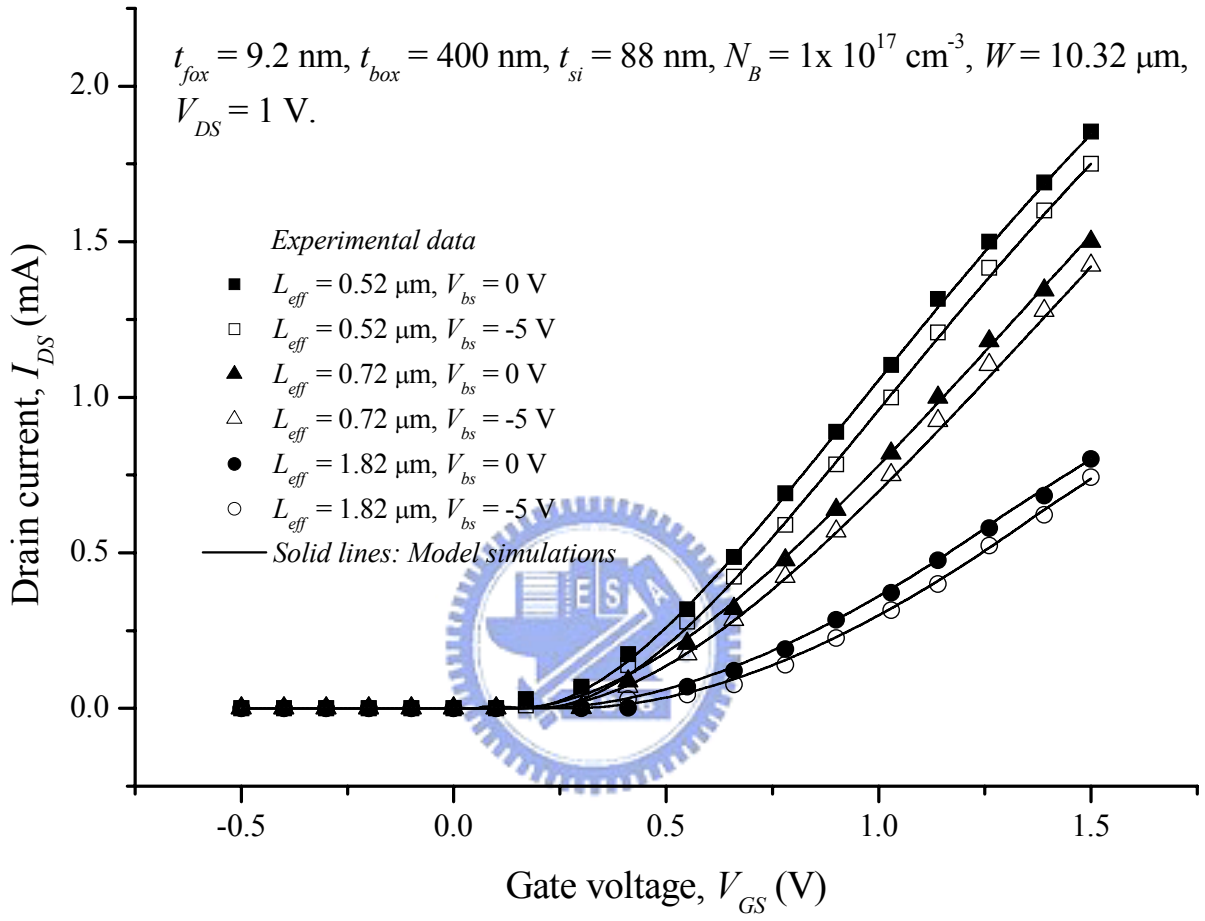

t_{fox} = 9.2 nm, t_{box} = 400 nm, t_{si} = 88 nm, N_B = 1x 10^{17} cm^{-3}, W = 10.32 μm,
V_{DS} = 1 V.
Experimental data
L_{eff} = 0.52 μm, V_{bs} = 0 V
L_{eff} = 0.52 μm, V_{bs} = -5 V
L_{eff} = 0.72 μm, V_{bs} = 0 V
L_{eff} = 0.72 μm, V_{bs} = -5 V
L_{eff} = 1.82 μm, V_{bs} = 0 V
L_{eff} = 1.82 μm, V_{bs} = -5 V
Solid lines: Model simulations
Drain current, I_{DS} (mA)
Gate voltage, V_{GS} (V)
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
0.5
1.0
1.5

Fig. 3–2(b)

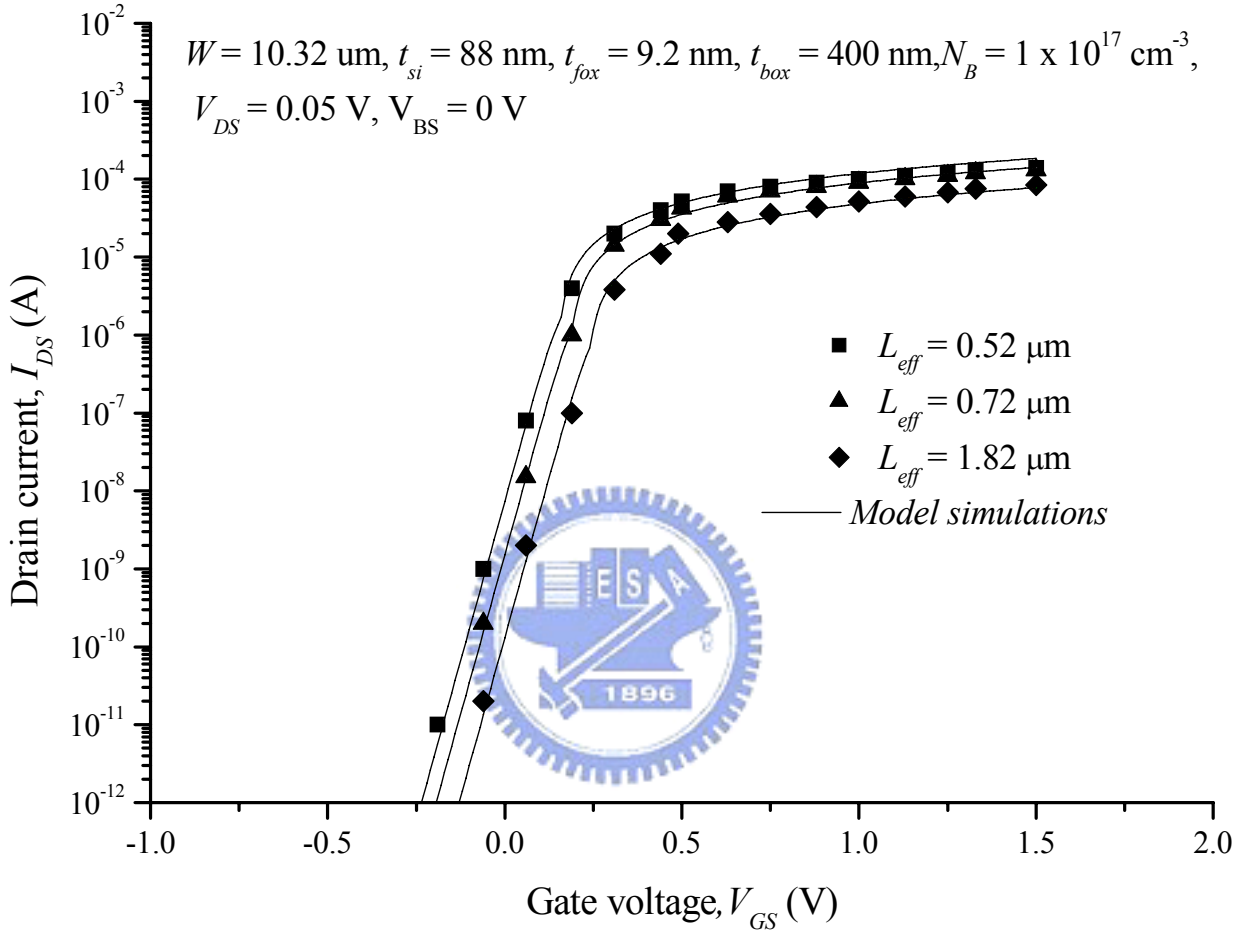

W = 10.32 um, t_si = 88 nm, t_fox = 9.2 nm, t_box = 400 nm, N_B = 1 x 10^17 cm^-3,
V_DS = 0.05 V, V_BS = 0 V
L_eff = 0.52 μm
L_eff = 0.72 μm
L_eff = 1.82 μm
Model simulations
Drain current, I_DS (A)
Gate voltage, V_GS (V)
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0

Fig. 3–3(a)

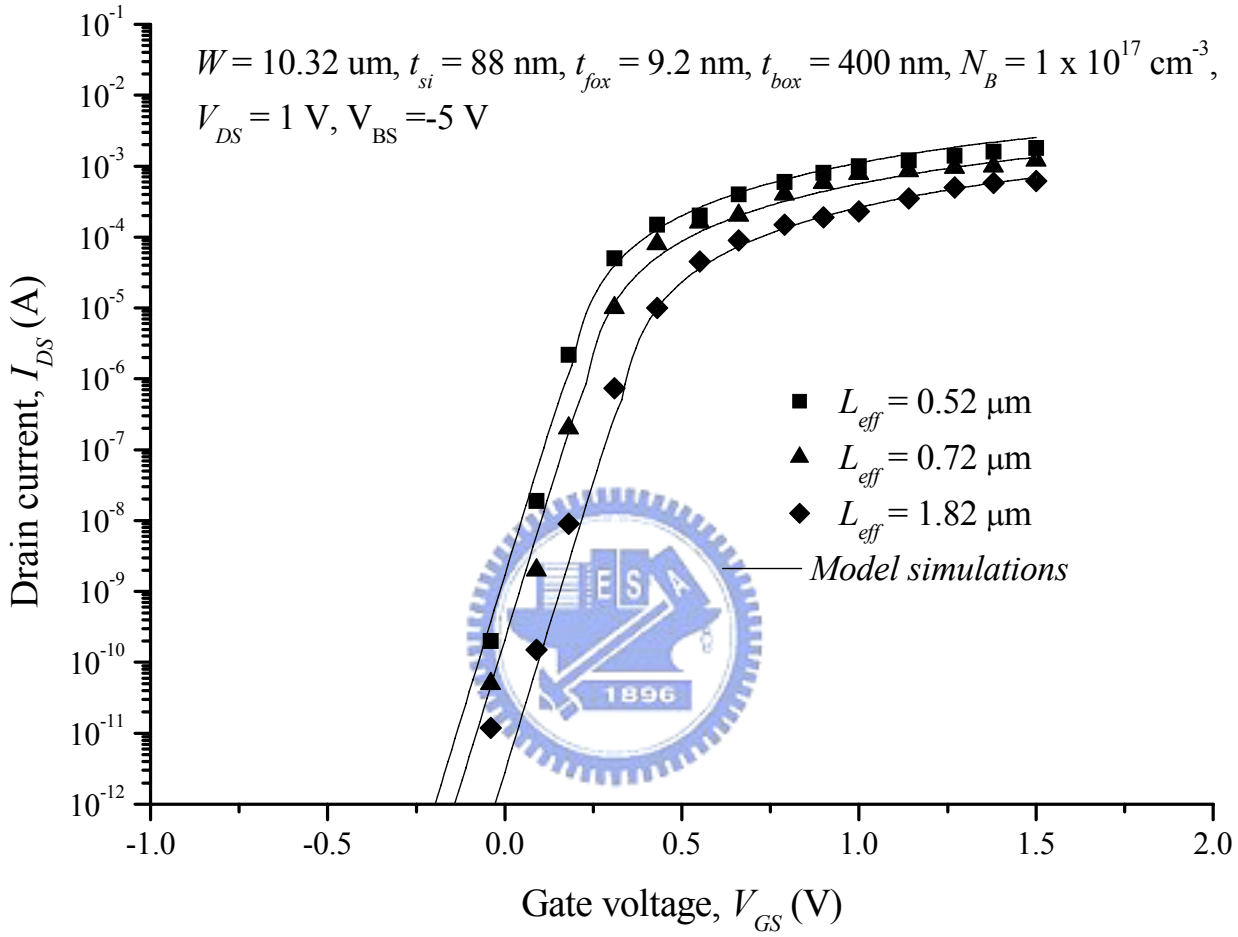

W = 10.32 um, t_si = 88 nm, t_fox = 9.2 nm, t_box = 400 nm, N_B = 1 x 10^17 cm^-3,
V_DS = 1 V, V_BS = -5 V
L_eff = 0.52 μm
L_eff = 0.72 μm
L_eff = 1.82 μm
Model simulations
Drain current, I_DS (A)
Gate voltage, V_GS (V)
10^-1
10^-2
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0

Fig. 3–3(b)

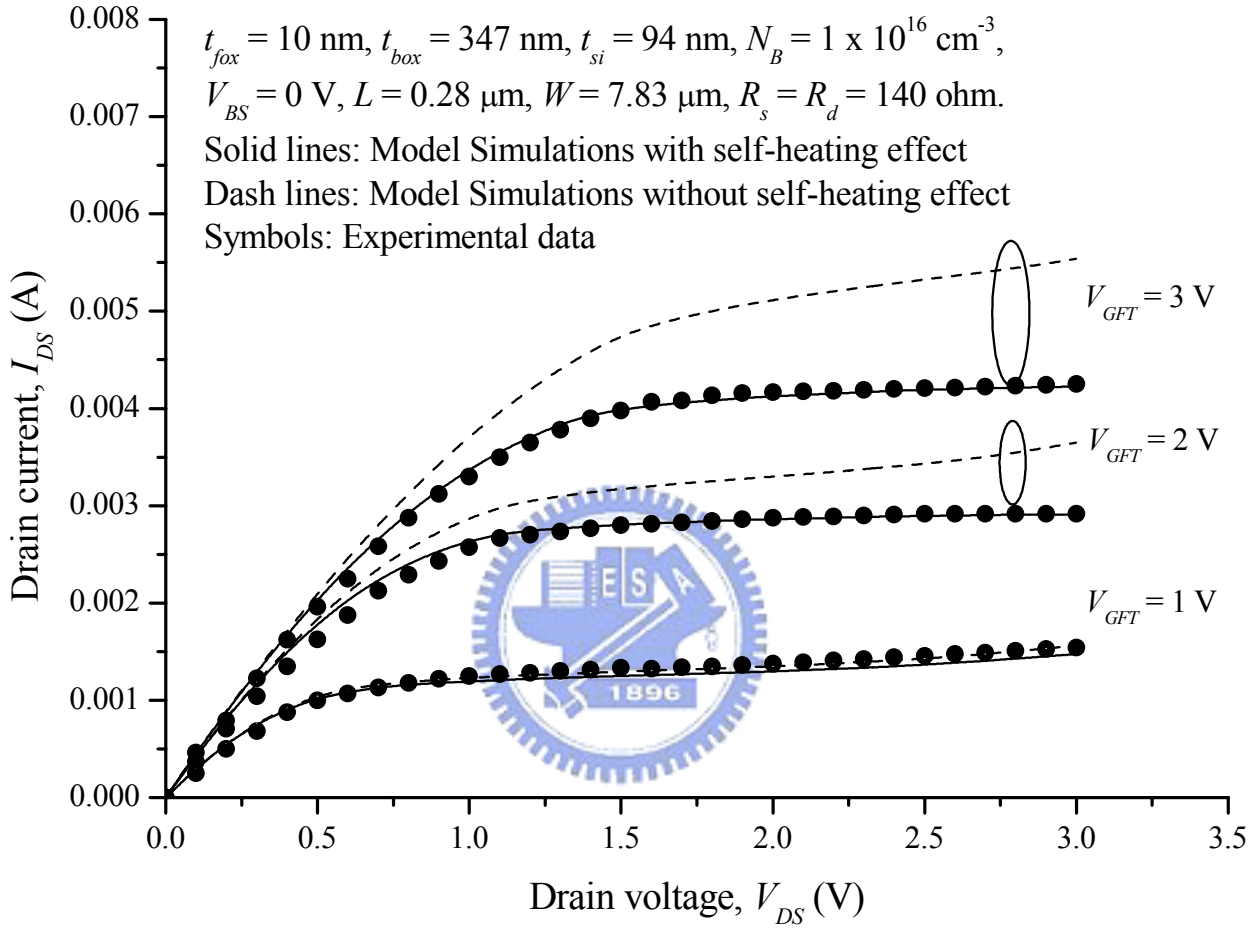

t_{fox} = 10 nm, t_{box} = 347 nm, t_{si} = 94 nm, N_B = 1 x 10^{16} cm^{-3},
V_{BS} = 0 V, L = 0.28 μm, W = 7.83 μm, R_s = R_d = 140 ohm.
Solid lines: Model Simulations with self-heating effect
Dash lines: Model Simulations without self-heating effect
Symbols: Experimental data
V_{GFT} = 3 V
V_{GFT} = 2 V
V_{GFT} = 1 V
Drain current, I_{DS} (A)
Drain voltage, V_{DS} (V)
0.000
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

Fig. 3–4(a)

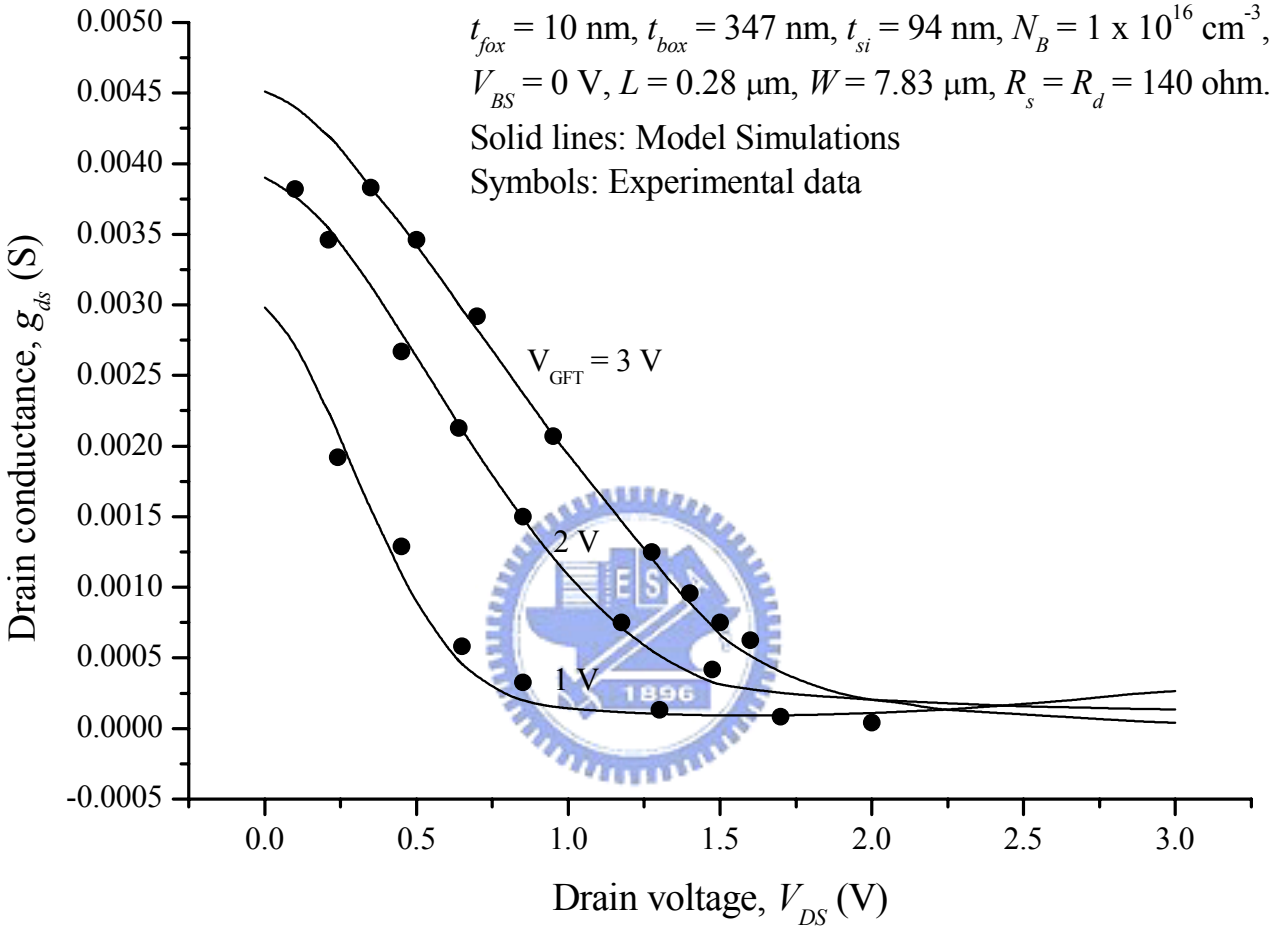

t_{fox} = 10 nm, t_{box} = 347 nm, t_{si} = 94 nm, N_B = 1 x 10^{16} cm^{-3},
V_{BS} = 0 V, L = 0.28 μm, W = 7.83 μm, R_s = R_d = 140 ohm.
Solid lines: Model Simulations
Symbols: Experimental data
V_{GFT} = 3 V
2 V
1 V
Drain conductance, g_{ds} (S)
Drain voltage, V_{DS} (V)
0.0050
0.0045
0.0040
0.0035
0.0030
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
-0.0005
0.0
0.5
1.0
1.5
2.0
2.5
3.0

Fig. 3–4(b)

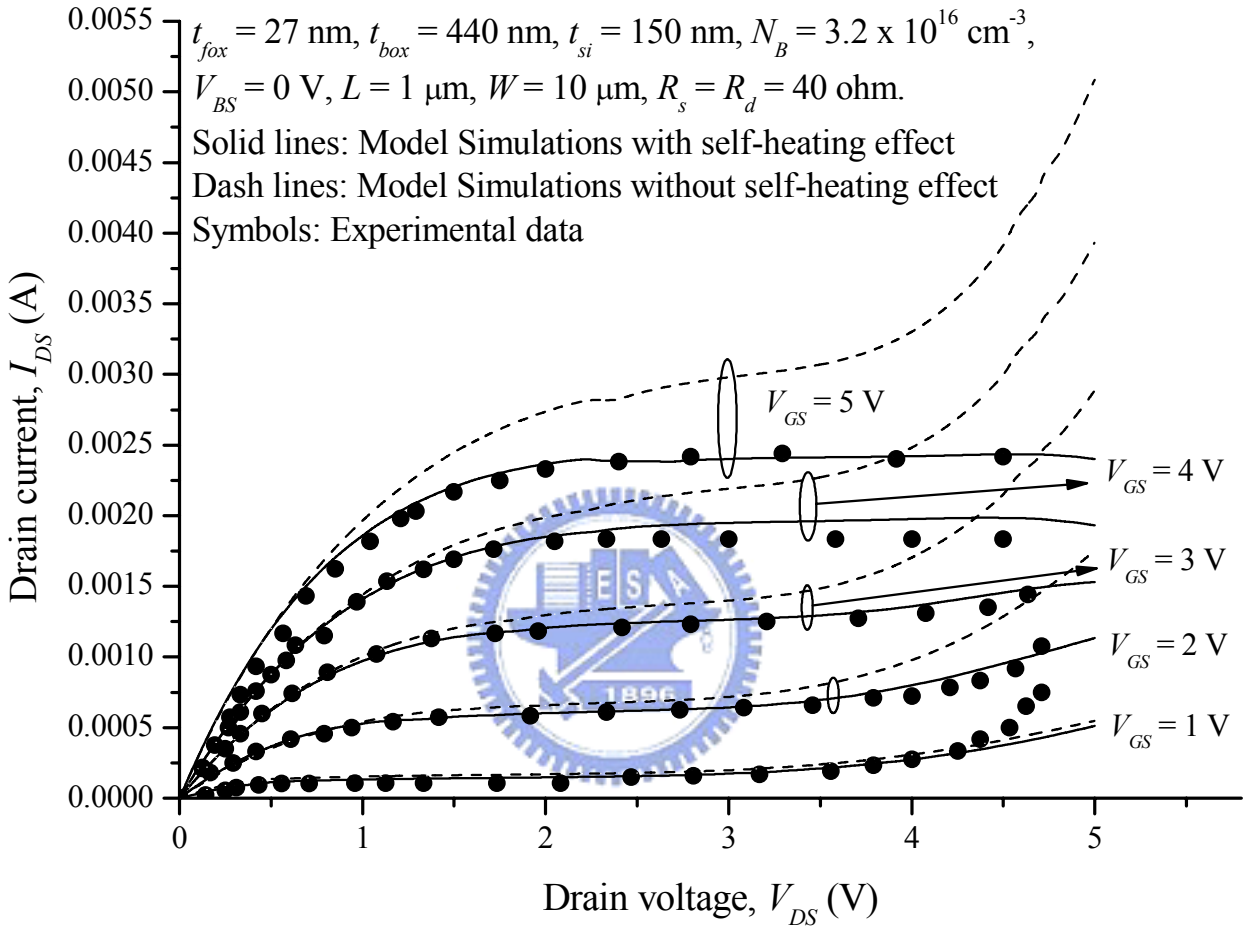

t_{fox} = 27 nm, t_{box} = 440 nm, t_{si} = 150 nm, N_B = 3.2 x 10^{16} cm^{-3},
V_{BS} = 0 V, L = 1 μm, W = 10 μm, R_s = R_d = 40 ohm.
Solid lines: Model Simulations with self-heating effect
Dash lines: Model Simulations without self-heating effect
Symbols: Experimental data
V_{GS} = 5 V
V_{GS} = 4 V
V_{GS} = 3 V
V_{GS} = 2 V
V_{GS} = 1 V
Drain current, I_{DS} (A)
Drain voltage, V_{DS} (V)
0.0055
0.0050
0.0045
0.0040
0.0035
0.0030
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
0
1
2
3
4
5

Fig. 3–5

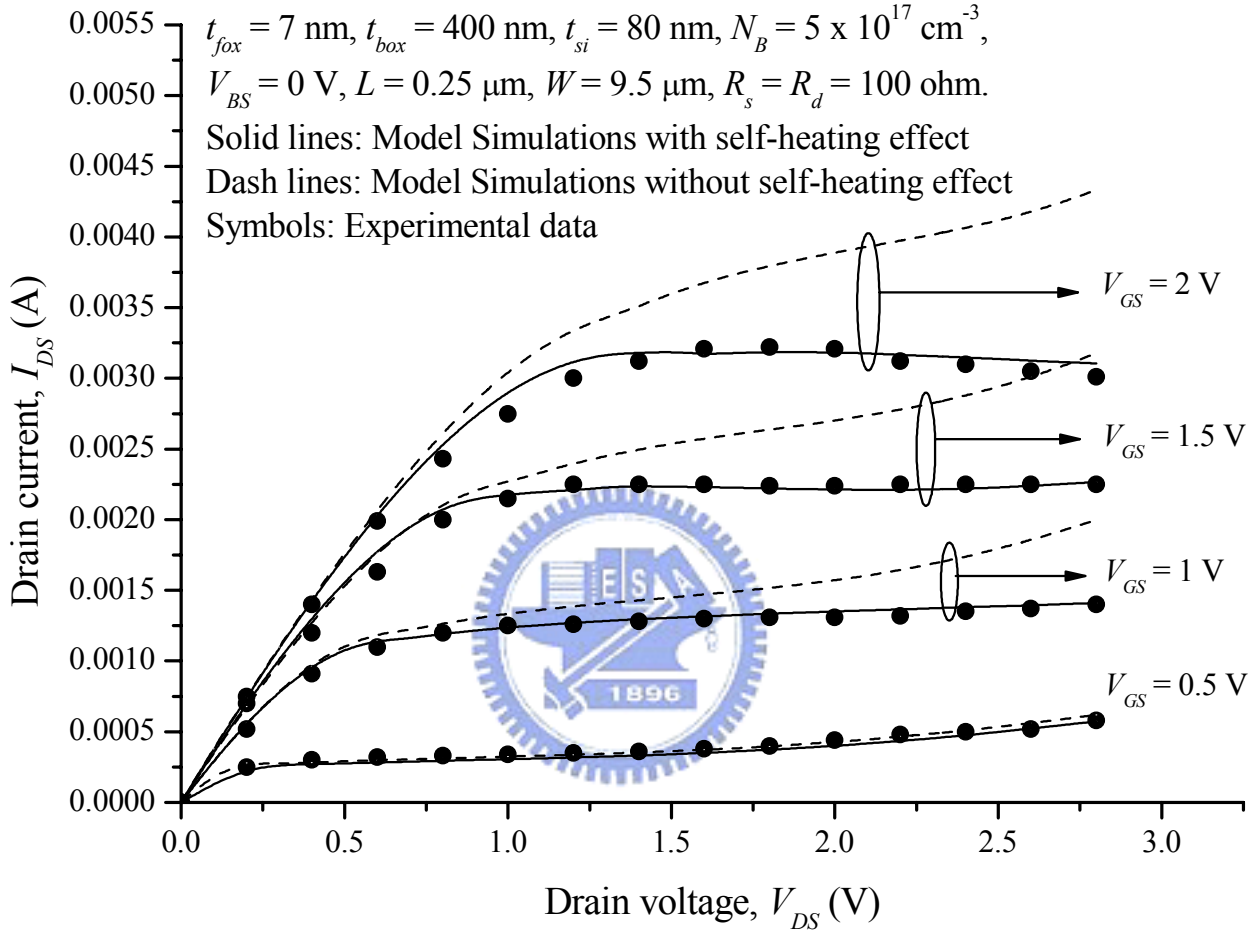

t_{fox} = 7 nm, t_{box} = 400 nm, t_{si} = 80 nm, N_B = 5 x 10^{17} cm^{-3},
V_{BS} = 0 V, L = 0.25 μm, W = 9.5 μm, R_s = R_d = 100 ohm.
Solid lines: Model Simulations with self-heating effect
Dash lines: Model Simulations without self-heating effect
Symbols: Experimental data
V_{GS} = 2 V
V_{GS} = 1.5 V
V_{GS} = 1 V
V_{GS} = 0.5 V
Drain current, I_{DS} (A)
Drain voltage, V_{DS} (V)
0.0055
0.0050
0.0045
0.0040
0.0035
0.0030
0.0025
0.0020
0.0015
0.0010
0.0005
0.0000
0.0
0.5
1.0
1.5
2.0
2.5
3.0

Fig. 3–6

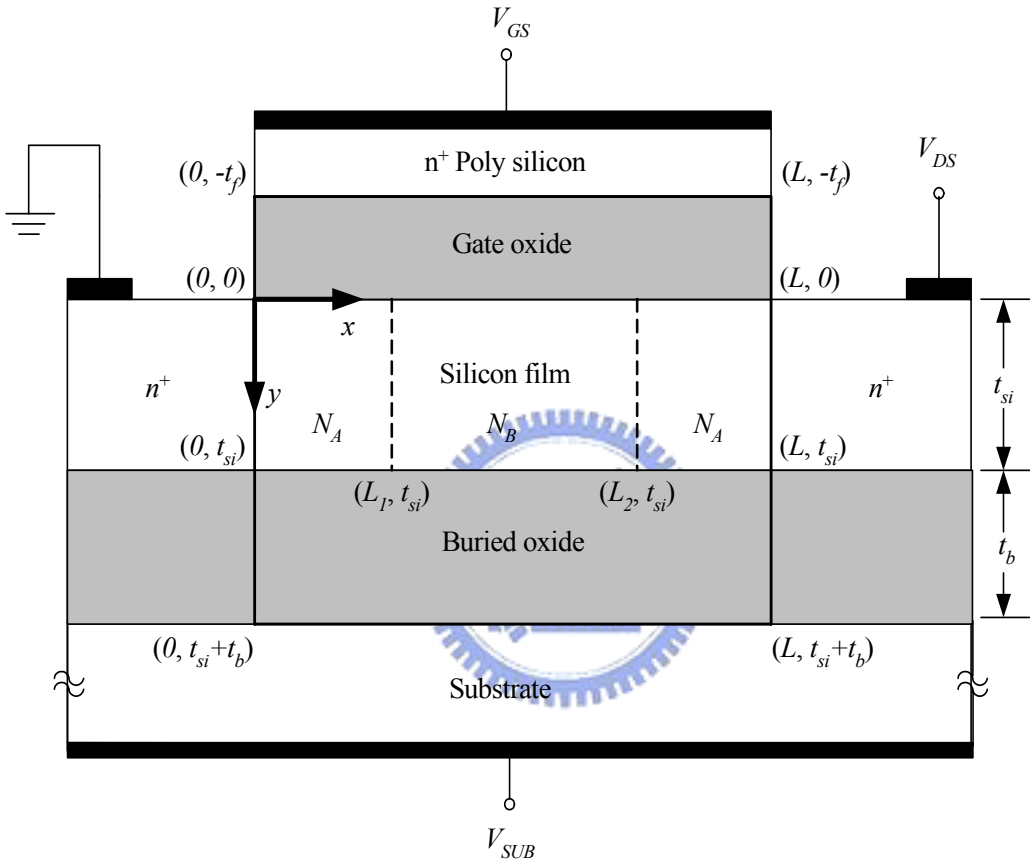

V_{GS}
n+ Poly silicon
$(0, -t_f)$
$(L, -t_f)$
V_{DS}
Gate oxide
$(0, 0)$
$(L, 0)$
x
y
n^+
Silicon film
n^+
N_A
N_B
N_A
t_{si}
$(0, t_{si})$
(L, t_{si})
(L_1, t_{si})
(L_2, t_{si})
Buried oxide
t_b
$(0, t_{si}+t_b)$
$(L, t_{si}+t_b)$
Substrate
V_{SUB}

Fig. 4–1

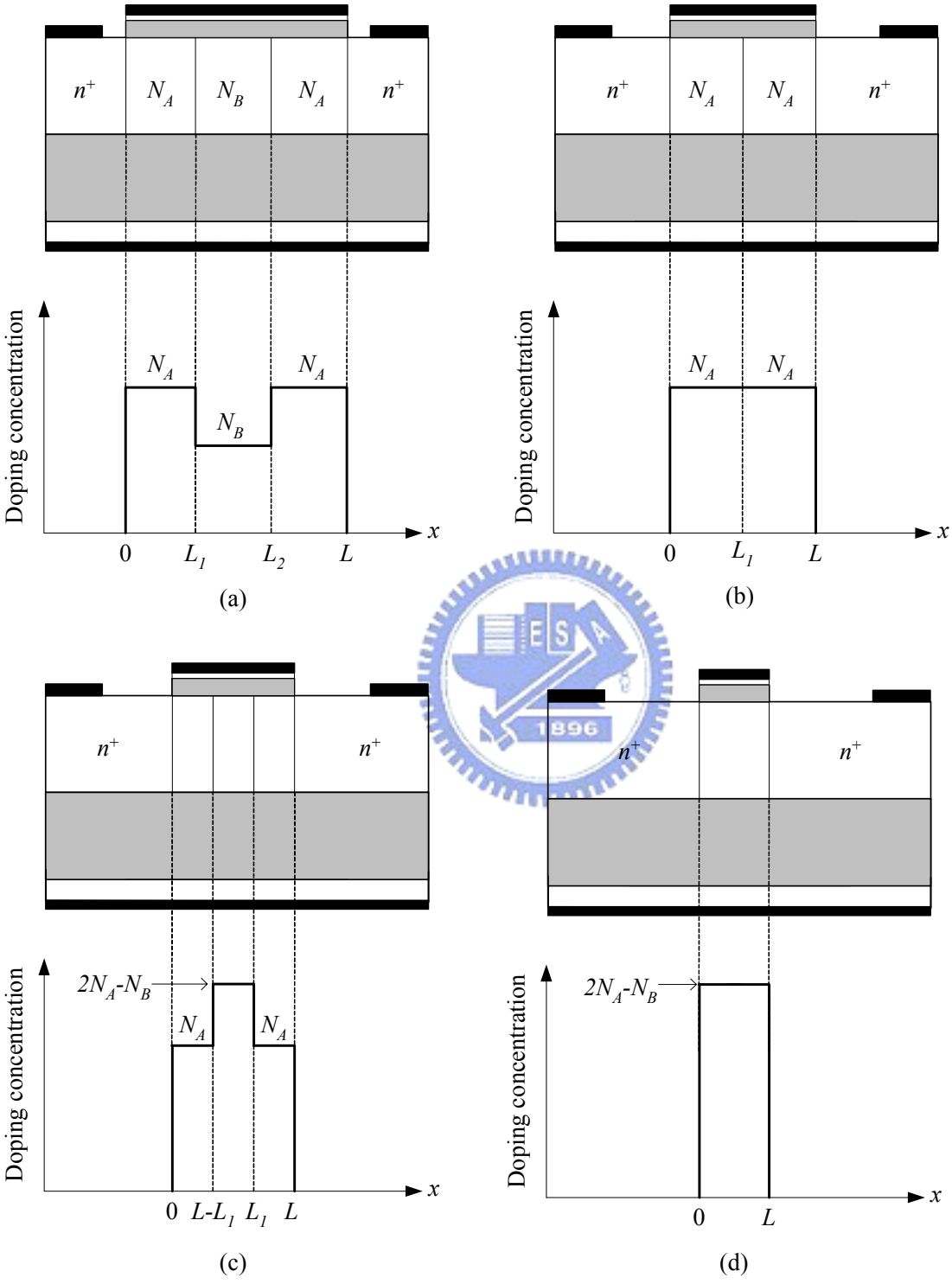

n^+
N_A
N_B
N_A
n^+
Doping concentration
N_A
N_B
N_A
x
0
L_1
L_2
L
(a)
n^+
N_A
N_A
n^+
Doping concentration
N_A
N_A
x
0
L_1
L
(b)
n^+
n^+
Doping concentration
$2N_A$-N_B
N_A
N_A
x
0
L-L_1
L_1
L
(c)
n^+
n^+
Doping concentration
$2N_A$-N_B
x
0
L
(d)

Fig. 4–2

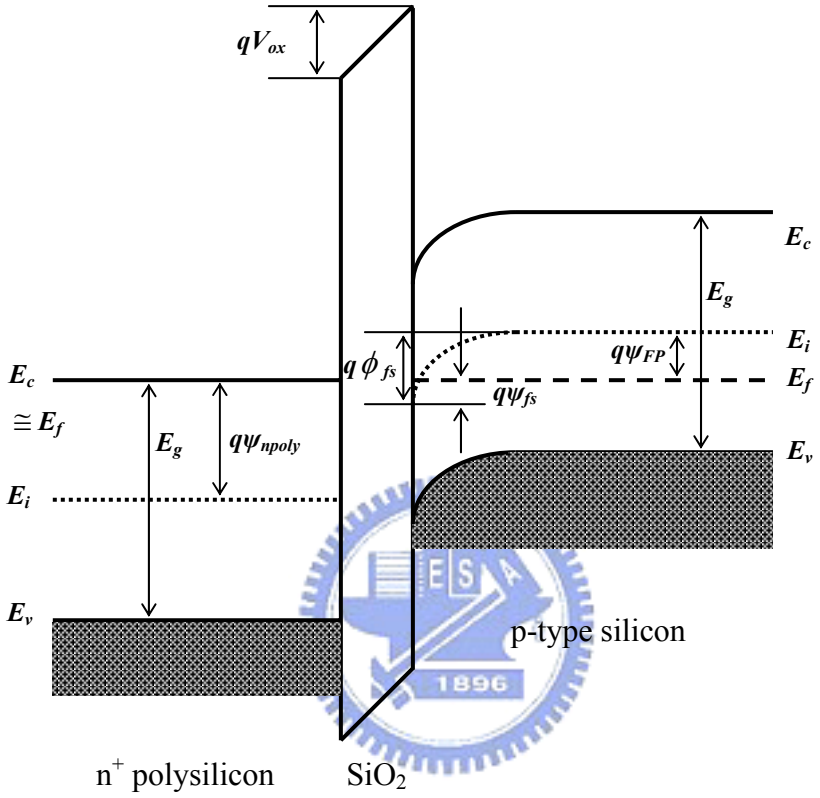

qV_{ox}
E_c
E_g
E_i
$q\psi_{FP}$
E_f
$q\phi_{fs}$
$q\psi_{fs}$
E_v
E_c
$\cong E_f$
E_g
$q\psi_{npoly}$
E_i
E_v
p-type silicon
n^+ polysilicon
SiO_2

Fig. 4–3

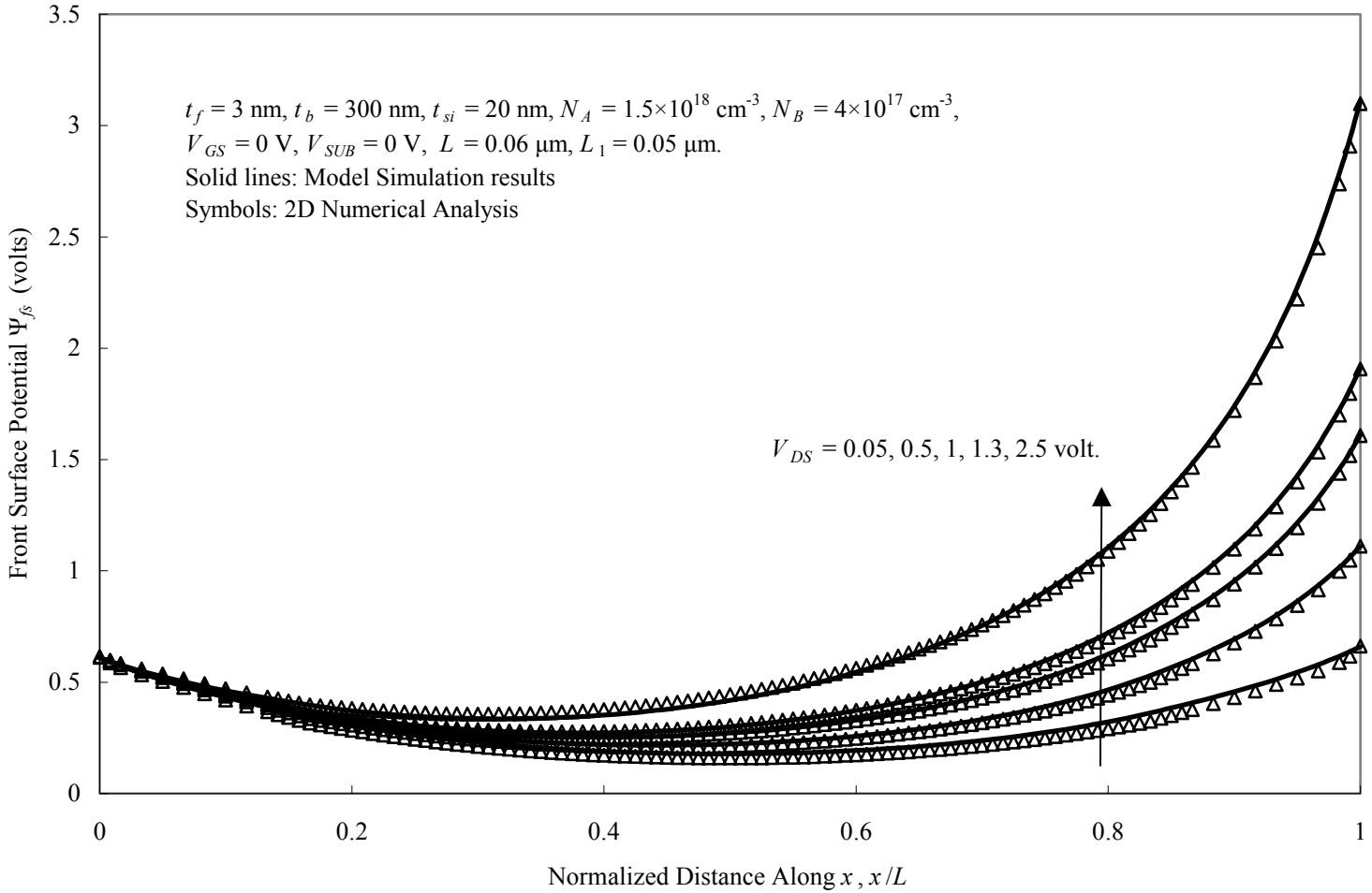

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5×10^18 cm^-3, N_B = 4×10^17 cm^-3,
V_{GS} = 0 V, V_{SUB} = 0 V, L = 0.06 μm, L_1 = 0.05 μm.
Solid lines: Model Simulation results
Symbols: 2D Numerical Analysis
V_{DS} = 0.05, 0.5, 1, 1.3, 2.5 volt.
Front Surface Potential Ψ_{fs} (volts)
Normalized Distance Along x, x/L
0
0.5
1
1.5
2
2.5
3
3.5
0.2
0.4
0.6
0.8

Fig. 4–4(a)

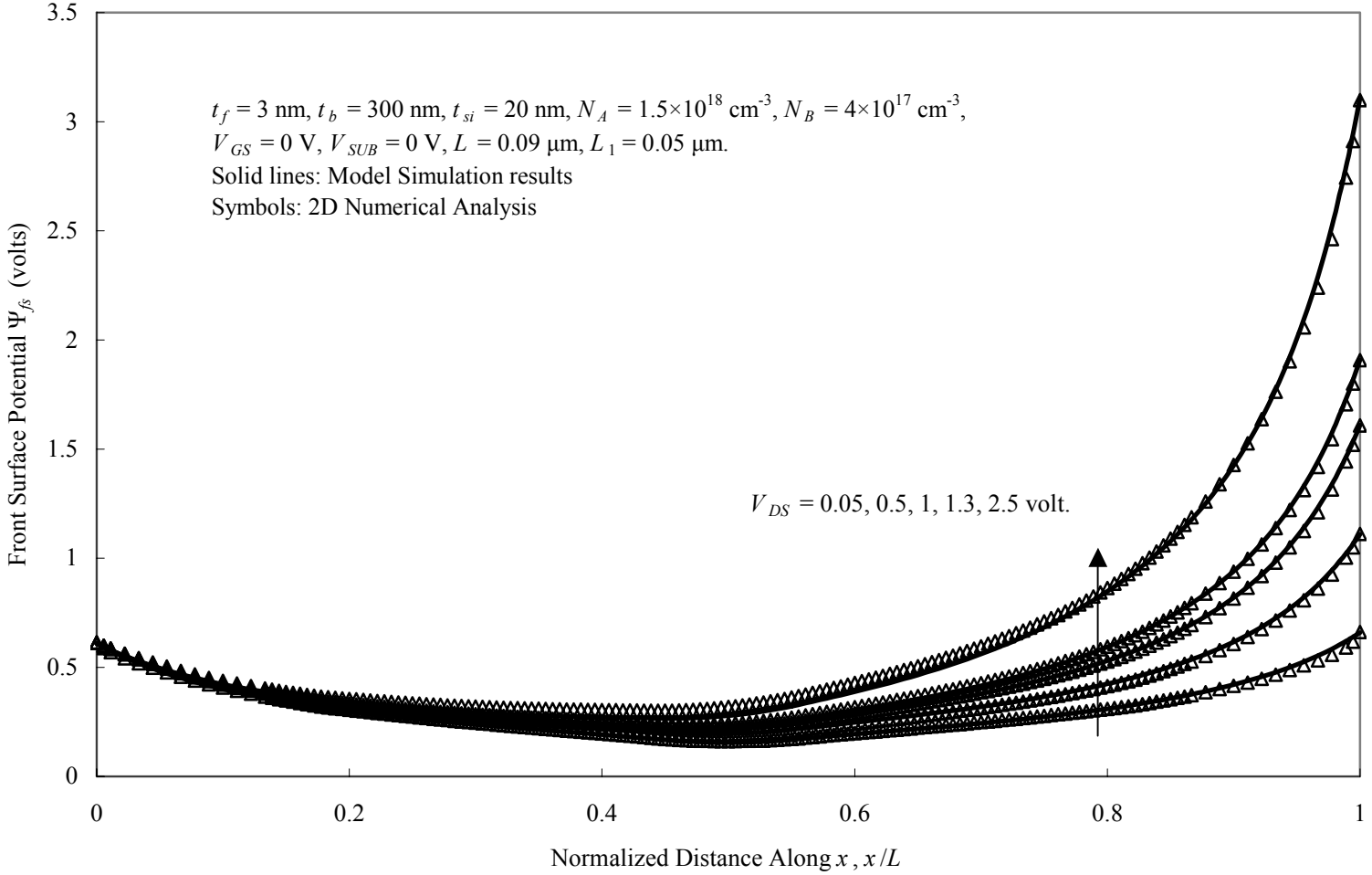

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5×10^18 cm^-3, N_B = 4×10^17 cm^-3,
V_{GS} = 0 V, V_{SUB} = 0 V, L = 0.09 μm, L_1 = 0.05 μm.
Solid lines: Model Simulation results
Symbols: 2D Numerical Analysis
V_{DS} = 0.05, 0.5, 1, 1.3, 2.5 volt.
Front Surface Potential Ψ_{fs} (volts)
Normalized Distance Along x, x/L
0
0.5
1
1.5
2
2.5
3
3.5
0.2
0.4
0.6
0.8

Fig. 4–4(b)

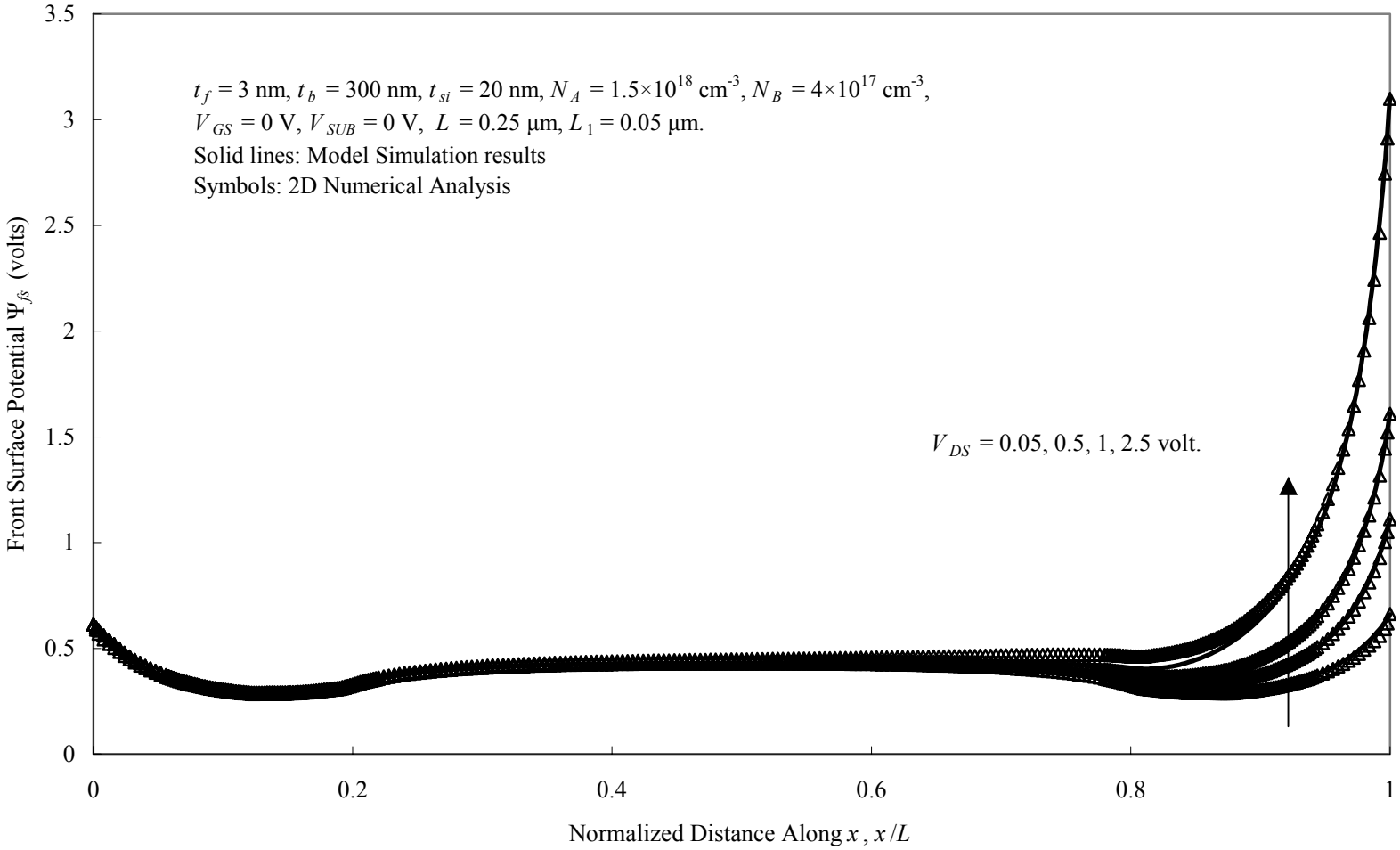

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5×10^18 cm^-3, N_B = 4×10^17 cm^-3,
V_{GS} = 0 V, V_{SUB} = 0 V, L = 0.25 μm, L_1 = 0.05 μm.
Solid lines: Model Simulation results
Symbols: 2D Numerical Analysis
V_{DS} = 0.05, 0.5, 1, 2.5 volt.
Front Surface Potential Ψ_{fs} (volts)
Normalized Distance Along x, x/L
0
0.5
1
1.5
2
2.5
3
3.5
0.2
0.4
0.6
0.8

Fig. 4–4(c)

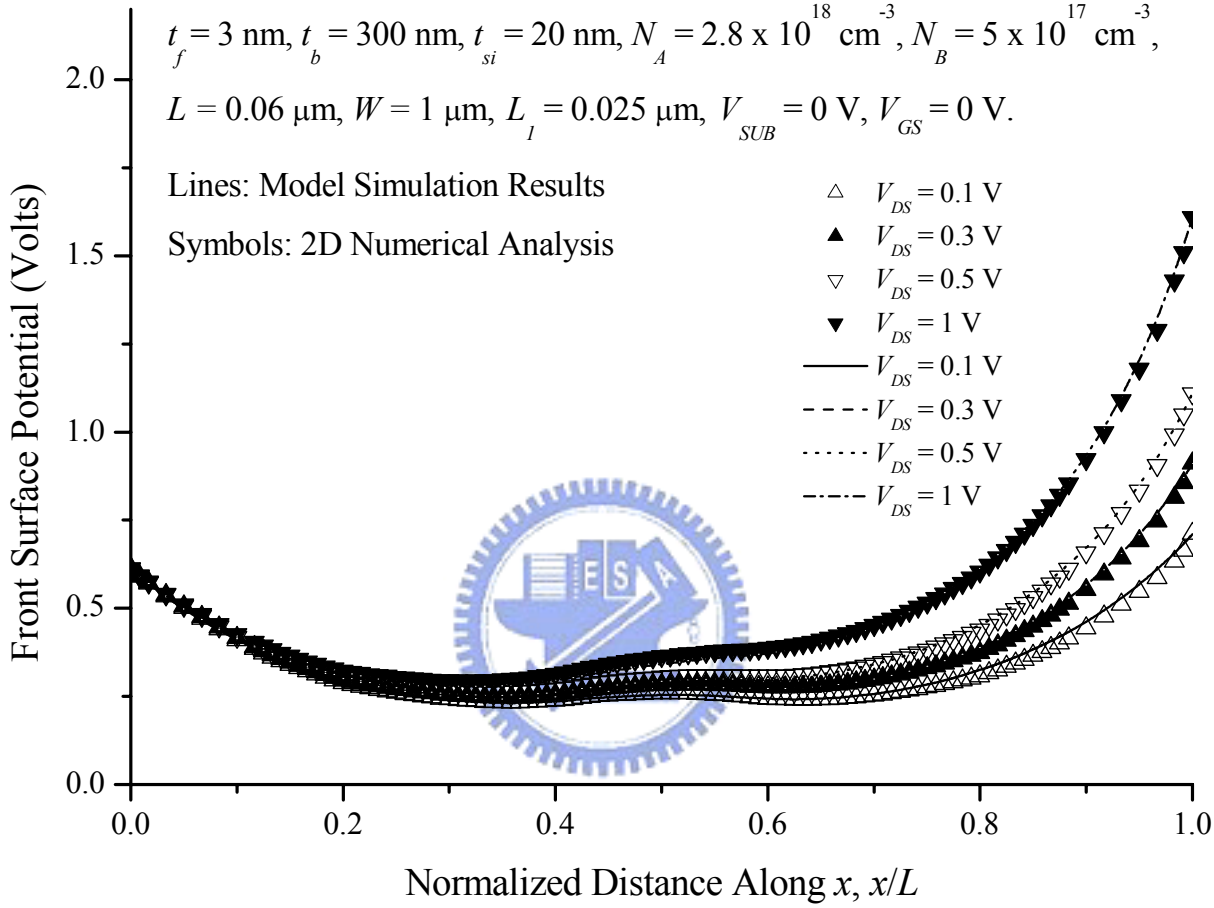

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x 10^{18} cm^{-3}, N_B = 5 x 10^{17} cm^{-3},
L = 0.06 μm, W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{GS} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{DS} = 0.1 V
V_{DS} = 0.3 V
V_{DS} = 0.5 V
V_{DS} = 1 V
V_{DS} = 0.1 V
V_{DS} = 0.3 V
V_{DS} = 0.5 V
V_{DS} = 1 V
Front Surface Potential (Volts)
Normalized Distance Along x, x/L
0.0
0.5
1.0
1.5
2.0
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–4(d)

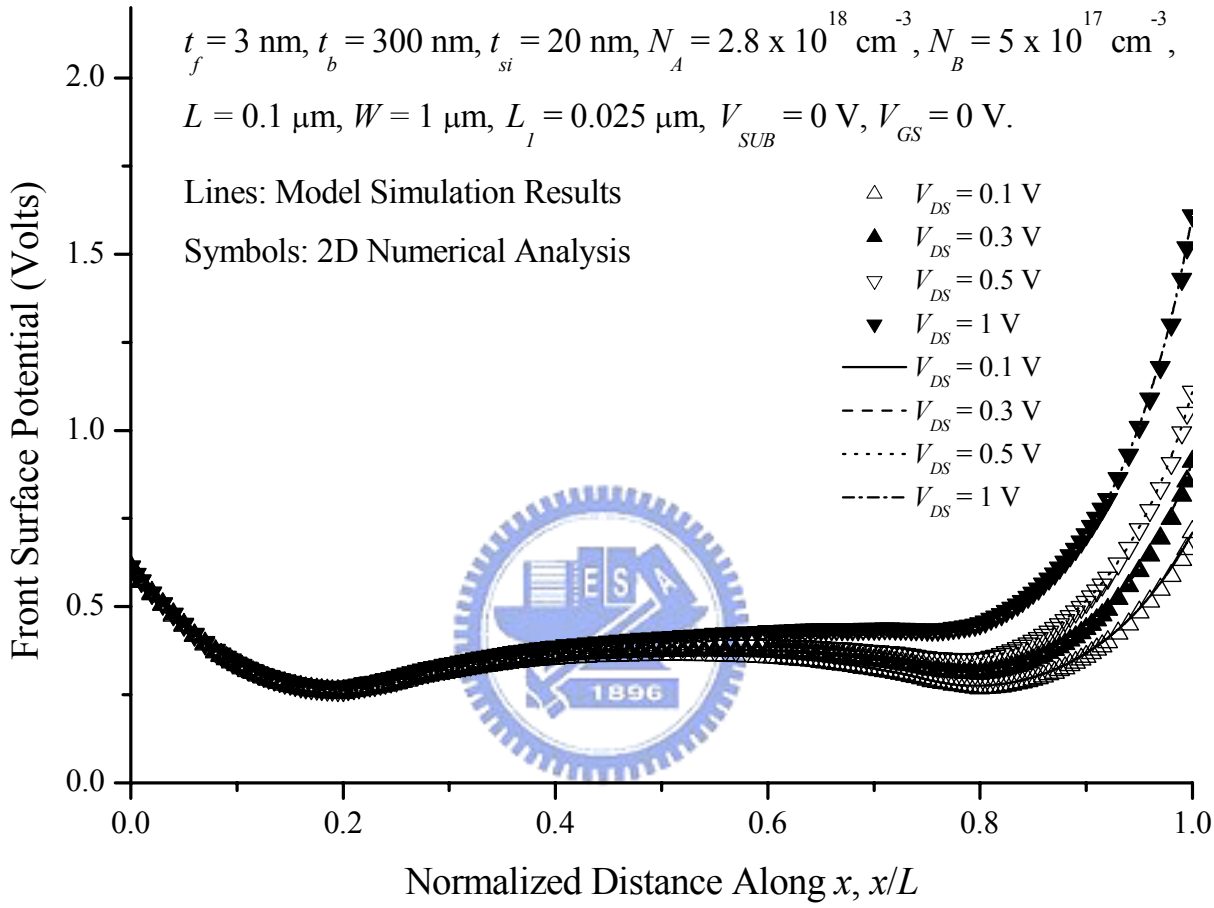

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x 10^{18} cm^{-3}, N_B = 5 x 10^{17} cm^{-3},
L = 0.1 μm, W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{GS} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{DS} = 0.1 V
V_{DS} = 0.3 V
V_{DS} = 0.5 V
V_{DS} = 1 V
V_{DS} = 0.1 V
V_{DS} = 0.3 V
V_{DS} = 0.5 V
V_{DS} = 1 V
Front Surface Potential (Volts)
0.0
0.5
1.0
1.5
2.0
0.0
0.2
0.4
0.6
0.8
1.0
Normalized Distance Along x, x/L

Fig. 4–4(e)

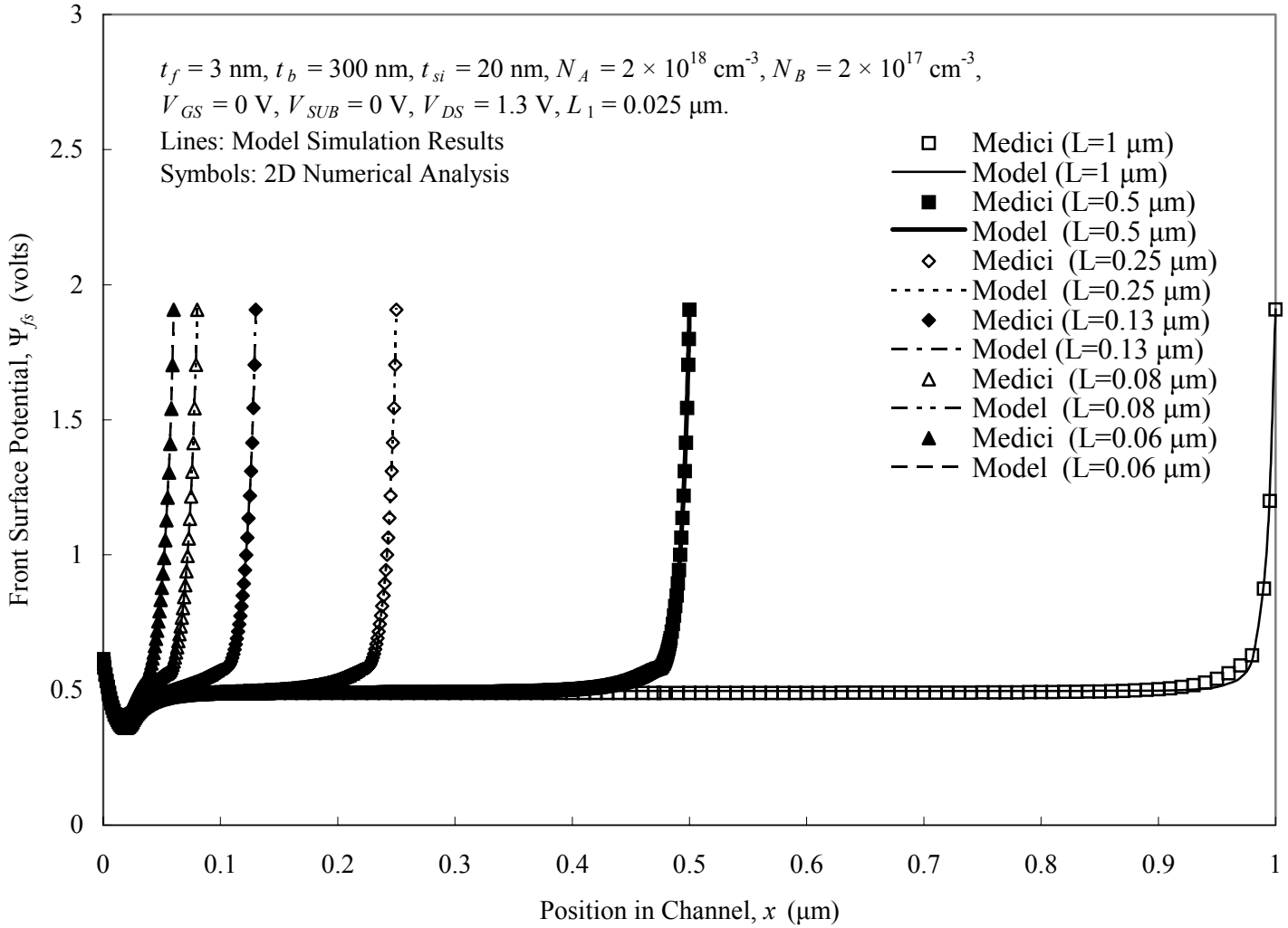

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, $N_A = 2 \times 10^{18}$ cm^{-3}, $N_B = 2 \times 10^{17}$ cm^{-3},
V_{GS} = 0 V, V_{SUB} = 0 V, V_{DS} = 1.3 V, L_1 = 0.025 μm.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
Medici (L=1 μm)
Model (L=1 μm)
Medici (L=0.5 μm)
Model (L=0.5 μm)
Medici (L=0.25 μm)
Model (L=0.25 μm)
Medici (L=0.13 μm)
Model (L=0.13 μm)
Medici (L=0.08 μm)
Model (L=0.08 μm)
Medici (L=0.06 μm)
Model (L=0.06 μm)
Front Surface Potential, Ψ_{fs} (volts)
Position in Channel, x (μm)
0
0.5
1
1.5
2
2.5
3
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

Fig. 4–5(a)

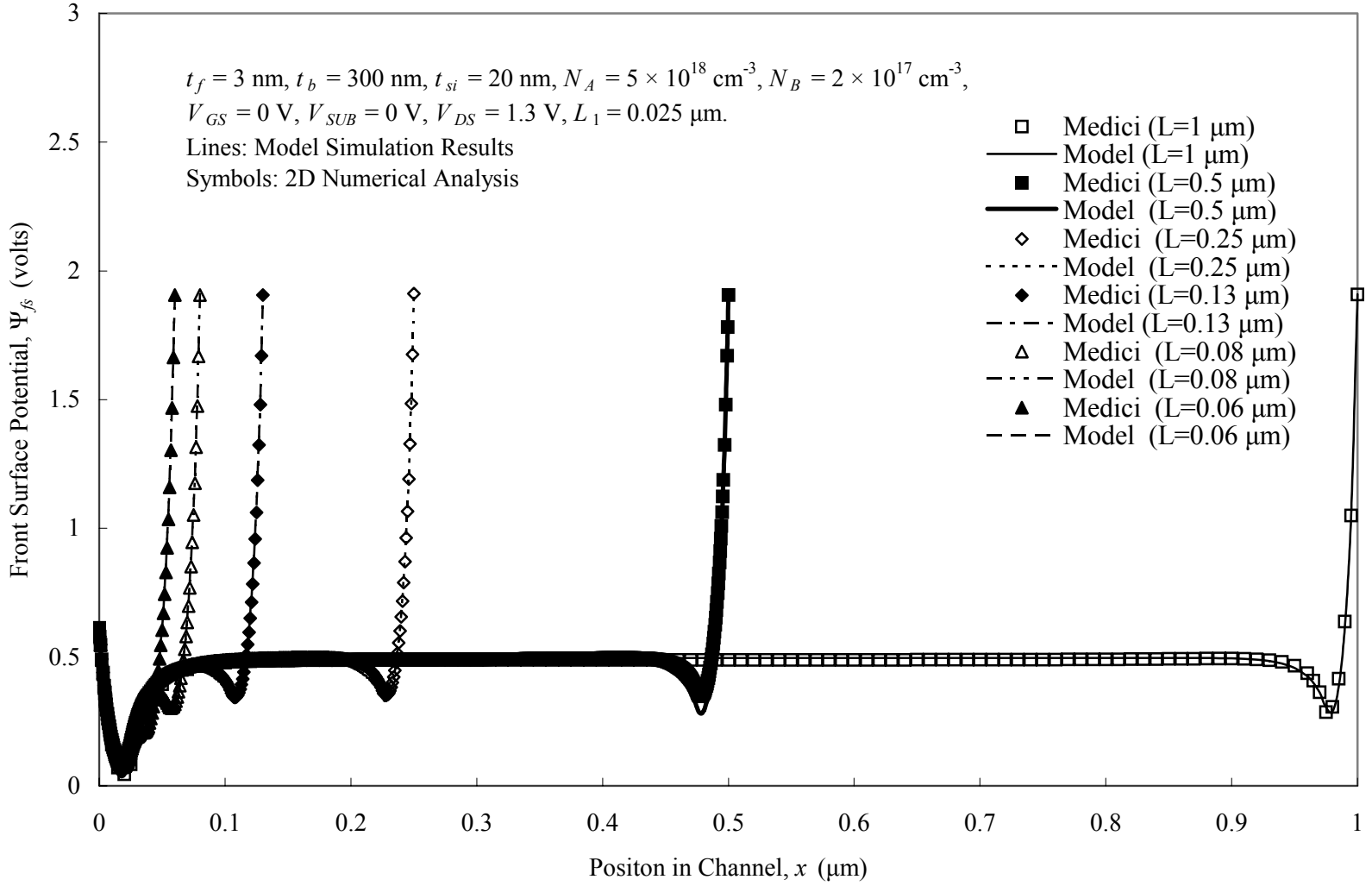

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, $N_A = 5 \times 10^{18}$ cm^{-3}, $N_B = 2 \times 10^{17}$ cm^{-3},
V_{GS} = 0 V, V_{SUB} = 0 V, V_{DS} = 1.3 V, L_1 = 0.025 μm.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
Medici (L=1 μm)
Model (L=1 μm)
Medici (L=0.5 μm)
Model (L=0.5 μm)
Medici (L=0.25 μm)
Model (L=0.25 μm)
Medici (L=0.13 μm)
Model (L=0.13 μm)
Medici (L=0.08 μm)
Model (L=0.08 μm)
Medici (L=0.06 μm)
Model (L=0.06 μm)
Front Surface Potential, Ψ_{fs} (volts)
Positon in Channel, x (μm)
0
0.5
1
1.5
2
2.5
3
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

Fig. 4–5(b)

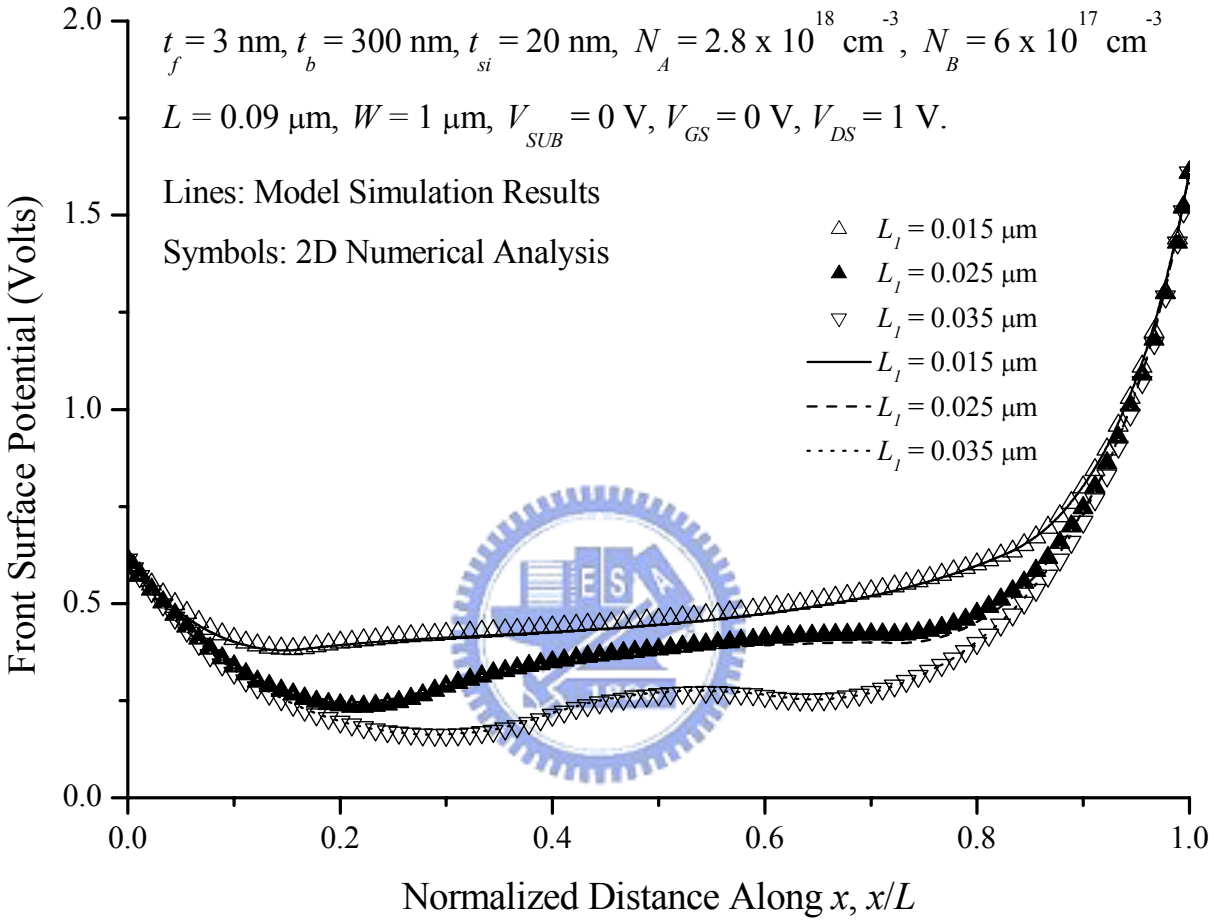

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x 10^{18} cm^{-3}, N_B = 6 x 10^{17} cm^{-3}
L = 0.09 μm, W = 1 μm, V_{SUB} = 0 V, V_{GS} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
L_1 = 0.015 μm
L_1 = 0.025 μm
L_1 = 0.035 μm
L_1 = 0.015 μm
L_1 = 0.025 μm
L_1 = 0.035 μm
Front Surface Potential (Volts)
Normalized Distance Along x, x/L
0.0
0.5
1.0
1.5
2.0
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–6

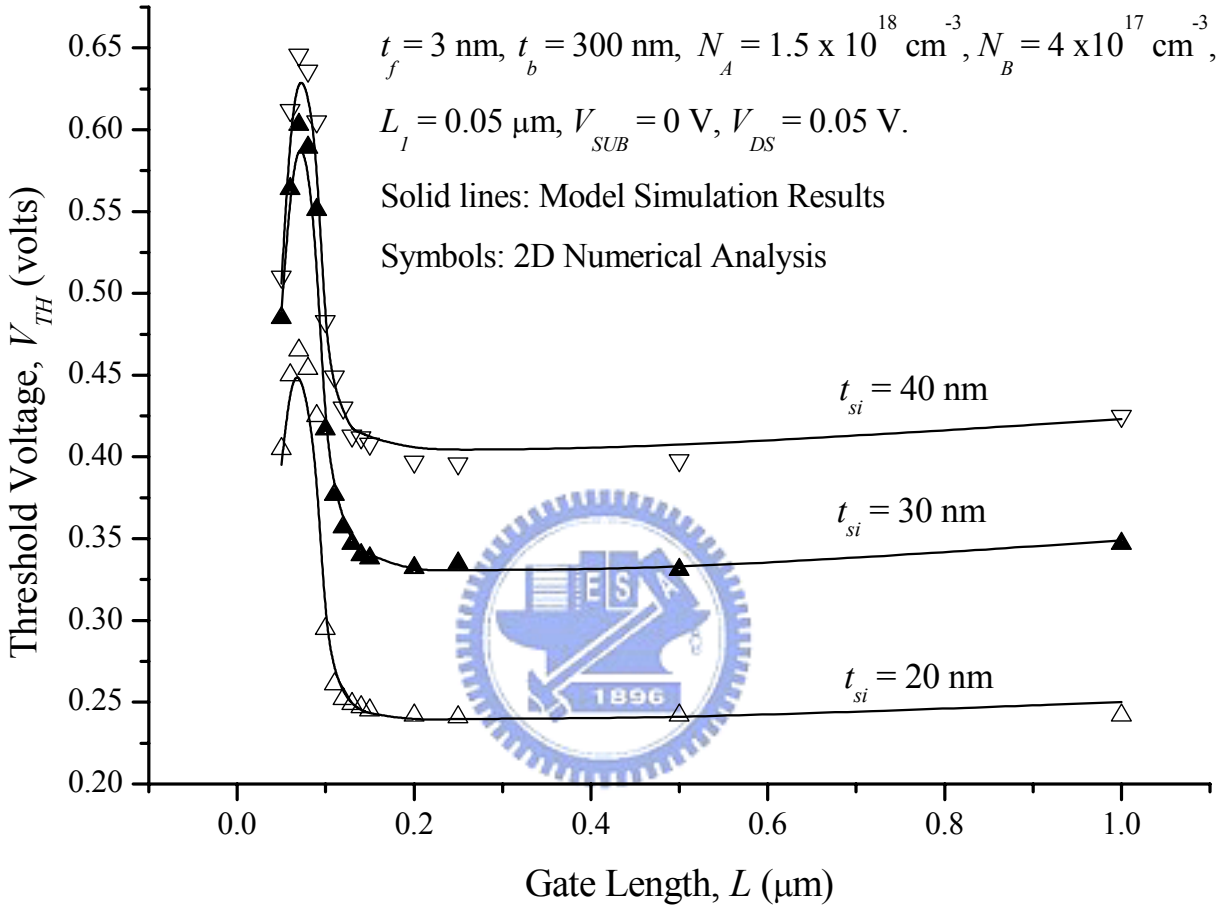

t_f = 3 nm, t_b = 300 nm, N_A = 1.5 x 10^{18} cm^{-3}, N_B = 4 x10^{17} cm^{-3},
L_1 = 0.05 μm, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Solid lines: Model Simulation Results
Symbols: 2D Numerical Analysis
t_{si} = 40 nm
t_{si} = 30 nm
t_{si} = 20 nm
Threshold Voltage, V_{TH} (volts)
Gate Length, L (μm)
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–7

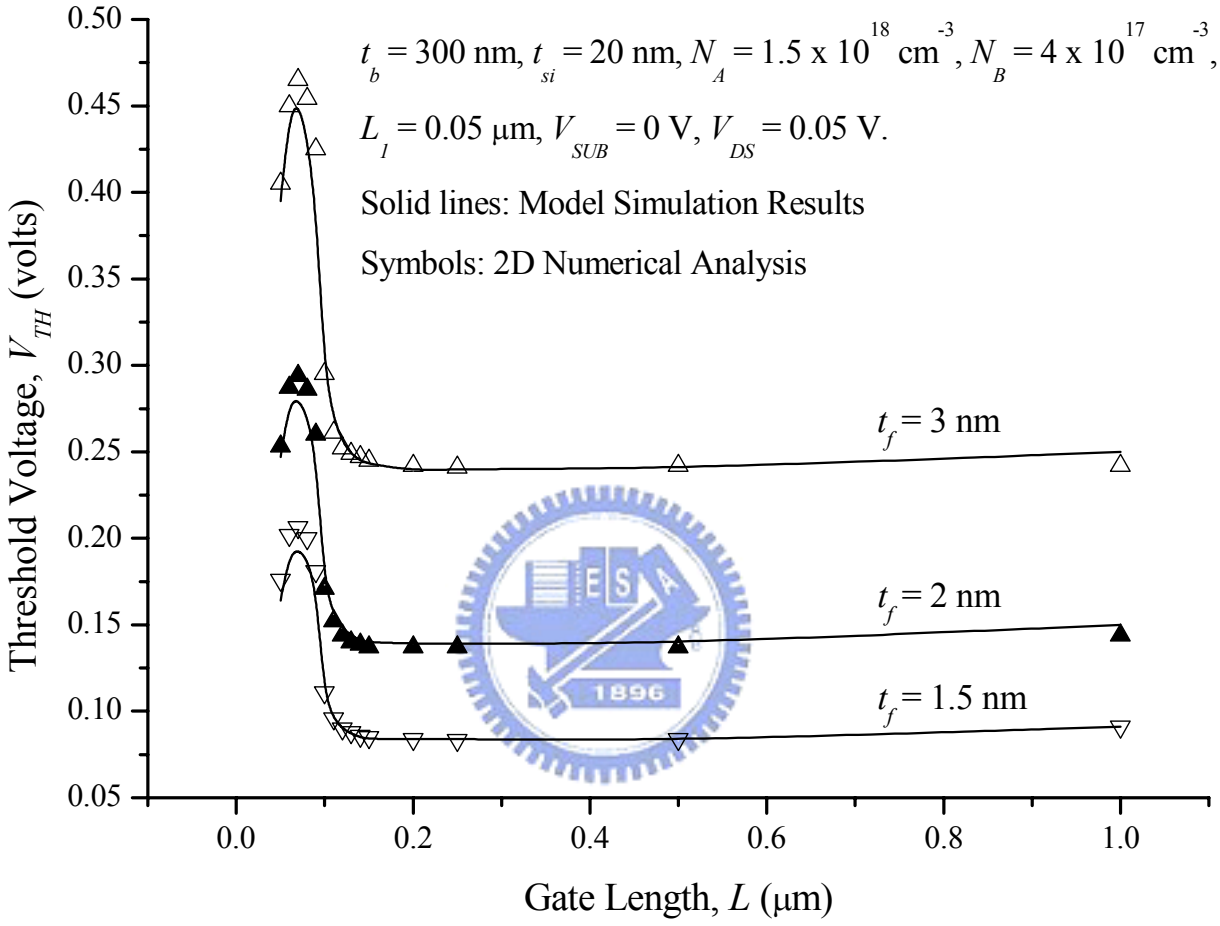

t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5 x 10^{18} cm^{-3}, N_B = 4 x 10^{17} cm^{-3},
L_1 = 0.05 μm, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Solid lines: Model Simulation Results
Symbols: 2D Numerical Analysis
t_f = 3 nm
t_f = 2 nm
t_f = 1.5 nm
Threshold Voltage, V_{TH} (volts)
Gate Length, L (μm)
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–8

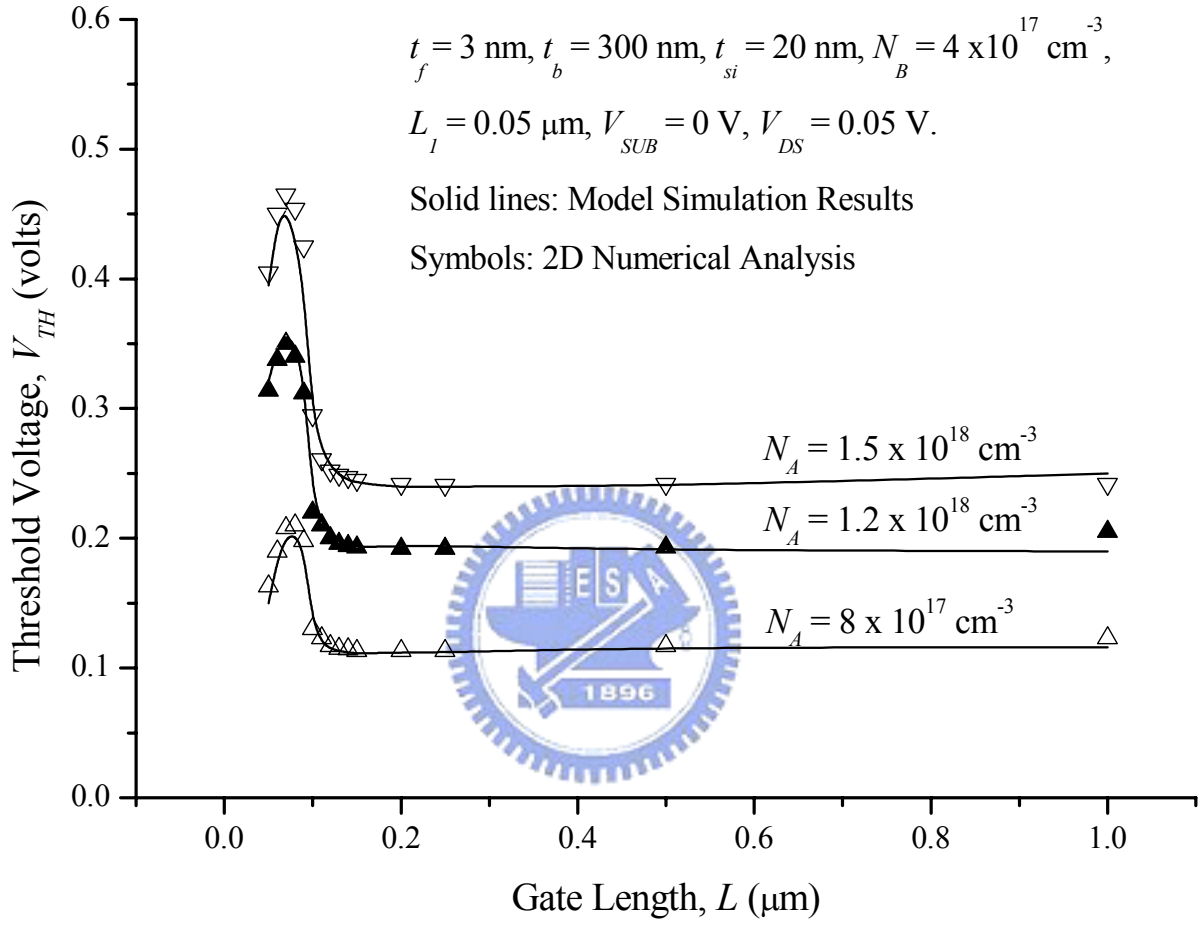

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 4 x10^{17} cm^{-3},
L_1 = 0.05 μm, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Solid lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 1.5 x 10^{18} cm^{-3}
N_A = 1.2 x 10^{18} cm^{-3}
N_A = 8 x 10^{17} cm^{-3}
Threshold Voltage, V_{TH} (volts)
Gate Length, L (μm)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–9

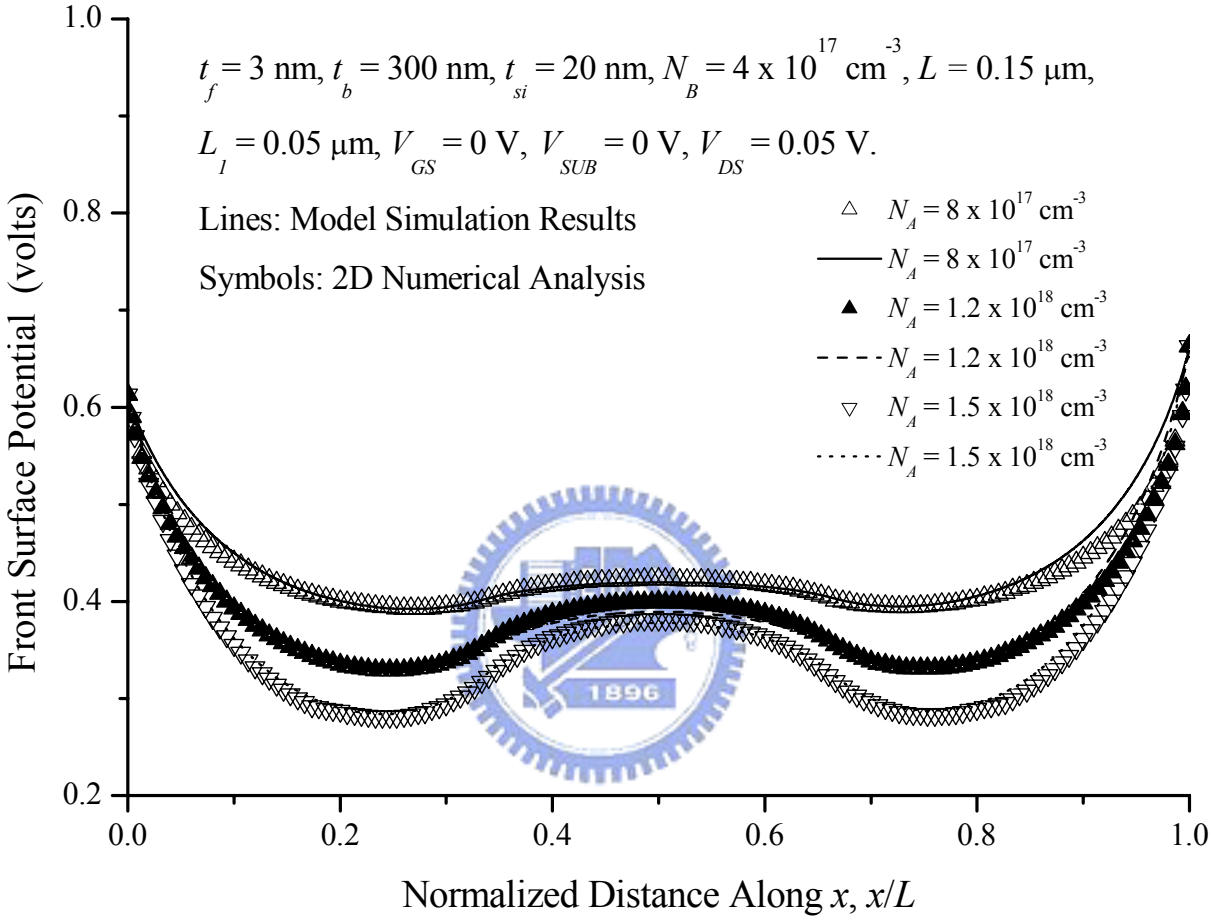

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 4 x 10^{17} cm^{-3}, L = 0.15 μm,
L_1 = 0.05 μm, V_{GS} = 0 V, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 8 x 10^{17} cm^{-3}
N_A = 8 x 10^{17} cm^{-3}
N_A = 1.2 x 10^{18} cm^{-3}
N_A = 1.2 x 10^{18} cm^{-3}
N_A = 1.5 x 10^{18} cm^{-3}
N_A = 1.5 x 10^{18} cm^{-3}
Front Surface Potential (volts)
1.0
0.8
0.6
0.4
0.2
0.0
0.2
0.4
0.6
0.8
1.0
Normalized Distance Along x, x/L

Fig. 4–10(a)

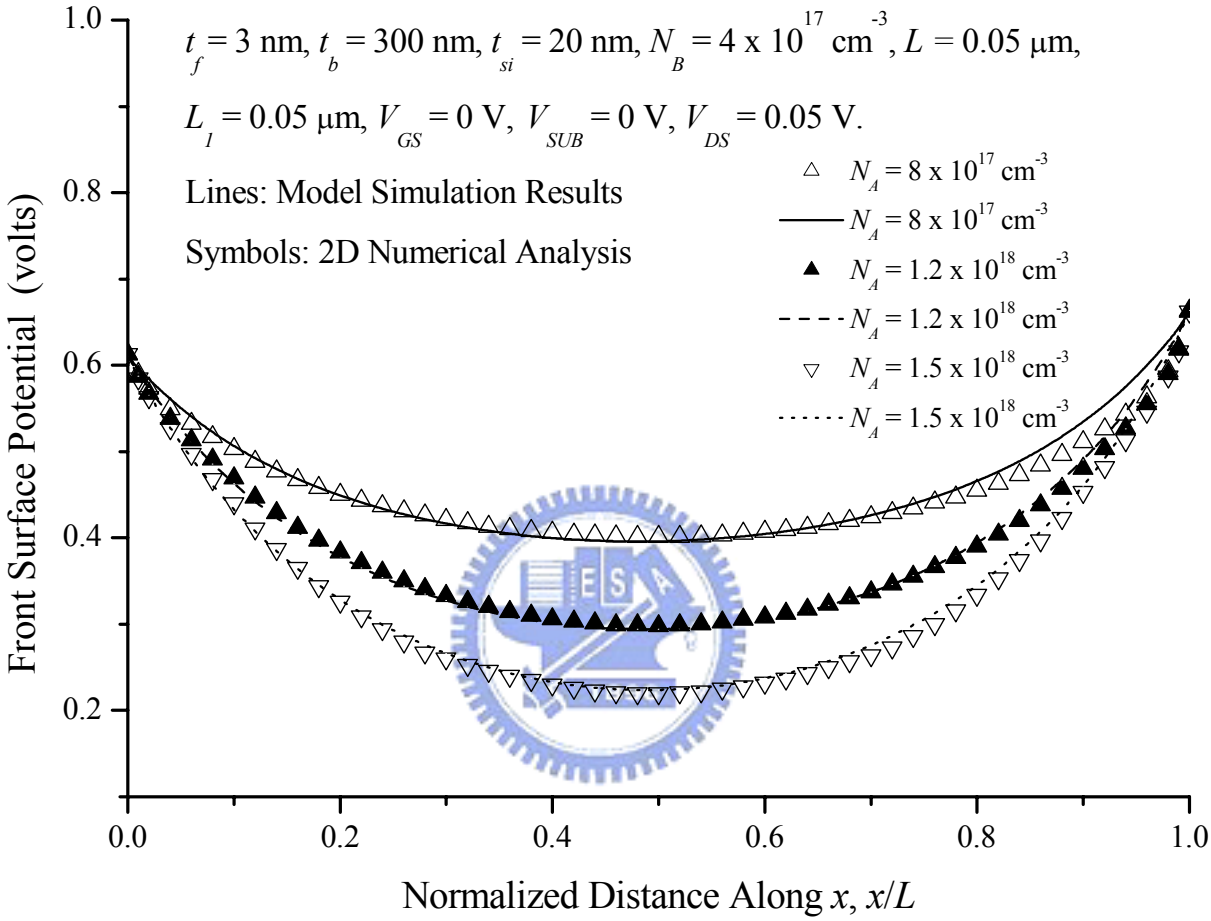

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 4 x 10^{17} cm^{-3}, L = 0.05 μm,
L_1 = 0.05 μm, V_{GS} = 0 V, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 8 x 10^{17} cm^{-3}
N_A = 8 x 10^{17} cm^{-3}
N_A = 1.2 x 10^{18} cm^{-3}
N_A = 1.2 x 10^{18} cm^{-3}
N_A = 1.5 x 10^{18} cm^{-3}
N_A = 1.5 x 10^{18} cm^{-3}
Front Surface Potential (volts)
1.0
0.8
0.6
0.4
0.2
0.0
0.2
0.4
0.6
0.8
1.0
Normalized Distance Along x, x/L

Fig. 4–10(b)

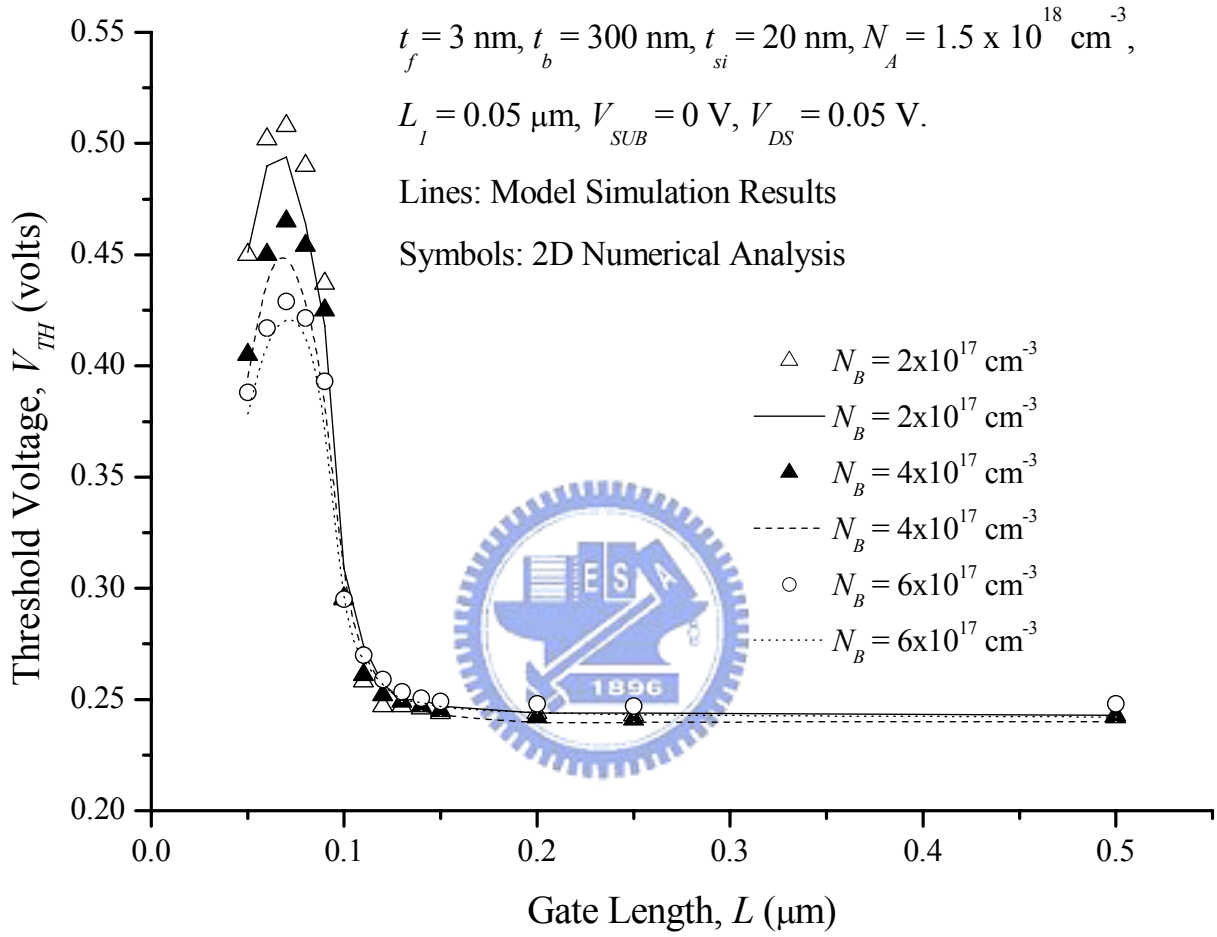

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5 x 10^{18} cm^{-3},
L_1 = 0.05 μm, V_{SUB} = 0 V, V_{DS} = 0.05 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 2x10^{17} cm^{-3}
N_B = 2x10^{17} cm^{-3}
N_B = 4x10^{17} cm^{-3}
N_B = 4x10^{17} cm^{-3}
N_B = 6x10^{17} cm^{-3}
N_B = 6x10^{17} cm^{-3}
Threshold Voltage, V_{TH} (volts)
Gate Length, L (μm)
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.0
0.1
0.2
0.3
0.4
0.5

Fig. 4–11

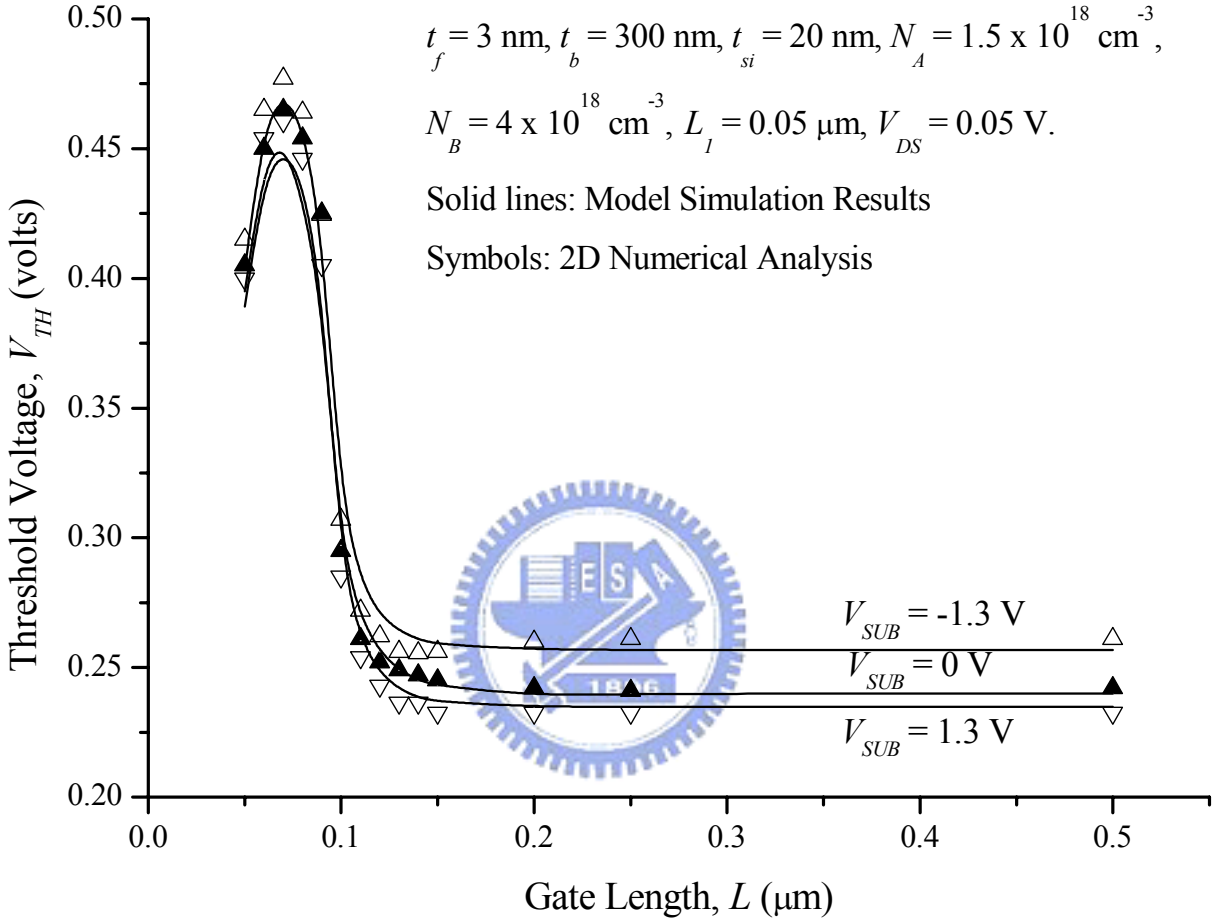

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5 x 10^18 cm^-3,
N_B = 4 x 10^18 cm^-3, L_1 = 0.05 μm, V_{DS} = 0.05 V.
Solid lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{SUB} = -1.3 V
V_{SUB} = 0 V
V_{SUB} = 1.3 V
Threshold Voltage, V_{TH} (volts)
Gate Length, L (μm)
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.0
0.1
0.2
0.3
0.4
0.5

Fig. 4–12

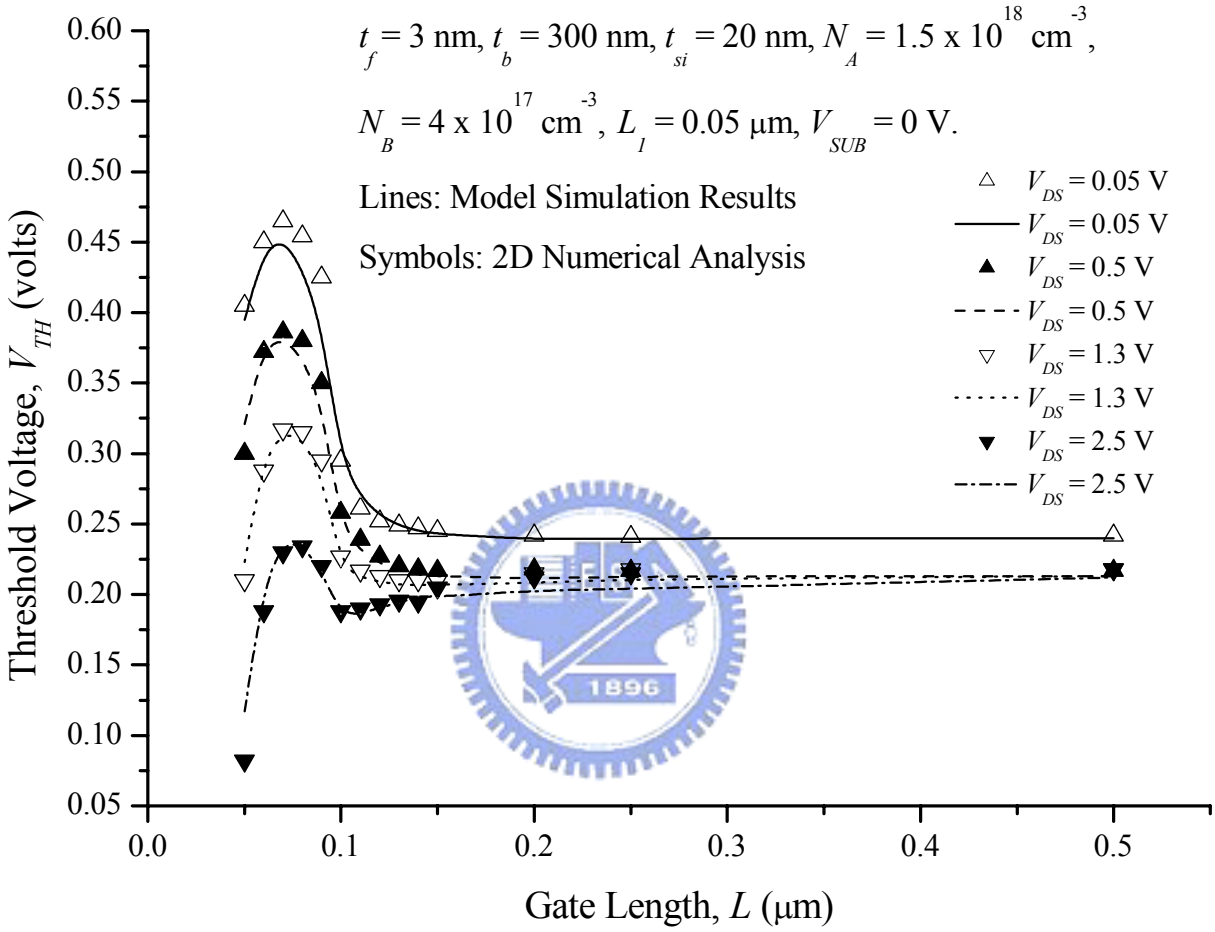

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 1.5 x 10^{18} cm^{-3},
N_B = 4 x 10^{17} cm^{-3}, L_1 = 0.05 μm, V_{SUB} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{DS} = 0.05 V
V_{DS} = 0.05 V
V_{DS} = 0.5 V
V_{DS} = 0.5 V
V_{DS} = 1.3 V
V_{DS} = 1.3 V
V_{DS} = 2.5 V
V_{DS} = 2.5 V
Threshold Voltage, V_{TH} (volts)
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.0
0.1
0.2
0.3
0.4
0.5
Gate Length, L (μm)

Fig. 4–13

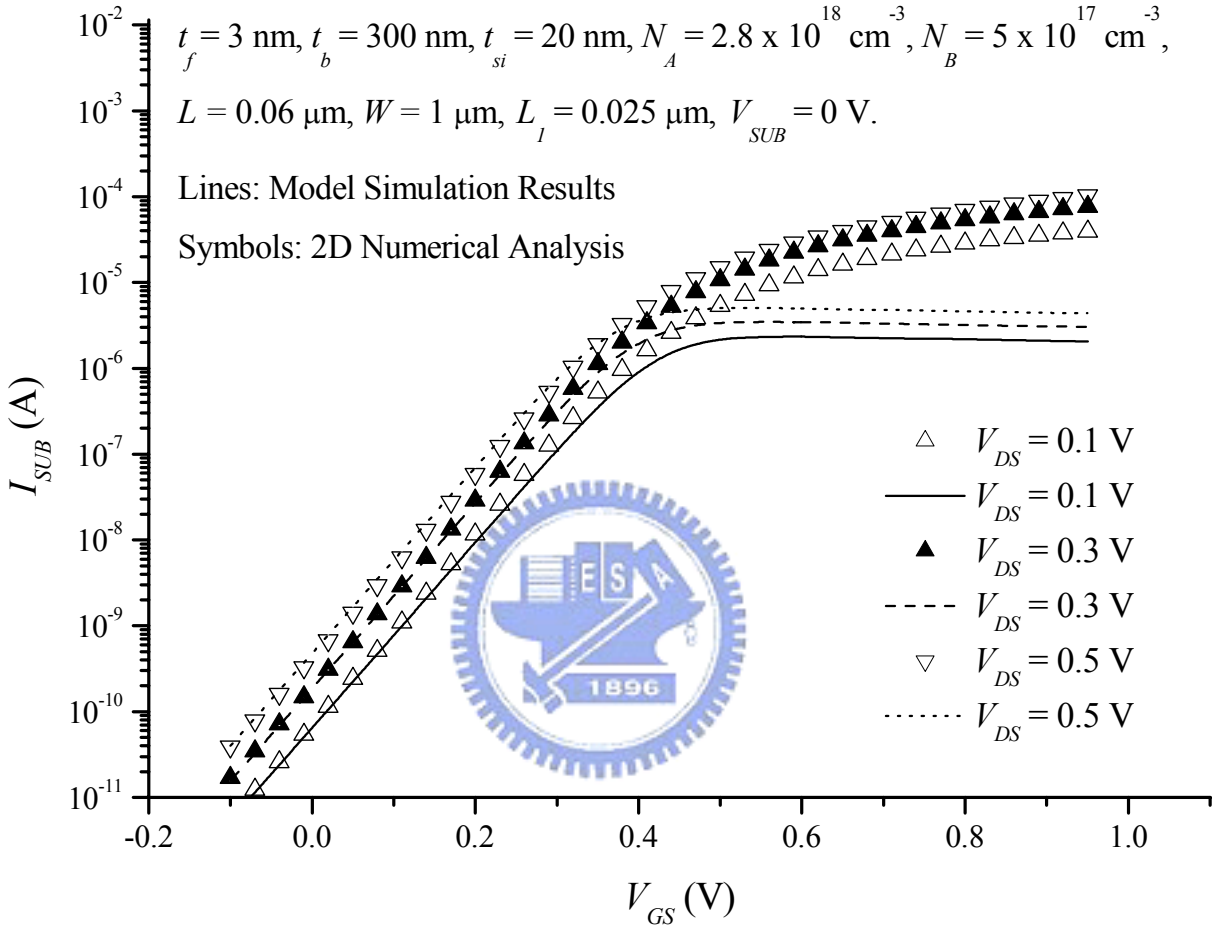

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x 10^{18} cm^{-3}, N_B = 5 x 10^{17} cm^{-3},
L = 0.06 μm, W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
V_{DS} = 0.1 V
V_{DS} = 0.1 V
V_{DS} = 0.3 V
V_{DS} = 0.3 V
V_{DS} = 0.5 V
V_{DS} = 0.5 V
I_{SUB} (A)
V_{GS} (V)
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
-0.2
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–14

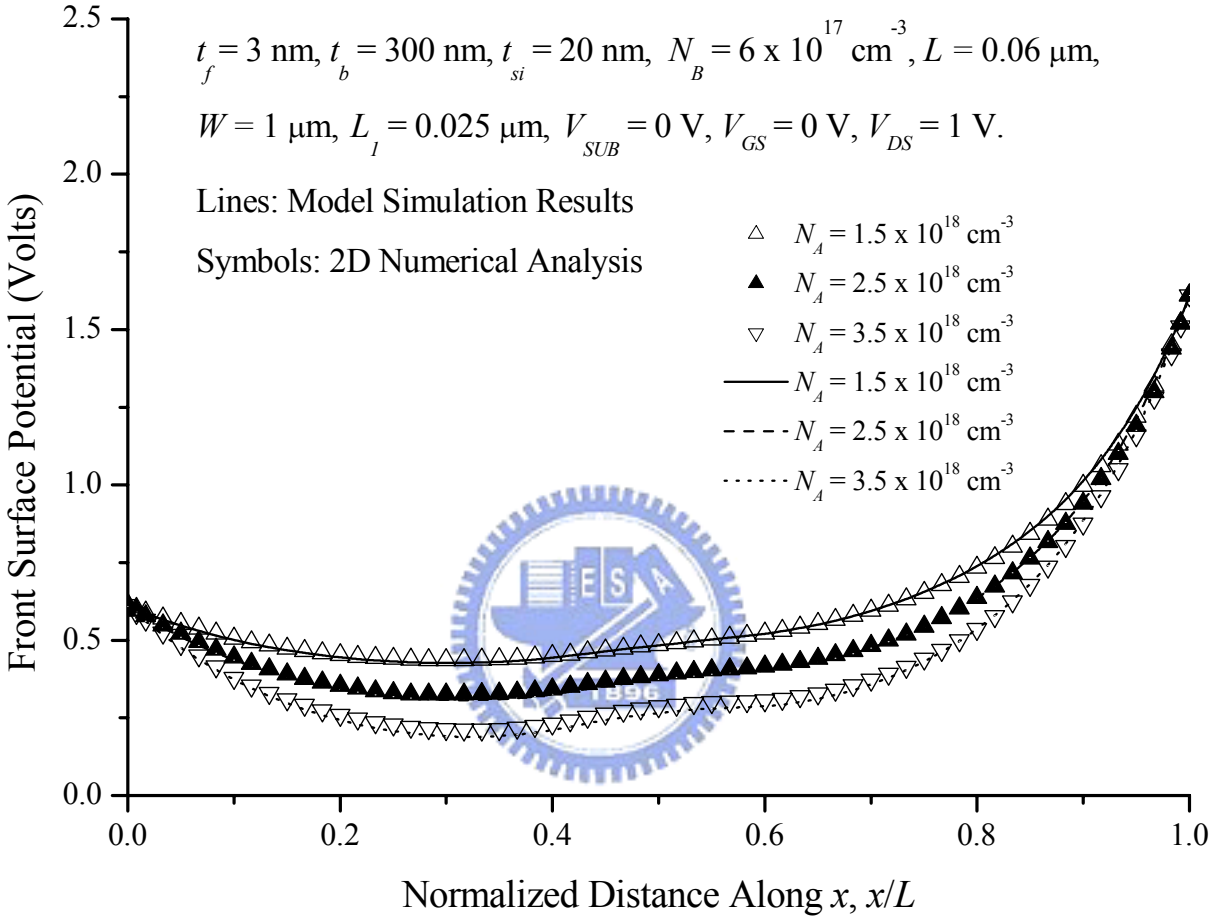

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 6 x 10^{17} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{GS} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 1.5 x 10^{18} cm^{-3}
N_A = 2.5 x 10^{18} cm^{-3}
N_A = 3.5 x 10^{18} cm^{-3}
N_A = 1.5 x 10^{18} cm^{-3}
N_A = 2.5 x 10^{18} cm^{-3}
N_A = 3.5 x 10^{18} cm^{-3}
Front Surface Potential (Volts)
Normalized Distance Along x, x/L
0.0
0.5
1.0
1.5
2.0
2.5
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–15

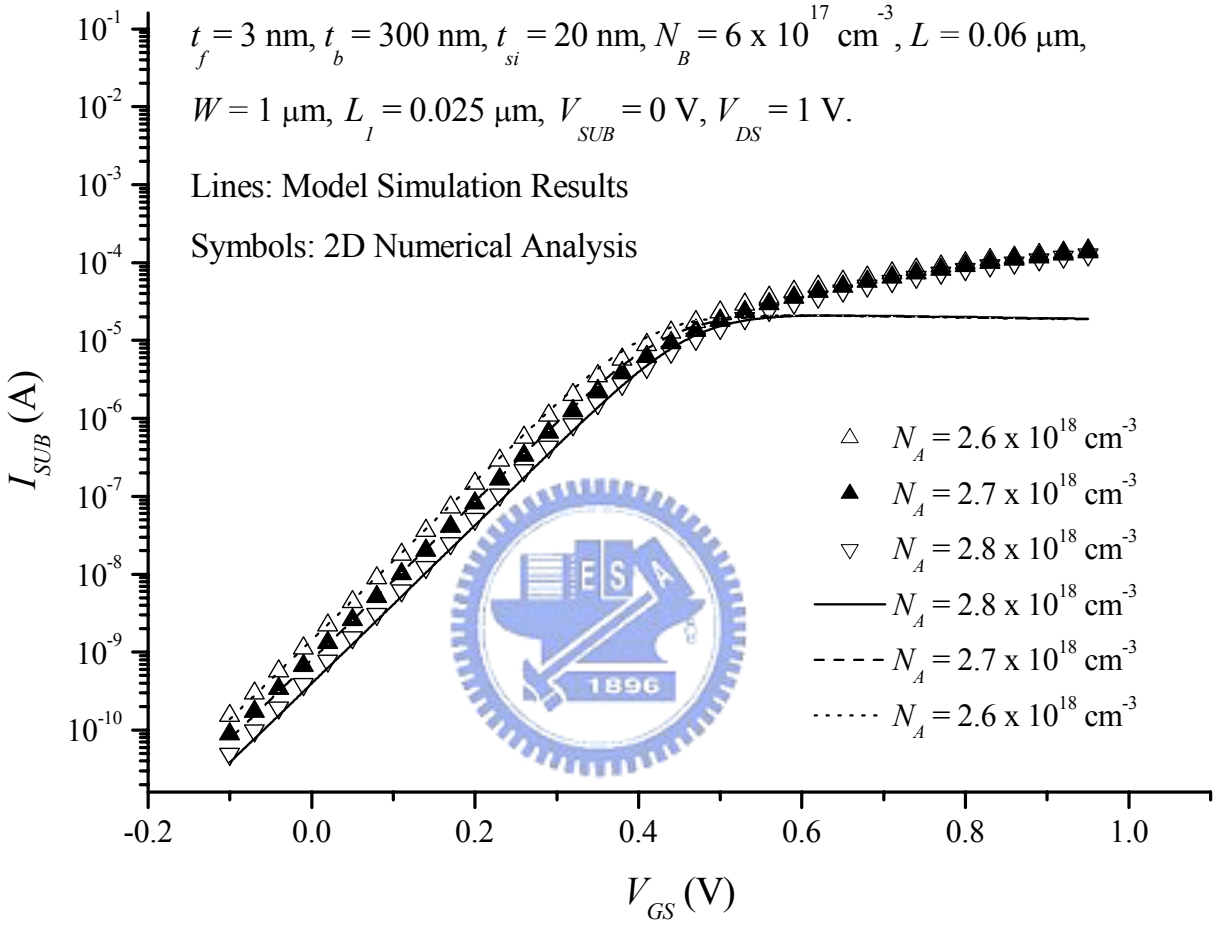

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 6 x 10^{17} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 2.6 x 10^{18} cm^{-3}
N_A = 2.7 x 10^{18} cm^{-3}
N_A = 2.8 x 10^{18} cm^{-3}
N_A = 2.8 x 10^{18} cm^{-3}
N_A = 2.7 x 10^{18} cm^{-3}
N_A = 2.6 x 10^{18} cm^{-3}
I_{SUB} (A)
V_{GS} (V)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
-0.2
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–16

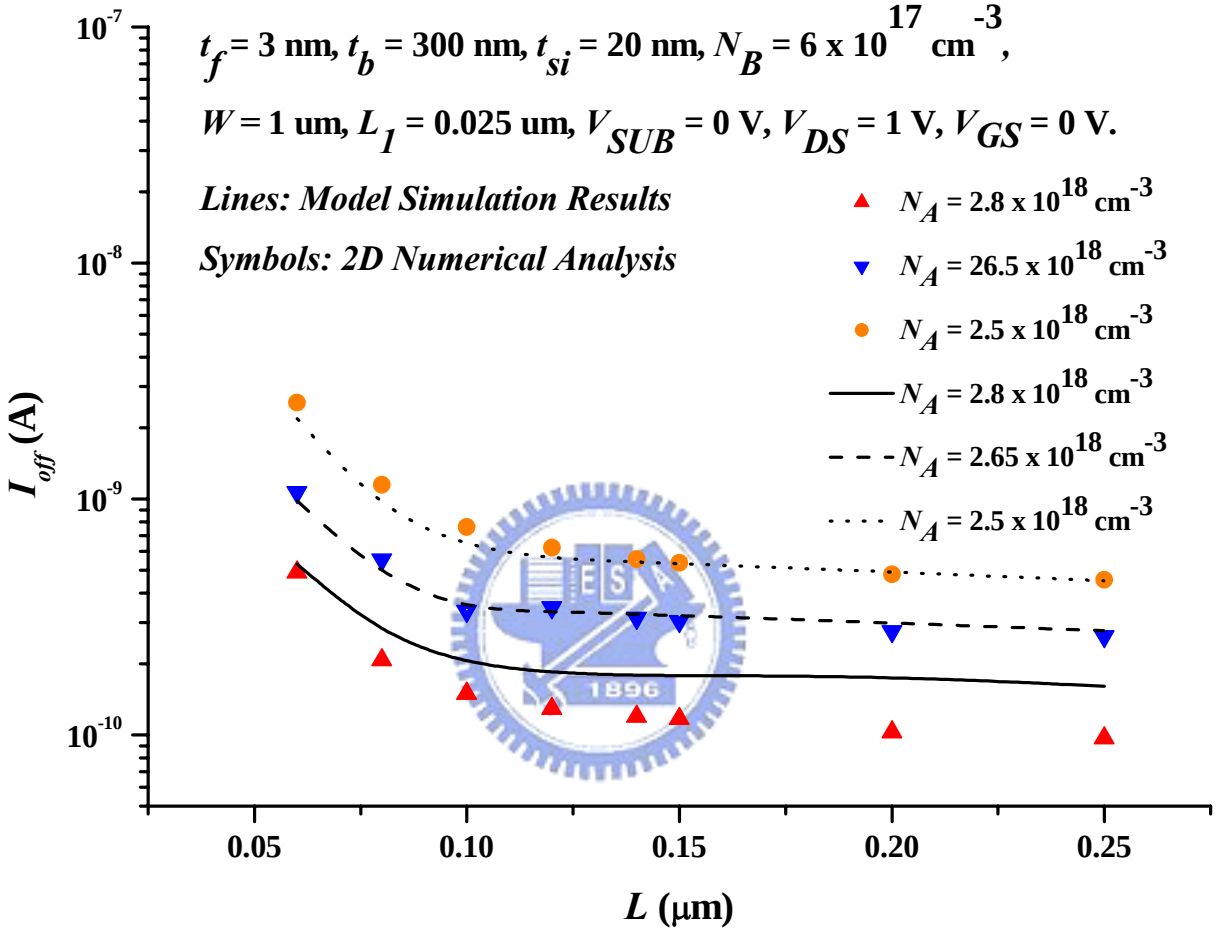

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_B = 6 x 10^17 cm^-3,
W = 1 um, L_1 = 0.025 um, V_{SUB} = 0 V, V_{DS} = 1 V, V_{GS} = 0 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_A = 2.8 x 10^18 cm^-3
N_A = 26.5 x 10^18 cm^-3
N_A = 2.5 x 10^18 cm^-3
N_A = 2.8 x 10^18 cm^-3
N_A = 2.65 x 10^18 cm^-3
N_A = 2.5 x 10^18 cm^-3
I_{off} (A)
10^-7
10^-8
10^-9
10^-10
0.05
0.10
0.15
0.20
0.25
L (μm)

Fig. 4–17

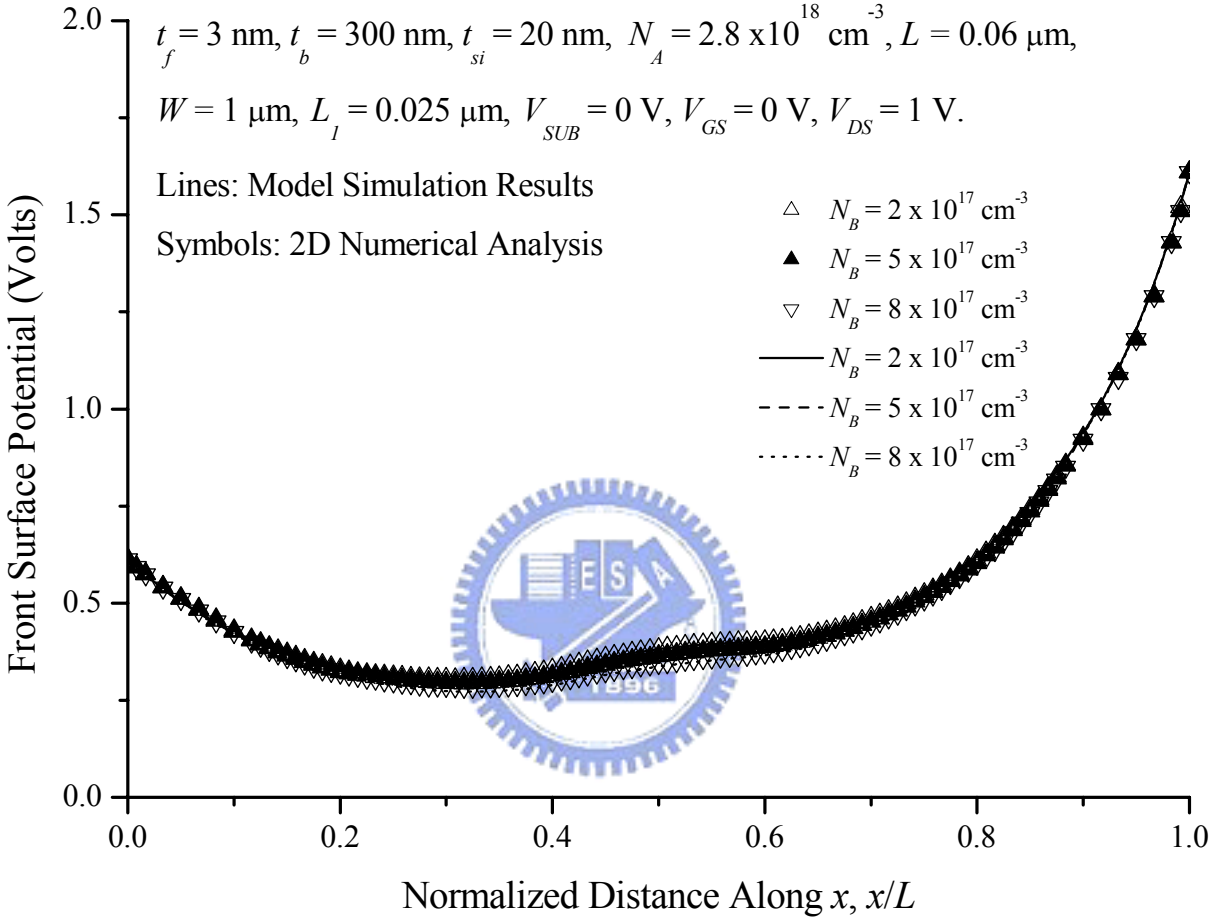

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x10^{18} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{GS} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 2 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 8 x 10^{17} cm^{-3}
N_B = 2 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 8 x 10^{17} cm^{-3}
Front Surface Potential (Volts)
Normalized Distance Along x, x/L
0.0
0.5
1.0
1.5
2.0
0.0
0.2
0.4
0.6
0.8
1.0

Fig. 4–18(a)

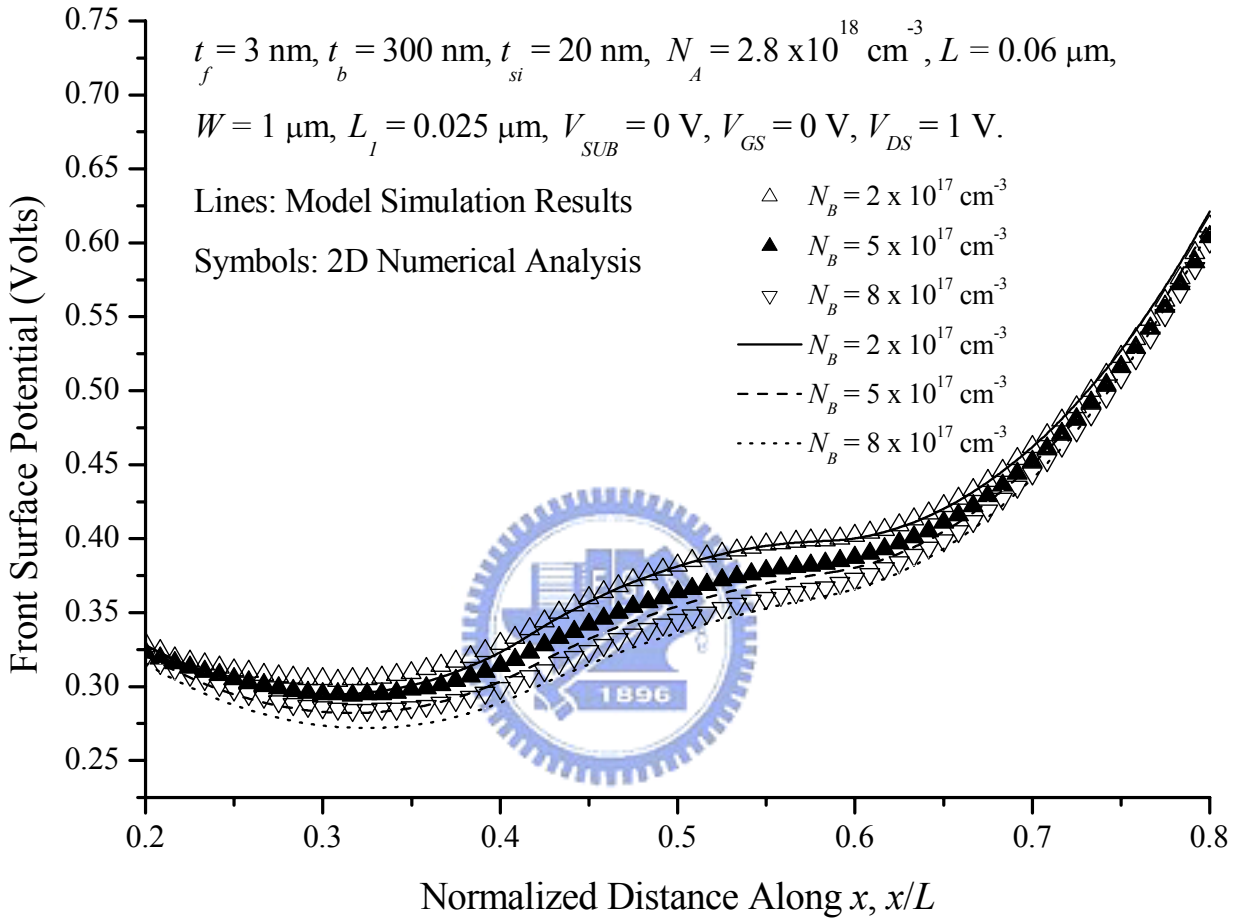

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x10^{18} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_I = 0.025 μm, V_{SUB} = 0 V, V_{GS} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 2 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 8 x 10^{17} cm^{-3}
N_B = 2 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 8 x 10^{17} cm^{-3}
Front Surface Potential (Volts)
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Normalized Distance Along x, x/L

Fig. 4–18(b)

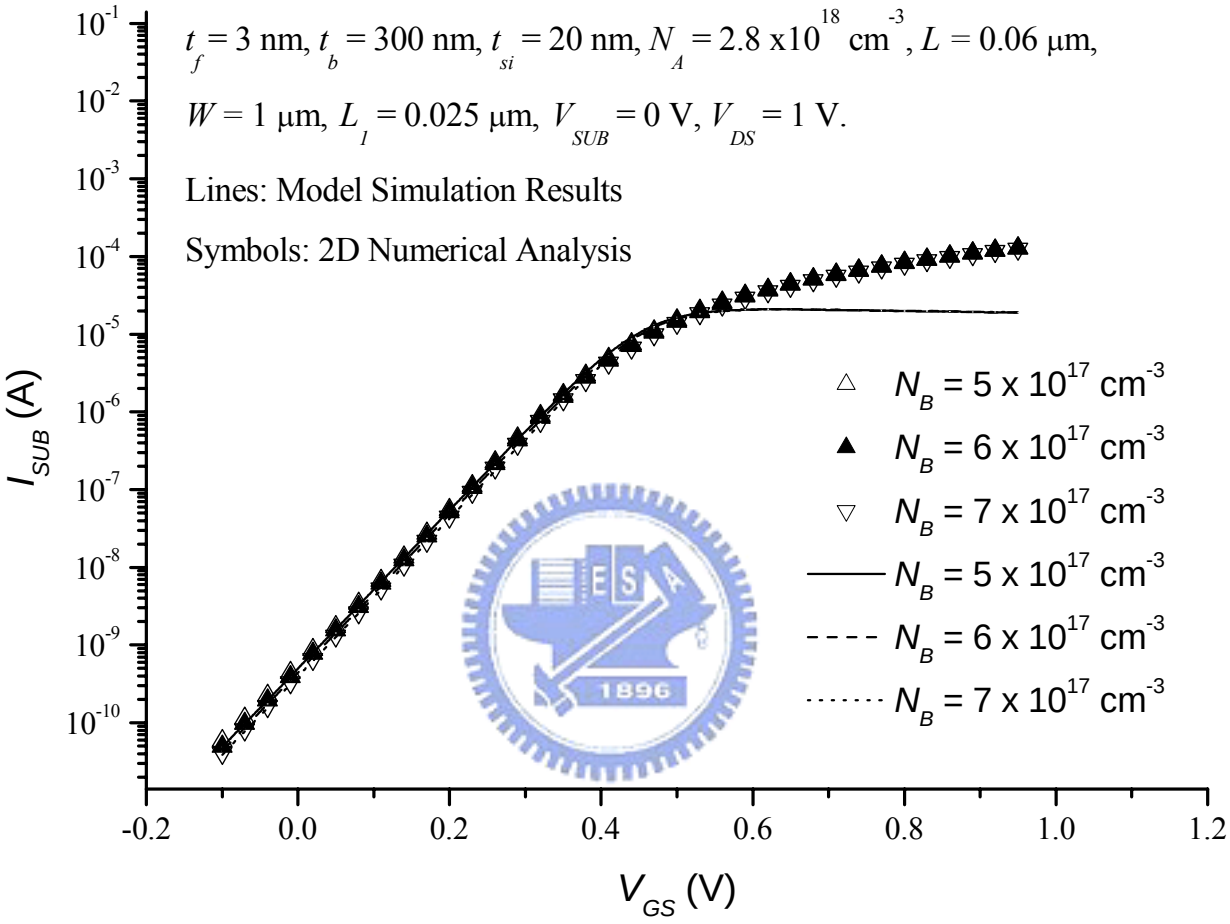

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x10^{18} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 5 x 10^{17} cm^{-3}
N_B = 6 x 10^{17} cm^{-3}
N_B = 7 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 6 x 10^{17} cm^{-3}
N_B = 7 x 10^{17} cm^{-3}
I_{SUB} (A)
V_{GS} (V)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
1.2

Fig. 4–19(a)

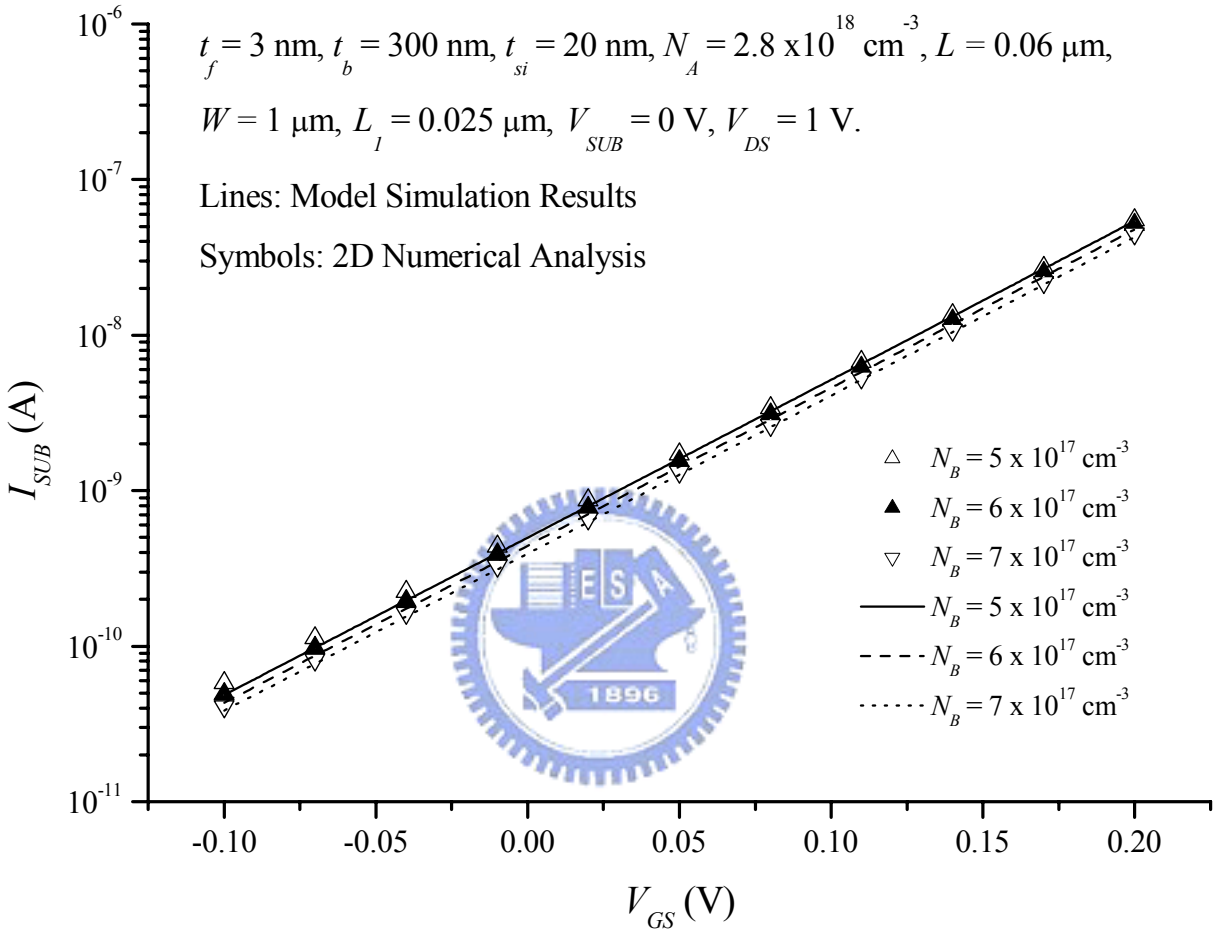

t_f = 3 nm, t_b = 300 nm, t_{si} = 20 nm, N_A = 2.8 x10^{18} cm^{-3}, L = 0.06 μm,
W = 1 μm, L_1 = 0.025 μm, V_{SUB} = 0 V, V_{DS} = 1 V.
Lines: Model Simulation Results
Symbols: 2D Numerical Analysis
N_B = 5 x 10^{17} cm^{-3}
N_B = 6 x 10^{17} cm^{-3}
N_B = 7 x 10^{17} cm^{-3}
N_B = 5 x 10^{17} cm^{-3}
N_B = 6 x 10^{17} cm^{-3}
N_B = 7 x 10^{17} cm^{-3}
I_{SUB} (A)
V_{GS} (V)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
-0.10
-0.05
0.00
0.05
0.10
0.15
0.20

Fig. 4–19(b)

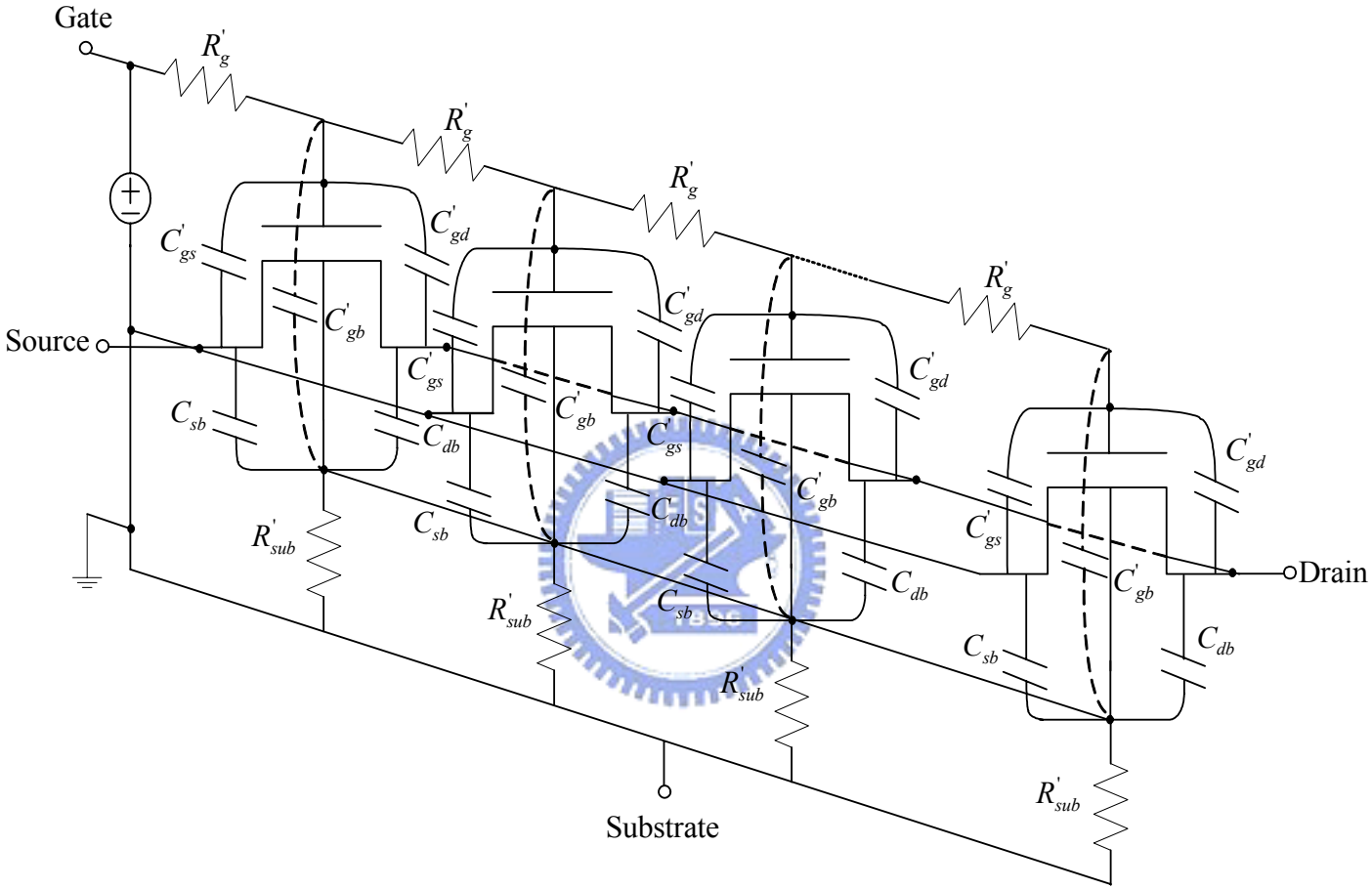


Fig. 5–1

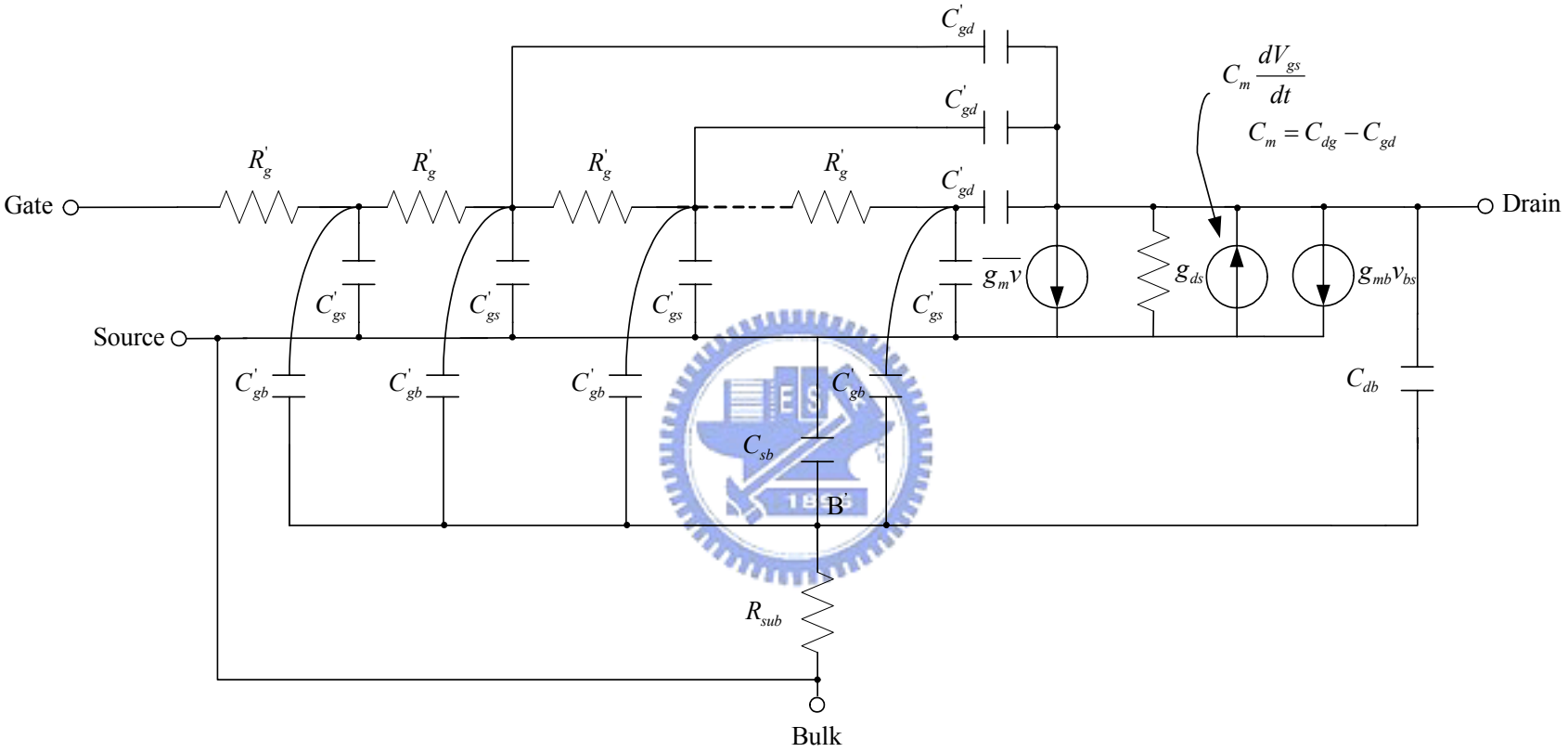
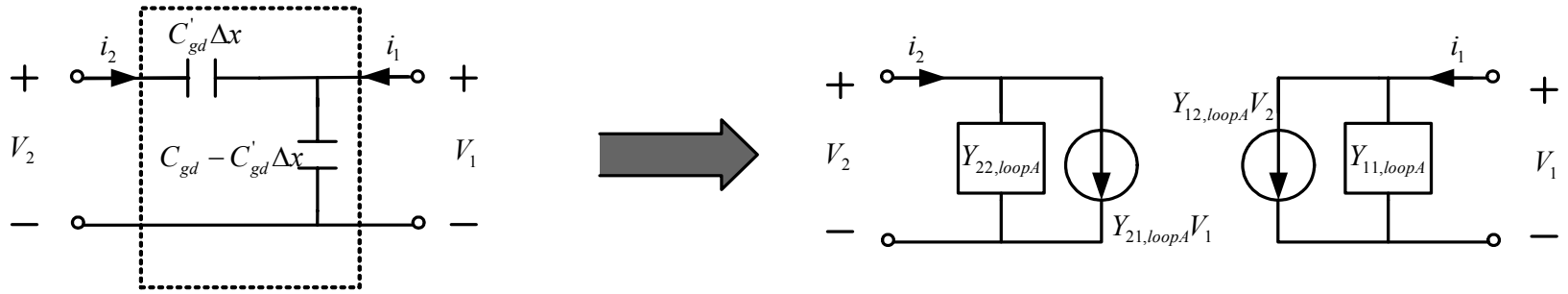

Gate
Source
Drain
Bulk
R_g'
C_{gd}'
$C_m \frac{dV_{gs}}{dt}$
$C_m = C_{dg} - C_{gd}$
C_{gs}'
C_{gb}'
$g_m v$
g_{ds}
$g_{mb} v_{bs}$
C_{db}
C_{sb}
B'
R_{sub}

Fig. 5–2

Feedback Loop A



Feedback Loop B

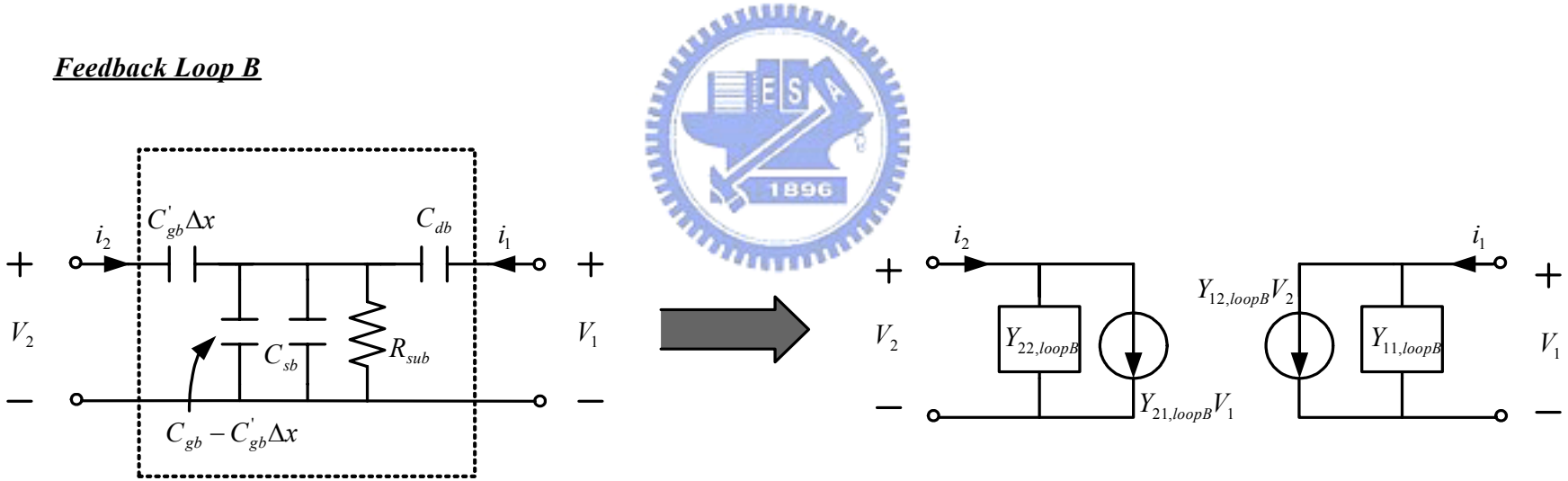


Fig. 5–3

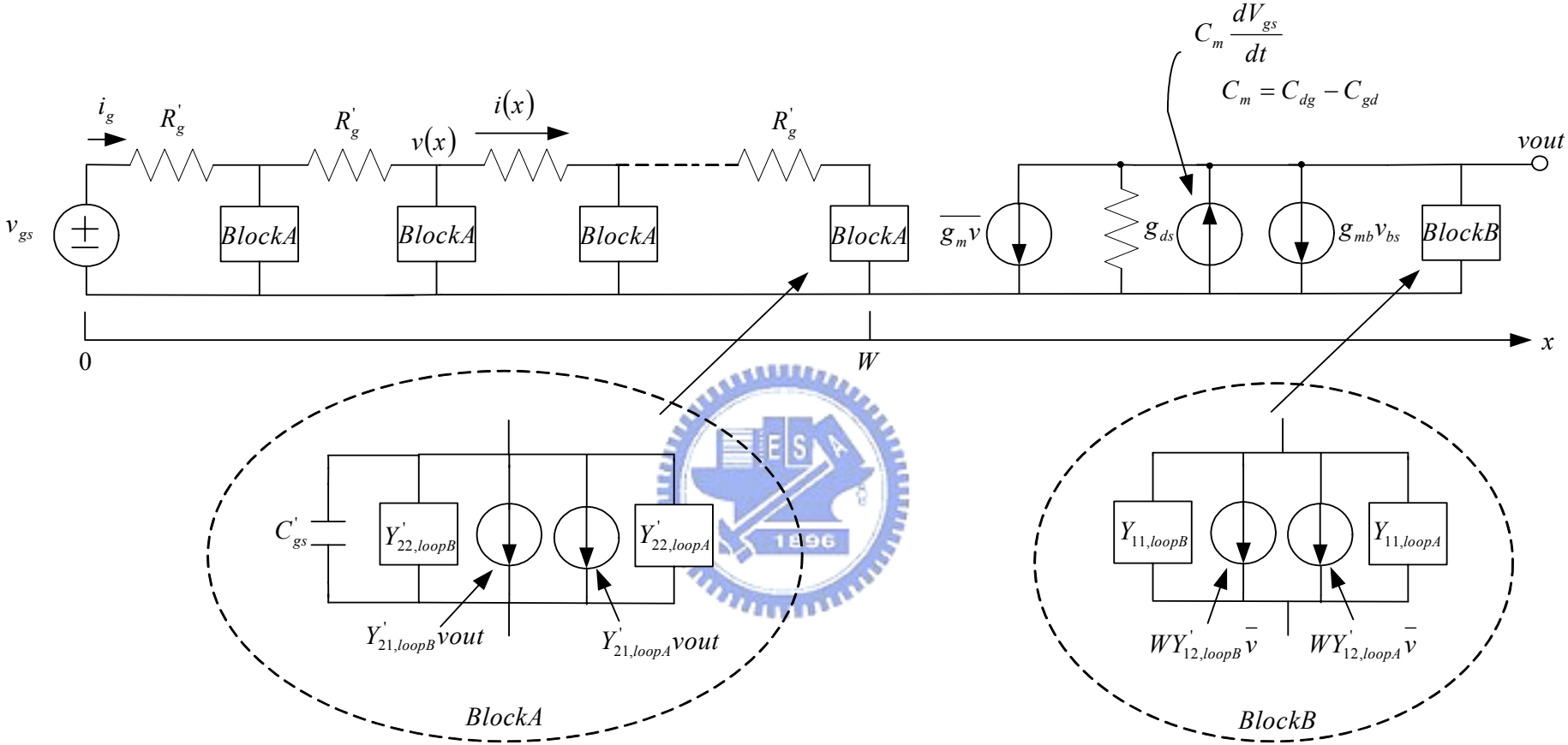

$C_m \frac{dV_{gs}}{dt}$
$C_m = C_{dg} - C_{gd}$
i_g
$R_g^{'}$
$R_g^{'}$
$v(x)$
$i(x)$
$R_g^{'}$
vout
v_{gs}
BlockA
BlockA
BlockA
BlockA
$\overline{g_m v}$
g_{ds}
$g_{mb} v_{bs}$
BlockB
0
W
x
$C_{gs}^{'}$
$Y_{22,loopB}^{'}$
$Y_{22,loopA}^{'}$
$Y_{21,loopB}^{'} vout$
$Y_{21,loopA}^{'} vout$
BlockA
$Y_{11,loopB}$
$Y_{11,loopA}$
$WY_{12,loopB}^{'} \bar{v}$
$WY_{12,loopA}^{'} \bar{v}$
BlockB

Fig. 5–4

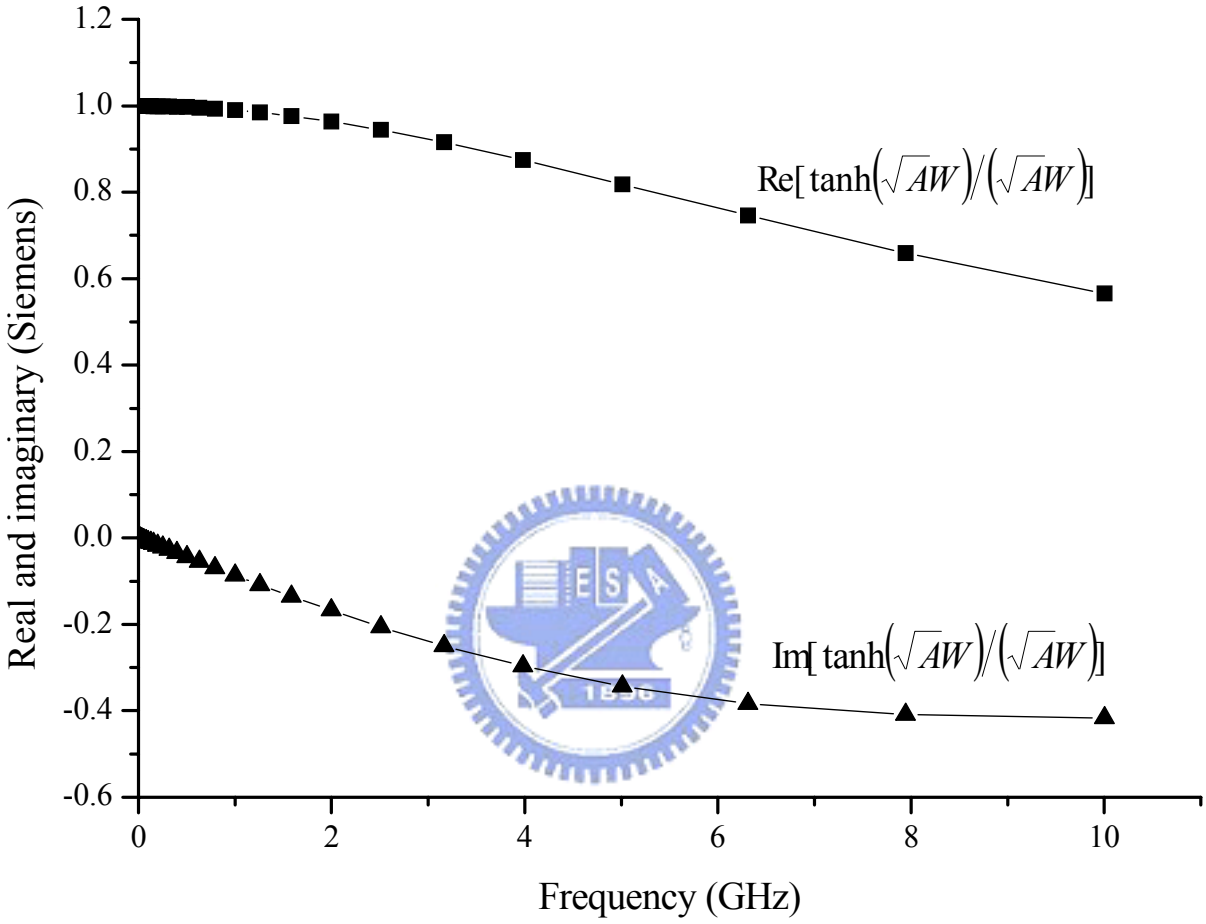

1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
0
2
4
6
8
10
Real and imaginary (Siemens)
Frequency (GHz)
Re[tanh(√AW)/(√AW)]
Im[tanh(√AW)/(√AW)]

Fig. 5–5

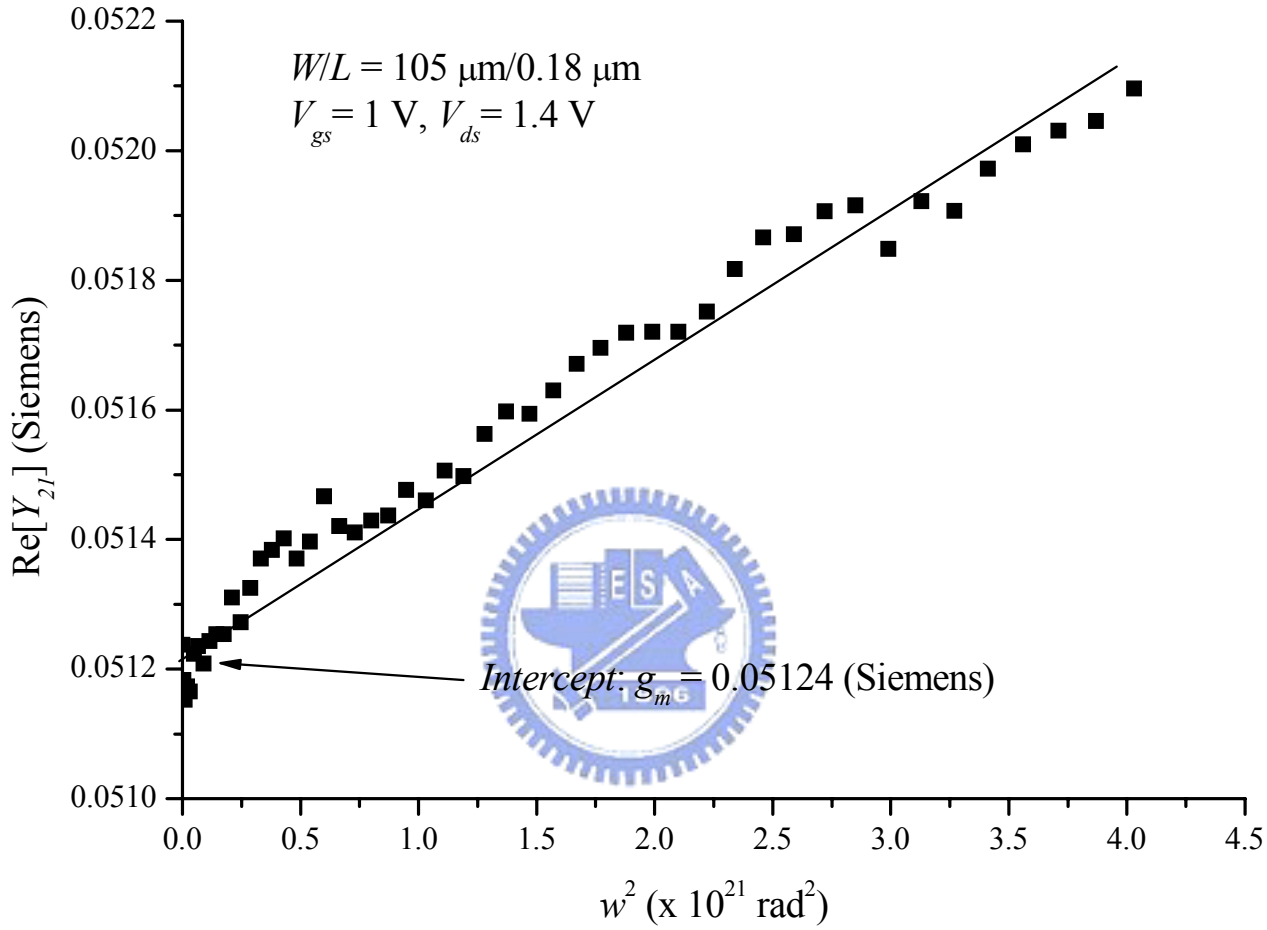

W/L = 105 μm/0.18 μm
V_gs = 1 V, V_ds = 1.4 V
Intercept: g_m = 0.05124 (Siemens)
Re[Y_21] (Siemens)
w^2 (x 10^21 rad^2)
0.0522
0.0520
0.0518
0.0516
0.0514
0.0512
0.0510
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

Fig. 5–6(a)

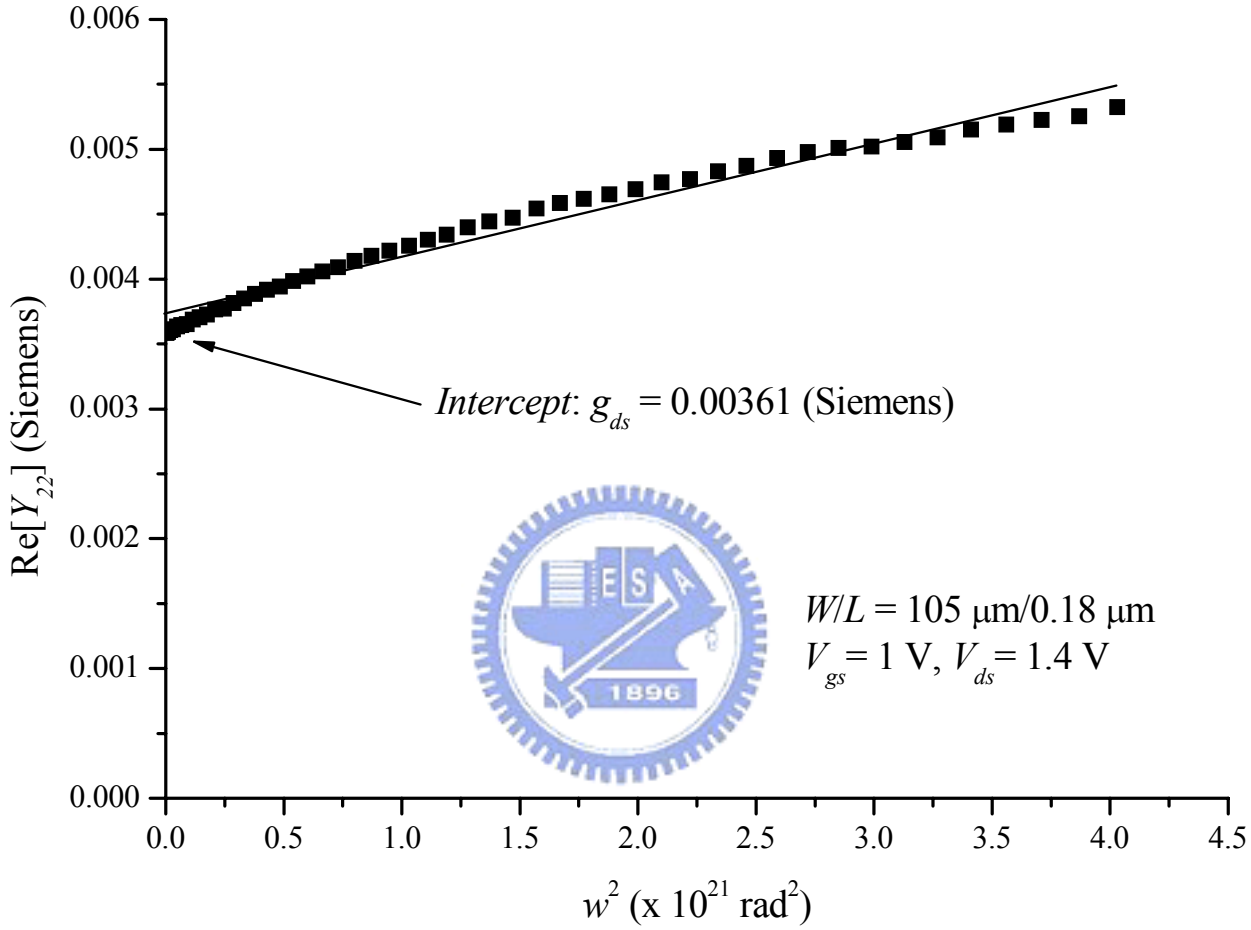

0.006
0.005
0.004
0.003
0.002
0.001
0.000
Re[Y_{22}] (Siemens)
Intercept: g_{ds} = 0.00361 (Siemens)
W/*L* = 105 μm/0.18 μm
V_{gs} = 1 V, V_{ds} = 1.4 V
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
w^2 (x 10^{21} rad^2)

Fig. 5–6(b)

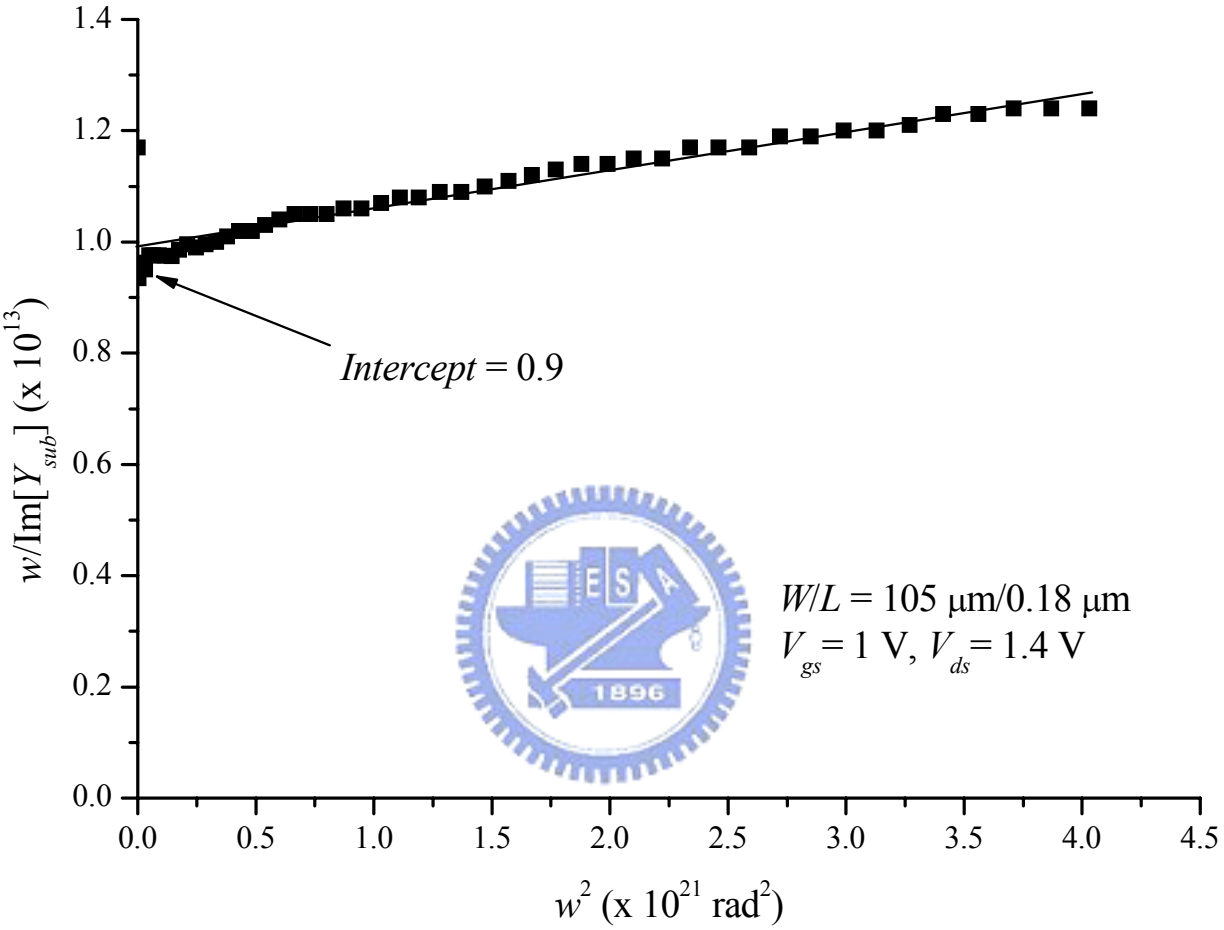

1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
w/Im[Y_sub] (x 10^13)
w^2 (x 10^21 rad^2)
Intercept = 0.9
W/L = 105 μm/0.18 μm
V_gs = 1 V, V_ds = 1.4 V

Fig. 5–7(a)

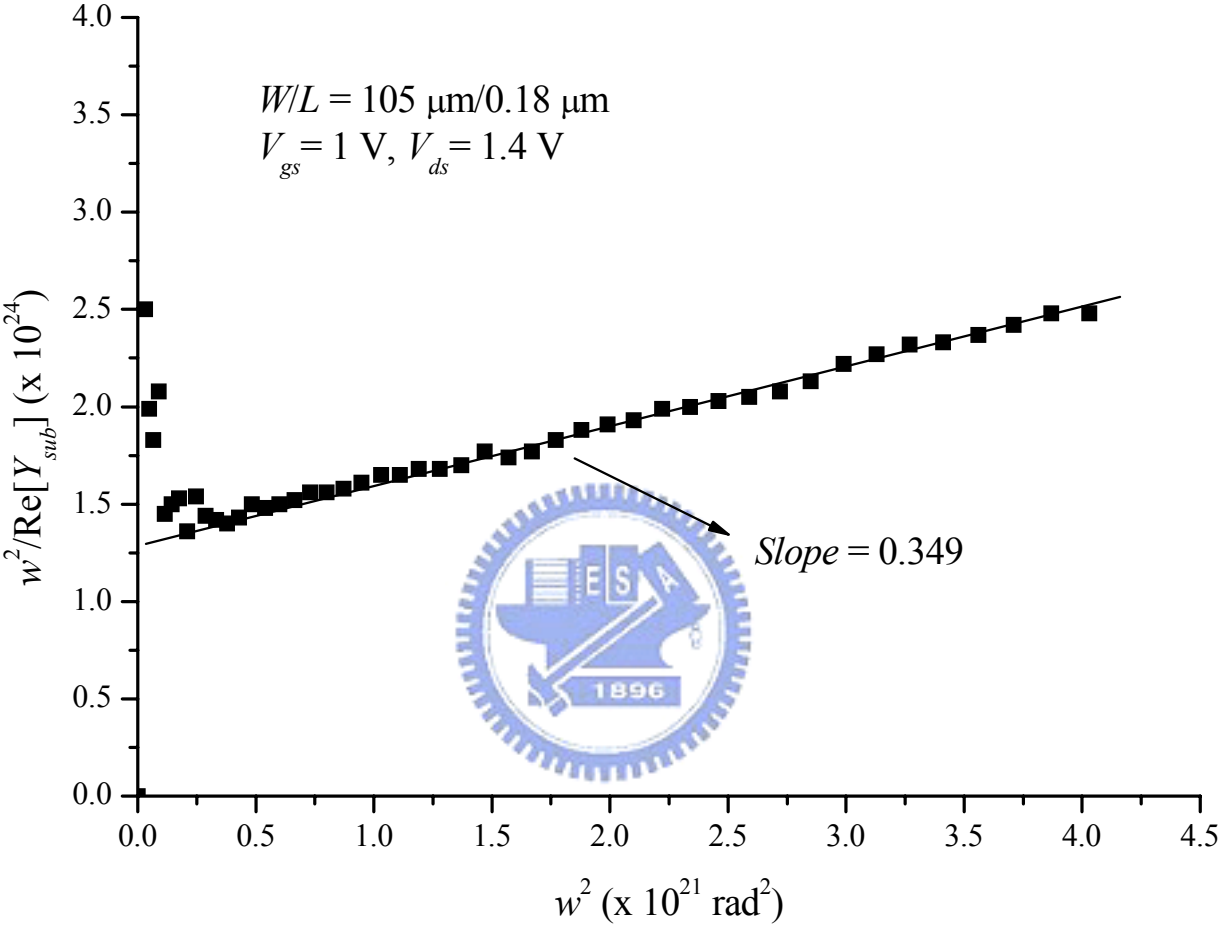

W/L = 105 μm/0.18 μm
V_gs = 1 V, V_ds = 1.4 V
Slope = 0.349
w²/Re[Y_sub] (x 10²⁴)
w² (x 10²¹ rad²)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5

Fig. 5–7(b)

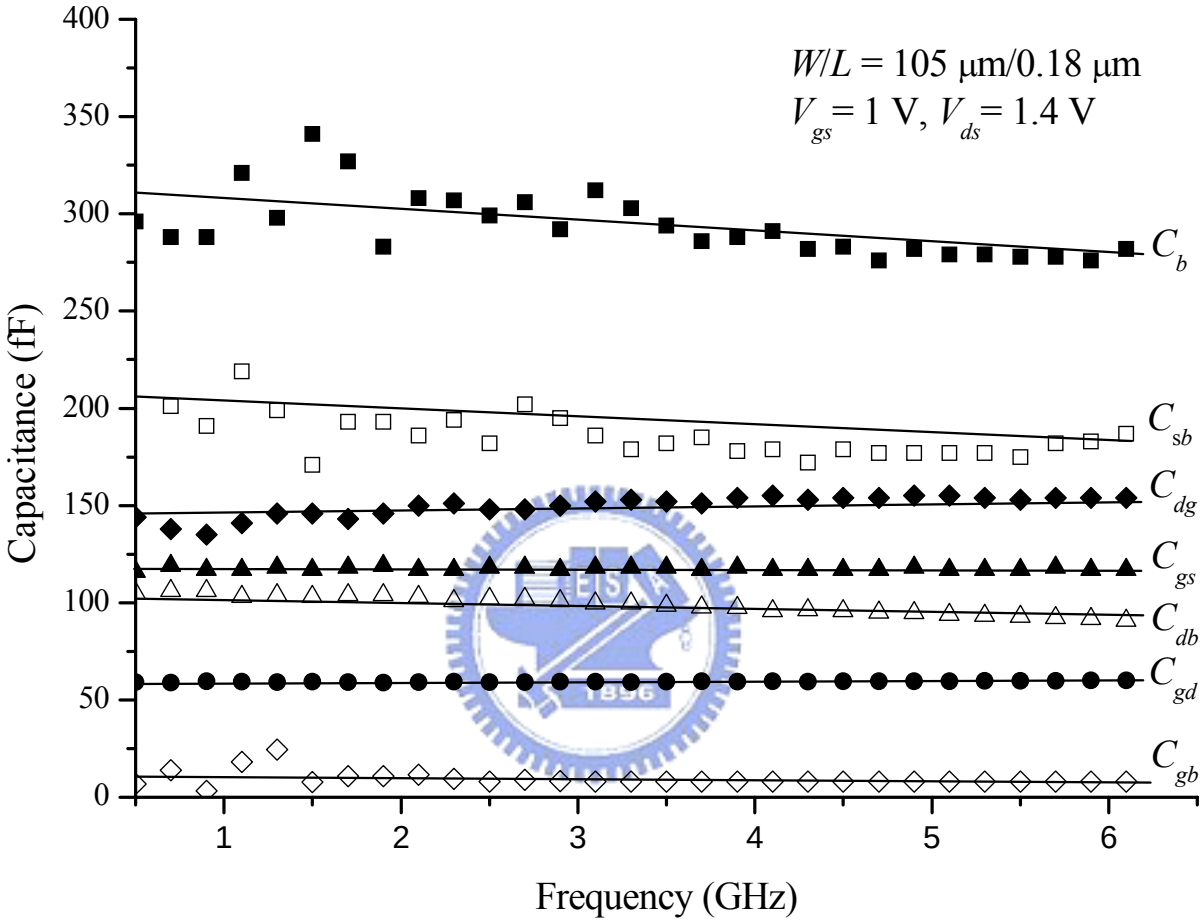

W/L = 105 μm/0.18 μm
V_gs = 1 V, V_ds = 1.4 V
C_b
C_sb
C_dg
C_gs
C_db
C_gd
C_gb
Capacitance (fF)
Frequency (GHz)
400
350
300
250
200
150
100
50
0
1
2
3
4
5
6

Fig. 5–8

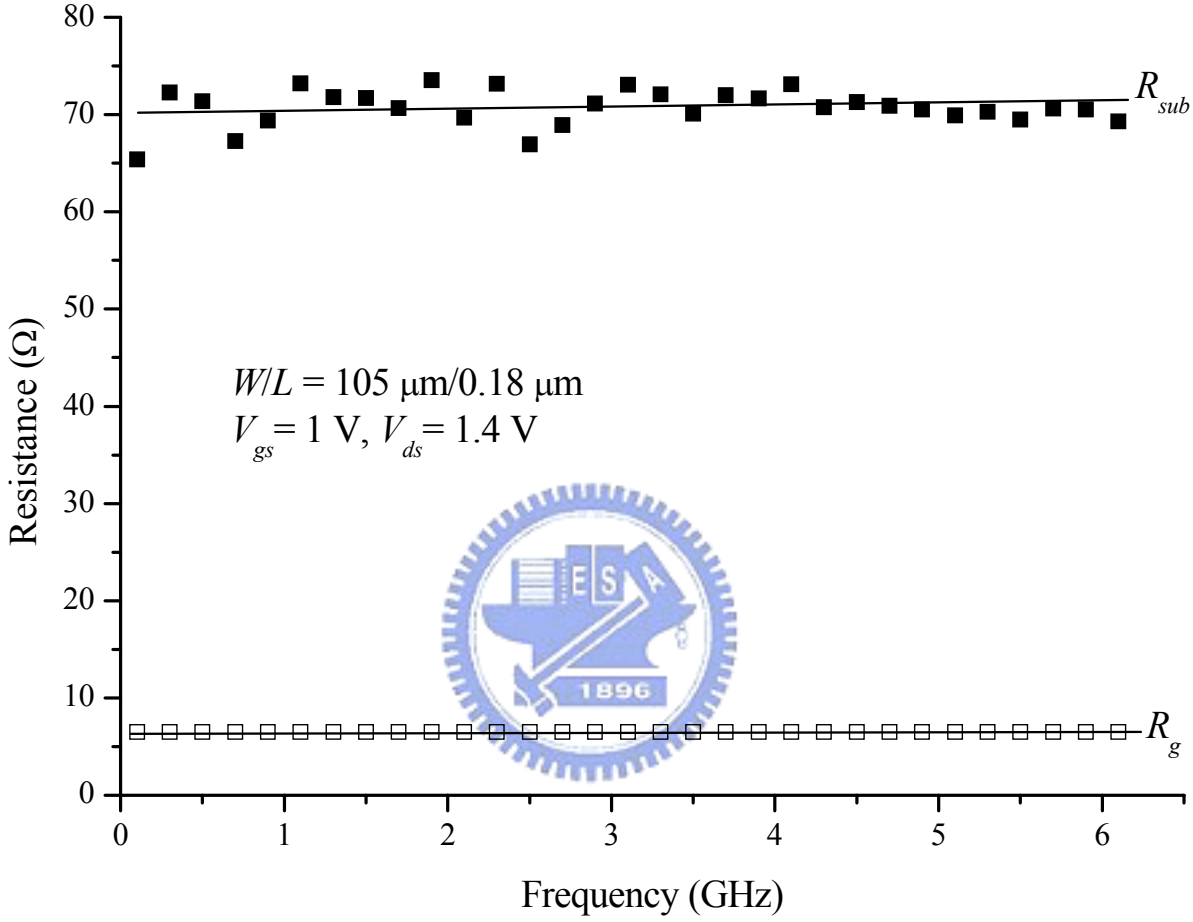

80
70
60
50
40
30
20
10
0
Resistance (Ω)
0
1
2
3
4
5
6
Frequency (GHz)
R_{sub}
R_g
W/L = 105 μm/0.18 μm
V_{gs} = 1 V, V_{ds} = 1.4 V

Fig. 5–9

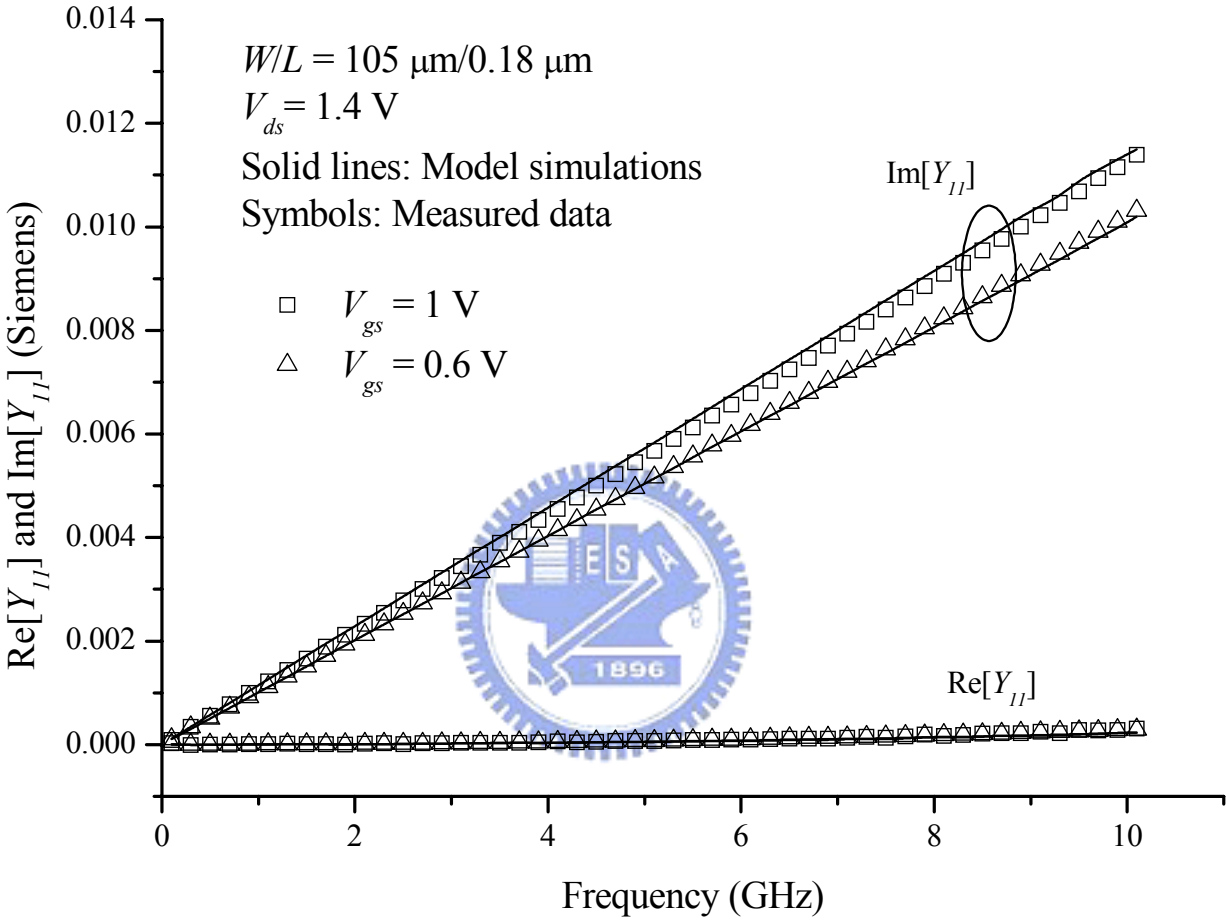

W/L = 105 μm/0.18 μm
V_ds = 1.4 V
Solid lines: Model simulations
Symbols: Measured data
V_gs = 1 V
V_gs = 0.6 V
Im[Y_11]
Re[Y_11]
Re[Y_11] and Im[Y_11] (Siemens)
Frequency (GHz)
0.014
0.012
0.010
0.008
0.006
0.004
0.002
0.000
0
2
4
6
8
10

Fig. 5–10(a)

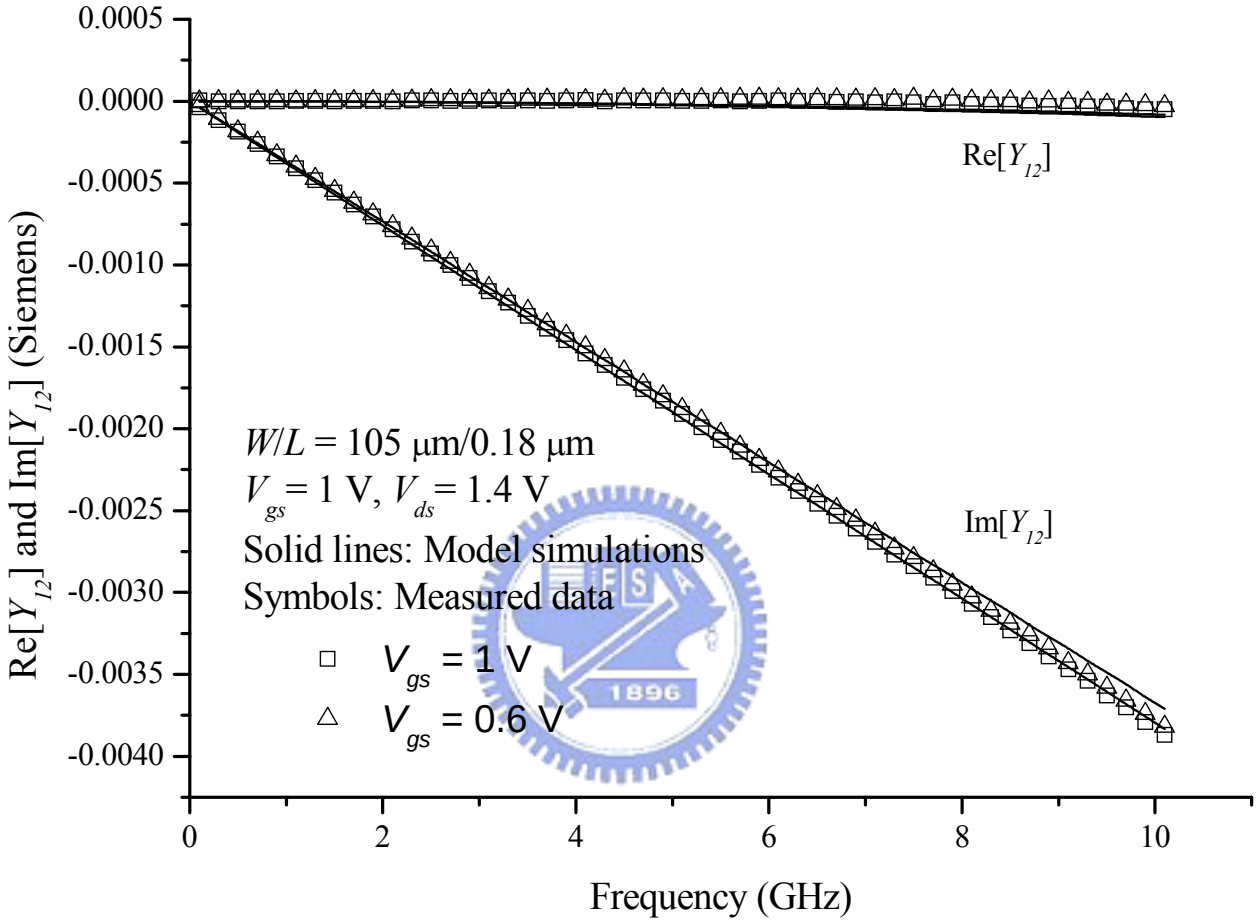

0.0005
0.0000
-0.0005
-0.0010
-0.0015
-0.0020
-0.0025
-0.0030
-0.0035
-0.0040
Re[Y_{12}] and Im[Y_{12}] (Siemens)
0
2
4
6
8
10
Frequency (GHz)
Re[Y_{12}]
Im[Y_{12}]
W/L = 105 μm/0.18 μm
V_{gs} = 1 V, V_{ds} = 1.4 V
Solid lines: Model simulations
Symbols: Measured data
□ V_{gs} = 1 V
△ V_{gs} = 0.6 V

Fig. 5–10(b)

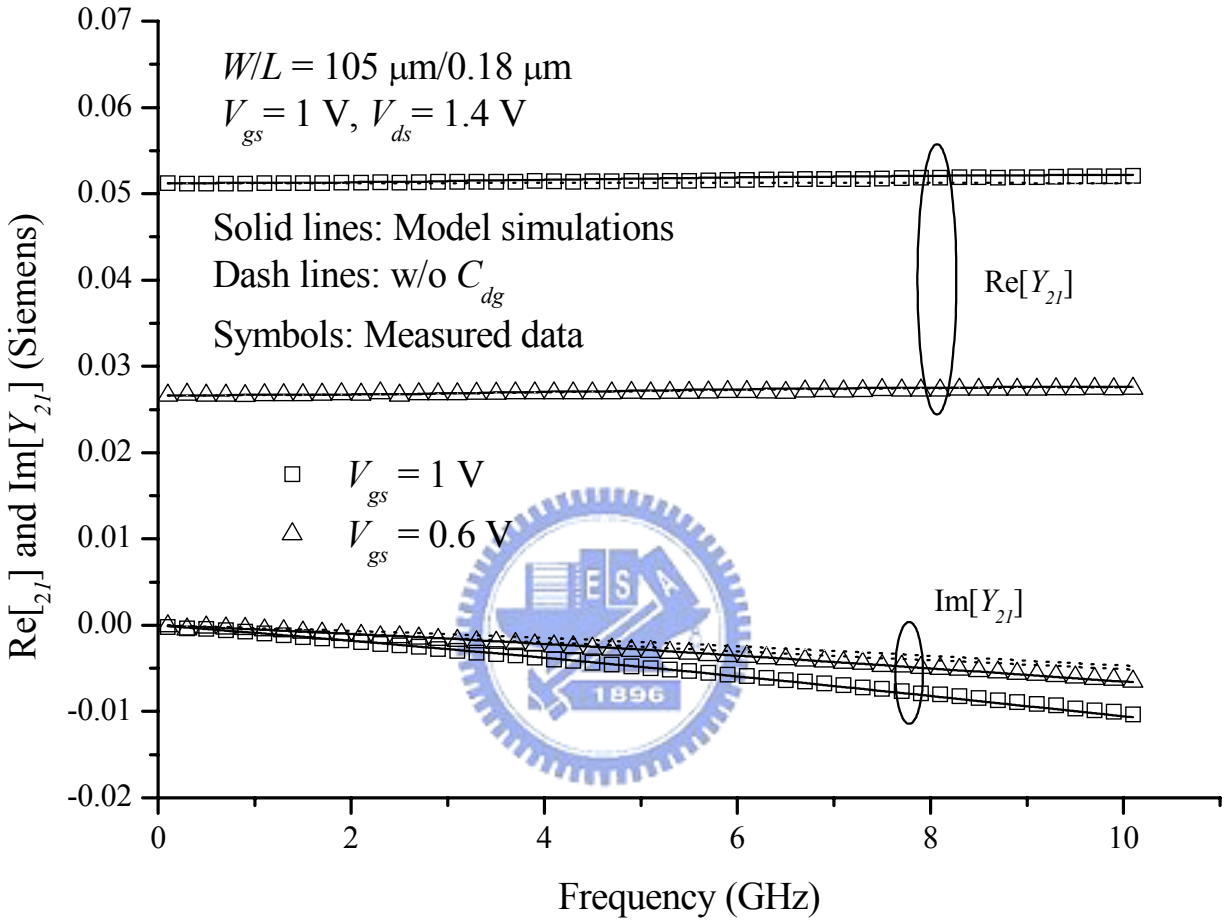

0.07
0.06
0.05
0.04
0.03
0.02
0.01
0.00
-0.01
-0.02
0
2
4
6
8
10
Re[Y_{21}] and Im[Y_{21}] (Siemens)
Frequency (GHz)
W/L = 105 μm/0.18 μm
V_{gs} = 1 V, V_{ds} = 1.4 V
Solid lines: Model simulations
Dash lines: w/o C_{dg}
Symbols: Measured data
Re[Y_{21}]
Im[Y_{21}]
V_{gs} = 1 V
V_{gs} = 0.6 V

Fig. 5–10(c)

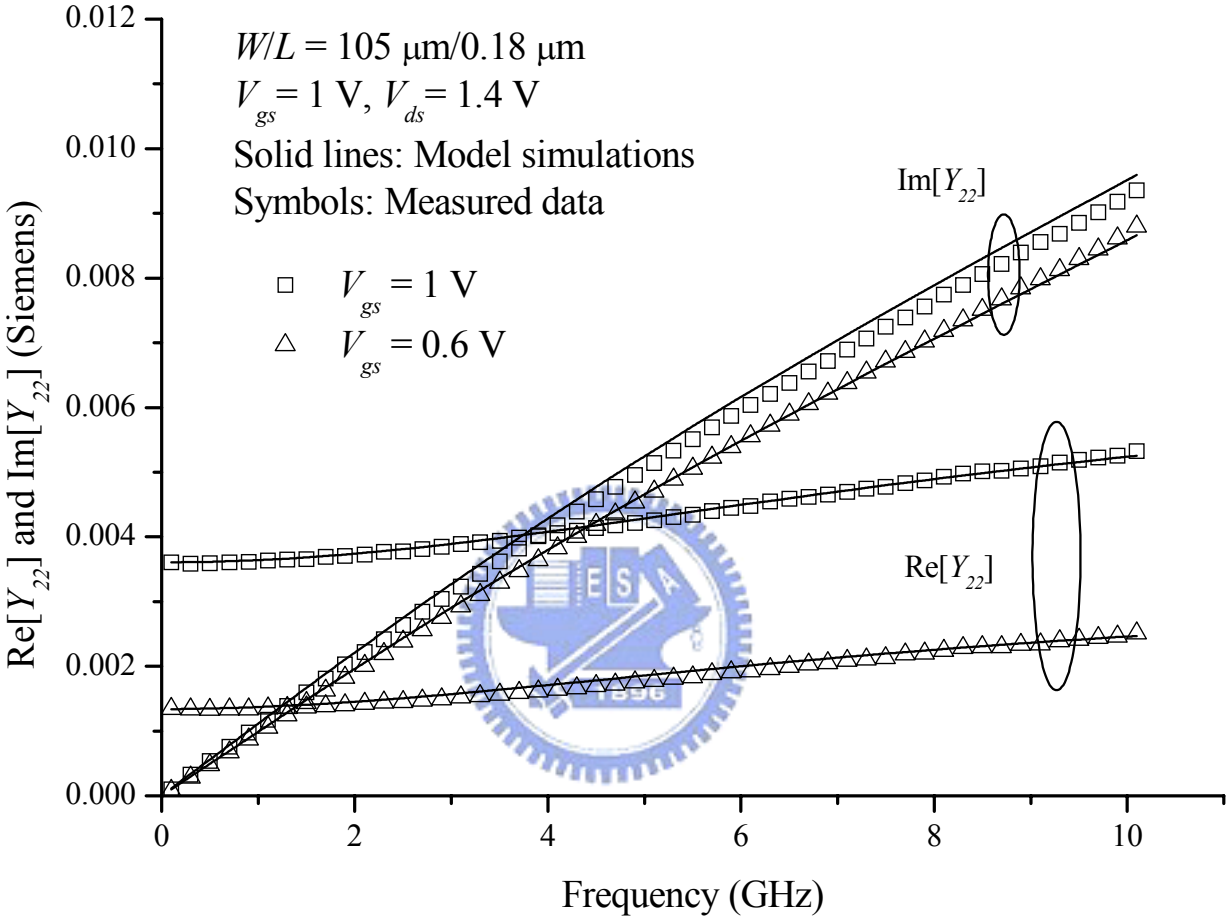

W/L = 105 μm/0.18 μm
V_gs = 1 V, V_ds = 1.4 V
Solid lines: Model simulations
Symbols: Measured data
V_gs = 1 V
V_gs = 0.6 V
Im[Y_22]
Re[Y_22]
Re[Y_22] and Im[Y_22] (Siemens)
Frequency (GHz)
0.000
0.002
0.004
0.006
0.008
0.010
0.012
0
2
4
6
8
10

Fig. 5–10(d)

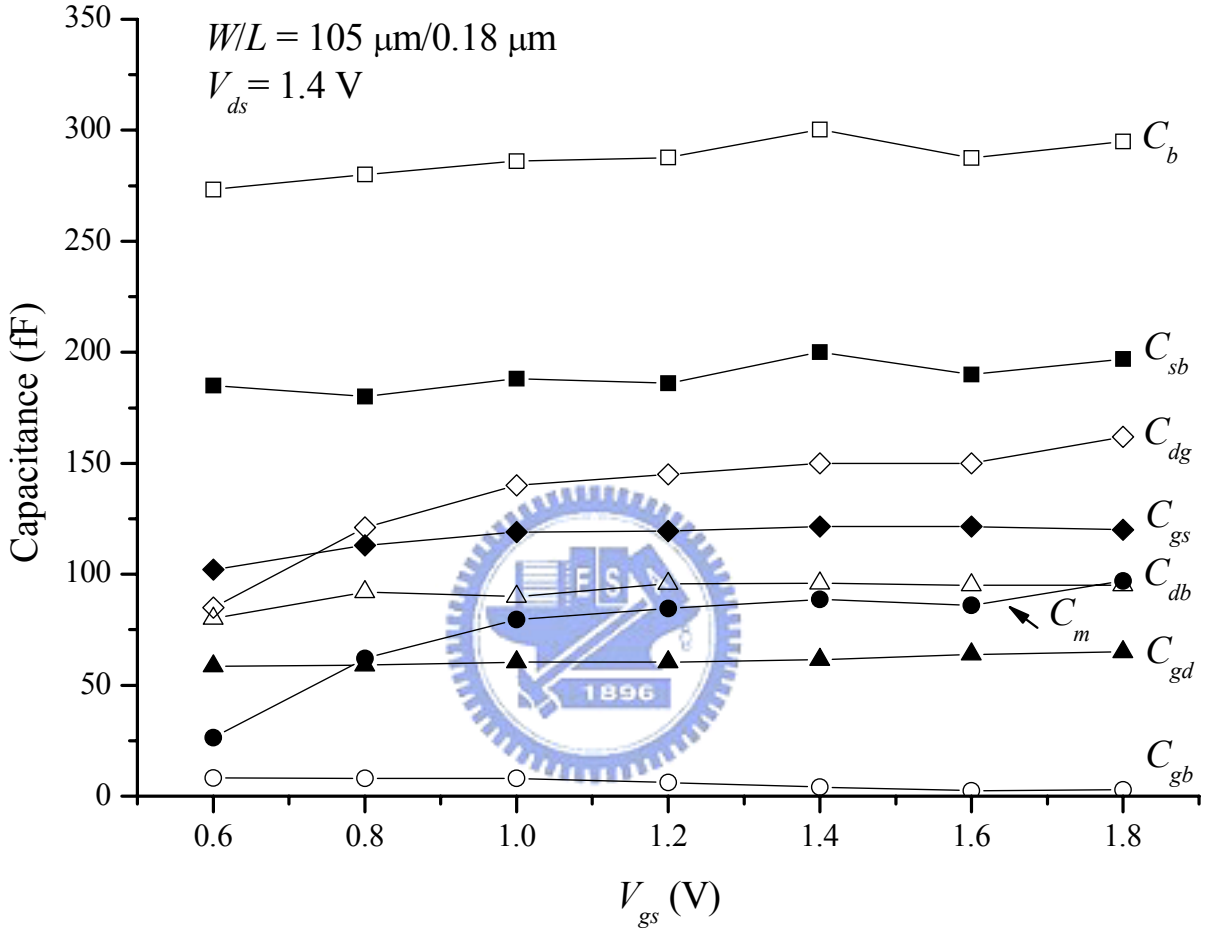

W/L = 105 μm/0.18 μm
V_ds = 1.4 V
C_b
C_sb
C_dg
C_gs
C_db
C_m
C_gd
C_gb
Capacitance (fF)
V_gs (V)
350
300
250
200
150
100
50
0
0.6
0.8
1.0
1.2
1.4
1.6
1.8

Fig. 5–11(a)

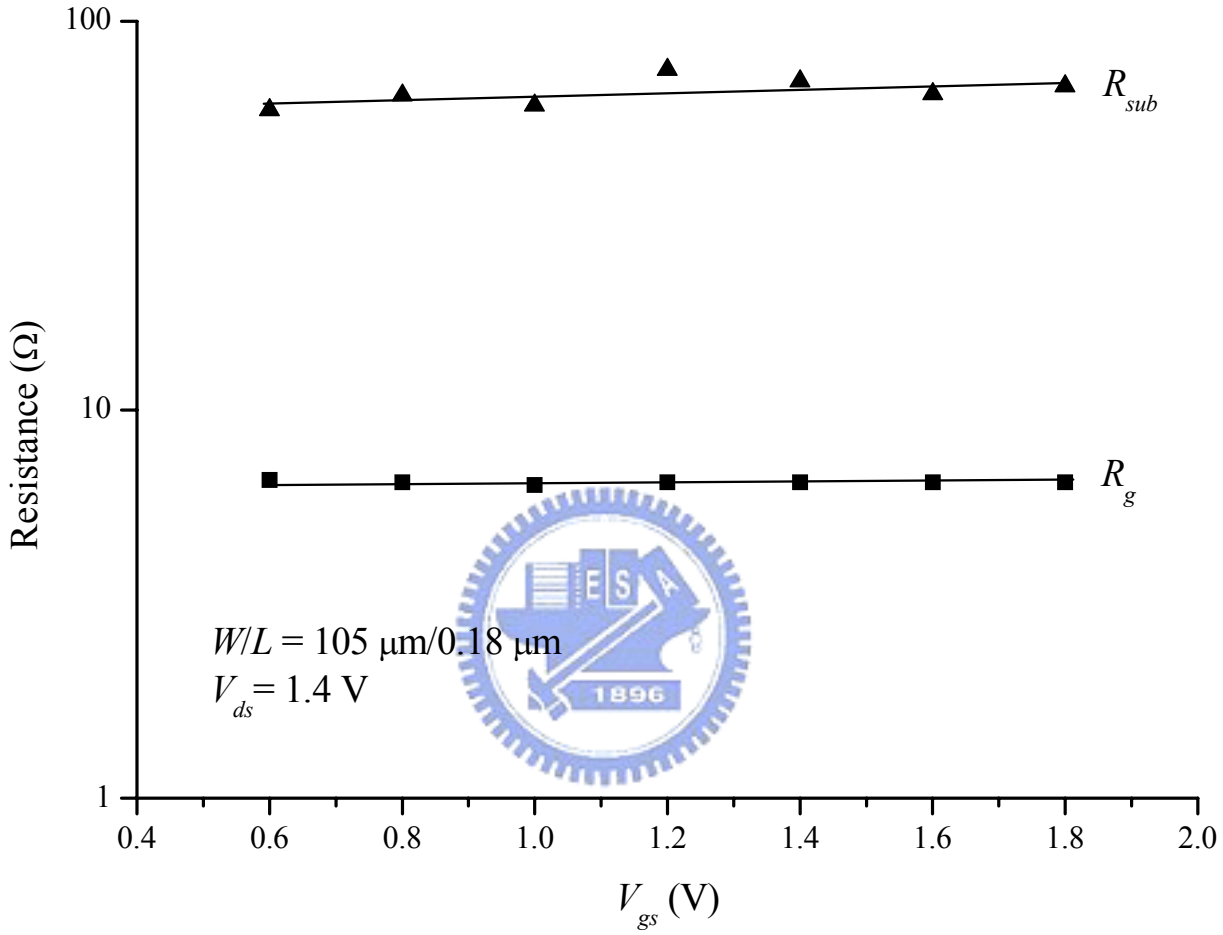

100
10
1
Resistance (Ω)
R_{sub}
R_g
W/L = 105 μm/0.18 μm
V_{ds} = 1.4 V
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
V_{gs} (V)

Fig. 5–11(b)

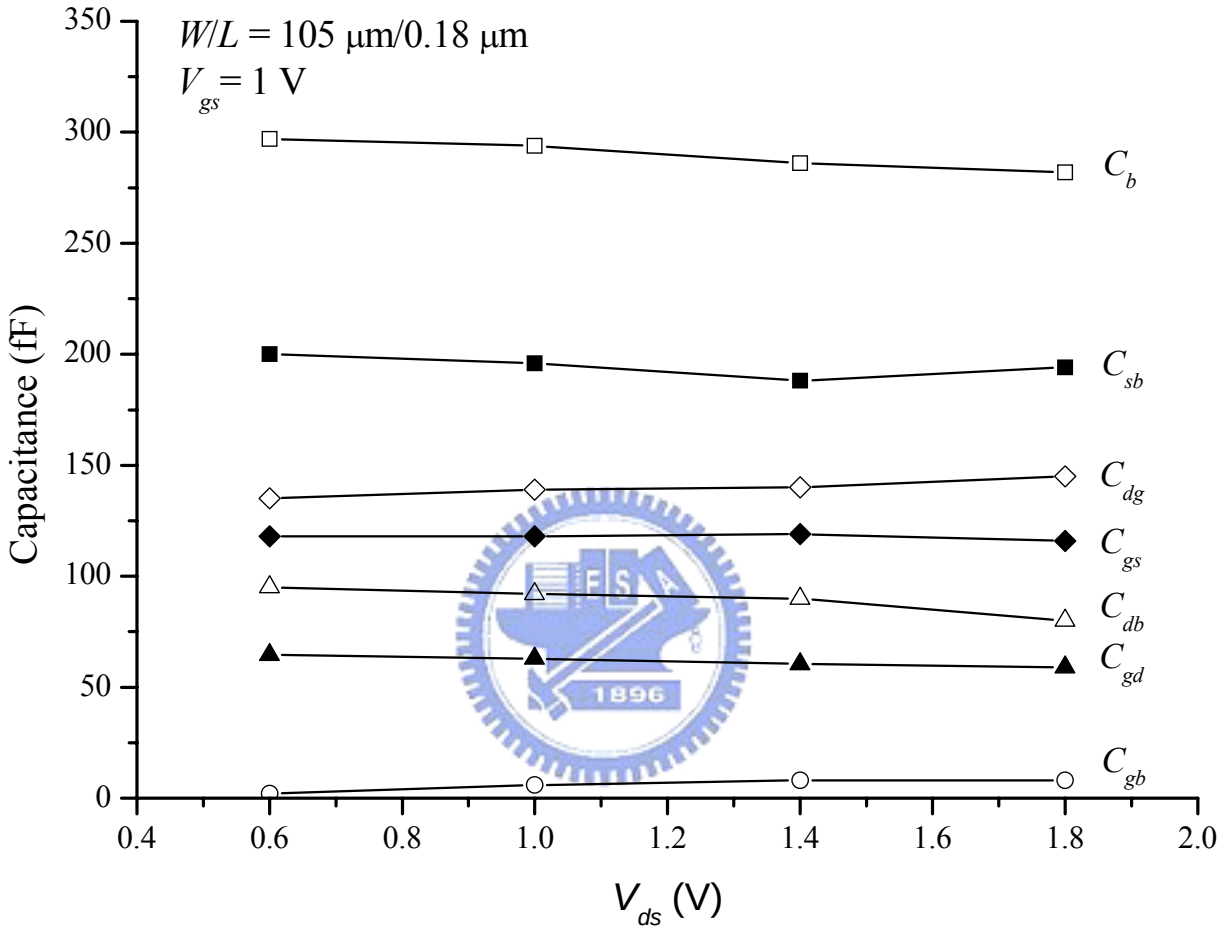

W/L = 105 μm/0.18 μm
V_gs = 1 V
Capacitance (fF)
V_ds (V)
C_b
C_sb
C_dg
C_gs
C_db
C_gd
C_gb
350
300
250
200
150
100
50
0
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

Fig. 5–12(a)

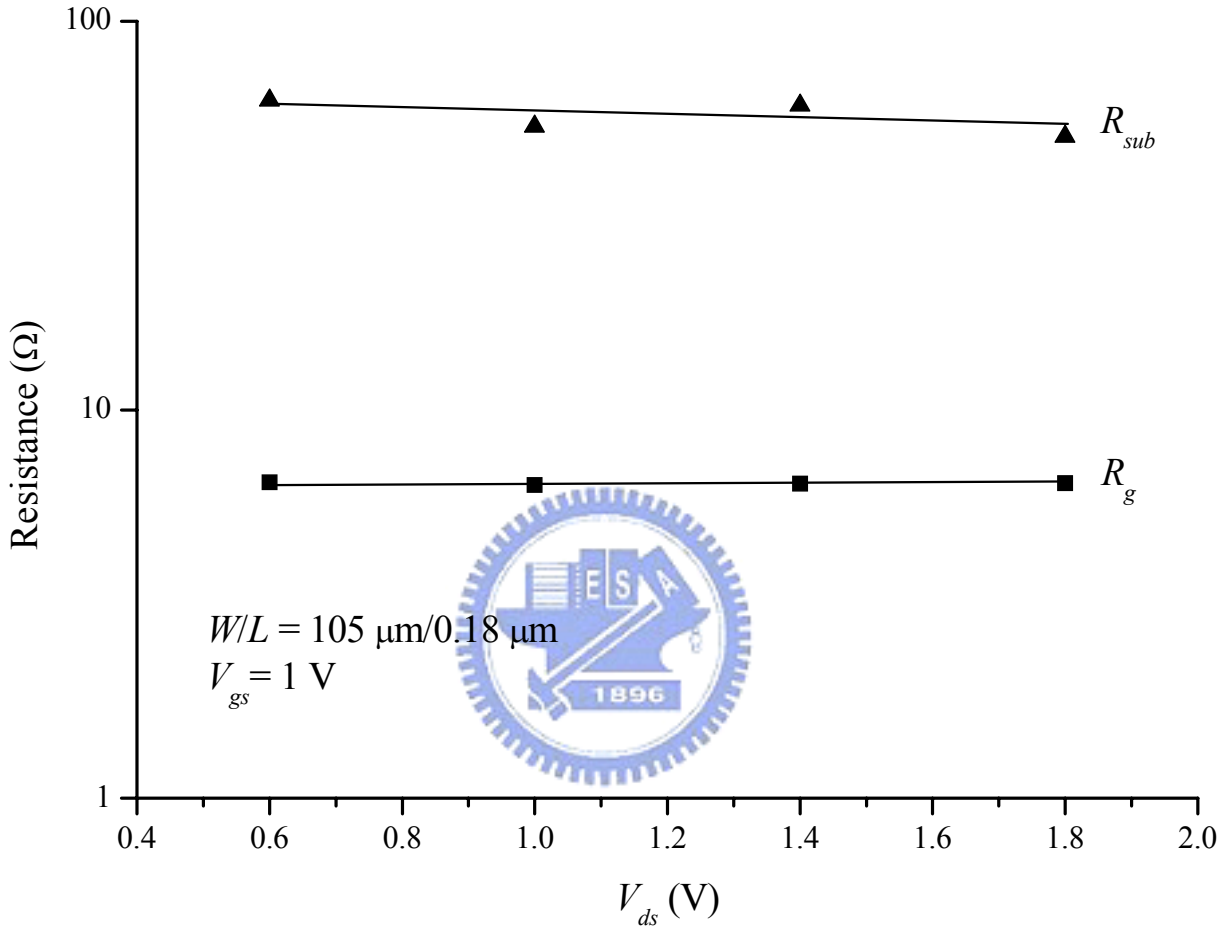

100
10
1
Resistance (Ω)
R_{sub}
R_g
W/L = 105 μm/0.18 μm
V_{gs} = 1 V
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
V_{ds} (V)

Fig. 5–12(b)

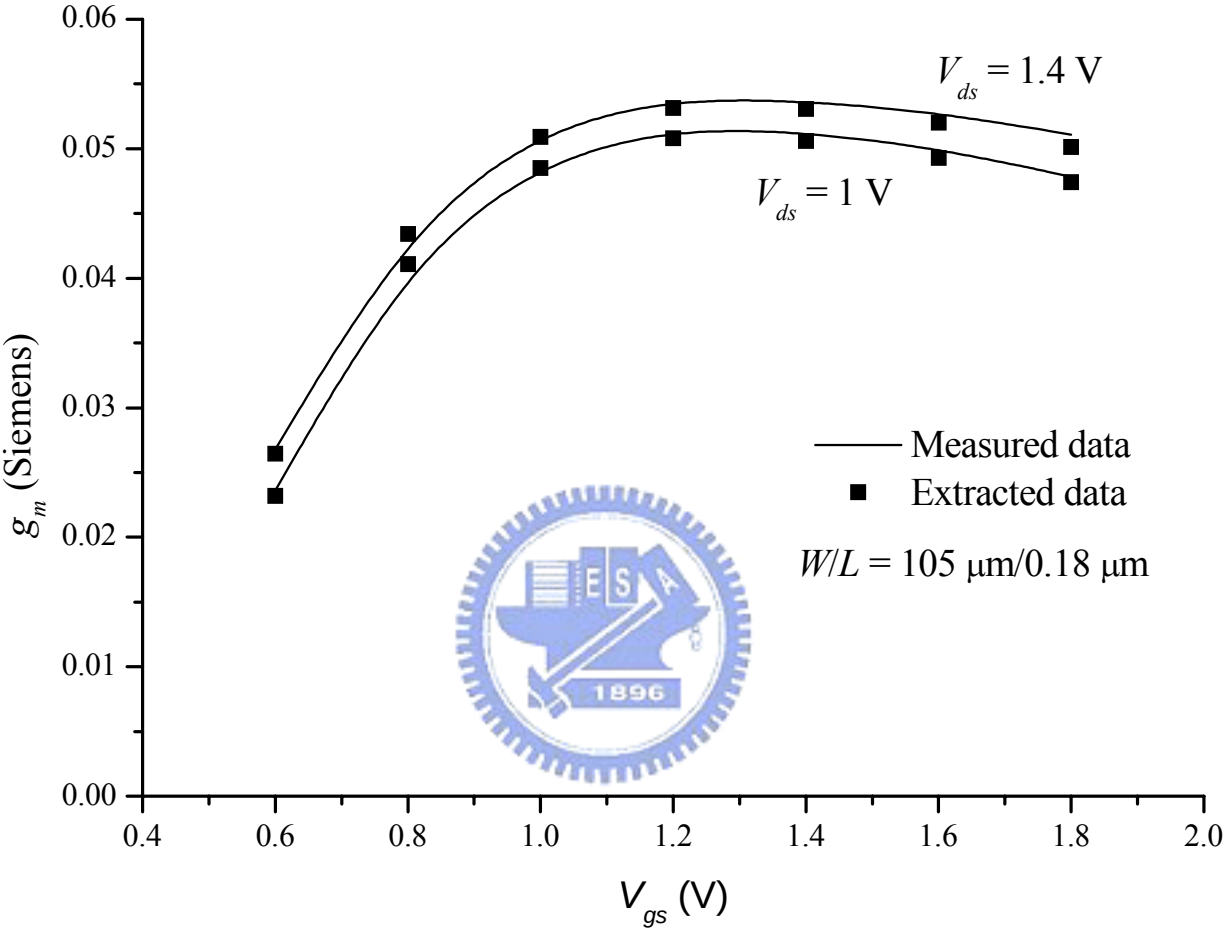

0.06
0.05
0.04
0.03
0.02
0.01
0.00
g_m (Siemens)
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
V_{gs} (V)
V_{ds} = 1.4 V
V_{ds} = 1 V
Measured data
Extracted data
W/L = 105 μm/0.18 μm

Fig. 5–13(a)

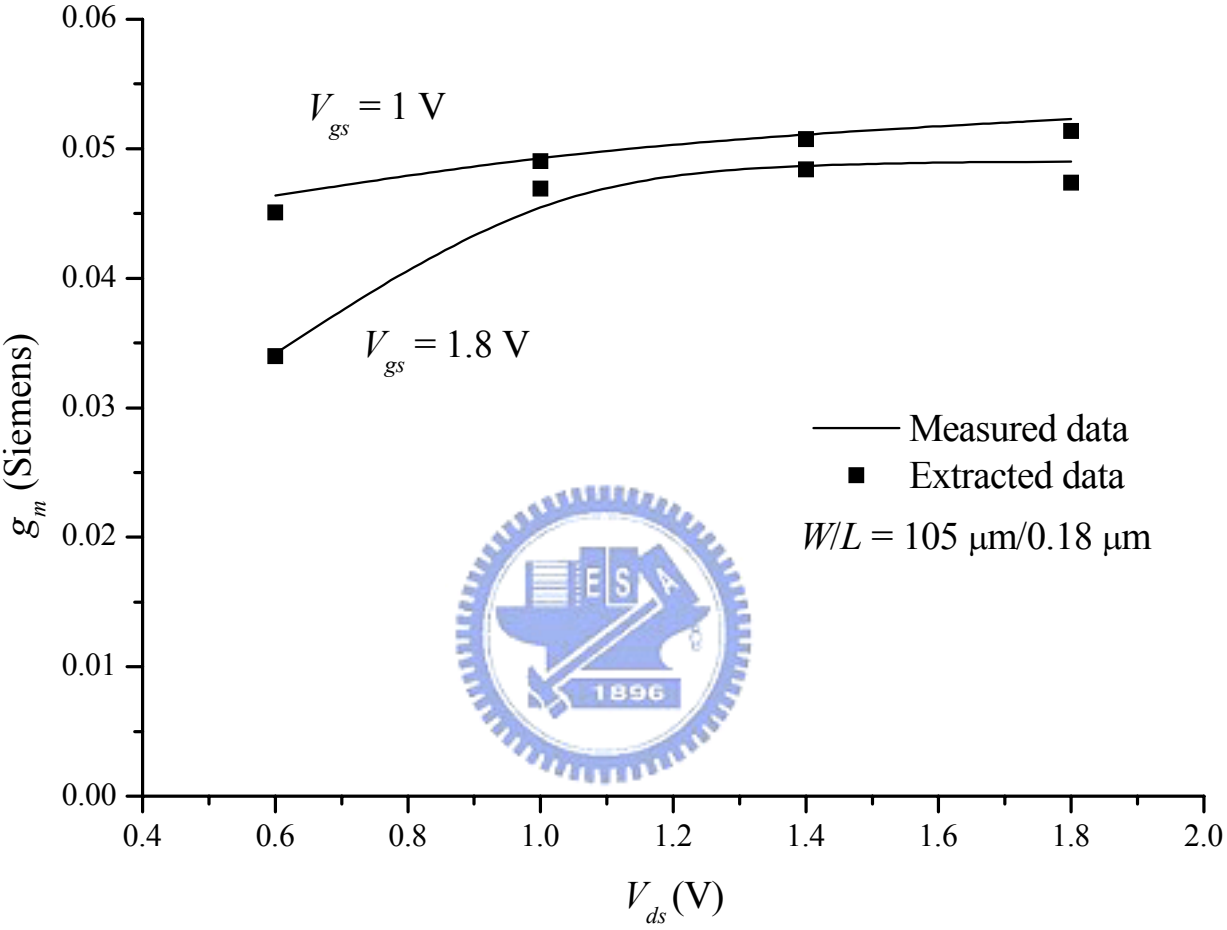

0.06
0.05
0.04
0.03
0.02
0.01
0.00
g_m (Siemens)
V_{gs} = 1 V
V_{gs} = 1.8 V
Measured data
Extracted data
W/L = 105 μm/0.18 μm
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
V_{ds} (V)

Fig. 5–13(b)

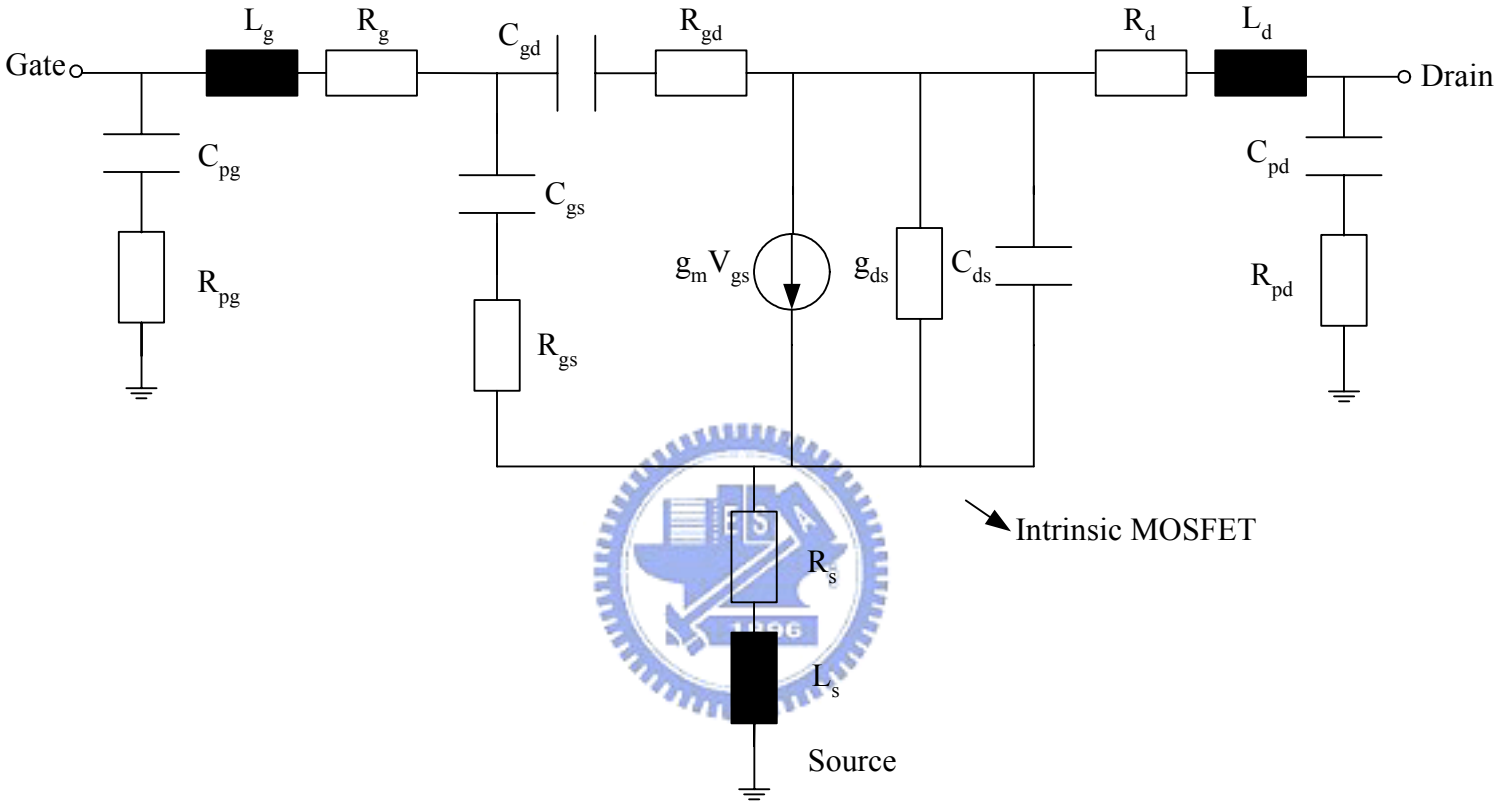

Gate
Drain
L_g
R_g
C_{gd}
R_{gd}
R_d
L_d
C_{pg}
R_{pg}
C_{gs}
R_{gs}
$g_m V_{gs}$
g_{ds}
C_{ds}
C_{pd}
R_{pd}
Intrinsic MOSFET
R_s
L_s
Source

Fig. 6–1

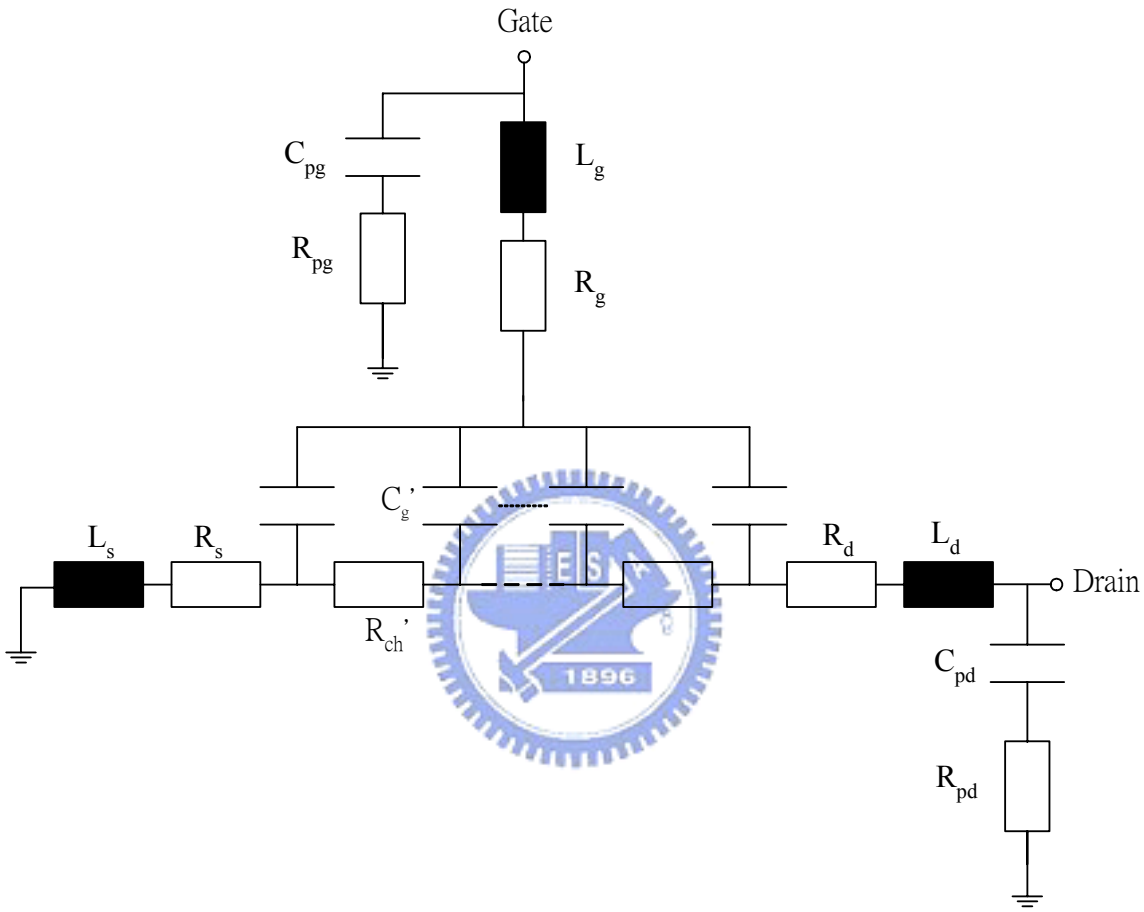


Fig. 6–2

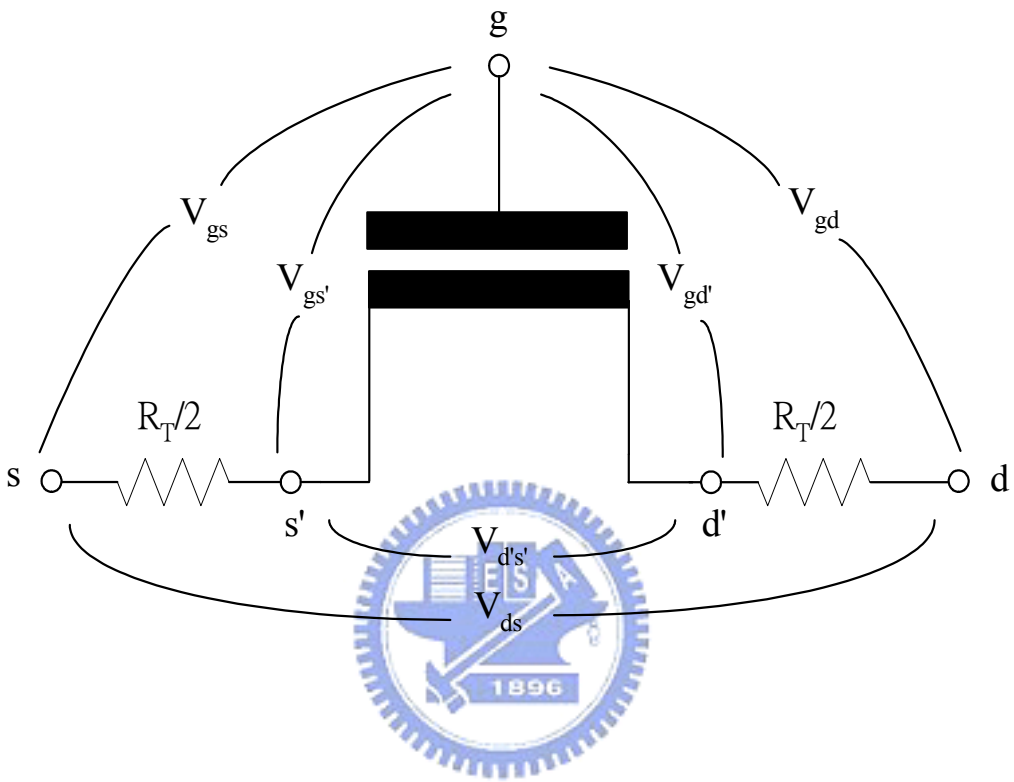


Fig. 6–3

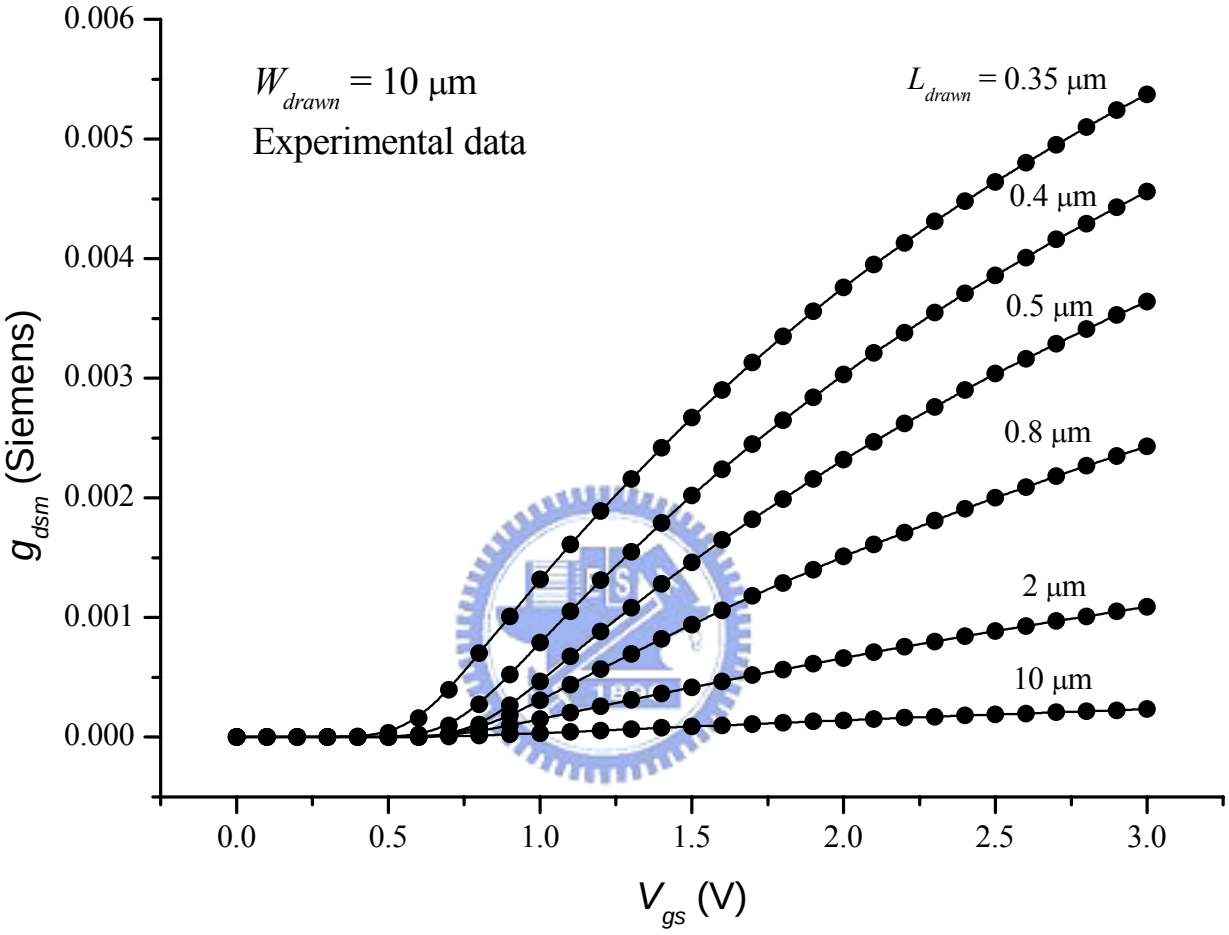

W_{drawn} = 10 μm
Experimental data
L_{drawn} = 0.35 μm
0.4 μm
0.5 μm
0.8 μm
2 μm
10 μm
g_{dsm} (Siemens)
V_{gs} (V)
0.006
0.005
0.004
0.003
0.002
0.001
0.000
0.0
0.5
1.0
1.5
2.0
2.5
3.0

Fig. 6–4

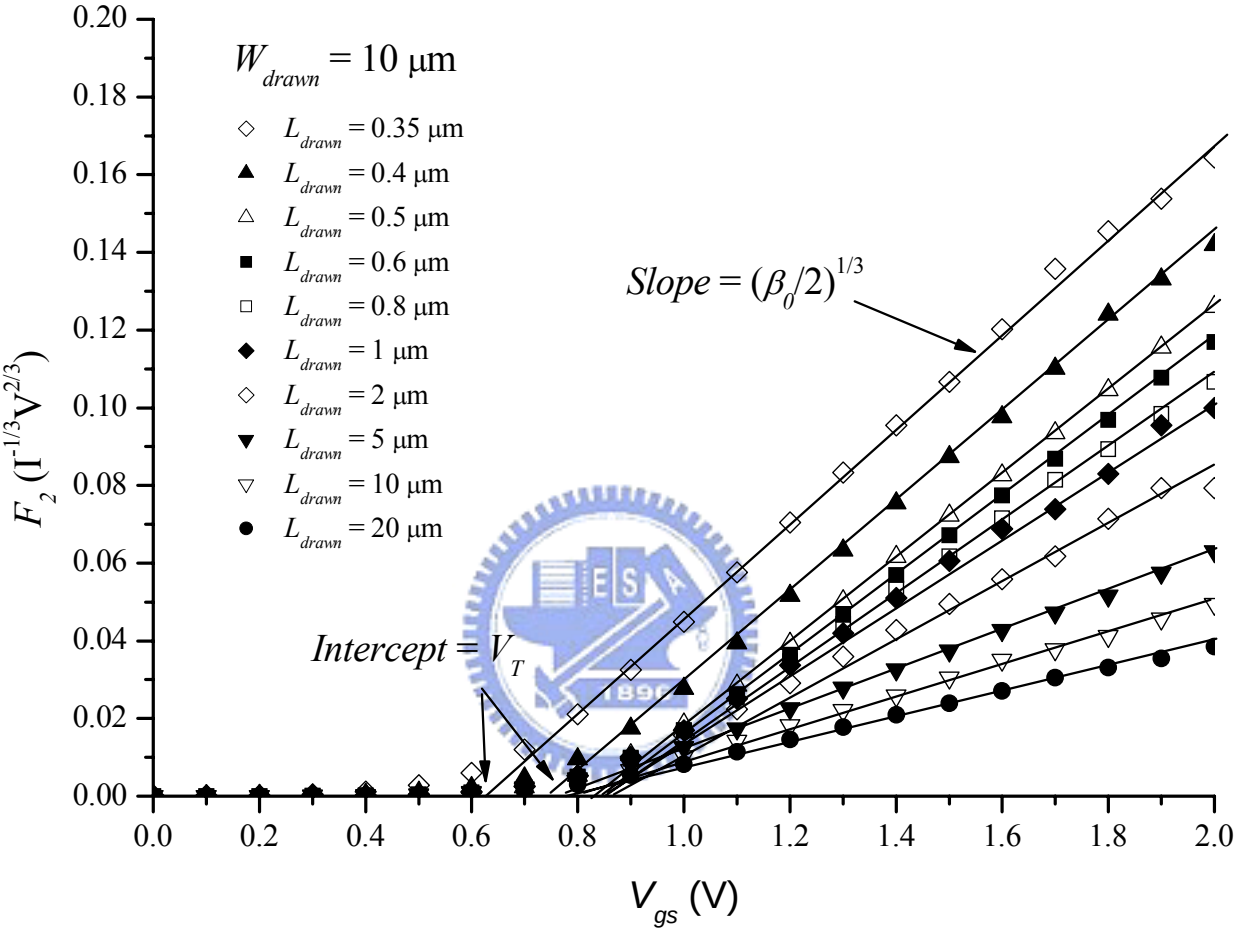

W_{drawn} = 10 μm
L_{drawn} = 0.35 μm
L_{drawn} = 0.4 μm
L_{drawn} = 0.5 μm
L_{drawn} = 0.6 μm
L_{drawn} = 0.8 μm
L_{drawn} = 1 μm
L_{drawn} = 2 μm
L_{drawn} = 5 μm
L_{drawn} = 10 μm
L_{drawn} = 20 μm
$Slope = (\beta_0/2)^{1/3}$
$Intercept = V_T$
$F_2 (I^{-1/3}V^{2/3})$
V_{gs} (V)
0.00
0.02
0.04
0.06
0.08
0.10
0.12
0.14
0.16
0.18
0.20
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0

Fig. 6–5

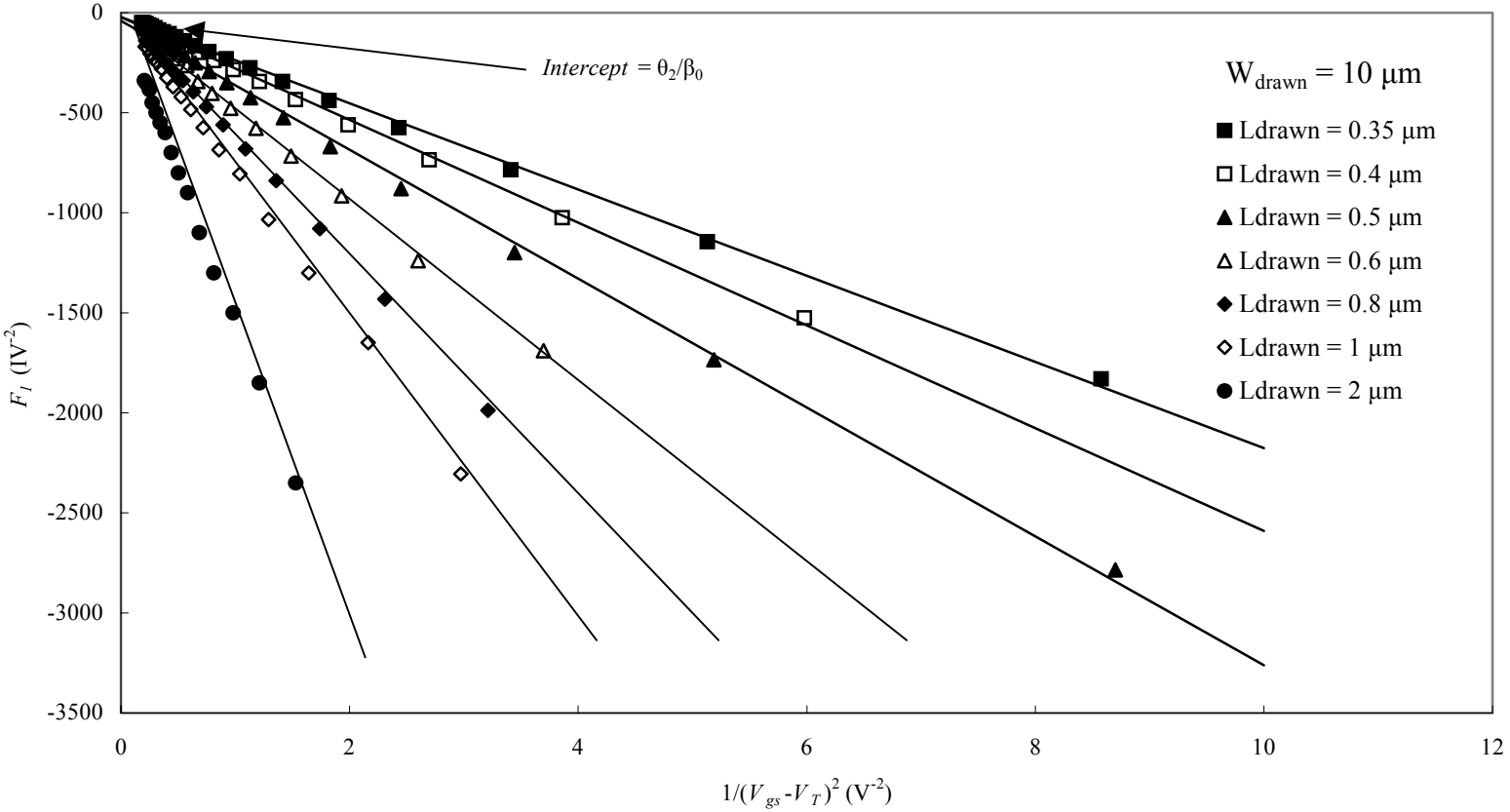

0
-500
-1000
-1500
-2000
-2500
-3000
-3500
0
2
4
6
8
10
12
F_1 (V^{-2})
$1/(V_{gs}-V_T)^2$ (V^{-2})
Intercept = θ_2/β_0
W_{drawn} = 10 μm
Ldrawn = 0.35 μm
Ldrawn = 0.4 μm
Ldrawn = 0.5 μm
Ldrawn = 0.6 μm
Ldrawn = 0.8 μm
Ldrawn = 1 μm
Ldrawn = 2 μm

Fig. 6–6

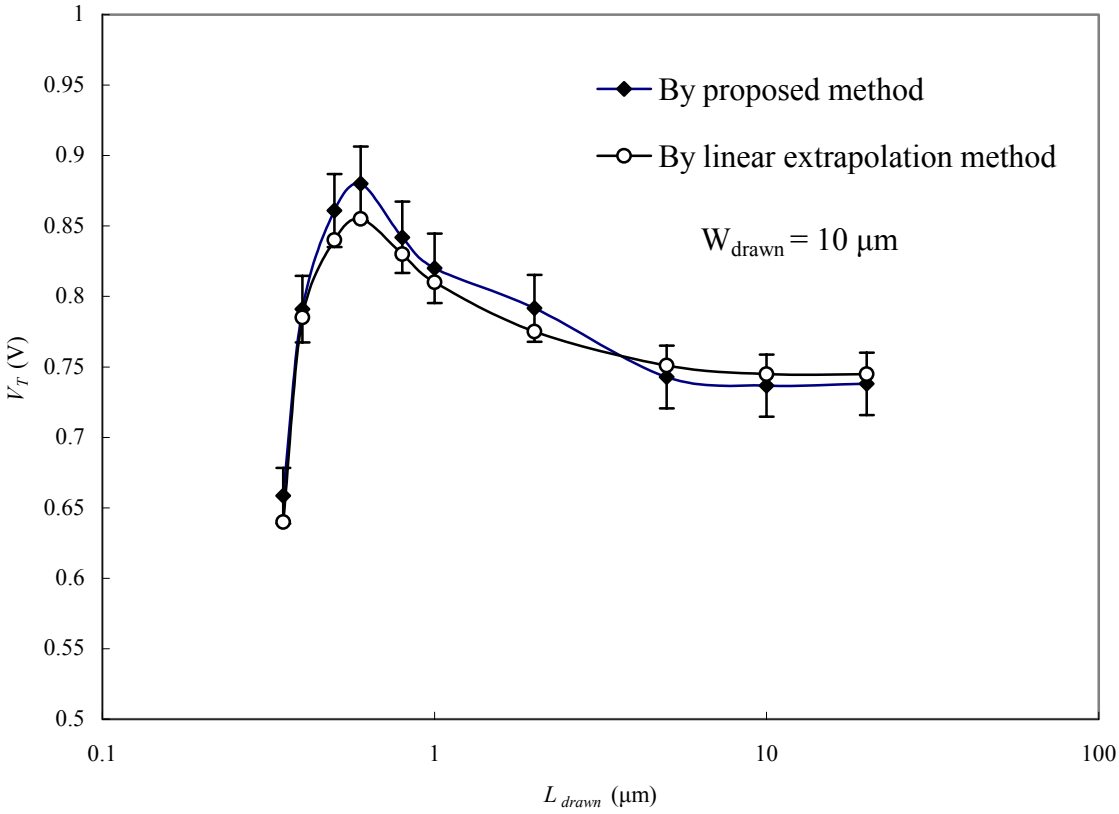

By proposed method
By linear extrapolation method
W drawn = 10 µm
V T (V)
L drawn (µm)
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.1
1
10
100

Fig. 6–7

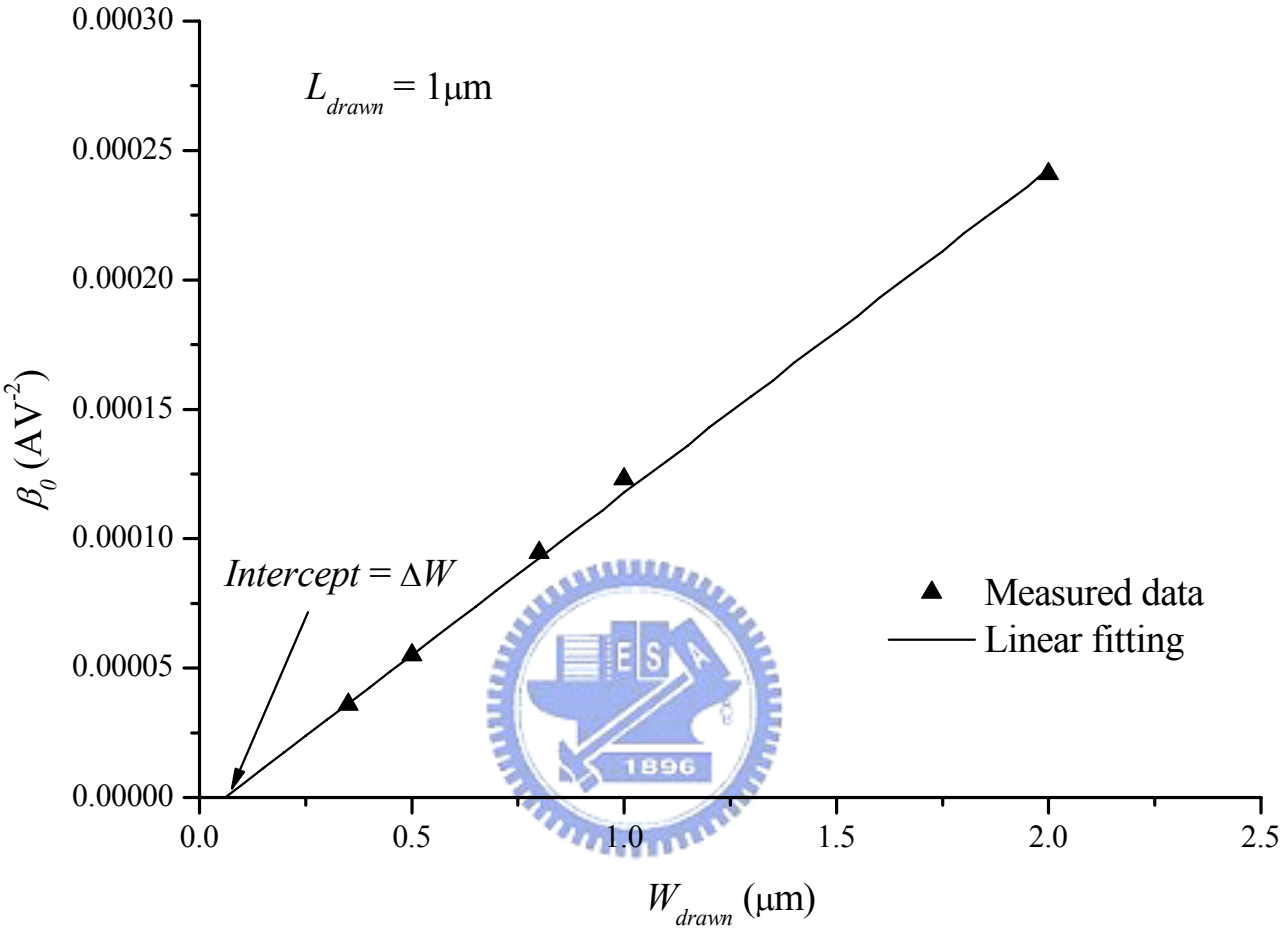

0.00030
0.00025
0.00020
0.00015
0.00010
0.00005
0.00000
β_0 (ΔV^{-2})
L_{drawn} = 1μm
Intercept = ΔW
Measured data
Linear fitting
0.0
0.5
1.0
1.5
2.0
2.5
W_{drawn} (μm)

Fig. 6–8(a)

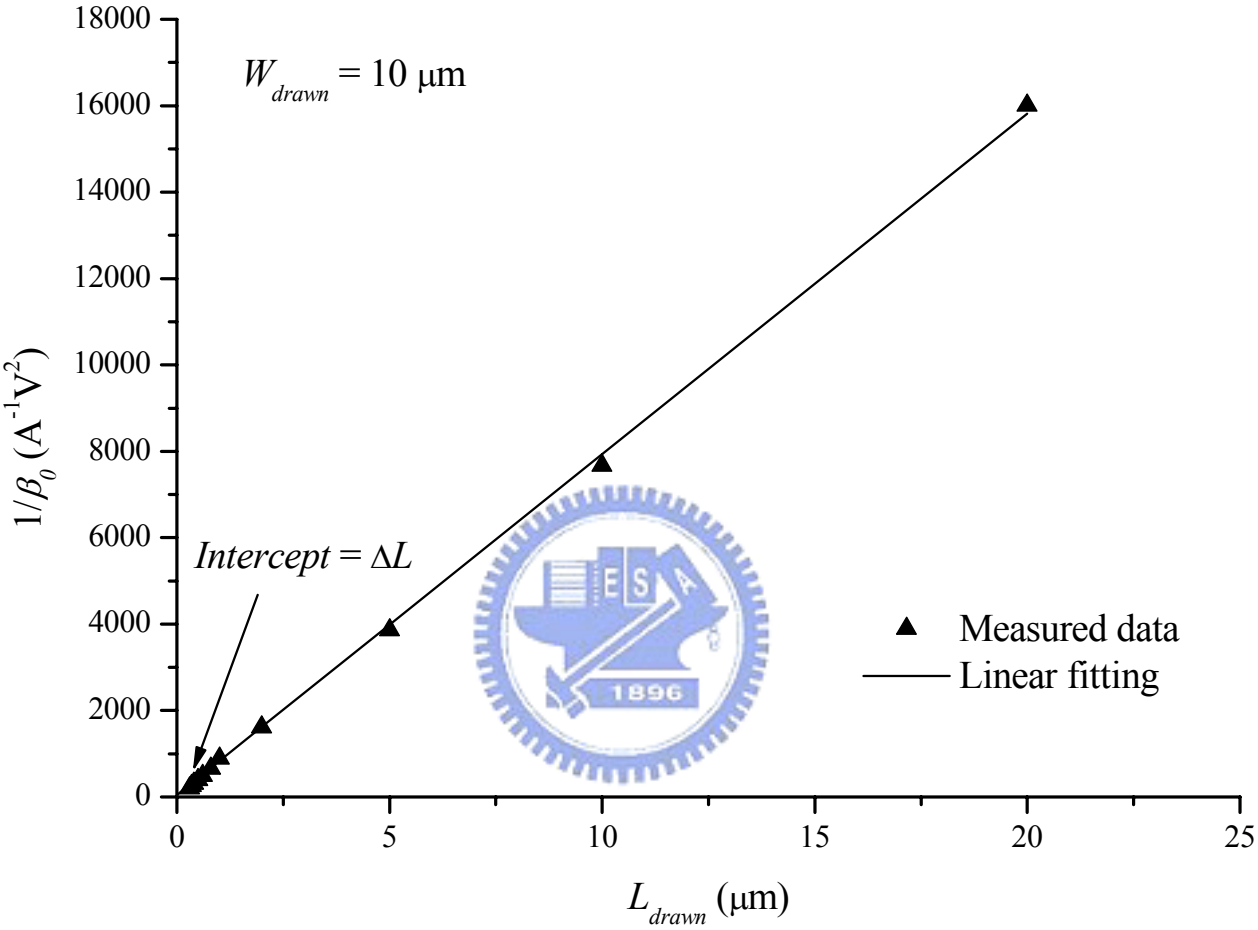

18000
16000
14000
12000
10000
8000
6000
4000
2000
0
0
5
10
15
20
25
W_{drawn} = 10 μm
$1/\beta_0$ ($A^{-1}V^2$)
Intercept = ΔL
Measured data
Linear fitting
L_{drawn} (μm)

Fig. 6–8(b)

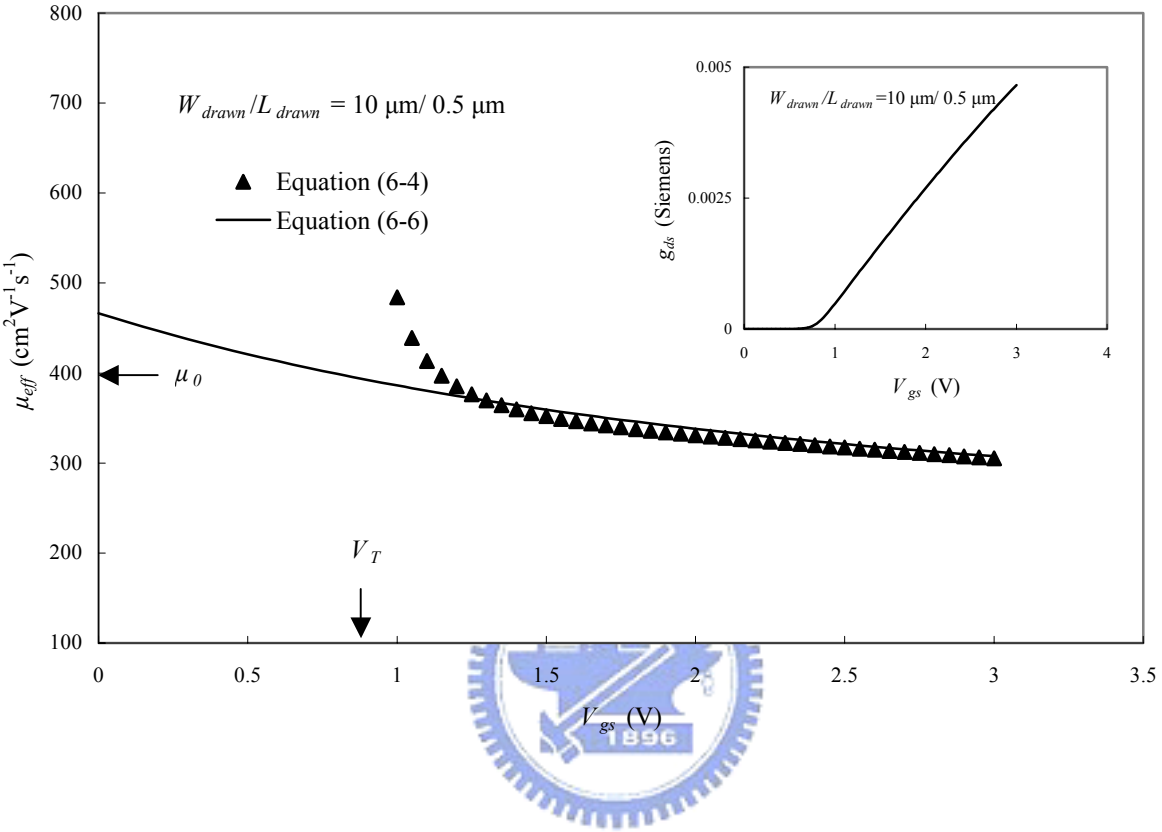

800
700
600
500
400
300
200
100
0
0.5
1
1.5
2
2.5
3
3.5
W_{drawn}/L_{drawn} = 10 μm/ 0.5 μm
Equation (6-4)
Equation (6-6)
μ_0
V_T
μ_{eff} ($cm^2V^{-1}s^{-1}$)
V_{gs} (V)
0.005
0.0025
0
g_{ds} (Siemens)
W_{drawn}/L_{drawn} =10 μm/ 0.5 μm
0
1
2
3
4
V_{gs} (V)

Fig. 6–9

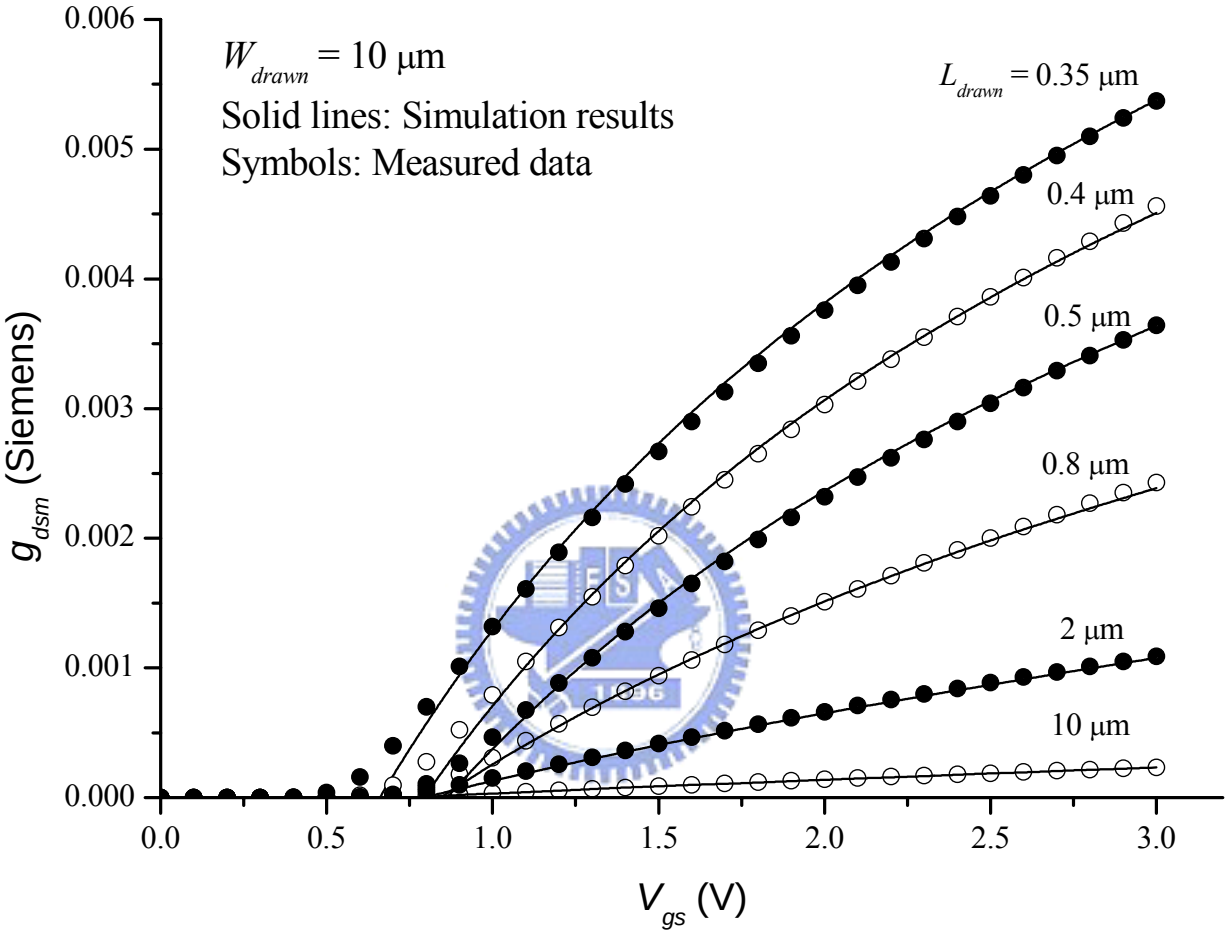

W_{drawn} = 10 μm
Solid lines: Simulation results
Symbols: Measured data
L_{drawn} = 0.35 μm
0.4 μm
0.5 μm
0.8 μm
2 μm
10 μm
g_{dsm} (Siemens)
V_{gs} (V)
0.000
0.001
0.002
0.003
0.004
0.005
0.006
0.0
0.5
1.0
1.5
2.0
2.5
3.0

Fig. 6–10

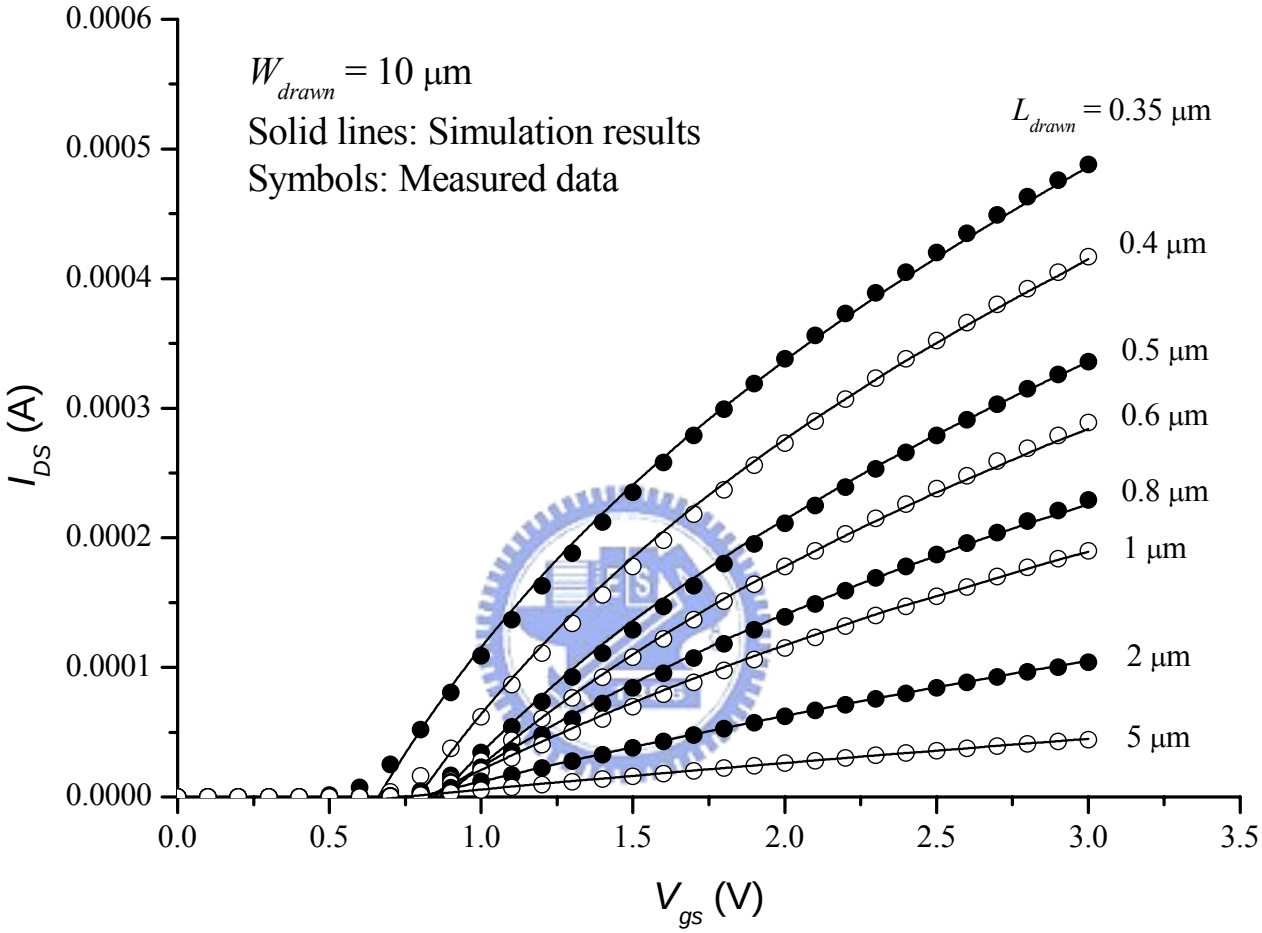

W_{drawn} = 10 μm
Solid lines: Simulation results
Symbols: Measured data
L_{drawn} = 0.35 μm
0.4 μm
0.5 μm
0.6 μm
0.8 μm
1 μm
2 μm
5 μm
I_{DS} (A)
V_{gs} (V)
0.0000
0.0001
0.0002
0.0003
0.0004
0.0005
0.0006
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5

Fig. 6–11

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博士論文題目：

完全空乏型單晶矽在絕緣層上之短通道金氧半場效電晶體的二維分析及新解析模式

2–D Analysis and New Analytical Models for Fully–Depleted SOI Short–Channel MOSFETs

PUBLICATION LIST

[1] Kow–Ming Chang and Han–Pang Wang, “A new small–signal MOSFET model and parameter extraction method for RF IC's application,” *Microelectronics Journal*, vol. 35, no. 9, pp. 749–759, Sept. 2004.

[2] Kow–Ming Chang and Han–Pang Wang, “Analytical Threshold Voltage and I–V Models for Fully–Depleted Short–Channel SOI MOSFET,” *accepted for publication in Japanese Journal of Applied Physics*.

[3] Kow–Ming Chang and Han–Pang Wang, “A Simple 2D Analytical Threshold Voltage Model for Fully–Depleted Short–Channel SOI MOSFETs,” *accepted for publication in Semiconductor Science and Technology*.

[4] Kow–Ming Chang and Han–Pang Wang, “A new quasi–2D analytical threshold–voltage model for partially–depleted short–channel SOI MOSFET,” *WSEAS Trans. Mathematics*, vol. 3, no. 4, pp. 341–345, Apr. 2004.

[5] Kow–Ming Chang and Han–Pang Wang, “A new small signal RF MOSFET model,” *WSEAS Trans. Circuit and Systems*, vol. 3, no. 5, pp. 453–458, May. 2004.

[6] Kow–Ming Chang and Han–Pang Wang, “Parameter extraction method for ultra–thin oxide MOSFETs using small–signal channel conductance measurement,” *WSEAS Trans. Circuit and Systems*, vol. 3, no. 7, pp. 1257–1261, July. 2004.

[7] Kow–Ming Chang and Han–Pang Wang, “New Analytical Models of Subthreshold Surface Potential and Subthreshold Current for Fully–Depleted Short–Channel SOI MOSFETs With Halo or Pocket Implantation,” *revised to Journal of Solid–State Electronics*, 2004.

[8] Kow–Ming Chang and Han–Pang Wang, “A New 2–D Model for the Potential Distribution and Threshold Voltage of Fully Depleted Short–Channel SOI MOSFETs With Halo or Pocket Implants,” *submitted to Journal of Solid–State Electronics*, 2004.

[9] Kow–Ming Chang and Han–Pang Wang, “An efficient method for determining threshold

voltage, effective inversion layer mobility, series resistance, and effective geometries of MOSFETs by *S*-parameters measurement," *submitted to IEEE Trans. Electron Devices*, 2004.