Chapter 4

High Voltage Applications and NBTI Effects of DTMOS with Reverse Schottky Substrate Contacts

4.1 Background and Motivation

The PN diode between substrate and source terminals would turn on as gate/substrate bias larger than 0.7 V for n-channel DT-MOSFETs. Considerably large leakage current due to the turn-on diode current between substrate and source terminals would restrict the operation voltage of DT-MOSFETs, as shown in Fig. 4.1(a). Schottky barrier contact [7-9] formation on the substrate contact under DT-mode operation was proposed to restrict the turn-on diode.

Using the structure, which reverse Schottky barrier was formed on substrate contact, DT-MOSFETs can operate at high voltage and exhibit excellent performance, even at high temperature. Furthermore, a drift in threshold voltage due to the reliability degradation is a major concern in the analog and mixed-signal applications. Negative Bias Temperature Instability (NBTI) of p^+-gate MOSFETs has been reported as one of the serious issues for the reliability of ultra-thin gate dielectrics due to a higher threshold voltage degradation [23-25]. The NBTI degradation was used as a limit of the device's lifetime when the gate oxide thickness was less than 3.5 nm. In

addition, the stressing temperature ranged from 100 ℃ to 200 ℃, and E_{OX} by gate electrode was from –6 MV/cm to –15 MV/cm. Higher temperature stress enhanced NBTI and its degradation was thermally activated, as well as being sensitive to temperature effects, as shown in Equations (4-1) and (4-2) [26].

$$\Delta N_{it} = 9\times10^{-4} E_{OX}^{1.5} t^{0.25} \times t_{OX}^{-1} \exp(-0.2/kT) \quad (4\text{-}1)$$

$$\Delta N_{f} = 490 E_{OX}^{1.5} t^{0.14} \exp(-0.15/kT) \quad (4\text{-}2)$$

However, the detailed degradation process is still not well understood. There are no reports about the effects of NBTI under DT-mode operation, which means that the gate oxide characteristics could not be understood as DTMOS operation. This is because the gate voltage of DT-pMOSFETs must be less than -0.7 V. In this chapter, the novel structure and electrical characteristics of DT-MOSFETs were reported with a reverse Schottky substrate contact for its high voltage and temperature applications. In addition, the NBTI effect of this device will be discussed in this chapter simultaneously.

4.2 Device Fabrication for nMOSFET with with reverse Schottky substrate contacts

N-channel MOS transistors with channel length down to 0.8 μm were fabricated on 6-in silicon wafers with resistivity of 15-20 Ω-cm using a conventional nMOSFET baseline. Local oxidation of silicon (LOCOS) was used for device isolation. A BF_2 channel implant (at 50 keV, 1×13 cm^{-2}) was used for V_{TH} adjustment

of all transistors. Gate dielectric thickness of 2.8 nm was grown in N_2O ambient followed by a 200 nm poly-Si deposition. The width is 100 μm. Shallow source/drain (S/D) extensions were formed by As^+ implant at 10 keV to a dose of 4×10^{14} cm^{-2}. After the formation of TEOS sidewall spacer (200 nm), deep S/D junctions were formed by As^+ implantation at 20 keV to a dose of 5×10^{15} cm^{-2}. Wafers were then annealed by a rapid thermal annealing (RTA) at 1020 °C for 20-sec. A 25nm Co film was sputtered followed by a 5 nm capping layer of TiN. Two-step RTA (first at 550 °C for 30-sec. and second at 850 °C for 30-sec.) was used for Co-salicidation. Finally, a 550-nm-thick TEOS by PECVD was deposited and etched for contact holes. A Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations were carried out with a HP4156 system, and the measurement temperature was 27, 75, 100 °C, respectively.

4.3 Experimental Results and Discussion for nMOSFET with with reverse Schottky substrate contacts

Fig. 4.2(a) shows the drain current and transconductance versus gate voltage curves for nMOSFETs which gate length was equal to 0.8 μm with width equal to 100 μm for DT-mode without reverse Schottky barrier on substrate contact. As the V_G>0.7 V, the diode between source and substrate would be turned on, and then both

the drain current and transconductance decrease quickly. The drain current versus drain voltage for the same device was shown in Fig. 4.2(b). The disaster under DT-mode was due to the leakage current between the substrate and source terminals diode, which limit the operation voltage of DT-mode to V_G<0.7 V. Figure 4.1(a) shows the cross-section of DT-MOSFETs with reverse Schottky barrier on substrate contacts (RSBSC) and equivalent circuit (Fig. 4.1(b)). From the figure, it can be seen that the gate to substrate connection was through n^+ poly-Si gate, Co-Schottky barrier and to p^- substrate. Since Co-Schottky barrier is reversed biased when V_G is larger than 0.7 V, the pn junction of substrate/source (S/S) will not turn on when V_G > 0.7 V. Furthermore, when using RSBSC, voltage will drop on the reverse Schottky barrier. Junction of S/S doesn't turn on as V_G > 0.7 V. Figure 4.3(a) shows the transconductance versus gate voltage for device, which gate length was equal to 0.8 μ m with width equal to 100 μ m for conventional mode operation (i.e., Vsub=0 V) and DT-MOSFETs (i.e., V_G=Vsub) at room temperature. About 7 % improvement was showed in Fig. 4.3(a) due to the dynamic reduction of the threshold voltage. The drain current versus drain voltage, where V_G is from 1 V to 3V with a 0.5 V step was shown in Fig.4.3(b). It is very interesting that the leakage current behavior due to the turn-on S/S diode do not exit for DT-MOSFETs with RSBSC scheme. In addition, the saturation current under DT-mode at high drain voltage was larger than that under

conventional mode. Therefore, DT-MOSFETs with RSBSC can be operated at V_G > 0.7 V. Due to the limited forward diode voltage drop, and the threshold voltage would be also decreased about 90 mV. The drain current under DT-mode in Fig. 4.3(b) is larger than that under conventional mode due to the reduction threshold voltage. However, the magnitude of improvement was lower than conventional DT-MOS without RSBSC due to the smaller magnitude of the dynamic threshold voltage reduction. The gate capacitance increases since it is tied to the substrate. To reduce this effect, the Schottky barrier contact can be formed only through the smallest size of contact hole in substrate. The threshold voltage versus gate length under different temperature was shown in Fig. 4.4(a). The reduction of V_{TH} under DT-mode at 27 °C was about 90 mV (from 570 mV to 480 mV for 0.8 μm), and the reduction of V_{TH} of DT-MOS with RSBSC at higher temperature at 75 and 100 °C shows the same result. The subthreshold behavior at high temperature of DT-MOSFETs with RSBSC shows excellent performance, an ideal S.S. value was found and shown in Fig.4.4(b). The ideal values of subthreshold slope at 27 °C, 75 °C, and 100 °C deduced from KT/q(ln10) are 60, 68, and 74 mV/dec. respectively. The value of S.S. under conventional mode increases from 78 to 102 mV/dec. as temperature increases from 27 to 100 °C. However, the S.S. under DT-mode with RSBSC at 27 °C, 75 °C, and 100 °C are 62, 70, 78 mV/dec., which were almost close to ideal value. The difference

of S.S. between conventional and DT- modes increases as temperature increases. The reason for excellent S.S. of DT-MOS with RSBSC at elevated temperature is due to the reduced magnitude of $1+\frac{C_D}{C_{OX}}+\frac{C_{it}}{C_{OX}}$ under DT-mode operation [27]. Figure 4.5 shows on-off current ratio under both the conventional and DT modes for different temperatures. Gate length varies from 10 to 0.8 μm, with a fixed width of 100 μm. The temperature was at 27 °C, 75 °C, and 100 °C, and the on-current was at V_G=V_D=1.8 V. Due to the reduction of V_{TH} and increasing transconductance under DT-mode, the on current was increased. On the other hand, the off current was not increased due to the V_G=V_{sub}=0 V at off state.

4.4 Device Fabrication for pMOSFET with with reverse Schottky substrate contacts

P-channel MOS transistors with channel length as small as 0.8 μm were fabricated on 6-in silicon wafers with resistivities of 15-20 Ω-cm using a conventional pMOSFET baseline. Local oxidation of silicon (LOCOS) was used to isolate the device. An As^+ channel implant (at 100 keV, 1×13 cm^{-2}) was used for the adjustment of the threshold voltage. A gate dielectric with a thickness of 2.8 nm was grown in an ambient N_2O atmosphere, followed by a 200 nm poly-Si deposition. The channel width was 100 μm. Shallow S/D extensions were formed by BF_2 implant at 10 keV to

a dose of 1×10^{15} cm^{-2}. After the formation of a TEOS sidewall spacer (200 nm), deep source/drain junctions were formed by BF_2 implantation at 20 keV to a dose of 6×10^{15} cm^{-2}. Wafers were then annealed by a rapid thermal process (RTP) at 1020 °C for 20 sec for dopant activation. Finally, a 550 nm-thick TEOS by PECVD was deposited, and a Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete the contact metallization. Without any substrate ion implantation, the substrate contact formed was a Ti-silicide on an n^- type substrate. Finally, gas sintering was performed on metal alloy at 400 °C. Electrical characterizations were performed using a HP4156 system and a temperature-regulated hot chuck at temperature ranging from 25 °C to 100 °C.

4.5 Experimental Results and Discussion for pMOSFET with reverse Schottky substrate contacts

4.5.1 Electrical characteristics of DT-pMOSFETs with Reverse Schottky Substrate Contacts.

Figure 4.6 shows the cross section and equivalent circuits of the device after silicidation. Instead of n^+ substrate ion implantation forming ohmic contact, the n^--substrate was reacted directly with Ti in order to form a Schottky barrier. In operation, the source was the ground, and the gate shorted to the substrate was biased

in negatively biased. It is well known that the serious issue under DT-mode occurs as substrate/source is forward biased, which is shown in Fig 4.6, exhibiting the diode's turn-on behavior. In order to avoid the condition to extend the application range of DT-MOSFETs, the substrate bias should be limited to below -0.7 V to avoid the junction turn-on behavior under DT-mode operation. Adding this reverse Schottky barrier, the voltage is only a cut-in voltage for source/substrate, and drops other voltage on the reverse Schottky barrier. Hence, it can be operated in high voltage without any concerns of turn-on behavior. In addition, this structure still maintained the advantages of conventional DT-MOSFETs. The transfer characteristics were shown in Fig 4.7(a). The subthreshold slope was steep under the DT-mode operation. Fig 4.7(b) shows the drain current versus drain voltage, under different modes at room temperature, with the gate voltage ranging from 0 V to 3 V at -0.5 V steps. As expected, no turn-on diode characteristic in Fig 4.6 was found by adding the reverse Schottky substrate contact because the gate voltage was larger than –0.7 V. In addition, the saturation current under DT-mode at V_D=-2.5 V and V_G=-3.0 V was large than that under conventional mode (about 20%). This was due to the good V_{TH} reduction and increasing transconductance under DT-mode operation [27-29]. The threshold voltages of DT-mode and conventional mode for the device were –241.8 mV and –350.4 mV, respectively. The gate voltage versus transconductance for DT and

conventional modes is depicted in Fig 4.8(a), where V_D=-0.1 V. The hump behavior of transconductance under DT-mode was due to the body potential limitation by the reverse Schottky Substrate barrier. The threshold voltage versus substrate bias for conventional devices with Schottky substrate contacts, which was simulated the DT-mode behavior, was also shown in Fig 4.8(b) for a range of temperatures. The absolute value of threshold voltage decreases as the value of the substrate bias decreases to a negative value. However, the threshold voltage was almost constant as the substrate bias ＜-0.6 V as a result from the reverse biased Schottky barrier at the substrate contacts. In addition, the reverse Schottky barrier contacts could prevent from the turn-on behavior between source/substrate junction, as shown in Fig 4.6. Saturation transconductance (V_G=V_D=-1.8 V) versus drain induced barrier lowering (DIBL) under different modes for two different temperature (25 °C &100 °C) was shown in Fig. 4.9. The magnitude of DIBL was decreased for DT-mode operation both for 25 °C &100 °C conditions. This is may be due to the substrate bias, which could decrease the depletion region as DTMOS operation [1]. Furthermore, the saturation transconductance was also increased for DT-MOSFETs due to the reduction of the threshold voltage, same as the linear transconductance.

4.5.2 NBTI effects of DT-MOSFETs

First of all, there is still no reference to the NBTI behaviors between

DT-MOSFETs and conventional MOSFETs comparisons due to the operation limitation of conventional DT-MOSFETs, as is shown in Fig. 4.6. The degradation of the threshold voltage due to NBTI effects of the DT-pMOSFETs was shown in Fig 10(a). The stressing conditions were V_G = -3.5 V, while other terminals were grounded at 100℃. As the interface density, D_{it}, and oxide trap charge increased, the absolute value of the threshold voltage increased as well [23-25]. To operate in conventional mode, the shift of the V_{TH} monotonically increases as the stressing time increases, and the value of ΔV_{TH} is about 46mV after 10000 seconds of stressing. However, it is interesting to note that the degradation of V_{TH} was significantly reduced and saturated by approximately 13 mV after 1000 seconds, while operating under DT-mode. This is due to the fact that the electrical field across gate oxide is alleviated by the substrate bias, $E_{OX} = \frac{V_G - V_{FB} - \varphi_s - V_{SUB}}{T_{OX}}$ under DT-mode operation. In addition, due to negative substrate bias while in DT-mode, the magnitude of the threshold voltage would be reduced [28], and DTMOS operation could decrease the variation of the threshold voltage [29]. Therefore, the threshold voltage degradation of NBTI effects under DT-mode operation could be effectively suppressed. Figure 10(b) depicts the log-log scale for Fig. 10(a). It is also interesting to note that the slopes as shown in Fig. 10(b), for DT and conventional modes do not depict any apparent differences. Finally, for the perspective of the NBTI effect, the threshold voltage degradation

under DT-mode operation was drastically improved due to the alleviated electrical field across the gate oxide and the threshold voltage adjustment. Stress time dependence of transconductance degradation ($\triangle$Gm= Gm(t)- Gm(0)) for pMOSFETs under different operation modes was also shown in Fig. 4.11. The magnitude of transconductance degradation was larger for the DT-mode operation, which was the same as the characteristics in Chapter 3. The dynamic behavior under DT-mode would enlarger the magnitude of transconductance magnitude.

4.6 Summary

DT-MOSFETs with reverse Schottky barrier on substrate contacts has been presented for high voltage and high temperature operations. Due to the reverse Schottky diode between gate and substrate, the operation voltage can be larger than 0.7 V. Both the saturation current and subthreshold slope could be improved by this scheme. We found that DT-MOSFETs with reverse Schottky barrier substrate contacts exhibit excellent performance operating at high temperature in terms of ideal substrate swing and increased driving current. Furthermore, the leakage current as V_G=0 V was the same for all devices due to the substrate bias V_{SUB}=0 V for DT devices. In addition, The electrical characteristics of DT-pMOSFETs with the reverse Schottky substrate contacts and its NBTI effects were reported in this study for the first time.

This structure showed the possibility that DT-MOSFETs operates at high voltage and temperature. It was found that the saturation current, DIBL, transconductance, and subthreshold slope could all be simultaneously improved. In addition, the serious V_{TH} degradation of NBTI stressing of conventional pMOSFETs was significantly reduced using the novel structure due to the alleviated electrical field across the gate oxide and the threshold voltage adjustment ability under DT-mode operation.

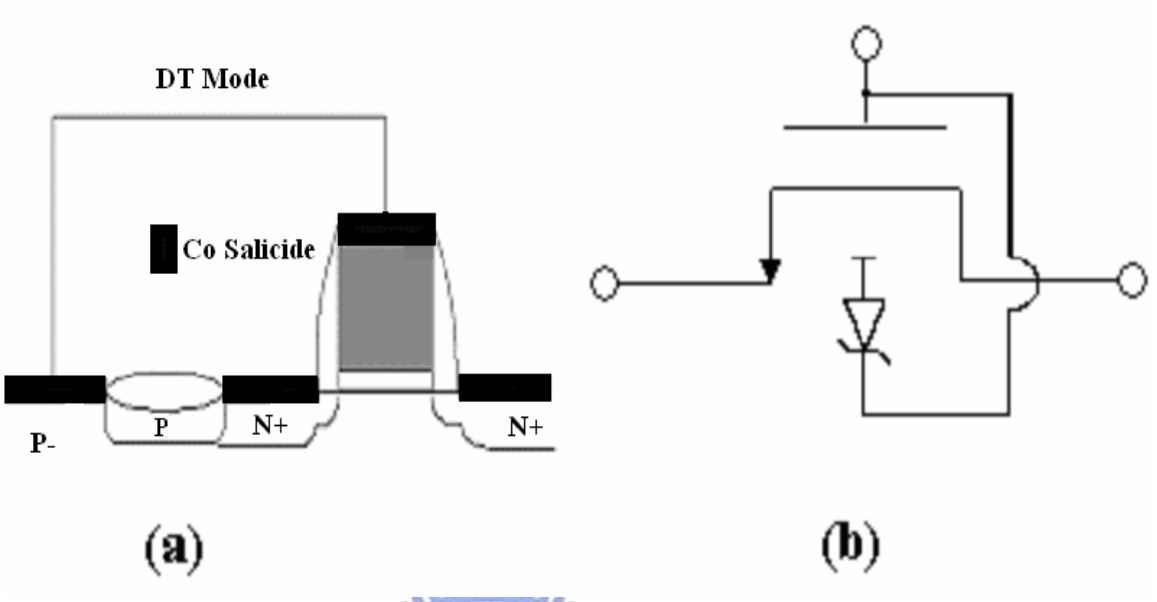
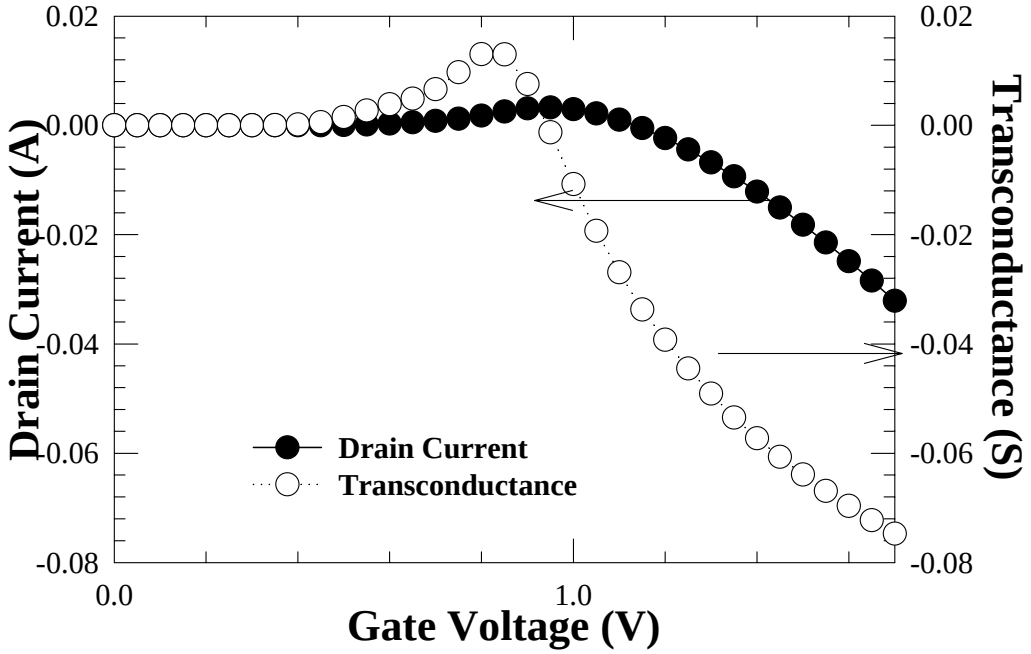
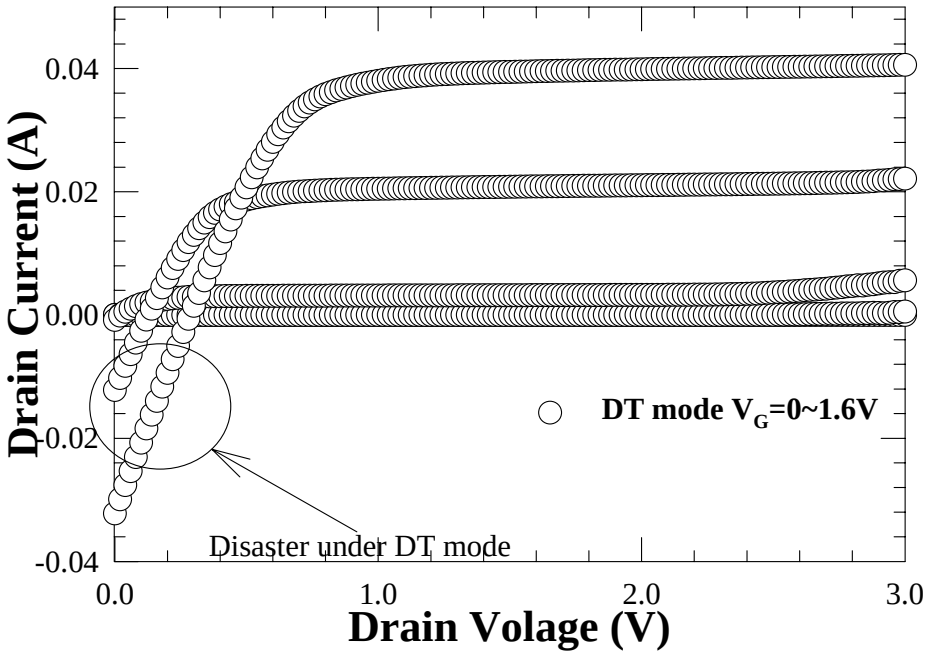


Fig. 4.1 (a) Connections of MOSFET under the DT-mode, and the reverse substrate contact was Schottky substrate contacts (Co salicide-P^- substrate). (b) Equivalent circuits.

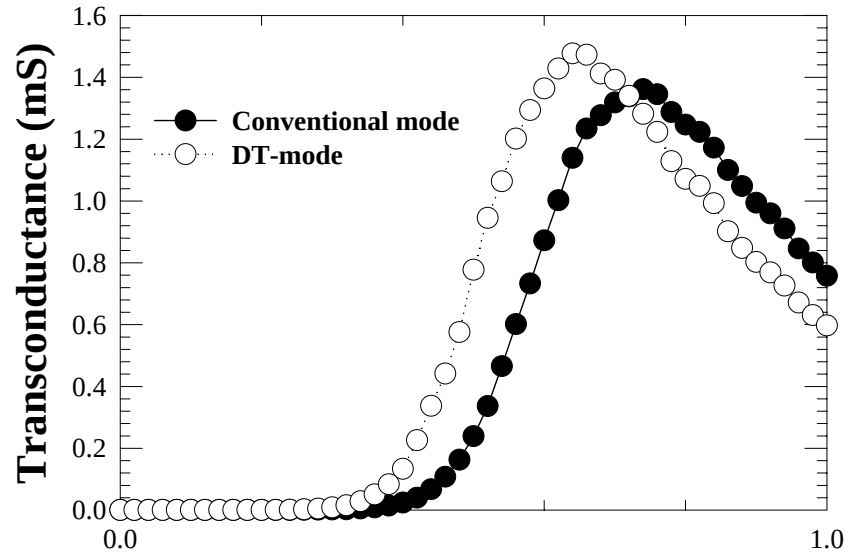


(a)

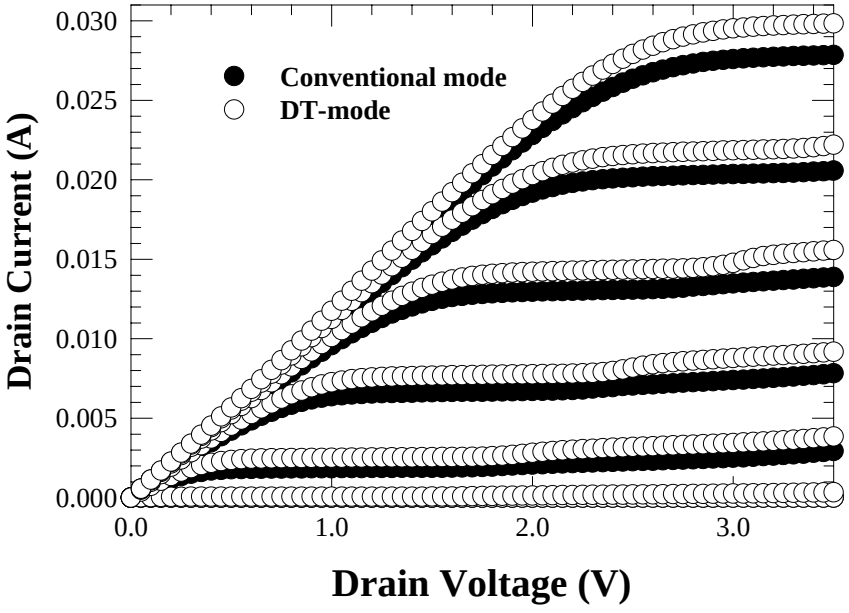


(b)

Fig. 4.2 (a) Drain current and transconductance versus gate voltage (b) drain current versus drain voltage, which gate length was equal to 0.8 μm with width equal to 100 μm for DT-mode without reverse Schottky barrier on substrate contact

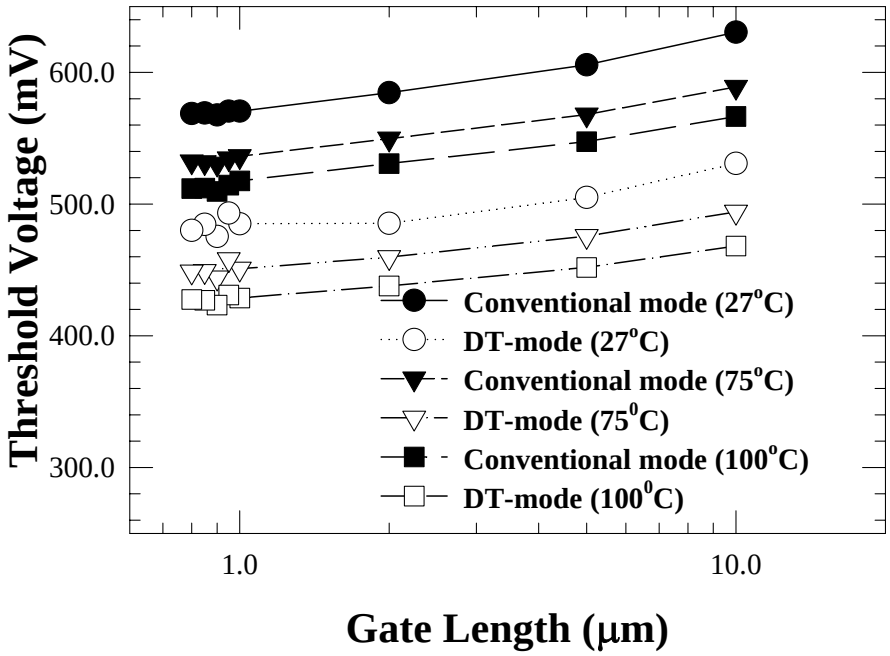


(a)

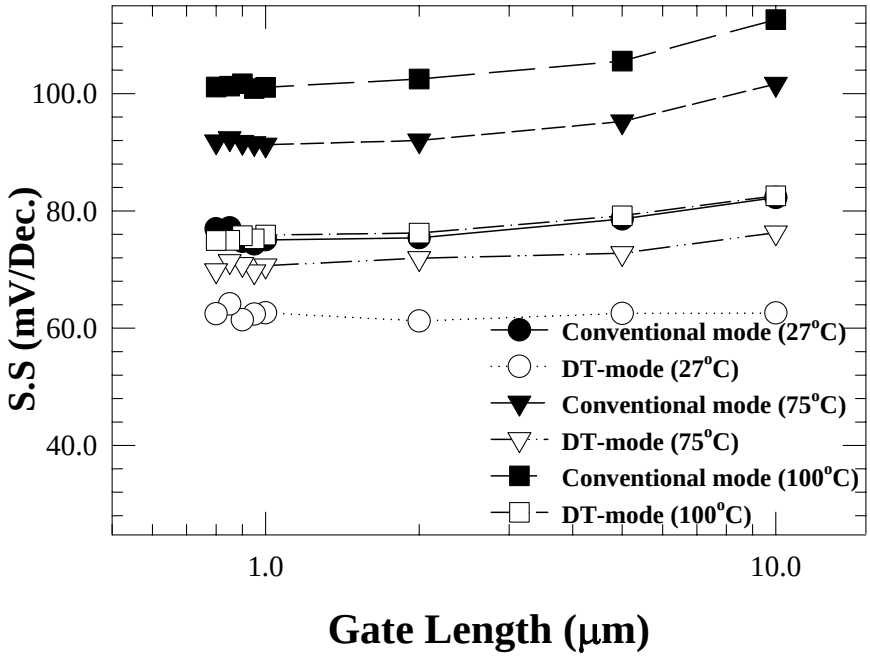


(b)

Fig. 4.3 Drain current versus drain voltage, which gate length was equal to 0.8 μm with width equal to 100 μm, (a) for DT-mode without reverse Schottky barrier on substrate contact, (b) DT-mode with reverse Schottky barrier on substrate contact and conventional modes at room temperature.



(a)



(b)

Fig.4.4 (a) Threshold voltage versus gate length under both the conventional and DT-mode for different temperatures. (b) S.S versus gate length under both the conventional and DT modes for different temperatures. The temperature was at 27 °C, 75 °C, and 100 °C.

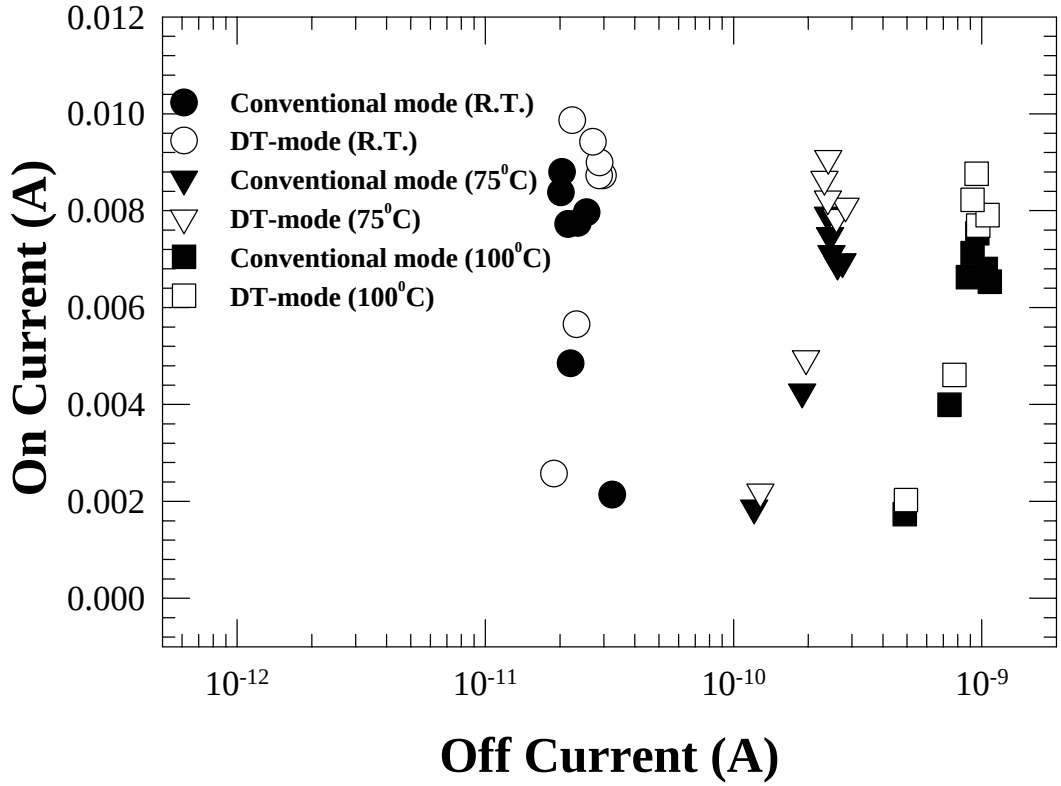


Fig.4.5 On-off current ratio under both the conventional and DT modes for different temperatures. The temperature was at 27 °C, 75 °C, and 100 °C, and the on-current was at V_G=V_D=1.8 V

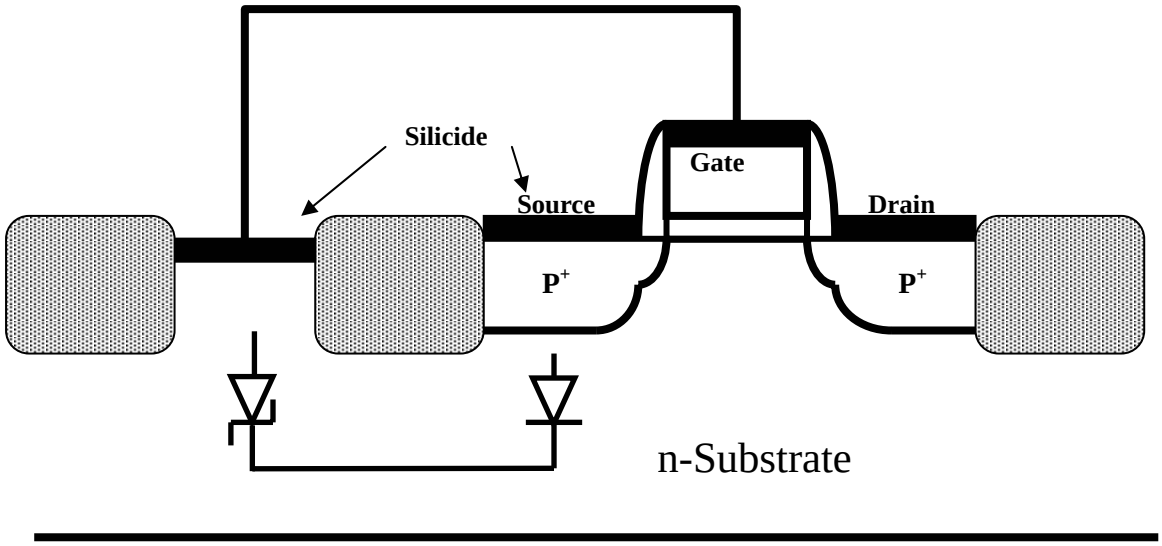
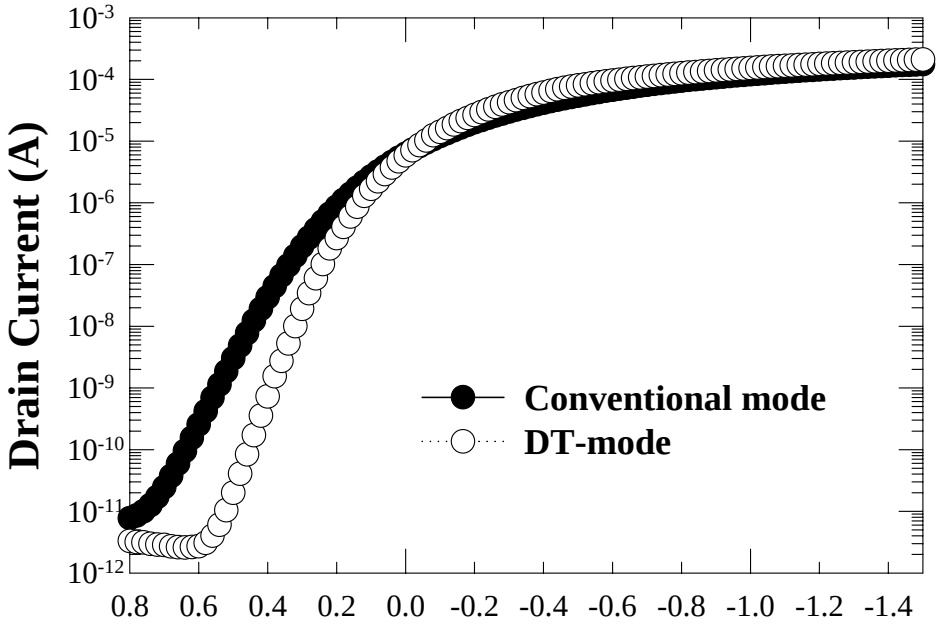
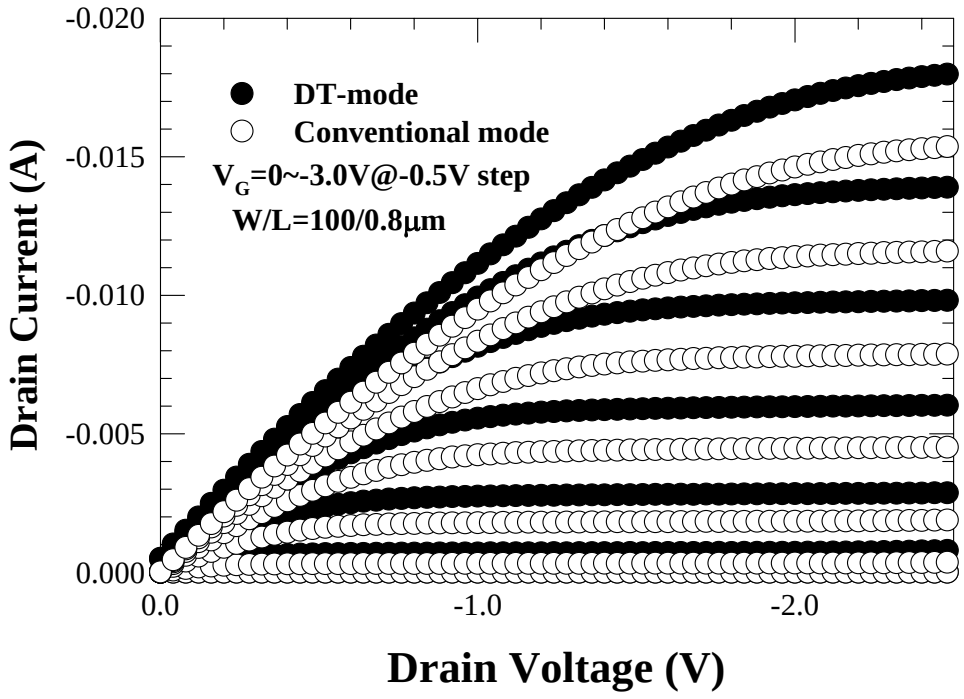


Fig 4.6 A cross section of the device and its equivalent circuit between source and substrate.

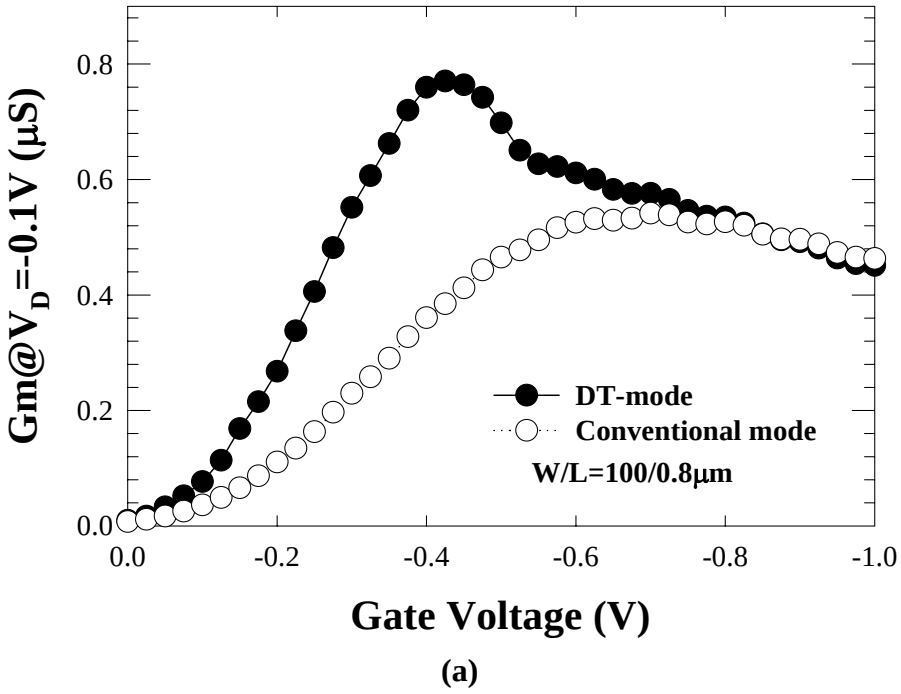


(a)

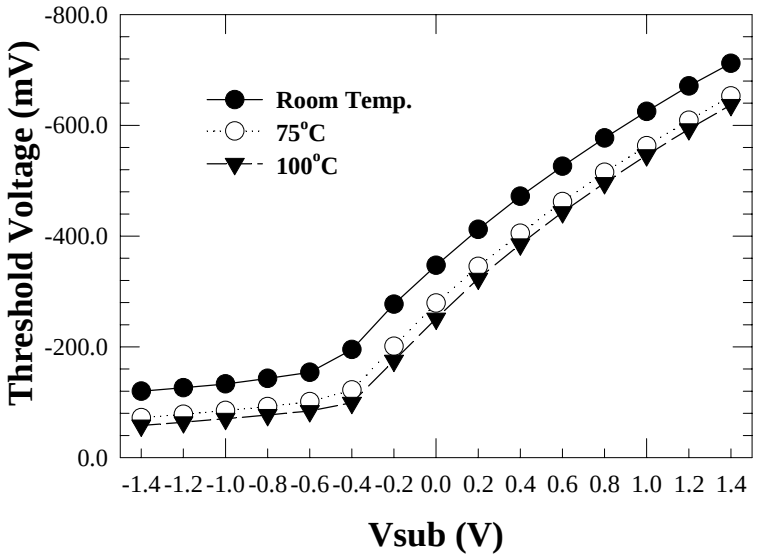


(b)

Fig 4.7 (a) Transfer characteristics, (b)Drain current versus drain voltage for both DT and conventional modes.



(a)



(b)

Fig 4.8 (a) Gate voltage versus transconductancefor both DT and conventional modes. (b) The threshold voltage versus substrate bias for different temperature (25 °C, 75 °C, and 100 °C).

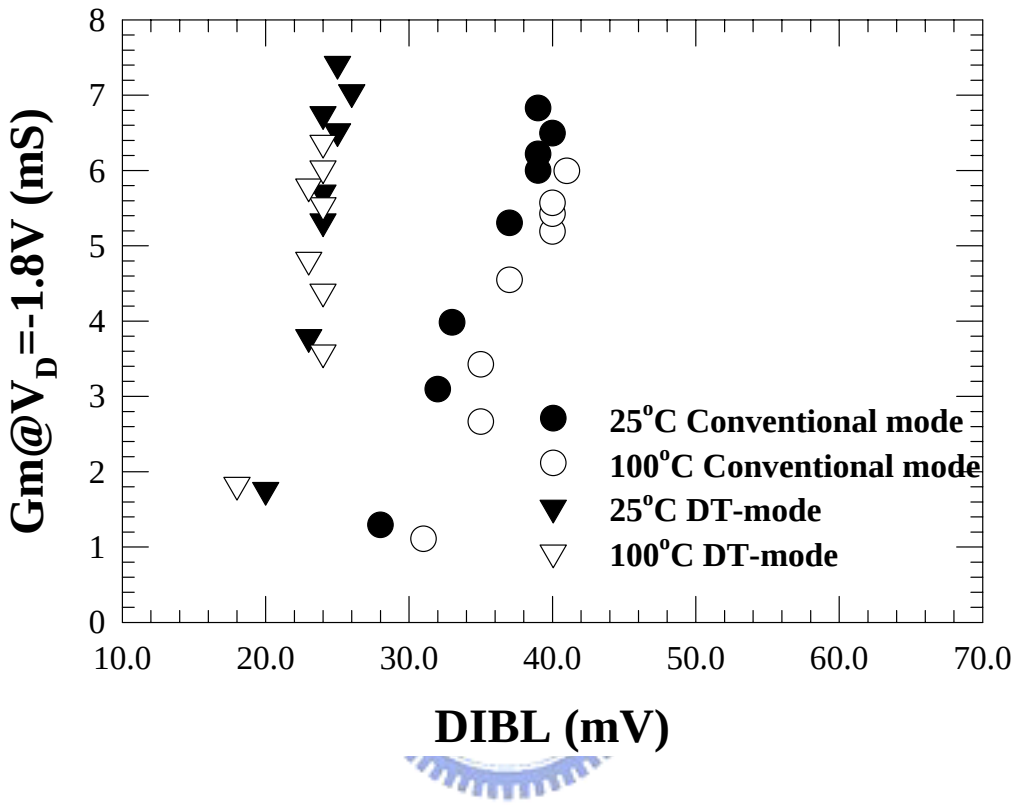
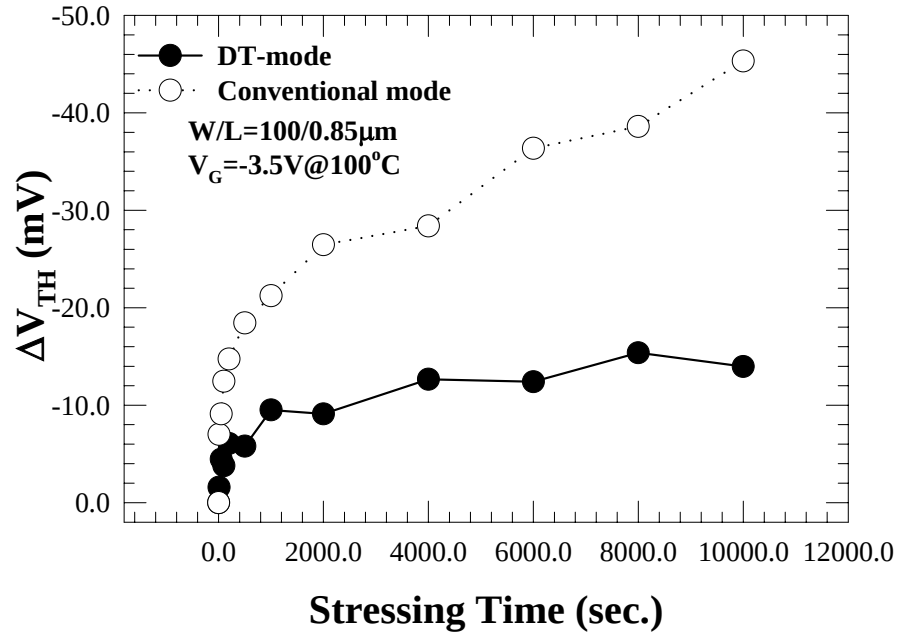
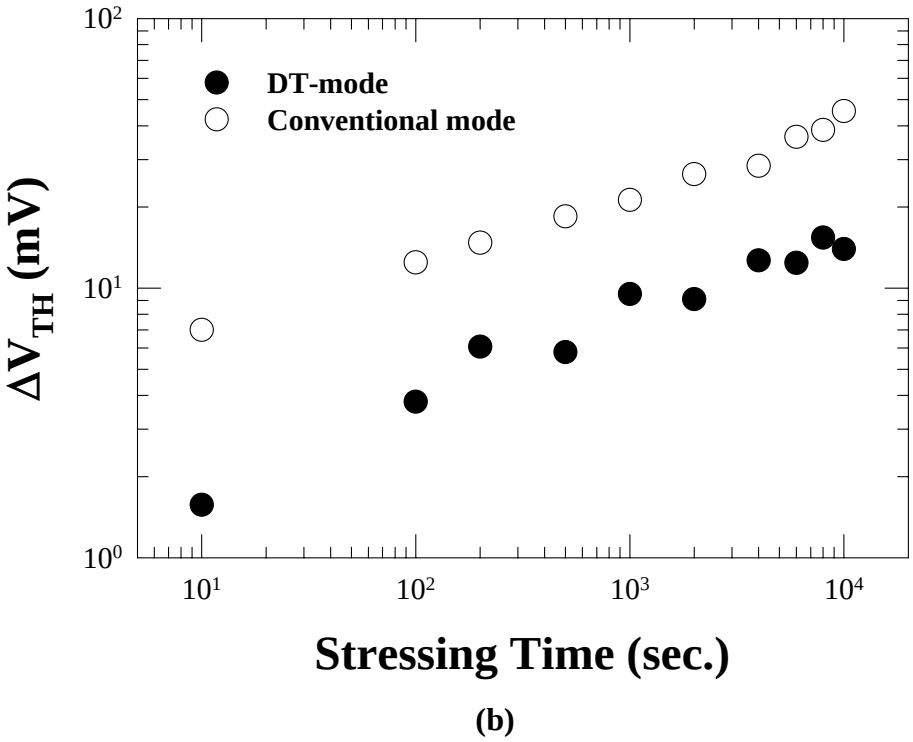


Fig 4.9 Saturation transconductance (V_D=-1.8 V) versus drain induced barrier lowering (DIBL) under different modes for different temperature (25 °C & 100 °C).



(a)



(b)

Fig 4.10 (a) Stress time dependence of threshold voltage degradation ($\Delta V_{TH}= V_{TH}(t)-V_{TH}(0)$) for pMOSFETs under different operation modes. The NBTI stressing was at V_G=-3.5 V and the other terminals were grounded. (b) Log-log scale for Fig 4.10(a).

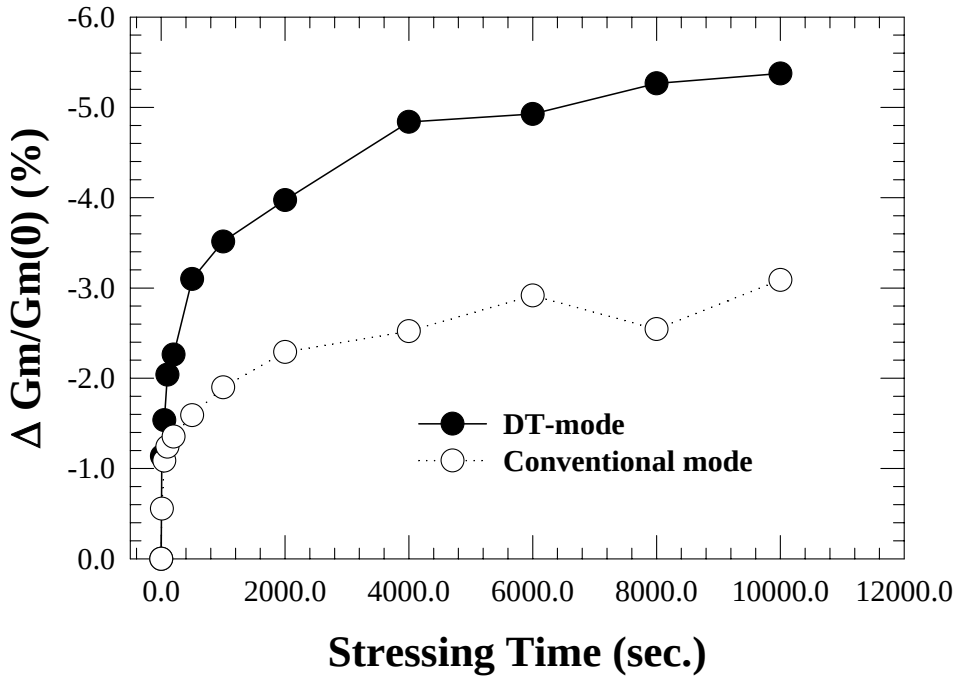


Fig 4.11 Stress time dependence of threshold voltage degradation (△Gm= Gm(t)-Gm(0)) for pMOSFETs under different operation modes. The NBTI stressing was at V_G=-3.5 V and the other terminals were grounded.