Appendix B

Crystal Orientation and Nitrogen Effects on the Carrier Mobility of pMOSFETs with Ultra-thin Gate Dielectrics

B.1. Background and Motivation

In the recent years, suppression of power consumption becomes more and more important than ever before for high-speed applications. Reduced supply voltage is one of the solutions to solve this problem. To maintain the increase of the driving current, gate oxide thickness has been scaled down the direct tunneling regime [A12]. Ultra-thin gate oxide thickness (1.5-2.0 nm) has been used for high-speed logic products. In addition, vertical or three-dimension (3D) MOSFETs with double or surrounded gate have been proposed for the next generation devices which could meet both high-speed and low power consumption requirements [A13-A16]. However, channels of the vertical or 3D-MOSFETs consist of different crystal orientations, which have been shown a significant impact on the electrical characteristics, especially for devices with ultra-thin gate oxide [A17-A18]. Nitrogen incorporation is also an important concern for the ultra-thin gate oxide preparation which exhibits advantages on the suppression of boron penetration and reduction of leakage current

[A19-A22]. It is well known that oxidation rate can be retarded with nitrogen incorporation in the substrates. Using this method, it is easy to grow multiple gate oxide thickness on the same wafer for the system-on-a-chip (SoC) application [A23]. However, the existence of nitrogen at the interface between the gate oxide and Si-substrate would degrade the transconductance at the lower electrical field compared to the pure O_2-grwon oxide [A24-A25]. In this paper, the crystal orientation and the nitrogen effects on pMOSFETs with ultra-thin gate dielectric has been investigated in detail. We found that electrical properties of pMOSFETs exhibit significant impact by the nitrogen incorporation at different dosages and also on different substrate orientation in terms of gate-oxide growth thickness, transconductance, geometry effects.

B.2 Device Fabrication

P-channel MOS transistors with channel length down to 0.8 μm were fabricated on 6-in (100) and (111)-oriented silicon wafers with resistivity of 15-20 Ω-cm using a conventional pMOSFET processes. Local oxidation of silicon (LOCOS) was used for the device's isolation. A BF_2 channel implant (at 80 keV, 1×10^{13} cm^{-2}) was used for V_{TH} adjustment of all transistors. Nitrogen implantation was executed on the substrate. The implantation energy was 15 keV, and the splits of dosage were w/o, 1×10^{13}, and 5×10^{14} cm^{-2}, respectively. Then, gate dielectric, thickness about 1.8 nm,

was grown in O_2 ambient by vertical furnace followed by a 200-nm poly-Si deposition. Shallow source/drain (S/D) extensions were formed by BF_2 implant at 8 keV to a dose of 1×10^{15} cm^{-2}. After the formation of TEOS sidewall spacer (200-nm), deep S/D junctions were formed by BF_2 implantation at 10 keV to a dose of 6×10^{15} cm^{-2}. Wafers were then annealed by a rapid thermal annealing (RTA) at 1000 °C for 10-sec. Finally, a 550-nm-thick TEOS by LPCVD was deposited and etched for contact holes. A Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete the contact metallization. Electrical characterizations were carried out with a HP4156 system, and the measurement temperature was set at room temperature, 75 °C, 125 °C, respectively.

B.3 Experimental Results and Discussion

B.3.1 Substrate orientation and nitrogen dosage effects:

Figure B.1(a) shows the effective gate-oxide thickness measured by the high frequency C-V method (1 MHz) versus different silicon substrate orientation and nitrogen implantation dosages. The effective gate-oxide thickness was deduced from the average of 25-capacitor on a 6-in wafers. It is found that the gate-oxide growth rate of Si-(111) by the vertical furnace was higher than that of Si-(100). The growth rate was retarded with the nitrogen incorporation for both Si-(100) and Si-(111). We found that the dependence of growth thickness on dosage of nitrogen of Si-(111) was

notable than that of Si-(100) due to Si-(111)'s high gate-oxide growth rate. Nitrogen dependence on the growth rate of Si-(100) substrate exhibits no significant difference for $1x10^{13}$ cm^{-2}, but decreases about 1.6 Å when nitrogen dosage increases to $5x10^{14}$ cm^{-2}. Threshold voltage, V_{TH}, versus different substrate orientations and nitrogen dosages are shown in Fig. B.1(b). The threshold voltage of both Si-(100) and Si-(111) was reduced about 180 mV as nitrogen dosage increases to 5×10^{14} cm^{-2}. The drain current versus drain voltage for different substrate orientation without nitrogen incorporation at the room temperature for pMOSFETs with W/L=10 μm/1 μm was shown in Fig. B.2. The gate voltage is from (Vg- V_{TH})= 0 V to -2 V in step of 0.5 V. It is found that the current of pMOSFETs on Si-(111) is about 42 % higher than that of Si-(100) splits as (Vg- V_{TH}) = -2 V. Since the driving current of pMOSFETs is dependent on the gate oxide thickness and carrier mobility, oxide thickness effect is eliminated from the deduced the mobility. The transconductance$\times T_{ox}$ versus (Vg-V_{TH}) for Si-(100) and Si-(111) without nitrogen incorporation was shown in Fig. B.3(a) and (b). A 64 % improvement was found for Si-(111) pMOSFETs as compared to that on Si-(100), as shown in Fig. B.3(a) for larger area devices, W/L=20 μm/20 μm, for the purpose of ignoring the edge effect. From this result, the carrier mobility of pMOSFETs with ultra-thin gate oxide on Si-(111) substrate shows excellent performance of improved carrier mobility. The same tendency (56 % increase) in

smaller area devices of pMOSFETs of W/L=10 μm/1 μm is also found as shown in Fig. B.3 (b). Reference [A17] only depicts 20% improved on Si-(111) pMOSFETs. One of the major concern of the device fabricated on the Si-(111) is the interfacial quality compared with that grown on Si-(100), since high interface density (D_{it}) will degrade the carrier mobility. Figure B.4 shows the interfacial charge Qss (deduced from $Icp_{,MAX}/f$) versus frequency on the log scale [A26]. The frequency was set from 800 kHz to 2 MHz. The slope deduced from Fig.4 was proportional to the value of D_{it}. It is noted that pMOSFETS on Si-(111) shows even a smaller slope than that of Si-(100) splits. This result implies that besides the mass of hole difference between Si-(100) and Si-(111), the less interfacial states of Si-(111) will contribute to the improved carrier mobility of pMOSFETs fabricated on it.

B.3.2 Impact of nitrogen and aspect ratio on carrier mobility

Figure B.5(a) shows the $G_m \times T_{ox}$ for pMOSFETs on Si-(100) with W/L= 10μm/1μm. It is found that the $G_m \times T_{ox}$ increases as the nitrogen dosage increases. A reverse phenomenon was found for Si-(111), as shown in Fig. B.5(b). It is clear that the $G_m \times T_{ox}$ of pMOSFETs on Si-(111) decreases as the nitrogen dosage increases. Different aspect rations are measured and shown in Fig. B.6 (a) and (b). For comparison, the device without any nitrogen incorporation is taken as the control

sample. Others pMOSFETs with nitrogen dosages on Si-(100) and Si-(111) are measured for different device aspect ratios (W/L). From Fig. B.6(a), it can be seen that $G_m \times T_{ox}$ increase as nitrogen dosage increases for all aspect rations. The same trend is found for pMOSFETs measured at elevated temperature at 125 °C, as shown in Fig. B.6(b). The pMOSFETs with the highest nitrogen dosage of 5×10^{14} cm^{-2} still shows highest $G_m \times T_{ox}$ than the control samples for all aspect ratios. This is totally different from that in nMOSFETs, in which nitrogen incorporation results in small $G_m \times T_{ox}$. [A24-A25] Therefore, instead of sacrificing on mobility, pMOSFETs with nitrogen incorporations on (100) wafers will benefit for carrier mobility. In addition, no crossover phenomenon was found from the transconductance behavior, which is frequently found for N_2O-oxynitride formed on nMOSFETs. [A24-A25]

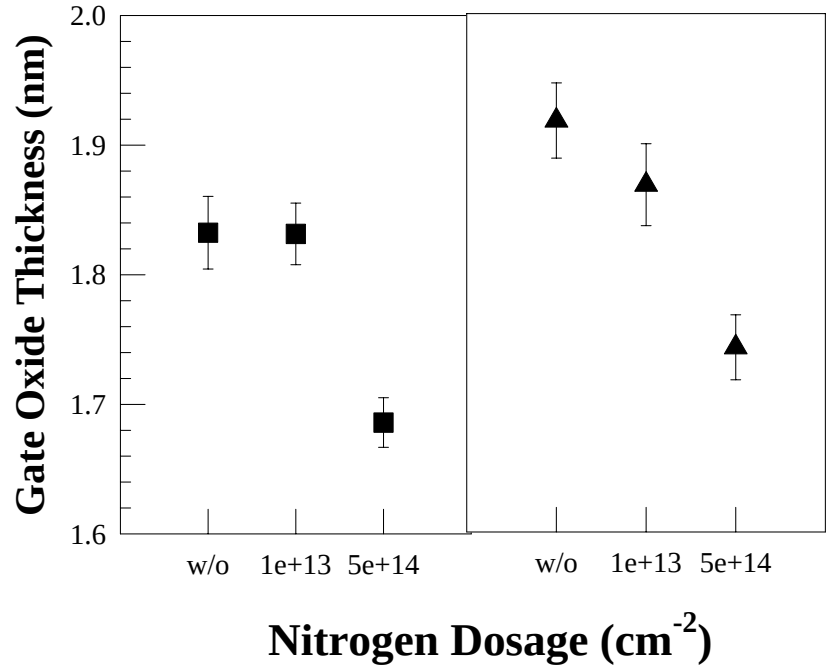
The aspect ratio effect for pMOSFETs on Si-(111) was shown in Fig. B.7 (a) and (b). On the contrast, serious degradation of mobility was found for all aspect ratios and different nitrogen dosage on Si-(111). It is noted that higher W/L ratio results in more degradation. As W = 10 μm, the degradation for different channel lengths L is 1μm > 2μm > 5 μm. As the W/L ratio decreases to W/L=1, such as 20/20 or 2/2, devices show less degradation. As temperature was increased to 125 °C, the degradation shows the same trend without significant dependence on W/L ratio, as shown in Fig. B.7 (b). The build-in strain of gate dielectric may be the major factor to

impact the carrier mobility [A27-A28], and nitrogen incorporation on different Si-orientations would cause two dimensional strain effects on channel region. Higher W/L ratio would cause unbalanced strain in channel, resulting in a more degradation of carrier mobility, as shown in Fig. B.8(a) and (b). As the nitrogen dosage increases from $1x10^{13}$ to $5x10^{14}$ cm^{-2}, the build-in strain increases. This increased strain with the unbalanced strain in X-Y axes results in the worse degradation for device with W/L = 10μm/1 μm of mobility as shown in Fig. B.7 (a) and B.7(b). Figure B.9 summaries the temperature effect on transconductance of pMOSFETs on Si-(100) and Si-(111) without the nitrogen incorporation. At elevated temperature at 125 °C, Si-(111) shows a larger degradation (2.5 %) than that of Si-(100) counterpart. The degradation ratio was obtained from the average of 10 devices. Therefore, as operated at high-temperature, pMOSFETs on Si-(111) have more sensitive behavior than those on Si-(100). The temperature effects of nitrogen incorporation for pMOSFETs on Si-(111) and Si-(100) were also measured and shown in Figure B.10(a) and (b). It is interesting that nitrogen incorporation don't play any role for temperature effects. This implies that interface scattering at elevated temperature is the still dominant factor.

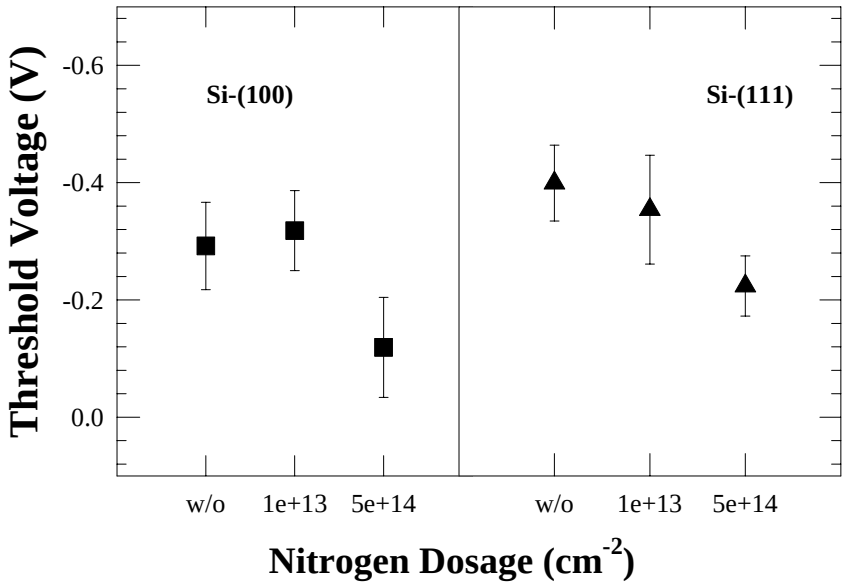
B.4 Summary

In this paper, the nitrogen dosage and temperature impacts on the mobility of

pMOSFETs on Si-(100) and Si-(111) with ultra-thin gate oxide were investigated in detail. The carrier mobility was improved up to 64% for pMOSFETs on Si-(111) than on Si-(100). We found that the nitrogen incorporation enhances the carrier mobility on Si-(100), but degrades on Si-(111). More over, compared to Si-(100), pMOSFETs on Si-(111) show a strong relation with aspect ration effect due to 2-dimensional strain effect. PMOSFETs with W/L close to 1 to eliminate this effect. Finally, pMOSFETs on Si-(111) show slightly large sensitive for temperature dependence, and nitrogen dosage shows no relationship.



(a)



(b)

Fig B.1 (a) Effective gate oxide thickness versus different orientation substrates and nitrogen incorporation dosage splits. In addition, the average gate oxide thickness was decided from 25 points. (b) The threshold voltage versus different orientation substrates and nitrogen incorporation dosage splits for the devices with W/L=10 μ m/1 μ m.

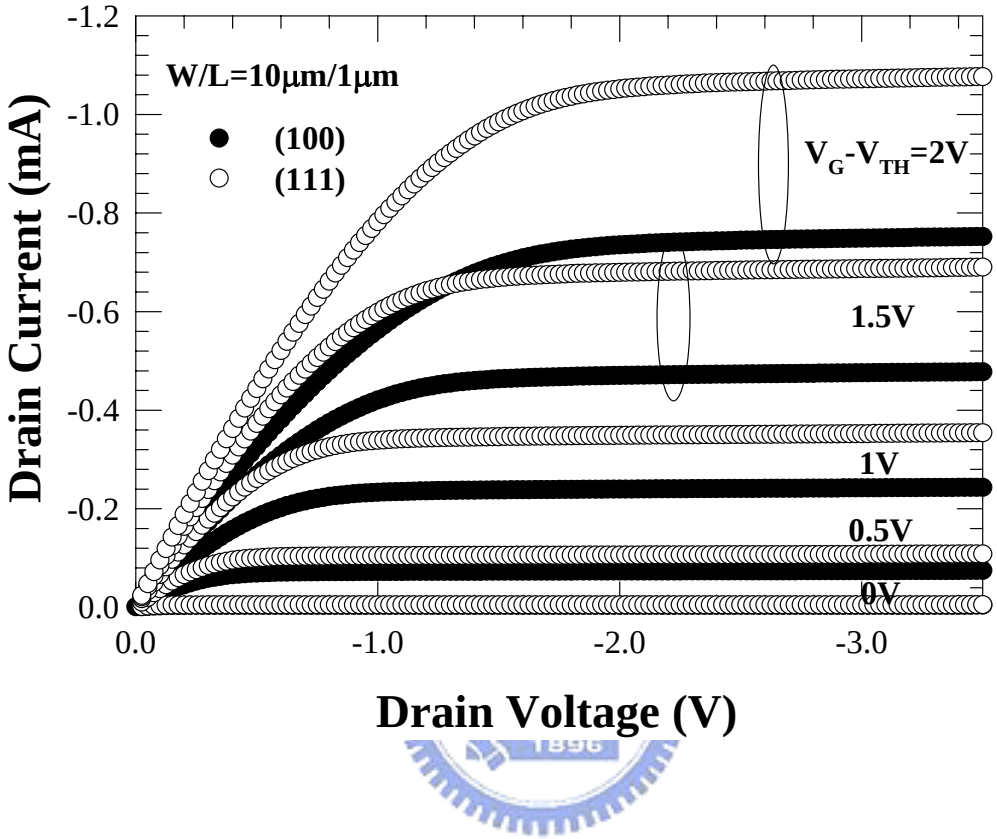
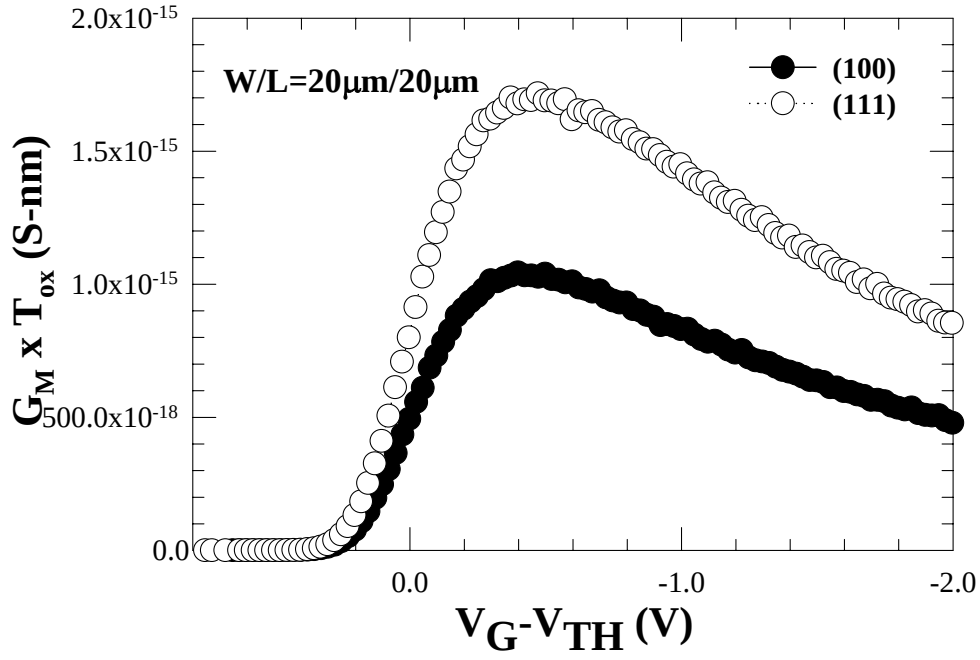
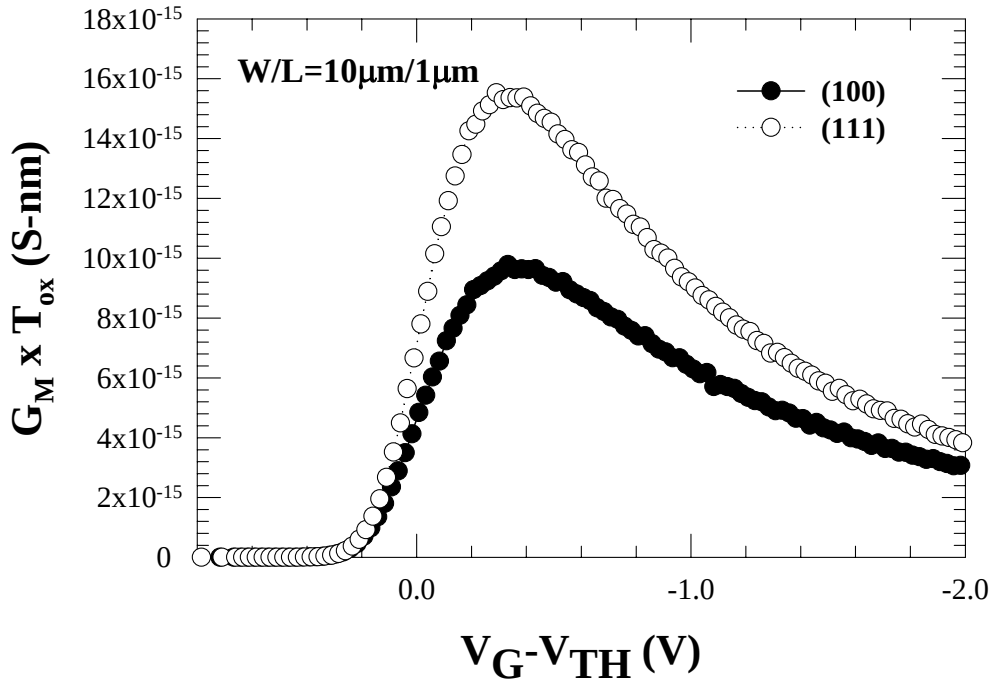


Fig. B.2 Drain current versus drain voltage for different orientation substrate wafers without nitrogen at room temperature for devices with W/L=10 μm/1 μm



(a)



(b)

Fig. B.3 (a) Transconductance × Tox versus (Vg-Vth) for different substrate orientation without nitrogen implantation for larger devices (W/L=20 μm/20 μm) (b) smaller devices (W/L=10 μm/1 μm)

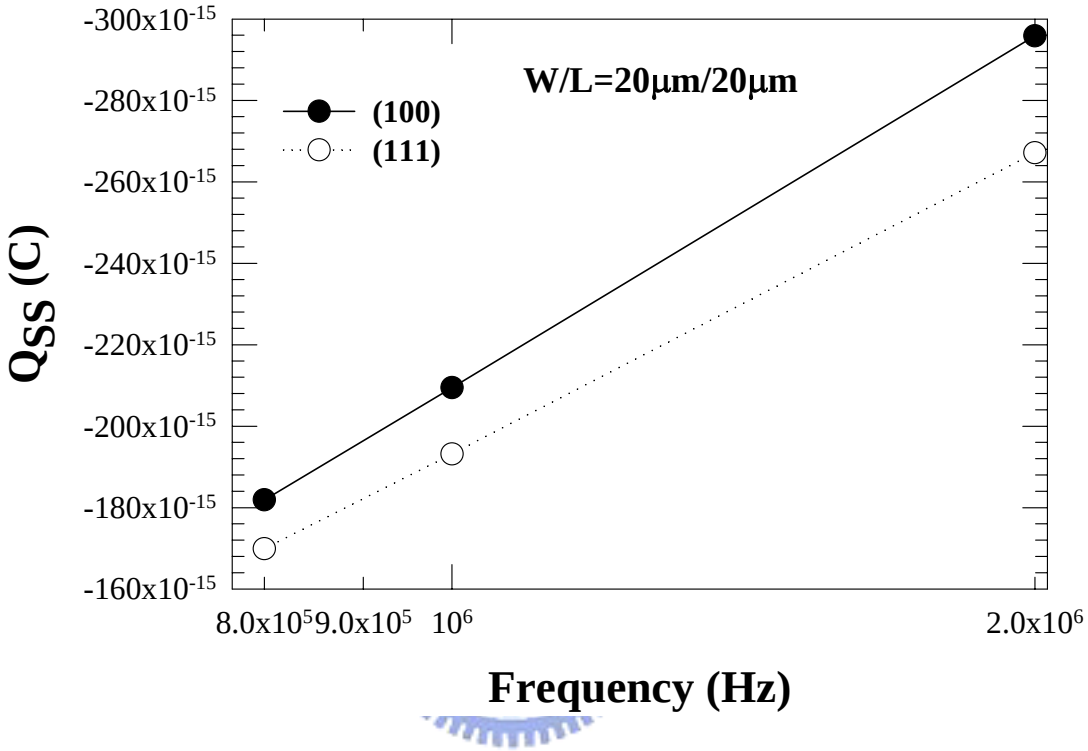
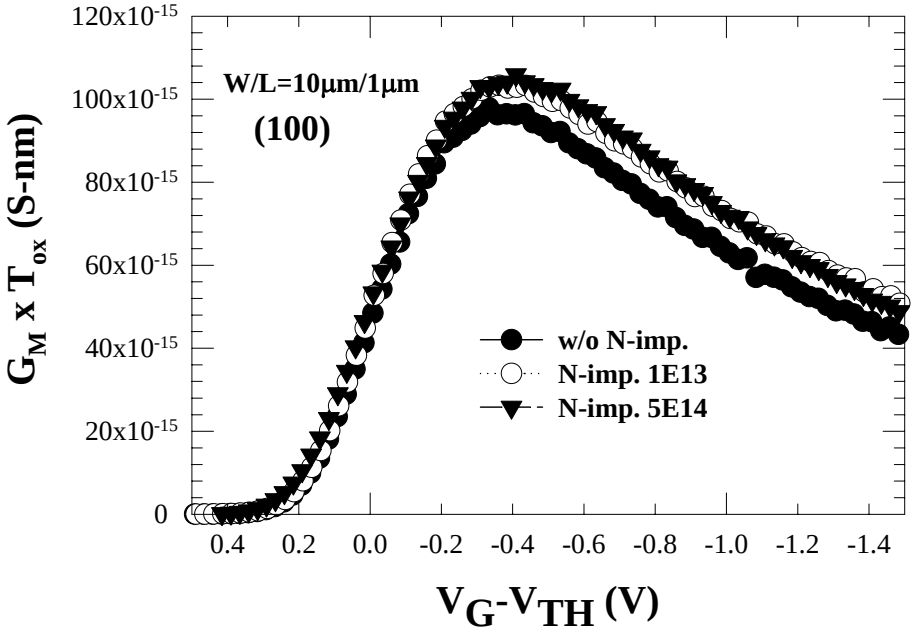
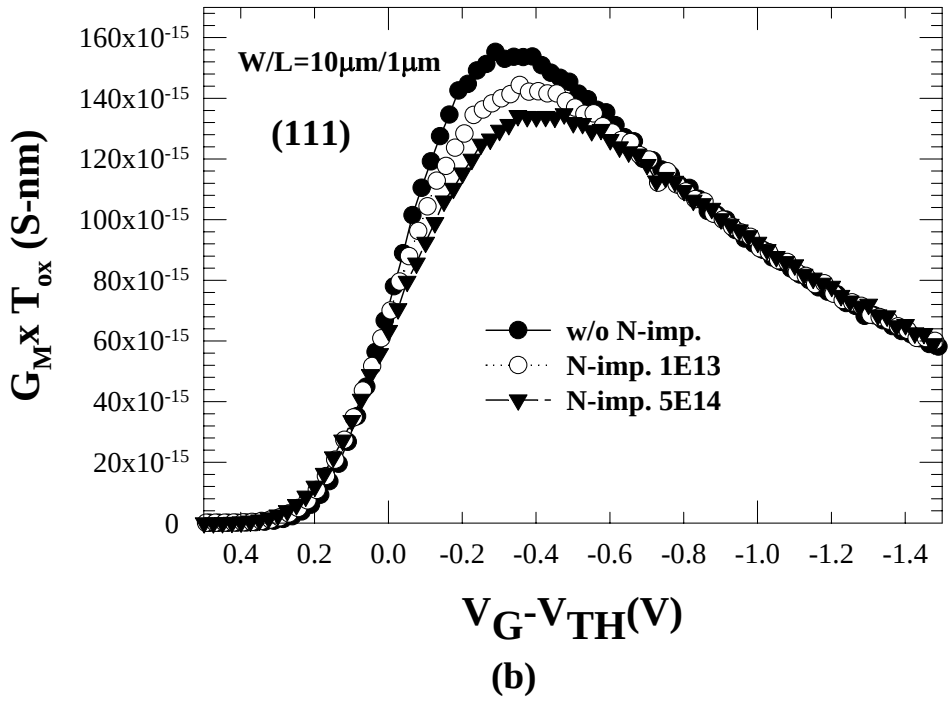


Fig. B.4 Qss ($Icp,_{MAX}$/f) versus frequency on log scale. The slope was proportional to the value of Dit.

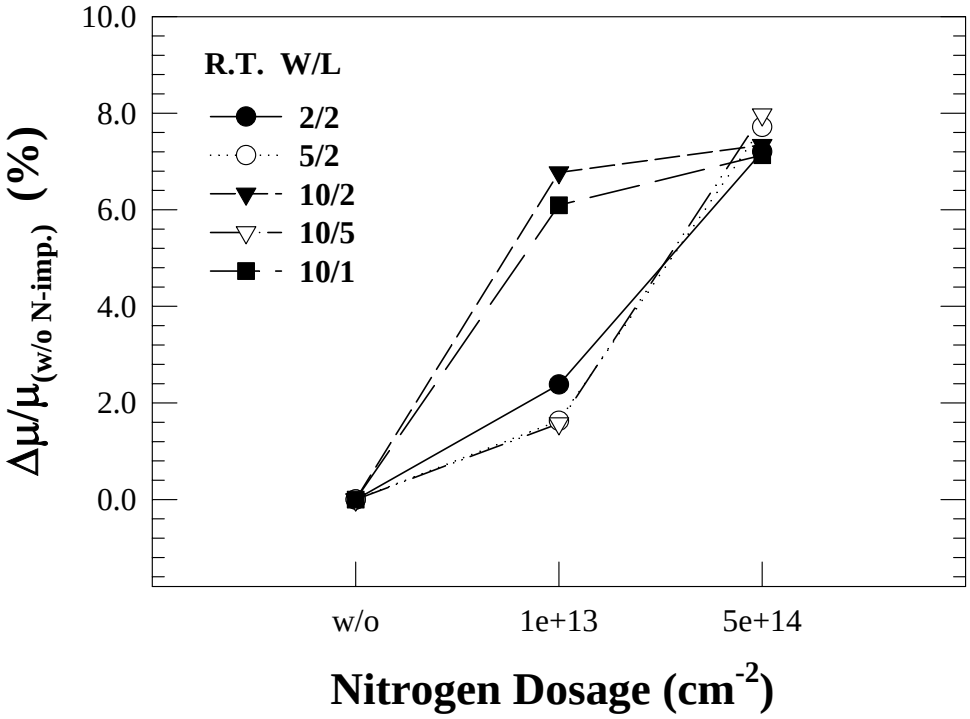


(a)

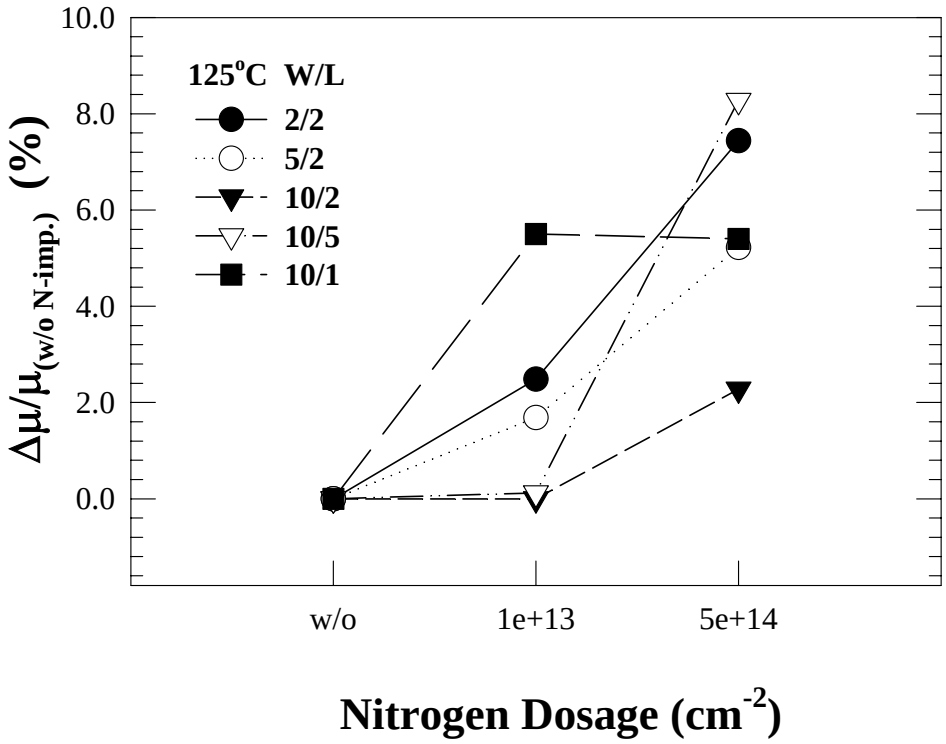


(b)

Fig. B.5 (a) $G_m \times T_{ox}$ for pMOSFETs on Si-(100) with different nitrogen dosage (W/L= 10μm/1μm) (b) Si-(111).

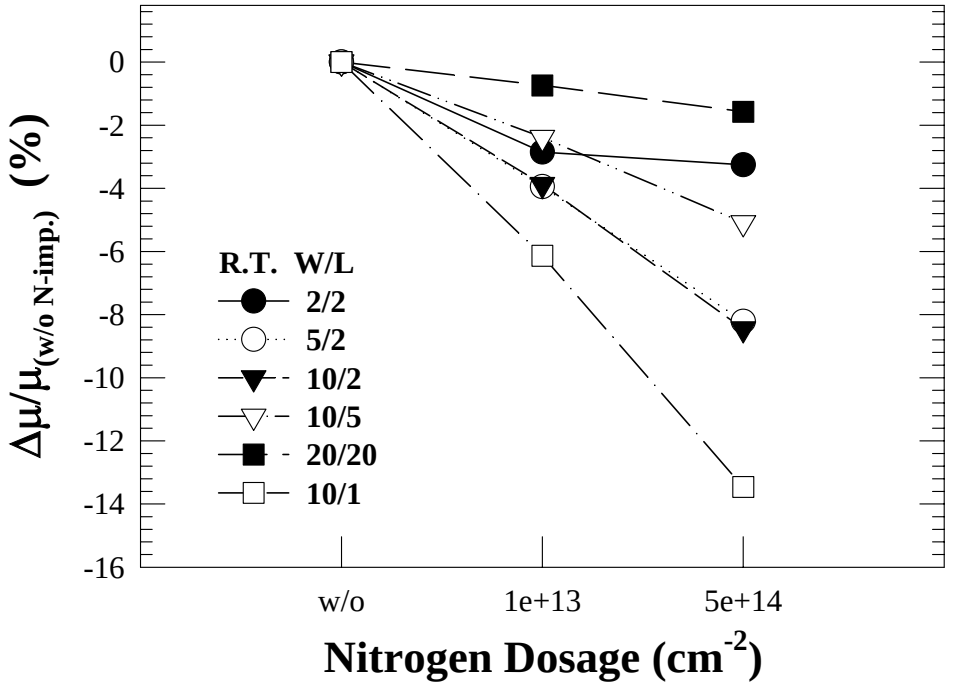


(a)

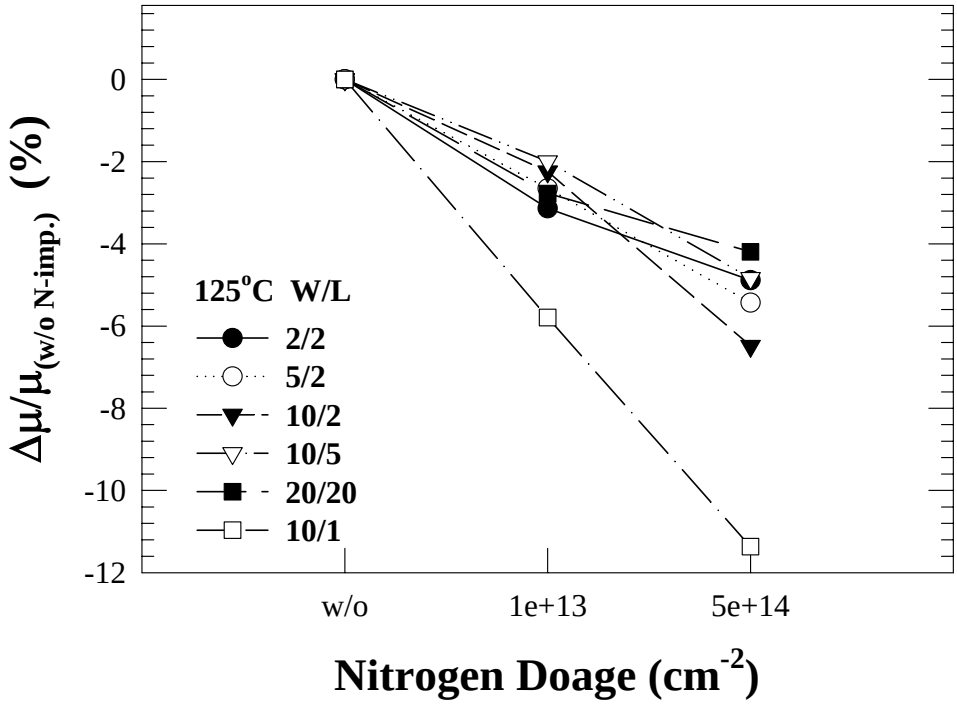


(b)

Fig. B.6 (a) (Gm×Tox for nitrogen incorporation splits minus control splits) versus different (100) splits for different device shape at room temperature (b) 125 °C

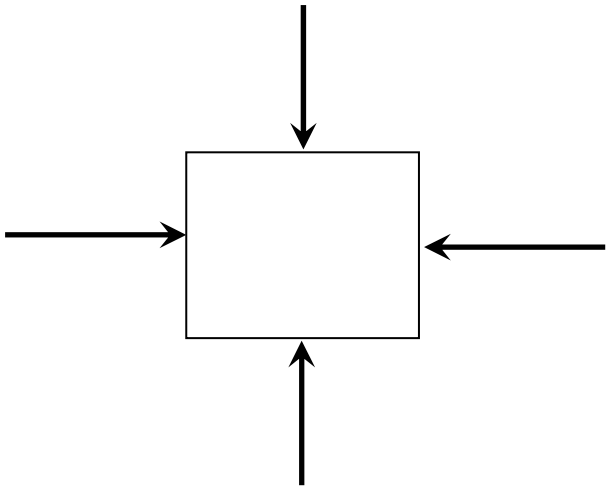


(a)

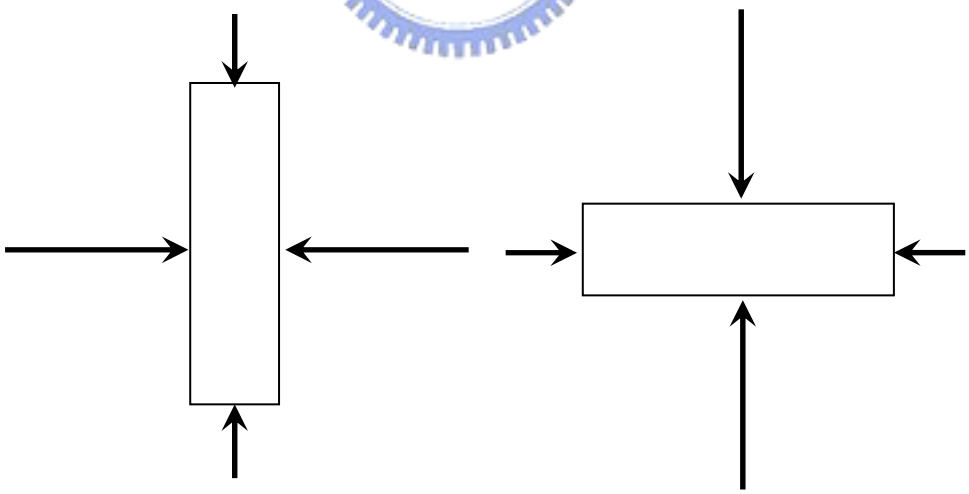


(b)

Fig. B.7 (a) (Gm×Tox for nitrogen incorporation splits minus control splits) versus different (111) splits for different device shape at room temperature (b) 125 °C



(a)



(b)

Fig. B.8 (a) The aspect ratio equal to 1, and the strain was balanced, (b) larger aspect ratio, which cause to serious degradation due to unbalanced strain.

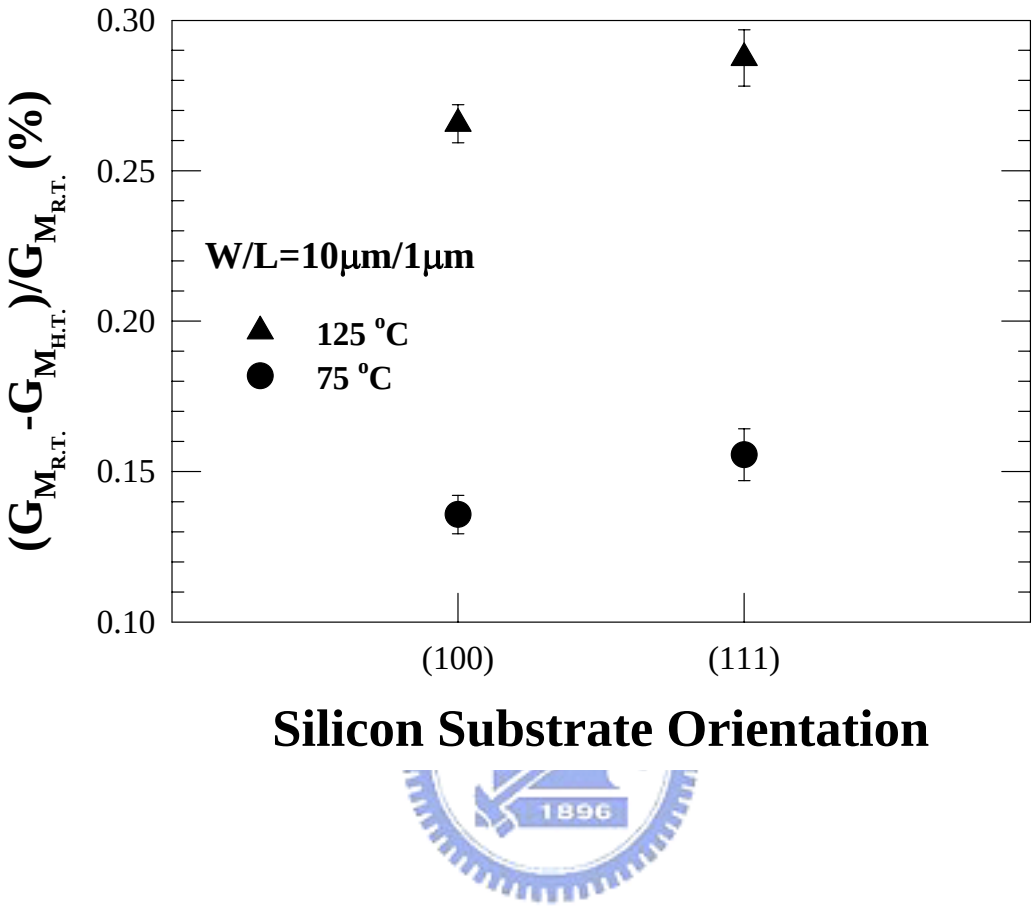
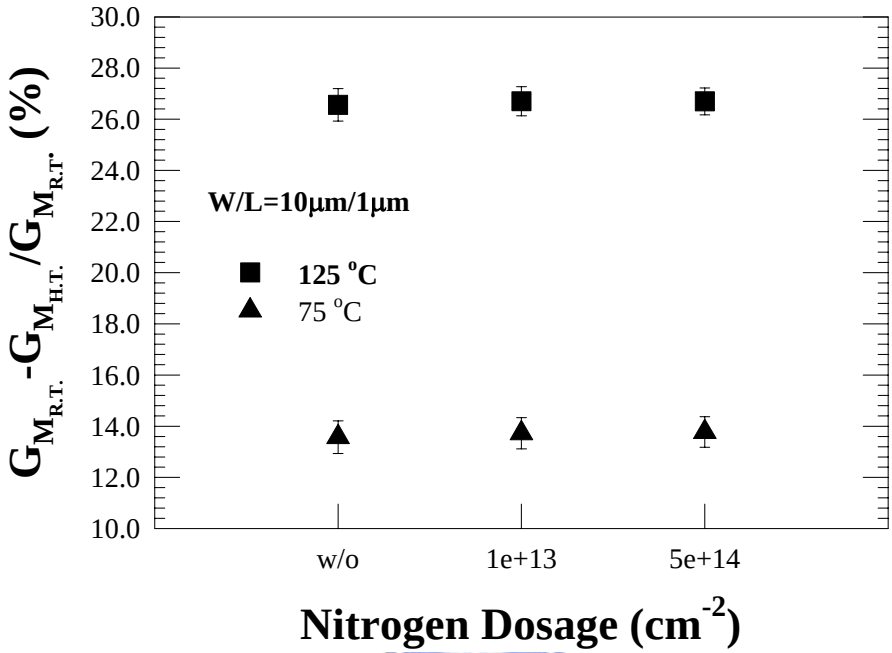
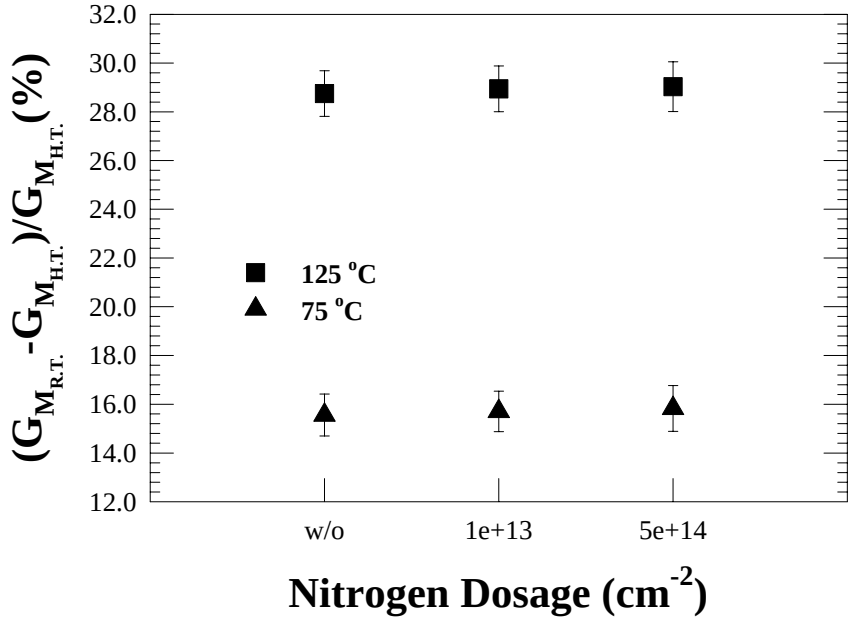


Fig. B.9 Temperature effects of transconductance between (100) and (111) splits (W/L=10 μ m/1 μ m)



(a)



(b)

Fig. B.10 Temperature effects of nitrogen incorporation for different orientation substrate (a) (100) splits (b) (111) splits (W/L=10 μ m/1 μ m)