Figure Captions

Chapter 2

Chapter 3

Fig. 3.4 Gate voltage versus transconductance for H-gate SOI pMOSFETs under normal modes with various substrate biases and also under DT-mode.

Fig. 3.5 Stress time dependence of on current (V_G=-0.7V, V_D=-0.7V) degradation for H-gate SOI pMOSFETs. Devices were stressed at $V_G=V_{TH}$, V_D=-4.5V, $\Delta I_{ON}/I_{ON}(0)= [I_{ON}(t)- I_{ON}(0)]/I_{ON}(0)$.

Fig. 3.6 Threshold voltage reduction ratio with respect to room temperature threshold voltage versus gate length for H-gate devices under both normal and DT modes at various temperatures. The gate length varies from 3.62 to 0.8 μm with width of 100 μm. $\Delta V_{TH}/V_{TH}$ (Room Temp.)= [V_{TH}(elevated temp.)- V_{TH}(room temp.)]/V_{TH}(room temp).

Fig. 3.7 Tansconductance versus gate voltage for H-gate SOI pMOSFETs with temperature varying from room temperature to 100℃.

Fig. 3.8 Tansconductance ratio between normal and DT-modes (left) and G_m/G_m (room temperature) for H-gate structures under normal and DT-modes (right) versus temperature.

Fig. 3.9 Stress time dependence of V_{TH} degradation for T-gate SOI pMOSFETs at various temperatures and operating under different modes. Devices were stressed at $V_G=V_{TH}$, V_D=-4.5V. the vertical log scale is ($\Delta V_{TH}= V_{TH}(t)- V_{TH}(0)$.

Chapter 4

Appendix A

implantation.)

Fig. A.3 (a) Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses implantation in (a) the channel and (b) the S/D extension. The stressing condition is 25℃, E_{OX}=15MV/cm. (N_2O oxide: 10kev, 5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}, and O_2 oxide: w/o implantation.)

Fig. A.4 (a) Qss (charge pumping current Icp/ frequency f) versus frequency for pMOSFETs with different nitrogen implant doses in (a) the channel and (b) the S/D wxrension region. (N_2O oxide, 10kev, 5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}, and O_2 oxide w/o implantation.)

Fig. A.5 The threshold voltage degradation for pMOSFETs with different well biases: V_{well}=0, 1, 2V, respectively. The stressing condition is 125 ℃, E_{OX}=13MV/cm. (N_2O oxide: 10kev, 5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}, and O_2 oxide: w/o implantation.)

Fig. A.6 (a) Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses (i.e., 5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}) in (a) the channel (b) and (b) the S/D extension. E_{OX}=13MV/cm for “high” state and V_G=1V for “ low” state. The temperature is kept at 125℃, , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.7 Stress time dependence of maximum charging current (L/W=10/100 μm) for pMOSFETs with different nitrogen implant doses (N_2O oxide: 5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}, and O_2 oxide: w/o implantation) in (a) the channel and (b) the source/drain extension. E_{OX}=13MV/cm for the "high" state and V_G=1V for the "low" state. The temperature is kept at 100℃, , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.8 Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses (N_2O oxide: 10kev, 5×10^{13} cm^{-2}, O_2 oxide: 10keV, 5×10^{13} cm^{-2}, respectively.) in (a) the channel and (b) the source/drain extension. The conditions of " high" state was for 125℃, E_{OX}=13MV/cm for the "high" state and V_G=1V for the "low" state. The temperature is kept at 125℃, and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.9 Stress time dependence of threshold voltage degradation for N_2O-oxide pMOSFETs with different nitrogen implant doses (5×10^{13}, 10^{14}, 5×10^{14} cm^{-2}) in (a) the channel and (b) the S/D extension. The conditions of " high" state ss for 125℃, E_{OX}=13MV/cm for the "high" state and E_{OX}=-13MV/cm for the "low" state. The temperature is kept at 125℃, , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Chapter 6

Fig. B.1 (a) Effective gate oxide thickness versus different orientation substrates and nitrogen incorporation dosage splits. In addition, the average gate oxide thickness was decided from 25 points. (b) The threshold voltage versus different orientation substrates and nitrogen incorporation dosage splits for the devices with W/L=10 μm/1 μm.

Fig. B.2 Drain current versus drain voltage for different orientation substrate wafers without nitrogen at room temperature for devices with W/L=10 μm/1 μm

Fig. B.3 (a) Transconductance × Tox versus (Vg-Vth) for different substrate orientation without nitrogen implantation for larger devices (W/L=20 μm/20 μm) (b) smaller devices (W/L=10 μm/1 μm)

Fig. B.4 Qss ($Icp_{,MAX}$/f) versus frequency on log scale. The slope was proportional to the value of Dit.

Fig. B.5 (a) $G_m \times T_{ox}$ for pMOSFETs on Si-(100) with different nitrogen dosage (W/L= 10μm/1μm) (b) Si-(111).

Fig. B.6 (a) (Gm×Tox for nitrogen incorporation splits minus control splits) versus different (100) splits for different device shape at room temperature (b) 125℃

Fig. B.7 (a) (Gm×Tox for nitrogen incorporation splits minus control splits) versus