

Figure Captions

Chapter 2

Fig. 2.1 Connections of MOSFET under DT mode, and split conditions of gate dielectrics.

Fig. 2.2 Threshold voltage versus gate length under both normal and DT modes for devices with thermal oxide. The oxide thickness is 4.1nm, and 6.2nm. The device width is $20 \mu\text{m}$.

Fig. 2.3 Subthreshold swing versus gate length under both normal and DT modes for devices with thermal oxide. The oxide thickness is 4.1nm, and 6.2nm. The device width is $20 \mu\text{m}$.

Fig. 2.4 Transfer characteristics for nMOSFETs under both normal (curve A) and DT (curve B) modes. The gate length is $0.57 \mu\text{m}$, while the gate dielectric is 6.2nm thermal oxide.

Fig. 2.5 Simulated subthreshold swing under DT-mode versus gate voltage with γ values varying from 0.2 to 1.2. The S.S. increases as gate voltage and γ value increase. (b) The subthreshold swing under DT-mode versus. gate voltage for distinct gate oxynitride thickness. Simulation of the S.S with different doping concentration (between $5\text{E}16 \text{ cm}^{-3}$ and $5\text{E}19 \text{ cm}^{-3}$) with different γ value versus. gate voltage V_g .

Fig. 2.6 Subthreshold swing versus gate length under both normal and DT modes.

The gate dielectric is grown by N₂O-oxynitride. The thickness is 2.0nm, 4.6nm, 6.1nm. The device width is 20 μ m.

Fig. 2.7 Normalized linear transconductance (i.e., the product of oxide thickness and linear transconductance) versus gate length under both normal and DT modes.

Fig. 2.8 Saturation transconductance versus drain-induced barrier lowering (DIBL) under both normal and DT modes. DIBL reduces dramatically under DT mode because of the narrower depletion width.

Chapter 3

Fig. 3.1 (a) Connections of SOI MOSFETs under DT mode, (b) T-gate structure, and (c) H-gate structure.



Fig. 3.2 Stress time dependence of V_{TH} degradation for SOI pMOSFETs at various temperatures and under both normal- and DT-modes for H-gate devices.

Devices were stressed at V_G=V_{TH}, V_D=-4.5V. The vertical log scale is

$$\Delta V_{TH} = V_{TH}(t) - V_{TH}(0).$$

Fig. 3.3 Stress time dependence of G_{mmax} degradation for SOI pMOSFETs at various temperatures and operating under both normal- and DT-modes for H-gate

devices. Devices were stressed at V_G=V_{TH}, V_D=-4.5V. The vertical log scale

$$\text{is } \Delta G_{mmax}(t)/G_{mmax}(0) = [G_{mmax}(t) - G_{mmax}(0)]/G_{mmax}(0) \text{ for } V_D = -0.1V.$$

Fig. 3.4 Gate voltage versus transconductance for H-gate SOI pMOSFETs under normal modes with various substrate biases and also under DT-mode.

Fig. 3.5 Stress time dependence of on current ($V_G=-0.7V$, $V_D=-0.7V$) degradation for H-gate SOI pMOSFETs. Devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$,

$$\Delta I_{ON}/I_{ON}(0) = [I_{ON}(t) - I_{ON}(0)]/I_{ON}(0).$$

Fig. 3.6 Threshold voltage reduction ratio with respect to room temperature threshold voltage versus gate length for H-gate devices under both normal and DT modes at various temperatures. The gate length varies from 3.62 to $0.8 \mu m$ with width of $100 \mu m$.
$$\Delta V_{TH}/V_{TH}(\text{Room Temp.}) = [V_{TH}(\text{elevated temp.}) - V_{TH}(\text{room temp.})]/V_{TH}(\text{room temp.}).$$

Fig. 3.7 Transconductance versus gate voltage for H-gate SOI pMOSFETs with temperature varying from room temperature to $100^\circ C$.

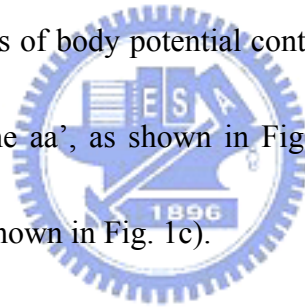
Fig. 3.8 Transconductance ratio between normal and DT-modes (left) and G_m/G_m (room temperature) for H-gate structures under normal and DT-modes (right) versus temperature.

Fig. 3.9 Stress time dependence of V_{TH} degradation for T-gate SOI pMOSFETs at various temperatures and operating under different modes. Devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$. the vertical log scale is $(\Delta V_{TH} = V_{TH}(t) - V_{TH}(0))$.

Fig. 3.10 Stress time dependence of G_{mmax} degradation for T-gate SOI pMOSFETs at various temperatures and operating under different modes. Devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$. The vertical log scale is $G_{mmax}(t)/G_{mmax}(0)=[G_{mmax}(t)-G_{mmax}(0)]/G_{mmax}(0)$ for $V_D=-0.1V$.

Fig. 3.11 Stress time dependence of drive current (measured at $V_G=-0.7V$, $V_D=-0.7V$) degradation for T-gate SOI pMOSFETs under both normal- and DT-modes. Devices were stressed at $V_G=V_{TH}$, $V_D=-4.5V$, $\Delta I_{ON}/I_{ON}(0)=[I_{ON}(t)-I_{ON}(0)]/I_{ON}(0)$.

Fig. 3.12 (a) Simulation results of body potential contour distribution under DT mode for T-gate (along line aa', as shown in Fig. 1b), and (b) H-gate structures (along line bb', as shown in Fig. 1c).



Chapter 4

Fig. 4.1 (a) Connections of MOSFET under the DT mode, and the reverse substrate contact was Schottky substrate contacts (Co salicide-P⁻ substrate). (b) Equivalent circuits.

Fig. 4.2 (a) Drain current and transconductance versus gate voltage (b) drain current versus drain voltage, which gate length was equal to $0.8 \mu m$ with width equal to $100 \mu m$ for DT-mode without reverse Schottky barrier on substrate contact

Fig. 4.3 (a) Connections of MOSFET under the DT mode, and the reverse substrate contact was Schottky substrate contacts (Co salicide-P⁻ substrate). (b) Equivalent circuits.

Fig. 4.4 Drain current versus drain voltage, which gate length was equal to $0.8 \mu\text{m}$ with width equal to $100 \mu\text{m}$, (a) for DT-mode without reverse Schottky barrier on substrate contact, (b) DT-mode with reverse Schottky barrier on substrate contact and conventional modes at room temperature.

Fig. 4.5 (a) Threshold voltage versus gate length under both the conventional and DT mode for different temperatures. (b) Subthreshold slope versus gate length under both the conventional and DT modes for different temperatures. The temperature was at 27°C , 75°C , and 100°C .

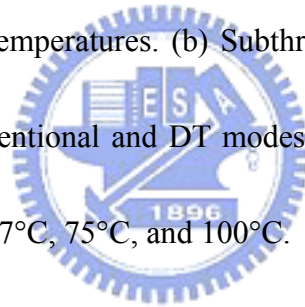


Fig. 4.6 On-off current ratio under both the conventional and DT modes for different temperatures. The temperature was at 27°C , 75°C , and 100°C , and the on-current was at $V_G=V_D=1.8\text{V}$

Fig. 4.7 4.6 A cross section of the device and its equivalent circuit between source and substrate.

Fig. 4.8 (a) Transfer characteristics, (b) Drain current versus drain voltage for both DT and conventional modes.

Fig. 4.9 (a) Gate voltage versus transconductance for both DT and conventional

modes. (b) The threshold voltage versus substrate bias for different temperature (25, 75, and 100°C).

Fig. 4.10 Saturation transconductance ($V_D=-1.8V$) versus drain induced barrier lowering (DIBL) under different modes for different temperature (25 °C & 100 °C).

Fig. 4.11 (a) Stress time dependence of threshold voltage degradation ($\Delta V_{TH}= V_{TH}(t)-V_{TH}(0)$) for pMOSFETs under different operation modes. The NBTI stressing was at $V_G=-3.5V$ and the other terminals were grounded. (b) Log-log scale for Fig 4.10(a).

Fig. 4.12 Stress time dependence of threshold voltage degradation ($\Delta G_m= G_m(t)-G_m(0)$) for pMOSFETs under different operation modes. The NBTI stressing was at $V_G=-3.5V$ and the other terminals were grounded.

Appendix A

Fig. A.1 Schematics for NBTI stress setup. Both substrate and well electrodes are grounded.

Fig. A.2 Stress time dependence of threshold voltage degradation for various pMOSFETs that received different nitrogen implant doses in (a) the channel and (b) the S/D extension. The stressing condition is 125°C, $E_{OX}=13MV/cm$. (N_2O oxide: 10keV, 5×10^{13} , 10^{14} , 5×10^{14} cm⁻², and O_2 oxide: w/o

implantation.)

Fig. A.3 (a) Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses implantation in (a) the channel and (b) the S/D extension. The stressing condition is 25°C , $E_{\text{OX}}=15\text{MV/cm}$. (N_2O oxide: 10keV , 5×10^{13} , 10^{14} , $5\times 10^{14}\text{ cm}^{-2}$, and O_2 oxide: w/o implantation.)

Fig. A.4 (a) Qss (charge pumping current I_{cp} / frequency f) versus frequency for pMOSFETs with different nitrogen implant doses in (a) the channel and (b) the S/D extension region. (N_2O oxide, 10keV , 5×10^{13} , 10^{14} , $5\times 10^{14}\text{ cm}^{-2}$, and O_2 oxide w/o implantation.)

Fig. A.5 The threshold voltage degradation for pMOSFETs with different well biases: $V_{\text{well}}=0, 1, 2\text{V}$, respectively. The stressing condition is 125°C , $E_{\text{OX}}=13\text{MV/cm}$. (N_2O oxide: 10keV , 5×10^{13} , 10^{14} , $5\times 10^{14}\text{ cm}^{-2}$, and O_2 oxide: w/o implantation.)

Fig. A.6 (a) Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses (i.e., 5×10^{13} , 10^{14} , $5\times 10^{14}\text{ cm}^{-2}$) in (a) the channel (b) and (b) the S/D extension. $E_{\text{OX}}=13\text{MV/cm}$ for “high” state and $V_{\text{G}}=1\text{V}$ for “low” state. The temperature is kept at 125°C , , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.7 Stress time dependence of maximum charging current ($L/W=10/100 \mu\text{m}$) for pMOSFETs with different nitrogen implant doses (N_2O oxide: 5×10^{13} , 10^{14} , $5 \times 10^{14} \text{ cm}^{-2}$, and O_2 oxide: w/o implantation) in (a) the channel and (b) the source/drain extension. $E_{\text{OX}}=13\text{MV/cm}$ for the “high” state and $V_G=1\text{V}$ for the “low” state. The temperature is kept at 100°C , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.8 Stress time dependence of threshold voltage degradation for pMOSFETs with different nitrogen implant doses (N_2O oxide: 10keV , $5 \times 10^{13} \text{ cm}^{-2}$, O_2 oxide: 10keV , $5 \times 10^{13} \text{ cm}^{-2}$, respectively.) in (a) the channel and (b) the source/drain extension. The conditions of “high” state was for 125°C , $E_{\text{OX}}=13\text{MV/cm}$ for the “high” state and $V_G=1\text{V}$ for the “low” state. The temperature is kept at 125°C , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Fig. A.9 Stress time dependence of threshold voltage degradation for N_2O -oxide pMOSFETs with different nitrogen implant doses (5×10^{13} , 10^{14} , $5 \times 10^{14} \text{ cm}^{-2}$) in (a) the channel and (b) the S/D extension. The conditions of “high” state ss for 125°C , $E_{\text{OX}}=13\text{MV/cm}$ for the “high” state and $E_{\text{OX}}=-13\text{MV/cm}$ for the “low” state. The temperature is kept at 125°C , and all other terminals (source, drain, well, and substrate) are grounded under both conditions.

Chapter 6

Fig. B.1 (a) Effective gate oxide thickness versus different orientation substrates and nitrogen incorporation dosage splits. In addition, the average gate oxide thickness was decided from 25 points. (b) The threshold voltage versus different orientation substrates and nitrogen incorporation dosage splits for the devices with $W/L=10 \mu\text{m}/1 \mu\text{m}$.

Fig. B.2 Drain current versus drain voltage for different orientation substrate wafers without nitrogen at room temperature for devices with $W/L=10 \mu\text{m}/1 \mu\text{m}$

Fig. B.3 (a) $G_m \times T_{ox}$ versus $(V_g - V_{th})$ for different substrate orientation without nitrogen implantation for larger devices ($W/L=20 \mu\text{m}/20 \mu\text{m}$) (b) smaller devices ($W/L=10 \mu\text{m}/1 \mu\text{m}$)

Fig. B.4 $Q_{SS} (I_{cp,MAX}/f)$ versus frequency on log scale. The slope was proportional to the value of D_{it} .

Fig. B.5 (a) $G_m \times T_{ox}$ for pMOSFETs on Si-(100) with different nitrogen dosage ($W/L=10 \mu\text{m}/1 \mu\text{m}$) (b) Si-(111).

Fig. B.6 (a) ($G_m \times T_{ox}$ for nitrogen incorporation splits minus control splits) versus different (100) splits for different device shape at room temperature (b) 125°C

Fig. B.7 (a) ($G_m \times T_{ox}$ for nitrogen incorporation splits minus control splits) versus

different (111) splits for different device shape at room temperature (b)
125°C

Fig. B.8 (a) The aspect ratio equal to 1, and the strain was balanced, (b) larger aspect ratio, which cause to serious degradation due to unbalanced strain.

Fig. B.9 Temperature effects of transconductance between (100) and (111) splits
(W/L=10 μ m/1 μ m)

Fig. B.10 Temperature effects of nitrogen incorporation for different orientation substrate (a) (100) splits (b) (111) splits (W/L=10 μ m/1 μ m)

