Chapter 1

Introduction

1.1 General Background

In recent years two distinct approaches, one targeting low power consumption and the other high performance, have been evolved regarding voltage scaling. The low-power-consumption approach is intended for battery-operated applications, such as laptop and notebook computers as well as personal communication systems. While the high-performance approach is appropriate for applications such as microprocessors. The reduction of power consumption is most crucial for the extended lifetime of batteries, prolonging mobile operation of portable systems. An effective method of lowering the system power consumption is to reduce the supply voltage. This is because the power consumption in Complementary Metal Oxide Silicon (CMOS) digital circuits is dependent on the square law of power supply voltage as

$$P=C_L V_{dd}^2 f_d, \qquad (1)$$

where P is the power consumed by the gate, C_L is the total switching capacitance of the gate, V_{dd} is the power supply voltage, and f_d is the average operating frequency of the gate. As a general rule of thumb, the power supply voltage should be at least three times the threshold voltage [1]. Since a low supply voltage will result in drive current

reduction and circuit speed degradation, scaling of the power supply voltage must be accompanied by threshold voltage reduction.

Assaderaghi et al.[2-4] have proposed a dynamic threshold voltage Metal Oxide Silicon (DTMOS) using a Separation by IMplantation of OXygen (SIMOX) wafer for lower power supply voltage applications. By shorting the gate to the body, the threshold voltage (V_{TH}) operating under the Dynamic Threshold (DT) mode is reduced by forward biasing of the body, so its current drive can be significantly enhanced in the on state. Since the device exhibits the normal V_{TH} in the off state (because V_G=V_{BS}=0), low standby power consumption is maintained. The DT-MOSFETs scheme thus appears to be very promising for future low-power and high-speed circuit applications, since it improves the circuit speed without compromising the standby power consumption. In addition, the DT-MOSFETs fabrication was more suitable on the partially-depletion SOI wafers than that on the bulk wafers due to its lower parasitic junction capacitance. However, due to the formation of device's isolation, the different gate structures of SOI devices, such as H-gate [5] and T-gate [6] structures were proposed for DT-mode operation. Therefore, first, we will discuss the effects of dielectric type and thickness on the characteristics of DT-MOSFETs. Then, the hot carrier effects of DT-MOSFETs with different gate structures at different temperature were also discussed in this dissertation. On the

other hand, PN diode between substrate and source would turn on as gate/substrate bias larger than 0.7 V for DT-MOSFETs. Considerably large leakage current due to the turn-on diode current between substrate and source terminals would restrict the operation voltage of DTMOS. Schottky barrier contact [7-9] formation on the substrate contact for DT-mode operation was also discussed in this dissertation.

In addition, the Negative Bias Temperature Instability (NBTI) has become one of the serious reliability concerns for deep sub-micron PMOS transistor. There are still no reports about the effects of NBTI under DT-pMOSFETs operation. This is because the gate voltage of DT-pMOSFETs must be less than -0.7V to prevent the turn-on diode behavior between gate and substrate terminals. We will discuss the characteristics of NBTI effects under DTMOS operation.

1.2 Organization of the Dissertation

This dissertation is divided into seven chapters

In Chapter 2, a comprehensive comparison of nMOSFETs with different gate dielectrics of various thicknesses that operate under the DT mode as well as the conventional mode is discussed. Formula and simulation results were proposed to explain the value of threshold voltage under DT-mode operation with different gate dielectrics of various thickness, the characteristics of subthreshold swing, and

transconductance.

In Chapter 3, we report hot carrier degradations on SOI pMOSFETs at various temperatures operating under both conventional and DT-modes. Then, we will discuss the characteristics of the threshold voltage shift, and transconductance degradations. In addition, different gate structures were also discussed in Chapter 3.

In Chapter 4, DT-MOSFETs with reverse Schottky substrate contacts for high voltage, temperature applications and NBTI effects were discussed simultaneously. The transconductance still depicted larger value under DT-mode operation than that under conventional operation, and the value of subthreshold swing was close the ideal value at different temperatures. Furthermore, NBTI effects of DT-pMOSFETs with reverse Schottky substrate contacts were also discussed for the first time, due to its high voltage applications of this novel structures. The degradation results of the threshold voltage and transconductance depicted contrast results, where the degradation value of the threshold voltage was low and that of transconductance was high for DT-mode operation.

Finally, a summary of the results in this dissertation and suggestions for future work are given in Chapter 5.