Chapter 2

The Effects of Dielectric Type and Thickness on the Characteristics of Dynamic Threshold Metal Oxide Semiconductor Transistors

2.1 Background and Motivation

DT-MOSFETs were used for the lower power supply voltage applications. By shorting the gate to the body, the threshold voltage operating under the DT-mode is reduced by forward biasing of the body, so its current drive can be significantly enhanced in the on state. In addition, the subthreshold slope could attain to the ideal value (~60mV/dec.) To enhance the drive current under DT-mode, large body factor, γ ($\equiv \frac{\Delta V_{TH}}{\Delta V_{BS}}$), is necessary to increase the threshold voltage reduction. The γ value was strongly depended on the ratio of gate oxide thickness to channel depletion layer width. Gate oxide thickness is known to be an important device parameter in dictating the threshold voltage and current drive under the conventional mode (i.e., non-DTMOS mode) operation. However, a previous report has also pointed out that the influence of the body-effect factor, γ, would significantly decrease with the substrate bias [4].

In this chapter, a comprehensive comparison of nMOSFETs with different gate

dielectrics of various thicknesses that operate under the DT-mode as well as the conventional mode is discussed. The two types of gate dielectrics are oxide grown in O_2 (denoted as O_2-oxide) and oxide-grown in N_2O (denoted as N_2O-oxynitride, or oxynitride for short). A model is proposed to explain the drain current in the subthreshold region. From the model and numerical analyses, additional insights into why the subthreshold swing (*S.S.*) of DTMOS can be as low as the ideal case, i.e., ~ 60 mV/dec are revealed.

2.2 Device Fabrication

N-channel MOSFETs with channel length down to 0.18μm were fabricated on 6 in p-type silicon wafers with a resistivity of 15-20 Ω-cm by a conventional nMOSFET process. Local oxidation of silicon (LOCOS) was used for device isolation. A BF_2 channel implant (at 90 keV and 1×10^{13} cm^{-2}) was used for threshold voltage, $V_{TH,}$ adjustment. Anti-punch-through implantation was also performed to prevent bulk punch-through by boron ions at 45 keV at a dose of 1×10^{12} cm^{-2}. Wafers were then split to grow gate oxides of various thicknesses in either O_2 or N_2O ambient. Specifically, the thickness splits for O_2-oxide were 4.1 nm, and 6.1 nm; while the thickness splits were 2.0 nm, 4.6 nm, 6.2 nm for N_2O-oxynitride. It should be noted here that gate dielectrics were grown using a conventional horizontal furnace, except

for 2.0nm-thickness split for N_2O-oxynitride that was grown by a vertical furnace. Next, a polysilicon (poly-Si) layer with a thickness of 200 nm was deposited by low pressure chemical vapor deposition (LPCVD). The poly-Si layer was then patterned and etched to define a 0.18μm gate length. Shallow S/D extensions were formed by As^+ implantation (at 4 keV, 1×10^{14} cm^{-2}). After the formation of TEOS sidewall spacer (200nm), deep source/drain junctions were formed by As^+ implantation at 20 keV at a dose of 1×10^{15} cm^{-2}. Finally, wafers were annealed by a rapid thermal process (RTP) at 1050 °C for 20 sec. for dopant activation. Afterwards, a 550 nm TEOS layer was deposited and etched for contact holes. Finally, a Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations were performed using a HP4156 system.

2.3 Experimental Results and Discussion

2.3.1. Characteristics of devices with different gate oxide thickness

Figure 2.1 shows the electrical connection under DTMOS operation, where the gate and substrate are shorted together during measurements. In contrast, the gate and substrate are not electrically connected under the conventional mode operation (denoted as Con in the figures). The effects of oxide thickness on the threshold voltage as a function of gate length for transistors under both the DT and conventional

modes are shown in Fig. 2.2. The gate oxide thicknesses are 4.1 and 6.2 nm respectively, while the nominal transistor gate length varies from 1.15 to 0.22 μm, with a fixed device width of 20 μm. The threshold voltage V_{TH} is derived from the maximum transconductance (Gm_{max}) method at V_D=0.1 V. For simplicity, by assuming a constant channel doping concentration N_A, V_{TH} can be expressed as:

$$V_{TH} = V_{FB} + 2 \cdot \phi_{FB} + \gamma \sqrt{2 \cdot \phi_{FB} + V_{BS}} \qquad (2)$$

and $\gamma \equiv C_{ox}^{-1} \sqrt{2 \cdot q \cdot \varepsilon_s \cdot N_A}$

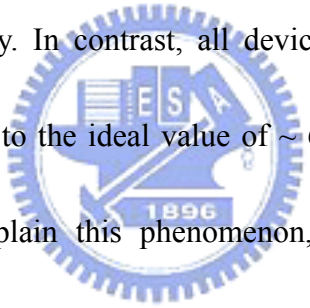
$$\phi_{FB} = \left(\frac{KT}{q} \right) \times \ln \left(\frac{N_A}{N_i} \right),$$

where V_{TH} is threshold voltage, V_{FB} is flat band voltage, ϕ_{FB} is the potential difference between the Fermi level and the intrinsic level of the bulk semiconductor, C_{OX} is the gate oxide capacitance, γ is the body-effect factor, N_A is the channel doping concentration, *Ni* is the intrinsic concentration, and V_{BS} is the substrate bias.

As shown in Fig. 2.2, the magnitude of V_{TH} operating under the conventional mode varies with gate oxide thickness. A thicker gate oxide leads to a larger V_{TH} due to a larger γ value, as predicted by eq. 2. However, an interesting phenomenon is observed in Fig.2.2 for devices operating under the DT mode. Specifically, all devices depict V_{TH} values of ~0.7 V, independent of the oxide thickness. This can be explained as follows: When the substrate is tied to the gate under DT mode, the term V_{BS} in eq. (2) equals $-\alpha V_G$, where α is a dimensionless factor that depends on the substrate

contact resistance and doping profile. Ideally, when there is negligible resistive voltage drop, α approaches 1. As V_G increases, V_{TH} decreases by a magnitude of $\gamma\sqrt{2\cdot\phi_{FP}-\alpha V_G}$. V_{TH} now equals $V_{TH}=V_{FB}+2\cdot\phi_{FP}$ as $2\cdot\phi_{FP}=\alpha V_G$. Under this condition, the influence of γ would be negligible. As a result, the V_{TH} under DT mode is essentially independent of gate oxide thickness.

Figure 2.3 shows the plot for *S.S.* versus gate length, *Lg*, for samples with different gate oxide thicknesses. It can be seen that under the conventional mode, a larger *S.S.* value is observed for devices with thicker gate oxides, as expected with its weaker gate control capability. In contrast, all devices under the DT mode depict similar *S.S.* values, i.e., close to the ideal value of ~ 60 mV/dec, independent of the gate oxide thickness. To explain this phenomenon, *S.S.* under the DT mode is simulated as shown in the next section.



2.3.2. Simulation of subthreshold swing under the DT-mode

Since the equations of drain current and *S.S.* are respectively [10]

$$I_D=\mu_n\left(\frac{W}{L}\right)\left(\frac{KT}{q}\right)^2 C_D(\phi_S)e^{q(V_G-V_{TH})/nKT}\left(\frac{n}{m}\right)\left[1-e^{-(qmV_{DS}/nKT)}\right] \quad (3)$$

$$S.S.\equiv\left(\frac{\partial\log I_D}{\partial V_G}\right)^{-1}=\frac{kT}{q}\times\ln 10\times n \quad (4)$$

$$C_D(\phi_S)=\left(\gamma\cdot\frac{C_{OX}}{2}\right)/\sqrt{\phi_S-\frac{KT}{q}} \quad (5)$$

$$n \equiv 1 + \frac{C_D}{C_{OX}} + \frac{C_{it}}{C_{OX}}$$

and $m \equiv 1 + \frac{C_D}{C_{OX}}$,

where C_D is the depletion layer capacitance; $C_{it} = qD_{it}$, where D_{it} is the interface-trap density, and ψ_S is the surface potential in the subthreshold region.

From eq. (3), one can see that the drain current in the subthreshold region is exponentially dependent on V_G, while V_{TH} is constant under the conventional mode. This relationship is shown in curve *A* of Fig. 2.4. In contrast, the drain current in the subthreshold region under the DT mode, i.e., curve B in Fig. 2.4, increases even more significantly with gate voltage, compared to that under the conventional mode. This is because the threshold voltage in eq. (3) decreases with increasing V_G. Therefore, the *S.S.* (which is proportional to the inverse slope in Fig. 2.4) decreases quickly under DT-mode operation.

Equation (4) represents the subthreshold swing, and is equal to $n \times \frac{kT}{q} \times \ln 10$ under the conventional mode. Under the DT mode, forward biasing the substrate decreases the depletion width [11], which increases the capacitance of the depletion layer, C_D. So, ψ_S in eq. (5) must be replaced by $\psi_S - \alpha V_G$ to account for the change in C_D. The *S.S.* under the DT mode now becomes

$$S.S. \equiv \left(\frac{\partial \log I_D}{\partial V_G} \right)^{-1} = \frac{kT}{q} \times \ln 10 \times n(V_G) / \left[1 - \left(\frac{\partial V_{TH}}{\partial V_G} \right) \right]. \qquad (6)$$

It is noted that n is now a function of V_G. From Eq. (2), and by substituting V_{BS}

by-αV_G, $\partial V_{TH} / \partial V_G$ becomes

$$\frac{\partial V_{TH}}{\partial V_G} = -\left(\gamma \frac{\alpha}{2}\right) / \sqrt{2 \cdot \phi_{FP} - \alpha V_G} \,. \tag{7}$$

The result in eq. (7) is negative. From the measured results, we found that its magnitude approaches C_D / C_{OX}. This explains why subthreshold swing significantly decreases to the ideal value of $KT/q \times \ln 10$. To make this point even more clear, we have performed simulation of the subthreshold swing. We assume that the channel doping concentration is 10^{18} cm^{-3}, and α is equal to 1. By neglecting the C_{it} effect, *S.S.* values versus gate voltage (which is varied from 0 to 0.7 V), with γ as a parameter (which is varied from 0.2 to 1.2) is calculated using eqs. (5)-(7). The results are shown in Fig. 2.5(a) which clearly shows that although S.S. increases as gate voltage increases under the DT mode, although increases as gate voltage increases, is still less than 62 mV/dec even when gate voltage reaches 0.65 V. It can also be seen that a large γ value leads to a larger S.S., due to a thicker oxide thickness as mentioned above. The experimental results were in Fig. 2.5(b), the trend was the same as the Fig. 2.5(a). Next, the S.S for different doping concentration will be discussed. The gate oxide was defined at 7.0nm, and the range of doping concentration was from 5×16 cm^{-3} to 5×19 cm^{-3}. From eq. (5), the devices with larger surface doping concentration would have larger depletion layer capacitance. Forward bias would cause smaller surface potential, and then decrease the depletion width W with increasing C_D. So, in

the condition with fixed forward bias, the S.S of devices with larger surface doping concentration would larger than that with smaller doping concentration. But, the devices in DT-mode mean that the threshold voltage V_{TH} is a variable, the term $\left[1-\left(\frac{\partial V_{TH}}{\partial V_G}\right)\right]$ in the denominator is also very important. The devices with larger surface doping concentration also have larger value, and increase rapidly than that with smaller doping concentration for increasing substrate bias. The most interesting is the ratio of $\left(1+\frac{C_D}{C_{OX}}\right)\left[1-\left(\frac{\partial V_{TH}}{\partial V_G}\right)\right]$ in Fig. 2.5(c)

2.3.3. Characteristics of N_2O-oxynitride versus O_2-oxide

The threshold voltage versus gate length plots for different N_2O-oxynitride thicknesses are shown in Fig. 2.6. The N_2O-oxynitride thicknesses are 2.0 nm, 4.1 nm, and 6.2 nm. The gate length varies from 1.15 μm to 0.22 μm, all with the same device width of 20 μm. As expected, the threshold voltage operating under the conventional mode depends on the oxynitride thickness. Compared to the O_2-oxide counterparts, N_2O-oxynitride devices exhibit a lower threshold voltage. This may be due to their higher dielectric constant [12]. In contrast, V_{TH} under the DT mode approaches 0.7 V, with a distribution tighter than the O_2-oxide counterparts. This is because a higher dielectric constant leads to a lower γ value, so the weighting of the third term in eq.(2)

diminishes under DT-mode operation. As a result, the V_{TH} of N_2O-oxynitride devices is closer to $V_{FB} + 2 \cdot \phi_{FP}$ than that of O_2-oxide devices.

The *S.S.* versus gate length for various N_2O-oxynitride splits is plotted and shown in Fig. 2.7. The trend is similar to that of O_2-oxide, i.e., a thicker dielectric results in larger *S.S.* under the conventional mode, while the *S.S.* of all devices operating under the DT mode is close to 60 mV/dec. Again the *S.S.* distribution of all N_2O-oxynitride devices is tighter that that of O_2-oxide counterparts, due to a lower γ value.

Other device parameters under the conventional and DT modes are also compared between O_2-oxide and N_2O-oxynitride devices. Normalized linear transconductance (i.e., the product of *Tox* and linear *Gm*) as a function of gate length with dielectric thickness as a parameter is shown in Fig. 2.8. Under the conventional mode of operation, devices with O_2-oxide depict slightly larger *Gm*, compared with their N_2O-oxynitride counterparts, despite a larger dielectric constant for N_2O-oxynitride. This is believed to be due to larger carrier mobility in O_2-oxide devices, as nitrogen-induced donor-like traps at the interface degrade the mobility of oxynitride devices [13-14].

Also shown in Fig. 2.8, it can be seen that the linear G_m under the DT mode is roughly three fold that under the conventional mode. This is true for both O_2-oxide

and N_2O-oxynitride devices. The higher *Gm* under the DT mode can be explained by considering the transconductance in the linear region for both the conventional and DT-modes, which can be expressed as:

$$G_{m.lin} = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \mu_n \left(\frac{W}{L}\right) C_{OX} V_D \qquad \text{(conventional mode) } \mathbf{(8)}$$

$$G_{m.lin} = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \mu_n \left(\frac{W}{L}\right) C_{OX} \left[1 - \left(\frac{\partial V_{TH}}{\partial V_G}\right)\right] V_D . \quad \text{(DT-mode) } \mathbf{(9)}$$

The drain current I_D in the DT mode depends on the dynamic V_{TH}, which decreases with increasing gate voltage, according to eq. 2. Therefore, the linear *Gm* under the DT mode must be corrected according to eq. 9. Since the term $\partial V_{TH} / \partial V_G$ is negative, $G_{m.lin}$ increases. This explains why devices operating under the DT mode have a much higher linear *Gm*. Moreover, since $\partial V_{TH} / \partial V_G$ also depends on the inverse of C_{OX}, a larger gate dielectric constant in N_2O-oxynitride devices with a higher mobility results in a smaller $\partial V_{TH} / \partial V_G$ than that of their O_2-oxide counterparts. This explains why G_m of O_2-oxide devices is larger than that of N_2O devices.

Saturation transconductance ($G_{m.sat}$) versus drain-induced barrier lowering (DIBL) are compared for oxide and oxynitride devices under both the DT and conventional modes. The results are shown in Fig. 2.9. Under the conventional mode, $G_{m.sat}$ is comparable between both samples. This can be explained by the equation for $G_{m.sat}$ shown in eq.10 below. However, under the DT mode, DIBL significantly decreases due to a narrower depletion width by forward biasing of the substrate [15].

The trend of $G_{m.sat}$ under the DT mode is similar to that of $G_{m.lin}$, i.e., by adding the term [1- $\partial V_{TH} / \partial V_G$] as shown in eq.(11).

$$G_{m.sat} = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=const} = \mu_n \left(\frac{W}{L}\right) C_{OX} \left(V_G - V_{TH}\right) \text{ (conventional mode)} \quad (10)$$

$$G_{m.sat} = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=const} = \mu_n \left(\frac{W}{L}\right) C_{OX} \left(V_G - V_{TH}\right)\left[1 - \left(\frac{\partial V_{TH}}{\partial V_G}\right)\right] \text{ (DT mode)} \quad (11)$$

Combining eq.(7), eq.(9) and eq.(11), the values of linear and saturation transconductance with the same channel doping concentration are proportional to $\mu_n C_{OX}$, rather than γ. Therefore, as far as the drive current under the DT mode is concerned, gate capacitance and channel doping concentration must be discussed separately.

2.4 Summary

In this Chapter, nMOSFETs of different dielectric types and thicknesses have been investigated in detail. When operating under the DT mode, all the devices depict essentially the same threshold voltage, and close to the ideal subthreshold slope value of 60 mV/dec. The threshold voltage for N_2O-oxynitride devices is closer to 0.7 V than that of O_2-oxide counterparts due to its higher dielectric constant. For the dynamic threshold operation, the term [1- $\partial V_{TH} / \partial V_G$] should be taken into consideration in all formulas for calculating the device parameters. Saturation transconductance is found to increase significantly when operating under DT mode. Furthermore, N_2O-oxynitride with a higher dielectric constant does not ensure a

higher saturation transconductance in DT mode because of the low value of [1- $\partial V_{TH} / \partial V_G$]. Finally, our results also show that both $G_{m.sat}$ and $G_{m.lin}$ are proportional to $\mu_n C_{OX}$, rather than γ.

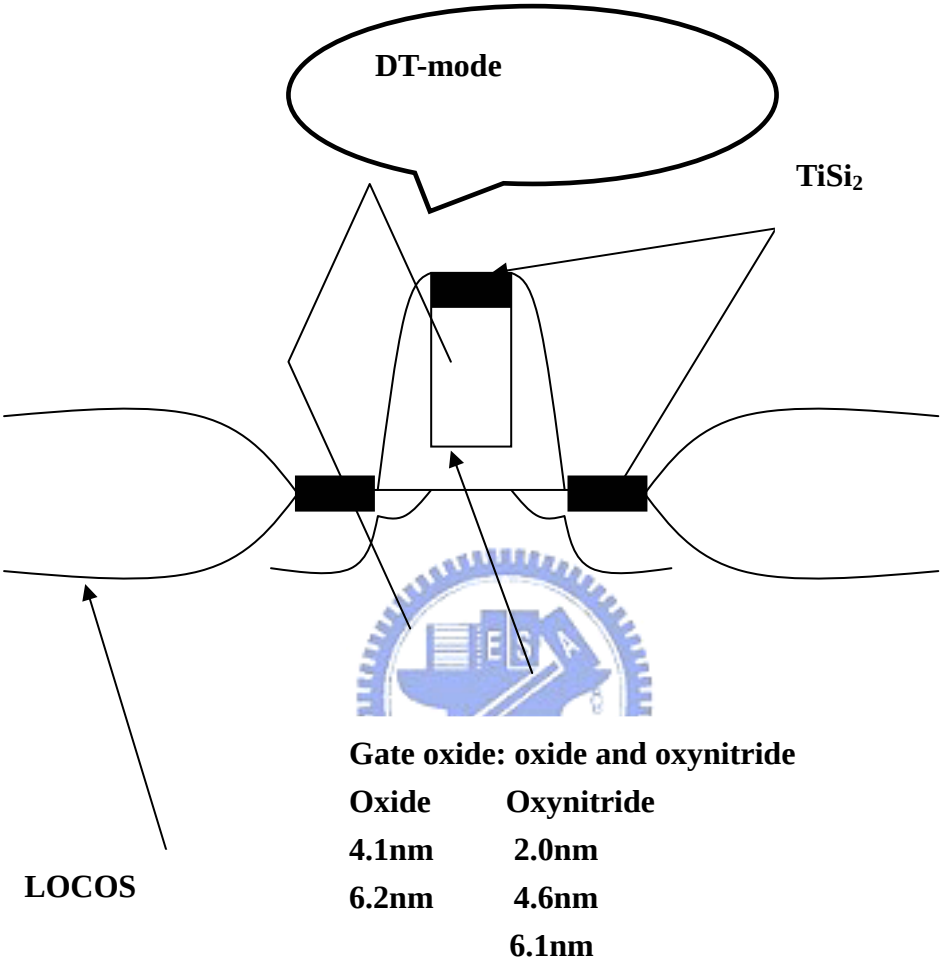


Fig.2.1 Connections of MOSFET under DT mode, and split conditions of gate dielecrics.

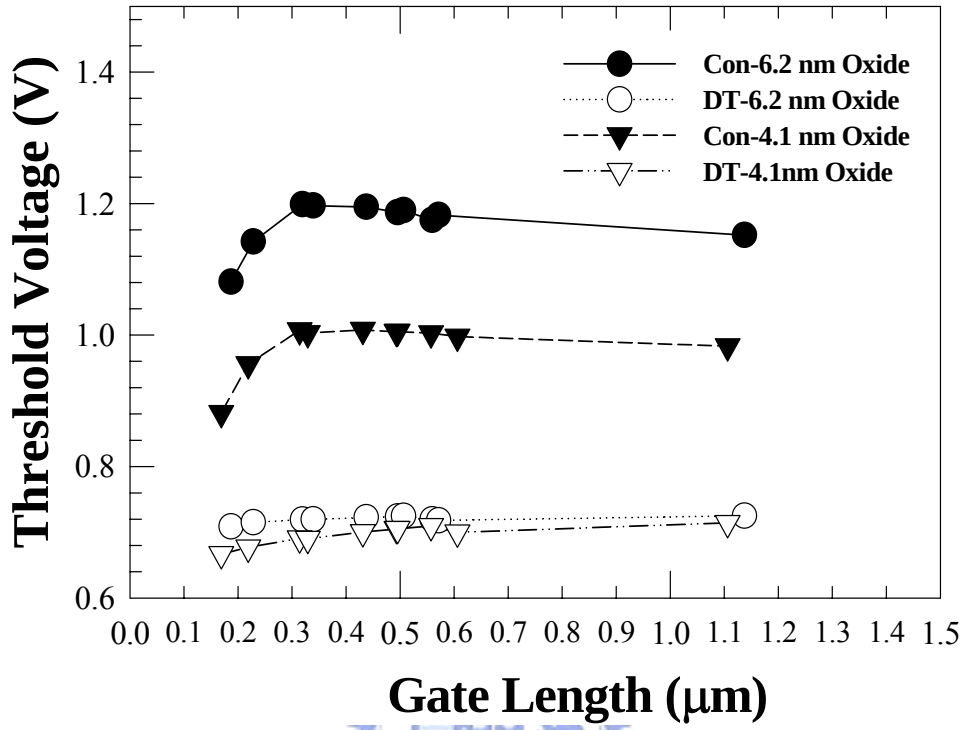


Fig.2.2 Threshold voltage versus gate length under both conventional and DT modes for devices with thermal oxide. The oxide thickness is 4.1 nm, and 6.2 nm. The device width is 20 μm.

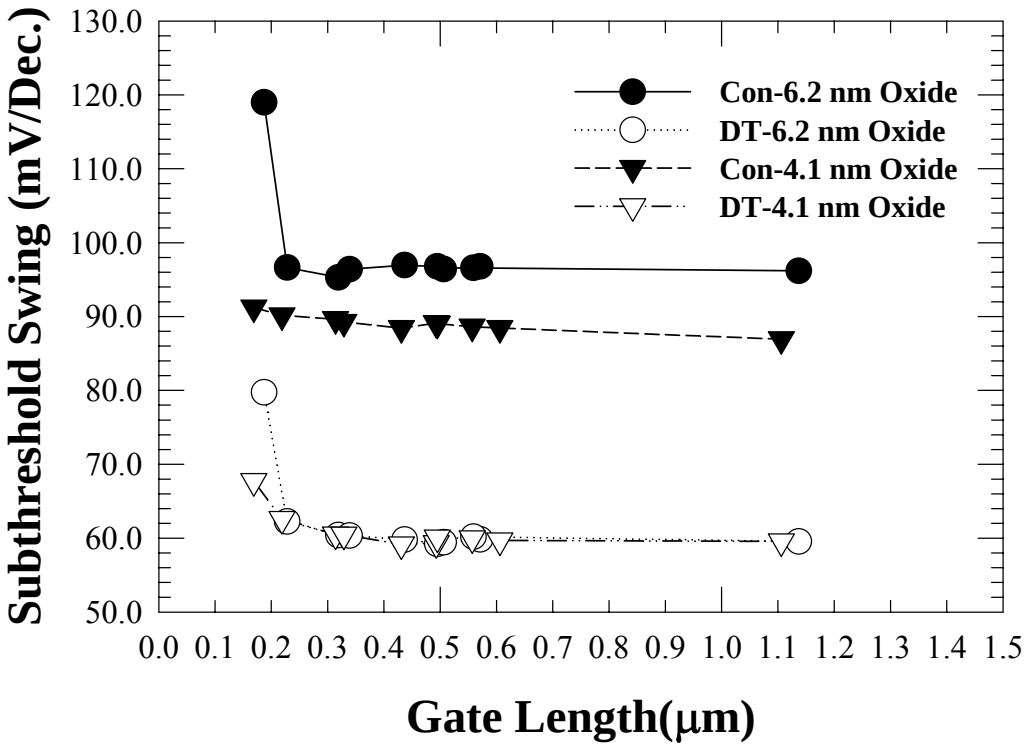


Fig.2.3 Subthreshold swing versus gate length under both conventional and DT modes for devices with thermal oxide. The oxide thickness is 4.1 nm, and 6.2 nm. The device width is 20 μm.

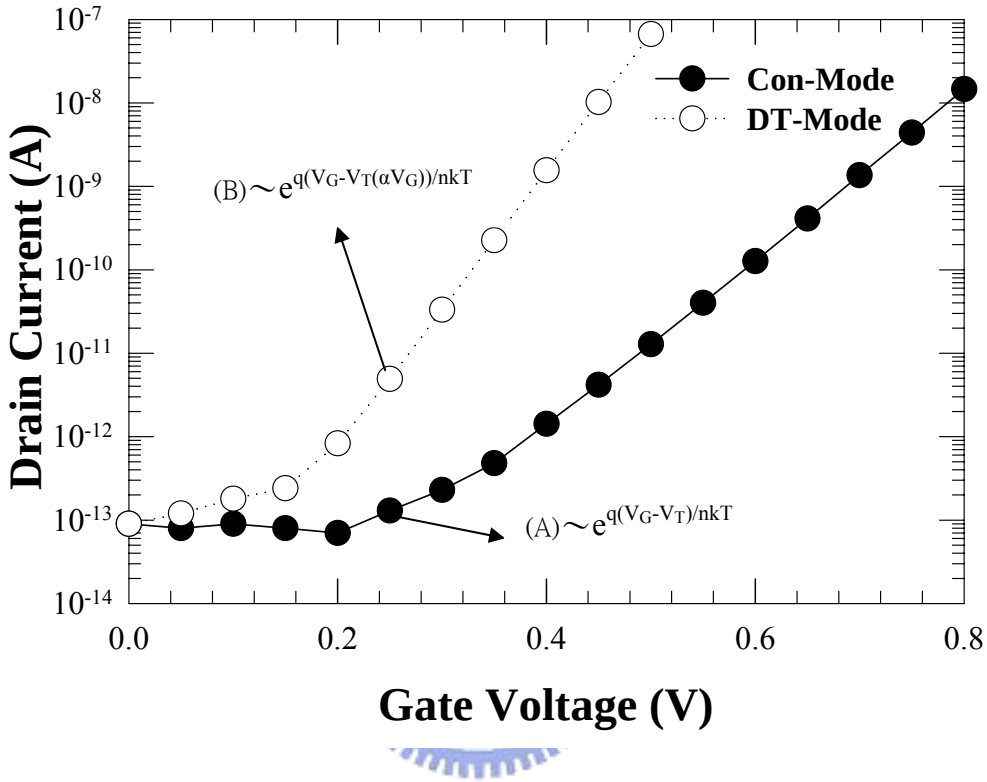


Fig.2.4 Transfer characteristics for nMOSFETs under both conventional (curve A) and DT (curve B) modes. The gate length is 0.57 μm, while the gate dielectric is 6.2 nm thermal oxide.

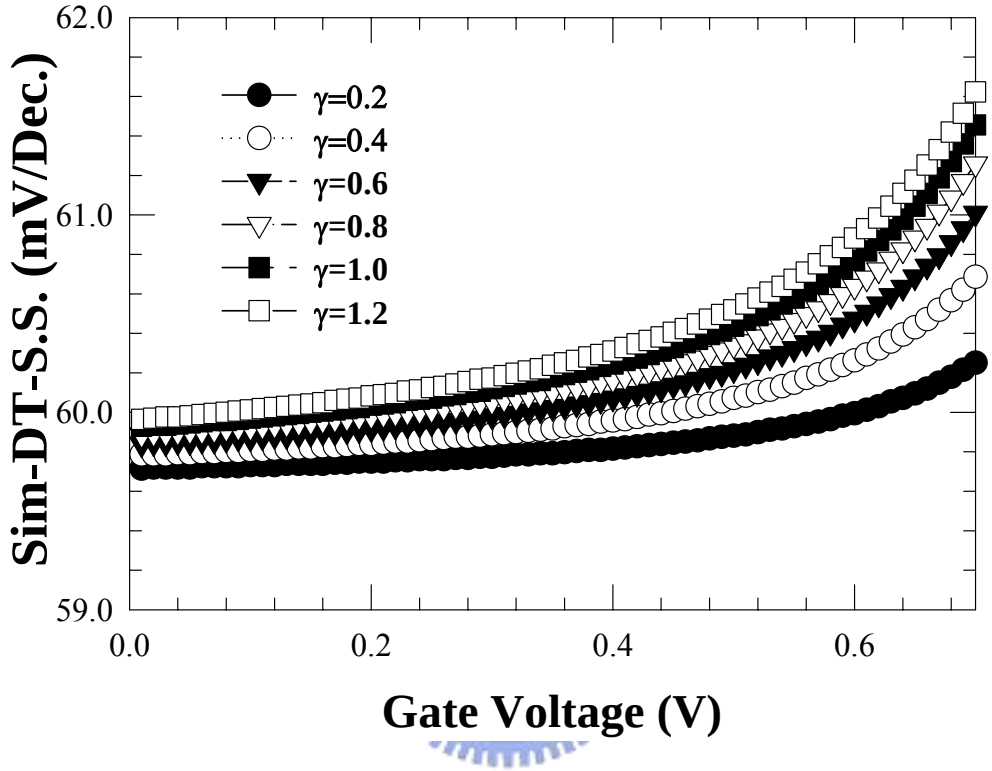


Fig.2.5(a) Simulated subthreshold swing under DT-mode versus gate voltage with γ values varying from 0.2 to 1.2. The *S.S.* increases as gate voltage and γ value increase.

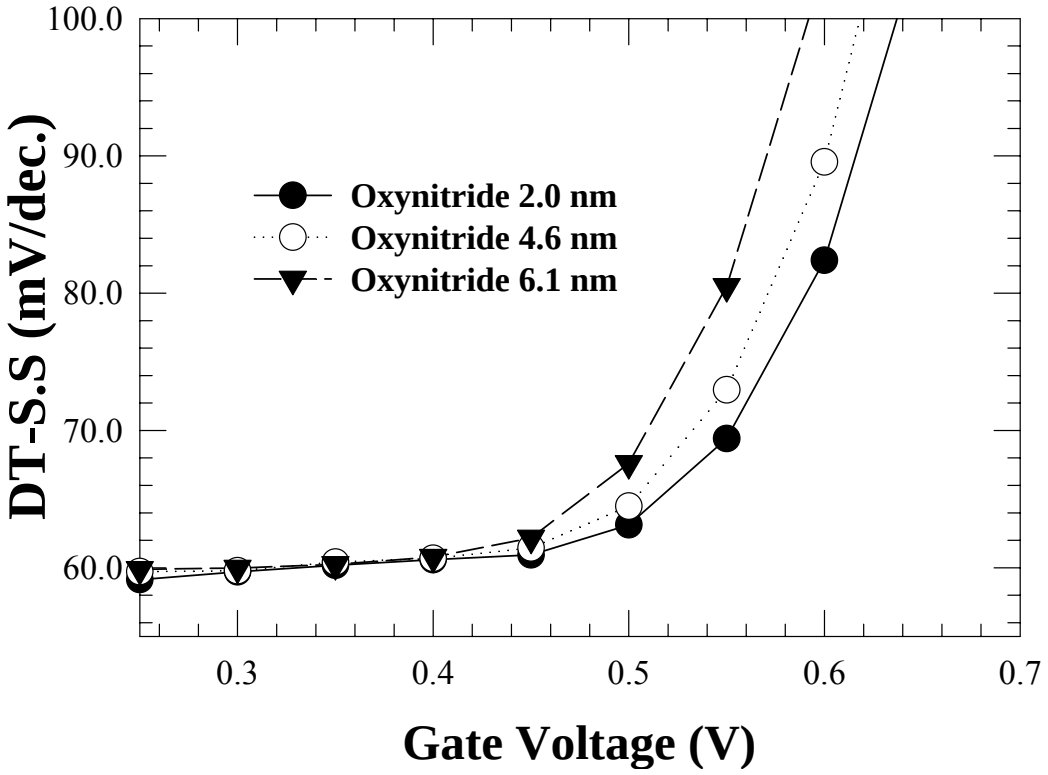


Fig.2.5(b) The subthreshold swing under DT-mode versus gate voltage for distinct gate oxynitride thickness.

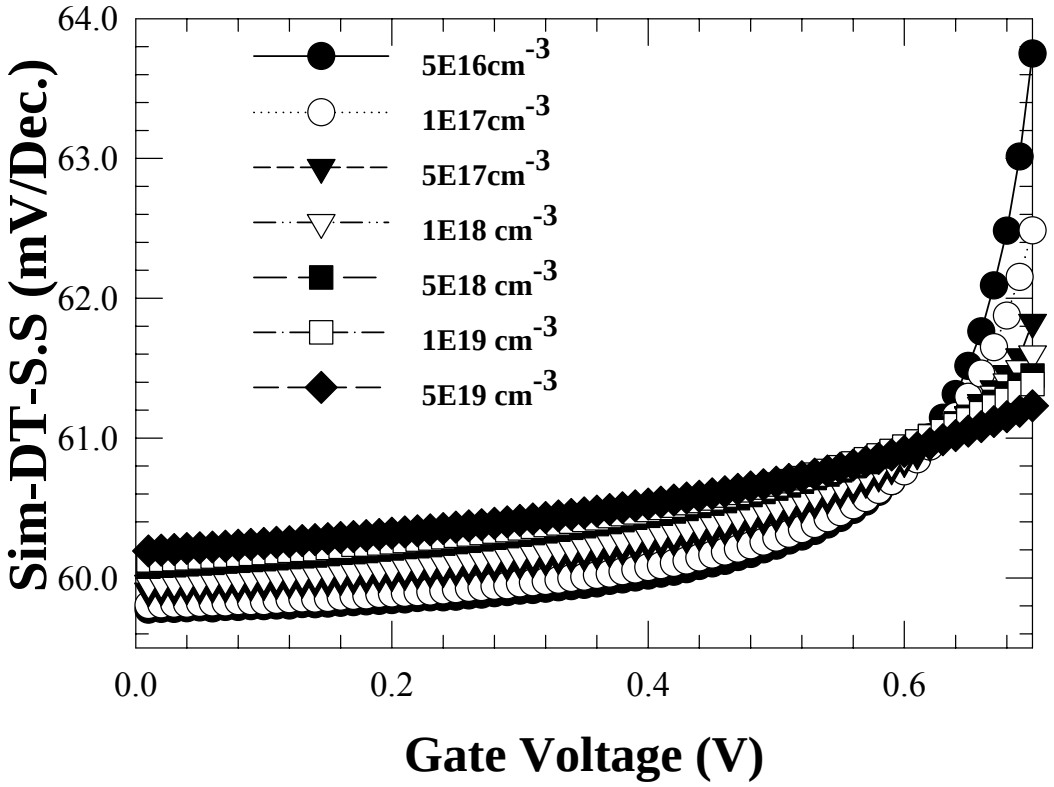


Fig. 2.5(c) Simulation of the S.S with different doping concentration (between 5×16 cm^{-3} and 5×19 cm^{-3}) with different γ value versus gate voltage Vg.

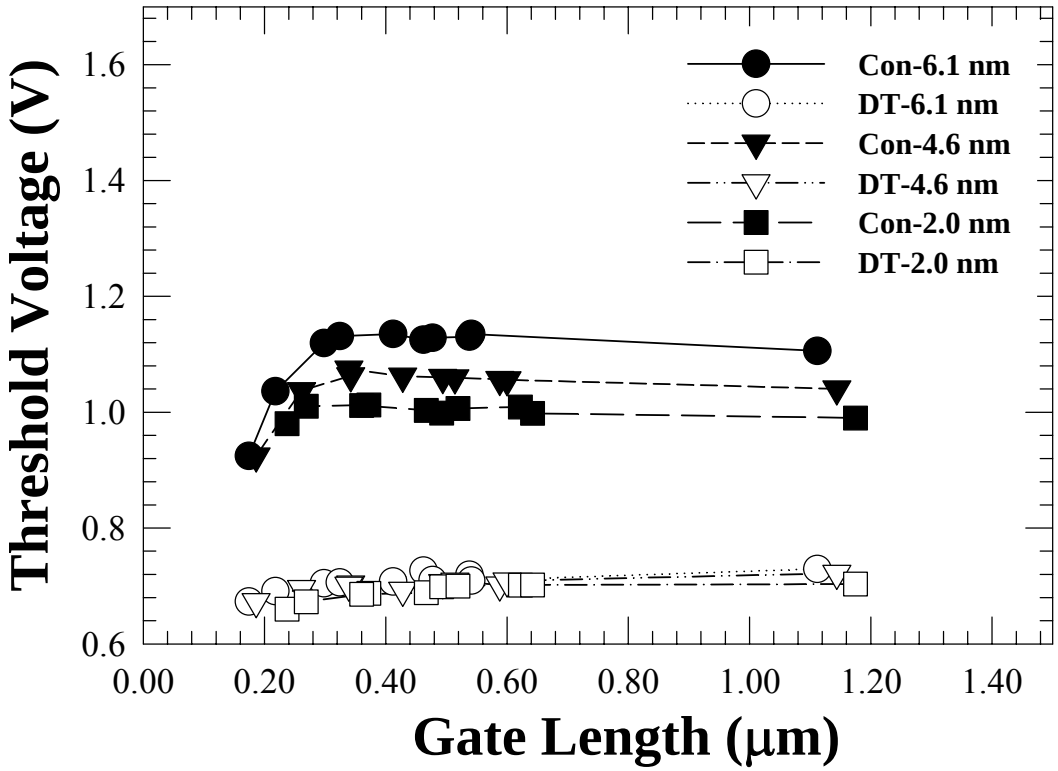


Fig.2.6 Threshold voltage versus gate length under both conventional and DT modes. The gate dielectric is grown by N_2O-oxynitride. The thickness is 2.0 nm, 4.6 nm, 6.1 nm. The device width is 20 μm.

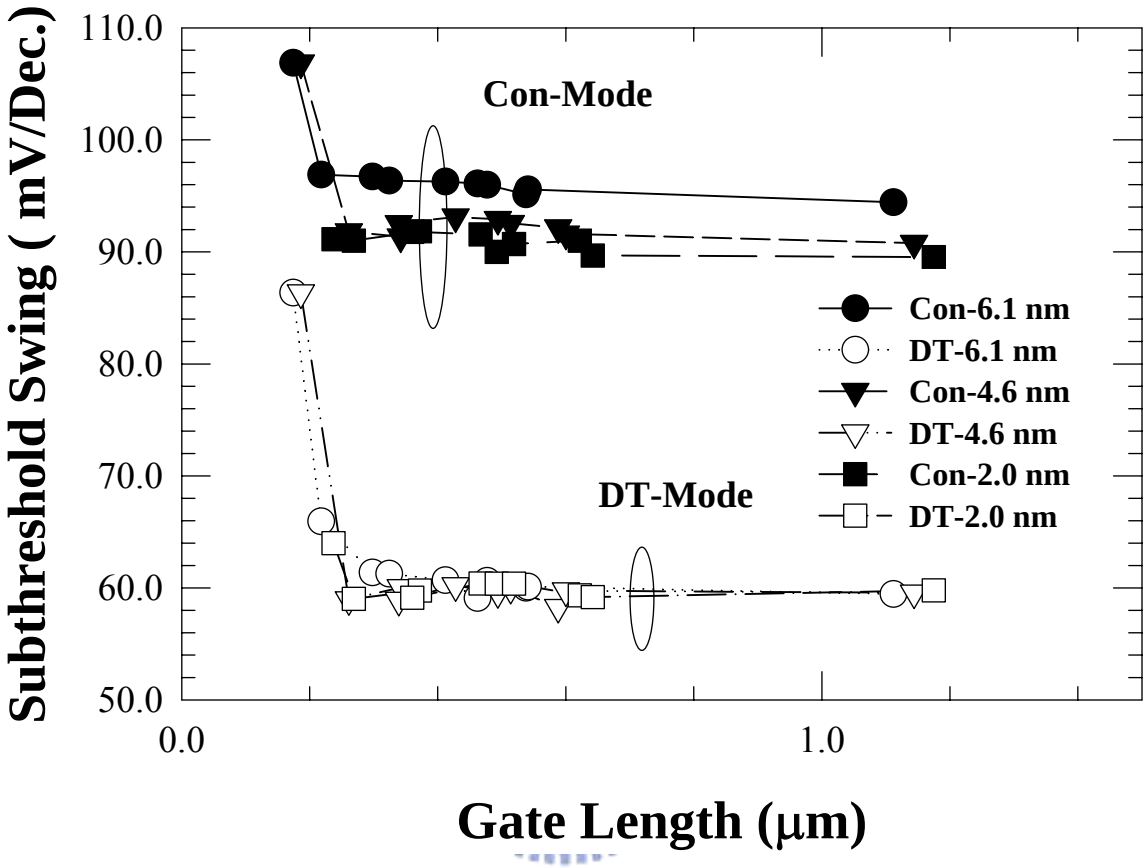


Fig.2.7 Subthreshold swing versus gate length under both conventional and DT modes. The gate dielectric is grown by N_2O-oxynitride. The thickness is 2.0 nm, 4.6 nm, 6.1 nm. The device width is 20 μm.

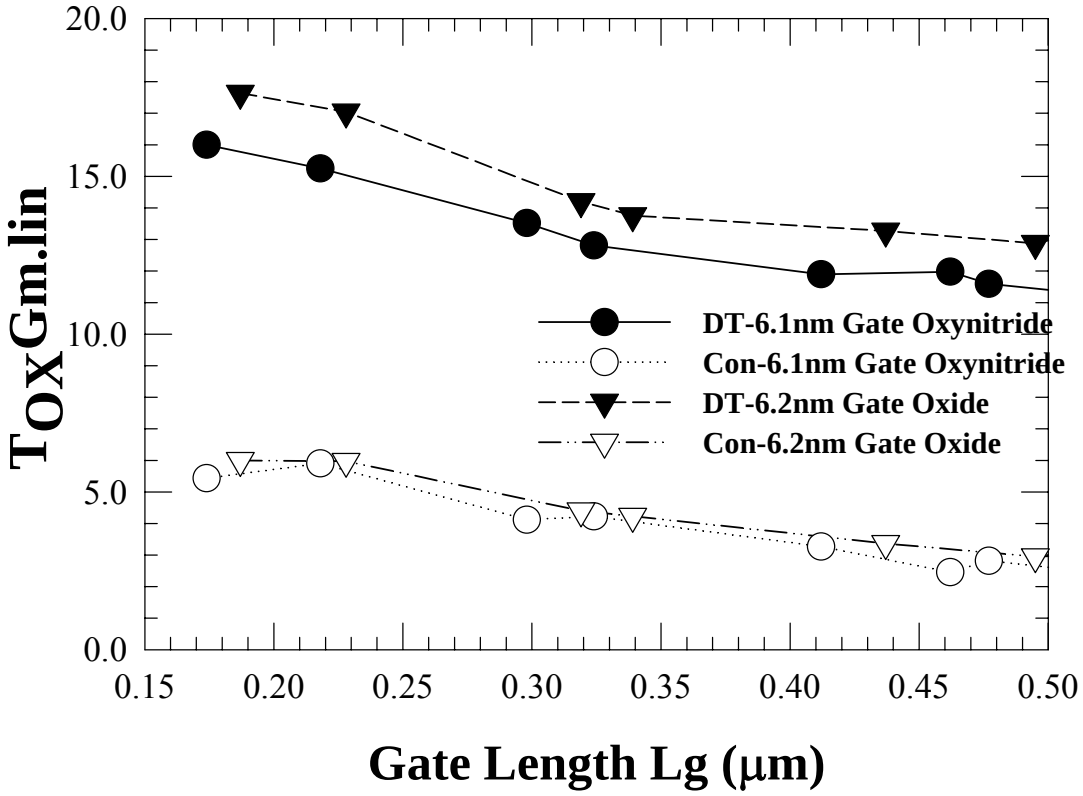


Fig.2.8 Normalized linear transconductance (i.e., the product of oxide thickness and linear transconductance) versus gate length under both conventional and DT modes.

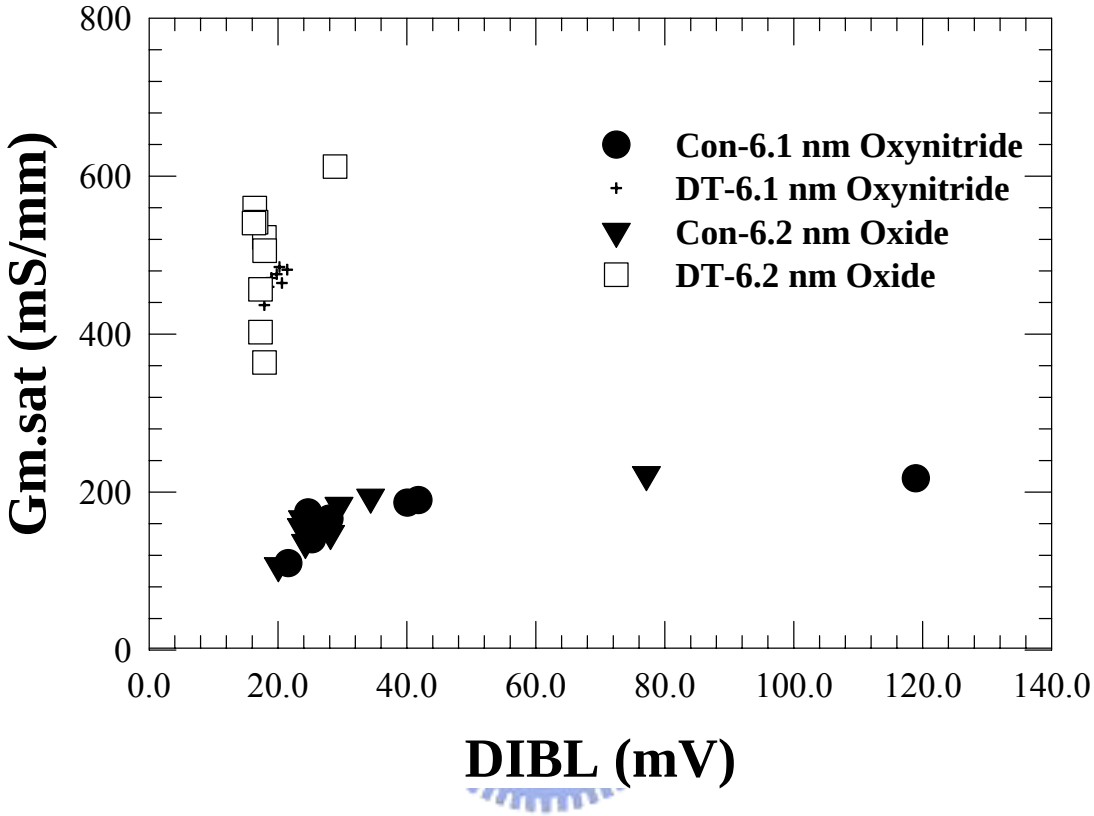


Fig.2.9 Saturation transconductance versus drain-induced barrier lowering (DIBL) under both conventional and DT modes. DIBL reduces dramatically under DT mode because of the narrower depletion width.