Chapter 3

Hot Carrier Degradations of Dynamic Threshold SOI-pMOSFETs

3.1 Background and Motivation

The forward bias between the source and substrate terminals under DT-mode operation would lead to higher junction parasitic capacitance and junction leakage current. Therefore, by fabricating DT-MOSFETs on partially depleted silicon-on-insulator (PD-SOI), the junction leakage current and parasitic capacitance can be greatly reduced. In addition, the neutral region in the substrate is necessary for the DTMOS operation, because the forward bias don't work for fully depleted SOI devices. Therefore, PD-SOI wafers are necessary for DT-MOSFETs fabrication.

Since the use of isolation, such as LOCOS and STI isolation, forbids the formation of body contacts in SOI devices, both H-gate [5] and T-gate [6] structures have been proposed to facilitate the formation of body contacts required for DT-mode operation.

There have been many literature reports regarding DT-MOSFETs [2,16-18]. Among them, only one study [19] discussed the reliability of SOI DT-nMOSFETs. The hot carrier reliability of SOI-pMPSFETs operating under DT-mode at elevated

temperature for different gate structures (i.e., H-gate or T-gate), to the best of our knowledge, is still lacking in the literature. In this chapter, we report hot carrier degradations on SOI pMOSFETs at various temperatures operating under both conventional and DT modes.

3.2 Device Fabrication

P-channel MOSFETs were fabricated on 6-in p-type SOI wafers with resistivity of 15-20 Ω-cm, and a top silicon device layer thickness of 200 nm. Local oxidation of silicon (LOCOS) was used for device isolation, with the top silicon layer fully oxidized (i.e., the active device layer not covered by the masking nitride was fully converted into oxide). As^+ implant with an energy of 100 keV and a dose of 1×10^{13} cm^{-2} was performed through a 30nm sacrificial oxide for threshold voltage (V_{TH}) adjustment. After stripping the sacrificial oxide, a final 3.4 nm gate oxide was grown in N_2O ambient, followed by a 200 nm poly-Si gate deposition. The poly-Si layer was then patterned and etched to define transistor gate length varying from 10.62 μm to 0.8 μm, with a channel width of 100 μm. Shallow S/D extensions were formed by BF_2 implant (10 keV, 1×10^{15} cm^{-2}). After the formation of TEOS sidewall spacer (200 nm), deep heavily-doped source/drain junctions were formed by BF_2 implantation. Afterwards, wafers were annealed by rapid thermal process (RTP) at 1020 °C for 20

sec. A 550 nm TEOS oxide layer was then deposited and etched to form contact holes. Finally, a Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations were performed using an HP4156 system. Hot carrier stressing tests were performed using a temperature-regulated hot chuck at temperature ranging from room temperature to 100 °C.

3.3 Experimental Results and Discussion

3.3.1 Hot carrier degradations for H-gate structure

Figure 3.1(a) shows the electrical connection under DT-mode operation, where the gate and substrate are shorted together during measurements. In contrast, the gate and substrate are not electrically connected under conventional mode operation. Figures 3.1(b) and 3.1(c) depict the device layout for H-gate and T-gate SOI pMOSFET structures, respectively. Body contacts of H-gate structure for SOI MOSFETs are formed on both sides of the transistor gate, as opposed to the single-sided body contacts in T-gate structure.

Fig. 3.2 shows V_{TH} degradations for SOI pMOSFETs at various temperatures and operating under different modes for H-gate structures. Devices were stressed at $V_G=V_{TH}$, and V_D=-4.5 V. Here highly negative drain voltage (V_D=-4.5 V) was used to accelerate the aging process to cause considerable degradation in a reasonable stress

time (i.e., about 6000 sec) [20]. The threshold voltage V_{TH} is deduced from the maximum transconductance (Gm_{max}) method at V_D=-0.1 V. It can be seen that the device operating under conventional mode depicts the worst ΔV_{TH} at room temperature among all measurement splits. Electron trapping appears to be the dominant degradation mechanism at the initial stage of stressing (i.e., before 10^3 seconds) for all splits. This is because the vertical electrical field favors the injection of electrons created by impact ionization near the drain region, where some of the injected electrons are captured by the traps in the dielectric layer. The observed ΔV_{TH} becomes negative for all splits above 10^3 sec., which is an indication of positive charge buildup in the gate dielectric layer. The positive charge may be from either hole trapping in the dielectric or the creation of positively charged interface states at the dielectric interface [21]. The threshold voltage shift under DT-mode is smaller (within 4mV), and is almost independent of temperature due to the DT-mode operation.

Fig. 3.3 shows the comparison of time dependence of G_{mmax} degradation ($\Delta G_{mmax}(t)/G_{mmax}(0)= [G_{mmax}(t)- G_{mmax}(0)]/G_{mmax}(0)$ at V_D=-0.1 V). At room temperature, the device operating under DT mode actually depicts aggravated linear G_{mmax} degradations, much worse than its conventional mode counterpart. This can be explained by the difference in the linear transconductance of SOI pMOSFETs

operating under conventional and DT-modes. The transconductance under conventional mode is proportional to carrier mobility μ_p. The negative substrate bias under DT mode operation will decrease the effective vertical electrical field, thus improves μ_p, and therefore increased the magnitude of G_{mmax}. This is illustrated by varying the substrate bias during conventional-mode operation. As shown in Fig. 3.4, the magnitude of G_{mmax} indeed increases slightly by increasing the magnitude of substrate bias under conventional mode. The linear G_{mmax} as V_D=-0.1 V under DT-mode is about 60 % larger than that of the conventional mode operation with a similar substrate bias V_{SUB}=-0.7 V. This result clearly indicates that the transconductance under DT-mode depends on both the effective vertical electric field and the dynamic behavior of the substrate bias, which was discussed in chapter 2 [22].

Therefore, to the point of view for transconductance under DT-mode operation, the magnitude of transconductance would be “enlarged”. In addition, during hot-carrier stressing, the carrier mobility μ_p decreases, and the dynamic behavior under DT-mode would enlarge the magnitude of G_m degradation.

To confirm this interesting phenomenon, a device was stressed at V_D=-4.5 V, V_G=V_{TH} under conventional mode, and the transconductance before and after stressing was measured under both conventional and DT modes. Interestingly, 3 % and 8 % degradations are found for conventional and DT-modes, respectively, which

clearly confirmed the enhanced transconductance degradation effect under DT-mode. This “enlargement” behavior dominates the transconductance degradation under DT mode at room temperature.

At higher temperatures (e.g., 75 ℃ and 100 ℃), however, the degradations under DT-mode are alleviated, and become comparable to those observed under conventional mode. Similar results are also depicted in Fig. 3.5, which shows the drive current degradation of SOI pMOSFETs under both conventional and DT modes at various temperatures. The drive current is measured at V_D=V_G=-0.7 V. Since the difference of ΔV_{TH} for devices of H-gate structures under DT-mode is small, the drive current degradation is dominated by transconductance degradation. The drive current degradation is alleviated at elevated temperature, consistent with that of transconductance shown in Fig. 3.3. This is because the carrier mean free path is reduced at higher temperature, so the carriers are more likely to collide before gaining sufficient energy for impact ionization, so the impact ionization rate is reduced at higher temperature.

3.3.2 The characteristics under DT mode at elevated temperature

The threshold voltage V_{TH} can be expressed as:

$$V_{TH} = V_{FB} + 2\cdot\phi_{FB} + \gamma\sqrt{2\cdot\phi_{FB} + V_{BS}} \qquad (1)$$

and $\gamma \equiv C_{ox}^{-1}\sqrt{2\cdot q\cdot\varepsilon_s\cdot N_A}$

$$\phi_{FB} = \left(\frac{KT}{q}\right) \times \ln\left(\frac{N_A}{N_i}\right)$$

where V_{TH} is threshold voltage, V_{FB} is flat band voltage, ϕ_{FB} is the potential difference between the Fermi level and the intrinsic level of the bulk semiconductor, C_{OX} is the gate oxide capacitance, γ is the body-effect factor, N_A is the channel doping concentration, N_i is the intrinsic concentration, and V_{BS} is the substrate bias. Higher temperature leads to a lower ϕ_{FB}, so the threshold voltage is reduced at elevated temperature. The effects of temperature on the reduction ratio of threshold voltage as a function of gate length for transistors under both DT and conventional modes are shown in Fig. 3.6 for H-gate devices. The nominal transistor gate length varies from 3.62 to 0.8 μm, with a fixed device width of 100 μm. The reduction ratio of threshold voltage under DT mode is larger than that under conventional mode.

The transconductance at various temperatures for H-gate structures under both conventional and DT modes are shown in Fig. 3.7. It is interesting to note that the transconductance reduction ratio at elevated temperature under DT mode is larger than that under conventional mode, and the gate voltage of maximum transconductance would shift due to the threshold voltage reduction. As a result, the transconductance ratio between DT and conventional modes is decreased from 1.7 to 1.5, as plotted in Fig. 3.8. The reduction ratio in transconductance with respect to the room temperature value under DT-mode is also larger than that under conventional

mode when the temperature increases from room temperature to 100°C, as shown in Fig. 3.8. In addition to the reduced carrier mean free path at higher temperature, which tends to reduce impact ionization, the “transconductance enlargement” effect is also reduced at elevated temperature due the decreasing transconductance ratio between both modes. Therefore, the drive current and transconductance degradation at elevated temperature would alleviate.

3.3.3 Hot carrier degradation for T-gate structure

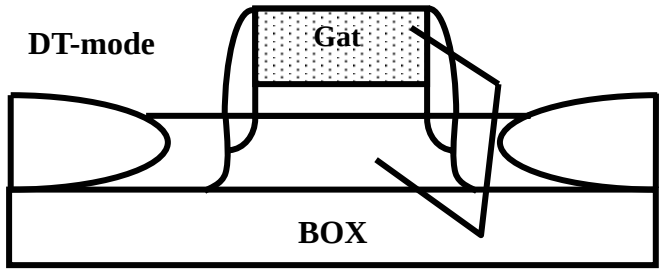
Threshold voltage degradations for devices with T-gate structure are shown in Fig. 3.9. The same stressing conditions as H-gate structures are used, i.e., $V_G=V_{TH}$, and V_D=-4.5 V. The same as H-gate structures, the threshold voltage degradation under DT mode is smaller (within 4 mV), and is almost independent of temperature. Fig. 3.10 shows the comparison of time dependence of G_{mmax} degradation for SOI pMOSFETs at various temperatures and operating under different modes for T-gate devices. The transconductance degradation under DT mode at room temperature still shows the worst behavior, and improves at elevated temperature. Fig. 3.11 depicts the drive current degradation for T-gate structures. The drive current degradation under DT-mode is dominated by transconductance degradation. Furthermore, for devices operating under DT-mode, the transconductance and drive current for T-gate structure depicts larger degradations than that for the H-gate structure. The body potential

distribution for both structures under DT-mode was simulated and shown in Fig. 3.12. Non-uniform body potential distribution was shown for T-gate structures under DT-mode. Therefore, the external electrical field for T-gate structures under DT-mode may cause the larger degradation of drive current and transconductance than that for H-gate structure, because other conditions, besides the body potential distribution, were the same for both structures under DT-mode.

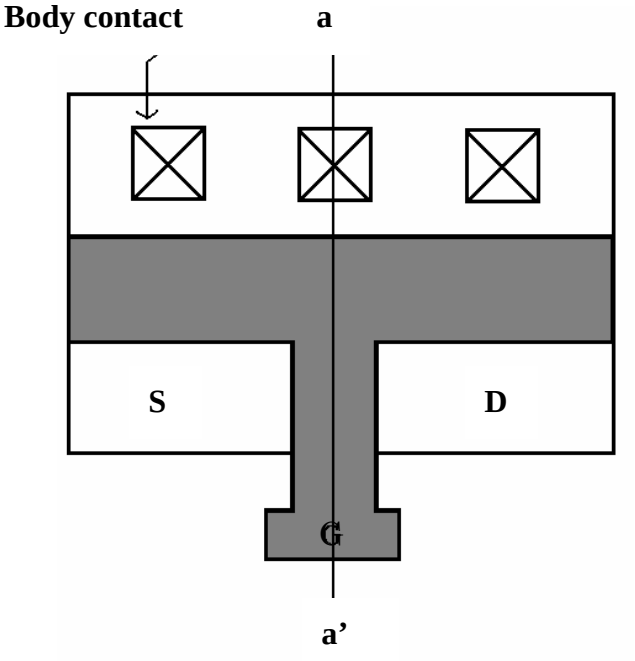
3.4 Summary

Hot carriers induced degradation in DT SOI-pMOSFETs for T- and H-gate structures at various temperatures have been investigated in this study. The maximum transconductance degradation, threshold voltage shift, and drive current degradation were measured. The ΔV_{TH} under DT-mode is less than that under conventional mode due to its lower interface state generation by the negative body bias. In addition, ΔV_{TH} under conventional mode is alleviated at elevated temperature due to reduced impact ionization. More importantly, G_{mmax} and drive current degradations are found to be enhanced under DT-mode due to the “transconductance enlargement” effects by both the decreasing effective vertical electrical field and dynamic behavior at room temperature. At elevated temperature, these enhanced degradations under DT mode would be improved and become comparable to those under conventional mode. In

addition, the degradation of T-gate structure is worse than that of H-gate structure.



(a)



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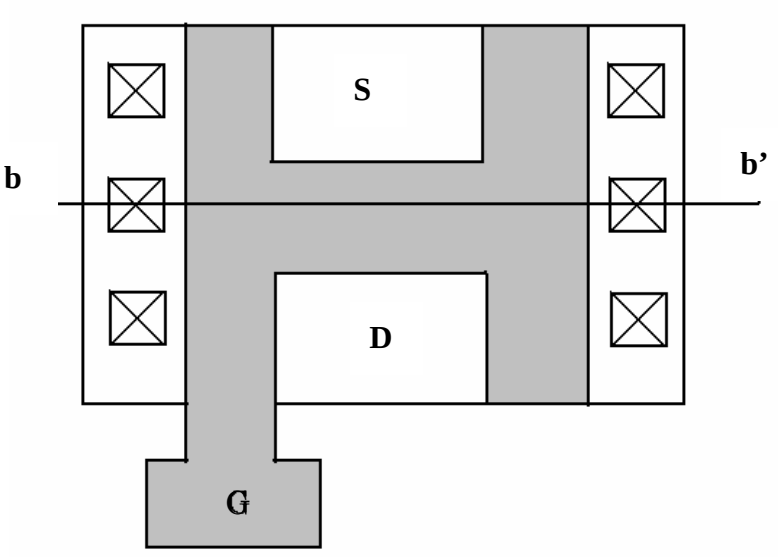


(c)

Fig. 3.1 (a) Connections of SOI MOSFETs under DT-mode, (b) T-gate structure, and (c) H-gate structure.

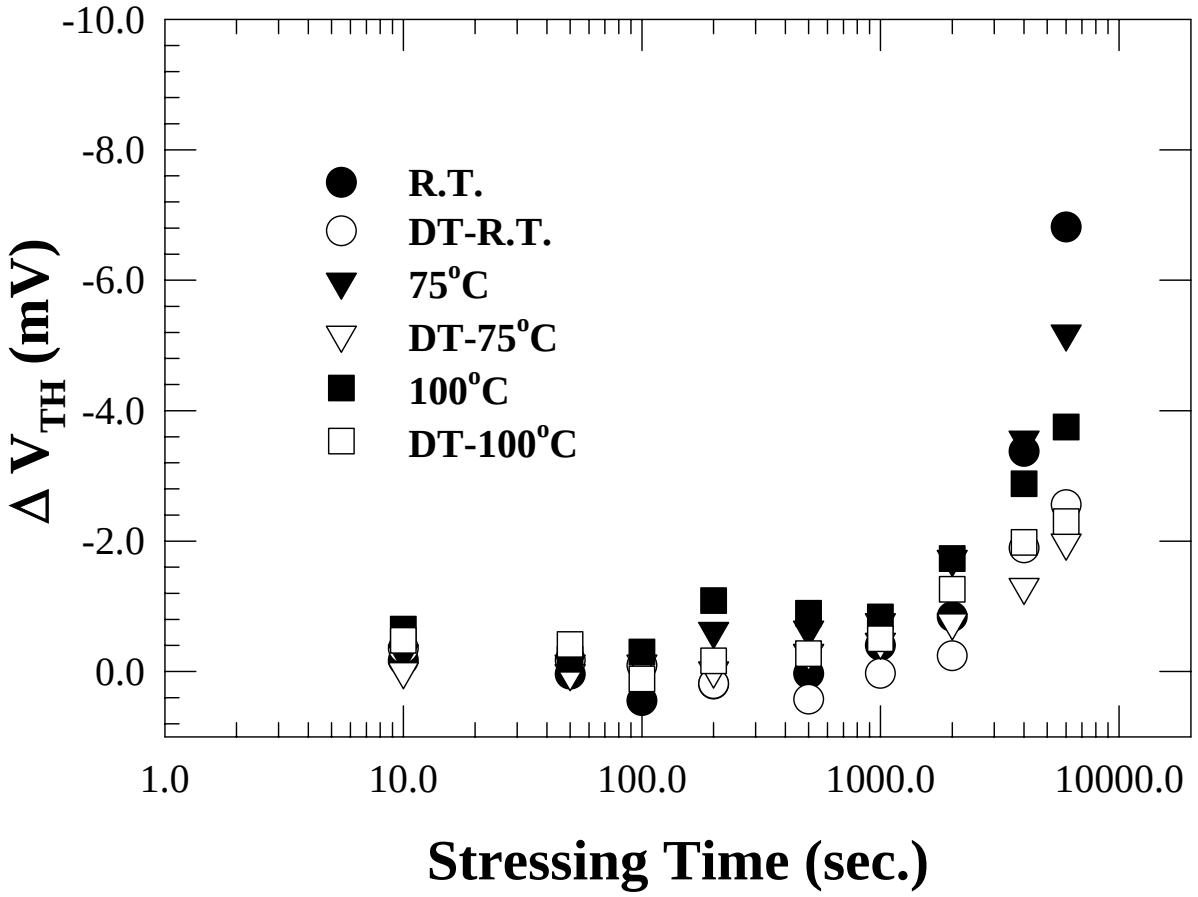


Fig. 3.2 Stress time dependence of V_{TH} degradation for SOI pMOSFETs at various temperatures and under both conventional and DT-modes for H-gate devices. Devices were stressed at $V_G=V_{TH}$, V_D=-4.5V. The vertical log scale is $\Delta V_{TH}= V_{TH}(t)- V_{TH}(0)$.

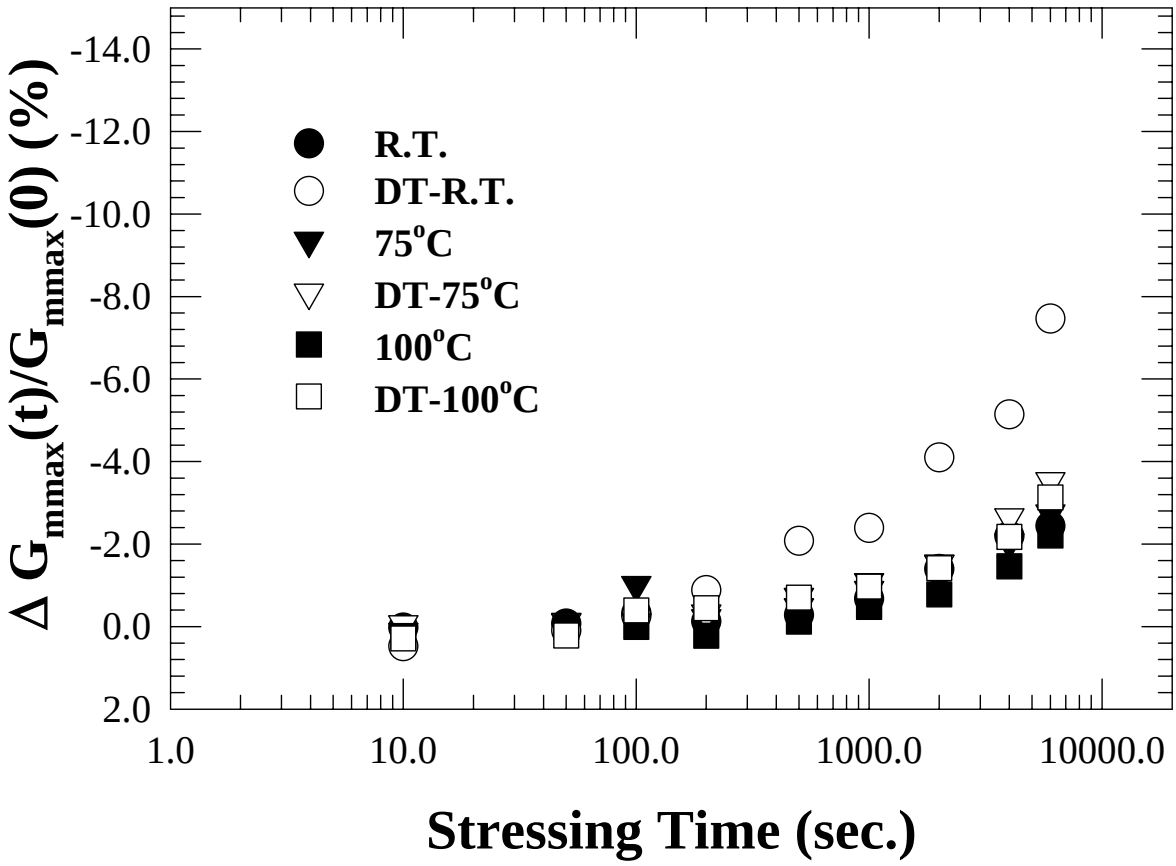


Fig. 3.3 Stress time dependence of G_{mmax} degradation for SOI pMOSFETs at various temperatures and operating under both conventional- and DT-modes for H-gate devices. Devices were stressed at $V_G=V_{TH}$, V_D=-4.5 V. The vertical log scale is $\Delta G_{mmax}(t)/G_{mmax}(0)= [G_{mmax}(t)- G_{mmax}(0)]/G_{mmax}(0)$ for V_D=-0.1 V.

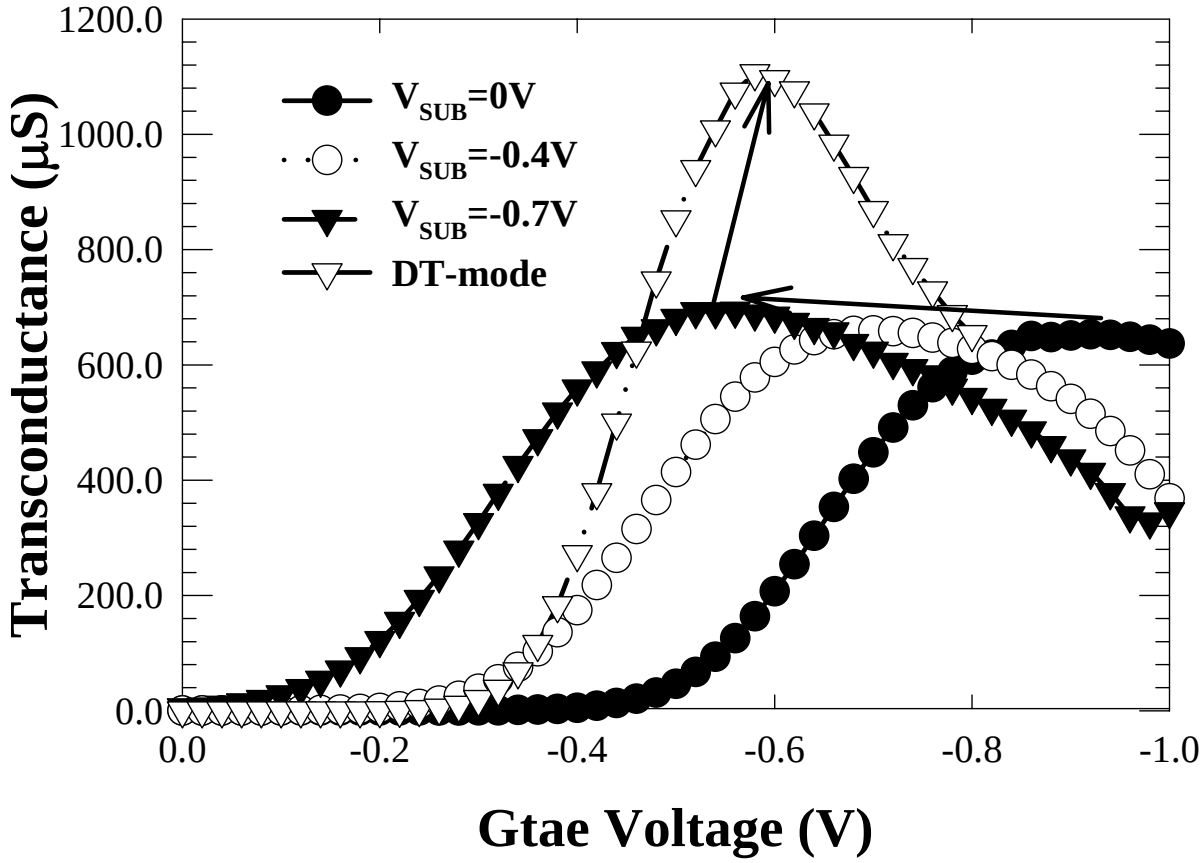


Fig. 3.4 Gate voltage versus transconductance for H-gate SOI pMOSFETs under conventional modes with various substrate biases and also under DT-mode.

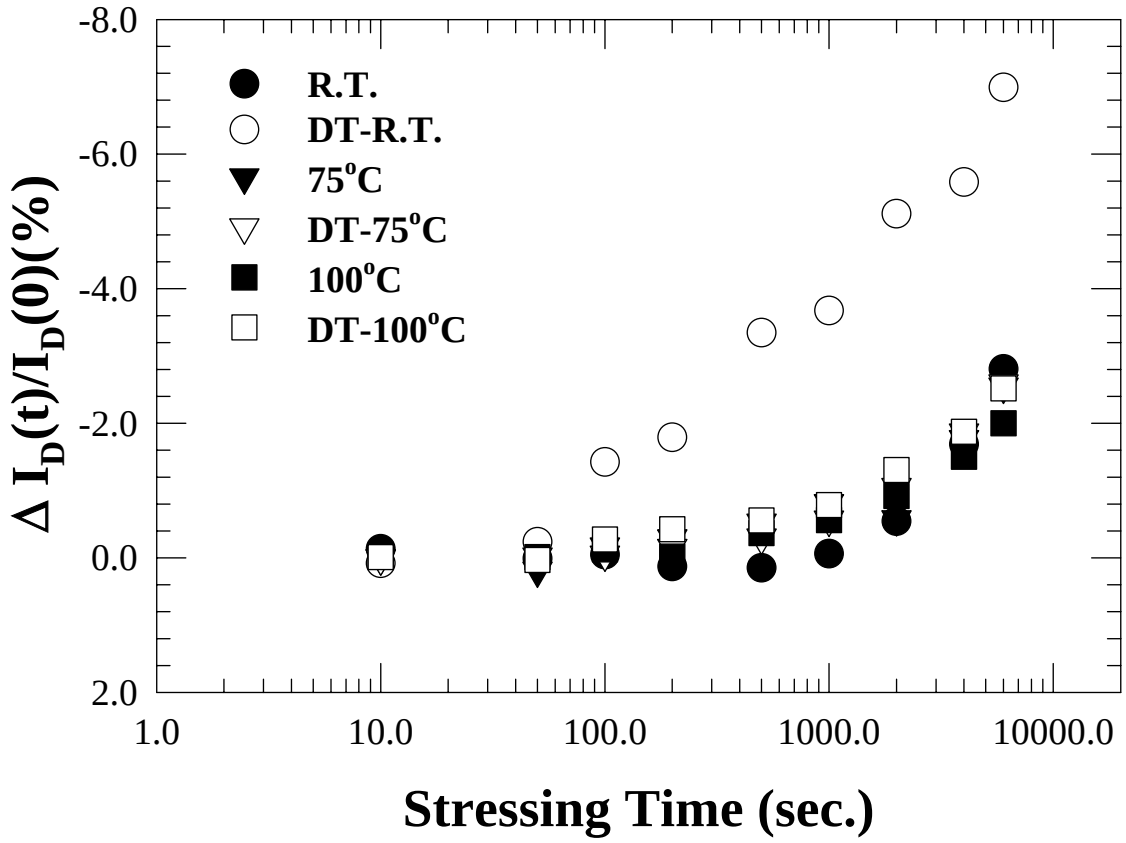


Fig. 3.5 Stress time dependence of on current (V_G=-0.7 V, V_D=-0.7 V) degradation for H-gate SOI pMOSFETs. Devices were stressed at V_G=V_{TH}, V_D=-4.5 V, $\Delta I_{ON}/I_{ON}(0)$= $[I_{ON}(t)- I_{ON}(0)]/I_{ON}(0)$.

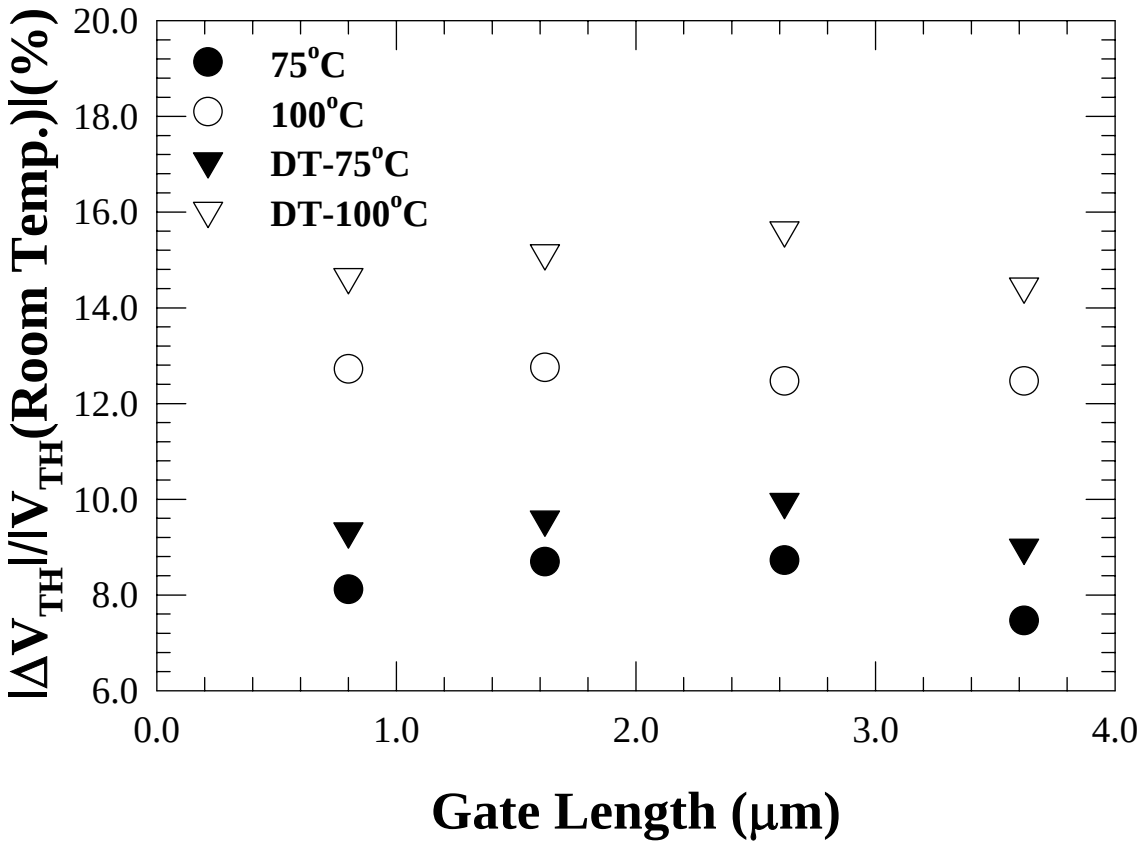


Fig. 3.6 Threshold voltage reduction ratio with respect to room temperature threshold voltage versus gate length for H-gate devices under both conventional and DT modes at various temperatures. The gate length varies from 3.62 to 0.8 μm with width of 100 μm. $\Delta V_{TH}/V_{TH}$ (Room Temp.)= [V_{TH}(elevated temp.)- V_{TH}(room temp.)]/V_{TH}(room temp.

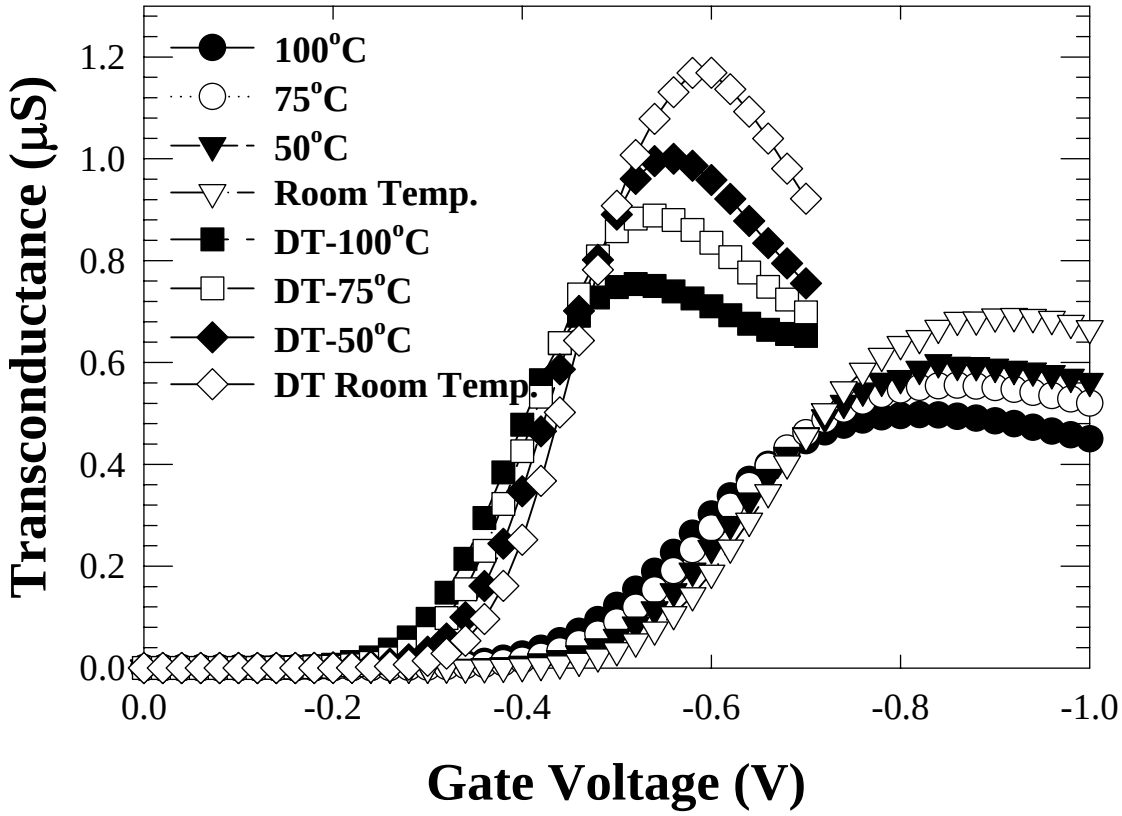


Fig. 3.7 Tansconductance versus gate voltage for H-gate SOI pMOSFETs with temperature varying from room temperature to 100 ℃.

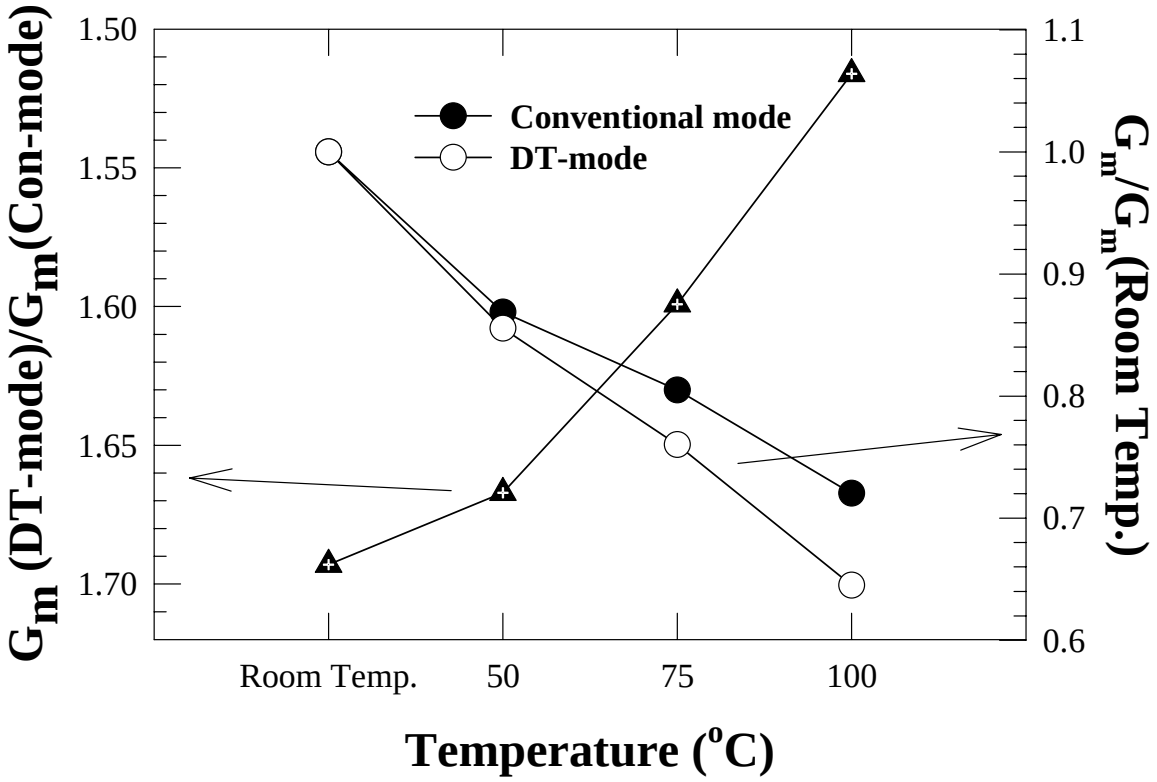


Fig. 3.8 Tansconductance ratio between conventional and DT-modes (left) and G_m/G_m (room temperature) for H-gate structures under conventional and DT-modes (right) versus temperature.

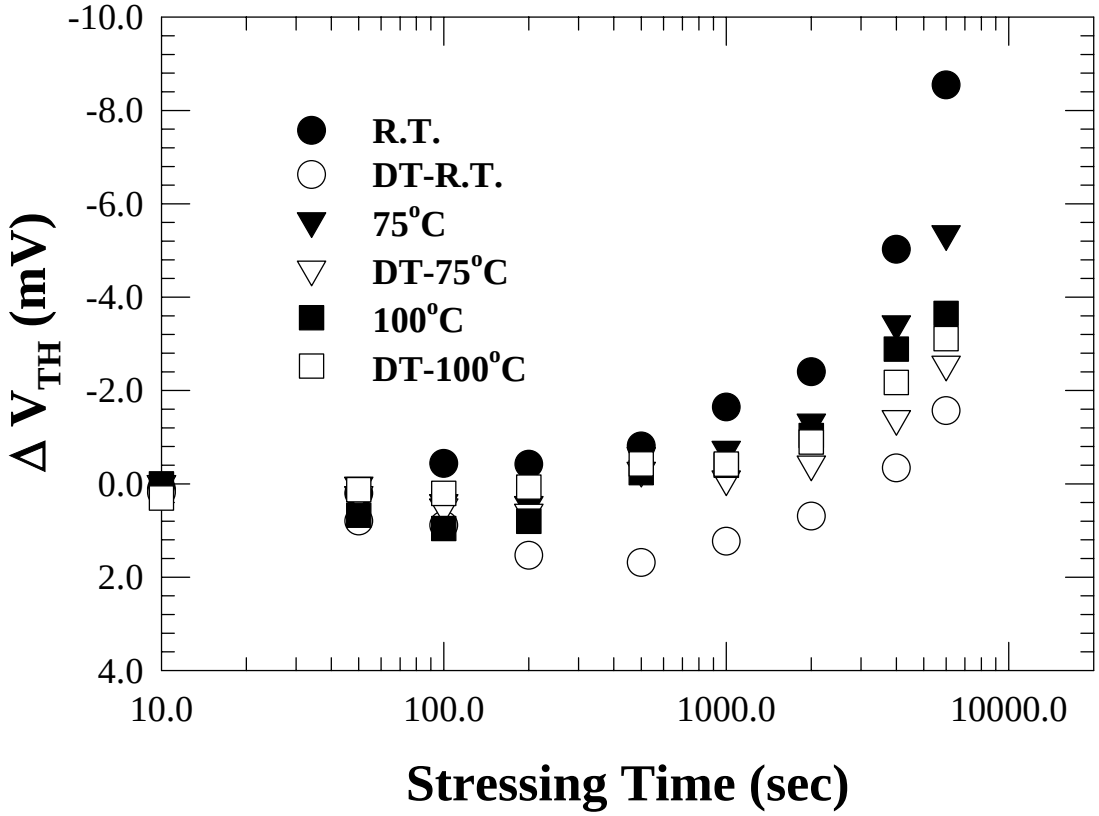


Fig. 3.9 Stress time dependence of V_{TH} degradation for T-gate SOI pMOSFETs at various temperatures and operating under different modes. Devices were stressed at $V_G=V_{TH}$, V_D=-4.5 V. the vertical log scale is ($\Delta V_{TH}= V_{TH}(t)- V_{TH}(0)$.

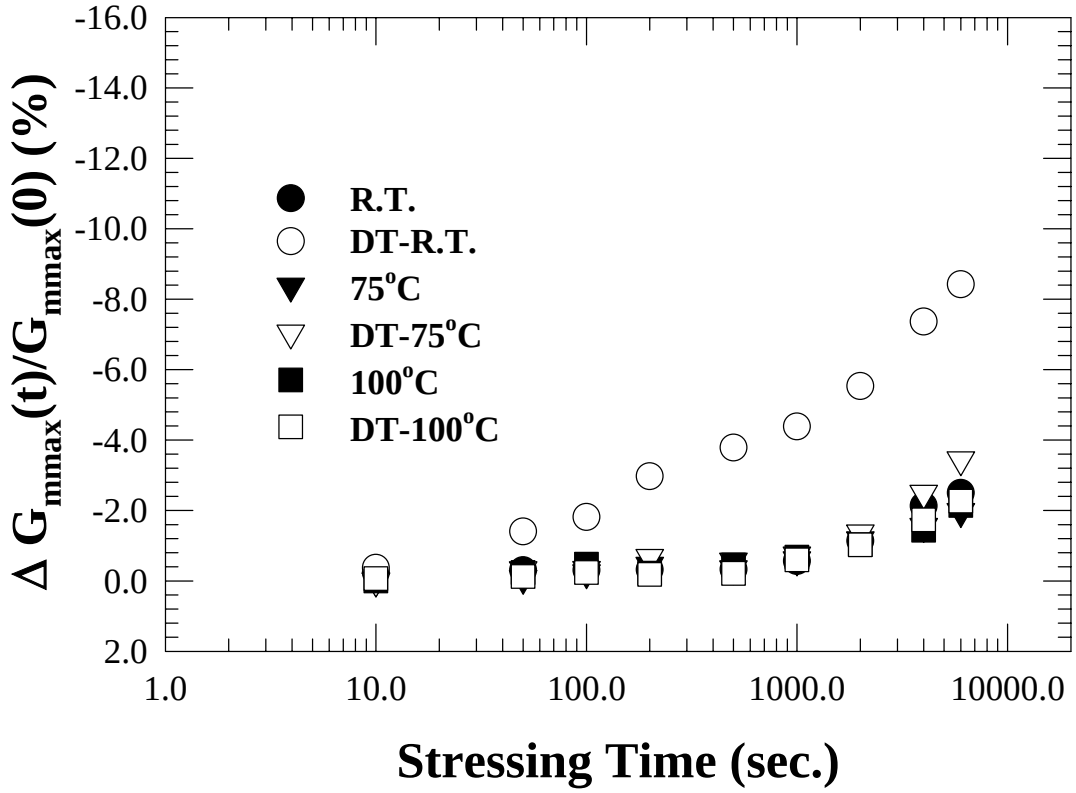


Fig. 3.10 Stress time dependence of G_{mmax} degradation for T-gate SOI pMOSFETs at various temperatures and operating under different modes. Devices were stressed at $V_G=V_{TH}$,V_D=-4.5 V. The vertical log scale is $G_{mmax}(t)/G_{mmax}(0)= [G_{mmax}(t)-G_{mmax}(0)]/G_{mmax}(0)$ for V_D=-0.1 V.

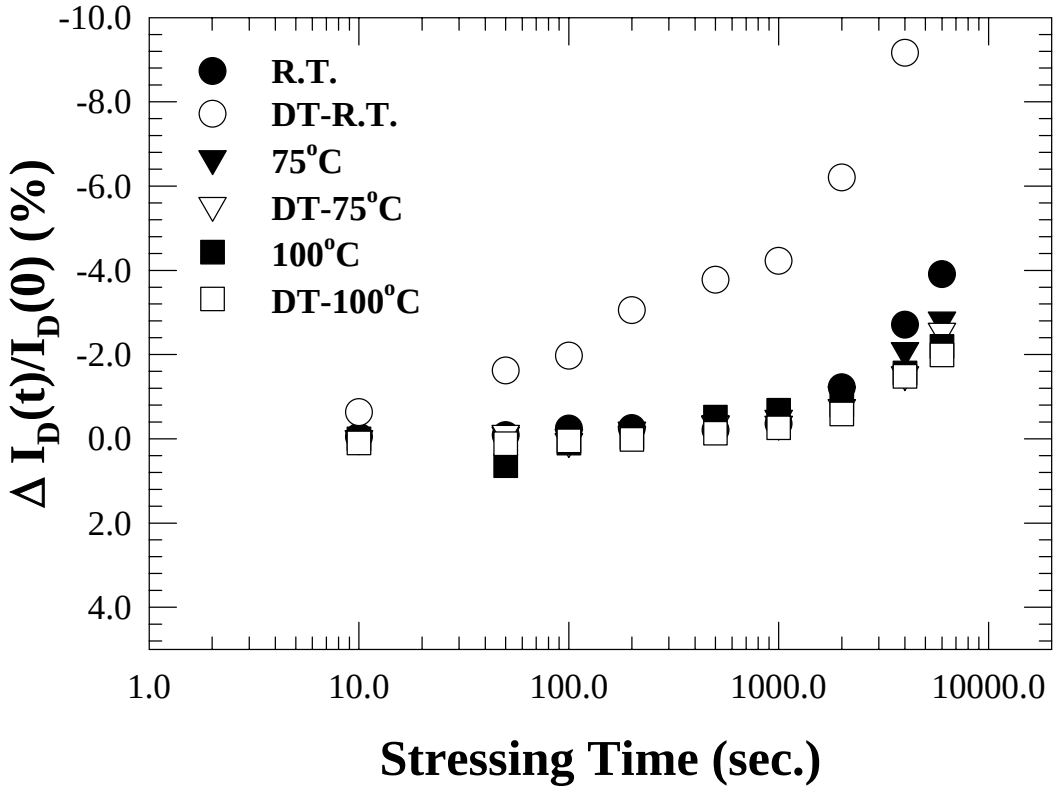
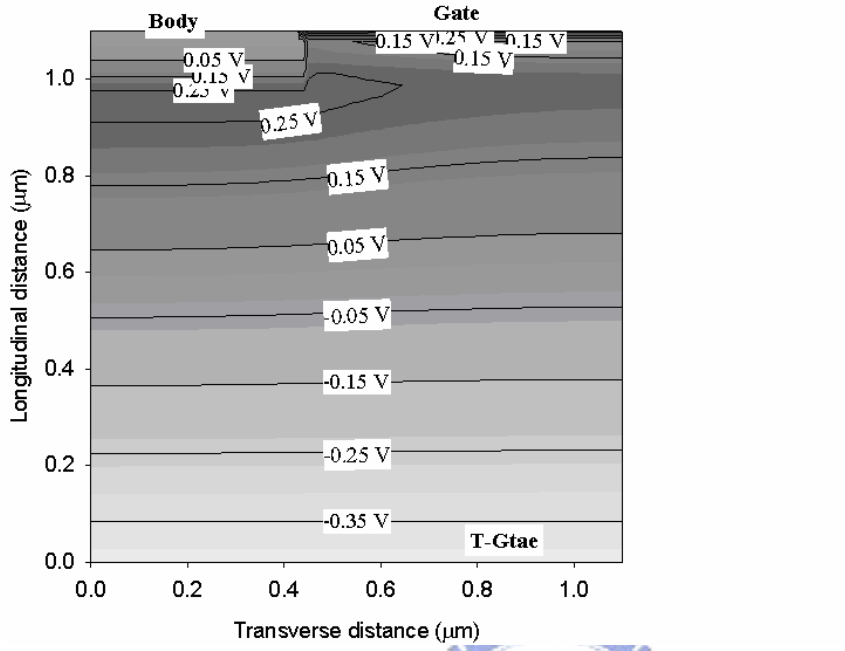


Fig. 3.11 Stress time dependence of drive current (measured at V_G=-0.7 V, V_D=-0.7 V) degradation for T-gate SOI pMOSFETs under both conventional and DT-modes. Devices were stressed at V_G=V_{TH}, V_D=-4.5 V, $\Delta I_{ON}/I_{ON}(0)= [I_{ON}(t)- I_{ON}(0)]/I_{ON}(0)$.



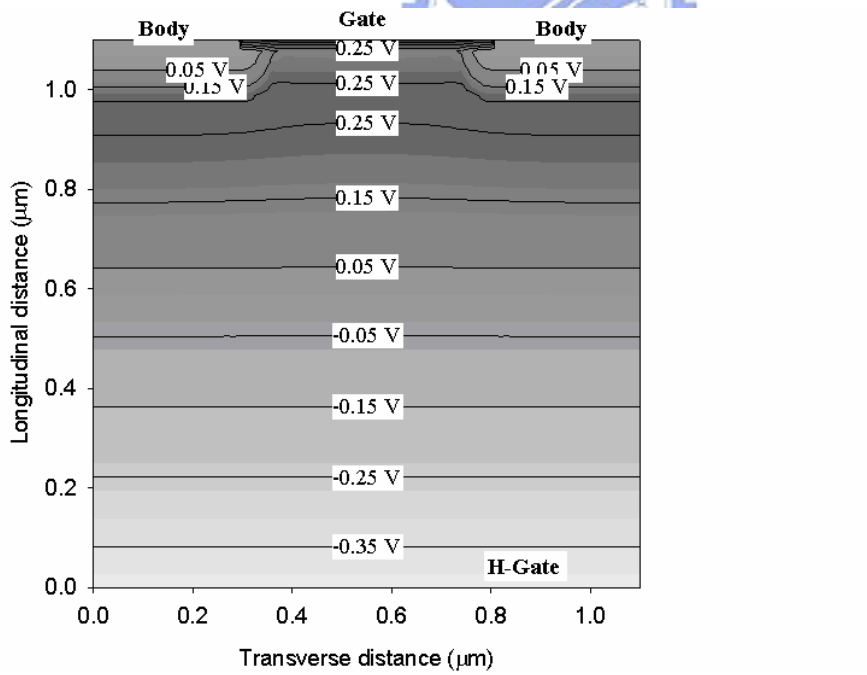


Fig. 3.12 (a) Simulation results of body potential contour distribution under DT mode for T-gate (along line aa', as shown in Fig. 1(b)), and (b) H-gate structures (along line bb', as shown in Fig. 1(c)).