國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

先進金氧半場效電晶體對於佈局之依賴效應

Layout Dependent Effect on Advanced MOSFETs

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中華民國九十六年三月

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國立交通大學

電子工程學系 電子研究所

博士論文

A Dissertation

Submitted to Department of Electronics Engineering &

Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of Doctor of Philosophy

in

Electronics Engineering

March 2007

Hsinchu, Taiwan, Republic of China

中華民國九十六年三月

先進金氧半場效電晶體對於佈局之依賴效應

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Abstract (in Chinese)

摘要

次 100 奈米先進互補金氧半技術中之金氧半場效電晶體對於佈局的依賴效應已經日趨明顯。本篇論文展示了兩個主要引起金氧半場效電晶體行為對於佈局依賴性的要素 - 製程引起的機械應力效應和井邊緣親近效應。

在製程引起的機械應力效應方面，第一點，本論文使用閘極長度為 65 奈米的先進互補金氧半技術完成了實驗之設計與執行。第二點，以包含種種機械應力來源並考慮全製程的數值運算完整的模擬了整個金氧半場效電晶體結構。第三點，提出了一個新的應力相依的摻雜擴散模型並將之加入於數值模擬軟體中，而模擬結果符合了矽晶片實驗實驗範圍內之金氧半場效電晶體的次臨限(subthreshold)特性。第四點，本論文探討了淺溝渠及熱氧化製程引起的機械應力和金氧半場效電晶體開狀態(on-state)對於佈局的依賴效應的關係，發展出一組精簡、可變化規模(scalable)的新積體電路模擬程式(SPICE)模型來解釋淺溝渠機械應力對金氧半場效電晶體性能的影響，並且成功預測晶片實驗中各條件的實驗結果。

本論文亦使用了次 100 奈米先進互補金氧半技術詳細探討了由離子佈植時邊界摻

雜散射引起的井邊緣親近效應。晶片實驗和技術電腦輔助設計(TCAD)模擬被用來從物理和製程的角度探討這個效應。蒙地卡羅離子散射模型和技術電腦輔助設計模擬提供了金氧半場效電晶體內部如何形成改變的物理了解。一個基於此物理了解的精簡新積體電路模擬程式模型被提出來並且以晶片實驗中各測試組結果完成此模型之校正。

Layout Dependent Effect on Advanced MOSFETs

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Abstract (in English)

The layout dependent effect on the MOSFETs characteristics has become more and more significant in advanced sub-100nm CMOS technologies. This dissertation demonstrates the experimental results, theories and modeling of two main factors making MOSFET behaviors layout dependent – process induced mechanical stress effect and well-edge proximity effect.

For the process induced mechanical stress effect, first, complete experiments are designed and conducted using novel CMOS technology with a minimum physical gate length of 65nm to investigate the mechanical stress effect. Second, full-process numerical simulations are performed for modeling complete MOSFET structures containing various mechanical stress sources. Third, a new stress-dependent dopant diffusion model is proposed and is implemented into the simulation software and the simulation results match MOSFET subthreshold characteristics of the silicon wafer experiment within the design space. Fourth, the

relationship between layout dependence of MOSFET on-state characteristics and mechanical stress caused by shallow trench isolation (STI) and thermal oxidation has been investigated, and a new compact and scaleable SPICE model accounting for the STI mechanical stress effect on MOSFET electrical performance is developed and successfully matches the experimental data under various conditions.

The well-edge proximity effect caused by the boundary dopant scattering during ion implantations is further explored using a sub-100nm CMOS technology in detail. TCAD simulations together with silicon wafer experiments have been conducted to investigate the impact of this effect from a physics and process perspective. The Monte Carlo ion scattering model and TCAD simulations provide a physical understanding of how the internal changes of the MOSFETs are formed. A new compact model for SPICE is proposed using physics-based understanding and has been calibrated using experimental silicon test sets.

Index Terms: dopant diffusion, mechanical stress, strain, shallow trench isolation, MOSFET, mobility, Well-Edge Proximity, ion scattering, SPICE, modeling and simulation

Acknowledgements

First of all, I would like to express my sincere gratitude to my advisor, Prof. Ming-Jer Chen, for his constant guidance and support during my doctorate studies. Moreover, I was also deeply affected by his passion and persistence on academic research.

I also wish to show my appreciation to all of the committee members, including, Prof. Lih-Juann Chen, Prof. Jenn-Gwo Hwu, Prof. Ya-Ming Lee, Prof. Tien-Sheng Chao, Dr. Chih-Sheng Chang, Prof. Tahui Wang, Prof. Horng-Chih Lin, and Prof. Ming-Jer Chen for their invaluable comments and suggestions.

I have been very lucky to work with such intelligent and experienced colleagues in Taiwan Semiconductor Manufacturing Company (TSMC) for many years. Especially, I would like to acknowledge Dr. Carlos H. Diaz, Dr. Chih-Sheng Chang, Dr. Ke-Wei Su, Dr. Sheng-Jier Yang, Dr. Huan-Tsung Huang, and Da-Wen Lin for frequently providing insightful opinions and stimulating discussions. My thanks also go to TSMC TCAD group members and my other colleagues who assist in the success of the experiments.

The electronics engineering department of NCTU has provided me not only the base knowledge for my research but also a truly delightful learning experience. I would like to express my appreciation to Prof. S. M. Sze, Prof. Long-Ing Chen, Prof. Ching-Yuan Wu, Prof. Shun-Tung Yen, and all of the scholars who helped expand my knowledge in their classes and lectures.

At last, I would like to thank my family for their never-ending support, love,

and encouragement throughout my whole life. This dissertation is dedicated to them.

謝誌

首先，誠摯的感謝指導教授陳明哲博士多年以來的細心指導及大力支持。除此之外，我深受老師對求學問的熱情與堅持所感動。

特別感謝論文口試委員陳力俊教授、胡振國教授、李雅明教授、趙天生教授、張智勝博士、汪大暉教授、林鴻志教授以及陳明哲教授在百忙之中給予寶貴的建議及指教。

很幸運的，能和台灣積體電路製造公司非常具有智慧及經驗的同事一起工作。其中，我特別要感謝 Carlos H. Diaz 博士、張智勝博士、蘇哲偉博士、楊勝傑博士、黃煥宗博士和林大文先生經常提供寶貴的意見及討論。在此，也要對台積電 TCAD 成員及其他對論文中實驗有幫助的同仁表達謝意。

交通大學電子工程研究所不僅提供我研究的基礎知識還有快樂的學習時光。課業上，感謝施敏教授、陳龍英教授、吳慶源教授、顏順通副教授及其他學者教授我豐富的知識及資訊。

最後，我要感謝我的家人長久以來支持、愛和鼓勵。這本論文，獻給他們。

Content (Index)

Table Captions

Chapter 2

Figure Captions

Chapter 1

Chapter 2

lines are the simulation without stress dependent diffusion model. Solid lines are the simulation with stress dependent diffusion model.

Fig. 2.9 Comparison of experimental and simulated nMOSFET V_G at different I_D level for various L_g and X_{active}. Minimum X_{active} for Lg=65nm is 0.6μm, for Lg=0.18μm is 0.74μm, and for Lg=0.42μm is 1μm. Final set of dopant diffusion parameters can model MOSFETs of different X_{active} under various drain voltages and substrate biases. Symbols stand for silicon data. Solid lines represent simulations with stress dependent diffusion model.

Fig. 2.10 Experimental and simulated threshold voltage dependence on X_{active} of (a) nMOSFET and (b) pMOSFET. nMOSFET threshold voltage, V_T, is more dependent on X_{active} than the p-type counterpart. Simulation with stress dependent diffusion model is able to describe stress induced V_T shift.

Fig. 2.11 Net doping contours for (a) X_{active}=10μm, no stress-dependent model, (b) X_{active}=10μm, with stress-dependent model, (c) X_{active}=0.6μm, no stress-dependent model, and (d) X_{active}=0.6μm, with stress-dependent model. For X_{active}=0.6μm, the source/drain junction is significantly shallower in the MOSFET core region when the stress-dependent diffusion model is turned on. The gate length is 65nm.

Fig. 2.12 Dopant profiles of (a) vertical direction for X_{active}=0.6μm nMOSFET, (b) vertical direction for X_{active}=10μm nMOSFET, (c) lateral direction for X_{active}=0.6μm nMOSFET, and (d) lateral direction for X_{active}=0.6μm nMOSFET. The vertical profiles are taken at gate edge and the lateral profiles are taken at 15nm deep cut-lines of the device. Solid lines are

simulation with stress-dependent diffusion model and dashed lines are without stress-dependent diffusion model. X_{active}=0.6μm with stress-dependent model device exhibits significant retardation of dopant diffusion.

Fig. 2.13 Experimental and simulated I_D-V_G curves for X_{active}=1.46μm. Symbols represent experimental data, dashed lines are the simulation results without considering stress-dependent diffusion models, and solid lines are the final simulated results including stress-dependent diffusion models.

Fig. 2.14 Simulated strain distribution in the silicon after entire front-end process for X_{active}=0.68μm. The total strain is in the MOSFET core region are compressive due to thermal gate oxidation and thermal mismatch between STI oxide and silicon.

Fig. 2.15 I_D values at V_G =-0.4 V for X_{active}=20.2 μm, X_{active}=1.46μm, and X_{active}=0.68μm. Symbols represent experimental data and solid lines are the final simulated results including stress-dependent diffusion models.

Fig. 2.16 Measured pMOSFET saturation threshold voltage versus the spacing between the nearby trench isolation sidewalls in the channel length direction. Also shown are those (lines) from the process-device coupled simulation with and without the strain induced activation energies.

Fig. 2.17 Uniaxial strain induced activation energy in the applied stress direction (parallel to the silicon surface) versus that normal to the silicon surface. The lines are from Eq. (2.14) and (2.15) for a literature range (Ref. [3.25]-[3.27]) of the activation volume and the migration strain anisotropy.

Also plotted are the data points from the underlying experiment and the existing *ab initio* calculations (Ref. [3.20], [3.29]).

Chapter 3

Chapter 4

Chapter 1
Introduction

1.1 Overview

During the last half of the previous century, the evolution of semiconductor technology became a major influence in the development of modern electronics. Developing a greater understanding of the function of both the positive and negative aspects of layout dependent effects such as the mechanical stress effect and the boundary ion implantation scattering effect is an essential part of device design and operation, and will no doubt continue to play an increasingly important role in the continuing evolution of the technology.

In Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSEFT) technology, layout dependent effects are inherently generated through the manufacturing processes, such as shallow trench isolation (STI), thermal oxidation, film deposition, and ion implantation scattering at the photoresist edges, which until recently were considered as a secondary effect. Moore's law states that the number of transistors that can be created in a specific space will approximately double for each successive generation (18~24 months), which means that, as the technology follows the predicted path, the mechanical stress effect becomes more severe and gains more importance and focus. The trend toward increasingly smaller device sizes combined with predictions by the ITRS [1.1], shown in Fig. 1.1, clearly illustrates the past achievements of the industry, and also suggests that this trend is likely to

continue to follow Moore's law for the foreseeable future.

Mechanical stress is the first effect being considered to make MOSFET layout dependent [1.2]-[1.5]. For some technologies, such as piezoresistive sensors and micro-electro-mechanical systems (MEMS), mechanical stress is a major feature of device operation. In the CMOS technologies, as the active area of each device is reduced, device designers are often forced to place the stress-generating sources closer together, with the influence of individual components often being superimposed upon each other, which, in turn, increases the magnitude of the mechanical stress. In addition, scaling rules also require MOSFET channel lengths to be reduced, thereby, accelerating the rate of increase in the average channel stress of the MOSFET, causing a significant impact on device performance that cannot be neglected [1.2]-[1.5]. Another aspect is that MOSFET performance can also be regarded as acting in a similar manner to Moore's law, increasing by ~15% per generation as, in the past, any improvement could be roughly achieved simply by scaling the length, oxide thickness and junction depth. The era of such simplicity has now dissipated as polysilicon gate depletion, gate oxide leakage, the quantum mechanical effect, and carrier scattering became more severe once the technology entered the sub-100nm regime. In this situation, mechanical stress is not only considered to be a by-product of the aggressive downscaling of device feature sizes, but, recently, has also been generated deliberately in order to improve MOSFET performance. Technologies, such as the inclusion of a cap layer with high-level intrinsic stress following the formation of source and drain [1.6], [1.7], strained

silicon epitaxy on a strain-relaxed SiGe [1.8], [1.9], and a lattice mis-matched source and drain using selective epitaxy of SiGe [1.10] or SiC [1.11], have been widely used to boost MOSFET drive currents. Fig. 1.2 illustrates a set of recent cross-sectional TEM pictures for a CMOSFET with 35nm gate lengths, which show that the mechanical strain improved the mobility of the NMOSFET by 40% and the PMOSFET by 100% when compared to the unstrained MOSFETs [1.12].

Any analysis of the influence of mechanical stress on a MOSFET can be divided into two categories: (1). Physical changes that occur during the device fabrication process and, (2). Energy band structure changes. Of the two most common physical changes, the first, crystal flaws, has been observed since the early stages of semiconductor technology. There are several types of defects that can be commonly observed in silicon crystal, which are usually classified from their dimensionalities, such as interstitial atoms and vacancies (point defects), dislocations (line defects), stacking faults and slip lines (area defects), and voids (volume defects). Point defects always exist in the crystals and are highly mobile, generated and eliminated with low energy barriers as temperature increases. Their distribution plays an important role in dopant diffusion and is also affected by mechanical stress. Line defects and area defects are generally unwanted and are produced under enormous levels of mechanical stress during the manufacturing process. These crystal flaws will induce a large unwanted leakage current, if they are located near the PN junctions (source and drain or wells), or damage the gate oxide of the MOSFET. Several papers [1.13]-[1.16] have reported that the crystal defects generated by the

mechanical stress produced a junction leakage current as a result of the scaling of the devices. Large volume defects in the crystal, such as voids, are detrimental, but are seldom observed nowadays since they are usually well-controlled in modern silicon crystal growth technology and are not easily generated during the CMOS manufacturing process. Instead, dopant clusters and precipitates have become an increasingly important type of volume defect due to high dopant concentration and shorter thermal annealing time.

Dopant diffusion changes under different magnitudes of stress represent the second most common physical change and have become more prominent recently as a result of increases in the magnitude of mechanical stress as the dimensions of the MOSFET are scaled down. Changes in dopant diffusion result in a difference in the final dopant distribution, which will be reflected in the changes in subthreshold behavior and short channel effects (SCE) in the MOSFET. One of the difficulties encountered in stress-dependent dopant diffusion studies is that it is hard to measure the 2-D dopant diffusion directly. Therefore, the methodology of inverse modeling [1.17], which makes use of the sensitivity of the MOSFET subthreshold current-voltage to 2-D dopant profile, is utilized in this dissertation.

The second category covers the resultant mechanical stress in the MOSFET, inducing a silicon energy band structure change, which, in turn, affects the carrier effective mass of the carrier, together with the mobility and the on-state drive current of the MOSFET [1.18]-[1.25]. Fig. 1.3 and 1.4 shows the simplified band structure changes with the mechanical stress for electrons and holes, respectively, adopted

from Ref.[1.21] and [1.25]. The benefit of improving carrier mobility using mechanical stress, rather than improving the gate dielectric constant, is that the loading capacitance will not increase.

The second effect making the highly scaled MOSFET characteristics layout dependent is the dopant scattering at photo-mask edge during the ion implantations. Recently, strong effects have been observed especially when CMOS wells are formed by using high energy ion implantations [1.26]-[1.30]. The effect of the well-edge proximity to the MOSFET gates was first reported by Hook [1.26] and originates from the lateral scattering of ion implantations at the photoresist edge when forming MOSFET wells, which in turn causes a change in the MOSFET threshold voltage. Fig. 1.5 shows the simulated two-dimensional dopant distribution contours and lateral doping profiles of B and P immediately below the silicon surfaces. The studies on this effect are still preliminary and the effect becomes of increasing importance as CMOS devices continue to shrink further.

1.2 TCAD modeling

Numerical simulation has been widely applied in many scientific and engineering fields. It has been utilized for the physical understanding of semiconductor technology development through physical understanding in semiconductors, and is named as Technology Computer-Aided Design, or TCAD. As the technology continues to be developed, TCAD has become of increasing importance for two main reasons. The first mainly is because both the process and

the device physics have become more and more complex. From the process perspective, except for mechanical stress increases during scaling, novel process flows, including multi-species ion implantations and extremely short thermal process times, cause the dopant diffusion behavior to greatly deviate from traditional diffusion laws. In such cases, it is difficult to predict the dopant distribution in the device simply by using empirical calculations. The dopant profiles can only be obtained by solving complex coupled equations, such as damage production, point defect annihilation, and the cluster effect between point defects and dopants.

The second reason is a result of the need for cost reductions by increasing the wafer size for mass production, so the cost of a single wafer for experimental purposes increases rapidly as the wafer diameter increases. Furthermore, the high process-complexity of nano-scaled CMOS technology makes the cost of a single experiment conditions even higher. Therefore, TCAD is needed to help comprehend the complex physical phenomena inside semiconductor devices, to predict the result from process conditions, and to decide the domain of the wafer experiment. In fact, it not only helps to reduce the cost, but also shortens the time taken to reach the mass production stage, since computer simulation time is generally much shorter than the wafer process times. With the development and addition of some remarkable computer capabilities, researchers are now able to quickly conduct "virtual experiments" using a computer before real experiments in silicon are performed, and they can aim for targets with smaller experiment domains.

One of the features of TCAD is based on numerical methods, such as

finite-differential and finite-element methods, which first establish the desired simulation structures (continuum) and divide the structures into diminutive elements and nodes using meshes. Then, basic physical equations are implemented and solved for the boundary conditions of each element and node, and a consistent result is obtained for the continuum. For process simulations, basic theories of dopant and defect diffusions, ion implantations, oxidation, and mechanical stress evolutions are solved. Fig. 1.6 shows the simulation results of dopant distribution in a MOSFET. After process simulation, device simulation is desired in order to determine the potential electrical behavior of the device. For device simulation, Poisson's equation, carrier drift-diffusion equations, tunneling equations and quantum effect approximation equations are solved according to terminal bias conditions. Fig. 4 shows the carrier distribution of the MOSFET.

As the rush toward the next generation of semiconductor technology gathers pace, the necessity for conducting experimental work, as well as numerical simulations, in order to realize the impact of layout dependent effects on scaled MOSFETs, has gained focus. The goal of this dissertation is to study the layout dependent effect by conducting experiments using nano-scaled MOSFET technology, and to perform numerical process and device simulations using TCAD tools to investigate the mechanical stress distribution, stress-dependent dopant diffusion, and boundary dopant scattering effects during ion implantations encountered in the MOSFET from a full process point of view, and to explain MOSFET behavior using the proposed physical-based models.

1.3 Dissertation Organization

Chapter two begins with an introduction to the theory and the experiments designed to explore dopant diffusion under mechanical stress. The implementation of the proposed stress-dependent diffusion model into the TCAD simulation tools, TSUPREM4 and MEDICI, is then presented. Three applications, stress dependent diffusion effect on the MOSFETs threshold voltage, stress dependent diffusion effect on the subthreshold leakage of the low dopant concentration well nMOSFET, and anisotropic diffusion under uniaxial strain are introduced in detail.

Chapter three discusses the influence of mechanical stress on the on-state behavior of the MOSFET. The change in structure of the energy-band, and the resulting impact on drive current for both n and pMOSFETs, is discussed. The implementation of a new model into SPICE that accounts for the mechanical stress effect is also proposed for the circuit design.

Chapter four first addresses the dopant scattering effect at well-mask edges on the modern MOSFETs by a designed wafer experiment. In-depth understanding is displayed using full process and device simulations of TCAD tools. Physic-based SPICE models is proposed and is validated with experimental data for better circuit simulation accuracies.

Finally, Chapter five offers a conclusion to the research, together with a summary of the accomplishments, and addresses future work to be extended to the topics of this dissertation.

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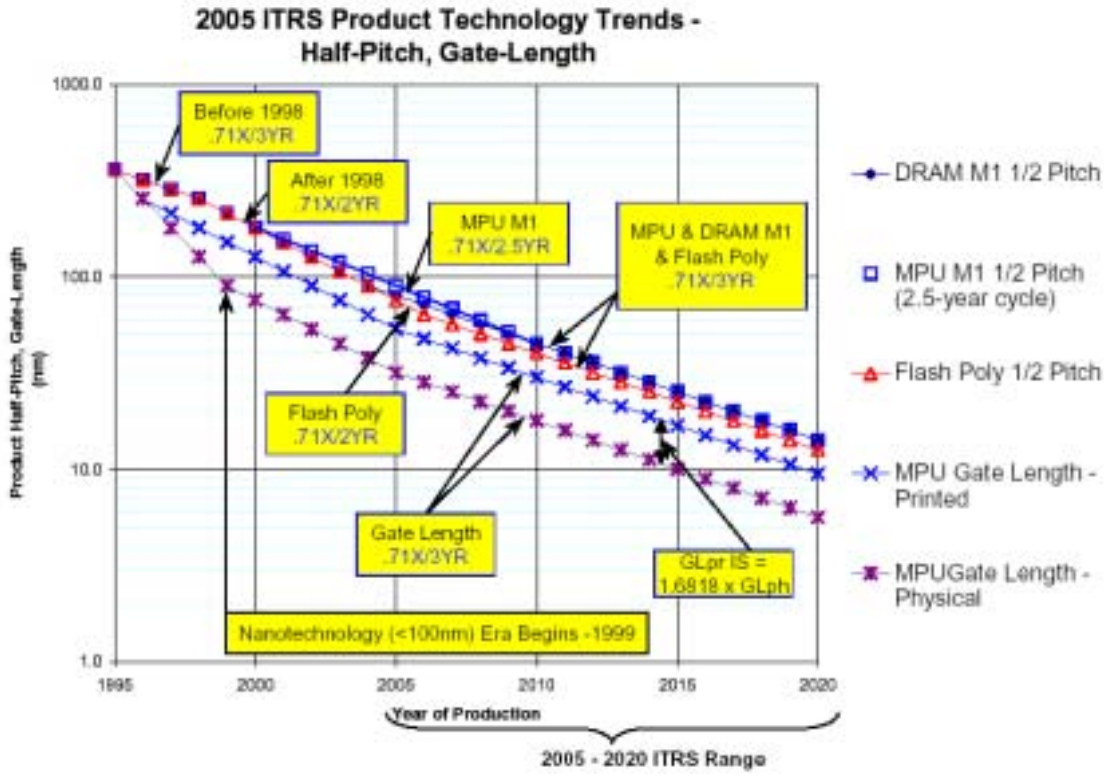


Fig. 1.1 Half pitch and gate length trends predicted by ITRS (adapted from Ref.[1.1]).

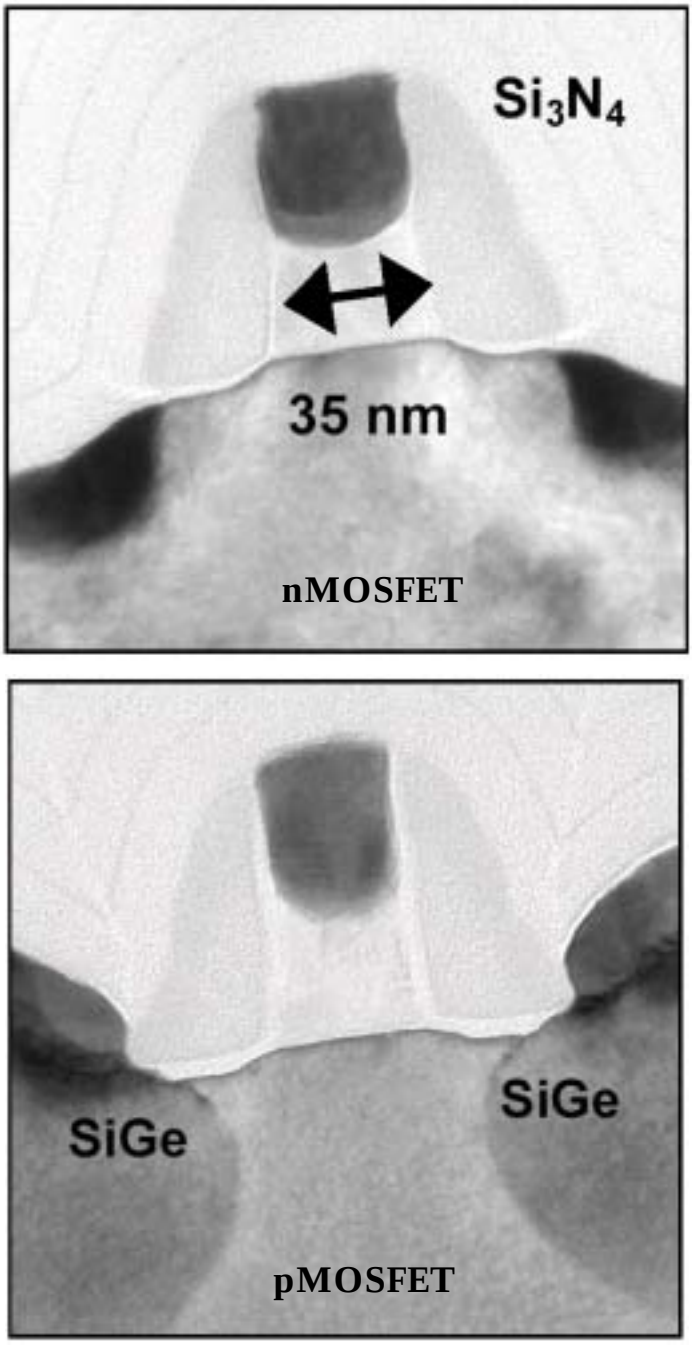


Fig. 1.2 TEM images of 35nm-gate-length MOSFETs using mechanical strained technologies (adapted from Ref.[1.12]).

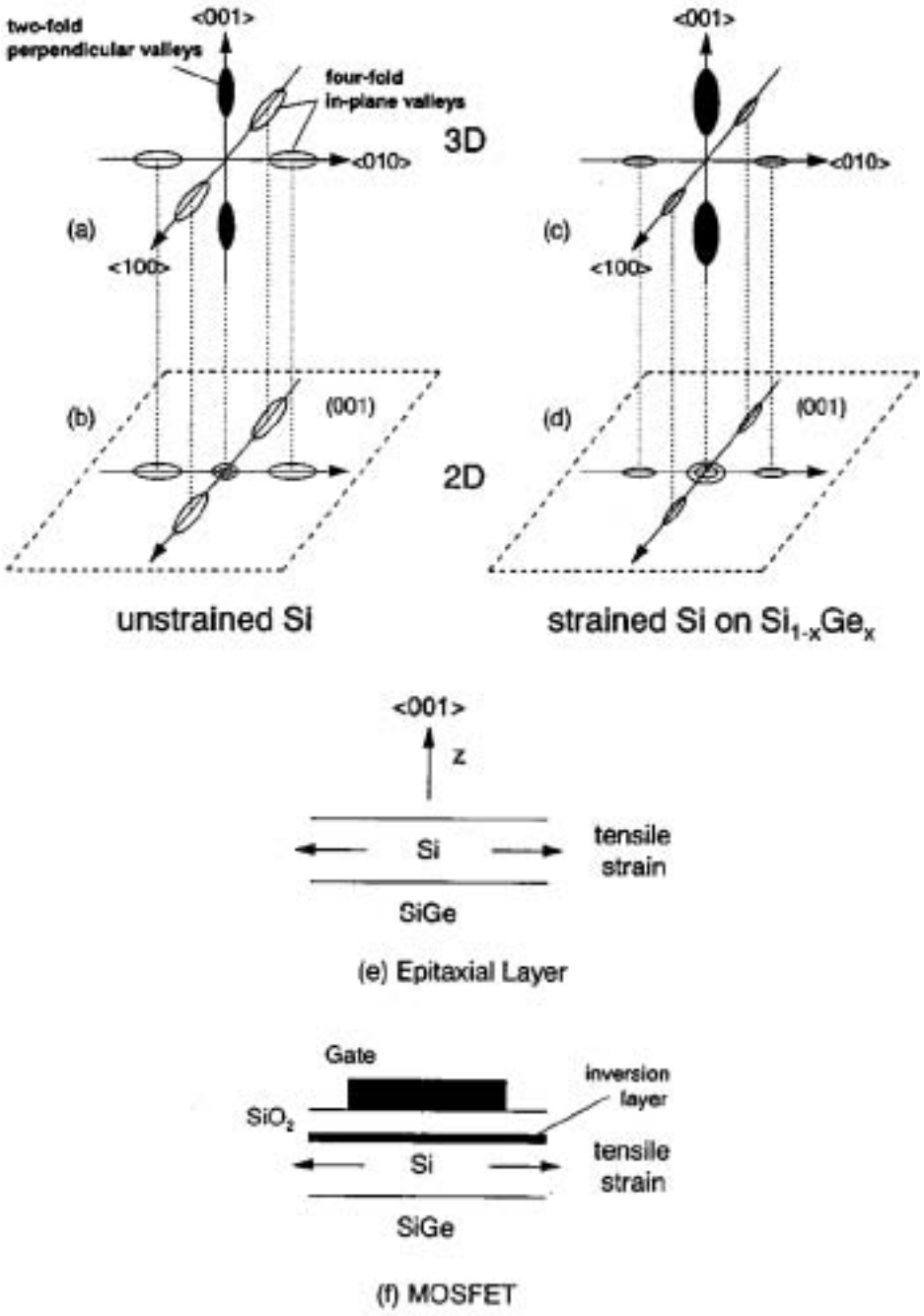


Fig. 1.3 Schematic representation of the constant-energy ellipses for (a) and (b) unstrained Si and (c) and (d) strained Si. (a) and (c) are for a 3DEG in bulk Si. (b) and (d) are those of a 2DEG in a Si inversion layer. (e) and (f) are the schematic diagrams for bulk strained Si and an inversion layer in strained Si, respectively. (adapted from Ref.[1.19]).

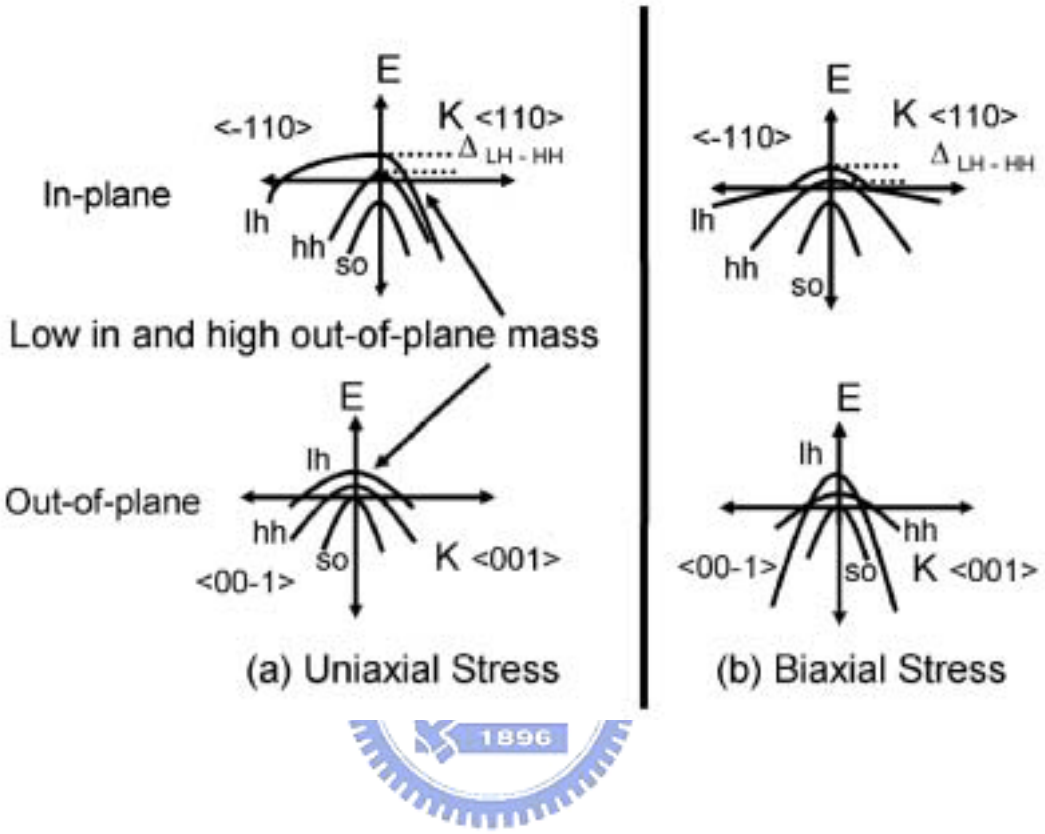
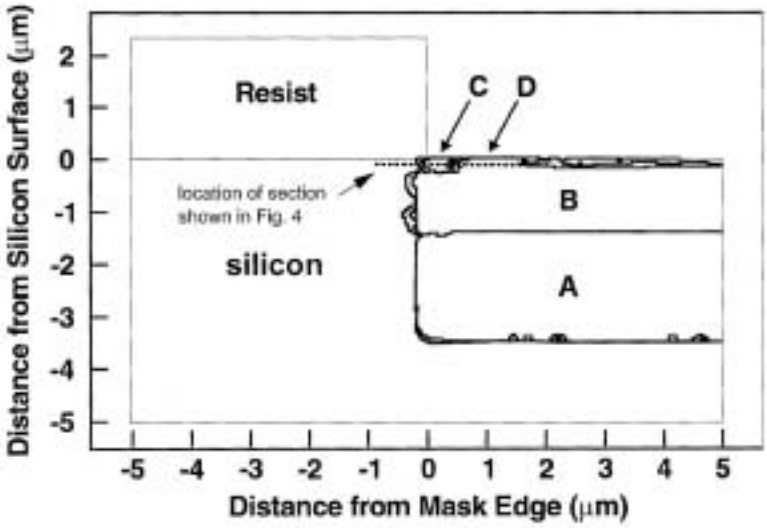
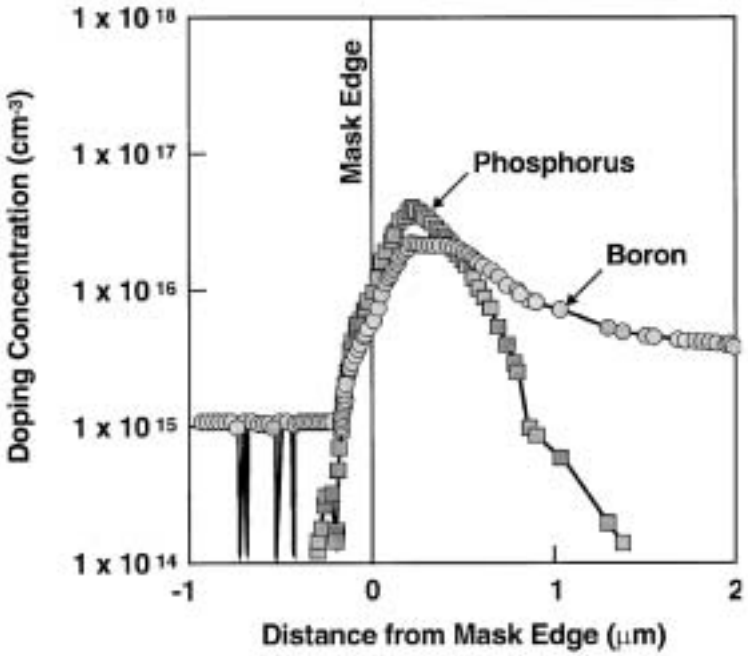


Fig. 1.4 Simplified valence band E vs. k diagram for strained Si (adapted from Ref.[1.25]).



(a) 2-D dopant concentration contour plot



(b) Dopant profiles of lateral cut line in the 2D contour plot

Fig. 1.5 (a) Contour plot of simulated doping near resist mask edge. Both boron (intermediate and near-surface) and phosphorus (deep) implantations were simulated. (b) Simulated lateral doping profiles of B and P immediately below the silicon surfaces (adapted from Ref.[1.12]).

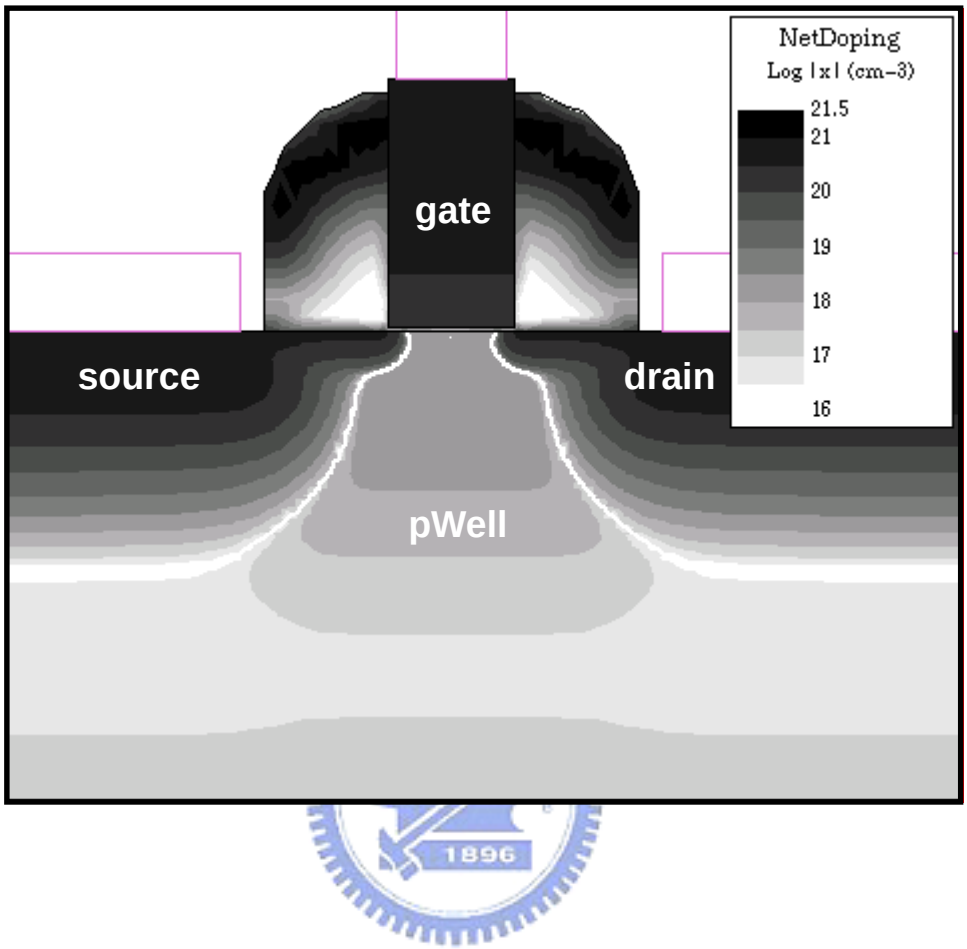


Fig. 1.6 Simulated dopant distribution contours of a novel MOSFET using a TCAD tool (TSURPEM4).

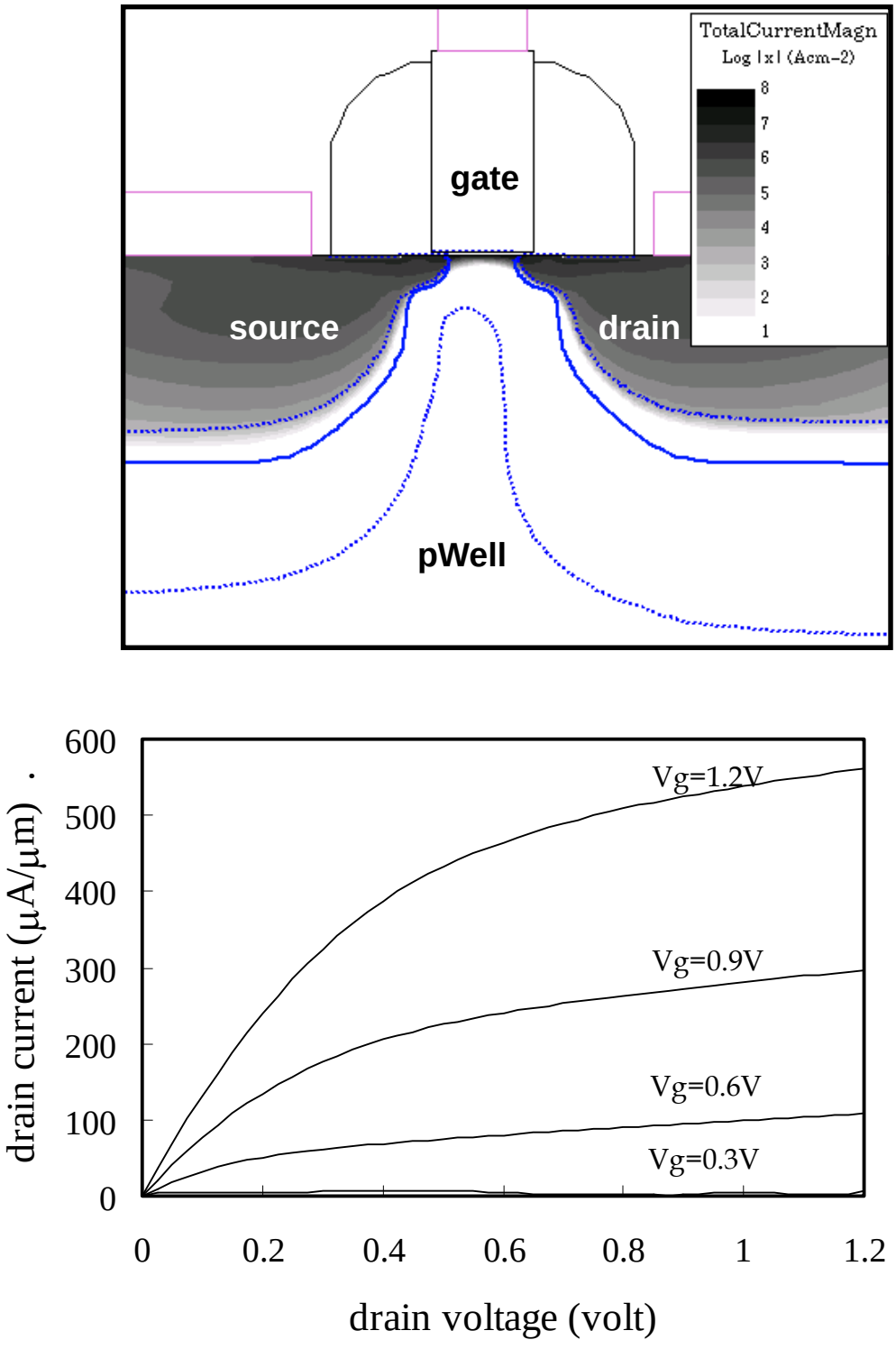


Fig. 1.7 Simulated (a) electrical current distribution contours and (b) output current-voltage plot of the MOSFET shown in Fig. 1.6.

Chapter 2

Dopant Diffusion Under Mechanical Stress

2.1 Preface

Shallow trench isolation (STI) induced mechanical stress increases in magnitude with reduced device active areas of highly scaled CMOS technology, causing a non-negligible impact on device performance [2.1]-[2.4]. Both experimental work and numerical simulations have been conducted to calculate the STI stress magnitude and distribution encountered in scaled MOSFETs [2.5]-[2.9]. The results show that the silicon stress level near the STI region is high. As design rules or layout dimensions scale down, the high-stress region encroaches further into the MOSFET channel. Thus, STI mechanical stress has a significant influence on state-of-the-art device performance.

Earlier work studying the mechanical stress effect has been focused on the MOSFET drive current shift, either in the form of localized or planar stress conditions [2.1]- [2.3], [2.6], [2.10]-[2.14]. Several studies have been performed to link STI mechanical stress to mobility changes while accounting for the observed current shift [2.2], [2.12], [2.13], although no threshold voltage shift mechanism has been investigated. G. Scott, *et al.* [2.14] have investigated both the drive current and threshold voltage shift, suggesting a difference in stress-induced diffusivity as the plausible origin of the threshold voltage shift. So far, however, there has been no further elaboration on this aspect. On the other hand, there has been a great deal of work devoted to dopant diffusion behavior in silicon under the influence of

mechanical stress [2.15]-[2.19]. Cowern, *et al.* [2.15] proposed a strain-induced dopant diffusivity model of boron diffusion in SiGe. S. T. Ahn, *et al.* [2.17] concluded that in the presence of high-stress nitride film, phosphorus diffusion in the silicon was retarded, whereas antimony diffusion was enhanced. Aziz [2.18] established a relationship between hydrostatic pressure and biaxial strain via thermodynamic formulation, while accommodating calculation of the activation energy shift due to strain. Based on Aziz's and Cowern's theoretical work [2.15], [2.18], Zangenberg, *et al.* [2.19] critically reviewed the findings over the past 10 years and further identified the strain effect on boron and phosphorus diffusion in SiGe. However, most studies in the area of mechanical stress induced dopant diffusion changes remain in fundamental research, i.e., at the silicon material level, and have not yet been extended to semiconductor device characterization and modeling.

It is well recognized that the key MOSFET parameters, such as threshold voltage, drain induced barrier lowering, body factor, and subthreshold swing, are all strongly dependent on dopant distribution details. Thus, it is crucial to examine stress-dependent dopant diffusion for scaled MOSFETs under mechanical stress.

In this chapter, a stress-dependent diffusion model and incorporate it into a two-dimensional process simulation environment to assess the doping distribution effect in scaled MOSFETs is presented. The proposed model is corroborated by extensive experimental data in a sub-100nm CMOS technology.

2.2 Stress-dependent Diffusion Model and Modeling Methodology

2.2.1 Model Description

The dopant diffusion change due to mechanical stress has been derived from point defect (interstitials and vacancies) changes [2.18]. Mechanical strain influences the point defect formation and migration, while the microscopic volume change and the pressure both contribute to the Gibb's free energy change. Thus, the dopant diffusivity ratio with and without strain can be expressed in an Arrhenius form; and the strain-induced point defect energy change can be translated to the dopant diffusivity change. For example, in the case of a compressively strained SiGe layer where Cowern studied boron diffusion [2.15], the stress condition is regarded as biaxial and the dopant diffusion dependence follows the Arrhenius form

$$D_S = D_A \exp\left[-\frac{sQ'}{kT}\right] \tag{2.1}$$

where D_S is the dopant diffusivity under strain, D_A is the dopant diffusivity without strain, s is the biaxial strain in the plane of the SiGe layer, and Q' is the activation energy per strain. The concept of this equation is consistent with experimental data [2.15], [2.18] and theoretical calculations [12)] showing a linear deffect of the mechanical strain to dopant diffusivity ratios on a log scale. Recently, Diebel [2.20] studied stress-dependent point defect equilibrium concentration and diffusion by means of *ab initio* calculations.

Analogous to equation (2.1), a stress dependent dopant diffusion model for dopant diffusion under STI mechanical stress, named Volume-change-ratio Induced Diffusion Activation Energy Shift Model (VIDAESM) is developed. The volume change ratio, V_{cr}, is a function of position due to non-uniform stress distributions. In this study, the MOSFET width is large enough to allow the three-dimensional stress effect to be reduced to the two-dimensional one. The activation energy involved is the product of a dopant dependent coefficient and volume change ratio, meaning that Eq. (2.1) can be re-written in the case of dopant diffusion under STI mechanical stress

$$D_S(T,x,y) = D_A(T)\exp\left[-\frac{\Delta E_S V_{cr}(T,x,y)}{kT}\right] \tag{2.2}$$

where D_S is the dopant diffusivity under strain, D_A is the dopant diffusivity without strain, V_{cr} is the volume change ratio due to stress, ΔE_S is the activation energy per volume change ratio depending on the dopant species, and T is the temperature. When the strain is small, the volume change ratio can be expressed as

$$V_{cr}(T,x,y) \cong \varepsilon_t(T,x,y) \equiv \varepsilon_{xx}(T,x,y) + \varepsilon_{yy}(T,x,y) + \varepsilon_{zz} \tag{2.3}$$

where ε_{xx} is the strain along the channel length direction, ε_{yy} is the strain in the direction perpendicular to the silicon surface, ε_{zz} is the strain along the channel width direction, and ε_t is the strain summation of ε_{xx}, ε_{yy}, and ε_{zz}. Note that ε_{zz} is zero in the two-dimensional simulation due to wide structures adopted. Therefore, Eq. (2.2)

becomes

$$D_S(T,x,y) = D_A(T)\exp\left[-\frac{\Delta E_S \varepsilon_t(T,x,y)}{kT}\right] \tag{2.4}$$

A two-dimensional numerical process simulator, TSUPREM4, is chosen to perform the process simulation. TSUPREM4 is capable of simulating intrinsic dopant diffusion, three-stream dopant-point defect pairing diffusion, oxidation enhanced diffusion effect, dopant clustering effect, and dislocation loop effect. For assessment of mechanical stress, the simulator also simultaneously solves force balance equations while taking into account thermal expansion, intrinsic stress, geometry re-arrangement after etch and deposition processes, and the thermal oxidation process [2.21]. The stress-dependent diffusion model, VIDAESM, has been incorporated into the simulator through the user-specified equation interface to adaptively calculate stress-dopant diffusivity during the process simulation.

2.2.2 Modeling Methodology

To model stress-dependent dopant diffusion for various stress levels, a series of MOSFETs with various active area sizes are designed and fabricated. Fig. 2.1 schematically shows the cross section view of a test device along the channel direction. The mechanical stress effect was explored here with active area size, X_{active}, and gate length L_g, both used as the main structural parameters.

The flow chart of the modeling procedure is shown in Fig. 2.2. Firstly, the

one-dimensional dopant profiles were processed using blanket control wafers, which covered the range of the process conditions of the device wafers. The results were then taken as stress-free dopant profiles and used to calibrate the dopant diffusion parameters without stress-dependent models.

Secondly, two-dimensional MOSFET structures were simulated using the mechanical stress model. Calibrated diffusion parameters were employed to simulate a large X_{active} MOSFET, where the stress level is low. All front-end major process steps from the STI to the source/drain anneal were considered. The corresponding simulation geometries were calibrated using TEM cross-sectional images. Some fine-tunings of two-dimensional dopant profile parameters, such as implant lateral straggles and segregation factors, are needed to fit the silicon device I-V characteristics. Fig. 2.3 shows the calibration result of a short channel nMOSFET I-V with a large X_{active}.

Next, with the stress distribution known, the stress-dependent diffusion models were introduced to simulate MOSFETs with varying X_{active} values. After implementing the stress-dependent diffusion model, process simulation results were used as device simulation inputs. MEDICI was chosen as the numerical device simulator. The device modeling parameters, such as carrier mobility, work function, and silicon/oxide interface charges were calibrated to fit the I-V of large X_{active} MOSFETs. Then, device simulations with various X_{active} values were performed and compared with silicon device data. The above procedure was iterated from process to device cycle until the current-voltage data was all satisfactorily reproduced in all

cases. The ΔE_S values from the previous work [2.15] were employed as the initial guess values. It is worth noting that the numerical convergence and simulation speed were not greatly influenced after implementing VIDAESM. The simulation time incorporating VIDAESM increases by about 7% compared to that without VIDAESM.

2.2.3 Experiment on MOSFET Threshold Voltages and Modeling Results

The silicon wafers were fabricated using novel CMOS processes. The control wafers for one-dimensional SIMS analysis were processed using the same thermal steps as device wafers. Fig. 2.4 displays SIMS results for both n and pMOSFET. The implant conditions were BF_2 2keV $1\times10^{15}cm^{-3}$ and As 2keV $1\times10^{15}cm^{-3}$ for ultra shallow junction calibration and the junction depths are around 260 angstroms for both devices by taking the substrate doping as $2\times10^{18}cm^{-3}$. The calibrated simulation profile is also plotted in Fig. 2.4. The calibration procedure included the fine-tuning of implant damage, dopant-point defect pairing diffusion, silicon-oxide dopant segregation, oxidation enhanced diffusion models, dopant clustering models, dopant-defect clustering models, and intrinsic diffusion models.

The stress simulation involved the main process steps, which are STI formation, gate oxidations, and poly-gate formation in sequence. Viscoelastic oxidation model was used to simulate the stress dependent oxide growth. The Young's moduli used were $1.87\times10^{12}dyne/cm^2$ for the silicon and $6.6\times10^{11}dyne/cm^2$ for the oxide layers. The intrinsic stress used is $-1.5\times10^{9}dyne/cm^2$ for the STI oxide and $3.3\times10^{8}dyne/cm^2$

for gate spacer oxide. The other parameters follow the default values in the TSUPREM4 manual [2.21]. The stress distribution results for different X_{active} values are given in Fig. 2.5. It can be seen that the polarity of the strain ε_{xx} in the lateral direction is negative, meaning that the MOSFET core area experiences a compressive stress. On the other hand, strain ε_{yy} in the vertical direction is tensile with a magnitude much smaller than ε_{xx}. In particular, Fig. 2.5(b) reveals that ε_{xx} drastically increases in magnitude with decreasing X_{active} values. Three reference points **A**, **B**, and **C** are chosen to inspect the value of the strain. **A** is at the center of the gate, **B** is 75nm away from the gate center and **C** is 150nm from the gate center. The depth of these points is 20nm from the silicon surface. Fig. 2.6 highlights the magnitude of the strain versus the X_{active} value at points **A**, **B**, and **C** in Fig. 2.5. The negative polarity of the strain means that the general strain conditions in the active area are compressive, and the magnitude increases rapidly as value of X_{active} decreases. The compressive stress mainly comes from lower thermal expansion rate of the STI oxide compared to silicon, and the thermal gate oxidation induced volume expansion at the STI edge. As X_{active} decreases, the STI approaches the MOSFET core region and increases the magnitude of compressive stress. The strain at rapid thermal peak temperature remains compressive and the magnitude is about 0.15% at the MOSFET core region for the minimum X_{active} case.

The MOSFET channel width in the silicon experiment was fixed at 10μm, large enough to ensure that the stress along the channel width direction is negligible. Simulations were conducted to evaluate the mechanical stress along the channel

width direction. The results showed that the average strain level for channel width W=10μm is around -0.02 %, which is at least two order of magnitude lower than the peak strain level used in this study. The MOSFET design set consisted of X_{active} values from 0.6μm to 10μm and L_g from 65nm to 0.42μm. It has been recognized that boron and phosphorus diffusion are retarded by compressive strain [2.15], [2.19], [2.22]. The stress simulation results show that the MOSFET channel stress and strain magnitudes for X_{active}=10μm are around -1×10^8 dyne/cm^2 and –0.04%, respectively. As the X_{active} value shrinks to 0.6μm, the corresponding stress and strain magnitudes become around -5×10^9 dyne/cm^2 and -0.4%, respectively. The compressive strain level in the channel region is quite close to the strain produced by 10% germanium in silicon, which falls within the range of Cowern's and Zangenberg's studies [2.15], [2.19].

In the present work, the impurities introduced to form nMOSFET are boron, indium, arsenic and phosphorus, while pMOSFET employed boron and arsenic. Boron, arsenic and phosphorus were all retarded by STI stress as encountered in fitting the silicon MOSFET I-V data. Indium was not considered as a fitting variable because it was observed to be almost immobile during the thermal process, meaning that dopant profile change due to mechanical stress would hardly be observed. As will be mentioned later, the nMOSFETs threshold voltage was observed to increase as the X_{active} value decreases. The subthreshold I-V with a low drain bias is strongly dependent on the accurate doping profile of the MOSFET shallow core region, which is mainly related to arsenic source/drain extension doping and boron halo doping.

In high drain bias cases, the subthreshold I-V depends significantly on the deeper part of the MOSFET doping profile, which is related to phosphorus source/drain, indium halo, and boron halo tail doping profiles. As the gate length varies, the extent of the superposition of tilt-implanted halo doping varies accordingly. Moreover, as the substrate bias increases in magnitude, the depletion region further extends into the substrate from the source, channel and drain regions, considerably influencing subthreshold I-V characteristics. Thus, biasing the MOSFET substrate can serve as a means of verification for the stress-dependent diffusion model. Fig. 2.7 shows the depletion region boundaries of a 65nm nMOSFET for low and high drain voltages.

After numerical iterations were completed, the effects of gate lengths, gate voltages, drain voltages, and substrate biases simultaneously matched with the nMOSFET subthreshold I-V data. This is sufficient to claim that the resulting dopant distributions for the whole device core region are correct. To assess the creditability of this model, device I-V simulations with and without VIDAESM were performed and compared. Fig. 2.8 shows the detailed I-V comparison for a small X_{active} MOSFET with and without VIDAESM. In the absence of VIDAESM, the simulation fails to correctly describe the I-V dependency on X_{active}. Fig. 2.9 displays a series of comparisons with measured gate voltage at different drain current levels for different combinations of gate lengths, active area sizes, drain voltages, and substrate biases. Remarkably, the extracted diffusion parameter set is able to reproduce all the silicon data well. The broad range of gate lengths, active areas,

drain voltages and substrate biases employed in this experiment confirm that the VIDAESM model is indeed suited for modeling the mechanical stress effect on scaled MOSFETs. To further ensure the extracted parameter set also valid for pMOSEFTs, threshold voltage dependence on X_{active} is simulated and compared with silicon data for both nMOSFETs and pMOSFETs. Fig. 2.10 shows the final results. The threshold voltage is defined by using constant drain current method. The strain effect is estimated to have less 10% drain current variations for L_g=65nm MOSFETs, which causes less then 4mV variations. It can be seen that the nMOSFET threshold voltage increases with decreasing X_{active} values while pMOSFET threshold voltage is relatively insensitive to X_{active}. The trends for both nMOSFETs and pMOSFETs are adequately described by the extracted parameter set.

Finally, Table I lists the extracted ΔE_S values for all impurities involved. The ΔE_S for phosphorus is -30eV per volume shift ratio and is largest among the impurities. The ΔE_S for arsenic is -14eV per volume shift ratio, whereas the ΔE_S for boron is -7eV. These coefficients confirm diffusion retardation by the compressive stress in pure silicon, excluding the Ge chemical effect in strained SiGe experiments. Fig. 2.11 illustrates the two-dimensional contour of the nMOSFET net doping concentration for a gate length of 65nm. As shown in the figure, for X_{active}=10μm, the dopant contours with and without the stress-dependent model are comparable, while the source/drain junction for X_{active}=0.6μm is significantly shallower and effective gate length is longer in the MOSFET core region when the stress-dependent diffusion model is introduced. To more clearly visualize the effect of the

stress-dependent model, one can inspect the dopant profile along specific cut-lines. Fig. 2.12 and 2.13 displays corresponding vertical and lateral doping profiles for a 65nm gate length nMOSFET with X_{active} as a parameter. As can be seen, significant dopant diffusion retardation prevails at small X_{active} values and this explains an increase in threshold voltage as the X_{active} decreases.

2.3 Experiment on MOSFET Subthreshold Leakage with Stress-Dependent Transient–Enhanced-Diffusion Effect Included

This work has been conducted to corroborate the validity of the STI mechanical stress-dependent diffusion model mentioned in section 2.2 using a MOSFET device with an underlying lightly doped well, which exhibits a significant mechanical stress effect on the subthreshold I-V characteristics. The stress-dependent point defect equilibrium concentration and diffusion, which dominates the transient enhanced diffusion (TED), has also been taken into account.

The results of Diebel's study [2.20] also show a linear dependence of both point defect equilibrium concentration and diffusivity in a log scale on the mechanical strain. Thus, it is reasonable to express the point defect equilibrium concentration and diffusion in an Arrhenius form:

$$C_S^*(T,x,y) = C_A^*(T)\exp\left[-\frac{\Delta E_C \varepsilon_t(T,x,y)}{kT}\right] \tag{2.5}$$

where C_S^* is the point defect equilibrium concentration under strain. To investigate the transient enhanced diffusion, only strain-dependent interstitial diffusion is needed. ΔE_C for the vacancy extracted from calculation results [2.20] is +7.9eV/unit strain. Extracted ΔE_C and ΔE_S (in Eq. (2.5)) values for the interstitial are –7.0 and +0.99eV/unit strain, respectively. Furthermore, interstitial diffusivity and equilibrium concentration product, $D_I C_I^*$, is reduced under the compressive strain conditions. Two-dimensional process/device simulators, TSUPREM4 and MEDICI, were employed. The stress-dependent diffusion models were incorporated into TSUPREM4 through its user-specified equation interface.

A series of n-channel MOSFETs were fabricated using state-of-the-art process technology. Test structures had three active area length (X_{active} in Fig. 2.1) values: 0.68μm, 1.46μm, and 20.2μm. X_{active} is the design parameter to modulate mechanical stress. The minimum X_{active} dimension of 0.68μm takes the presence of one contact window area in the source/drain into account. The gate length and width were 0.17μm and 10μm, respectively. The retrograde well implantations are omitted so as to enhance the sensitivity of the subthreshold characteristics to STI mechanical stress, offering the opportunity to verify the validity of the above mentioned diffusion model. The measured subthreshold I-V characteristics at V_D = 1.2V are depicted in Fig. 2.13, with the substrate bias as a parameter. Previous work [2.23] revealed that the substrate bias measurement is a suitable verification index of the MOSFET doping profile because of the high sensitivity of carrier diffusion current to the dopant profile. The procedure for obtaining ΔE_S values for various impurities began

by calibrating the one-dimensional dopant profiles in blanket control wafers, using processes that covered the range of device wafer process conditions. The results were taken as stress-free dopant profiles and used to calibrate the dopant diffusion parameters without considering stress-dependent diffusion effect. Two-dimensional MOSFET structures were then simulated in conjunction with the mechanical stress model. Calibrated diffusion parameters were employed to simulate a large X_{active} case, where the stress level is negligible. All major front-end process steps from the STI to the source/drain anneal were considered. The corresponding simulation geometries were calibrated using TEM cross-sectional images. Device simulations were performed and the device model parameters were calibrated to fit the I-V of the large X_{active} MOSFET. Next, the process simulations based on VIDAESM for all X_{active} values were conducted with an initial set of ΔE_S values. Then, the device simulations with smaller X_{active} values were performed and compared with the I-V data. The above procedure was iterated until a satisfactory reproduction of subthreshold I-V data was achieved in all cases.

The simulated strain distribution results for X_{active} = 0.68μm are given in Fig. 2.14. It can be seen that the magnitude of the total strain, or volume change ratio, ($\varepsilon_{xx}+\varepsilon_{yy}$), is negative in the MOSFET core area, meaning that the device experiences compressive stresses during the process. In addition, the ($\varepsilon_{xx}+\varepsilon_{yy}$) of X_{active} = 0.68 m was found to be much larger in magnitude than X_{active} = 20.2μm. The compressive stress stems mainly from the lower thermal expansion rate of the STI oxide when compared to silicon, as well as the thermal gate oxidation induced

volume expansion at the STI edge. Thus, as X_{active} decreases, the STI approaching the MOSFET core region increases the magnitude of the compressive stress. The extracted the ΔE_S for phosphorus, arsenic and boron in the last section are –30, –14, and –7 eV/unit strain, respectively. The negative sign of ΔE_S denotes diffusion retardation caused by the compressive stress in pure silicon for these impurities, and is in agreement with the literature [2.15],[2.19],[2.22]for boron and phosphorus. Note that, so far, no conclusive argument has been reached regarding the arsenic diffusion behavior under a general non-uniformly compressive stress in pure silicon.

In the MOSFET structure used in this section, source and drain phosphorus diffusion is much more sensitive to the mechanical stress than boron and arsenic because of the absence of the high concentration retrograde P-type doping well. The experimental silicon and simulation results are shown in Fig. 2.13 and Fig. 2.15. In the absence of the VIDAESM, the simulated leakage current (that is, the flat region in Fig. 2.14) was found to be much higher for MOSFETs with smaller X_{active} values as illustrated in dashed lines in Fig. 2.13. The I_D value for X_{active}= 1.46 μm at V_B = –1 V and V_G = –0.4 V is 2.5×10^{-10}A/μm without using VIDAESM, which is much larger than the result obtained using VIDAESM (6.3×10^{-11}A/μm). The corresponding silicon experimental data is 5.6 $\times10^{-11}$A/μm. The simulations that incorporated VIDAESM revealed that the punchthrough between the deeper part of the phosphorus source and drain is responsible for the leakage current. This means that the dopant diffusion becomes less as X_{active} is decreased, and is consistent with the results indicated in Fig. 2.15: a decrease in X_{active} produces a substantially large reduction in leakage current.

In Fig 2.15, the gate-edge tunneling current of X_{active} = 0.68μm MOSFET prevails in the background current, regardless of high negative substrate biases.

To investigate the impact of the mechanical stress on transient enhanced diffusion, the stress-dependent point defect diffusion and equilibrium concentration models described in Eqs. (2.4) and (2.5) are applied to the numerical simulator. The simulation results show slightly higher subthreshold leakage current, which implies that the dopant diffusion is the stronger. The I_D value for X_{active}= 1.46 μm at V_B = –1 V and V_G = –0.4 V increase from 6.3×10^{-10}A/μm to 7.1×10^{-10}A/μm. The explanation for this phenomenon is that the interstitial equilibrium concentration C_I^* decreases under the compressive stress and therefore the interstitial supersaturation factor, C_I / C_I^*, increases after impurity ion implantation, which results in the TED enhancement. The effect is not significant because high ramp rate rapid thermal anneals were applied after ion implantations. To further fit the experimental data after taking the stress-dependent TED effect into account, the final value ΔE_S of phosphorus is fine tuned from –30 to –33eV/unit strain. Fig 2.15 depicts the corresponding results of experimental data fitting.

2.4 Anisotropic Diffusion Derivation for Uniaxial Strain Cases

In this section, a new set of uniaxial-strain-dependent-anisotropic-diffusion equations is derived based on Aziz's theory. The equations will be implemented to the TCAD tool, TSUPREM4, and the simulation work was done to verify the silicon experiment with STI stressed PMOSFETs.

The thermodynamics framework constructed by Aziz (see Ref.[2.25], which is more recent and more thorough than the earlier works cited above), the activation volume ($\tilde{V}$) and the anisotropy of the migration volume ($\tilde{V}_{||}^{m} - \tilde{V}_{\perp}^{m}$) exist in nature. The combination of the activation energy, the activation volume, and the anisotropy of the migration volume is remarkable, as demonstrated in a physical model [2.18], [2.25]-[2.27] dedicated to both the hydrostatic pressure experiment and the in-plane biaxial stress experiment:

$$\tilde{V} + \frac{3}{2}\frac{Q'_{33-biax}}{Y_{biax}} = \pm\Omega + (\tilde{V}_{||}^{m} - \tilde{V}_{\perp}^{m}) \tag{2.6}$$

$$\tilde{V} + \frac{3}{2}\frac{Q'_{11-biax}}{Y_{biax}} = \pm\Omega - \frac{1}{2}(\tilde{V}_{||}^{m} - \tilde{V}_{\perp}^{m}) \tag{2.7}$$

where $Q'_{33-biax}$ is the biaxial strain induced activation energy in the direction normal to the silicon surface, Y_{biax} is the biaxial modulus, Ω is the lattice site volume, and $Q'_{11-biax}$ is the biaxial strain induced activation energy in the direction parallel to the surface.

On the other hand, in the case of uniaxial stress as encountered while fabricating the MOSFET, without the use of a relaxed SiGe buffer layer, the stress is created through the trench isolation, silicide, or cap layers in a manufacturing process. Therefore, a straightforward extension to the uniaxial strain counterpart is essential. The uniaxial model is derived and its linkage to the case of biaxial strain, Eqs. (2.6) and (2.7), is established. When applied to boron, a process-device coupled simulation is performed on a p-type MOSFET undergoing uniaxial stressing during

the manufacturing process, followed by a systematic assessment of the fundamental material parameters.

According to Aziz [2.18], [2.25], in the case of equilibrium or a quickly equilibrated point defect, the effect of stress on the dopant diffusivity in the direction normal to a (001) surface can be written as:

$$\frac{D_{33}(\sigma)}{D_{33}(0)} = \exp\left(\frac{\sigma \bullet [V^f + \tilde{V}_{33}^m]}{k_B T}\right) \tag{2.8}$$

Here the product of the stress tensor σ and the formation strain tensor V^f is the work done against the stress field in defect formation; the product of the stress tensor σ and the migration strain tensor $\tilde{V}_{33}^m$ is the work required for the successful transition in the migration path; k_B is Boltzmann's constant; and T is the diffusion temperature. The tensor V^f involves the creation or annihilation of a lattice site, followed by a relaxation process [2.18], [2.25]:

$$V^f = \pm\Omega \begin{bmatrix} 0 & & \\ & 0 & \\ & & 1 \end{bmatrix} + \frac{V^r}{3} \begin{bmatrix} 1 & & \\ & 1 & \\ & & 1 \end{bmatrix} \tag{2.9}$$

The + sign denotes vacancy formation and the – sign represents interstitial formation. The relaxation volume propagates elastically to all surfaces, resulting in a change in the volume of the crystal by an amount V^r. $\tilde{V}_{33}^m$ is expected to have the form [2.18], [2.25]:

$$\tilde{V}_{33}^m = \begin{bmatrix} \tilde{V}_{\perp}^m & & \\ & \tilde{V}_{\perp}^m & \\ & & \tilde{V}_{||}^m \end{bmatrix} \tag{2.10}$$

In Eq. (5), $\tilde{V}_{\perp}^{m}$ and $\tilde{V}_{||}^{m}$, respectively, reflect the dimension changes perpendicular and parallel to the direction of the net transport when the point defect reaches its saddle point [2.18], [2.25]. Aziz further defined the activation volume as the sum of the three diagonal elements of the formation strain tensor and the migration strain tensor, as expressed by:

$$\tilde{V} = \pm \Omega + V^{r} + 2\tilde{V}_{\perp}^{m} + \tilde{V}_{||}^{m}. \tag{2.11}$$

It is well recognized [2.20] that when applying a uniaxial stress in a certain direction parallel to the silicon surface, the solid will modify its shape in order to minimize the energy of the system. In other words, the solid will deform in such a way that each surface perpendicular to the applied stress direction becomes stress free. The underlying stress tensor therefore is

$$\sigma = \sigma_{uniax}\begin{bmatrix}1\\0\\0\end{bmatrix}. \tag{2.12}$$

On the basis of Hooke's law, σ_{uniax} in the linear elastic regime can be related to the uniaxial strain ε_{uniax} induced in the same direction: $\sigma_{uniax} = Y_{uniax}\varepsilon_{uniax}$, where the uniaxial modulus $Y_{uniax} = (C_{11} - 2\nu C_{12})$ with the Poisson's ratio $\nu = C_{12}/(C_{11} + C_{12})$. C_{11} and C_{12} are the elasticity constants. Analogous to previous work [2.15], the uniaxial strain induced activation energy in the direction normal to the (001) surface, $Q'_{33-uniax}$, can be linked to the underlying diffusivity:

$$\frac{D_{33}(\varepsilon_{uniax})}{D_{33}(0)} = \exp\left(-\frac{Q'_{33-uniax}\varepsilon_{uniax}}{k_B T}\right). \tag{2.13}$$

By combining Eqs. (2.9), (2.10), and (2.12) and equalizing (2.8) to (2.13), one

obtains $Q'_{33-uniax} / Y_{uniax} = -V^r/3 - \tilde{V}^m_{\perp}$. Again, by incorporating Eq. (2.11), the following expression is produced:

$$\tilde{V} + 3\frac{Q'_{33-uniax}}{Y_{uniax}} = \pm\Omega + (\tilde{V}^m_{||} - \tilde{V}^m_{\perp}) \tag{2.14}$$

It is then a straightforward task to derive the uniaxial strain induced activation energy $Q'_{11-uniax}$ in the applied stress direction: $Q'_{11-uniax} / Y_{uniax} = - V^r/3 - \tilde{V}^m_{||}$. Consequently, a similar model is achieved:

$$\tilde{V} + 3\frac{Q'_{11-uniax}}{Y_{uniax}} = \pm\Omega - 2(\tilde{V}^m_{||} - \tilde{V}^m_{\perp}) \tag{2.15}$$

Obviously, the uniaxial strain version is closely related to its biaxial counterpart: by comparing Eq. (2.6) and (2.14), $2Q'_{33-uniax} = (Y_{uniax} / Y_{biax})Q'_{33-biax}$ is obtained. Another equation expressing $Q'_{11-uniax}$ as a function of $Q'_{11-biax}$ and $Q'_{33-biax}$ can then be readily derived.

To produce the experimental parameters in terms of the anisotropy of the uniaxial strain induced activation energy, a uniaxial stress experiment was carried out in terms of a p-channel MOSFET in a state-of-the-art manufacturing process [2.24]. The channel length was maintained at 65 nm while changing the spacing in the channel length direction between the two trench isolation sidewalls. The structure schematic is detailed Fig. 2.1. Under such a situation, the channel zone encounters a compressive stress from the nearby trench isolation regions. The devices used are quite wide (10 μm), meaning that the stress in the channel width direction can be neglected. The (001) silicon surface is supposed to be stress free. This

hypothesis has been validated using the sophisticated simulations detailed in Ref.[2.24], which revealed that in the proximity of the silicon surface, the stress in the channel length direction is much larger in magnitude than that in the direction normal to the surface. Therefore, the proposed physical model can be adequately applied. The effect of changing the spacing between the two trench isolation regions in the channel length direction is reflected in the measured saturation threshold voltage as displayed in Fig. 2.16. The threshold voltage is defined by using constant drain current method. The positive shift in the saturation threshold voltage with increasing stress (via decreasing spacing between the trench isolation regions) shown in Fig. 2.16 can be attributed to the retarded boron diffusion.

A two-dimensional process-device coupled simulation, as detailed in Ref.[2.24], was slightly modified by taking the anisotropy of the boron diffusivity into account:

$$\frac{D_{33}(\varepsilon_t)}{D_{33}(0)} = \exp(-\frac{Q'_{33-TCAD}\varepsilon_t}{k_B T}) \tag{2.16}$$

$$\frac{D_{11}(\varepsilon_t)}{D_{11}(0)} = \exp(-\frac{Q'_{11-TCAD}\varepsilon_t}{k_B T}) \tag{2.17}$$

According to the work in [2.24], the total strain ε_t is the sum of the three strain components: ε_{xx} in the channel length direction, ε_{yy} in the channel width direction, and ε_{zz} in the direction normal to the silicon surface. From the simulated strain distributions, $\varepsilon_t \sim \varepsilon_{xx}$, leading to $Q'_{33-TCAD} \approx Q'_{33-uniax}$ and $Q'_{11-TCAD} \approx Q'_{11-uniax}$. The simulated saturation threshold voltages for different values of $Q'_{33-uniax}$ and $Q'_{11-uniax}$ are plotted in Fig. 2.16 for comparison. The figure clearly exhibits that (i) the largest

deviation occurs at $Q'_{33-uniax} = 0$ and $Q'_{11-uniax} = 0$, the case of no stress dependencies; (ii) the most accurate reproduction is achieved with the anisotropic activation energies, rather than the isotropic variety; and (iii) the anisotropy of the activation energy must be adequate, that is, $Q'_{11-uniax} = -7$ eV per unit strain and $Q'_{33-uniax} = -3.5$ eV per unit strain are more favorable than $Q'_{11-uniax} = -3.5$ eV per unit strain and $Q'_{33-uniax} = -7$ eV per unit strain.

Prior to determining the fundamental material parameters, a systematic treatment, such as that indicated in Fig. 2.17, is demanded. In Fig. 2.17 a series of straight lines of $Q'_{11-uniax}$ versus $Q'_{33-uniax}$ are from Eq. (2.16) and (2.17) for a literature range [2.25]-[2.27] of $\tilde{V}$ and the migration strain anisotropy $\tilde{A}$ ($\equiv(\tilde{V}^m_{||} - \tilde{V}^m_{\perp})/\Omega$) [2.25]. In the calculation procedure, the following literature values were employed [2.28]: (i) C_{11} = 168 GPa and C_{12} = 65 GPa, giving rise to Y_{uniax} = 131 GPa and ν = 0.28; and (ii) $\Omega = 2.26\times10^{-23}$ cm^3. The above experimental parameters are also added to the figure. From the figure a set of $\tilde{V}$ and $\tilde{A}$ can be clearly located around the data point. On the other hand, uncertainties exist based on a series of literature data: $\tilde{V} = (-0.16 \pm 0.05)\ \Omega$ [2.25]. Taking such uncertainties into account, Fig. 2.17 reveals that the data point does match the upper limit, that is, $\tilde{V} = -0.21\ \Omega$. The corresponding $\tilde{V}^m_{||} - \tilde{V}^m_{\perp}$ in the vicinity of 0.15 Ω is determined accordingly, falling within the reasonable range [2.25]-[2.27]. Such corroborating experimental evidence further indicates that the transient enhanced diffusion effect is relatively insignificant when compared to the long-term diffusion times in the underlying manufacturing

process. Under such circumstances, the point defect is rapidly equilibrated relative to the entire diffusion time.

Finally, the existing *ab initio* calculations is quoted [2.20], [2.29]: $Q'_{11-biax}$ = –19.2 eV per unit strain and $Q'_{33-biax}$ = –13.9 eV per unit strain, which were transformed via the aforementioned relationship into the equivalent $Q'_{11-uniax}$ of – 8.77 eV per unit strain and $Q'_{33-uniax}$ of – 4.975 eV per unit strain. In this process, the Y_{biax} used was equal to 183 GPa according to $Y_{biax} = (C_{11} + C_{12} - \nu C_{12})$ with its Poisson's ratio $\nu = 2C_{12}/C_{11}$. Evidently, the two data points are quite comparable to each other, as displayed in Fig. 2.17.

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Tab. 2.1

Impurity ΔE_S extracted in the study

Impurity	Boron	Phosphorus	Arsenic
ΔE_S(eV/volume shift ratio)	-7	-30	-14

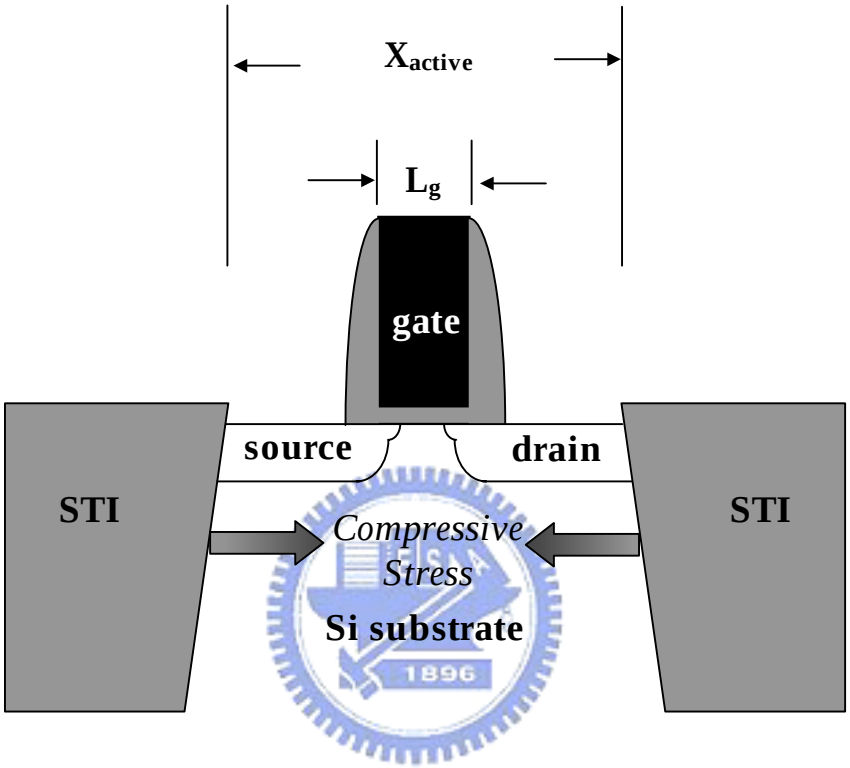


Fig. 2.1 Schematic cross section of the device along channel length direction with active area size X_{active} and gate length L_g both as parameters. The stress condition is compressive mainly because of the lower thermal expansion rate of STI oxide compared to silicon, and the thermal gate oxidation induced volume expansion at the STI edge.

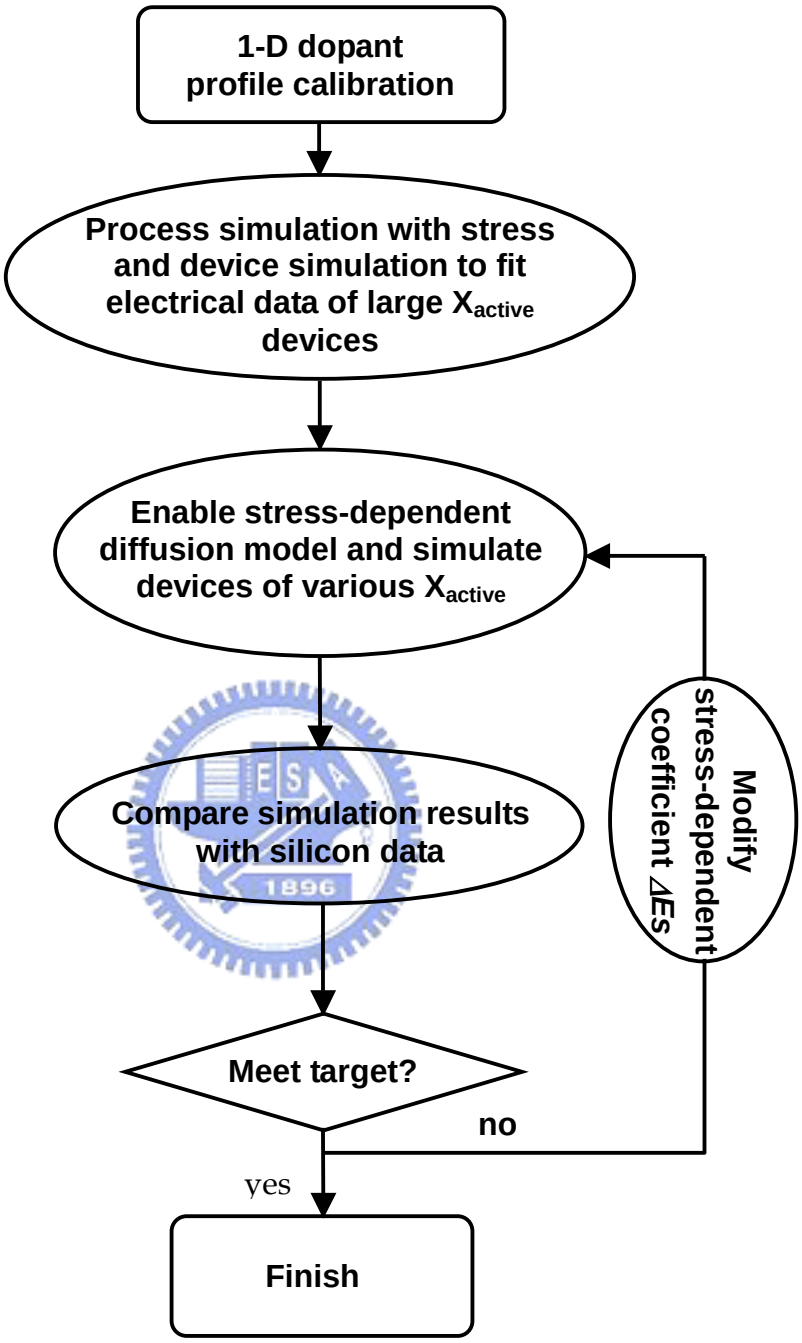
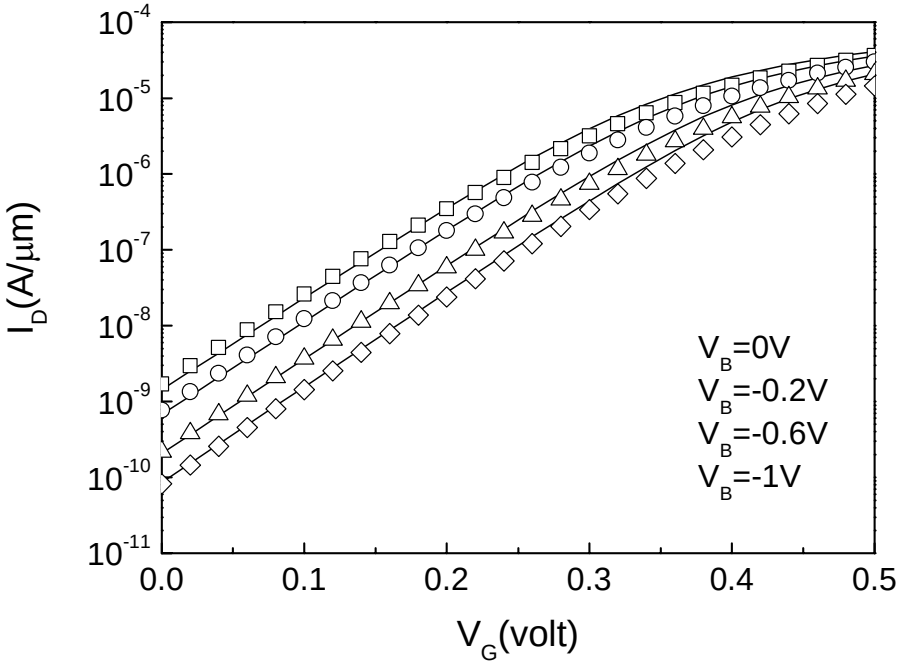
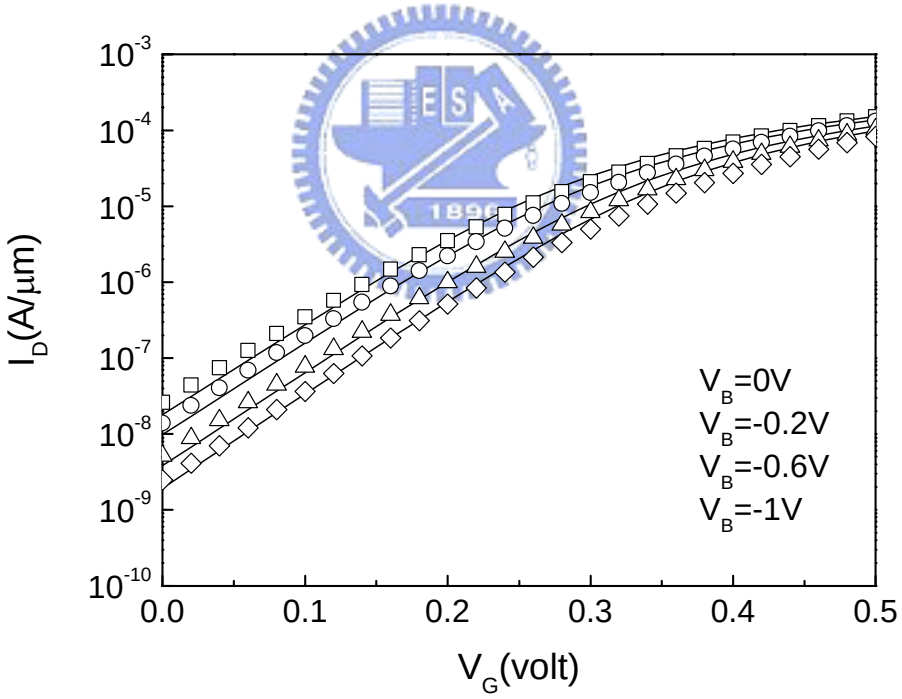


Fig. 2.2 Flow chart of the modeling procedure.

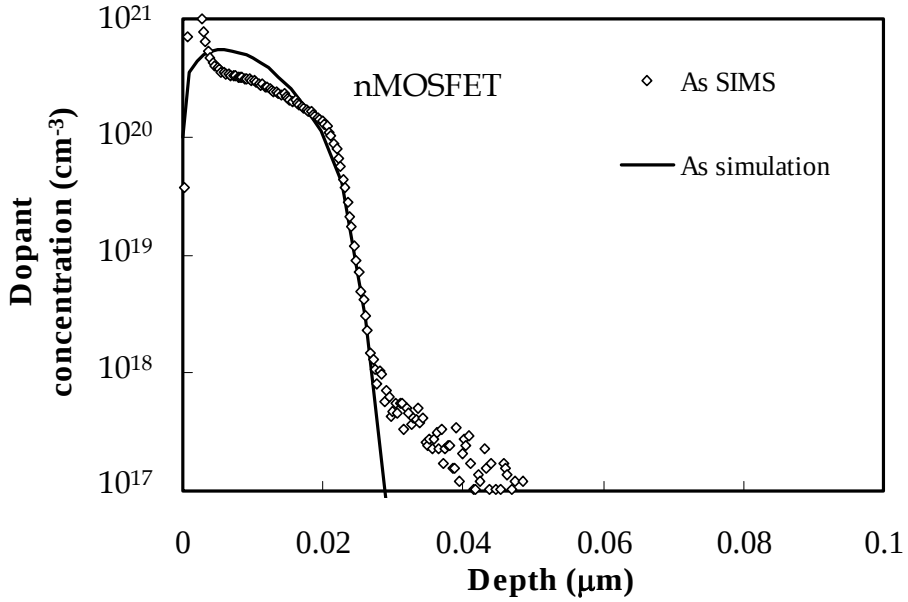


(a) L_g=65nm, X_{active}=10μm, V_D=0.05V

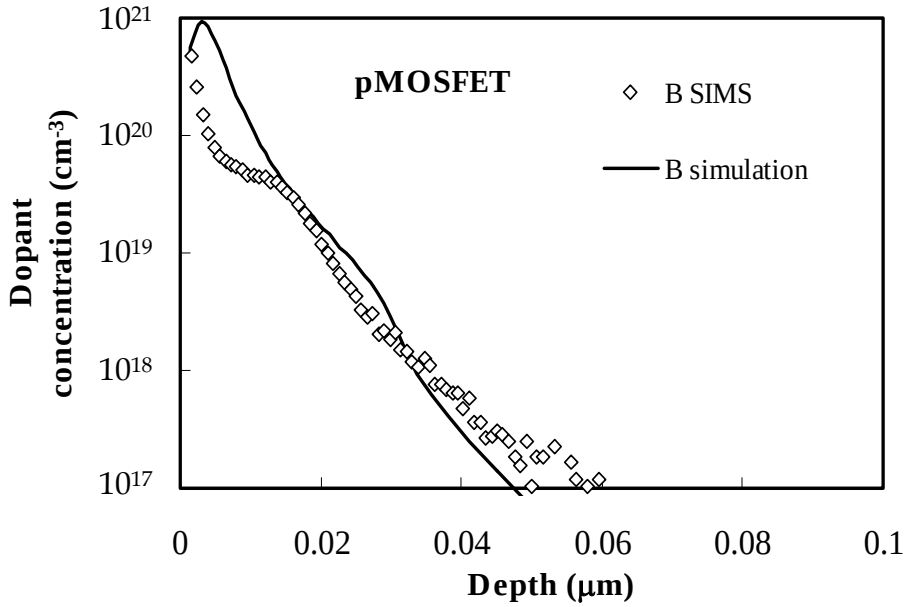


(b) L_g=65nm, X_{active}=10μm, V_D=1V

Fig. 2.3 I-V calibration result of a short channel nMOSFET with large X_{active} for (a) V_D=0.05V and (b) V_D=1V. Lg=65nm and X_{active}=10μm. Symbols stand for the silicon data. Solid lines are the calibrated simulation result.

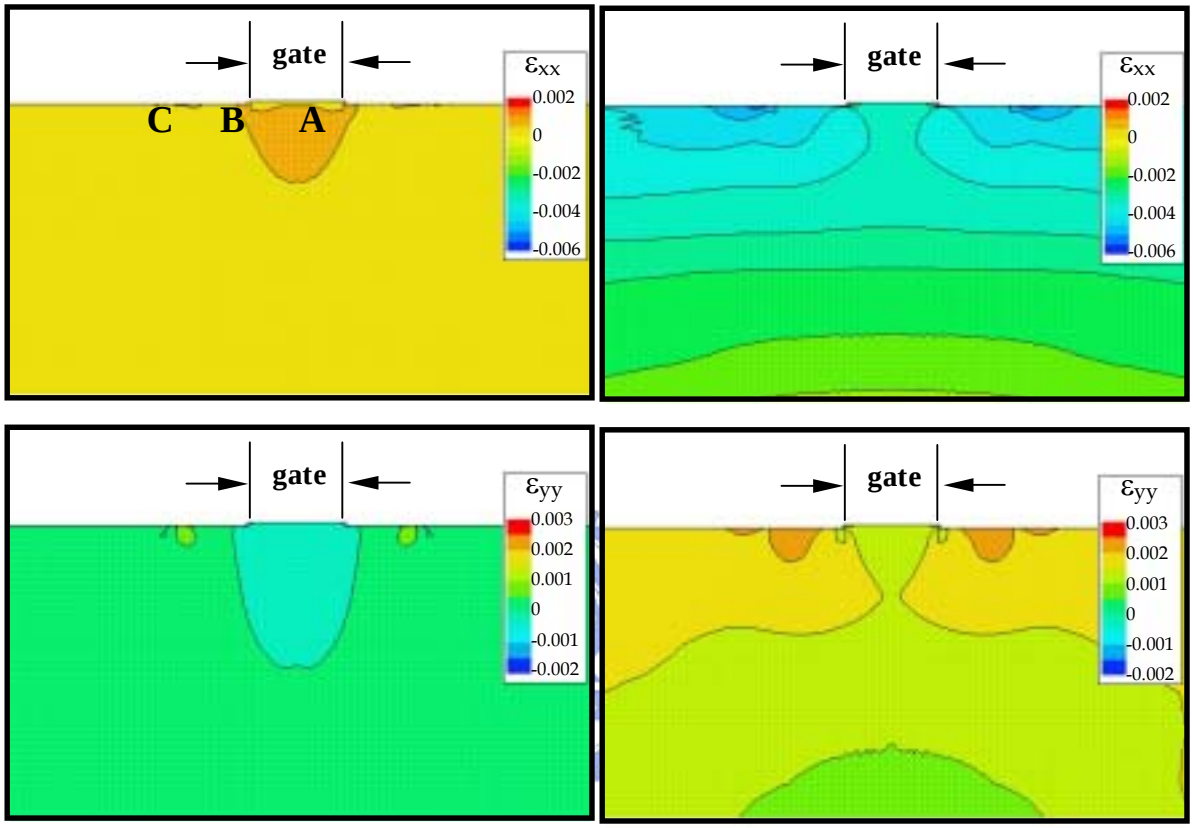


(a) nMOSFET



(b) pMOSFET

Fig. 2.4 SIMS and calibration results of one-dimensional dopant profile for (a) nMOSFET and (b) pMOSFET.



(a) X_{active} = 10μm (b) X_{active} = 0.6μm

Fig. 2.5 Simulated strain distribution in the silicon of entire front-end process for Lg=65nm and (a) X_{active}=10μm and (b) X_{active}=0.6μm. A small X_{active} causes a much higher strain.

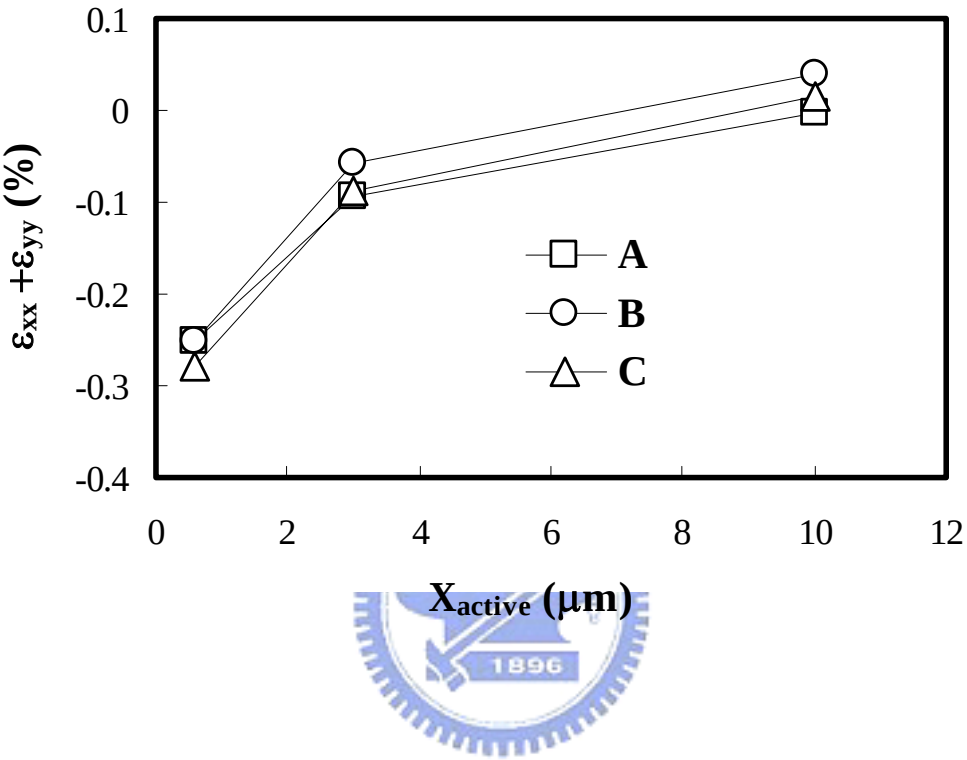
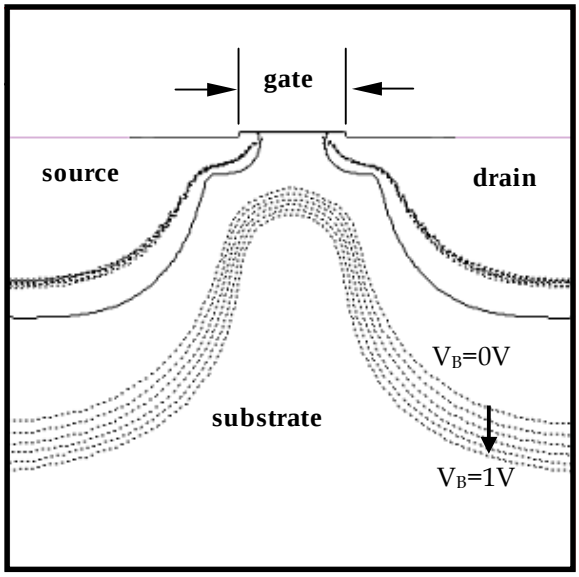
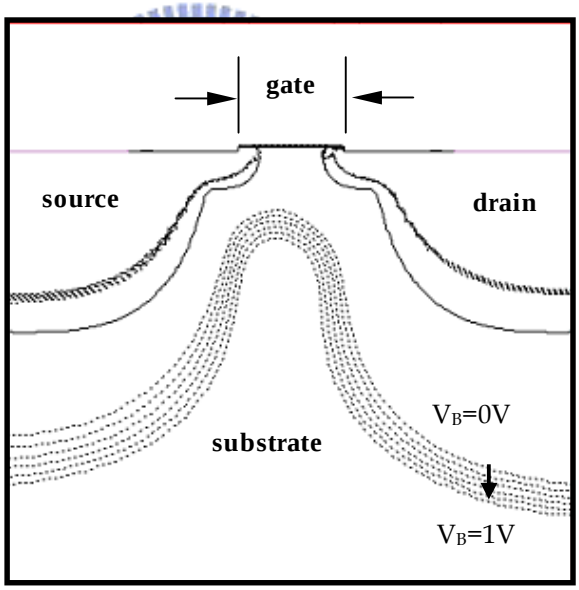


Fig. 2.6 The magnitude of strain versus X_{active} corresponding to three points **A**, **B**, and **C** in Fig. 2.5.

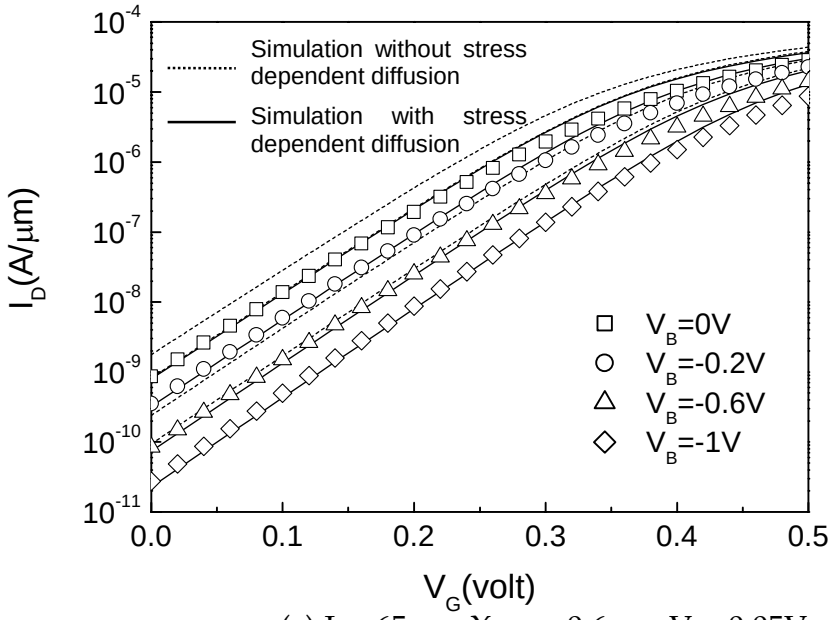


(a) V_D=0.05 V

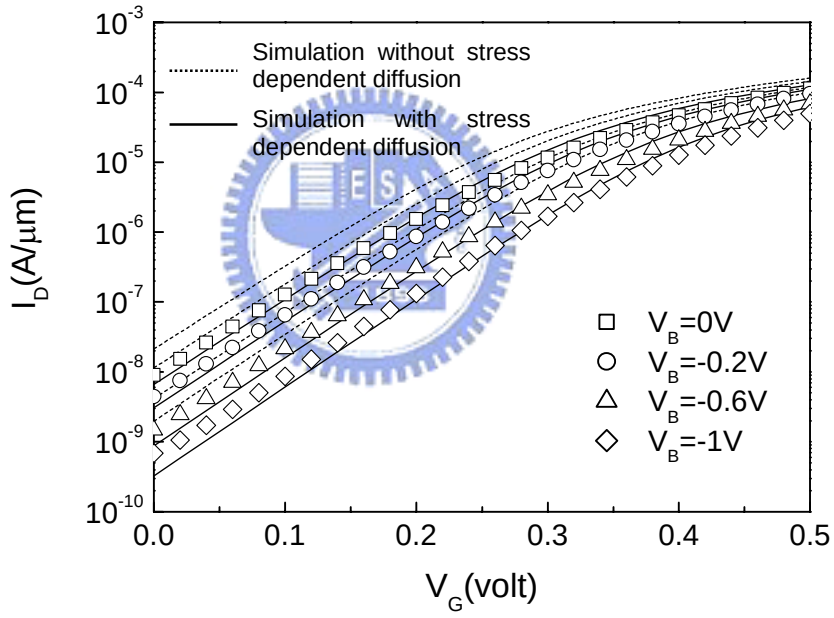


(b) V_D=1 V

Fig. 2.7 The depletion region boundaries with substrate bias, V_B, for 65nm nMOSFET at (a) V_D=0.05V and (b) V_D=1V.

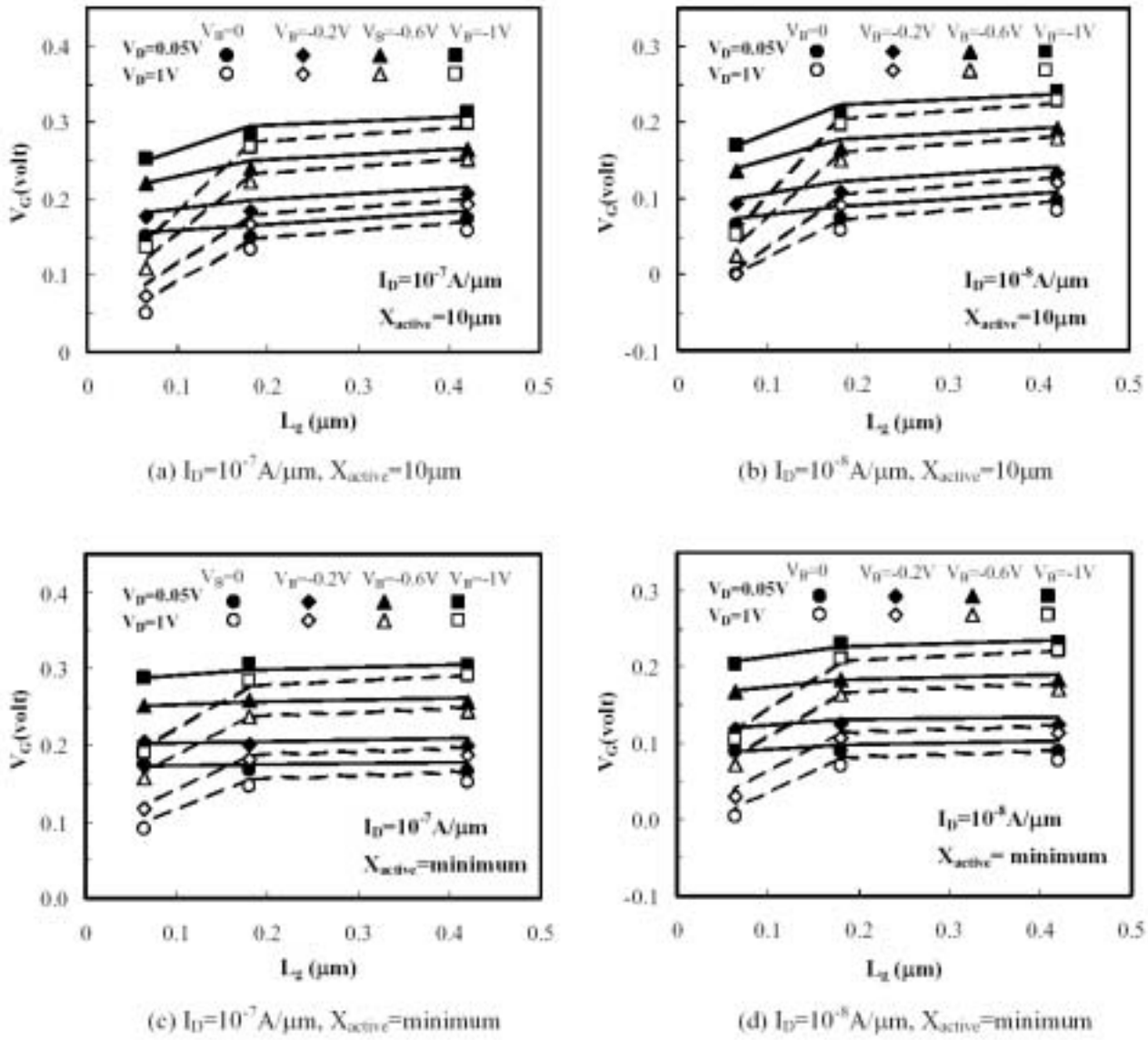


(a) L_g=65nm, X_{active}=0.6μm, V_D=0.05V



(b) L_g=65nm, X_{active}=0.6μm, V_D=1V

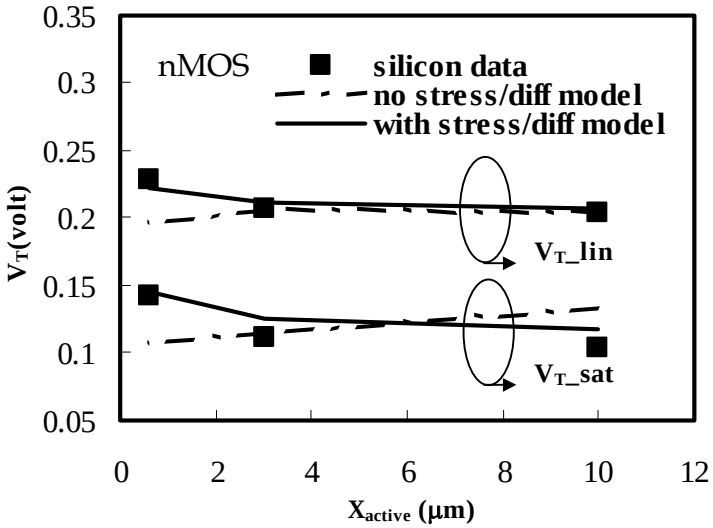
Fig. 2.8 I-V comparison among experimental data, simulation without stress-dependent diffusion model, and simulation with stress-dependent diffusion model for a small X_{active} MOSFET at (a) V_D=0.05V and (b) V_D=1V. L_g=65nm and X_{active}=0.6μm. Symbols stand for the silicon data. Dashed lines are the simulation without stress dependent diffusion model. Solid lines are the simulation with stress dependent diffusion model.



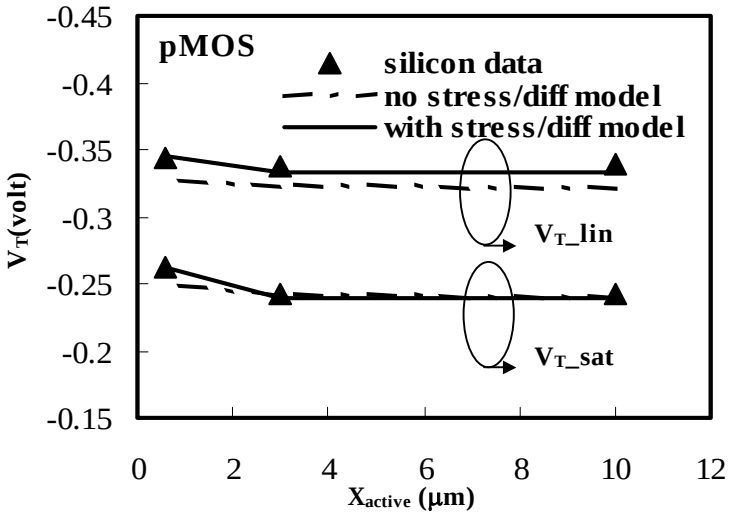
(a) I_D=10^{-7}A/μm, X_{active}=10μm (b) I_D=10^{-8}A/μm, X_{active}=10μm

(c) I_D=10^{-7}A/μm, X_{active}=minimum (d) I_D=10^{-8}A/μm, X_{active}=minimum

Fig. 2.9 Comparison of experimental and simulated nMOSFET V_G at different I_D level for various L_g and X_{active}. Minimum X_{active} for Lg=65nm is 0.6μm, for Lg=0.18μm is 0.74μm, and for Lg=0.42μm is 1μm. Final set of dopant diffusion parameters can model MOSFETs of different X_{active} under various drain voltages and substrate biases. Symbols stand for silicon data. Solid lines represent simulations with stress dependent diffusion model.

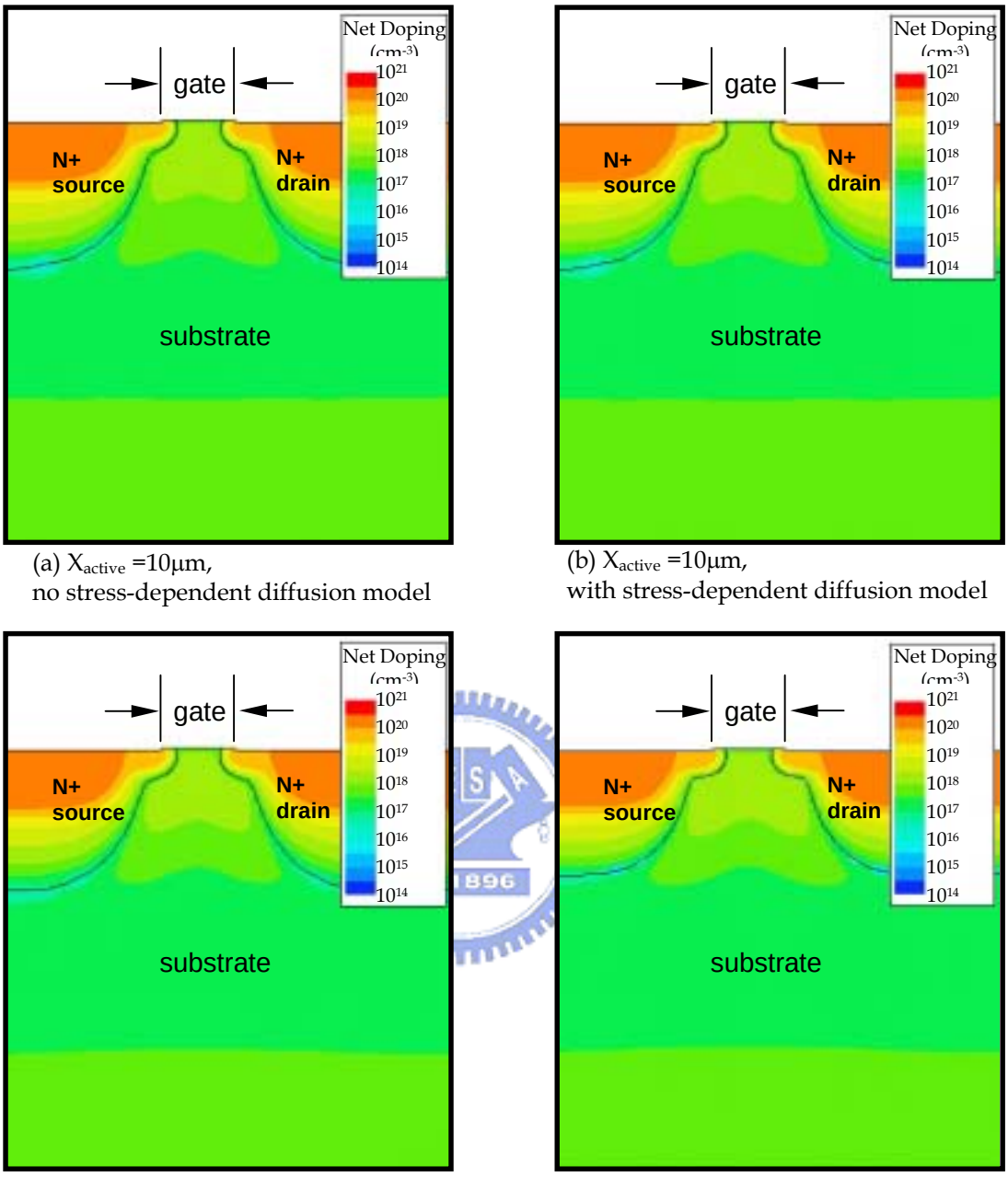


(a) nMOSFET



(b) pMOSFET

Fig. 2.10 Experimental and simulated threshold voltage dependence on X_{active} of (a) nMOSFET and (b) pMOSFET. nMOSFET threshold voltage, V_T, is more dependent on X_{active} than the p-type counterpart. Simulation with stress dependent diffusion model is able to describe stress induced V_T shift.



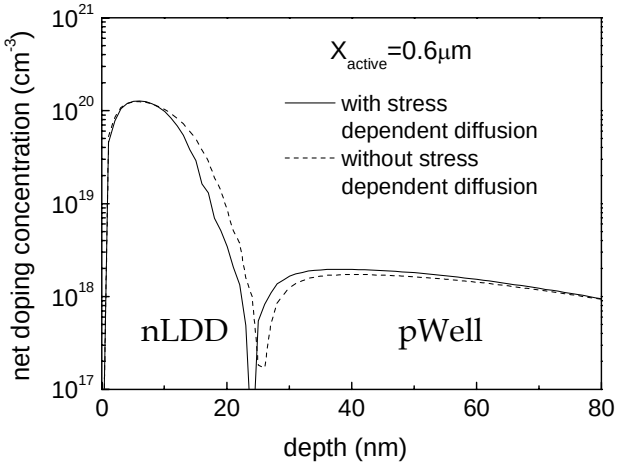
(a) X_{active} =10μm,
no stress-dependent diffusion model

(b) X_{active} =10μm,
with stress-dependent diffusion model

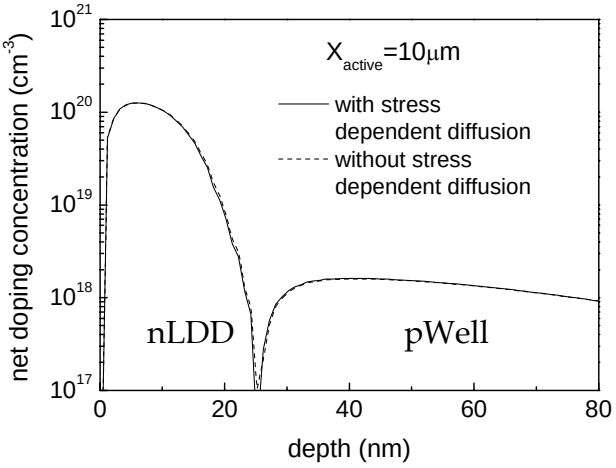
(c) X_{active} =0.6μm,
no stress-dependent diffusion model

(d) X_{active} =0.6μm,
with stress-dependent diffusion model

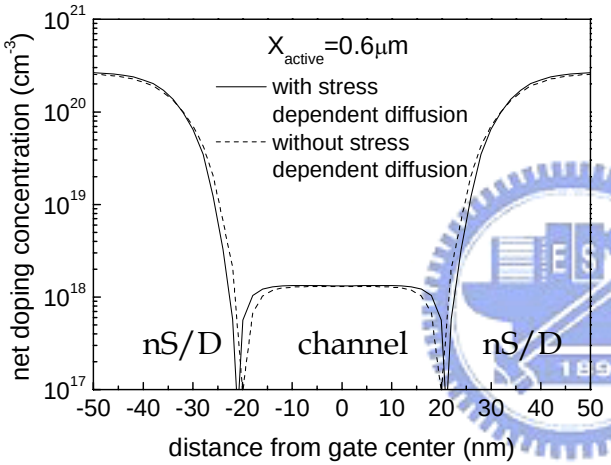
Fig. 2.11 Net doping contours for (a) X_{active}=10μm, no stress-dependent model, (b) X_{active}=10μm, with stress-dependent model, (c) X_{active}=0.6μm, no stress-dependent model, and (d) X_{active}=0.6μm, with stress-dependent model. For X_{active}=0.6μm, the source/drain junction is significantly shallower in the MOSFET core region when the stress-dependent diffusion model is turned on. The gate length is 65nm.



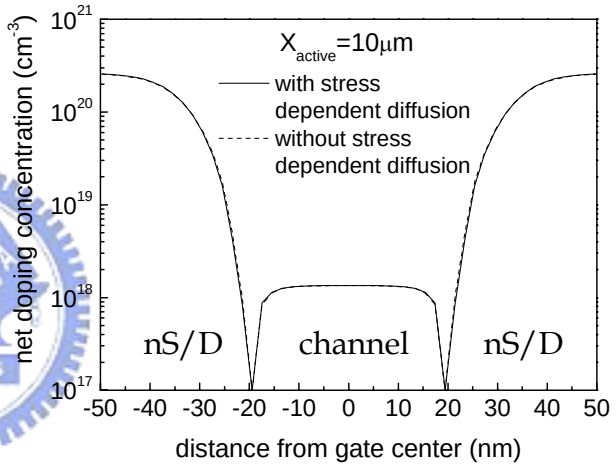
(a) vertical net doping profiles for X_{active}=0.6μm nMOSFET



(b) vertical net doping profiles for X_{active}=10μm nMOSFET



(c) lateral net doping profiles for X_{active}=0.6μm nMOSFET



(d) lateral net doping profiles for X_{active}=10μm nMOSFET

Fig. 2.12 Dopant profiles of (a) vertical direction for X_{active}=0.6μm nMOSFET, (b) vertical direction for X_{active}=10μm nMOSFET, (c) lateral direction for X_{active}=0.6μm nMOSFET, and (d) lateral direction for X_{active}=0.6μm nMOSFET. The vertical profiles are taken at gate edge and the lateral profiles are taken at 15nm deep cut-lines of the device. Solid lines are simulation with stress-dependent diffusion model and dashed lines are without stress-dependent diffusion model. X_{active}=0.6μm with stress-dependent model device exhibits significant retardation of dopant diffusion.

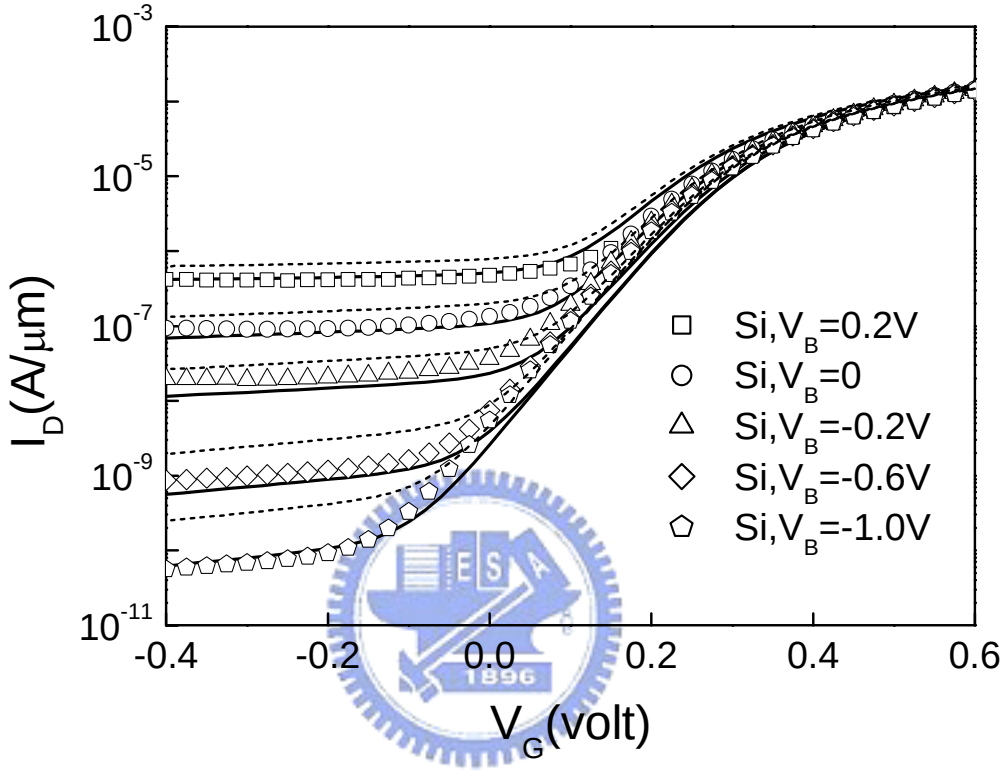


Fig. 2.13 Experimental and simulated I_D-V_G curves for X_{active} = 1.46 μm. Symbols represent experimental data, dashed lines are the simulation results without considering stress-dependent diffusion models, and solid lines are the final simulated results including stress-dependent diffusion models.

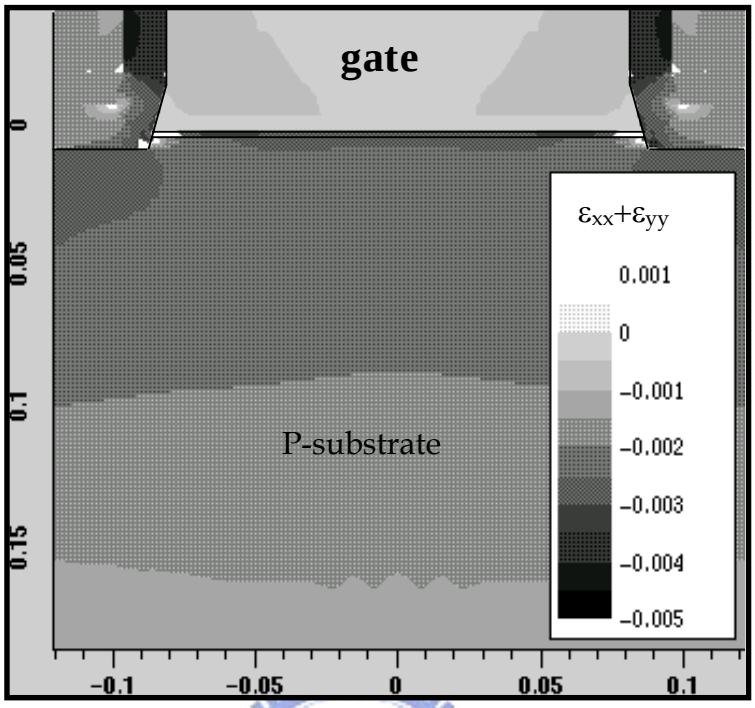


Fig. 2.14 Simulated strain distribution in the silicon after entire front-end process for X_{active} = 0.68 μm. The total strain is in the MOSFET core region are compressive due to thermal gate oxidation and thermal mismatch between STI oxide and silicon.

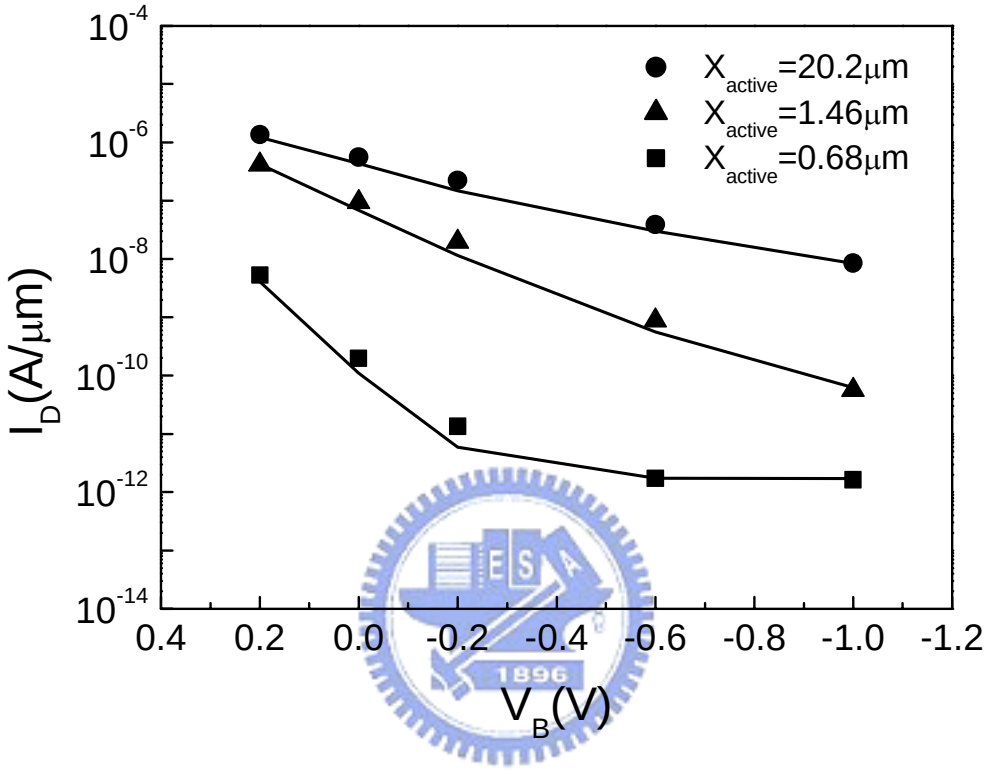


Fig. 2.15 I_D values at V_G = -0.4 V for X_{active} = 20.2 μm, X_{active} = 1.46 μm, and X_{active} = 0.68 μm. Symbols represent experimental data and solid lines are the final simulated results including stress-dependent diffusion models.

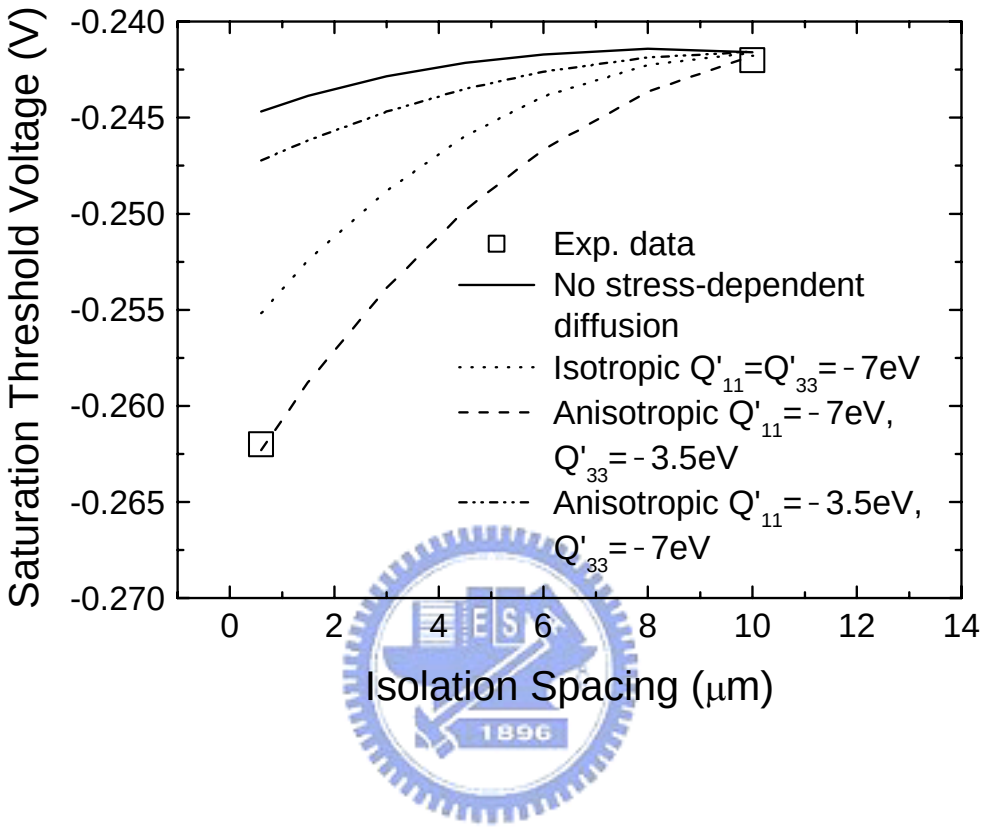


Fig. 2.16 Measured p-MOSFET saturation threshold voltage versus the spacing between the nearby trench isolation sidewalls in the channel length direction. Also shown are those (lines) from the process-device coupled simulation with and without the strain induced activation energies.

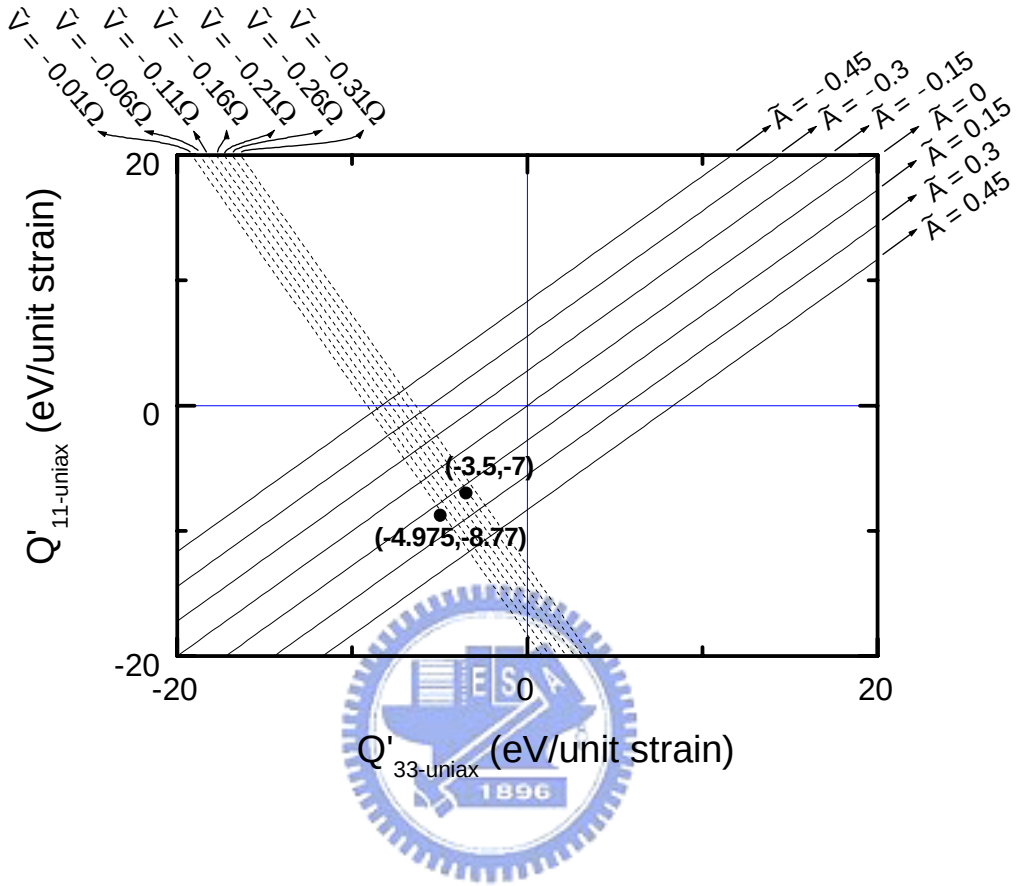


Fig. 2.17 The uniaxial strain induced activation energy in the applied stress direction (parallel to the silicon surface) versus that normal to the silicon surface. The lines are from Eq. (9) and (10) for a literature range (Ref. [3.25]-[3.27]) of the activation volume and the migration strain anisotropy. Also plotted are the data points from the underlying experiment and the existing *ab initio* calculations (Ref. [3.20], [3.29]).

Chapter 3
Mechanical Stress Effects on MOSFET Performances and SPICE Modeling

3.1 Preface

One characteristic of the exploitation of mechanical stress as a MOSFET performance booster, unlike the classical scaling approaches, is that mechanical stress are usually sensitive to the circuit layout. It was reported [3.1] that mechanical stress deteriorates drive current of nMOSFET by a factor as large as 13%. The origin of the degradation is the locally distorted silicon crystal affecting the carrier mobility via band scattering rates and/or carrier effective mass. This effect becomes of increasing importance as CMOS devices continue to shrink further. In this chapter, the STI mechanical stress issue is explored by means of a full-matrix active area layout experiment with emphasis on the center and edge location. Contrary to the report in [3.1], p-channel MOSFET device is remarkably found to be quite sensitive to STI mechanical stress.

3.2 STI Mechanical Stress Effects on Modern MOSFET Drive Currents

3.2.1 Layout Matrix and Experimental Results

Fig. 3.1 schematically shows the topside view of test MOSFET device as well as the cross section along the channel length direction. Four key layout parameters are defined: channel width W, gate length Lg, lateral active area size X_{active} and eccentric

distance between gate and active area center X_{ecc}. The range of each parameter in design matrix is: W = 0.6μm to 10μm; Lg = 0.09μm, 0.1μm and 0.5μm; X_{active} = 0.6μm to 50μm; and X_{ecc}=0 to 4.7μm. Both n and pMOSFETs were investigated under the same condition. The minimum W was set to 0.6μm to avoid electric field concentration effect near the STI corner. Wafers were processed with advanced CMOS dual gate oxide technology [3.2]. The experimental results in Fig. 3.2 show that threshold voltage is essentially intact even under the influence of STI mechanical stress. It also implies that dopant distribution under gate of MOSFET does not change much for various X_{active} and X_{ecc}.

Different behaviors of silicon carrier mobility versus strain had been studied by addressing energy band structure and Monte Carlo simulation in Ref. [3.3]. Basically, biaxial compressive stress degrades in-plane electron mobility while enhancing in-plane hole mobility. The active area stress is compressive in our work according to simulation results. Idsat-Ioff performances are used as drive current indices. In Fig. 3.3, experimental Idsat-Ioff curves for both n and pMOSFETs with different X_{active} are plotted. To facilitate the analysis, Idsat specifically at Ioff =10nA was extracted adequately using least-squares method for different dimensions. The results are depicted in Fig. 3.4 to 3.6. Fig. 3.4 reveals that Idsat of nMOSFET is degraded by a factor as large as 5% while Idsat of pMOSFET is increased with a large factor of 9%. The sensitivity of Idsat to X_{active} increases as X_{active} decreases while tending to saturate for X_{active} larger than 5μm, as encountered in both n and pMOSFETs. The effect of mechanical stress is also tremendous when gate is made

close to the STI edge. The dependencies are comparable to the case of X_{active} getting smaller. It was found that as the gate is placed closer to the STI edge, Idsat degrades up to 3% for nMOSFET while enhancing to 6% for p-channel counterpart. On the other hand, the linear current Idlin (not shown here) exhibited STI mechanical stress dependencies quite similar to Idsat. STI stress effect on drive current in the direction perpendicular to channel current flow is different from the X_{active} direction. Fig. 3.6 shows that short channel nMOSFET degrades by 2% and pMOSFET degrades by 10% as W decreases from 10μm to 0.6μm. It is worth noting that short channel nMOSFET degradation becomes severe when both W and X_{active} are small.

3.2.2 Simulation and Systematic Analysis

To visualize distribution and evolution of underlying mechanisms inside silicon, mechanical stress simulation is of value and some attempts were reported [3.4], [3.5]. In this work, the detailed mechanical stress simulation based on TSUPREM4 (featuring volume change and viscous flow during oxidation) over entire front end of process line for different active area dimensions is presented. The dimensions between two STI regions in the simulation can be regarded as either X_{active} or W in Fig. 3.1. The stress distribution approximates to 2-D case for W/ X_{active} far exceeding unity. Different behaviors of silicon carrier mobility against strain had been thoroughly studied by addressing energy band structure and Monte Carlo simulation in [3.3]. By citing the work of [3.3], biaxial compressive stress degrades in-plane electron mobility while enhancing in-plane hole mobility. Thus,

it is key to judge whether the stress in our test devices is compressive or not.

Simulated final mechanical stress σ_{xx} mapping is shown in Fig. 3.7. In all cases, the silicon surface of the active area is found to compressive, successfully interpreting our experimental observations. It is likely to focus on the magnitude of stress at 20 Å deep below the Si/SiO2 interface where the carrier inversion layer is located due to quantum confinement effect. Lateral strain ε_{xx} distributions for different active area sizes are displayed in Fig. 3.8, showing increased magnitude of strain with downscaling in the size of active area. Fig. 3.8 also reveals the existence of two high compressive regions near STI top corners for large active areas, whereas the overlap is becoming significant and eventually prevails for area less than 5μm. This successfully explains the critical area size of about 5μm mentioned above. Again, Fig. 3.9 shows that the stress or strain magnitude responsible is low for large pattern area while increasing rapidly as dimension becomes less than 5μm.

Remarkably, it is found that the experimental drive current sensitivity tracks well the compressive-type strain along the channel, leading to a correlation established between the two. This one-to-one mapping is shown in Fig. 3.10. A comprehensive comparison involving the effect of gate placement distance is depicted in Fig. 3.11. As expected, one-to-one mapping remains effective. Fig. 3.11 also figures out that a significant change happens not only in n-FETs but also in p-FETs when the gate is made closer to the STI edge. Simulation suggests that the oxidation step after STI formation is responsible for the surface compressive stress creation.

3.3 SPICE Model for STI Mechanical Stress Effect

This section demonstrates a new compact and scalable model related to the mechanical stress effect on MOSFET electrical performance induced by the shallow trench isolation (STI). This model includes the influence of STI stress not only on the mobility and saturation velocity, but also on the threshold voltage.

The STI stress effect and its impact on model parameters is analyzed. The 2-D full-process mechanical stress simulation result had been presented in a previous section. Now, a phenomenological model is proposed based on the trend of the MOSFET electrical measurement data from the active area dimension experiment. The model has been extended to account for the shapes of active regions by calculating the effective distance to the STI. All equations have been verified using MOSFET measurement data. The importance of the model and how it improves the circuit design of advanced CMOS technologies will also be discussed.

3.3.1 MOSFET Measurement Data Analysis

There are three MOSFET active region dimension parameters that need to be re-defined for the SPICE model usage and they are shown in Fig. 3.12. First, the length of the active region is re-defined as LOD (Length of the thin Oxide Definition area). The other two are *SA* and *SB*, which are the left side and right side gate-to-STI distance. As can be seen, LOD is equal to the sum of the gate, SA and SB of the MOSFET.

The measurement indicates that the drain current will be enhanced or

degraded depending on the values of LOD because of mobility changes [3.3], [3.6]. As shown in Fig. 3.13, the drain current (*Id*) shift versus LOD curves will move left as the channel length becomes shorter, and is explained in Fig. 3.14. Fig. 3.14 illustrates the stress distribution under the channel region. Although MOSFETs with the same LOD will generally have the same stress distribution along the channel region, only the stress under the gate has direct impact on MOSFET performance. By comparing the channel region shown in Fig. 3.14, it can be seen that channel lengths clearly have a higher average stress within the channel region, even if the LOD values are kept the same. Therefore, longer channel MOSFETs will suffer a greater stress effect than those containing shorter channels with regard to mobility shift.

The MOSFET threshold voltage (*Vth*) shift has the 1/LOD trend as *Id* shift. However, it shows the opposite trend to the channel length scaling. As shown in Fig. 3.15, the shift in threshold voltage increases significantly for shorter channel lengths. The threshold voltage is defined by using maximum transconductance method. The polysilicon gate length of the MOSFETs has been verified to have no significant effect by using in-process SEM measurements. Therefore, the *Vth* change is mainly coming from the doping profile change under different STI stress discussed in Chapter 2.

3.3.2 Model Development

From the above analysis, it can be proved that two mechanisms exist to have a stress effect on the MOSFET characteristics. The first is mobility-related and is

induced by the band structure change [3.3], [3.6]. The second is Vth-related as a result of doping profile variations [3.1], [3.7]. Both follow the same 1/LOD trend, but reveal different L and W scaling. A phenomenological model based on these findings has been derived by modifying some parameters in the Berkeley Short-channel IGFET Model (BSIM). It should be noted that the following equations have no impact on iteration time because they contain no voltage-controlled components.

A. Mobility-Related Equations

This model introduces the first mechanism by adjusting the *U0* and *Vsat* according to different *W*, *L* and OD shapes. Here are the equations:

$$Inv\_sa = \sum_{i=1}^{n} \frac{\mathrm{sw_i}}{W_{drawn}} \cdot \frac{1}{\mathrm{sa_i} + 0.5 \cdot L_{drawn}}, Inv\_sb = \sum_{i=1}^{n} \frac{\mathrm{sw_i}}{W_{drawn}} \cdot \frac{1}{\mathrm{sb_i} + 0.5 \cdot L_{drawn}} \tag{3.1}$$

$$rho = \frac{\mathrm{ku0}}{Kstress\_u0} \cdot \left(Inv\_sa + Inv\_sb\right) \tag{3.2}$$

$$Inv\_sa0 = \frac{1}{\mathrm{sa0} + 0.5 \cdot L_{drawn}}, Inv\_sb0 = \frac{1}{\mathrm{sb0} + 0.5 \cdot L_{drawn}} \tag{3.3}$$

$$rho\_def = \frac{\mathrm{ku0}}{Kstress\_u0} \cdot \left(Inv\_sa0 + Inv\_sb0\right) \tag{3.4}$$

$$Kstress\_u0 = \left(1 + \frac{\mathrm{lku0}}{(L_{drawn} + XL)^{\mathrm{llodku0}}} + \frac{\mathrm{wku0}}{(W_{drawn} + XW + \mathrm{wlod})^{\mathrm{wlodku0}}} + \frac{\mathrm{pku0}}{(L_{drawn} + XL)^{\mathrm{llodku0}} \cdot (W_{drawn} + XW + \mathrm{wlod})^{\mathrm{wlodku0}}}\right) \times \left(1 + \mathrm{tku0} \cdot \left(\frac{Temperature}{TNOM} - 1\right)\right) \tag{3.5}$$

$$u0temp = \frac{1 + rho}{1 + rho\_def} \cdot u0temp_{original}, vsattemp = \frac{1 + \mathrm{kvsat} \cdot rho}{1 + \mathrm{kvsat} \cdot rho\_def} \cdot vsattemp_{original} \tag{3.6}$$

where *swi*, *sai* and *sbi* are new instant parameters to describe the shape of OD region as shown in Fig. 3.16.

B. Vth-Related Equations

Vth0, *K2* and *ETA0* are modified to cover the doping profile changes in the MOSFETs with different LOD. The same 1/LOD formulas as shown in section A is used. However, different equations for *W* and *L* scaling are necessary:

$$Kstress\_vth0 = 1 + \frac{\text{lkvth0}}{(L_{drawn} + XL)^{\text{llodkvth}}} + \frac{\text{wkvth0}}{(W_{drawn} + XW + \text{wlod})^{\text{wlodkvth}}} + \frac{\text{pkvth0}}{(L_{drawn} + XL)^{\text{llodkvth}} \cdot (W_{drawn} + XW + \text{wlod})^{\text{wlodkvth}}} \tag{3.7}$$

$$vth0 = vth0_{original} + \frac{\text{kvth0}}{Kstress\_vth0} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa0 - Inv\_sb0\right) \tag{3.8}$$

$$k2 = k2_{original} + \frac{\text{stk2}}{Kstress\_vth0^{\text{lodk2}}} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa0 - Inv\_sb0\right) \tag{3.9}$$

$$eta0 = eta0_{original} + \frac{\text{steta0}}{Kstress\_vth0^{\text{lodeta0}}} \cdot \left(Inv\_sa + Inv\_sb - Inv\_sa0 - Inv\_sb0\right) \tag{3.10}$$

C. Effective *SA* and *SB* for Irregular LOD

Additional instance parameters as shown in Fig. 3.16 are required to fully describe the shape of *OD* region. However, this will result in too many parameters

in the net lists and would massively increase the reading time and degrade the readability of parameters. One way to overcome this difficulty is the concept of effective SA and SB similar to [3.8]. The following effective SA and SB equations are proposed here to improve the efficiency and also to keep the accuracy and compatibility of the above LOD model:

$$\frac{1}{\mathrm{sa}_{\mathrm{eff}} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{\mathrm{sw}_{\mathrm{i}}}{W_{drawn}} \cdot \frac{1}{\mathrm{sa}_{\mathrm{i}} + 0.5 \cdot L_{drawn}} \tag{3.11}$$

$$\frac{1}{\mathrm{sb}_{\mathrm{eff}} + 0.5 \cdot L_{drawn}} = \sum_{i=1}^{n} \frac{\mathrm{sw}_{\mathrm{i}}}{W_{drawn}} \cdot \frac{1}{\mathrm{sb}_{\mathrm{i}} + 0.5 \cdot L_{drawn}} \tag{3.12}$$

These two equations are parameter independent and could be implemented directly in the layout extraction tools. Therefore only one set of SA_{eff} and SB_{eff} is extracted from complicated layouts and is enough to represent the influence of stress effect.

3.3.3 Model Verification

The model has been verified using different technologies with different dimensions and various MOSFET layout styles. The following model results have been achieved using global fitting.

A. Drain Current

Fig. 3.17 shows the drain current shift in percentages, biased in the saturation region for various W and L values. The fitting results of the model created by

Bianchi, et al. [3.8] are also included for comparison. From Fig. 3.17, it can be seen that the LOD effect is slightly alleviated in the cases where the channel is narrower. The most interesting phenomenon is that a peak Id shift exists around L = 0.5μm to L = 1μm if the *SA* difference is the same. Previous work [3.8] has indicated a good fitting result where L < 0.5μm, but is not able to predict this behavior and will overestimate the LOD effect for long-channel devices (L>0.5μm). In contrast, our new LOD model fits the data well over the entire range of channel lengths because 1/LOD, rather than 1/*SA*, is adopted. Fig. 3.18 shows that the stress effect has a different impact on drain currents biased in linear and saturation regions, and can be interpreted from the change in saturation velocity [3.6]. Other parameters have been excluded because detailed analysis indicates that this difference is irrelevant to the doping profile change. The temperature dependence of the LOD effect has also been checked. As shown in Fig. 3.19, the LOD effect shows little sensitivity to temperature and a simple linear equation can simulate this dependence.

B. Threshold Voltage, DIBL and Body Effects

Significant Vth shifts only occur in short channel MOSFETs, as illustrated in Fig. 3.20 and is mainly due to doping profile changes at different LOD values, which is why the DIBL and body effect change at the same time. As shown in Fig. 3.20, the *Vth* in the saturation region will shift more seriously than in the linear region because the DIBL effect has been modulated. This effect has been model using TCAD simulation and is described in Chapter 2. The body effect factor, gamma, in Fig.

3.21 also exhibits a similar behavior. The *Idlin*, *Idsat*, *Vth0*, DIBL and body effects follow the same 1/LOD trend, and their behaviors can be explained by the mechanical stress dependent dopant diffusion mentioned in Chapter 2. The short channel length phenomenon showing a larger *Vth* is also consistent with the active area size mechanical stress simulations.

C. Irregular LOD

This model has been verified using different types of irregular layout styles, as demonstrated in Fig. 3.22. The width ratio is calculated from the gate to active area distance and the gate length:

$$W_{ratio} = \frac{\left(\frac{1}{\mathrm{sa}_{\mathrm{eff}} + 0.5 \cdot L_{drawn}} + \frac{1}{\mathrm{sa}_{\mathrm{eff}} + 0.5 \cdot L_{drawn}}\right) - \frac{2}{\mathrm{sa}_{\mathrm{i}} + 0.5 \cdot L_{drawn}}}{\frac{2}{\mathrm{sa}_2 + 0.5 \cdot L_{drawn}} - \frac{2}{\mathrm{sa}_1 + 0.5 \cdot L_{drawn}}} \tag{3.13}$$

The experiment and model fitting results show that a linear interpolation, weighted based on the width of each segment, as proposed in our model, can fit the data well. These results also reconfirm that the suggested equivalent *SA/SB* approach is efficient and accurate enough for the various shapes used in complicated layouts.

3.3.4 Impact on Circuit Design

It would not be sufficient to consider only the *W* and *L* of MOSFETs during the design of circuits for advanced CMOS technologies. Both the layout shape and device location will also have a direct influence on MOSFET behavior, and thus the

circuit performance. It is quite a straightforward matter to simply enlarge the design margin of the circuit to cover the LOD effect, but this would be too luxurious and impractical. Designers may need to take the LOD effect into rough consideration at the beginning of the design process and should check it again when the layout is completed.

As shown in Figs. 3.17 and 3.18, the PMOS performance is enhanced, but the NMOS performance is degraded when the LOD is shrunk. So the total circuit delay may not change too much because the LOD effect on the nMOSFET and the pMOSFET drive current is opposite. However, the rise time and fall time will probably have been seriously altered. The threshold voltage shift induced by the LOD effect is another issue, which will further cause the NMOS devices performance degradation, and will also possibly worsen the cases with corner conditions. In general, the LOD effect is more significant for longer channel (0.2um~1um) and wider channel (>1um) and thus high-speed input/output (IO) circuits would be more susceptible to the LOD effect than core circuits. The impact of the LOD effect also needs to be considered when designing patterns for SPICE modeling. Modeling accuracy would be greatly enhanced if the proper choice were made with regard to the default LOD size.

References

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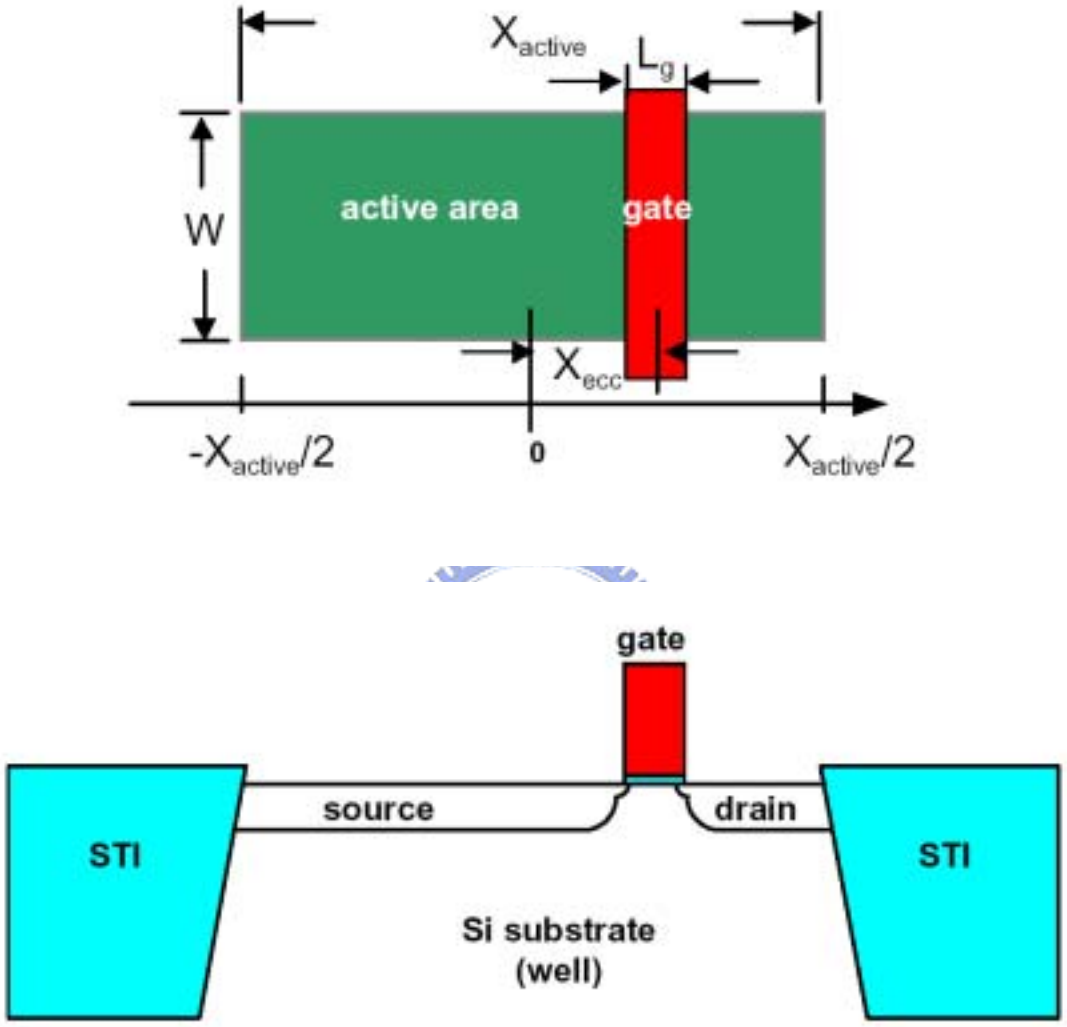

Fig. 3.1 Key MOSFET layout parameter definitions in this work and schematic cross section along channel length direction.

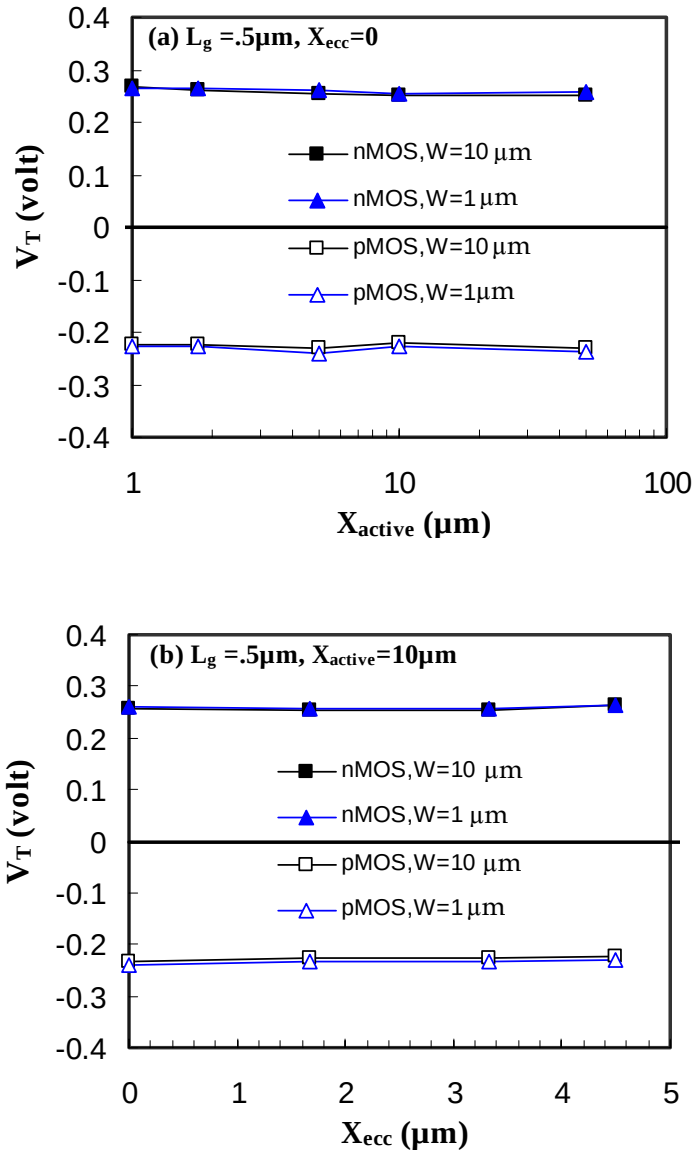

Fig. 3.2 Long channel threshold voltage VT versus (a) X_{active} and (b) X_{ecc} for a variety of W. Obviously, VT is insensitive to STI mechanical stress.

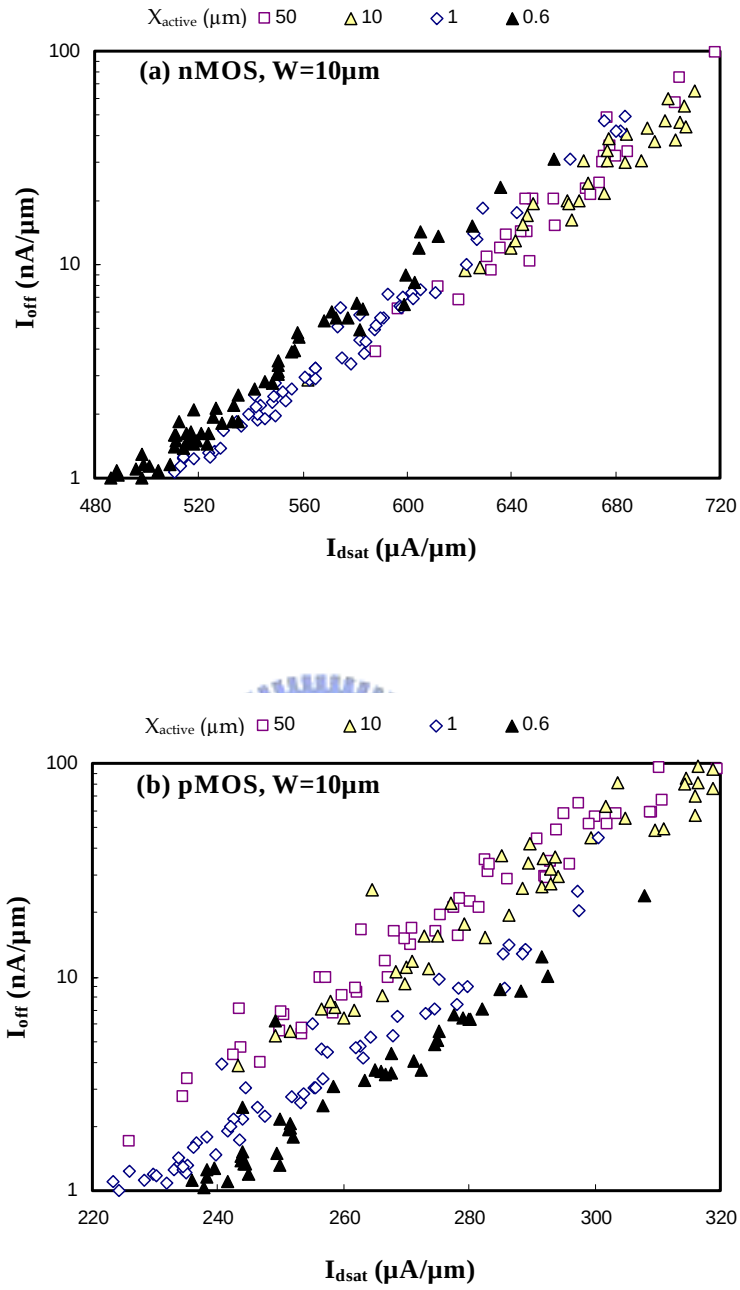

Fig. 3.3 Short channel Idsat-Ioff for (a) nMOSFET and (b) pMOSFET for a variety of X_{active}. Idsat at Ioff=10nA/μm is taken as drive current index.

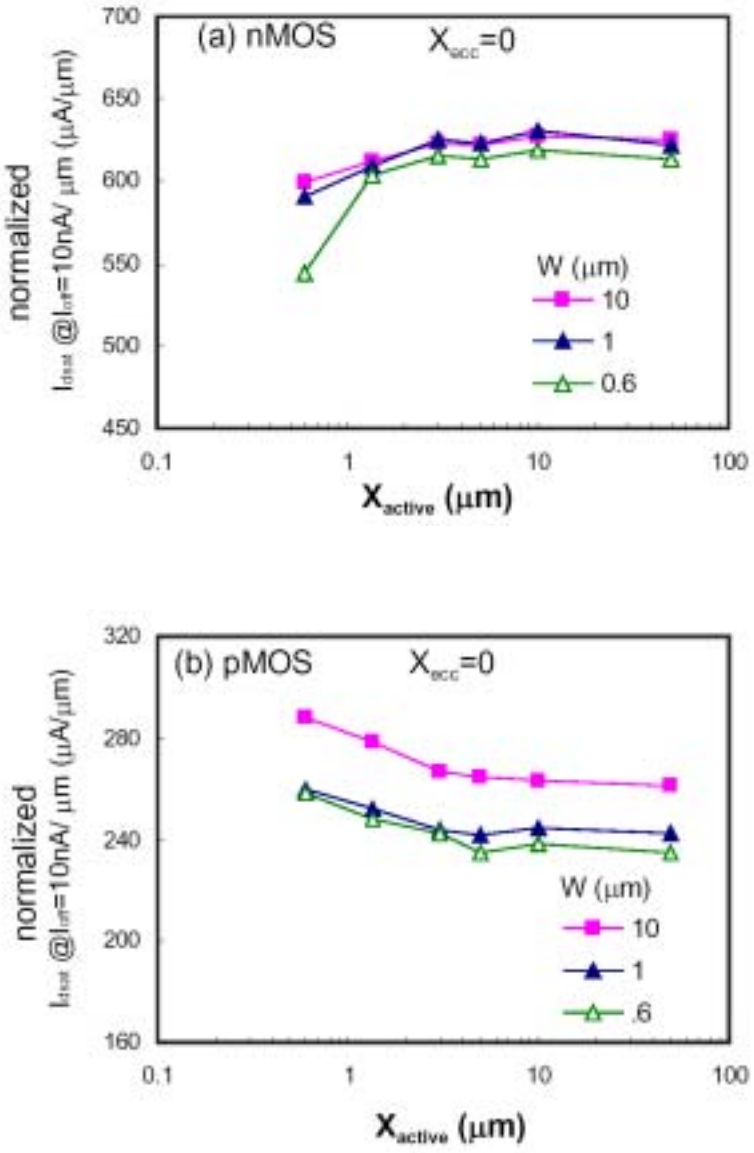

Fig. 3.4 Short channel Idsat versus active area dimension X_{active} with different W for (a) nMOSFET and (b) pMOSFET. nMOSFET Idsat is degraded while pMOSFET Idsat is enhanced as active area size decreases. Idsat becomes insensitive to X_{active} when active area size is greater than 5μm.

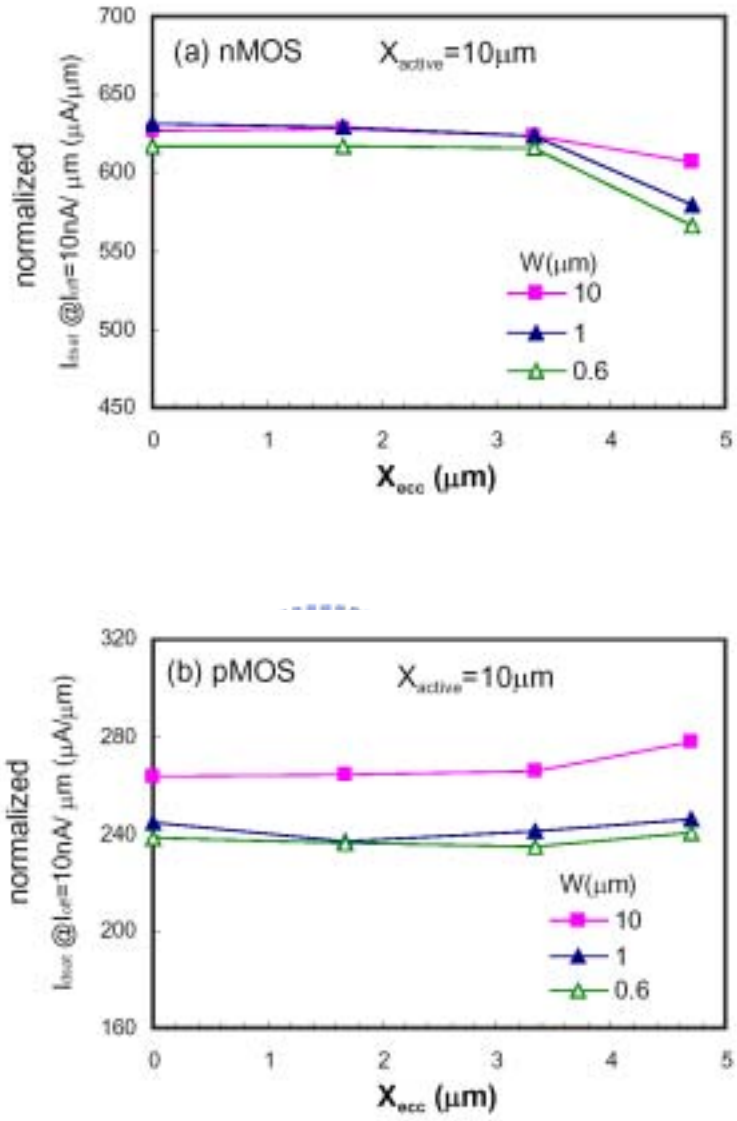

Fig. 3.5 Short channel Idsat versus gate placement inside active area Xecc for different W for (a) nMOSFET and (b) pMOSFET. nMOSFET Idsat is degraded while pMOSFET Idsat is enhanced as gate placement is closer to STI edge.

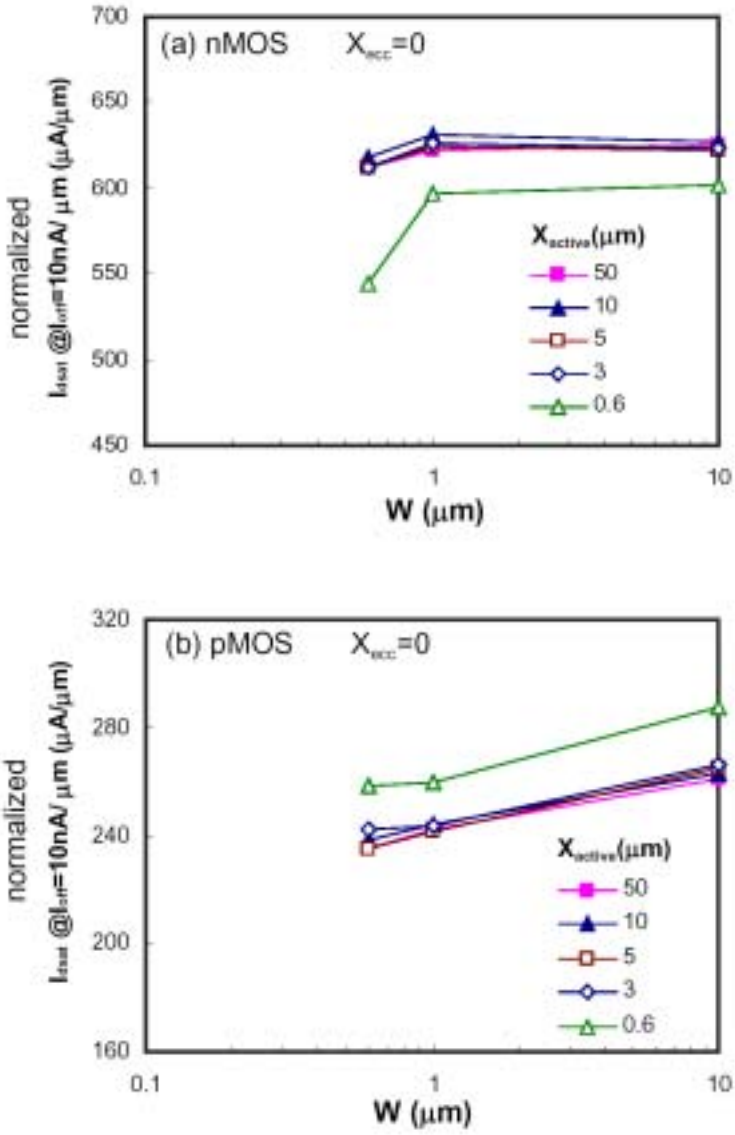

Fig. 3.6 Short channel Idsat versus W for (a) nMOSFET and (b) pMOSFET with various Xactive. Both n and pMOSFET drain currents degrade as W decreases.

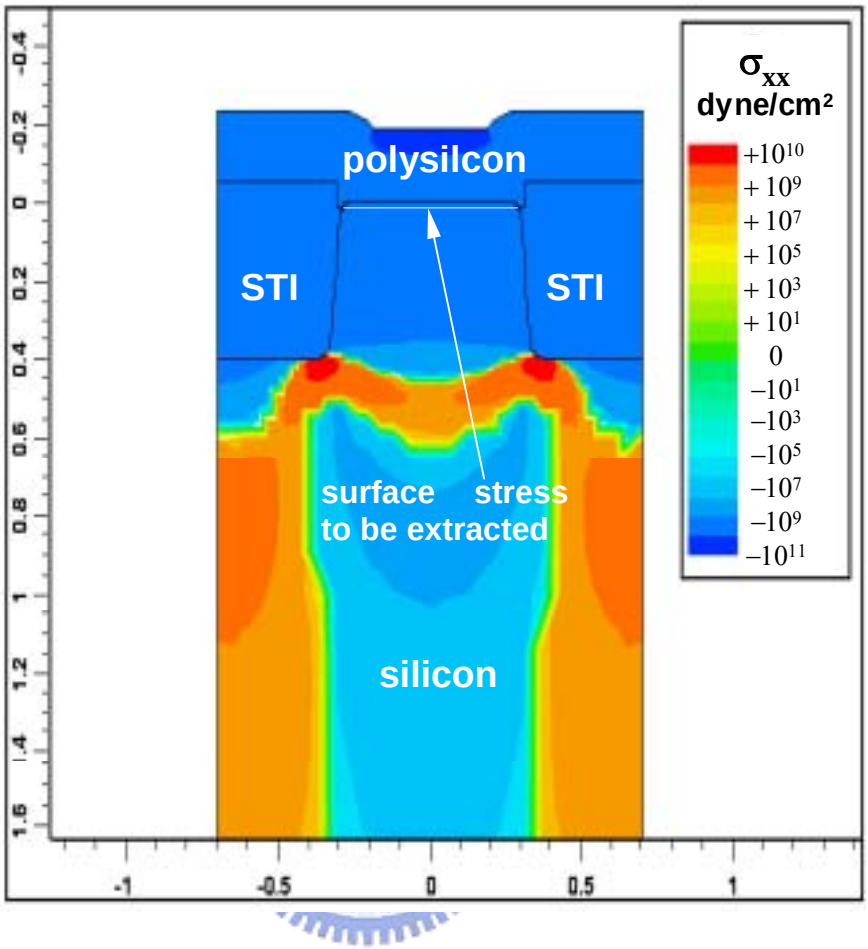

Fig. 3.7 Simulated final stress Sxx distribution for X_{active}=0.6μm. Stress near Si/SiO2 interface is found to be compressive.

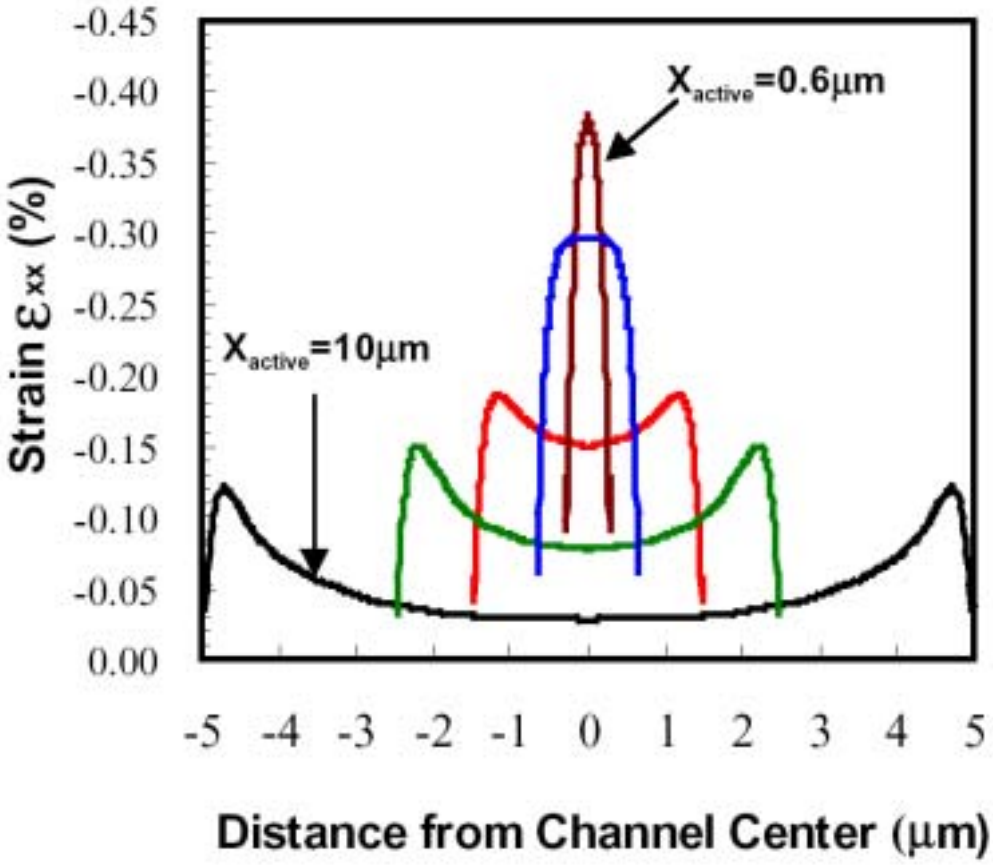

Fig. 3.8 Simulated strain ε_{xx} inside silicon along a line 20Å deep below Si/SiO2 interface for different active area dimensions. Strain magnitude increases as active area size decreases.

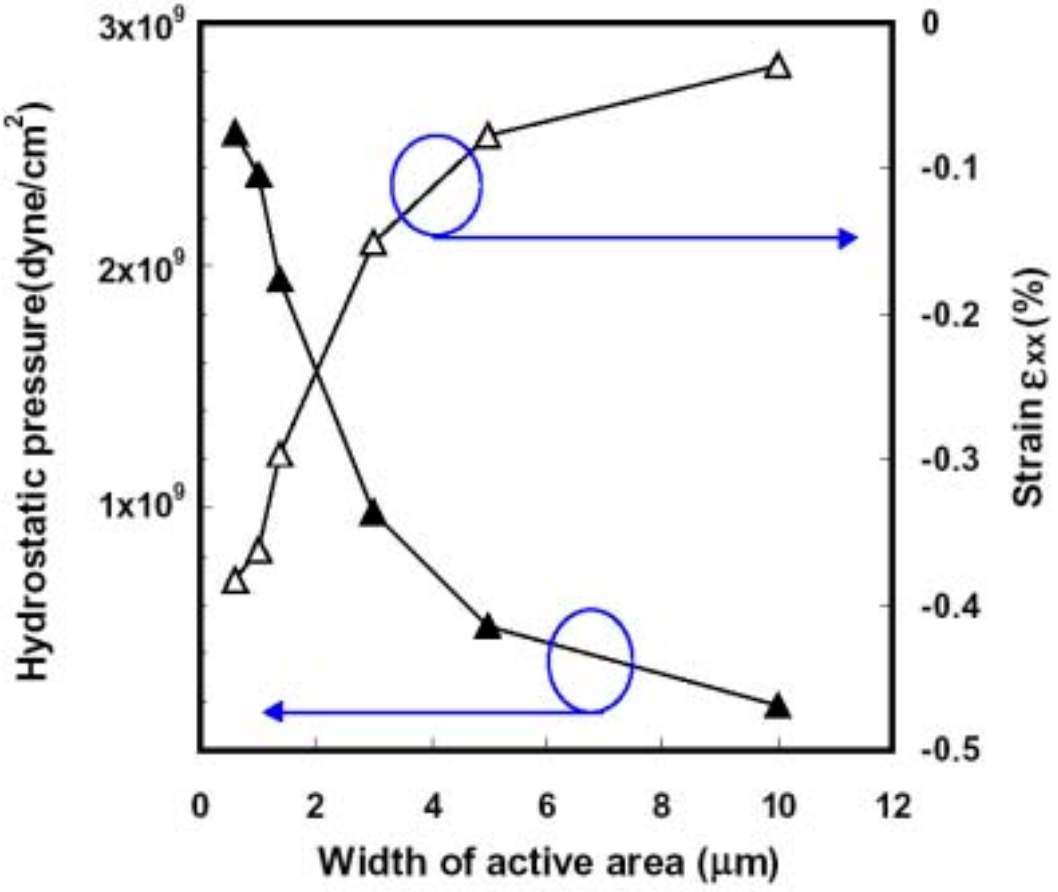

Fig. 3.9 Simulated hydrostatic pressure and strain ε_{xx} for different active area dimensions. Stress and strain magnitudes increase rapidly as active area size decreases from around 5μm.

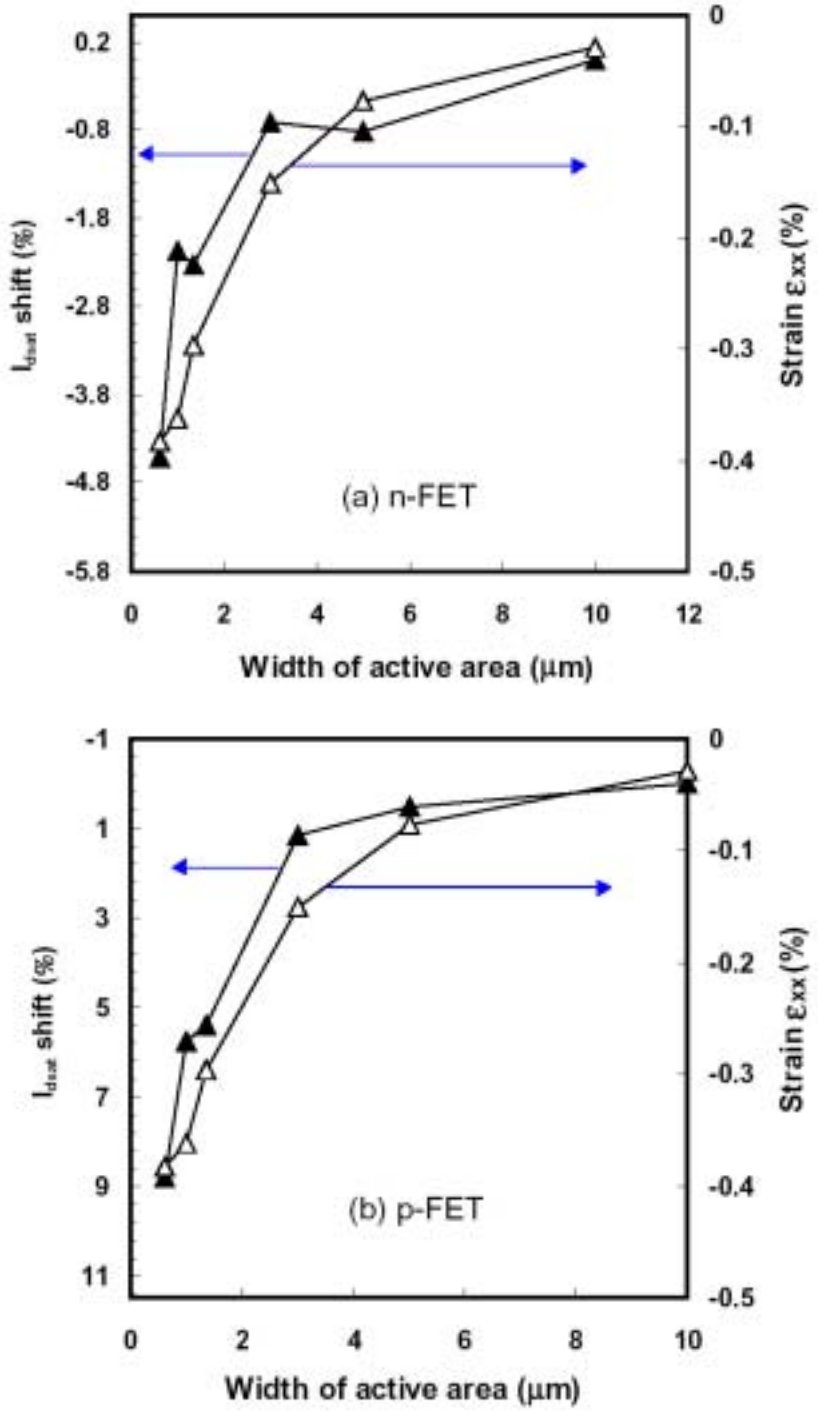

Fig. 3.10 Experimental drive current sensitivity and simulated strain ε_{xx} both versus active area size for (a) n-FET and (b) p-FET. A one-to-one mapping remains effective for both n-FETs and p-FETs.

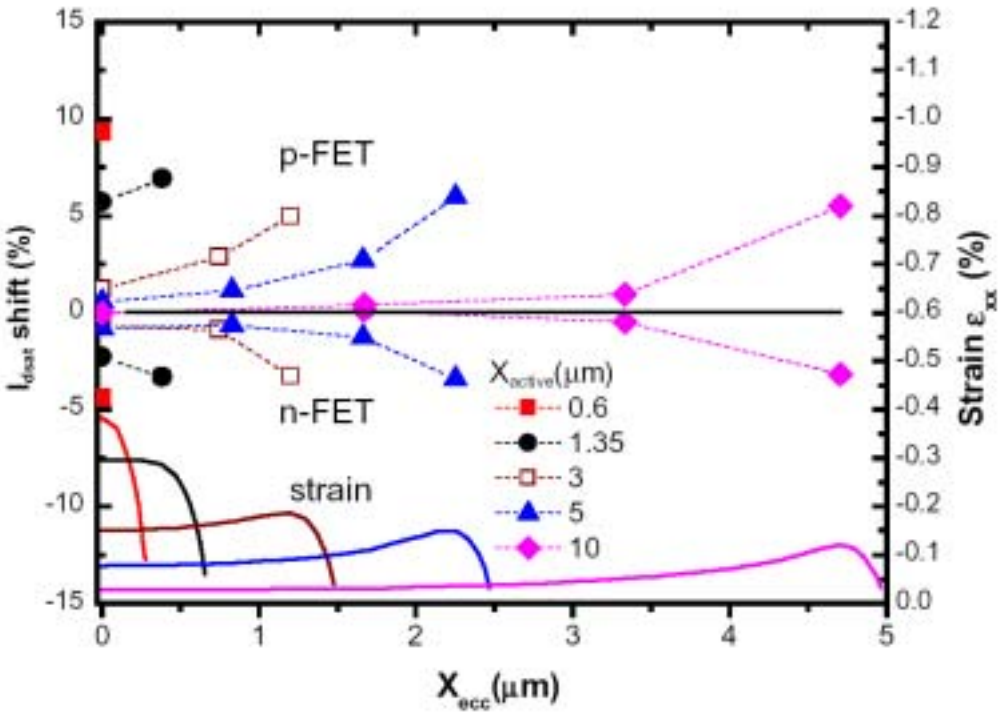

Fig. 3.11 Experimental drive current shift with respect to W=10mm, X_{ecc}=0 versus X_{ecc} for different X_{active}. Simulated strain ε_{xx} is also shown together for comparisons. The trends of drive current and strain match well.

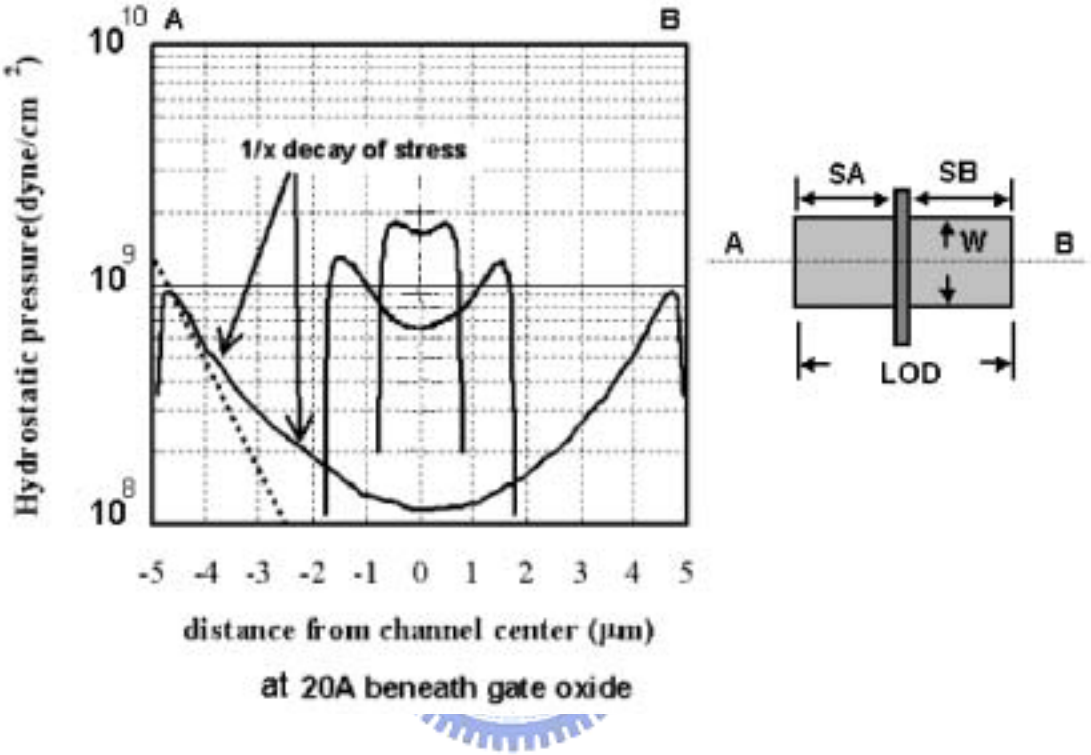

Fig. 3.12 Stress distribution near the gate oxide interface of MOSFET using 2D simulation.

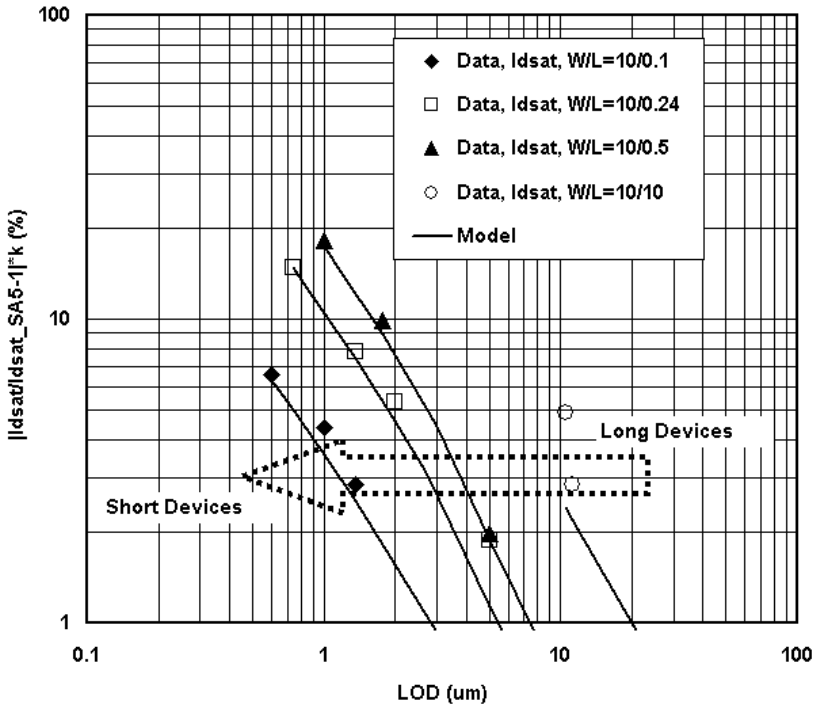

Fig. 3.13 Drain current shift with respect to different LOD sizes for different channel lengths.

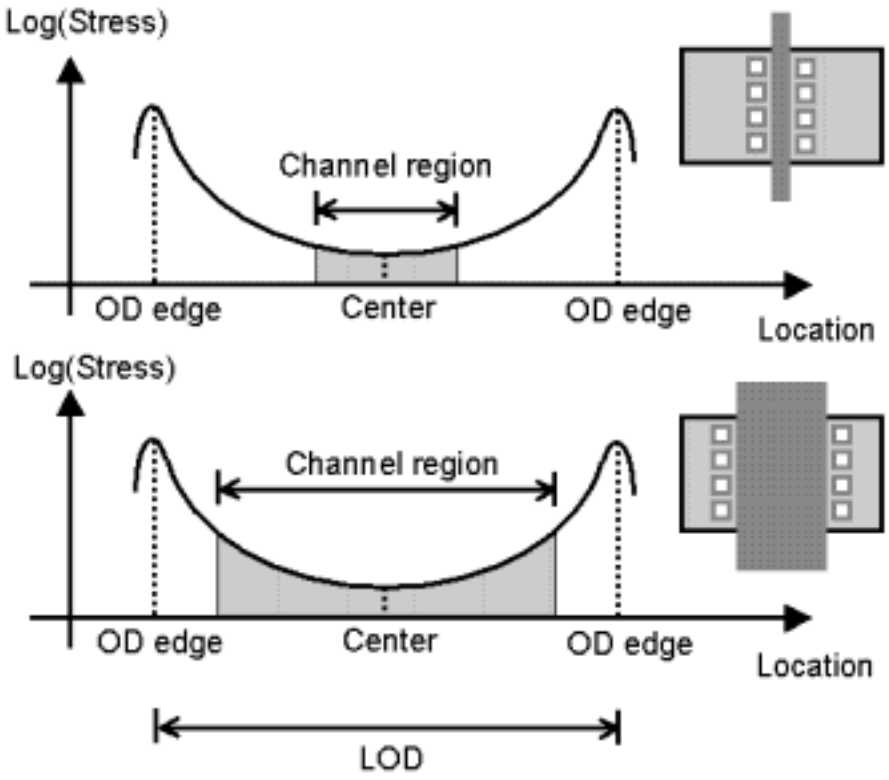

Fig. 3.14 schematic stress distribution within the channel regions.

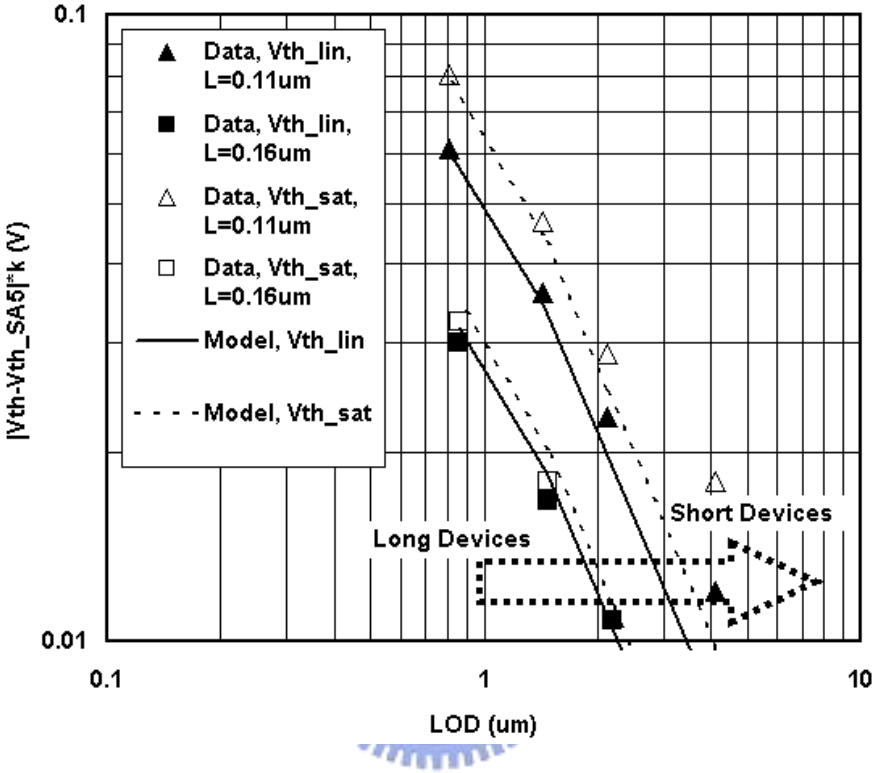

Fig. 3.15 Threshold voltage shift with respect to different LOD sizes for different channel lengths.

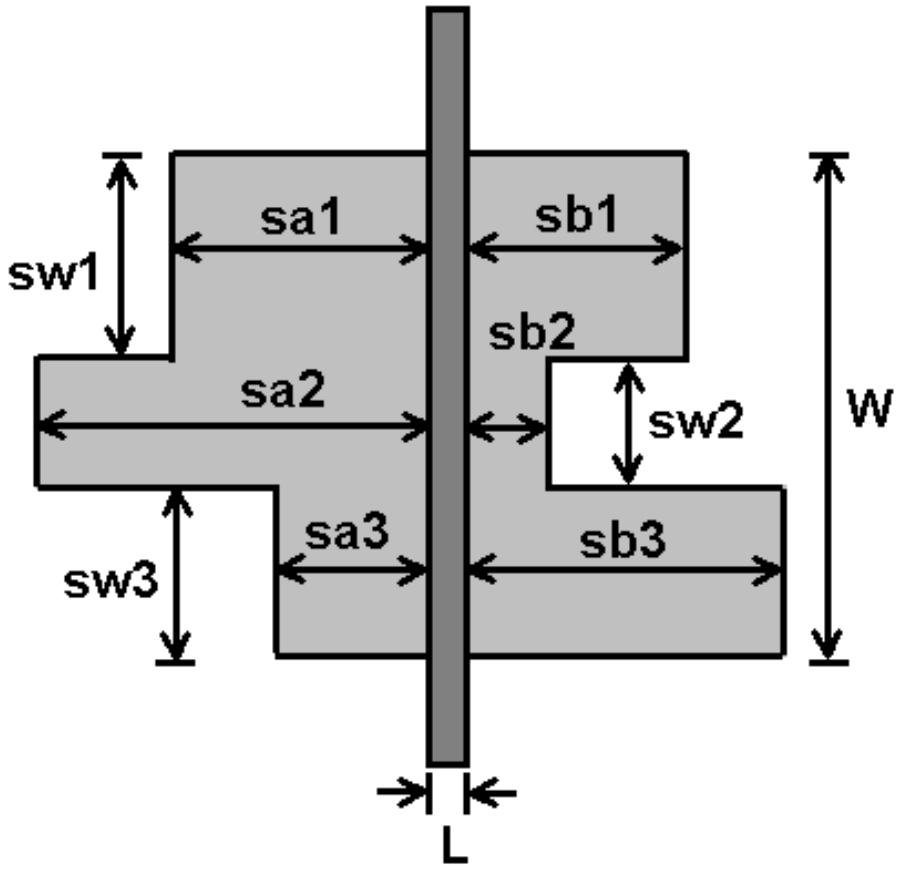

Fig. 3.16 A typical layout of MOS devices needing more instance parameters (swi, sai and sbi) in addition to the traditional L and W.

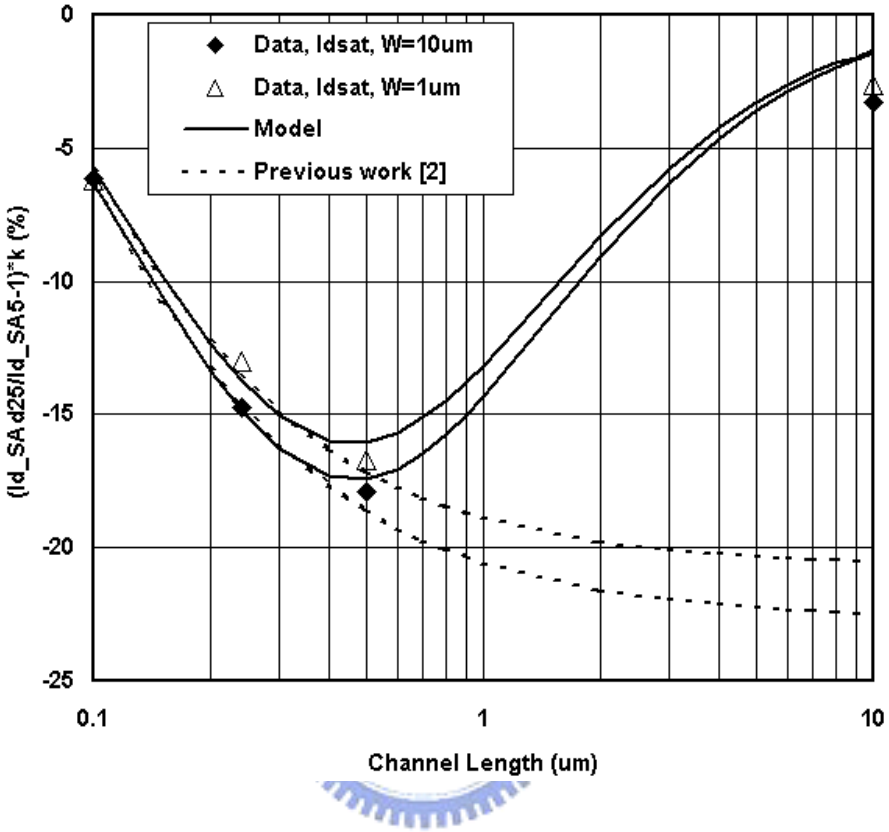

Fig. 3.17 nMOSFET drain current (Id) difference in percentage between SA=0.25μm and 5μm comparing various channel lengths and widths.

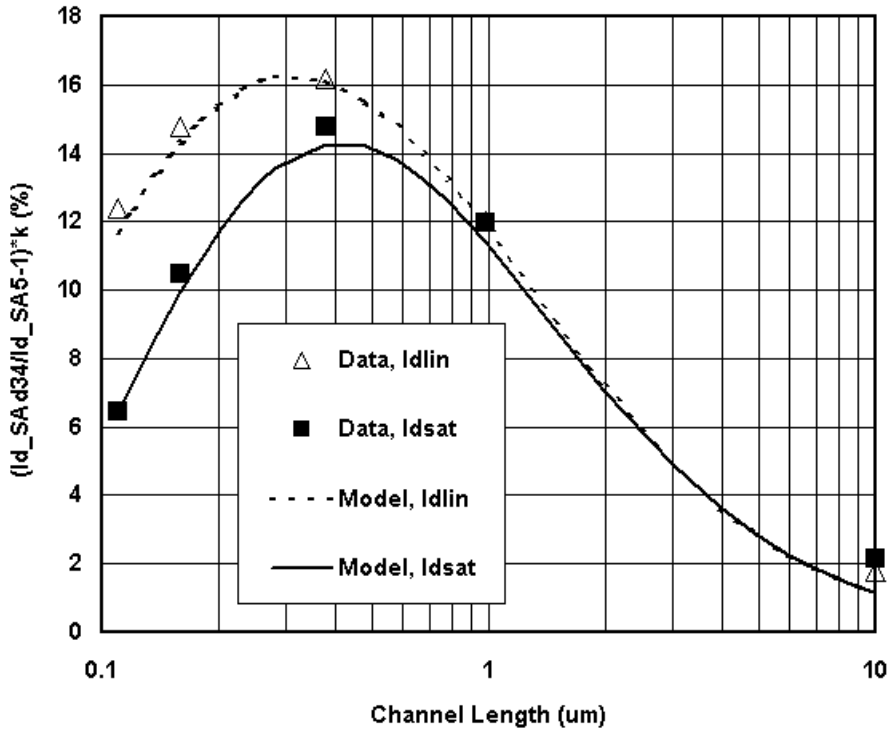

Fig. 3.18 pMOSFET drain current (Id) difference in percentage between SA=0.25μm and 5μm comparing drain currents in linear and saturation regions.

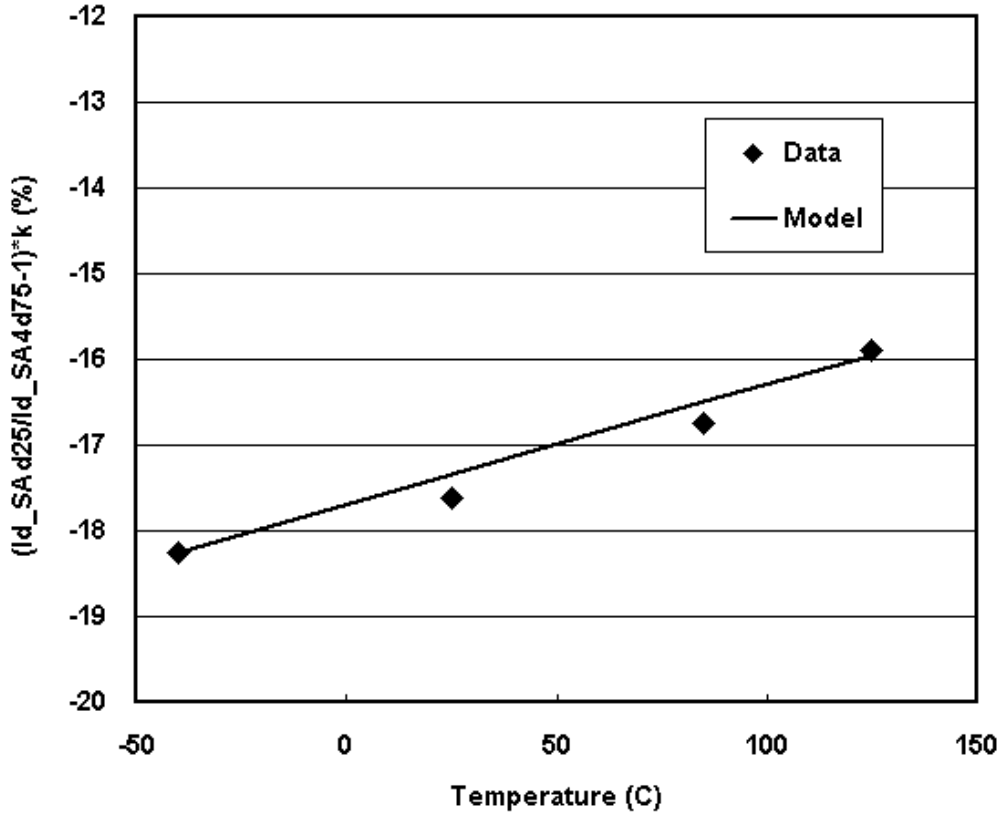

Fig. 3.19 Temperature sensitivity of LOD effect. LOD effect is quite insensitive to temperature and simply a linear equation could simulate the dependence.

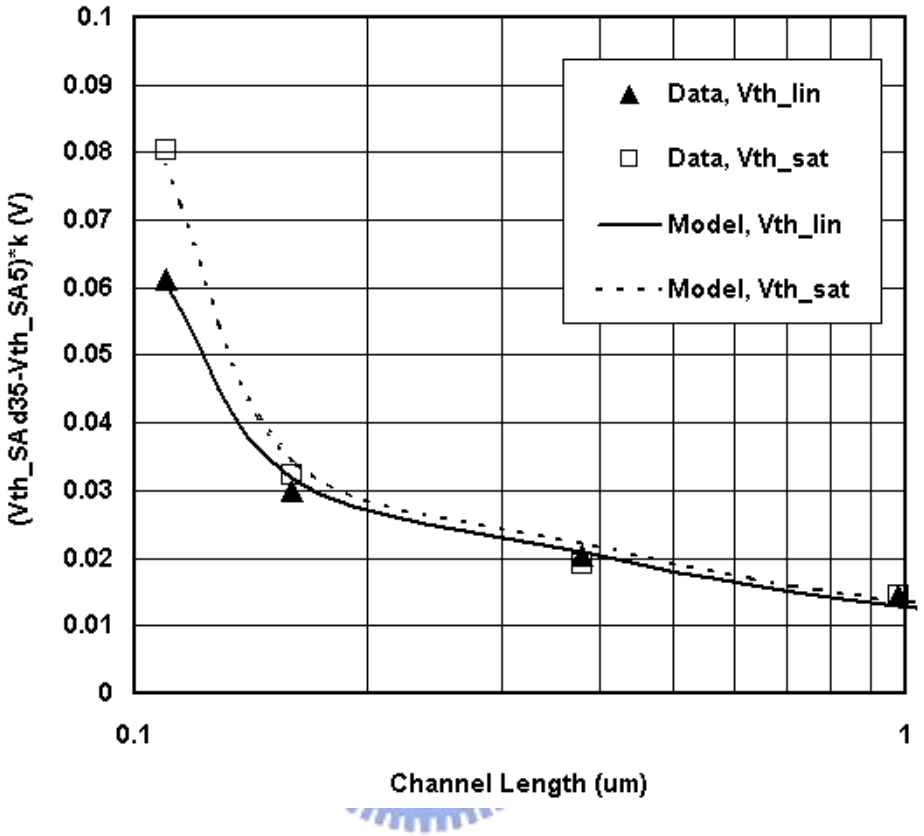

Fig. 3.20 Vth shift between SA=0.25μm and SA=5μm with Vds=0.1V and Vdd for different channel lengths.

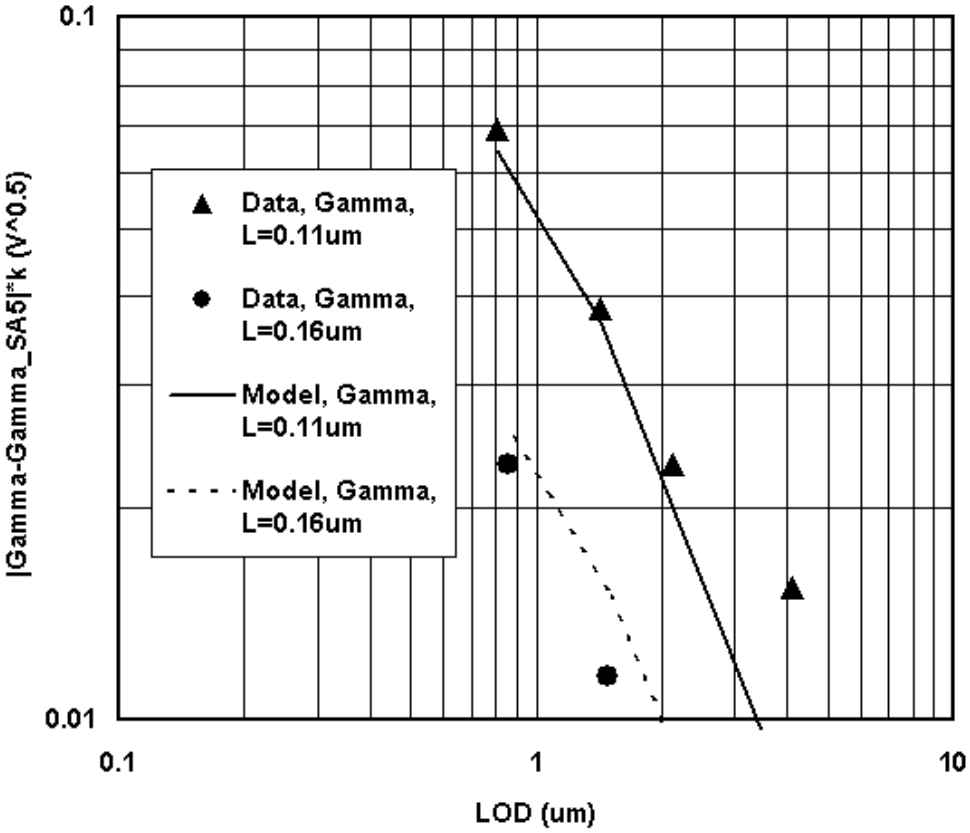

Fig. 3.21 Gamma shift versus LOD with different channel lengths. Gamma increases as LOD decreases because of higher channel doping concentrations due to diffusion retardations by compressive stress.

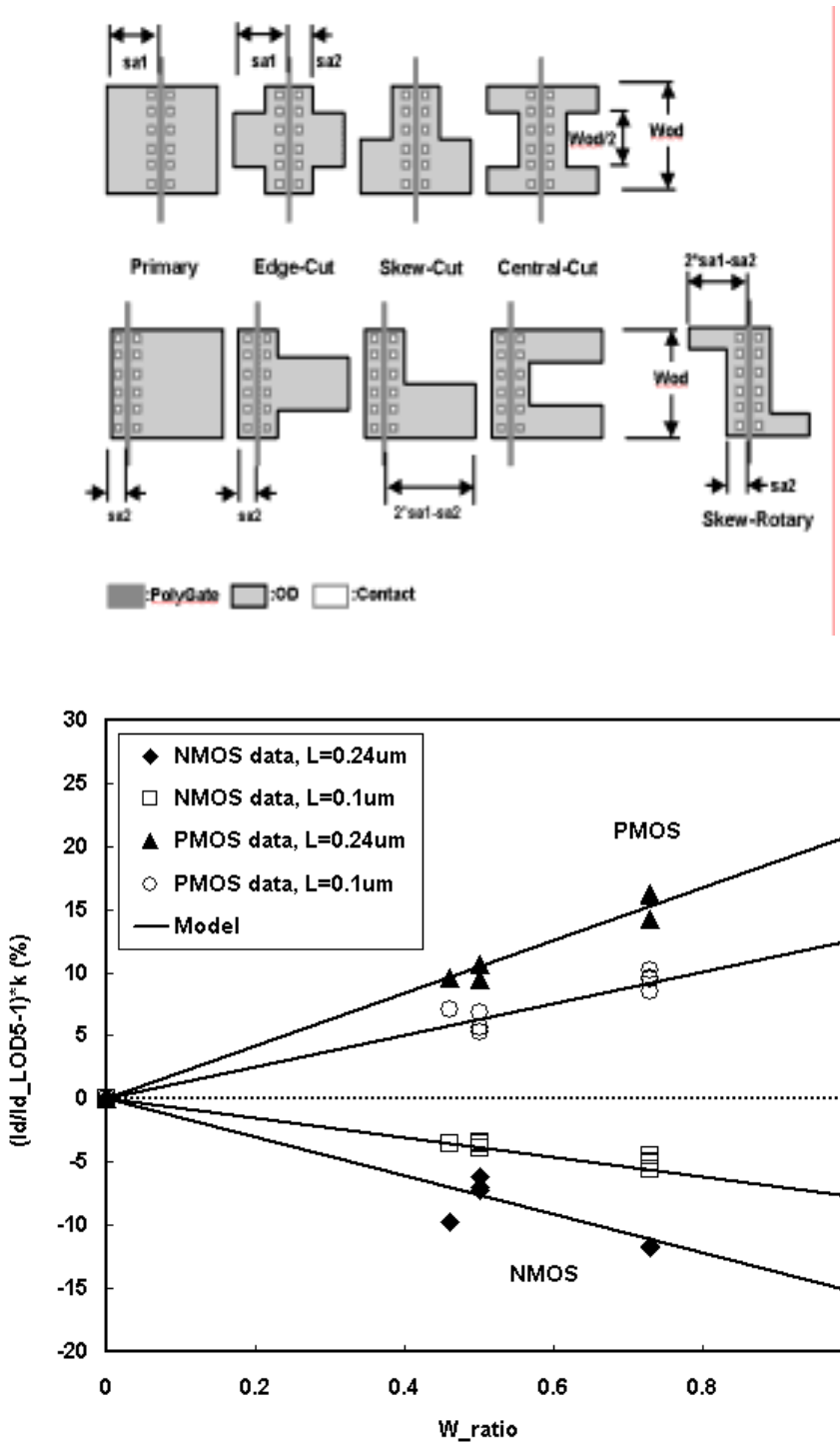

Fig. 3.22 Symmetric and asymmetric irregular layouts under study and the corresponding drain current shift in percentage.

Chapter 4
Well-Edge Proximity Effect

4.1 Preface

As CMOS VLSI technology progresses to the nanometer regime, several physical effects become significant as a result of aggressive layout scaling [4.1]-[4.3]. MOSFETs are formed during the front-end of the fabrication process, which mainly consists of shallow trench isolation (STI), MOSFET wells, and MOSFET gate formation. The effect of the well-edge proximity to the MOSFET gates was first reported by Hook [4.4] and originates from the lateral scattering of ion implantations at the photoresist edge when forming MOSFET wells, which in turn causes a change in the MOSFET threshold voltage.

In this chapter, a silicon wafer experiment was performed using state-of-the-art CMOS technology to investigate this effect. Monte Carlo ion scattering and integrated TCAD simulation was conducted to evaluate the dopant profile variations of the well ion implantation. The calibrated process and device TCAD simulations were used to quantify the impact on MOSFET electrical characteristics. Utilizing a physics-based understanding and silicon experimental results, a new model that corrects the inaccuracies of current SPICE models is proposed.

4.2 Ion Scattering Physics and Modeling

Moving ions (projectiles) in a solid lose their energy via two independent

mechanisms. The first mechanism is elastic nuclear stopping, which causes the ions to be scattered away from their original paths. The second mechanism is inelastic electronic stopping, which acts as a drag force causing negligible angular deflections of the moving ions.

The principal assumption of the Monte Carlo model is that the interaction of the energetic ions with the solid may be separated into a series of distinct two-body collisions (binary collision approximation). Thus, Monte Carlo modeling of ion implantation consists of following the ions from one scattering event to the next, and properly accounting for all energy loss mechanisms and deflections. The Monte Carlo model for implants into crystalline silicon was described in detail in [4.5]. Here, only the models pertaining to high-energy ion implantation into the photoresist will be discussed.

In the Monte Carlo model, the photoresist is treated as an amorphous material with the average path length of the ion between collisions being $l = 1/\sqrt[3]{N}$, where N is the atomic density of the photoresist. The collision partners are randomly selected, assuming that the probabilities of encountering each component of atoms are proportional to their stoichiometric abundances (assuming 50% hydrogen, 37.5% carbon, and 12.5% oxygen). For each collision, the impact parameter is determined by $p = \sqrt{R_n}\, p_{\max}$, where R_n is a uniformly distributed random number between 0 and 1, and p_{max} is the maximum impact parameter given by $l/\sqrt{\pi}$. The interactions between the ions and the target atoms are modeled using the Ziegler-Biersack-Littmark (ZBL) universal interatomic potential [4.6]. If the atomic

mass of the projectile is greater than that of the target atom, it can be shown that, for a single collision, a maximum scattering angle exists:

$$\theta_{\max} = \arcsin(\frac{m_2}{m_1}) \tag{4.1}$$

where m_1 and m_2 are the atomic mass of the projectile and the target atom, respectively. Therefore, although hydrogen is more abundant in composition, carbon and oxygen are more effective in deflecting the implanted ions. Most ions experience many collisions before they are scattered out of the photoresist.

For electronic stopping, the Lindhard-Scharff (LS) formula [4.7] is used:

$$S_e = \alpha \frac{1.212 Z_1^{7/6} Z_2}{[Z_1^{2/3} + Z_2^{2/3}]^{3/2} m_1^{1/2}} \sqrt{E} \tag{4.2}$$

where Z_1 and E are the atomic number and the kinetic energy of the projectile, respectively. Z_2 is the average atomic number of the photoresist, and α is an empirical correction factor. It is interesting to note that without any adjustment of the parameter α (=1), LS stopping power predicts the projected ranges of B and P implants below 1 MeV very well.

At high energy, the cross-section for nuclear scattering is small, and the ions experience very few nuclear collisions. Thus electronic stopping is the dominant energy loss mechanism. For example, for a B 300 keV implant, electronic stopping accounts for 88% of the total energy loss. In this energy regime, most ions move in approximately straight lines, and are rarely scattered out of the photoresist. As the ions slow down and approach their projected range, the nuclear scattering cross-section increases significantly, and nuclear stopping becomes dominant. After

experiencing many collisions, some ions are scattered out of the photoresist edge. Once an ion is scattered out of the photoresist, it is assumed to move in a straight line until it re-enters the silicon substrate. The exact entry point depends on the position at which the ion exits the photoresist, its direction of motion, and the topography of the device.

Fig. 4.2 shows the angular distribution and the depth distribution of the ions that are scattered out of the photoresist edge for B 300 keV and P 625 keV implants. Both of these dopants have approximately the same projected range at 1.08μm in the photoresist. It is worthwhile noting that, for the given implant conditions, the total number of ions that are scattered out of the photoresist is roughly the same for both B and P. It can also be seen that most ions are scattered out of the photoresist just before reaching the projected range. In addition, ions exit the photoresist edge with a peak at angle of ~10°, and a significant portion of ions exit with angles below 30°. Ions exiting at large angles may travel a long distance in a lateral direction and be implanted into the active area of the MOSFET. Thus, the dopant distribution due to the well-edge proximity effect can be accurately simulated using the Monte Carlo simulator.

4.3 TCAD Numerical Simulation

Full process two-dimensional TCAD simulation was performed to model MOSFET dopant distribution and electrical behavior. Monte Carlo well ion implantation mentioned in the previous section was applied to simulate the dopant

scattering effect at the edge of the well photoresist. The well to gate-edge distance is denoted as *SC*, and is shown in Fig. 4.1. Ions scatter from the well photoresist edges and are implanted into the silicon active areas when forming retrograde wells using high-energy boron and phosphorus ion implantations for n and pMOSFETs, respectively. Fig. 4.3 shows the simulation dopant distributions after the well ion implantations. In the graph for *SC*=0.9μm, the well dopant concentrations are low and almost constant at the silicon surfaces through the active area for both n and p-wells. As *SC* decreases to 0.54μm, several extra dopant clusters introduced from well-edge ion scattering can be observed at the STI and silicon surface near the well photoresist edges. When *SC* further decreases to 0.4μm, the extra dopant clusters move toward the center of the active area and the well dopant concentrations become higher in cases where the *SC* is larger. In Fig. 4.4, final vertical boron and phosphorus profiles along the MOSFET center for various well to gate edge distances are shown for n and pMOSFETs, respectively. The additional implants, besides the retrograde well implants, are boron 1.4×10^{13} cm^{-2} 100 KeV for the n-MOSFET and phosphorus 1×10^{13} cm^{-2} 240 KeV for the pMOSFET. As observed, the channel dopant concentration increases as the well photoresist edge approaches the MOSFET active area. To further quantify the extra dopant concentration introduced by well-edge ion scattering, the average dopant concentration for the area 20nm below the MOSFET gate versus *SC* were plotted in Fig. 4.5.

The silicon experiment using novel CMOS technology was conducted to explore the well-edge proximity effect. MOSFETs with various well to gate-edge

distances were designed, fabricated, and electrically measured. The process and device simulations were first calibrated according to a standard MOSFET set, in which the SC is larger than 10μm. Then simulations using various *SC* values were performed to obtain the threshold voltage trend of the MOSFET versus *SC*. Fig. 4.6 shows the matched result of silicon experiment and TCAD simulation.

4.4 Compact Model for SPICE

Since this new layout-dependent phenomenon increases the threshold voltage and thus decreases the drain current of the MOSFETs, it is especially important for those circuits with high integration density. This effect might also introduce uncertainties to those circuits that are sensitive to the matching of threshold voltage. Therefore, it is necessary to consider this effect in the SPICE simulation and the post-layout extraction flow. However, the most challenging part of a layout-dependent model is to determine a method of catering for various layout styles in as complete a manner as possible while retaining the efficiency of the procedure.

Fig. 4.7 shows typical several layout styles of a MOSFET in a well. As shown in Fig. 4.7(a) and (b), the well edges are close to the MOSFETs in the channel-length direction, and in Fig. 4.7(c) and (d) the proximity occurs in the channel-width direction. Narrow MOSFETs will have a strong well-edge proximity effect for layout (c) and (d) as a large portion of the channel region is influenced by the dopant ion scattering at the well edge. However, the MOSFET channel width does not play an

important role in layout (a) and (b). A useful compact model should cover each of these possibilities.

Fig. 4.8 is another generalized example to cover various layout conditions, including those shown in Fig. 4.7. From Fig. 4.8, the overall additional dose of dopant introduced by ion scattering at the well edges and that affect the channel region can be represented by the following integrals:

$$\text{additional\_dose} \propto \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \int_{SC_i}^{SC_i + L_{drawn}} f(x)dx \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \int_{SC_i}^{SC_i + W_{drawn}} f(y)dy \right) \right] \tag{4.3}$$

where f(x) is used to account for both the lateral and vertical distribution variations of the scattered well dopants. In some cases, f(x) might be a combination of several exponential terms. However, our analysis shows that $1/x^2$ is a good approximation for f(x) to cover most conditions. With this approximation, an effective device-to-well-edge distance, SC_{eff}, is proposed:

$$\begin{aligned} SC_{eff} &= \left\{ \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \int_{SC_i}^{SC_i + L_{drawn}} \frac{1}{x^2} dx \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \int_{SC_i}^{SC_i + W_{drawn}} \frac{1}{y^2} dy \right) \right] \right\}^{-0.5} \\ &= \left\{ \frac{1}{W_{drawn} \cdot L_{drawn}} \cdot \left[\sum_{i=1}^{n} \left(W_i \cdot \left(\frac{1}{SC_i} - \frac{1}{SC_i + L_{drawn}} \right) \right) + \sum_{i=n+1}^{m} \left(L_i \cdot \left(\frac{1}{SC_i} - \frac{1}{SC_i + W_{drawn}} \right) \right) \right] \right\}^{-0.5} \end{aligned} \tag{4.4}$$

Note that the SC_{eff} can easily summarize all four conditions shown in Fig. 4.7. A smaller SC_{eff} indicates that the MOSFET is closer to the well edge and the well-edge proximity effect will be more severe. Then, the impact of the well-edge proximity effect can be described by adding more SC_{eff}-dependent equations to the conventional model. Since the major effect is due to the MOSFET dopant profile change, three corresponding MOSFET parameters, threshold voltage, body effect coefficient, and carrier mobility, are modified to include the variations caused by this effect. The respective equations are shown as follows:

$$Vth0 = Vth0_{org} + \mathrm{KVTH0WE} \cdot \left(\frac{1}{\mathrm{SC_{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} - \frac{1}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} \right) \tag{4.5}$$

$$K2 = K2_{org} + \mathrm{K2WE} \cdot \left(\frac{1}{\mathrm{SC_{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} - \frac{1}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}} \right) \tag{4.6}$$

$$\mu_{eff} = \mu_{eff,org} \cdot \frac{1 + \dfrac{\mathrm{KU0WE}}{\mathrm{SC_{eff}}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}}}{1 + \dfrac{\mathrm{KU0WE}}{\mathrm{SCREF}^{\mathrm{NWE}} + \mathrm{SC0}^{\mathrm{NWE}}}} \tag{4.7}$$

where *Vth0* is the threshold voltage of the MOSFET, *K2* is the body effect parameter, and the μ_{eff} is the effective carrier mobility. SC_{eff} is the effective distance from the well edge to the channel region, which can be extracted from circuit layouts for each MOSFET by the layout parameter extraction (LPE) tools using equation (4.4). SCREF, SC0, KVTH0WE, K2WE, KU0WE, and NWE are the fitting parameters.

This model has been verified using various types of MOSFET layout patterns,

as shown in Fig. 4.7. Devices with different channel lengths and widths are also considered here in order to check the dependence of the well-proximity effect on W and L. Fig. 4.9, Fig. 4.10 and Fig. 4.11 show the comparison between the model and the silicon for the threshold voltage shift, drive current degradation, and body effect increase of MOS transistors. As shown in these plots, the correlation between the model and the silicon is quite reasonable. Note that no matter whether the device is close to the well edge either in the channel length or in the width direction, the concept of SC_{eff} can explain those differences and thus the data obtained from layouts illustrated in Fig. 4.7 show the same trend in the threshold voltage change (dVth) vs. SC_{eff} plot, as indicated in fig. 4.9. For those devices with smaller SC_{eff}, the threshold voltage will also increase further, but it may saturate at a certain value.

Fig. 4.10 shows the drive current degradation induced by the well-edge proximity effect. When SC_{eff} becomes smaller, the threshold voltage increases and thus the drive current will decrease. In addition to the V_{th} change, our analysis shows that the effective mobility is also degraded by the well-edge proximity effect. This is because the impurity scattering becomes more severe as the dopant concentration increases. Fig. 4.11 demonstrates the dependence of the body effect on the well-proximity effect. When SC_{eff} is small, the average doping density in the channel region will increase. Then the body effect (gamma) will become higher at the same time. The model is able to predict this change.

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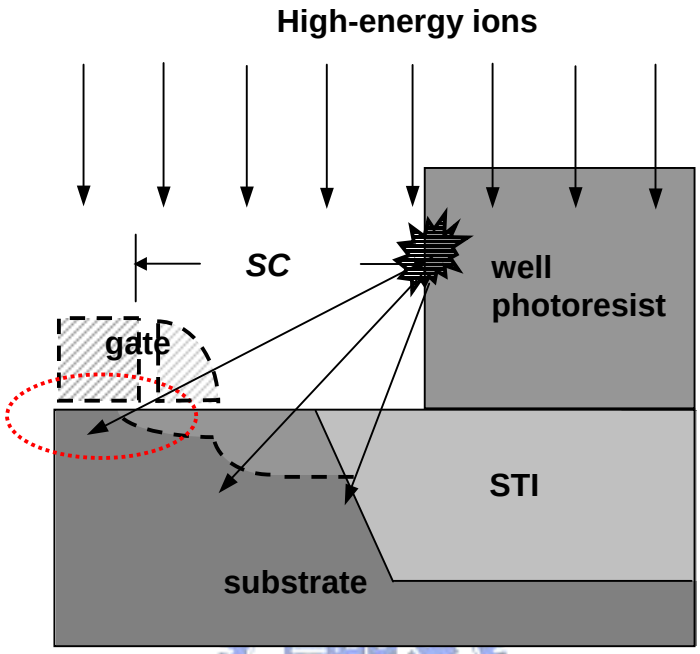

Fig. 4.1 Origin of well edge proximity effect. High-energy dopant ions scatter at the well photoresist edge during the well ion implantation and the scattered ions are implanted in the MOSFET channel before the gate is formed. *SC* denotes the distance of well-photoresist edge to MOSFET gate edge.

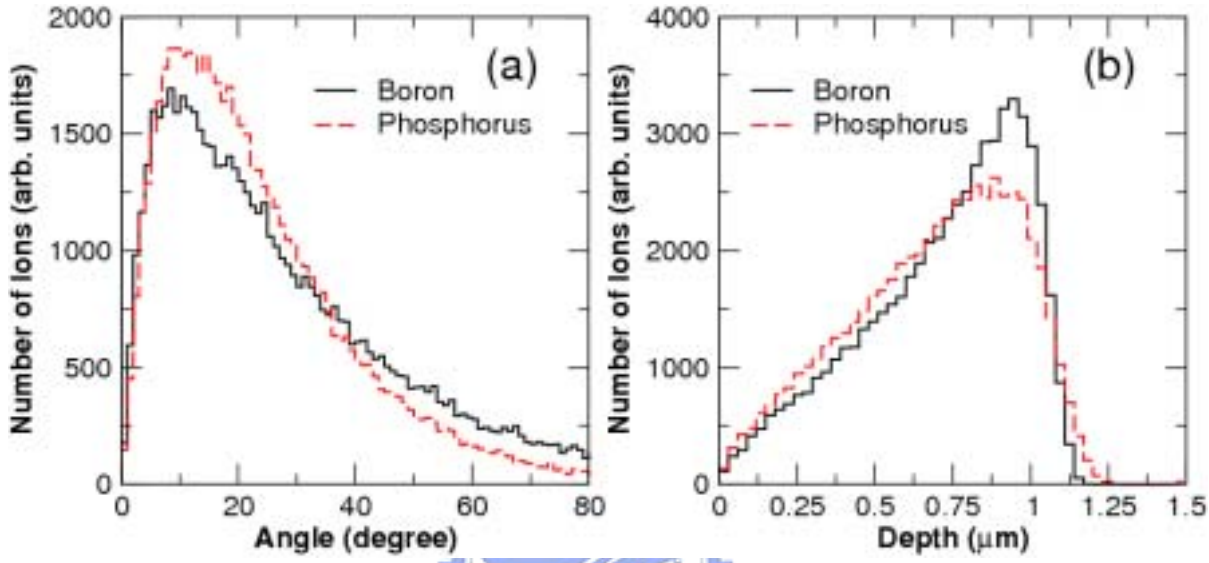

Fig. 4.2 (a) Angular and (b) depth distributions of the ions scattered out of the photoresist edge for B 300 keV and P 625 keV implants. The angle is measured from the incident direction, and the depth is the vertical distance from the top surface of the photoresist to the point where the ion exits from the photoresist edge.

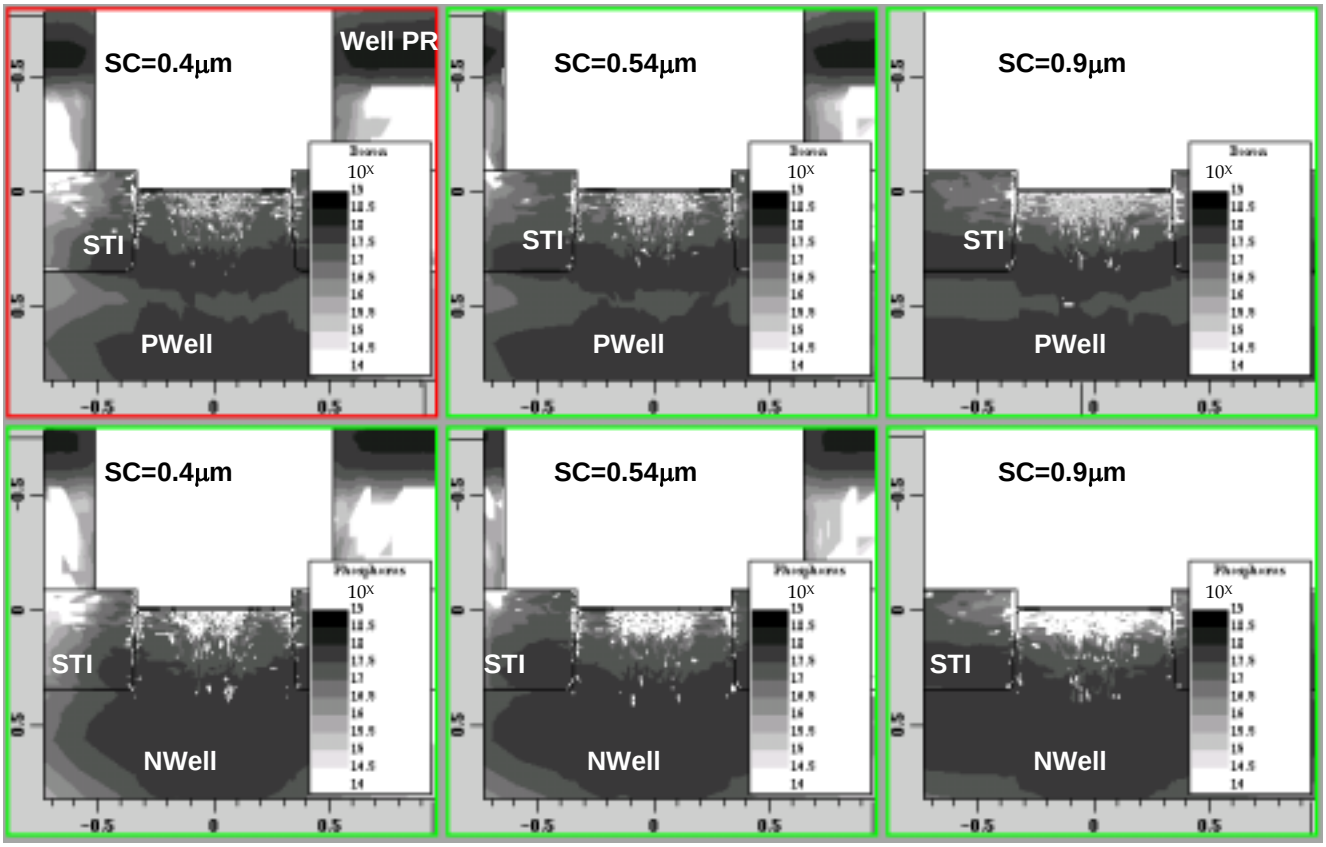

Fig. 4.3 TCAD simulated dopant distribution versus well to gate edge distance, SC. The well dopant distributions are influenced by the SC value. When SC decreases, extra well dopant clusters move toward the center of the active area.

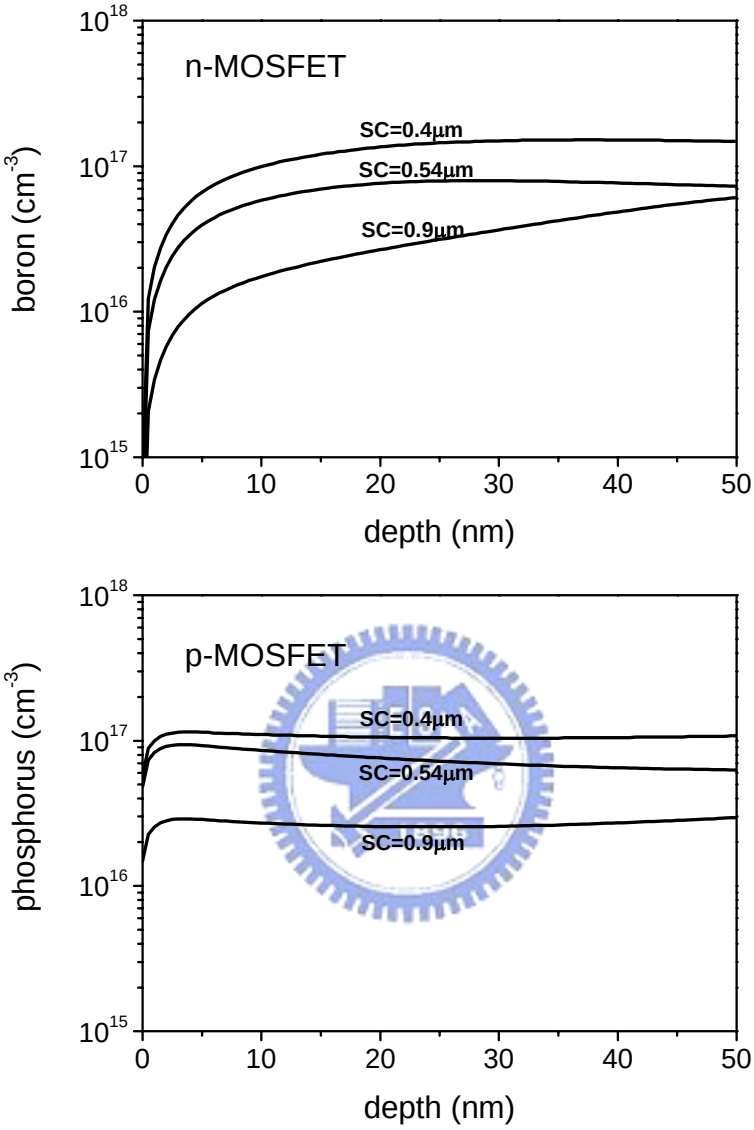

Fig. 4.4 TCAD simulated vertical channel dopant profile versus well to gate edge distance, SC. The channel dopant concentration increases as the well photoresist edge approaches the MOSFET active area.

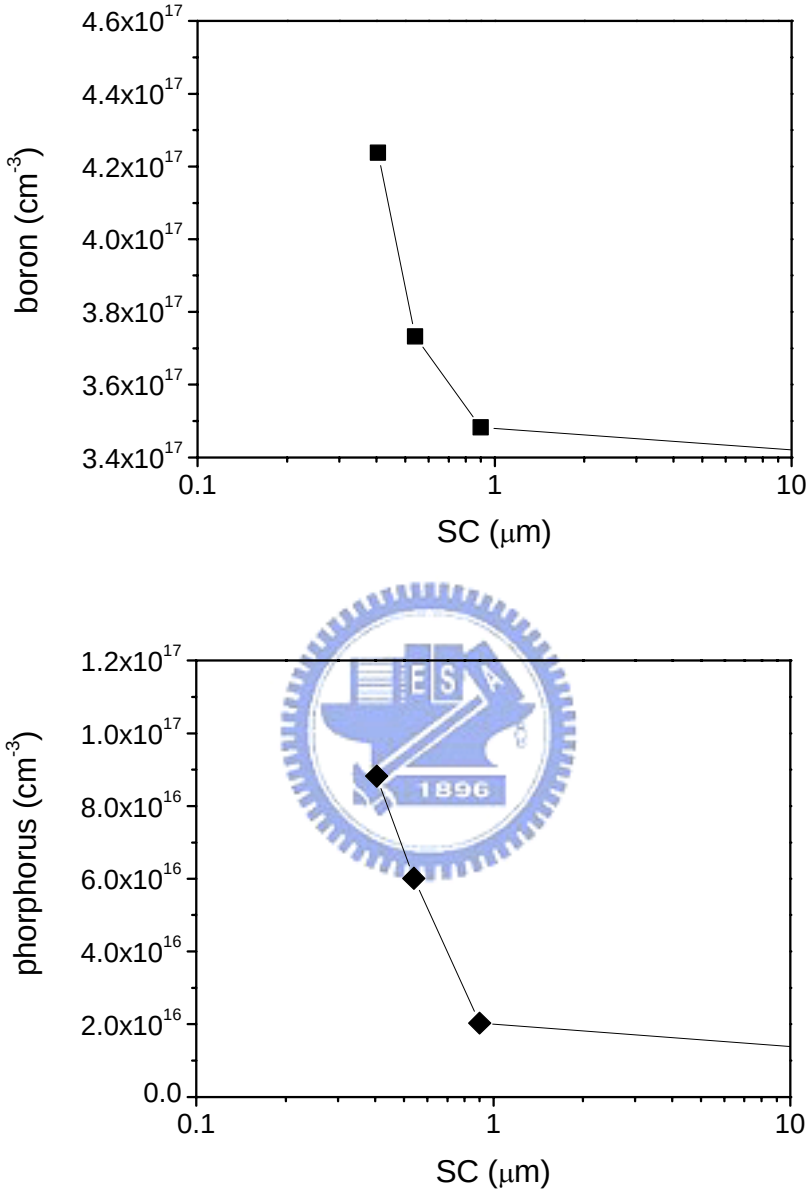

Fig. 4.5 TCAD simulated average dopant concentration for the area 20nm below the MOSFET gate versus SC.

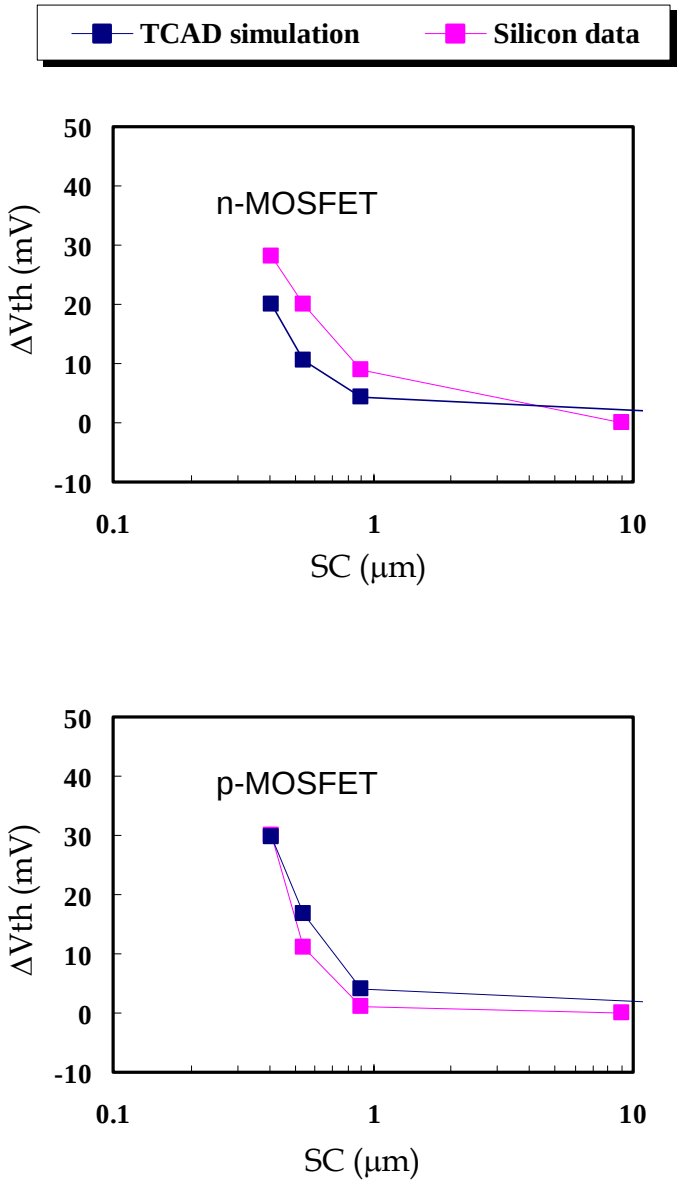

Fig. 4.6 MOSFET threshold voltage shift versus well to gate edge distance of the silicon experimental and TCAD simulated results for n and pMOSFET. Lg=0.216μm.

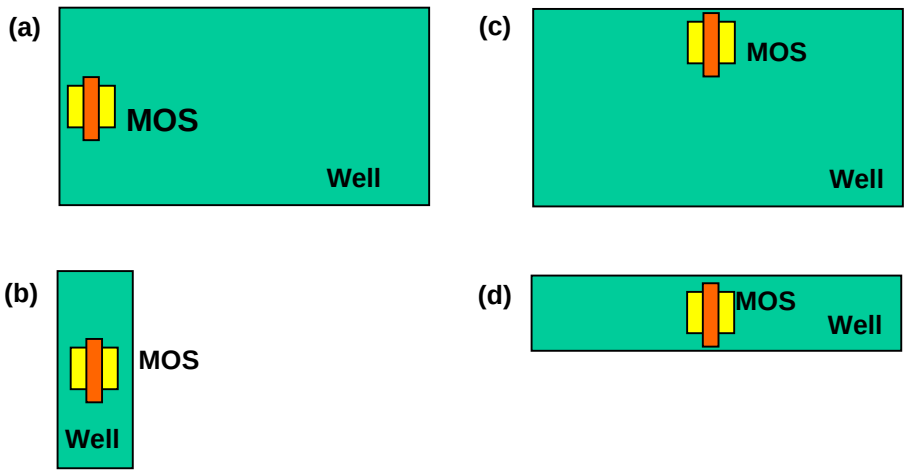

Fig. 4.7 Typical layouts showing different positions of MOS transistors in a well.

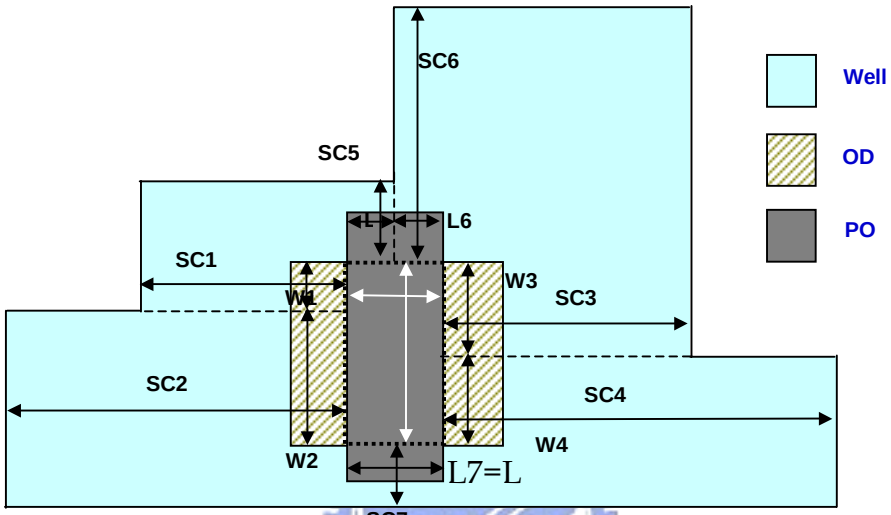

Fig. 4.8 Schematic presentation of a MOSFET layout and parameters used to establish a well-edge proximity SPICE model.

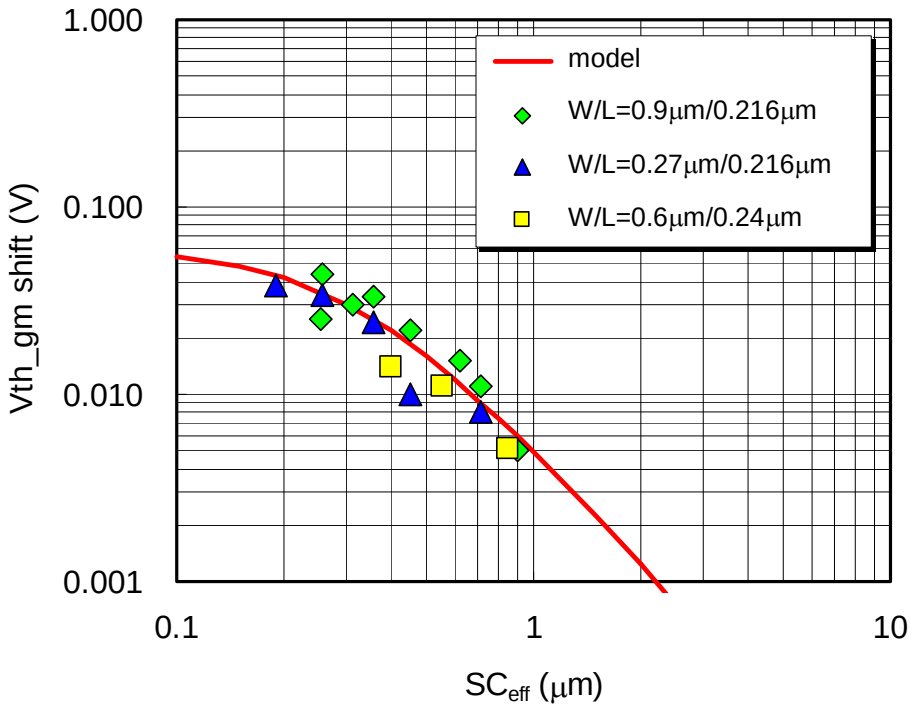

Fig. 4.9 Model verification results of the MOSFET threshold voltage shift compared to the silicon experiment data.

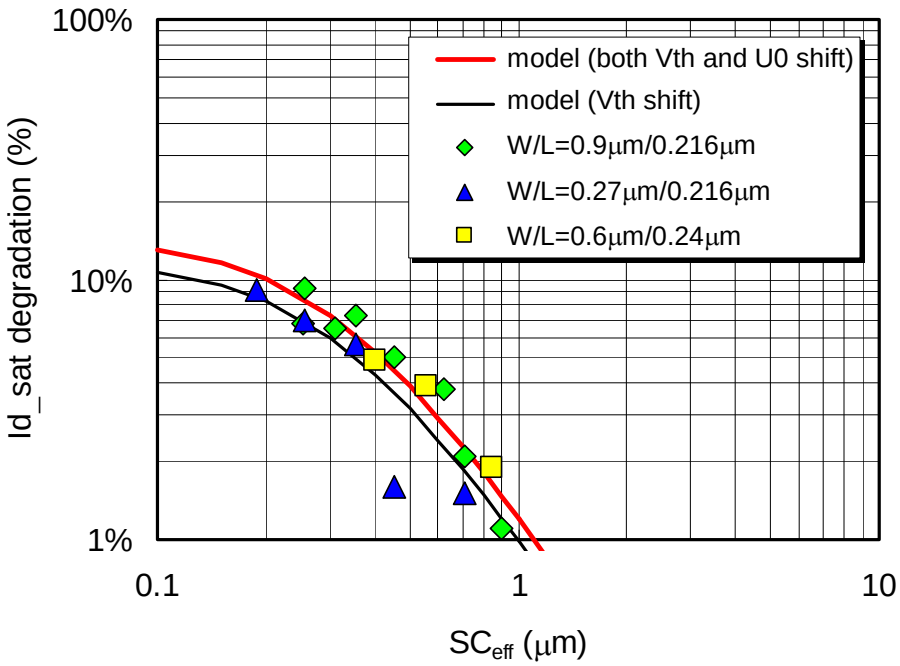

Fig. 4.10 Model verification results of the MOSFET drive current degradation compared to the silicon experiment data.

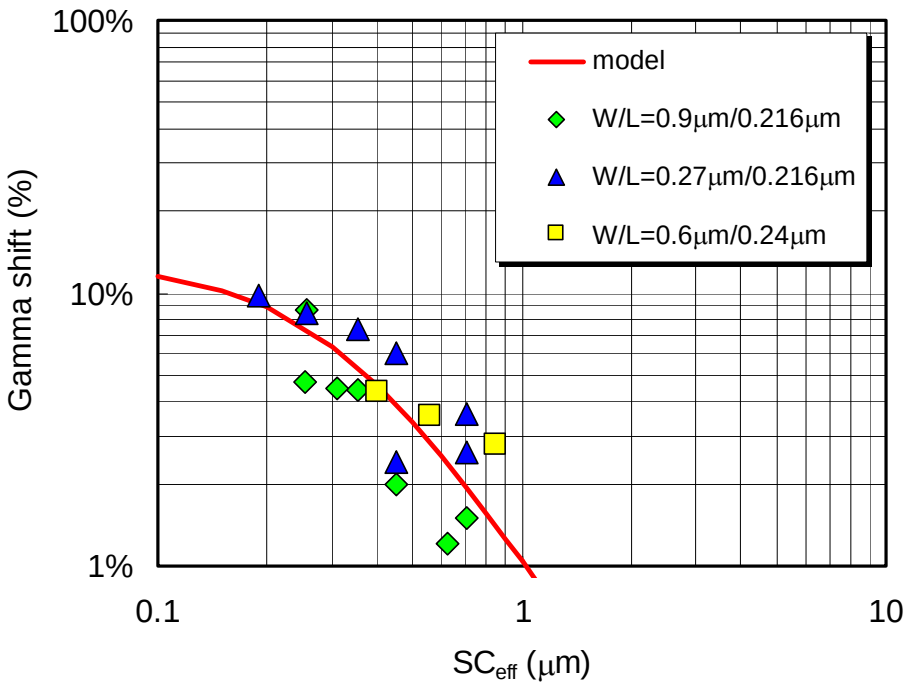

Fig. 4.11 Model verification results of the MOSFET body effect change compared to the silicon experimental data.

Chapter 5

Summary and Future Work

5.1 Summary

This dissertation concerns the accomplishment of exploring and modeling of two main layout dependent effects- mechanical stress and boundary dopant scattering during ion implantations on the modern MOSFETs.

The mechanical stress dependent dopant diffusion phenomenon is investigated through the wafer experiments using the sub-100nm CMOS technologies. An accurate stress-dependent dopant and point defects diffusion model is proposed. The model has been implemented into process and device simulators and has been validated by the extensive experimental data. A complete set of MOSFET devices with various gate lengths and active areas have been designed and fabricated from state-of-the-art sub-100nm process for model verification. Retarded dopant diffusion for phosphorus, boron, and arsenic has been observed and explained by calibrated dopant profiles while accurately accounting for silicon threshold voltage changes and I-V behaviors. The major benefit of this model is that only a single set of physically based diffusion parameters is required to reproduce device subthreshold characteristics for different active areas, gate lengths, drain voltages, and substrate biases. The proposed model therefore can serve as a compact and accurate method for practically dealing with STI mechanical stress dependent dopant diffusion in ULSI devices. A physical model dealing with anisotropic diffusion in uniaxially stressed silicon is also derived and is quantitatively connected to the

biaxial case. A process-device coupled simulation is performed on a p-type MOSFET undergoing uniaxial stress during the manufacturing process. A systematic treatment is conducted and the resulting fundamental material parameters are in satisfactory agreement with literature values.

For mechanical stress effect on the MOSFEST on-state characteristics, a well-planned active area layout experiment to examine STI mechanical stress effect on state-of-the-art bulk n and pMOS transistors; highlighting the effect of active area scaling and gate placement is demonstrated. Mechanical stress simulation yields compressive-type strain, successfully explaining experimental observations. Systematic analysis is then achieved, yielding striking results: (i) the experimental drive current sensitivity tracks the compressive-type strain along the channel well; (ii) the oxidation step after STI formation is identified the primary origin of the strain. A scaleable model for the mechanical stress effect on MOS electrical performance is also proposed. This model includes the influence of STI stress not only on the mobility and saturation velocity, but also on the threshold voltage and other important second-order parameters. Based on the model, new effective MOSFET active area length formulas are derived to improve the simulation efficiency and have been verified by data from various layouts. This model matches the measurement data well and is proven to be useful for circuit design in advanced CMOS technologies.

For the boundary dopant scattering effect during ion implantations, the well mask edge proximity is investigated. An experiment accounting for the impact of

this effect is conducted using a sub-100nm CMOS technology. Ion scattering models and TCAD simulations provide an internal view of the influence of this effect on the MOSFET. Additional SPICE models are established based on the physical understanding observed from the TCAD simulation and verified using the results from specially designed silicon experiment.

5.2 Recommendations for Future Work

The mechanical stress has become a major strategy for MOSFETs scaling in the advanced CMOS technologies. In this work, the isotropic stress-dependent diffusion model and anisotropic diffusion derivation for uniaxial stress cases have been developed and are sufficient to explain the experimental data. However, even stronger anisotropic stress can be expected in future technologies, and then a generalized anisotropic stress-dependent diffusion model for arbitrary stress conditions and the experiment designed for extracting the stress-dependent activation energies is necessary.

More mechanical stress simulations and analyses other than STI and oxidations, such as, silicon germanium/silicon carbon source and drain, strained cap layers and damascene gate are good topics for further studies on MOSFET performance improvements. Analytical stress-mobility models and stress induced band edge shift models can be implemented into the device simulators for more precise analyses on the stress induced MOSFEST on-state characteristics.

More boundary dopant scattering effects of the ion implantations other than

well formation ion implantations can be explored in the future. This topic can be combined with random dopant concentration fluctuation effects since the device scaling leads to limited counts of dopant atoms in a scaled MOSFET.

As the devices continued scaled, three dimensional (3-D) dopant diffusion, mechanical stress, and the boundary dopant scattering effects will also be more pronounced and need to be taken into considerations for the device design. Meanwhile, the three dimensional capability of TCAD tools needs to be improved on the numerical solving issues.

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16. (3 點) Ming-Jer Chen, and Yi-Ming Sheu, "Effect of uniaxial strain on

anisotropic diffusion in silicon," Appl. Phys. Lett., vol. 89, pp. 161908-1–161908-1, October 2006.

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Yi Ming Sheu Patent Filing List:

U.S.A. patent list:

1. Method of forming a self-aligned twin well structure with a single mask

Inventor: SHEU YI-MING (TW); YANG FU-LIANG (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US6703187.

2. Planarizing method for fabricating gate electrodes

Inventor: LIN YO-SHENG (TW); SHEU YI-MING (TW); LIN DA-WEN (TW); HSIEH CHI-HSUN (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US6670226.

3. Electrostatic discharge device protection structure

Inventor: CHAN YI-LANG (TW); YANG FU-LIANG (TW); SHEU YI MING (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US6800516.

4. Damascene gate electrode method for fabricating field effect transistor (FET) device with ion implanted lightly doped extension regions

Inventor: SHEU YI-MING (TW); CHAN YI-LING (TW); LIN DA-WEN (TW); LIEN WAN-YIH (TW); DIAZ CARLOS H (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US6673683.

5. Damascene gate electrode method for fabricating field effect transistor (FET)

device with ion implanted lightly doped extension regions

Inventor: DIAZ CARLOS H (US); SHEU YI-MING (TW); JANG SYUN-MING (TW); TAO HUN-JAN (TW); YANG FU-LIANG (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US6974730.

6. Narrow width effect improvement with photoresist plug process and STI corner ion implantation

Inventor: SHEU YI-MING (TW); LIN DA-WEN (TW); CHEN CHENG-KU (TW); YEH PO-YING (TW); PENG SHI-SHUNG (TW); WU CHUNG-CHENG (TW)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US7071515.

7. Recessed gate structure with reduced current leakage and overlap capacitance

Inventor: LIN DA-WEN (TW); SHEU YI-MING (TW); LEUNG YING-KEUNG (HK)

Applicant: TAIWAN SEMICONDUCTOR MFG

Patent no. US7012014.

中華民國專利：

1. 第 33 卷 31 期－公告編號 公告日期：95 年 11 月 01 日

專利名稱：積體電路裝置、半導體裝置及其製造方法

申請單位：台灣積體電路製造股份有限公司

申請案號：093136129 申請日期：93 年 11 月 24 日 專利證書號：I265638

發明人：鄭水明 、馮家馨 、程冠倫、許義明

2. 第 33 卷 15 期－公告編號 公告日期：95 年 05 月 21 日

專利名稱：電晶體元件與其形成方法及互補式金氧半元件的製造方法

申請案號：093102910 申請日期：93 年 02 月 09 日 專利證書號：I255530

申請單位：台灣積體電路製造股份有限公司

發明人：許義明、吳忠政

3. 第 33 卷 10 期－公告編號 公告日期：95 年 04 月 01 日

專利名稱：具有低電流洩漏及重疊電容之嵌壁式閘極結構

申請案號：093137422 申請日期：93 年 12 月 03 日 專利證書號：I252583

申請單位：台灣積體電路製造股份有限公司

發明人：林大文、許義明、梁英強

4. 第 31 卷 30 期－公告編號 公告日期：93 年 10 月 21 日

專利名稱：降低反窄通道效應之淺溝渠隔離製程

申請案號：092113971 申請日期：92 年 05 月 23 日 專利證書號：222701

申請單位：台灣積體電路製造股份有限公司

發明人：許義明、林大文、陳政谷、葉柏盈、彭世熊、吳忠政

5. 第 31 卷 04 期－公告編號 574746 公告日期：93 年 02 月 01 日

專利名稱：具凹陷通道之金氧半場效應電晶體之製造方法

申請案號：091136749 申請日期：91 年 12 月 19 日 專利證書號：196526

申請單位：台灣積體電路製造股份有限公司

發明人：卡羅司、許義明、章勳明、陶宏遠、楊富量

6. 第 31 卷 01 期－公告編號 569346 公告日期：93 年 01 月 01 日

專利名稱：在無邊界接觸窗製程中形成蝕刻終止層之方法

申請案號：091122713 申請日期：91 年 10 月 02 日 專利證書號：193690

申請單位：台灣積體電路製造股份有限公司

發明人：傅竹韻、謝奇勳、許義明、章勳明

7. 第 30 卷 32 期－公告編號 561506 公告日期：92 年 11 月 11 日

專利名稱：金氧半場效電晶體的製造方法

申請案號：091116299 申請日期：91 年 07 月 22 日 專利證書號：192142

申請單位：台灣積體電路製造股份有限公司

發明人：許義明、詹宜陵、林大文、連萬益、卡羅司

8. 第 30 卷 12 期－公告編號 529152 公告日期：92 年 04 月 21 日

專利名稱：汲極內具有缺陷區之靜電放電保護結構及其製造方法

申請案號：091100994 申請日期：91 年 01 月 22 日 專利證書號：176409

申請單位：台灣積體電路製造股份有限公司

發明人：詹宜陵、楊富量、許義明

9. 第 29 卷 31 期－公告編號 508727 公告日期：91 年 11 月 01 日

專利名稱：形成淺溝槽隔離結構之方法

申請案號：090122991 申請日期：90 年 09 月 19 日 專利證書號：166780

申請單位：台灣積體電路製造股份有限公司

發明人：陳方正、許義明、陶宏遠、邱顯光、張銘慶

10. 第 29 卷 26 期－公告編號 502315 公告日期：91 年 09 月 11 日

專利名稱：具有不同摻質之複晶矽層的製作方法

申請案號：090125933 申請日期：90 年 10 月 19 日 專利證書號：163288

申請單位：台灣積體電路製造股份有限公司

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