國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

超薄氧化層絕緣層上覆矽元件中軟式崩潰

所引發之可靠性議題的探討

Investigation of Soft Breakdown Induced Reliability Issues in Ultra-Thin Oxide SOI Devices

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摘要

當積體電路製程推進到奈米(sub-100nm)元件世代，絕緣層上覆矽技術的使用將是可行性的替代方案之一。當元件尺寸縮小到 100 奈米時，閘極介電層的等效氧化層厚度必須薄於 20 埃以下。然而，在如此薄氧化層的絕緣層上覆矽元件中，軟式崩潰所引發之可靠性問題將是異常重要。

本篇論文將針對超薄氧化層絕緣層上覆矽金氧半場效電晶體中軟式崩潰所引發之可靠性議題作一系列的探討。首先，吾人探討超薄閘極氧化層中直接穿隧區域的電荷傳輸機制。主要的閘極穿隧漏電流可以分成源/汲極穿隧電流和基底極穿隧電流。在此吾人利用一套量子化電荷傳輸機制來解釋源/汲極電流和用古典的電荷傳輸機制來解釋基底極電流。為了精準的模擬穿隧電流，吾人藉由解波松和薛丁格聯立方程式來計算氧化層電場。在超薄氧化層絕緣層上覆矽金氧半場效電晶體中，由於浮動基底極的原因，這些穿隧漏電流將對可靠性造成一些新奇的影響。

接下來，在浮動基底極絕緣層上覆矽元件中，吾人知道大量的基底漏電流所造成的基底電位的調變和所導致不可避免的磁滯效應已

被廣泛的討論。由於氧化層崩潰將增加基底極的穿隧漏電流，所以在浮動基底極的超薄閘極氧化層絕緣層上覆矽元件中，崩潰位置對臨界電壓磁滯現象的影響將在這部分探討。吾人將發表兩種在關閉狀態的金氧半電晶體中氧化層崩潰增強磁滯現象的模型。吾人所提供的基底充電機制和實驗結果相符。在浮動基底結構下的超薄閘極氧化層部份空乏絕緣層上覆矽金氧半場效電晶體中，軟式崩潰增強的磁滯現象將成為一種嚴重的可靠性議題。

再者，吾人發現在浮動基底絕緣層上覆矽金氧半場效電晶體中通道軟式崩潰導致一種新的低頻汲極電流雜訊退化現象。這種額外的雜訊來源來自於通道軟式崩潰導致大量基底極的價帶電子穿隧電流產生微量的白雜訊放大所致。在超薄閘極氧化層類比絕緣層上覆矽元件中，即使在操作電壓小於一伏特，通道軟式崩潰增加額外的雜訊仍會發生並將成為一個重要的可靠性問題。

最後，直接穿隧效應也會對超薄氧化層的崩潰及元件之毀壞產生影響。一般來說，元件的毀壞與否是由氧化層崩潰所造成破壞程度所決定，代表破壞程度較低的氧化層漏電流對實際電路應用而言，並不會造成任何操作上的影響。吾人在 p 型超薄氧化層絕緣層上覆矽電晶體中，針對浮動基底極對氧化層崩潰的破壞程度作完整之研究。在 p 型超薄氧化層元件中，吾人發現了正偏壓基底極操作模式下所產生的加速崩潰破壞。當氧化層初崩潰時，高能量的通道電洞在正偏基底極時產生較大的電動加壓電流，進而使得氧化層產生更大的破壞。藉由熱載子光激發實驗及熱電洞在通道能階上的分佈分析，吾人成功地解釋出此基底極偏壓相依性。吾人並預測此種崩潰破壞將對浮動基底超薄閘極氧化層絕緣層上覆矽 p 型金氧半場效電晶體產生新的可靠性議題。

Investigation of Soft Breakdown Induced Reliability Issues in Ultra-Thin Oxide SOI Devices

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Abstract

The silicon-on-insulator (SOI) technology is a promising candidate of IC manufacture required for sub-100nm CMOS devices. As device size shrinks below 100nm, the effective oxide thickness of gate dielectric must scale below 20Å. While, a great reliability concern induced by soft breakdown (SBD) in such thin oxides SOI devices is being aroused.

The objective of this dissertation is to investigate soft breakdown induced reliability issues in such ultra-thin oxide SOI MOSFETs. First of all, the charge transport mechanisms of oxide in direct tunneling regime is investigated. The gate tunneling leakage current can be separated by source/drain tunneling current and substrate tunneling current. In this work, a quantum charge transport mechanism is proposed to explain the source/drain current. And, a classical charge transport mechanism is proposed to explain the substrate current. To calculate the tunneling current accurately, the oxide electric field is simulated by means of solving the combined Poisson and Schrodinger equations. These tunneling leakage currents may bring about some reliability concerns in floating body ultra-thin oxide SOI

MOSFETS.

Further, substrate leakage current has been known to cause substrate bias variation and induce unavoidable hysteresis effects in floating body SOI devices. Since oxide breakdown can enhance substrate tunneling leakage current, the impact of breakdown location on threshold voltage hysteresis in ultra-thin oxide SOI devices is investigated in this part. Two breakdown enhanced hysteresis modes in off-state CMOS are identified. The proposed body charging mechanisms are verified by our measurement results. The SBD enhanced hysteresis effect would be a serious reliability subject in ultra-thin oxide MOSFETs with floating body configuration.

Moreover, a new low frequency drain current noise source in floating body SOI nMOSFETs caused by channel soft breakdown is studied. The excess noise originates from channel soft breakdown enhanced valence band electron tunneling and the amplification by the small white noise of the substrate current. The c-SBD enhanced excess noise may occur even with supply voltage less than 1.0V and would be an important reliability problem in analog applications.

Finally, a large direct tunneling current can decrease oxide time-to-breakdown and limit oxide further scaling. Actually in most circuits, the failure criterion is determined by the hardness of oxide breakdown. In this part, floating body enhanced breakdown progression in ultra-thin oxide SOI pMOS is proposed. The enhanced progression is attributed to the increase of hole tunneling current resulting from breakdown induced channel carrier heating. The substrate bias dependence of post-breakdown hole tunneling current is confirmed through the calculation of channel hole distribution in sub-bands. This observed phenomenon is significant to ultra-thin gate oxide reliability in floating body SOI pMOSFETs.

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首先，這本博士論文的完成，必須感謝我的指導老師汪大暉教授。他有深厚的理論基礎，再加上細心與耐心的指導態度，使得我很容易從他的隻字片語中學習到新的知識及觀念。最重要的是，在他身上感受到對學術的熱忱，並學習到做學問的方法和應有的嚴謹態度，以及面對問題時，該如何抽絲剝繭，最終能接近真相。

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最後，謹將這份榮耀獻給我最親愛的父母。

Contents

Figure Caption

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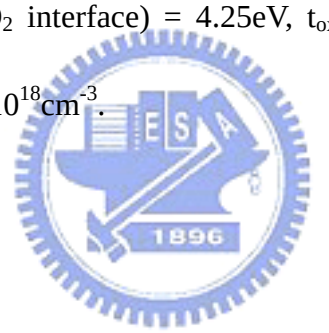

Chapter 1
Introduction

Gate oxide thickness scaling has been recognized as one of major keys in CMOS device scaling. With the device shrinkage, gate oxides below 2 nm are needed for sub-100nm CMOS technology. It is amazing that such thin oxide doesn't suffer much from extrinsic factors such as defect density, surface roughness and uniformity control. The physical limitation of oxide thickness is caused by quantum-mechanical tunneling of carriers. The direct tunneling current increases exponentially by about one order of magnitude for every 2~3Å reduction in oxide thickness [1.1]. Large tunneling currents with device scaling make oxide breakdown play an important role in reliability issues. Additionally, silicon-on-insulator (SOI) CMOS has been emerged as one promising solution to increase the performance of CMOS over that offered by simple scaling.[1.2,1.3] In bulk CMOS, the oxide soft breakdown (SBD) just increases the tunneling leakage current and does not disrupt circuit operation.[1.4] In fact, this unnecessary leakage current not only causes increased power dissipation but also may bring about some reliability subjects such as hysteresis effects, noise degradation and oxide breakdown in ultra-thin oxide SOI CMOS devices.

Partially Depleted (PD) SOI MOSFETs have the advantages in better threshold voltage control and easier fabrication process than fully depleted SOI MOSFETs. However, the floating body configuration of PD SOI MOSFETs has aroused several serious problems in device characteristics. An excess substrate leakage current can charge the substrate and cause annoying hysteresis effects. The SBD enhanced substrate tunneling leakage current may make the hysteresis effects more serious in PD SOI CMOS. The influence of SBD location on hysteresis effects in PD SOI MOSFETs will be investigated in various device operation modes.

High performance SOI MOSFETs have been the primary platform of RF and microwave

analogy circuits due to reduced junction capacitance and also due to the benefits of a high receptivity substrate.[1.5,1.6] Low-frequency noise is a key design constraint and an important figure-of-merit in analogy MOS circuits. Moreover, unwanted floating-body effects including the excess low-frequency noise have been extensively studied for SOI MOSFETs.[1.7,1.8] In this thesis, we will explore the noise properties of PD SOI MOSFETs in different SBD modes. The impact of SBD location on low frequency noise in SOI devices will be investigated in this thesis, too.

Time dependence dielectric breakdown (TDDB) is an important reliability index of ultra-thin gate oxide. Although stress oxide field of SOI MOSFETs is not varied by floating body induced forward substrate bias, the negative substrate bias may enhance the pMOS breakdown progression.[1.9,1.10] The comparison of breakdown hardness in SOI and bulk pMOSFETs will be discussed in this thesis. Our result shows that oxide breakdown rate is enhanced in SOI devices. This points toward that SBD will be an urgent reliability issue in ultra-thin PD SOI MOSFETs.

Organization of this Thesis

This thesis is organized into six chapters.

Following the introduction, the gate tunneling leakage current in n- and p- MOSFETs with ultra-thin oxide is calculated in Chapter 2. The gate leakage current contains quantum charge transport of inversion carrier (source/drain tunneling current, I_{sd}) and classical charge transport of valance band electron (substrate tunneling current, I_b). To calculate charge transport accurately, the Poisson and Schrodinger equations are solved self-consistently. The carrier energy quantization and corresponding wave-functions in the inversion layer are obtained from the Schrodinger equation. The ploy-gate depletion effect is investigated by solving the Poisson equation. A modified WKB approximation for charge transmission probability is employed in the calculation of the tunneling leakage current. The simulation of

C-V curves is also identified in this chapter.

The impact of oxide soft breakdown location on threshold voltage hysteresis in PD SOI MOSFETs with an ultra-thin oxide is investigated in Chapter 3. Two breakdown enhanced threshold voltage hysteresis modes are identified. In a drain-edge breakdown device, excess holes resulting from band-to-band tunneling flow to the floating body, thus causing threshold voltage variation in drain bias switching. In contrast, in a channel breakdown device, enhanced threshold hysteresis is observed during gate bias switching because of increased valence band electron tunneling. Our findings reveal that soft breakdown enhanced hysteresis effects can be a serious reliability issue in ultra-thin oxide SOI devices with floating body configuration.

In Chapter 4, a new low frequency noise degradation mode in nMOSFETs due to breakdown enhanced floating body effect is proposed. In a channel breakdown device, a noise overshoot phenomenon is observed in the ohmic regime. It is characterized by a peak in drain current noise spectral density versus the operation gate voltage, whereby the peak amplitude can be about one order of magnitude higher than the background 1/f noise. In addition, it is shown that the corresponding spectrum has a Lorentzian shape. The origin of this excess noise is due to c-SBD enhanced valance band electron tunneling induced amplification of the substrate shot noise. The excess low frequency noise model in SOI MOSFETs is also proposed. The findings indicate that c-SBD enhanced drain current noise can be a reliability issue in PD analog SOI CMOS circuit.

In Chapter 5, enhanced oxide breakdown progression in ultra-thin oxide SOI pMOS is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support our proposed theory. This phenomenon is particularly significant to the reliability of floating body SOI pMOS with thinner oxides and

lower gate voltage.

Conclusions are finally made in Chapter 6.

Chapter 2
Simulation of Charge Transport in Ultra-Thin Oxide MOSFETs

2.1 Introduction

With the continuing device scaling, gate oxides below 20Å are needed for sub-100nm CMOS technology [2.1]. In such small devices, the oxide field reaches a maximum of 5MV/cm, while the field in silicon exceeds 1 MV/cm [2.2,2.3]. The operation of deep-sub micron MOSFETs is entering a regime where quantum-mechanical effects become noticeable and classical physics is no longer sufficient for accurate modeling of device characteristics. The finite thickness of the inversion/accumulation layer (mostly due to quantum-mechanical effects) causes a significant discrepancy between calculated oxide capacitance and measured result [2.4]. In addition, as the surface electric field continues to increase due to oxide thickness scaling, the poly-silicon gate depletion effects appear to be more significant [2.5]. The depletion can further reduce the measured gate capacitance and degrade the charge control capability for a given gate bias. Furthermore, substantial charge tunneling through the gate insulator takes place even at operating biases as low as 1-1.5V. This gate leakage current increases exponentially as the oxide thickness is decreased and eventually becomes a limiting factor in device off-state leakage. Consequently, future low-voltage circuits may operate with considerable gate-oxide tunneling [2.6]. Therefore, the tunneling behavior of carriers through ultra-thin oxides must be well understood for future technology development.

In this chapter, the C-V and I-V characteristics of ultra-thin oxide n- and p-MOSFETs will be simulated and measured. A quantum-mechanical approach is developed to study some major concerns for ultra-thin oxide MOS structures, such as surface quantization and poly-gate depletion. The Poisson and the effective-mass Schrodinger equations are solved self-consistently in our simulation. Simulated results are found to be in agreement with experimental results. In this work, the devices have a large area (3μm*300μm) and the C-V

and I-V measurements are performed by using HP 4284 and HP4156B.

2.2 Surface Quantization and Gate Capacitance Modeling

In this section, we will discuss the Schrodinger and the Poisson equations first. Then, we will show the flowchart for a self-consistent solution of those equations. Finally, the measurement and simulation results of C-V curve will be presented and discussed.

2.2.1 Simulation Model for Potential Distribution

When energy bands are bent strongly near the Si substrate surface, the potential well formed by the surface barrier and the electrostatic potential in the Si substrate is sufficiently narrow that quantum-mechanical effects become important [2.7]. Only a single carrier needs to be treated quantum-mechanically when confined by the surface potential. For example, at a positive gate bias in a nMOSFET only surface electrons have quantum confinement effect while the surface holes do not exhibit quantization effects. When the carriers are confined, the electrical characteristics of an MOS structure should be modeled by solving the coupled effective-mass Schrodinger (in the oxide and silicon regions) and Poisson equations (in the poly-silicon, gate dielectric, and silicon regions) self-consistently. A closed quantum mechanical system is assumed, i.e., the tunneling current in oxides is neglected while solving the Schrodinger equation [2.8,2.9]:

$$[-\frac{\hbar^2}{2}\frac{d}{dz}\frac{1}{m_i^*}\frac{d}{dz}+V(z)-E_{ij}]\psi_{ij}(z)=0 \qquad (2\text{-}1)$$

and

$$\frac{d}{dz}[\varepsilon(z)\frac{d}{dz}]\varphi(z) = \frac{q}{\varepsilon_0}[n(z) - p(z) + N_A^- - N_D^+] \quad (2\text{-}2)$$

where z is the direction perpendicular to the channel, m_i^* is the electron effective mass in the ith valley , ψ_{ij} is the envelope wave function for the jth sub-band in the ith valley, V is the potential energy, and N_A^- and N_D^+ are respectively the ionized acceptor concentration and donor concentration. The potential energy V(z) in Equation (2-1) is related to the electrostatic potential φ(z) in Equation (2-2) as follows:

$$V(z) = -q\varphi(z) + \Delta E_C(z) \quad (2\text{-}3)$$

where $E_C(z)$ is the energy due to the band offset at the Si/SiO_2 interface. The wave function ψ(z) [2.10] in Equation (2-1) and the electron density n(z) in Equation (2-2) are related by

$$n(z) = \frac{k_B T}{\pi\hbar^2}\sum_i g_i m_{di}^* \sum_j \ln[1+\exp((E_f - E_{ij})/k_B T))]\psi_{ij}^2(z) \quad (2\text{-}4)$$

where g_i and m_{di}^* are the ith valley degeneracy and the ith density-of-states effective mass. The equations describing hole quantization are similar to Equations (2-1)-(2-4).

The dielectric constant ε(z) is 11.7 for Si and poly-silicon, and 3.9 for SiO_2. The boundary condition for the charge wave function at the poly-silicon/SiO_2 interface is set to be zero; i.e., there is no tunneling current. The electron wave function obtained here is a starting approximation. To accurately model the poly-silicon depletion effect, the free-carrier density in the poly-silicon region is described by the Fermi-Dirac statistics and an incomplete ionization model [2.11]. The charge-balance equation for heavily doped n-type poly-silicon is

$$\frac{2}{\sqrt{\pi}} N_C F_{1/2}(\eta_f) = \frac{N_D}{1+2\exp(\eta_f)} \tag{2-5}$$

where N_C is the effective density of states in the conduction-band, $F_{1/2}(\eta_f)$ [2.12] is the Fermi-Dirac integral, and $\eta_f = (E_f - E_C)/k_B T$.

2.2.2 Self Consistent Solution of Schrodinger's and Poisson's Equations

Fig. 2.1 shows the flowchart of the potential and quantization effect simulation. First, we need to make space discretion for numerical calculation. Then we give an initial guess of the potential distribution in the vertical direction. To get the wave function of each state, we must step by step find the eigen-energies by solving the Schrodinger equation with the aforementioned boundary condition. The eigen-functions are shown in Fig. 2.2. By using the same method, we can obtain the lowest six eigen-state energies and corresponding wave functions in Fig. 2.3. From the wave functions, we can evaluate the corresponding charge distribution in the quantum well. Then the charge distribution is fed back to the Poisson equation to update the potential distribution. This iteration process is continued until a self-consistent charge distribution and potential distribution is achieved. By using such result, we can further evaluate the charge transport in oxides. The differences of the electron and hole distributions in the Si substrate from the quantum approach and from the classical Boltzaman or Fermi-Dirac statistics are shown in Fig. 2.4 and Fig. 2.5. The peak of the carrier density from the quantum approach is about 10Å away from the surface while the classical statistics predicts a peak value at the surface. Such difference may cause a significant error in the C-V characterization.

2.2.3 Gate Capacitance Modeling

The gate capacitance of a semiconductor layer in a MOSFET's, C, for an ideal MIS

structure can be calculated as

$$C = \frac{dQ}{dV} \tag{2-6}$$

where Q is the total surface charge density in the semiconductor and V is the surface potential. The net charge in the Si substrate should be equal to the integral of the substrate field as follows;

$$Q = -\int_s P \cdot a_n ds = \int_s E \cdot ds \tag{2-7}$$

where P is the polarization vector and a_n is the outward normal vector. From Eq (2-7) we can calculate the gate capacitance C_g by

$$C_g = \frac{d\varepsilon_{ox} E_{ox} S}{dV_g}, \text{and } S=WL \tag{2-8}$$

where ε_{ox} is the electrical permittivity of SiO_2, E_{ox} is the gate oxide field, W is the gate width and L is the gate length. We can solve Eq (2-1) and Eq (2-2) numerically to get the oxide field [2.13-2.16].

Then, we calculate the C-V characteristics from our numerical simulation. We find that it can fit the measurement data well by choosing reasonable oxide thickness, poly-gate doping concentration and substrate doping concentration. In Fig. 2.6 and Fig. 2.7, the simulation results and measurement data of n-MOSFET and p-MOSFET are shown.

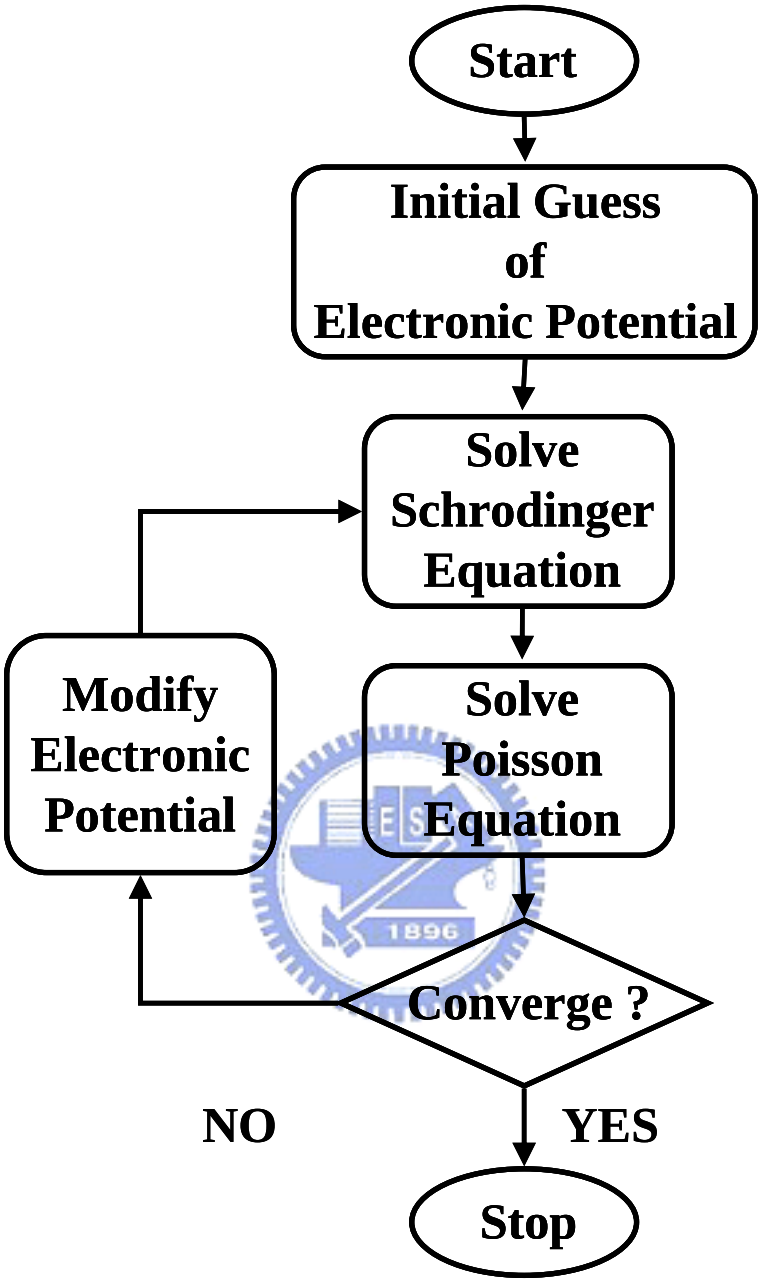

Fig.2.1 Algorithm to solve Poisson's and Schrodinger's equations self-consistently.

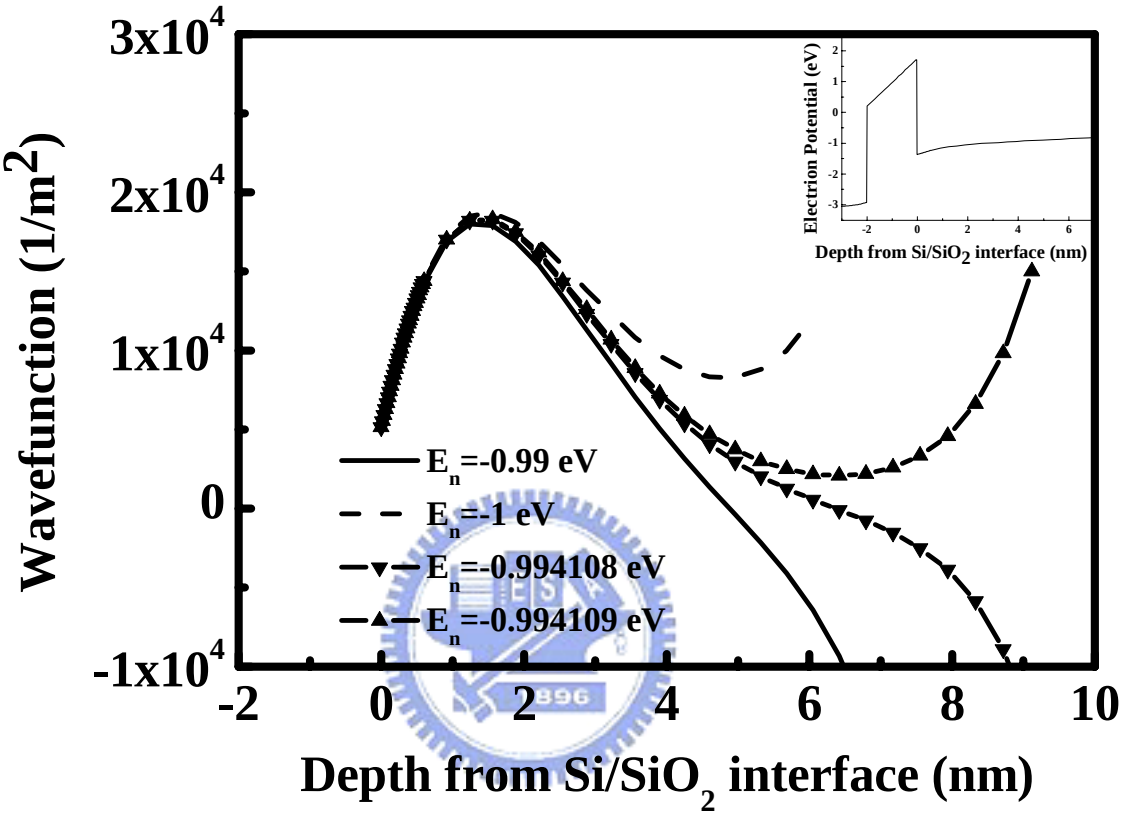

Fig.2.2 Sub-band wave-functions in substrate calculated from a pre-guessed potential.

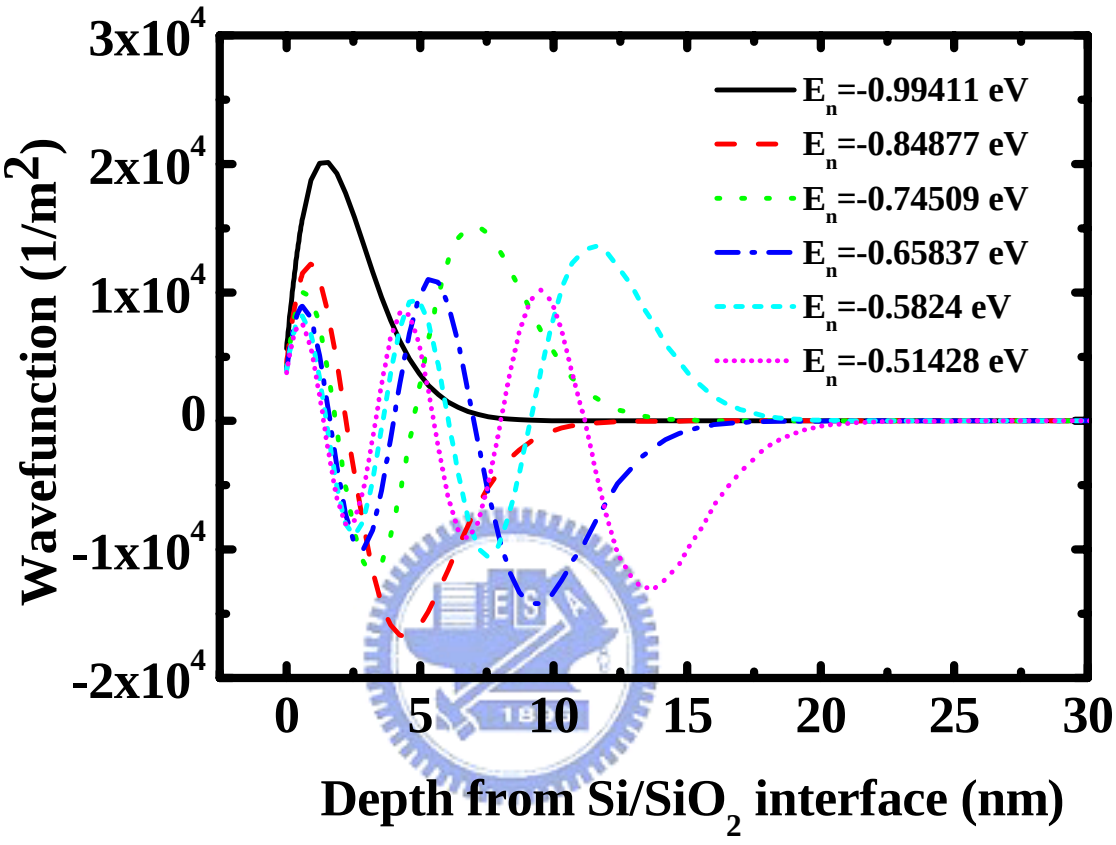

Fig.2.3 Six state wave-functions and energy levels from a pre-guessed potential.

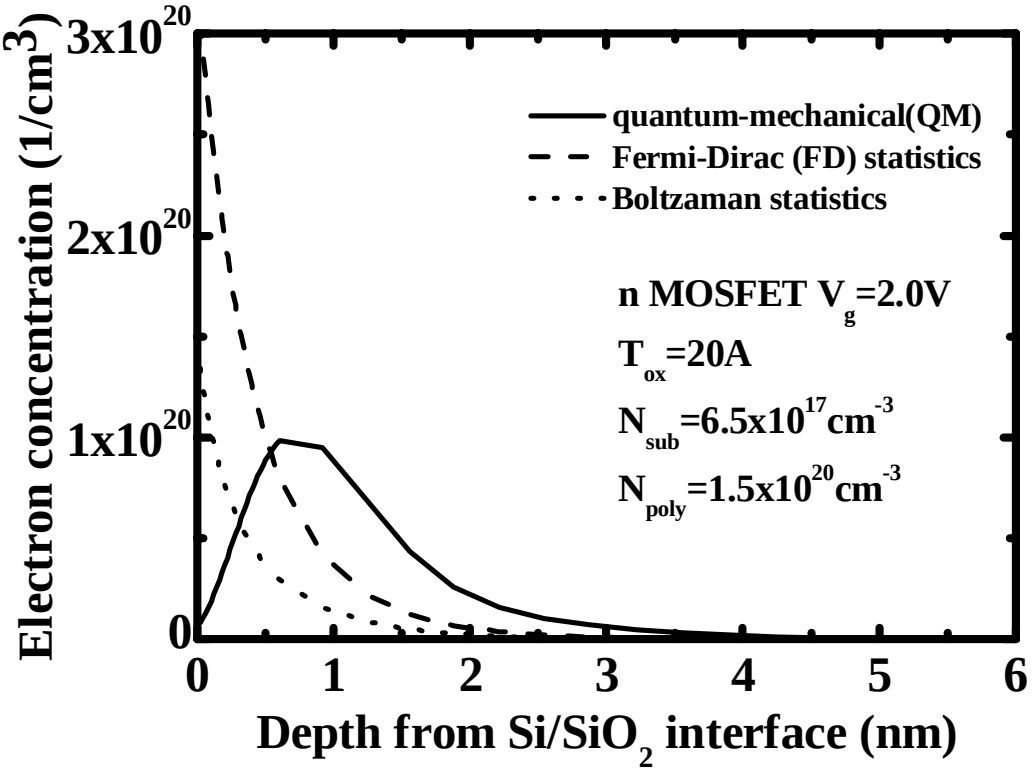

Fig.2.4 Electron distributions calculated from classical and quantum-mechanical models.

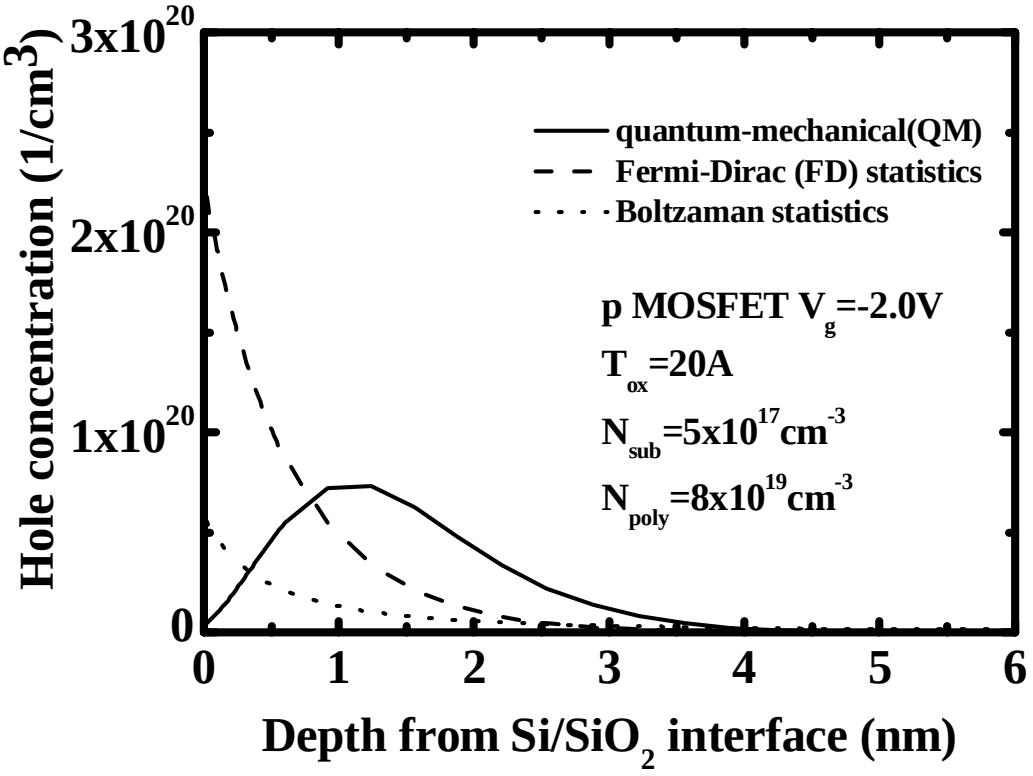

Fig.2.5 Hole distributions calculated from classical and quantum-mechanical models.

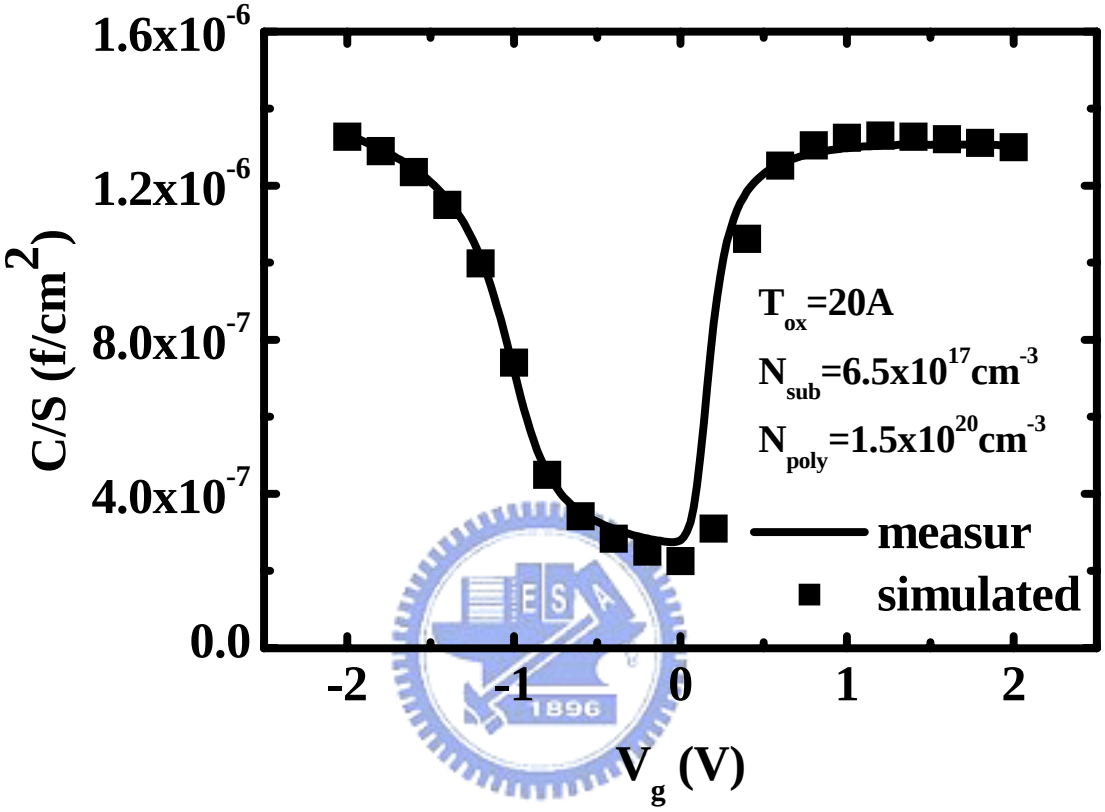

Fig.2.6 Measured and simulated C-V curves of an n-MOSFET device.

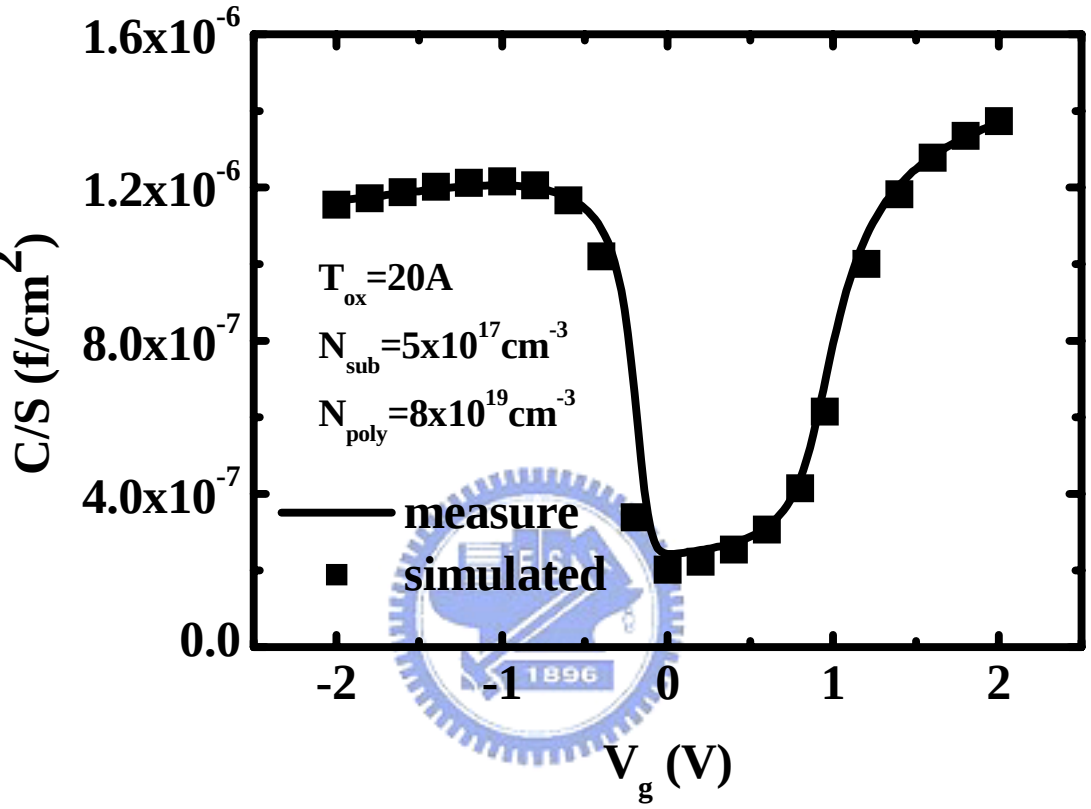

Fig.2.7 Measured and simulated C-V curves of a p-MOSFET device.

2.3 Source/Dreain Tunneling Current Modeling

In this section, the conduction (valance) band electron (hole) tunneling current model will be derived to calculate the source/drain tunneling leakage current of nMOSFETs (pMOSFETs). The quantum interference effect is taken into account by solving the tunneling probability exactly. Then, we will discuss the measured and simulated source/drain tunneling leakage currents.

2.3.1 Transport of Conduction Band Electrons

For a three-dimensional (3D) system the number of allowed wave vectors k per unit volume of k-space and per unit volume in real space is $1/(2p)^3$. The number of allowed k within the volume $dk_X dk_Y dk_Z$ in k-space is thus $(dk_X dk_Y dk_Z)/(2p)^3$. Here, x is defined as the direction perpendicular to the Si/SiO_2 interface while y and z indicate the directions parallel to the Si/SiO_2 interface. All the electrons located within $(dk_X dk_Y dk_Z)/(2p)^3$ contribute to an infinitesimal tunneling current expressed by

$$j_{si\to poly} = qnv_x = q(((dk_x dk_y dk_z)/(2\pi)^3)\cdot n_v \cdot 2\cdot f'\cdot D\cdot(1-f))v_x \qquad (2\text{-}9)$$

where q is the electron charge, n is the number of tunneling electrons, v_X is the electron group velocity, n_V is the valley degeneracy factor, the factor 2 accounts for the electron spin degeneracy, D is the tunneling probability, and f and f' are the Fermi-Dirac distributions in the substrate and gate electrodes, respectively. Thus, the conduction band electron tunneling current density can be obtained from the summation of Eq. (2-9) over all energy state in the conduction band. Because D depends only on energy in x-direction and v_X can be written as

$$v_x = (1/\hbar)(\frac{\partial E_x}{\partial k_x}) \qquad (2\text{-}10)$$

the tunneling current density from the substrate to the gate becomes

$$j_{si\to poly} = (qn_v)/(4\pi^3\hbar)\sum_{E_x=0}^{\infty}\int_{k_y}\int_{k_z} Df(1-f')dk_z dk_y \tag{2-11}$$

Similarly, the tunneling current density from the gate to the substrate has the following from

$$j_{poly\to si} = (qn_v)/(4\pi^3\hbar)\sum_{E_x=0}^{\infty}\int_{k_y}\int_{k_z} D' f'(1-f)dk_z dk_y \tag{2-12}$$

where D' is the tunneling probability in the reverse direction and D=D' [2.17]. The net conduction band electron tunneling current density j is the difference between Eq. (2-11) and Eq. (2-12).

E_X is the energy level measured from the conduction band-edge of the substrate. The surface quantization effect is included in the simulation, as shown in Fig. 2.8. As a result, the net tunneling current density has the following from

$$j = (qn_v)/(4\pi^3\hbar)\sum_{E_x=0}^{\infty}\int_{k_y}\int_{k_z} D'(f-f')dk_z dk_y \tag{2-13}$$

By using the Fermi-Dirac distribution and transforming the rectangular coordinates in k-space to the polar coordinates, we have

$$f = 1/(1+\exp(((E-E_f)/(k_B T))) \tag{2-14}$$

where E is total energy of the electron, E_f is the Fermi level, k_B is the Boltzman constant, and T is the absolute temperature, and we get

$$\int_{all\ k_y}\int_{all\ k_z} f dk_z dk_y = \int_{k_{//}=0}^{\infty}\int_{\theta=0}^{2\pi}(k_{//}\, d\theta dk_{//})/(1+\exp((E-E_f)/(k_B T))) \tag{2-15}$$

where $k_{//}$ represents the wave vector parallel to the Si/SiO_2 interface. Because of $E=E_{//}+E_x$ ($E_{//}$ is the electron energy parallel to the tunneling interface), if we assume there exists a parabolic $E_{//}$-$k_{//}$ relationship, i.e.

$$E_{//} = (\hbar^2 k_{//}^{\ 2})/(2m_{//}^*) \quad \text{,thus} \quad dE_{//} = (\hbar^2 k_{//} dk_{//})/(m_{//}^*) \tag{2-16}$$

($m_{//}^*$ is the electron effective mass parallel to tunneling interface).

In accordance with the Fermi-Dirac Integral with zero exponent [2.18],

$$F_0(\xi) = \int_0^{\infty} d\xi/(1+\exp(\zeta-\xi)) = \ln(1+\exp(\xi)) \tag{2-17}$$

Eq (2-15) reduces to

$$\begin{aligned} &2\pi m_{//}^*(1/\hbar^2)\int_0^{\infty} dE_{//}/(1+\exp((E_x+E_{//}-E_f)/(k_B T))) \\ &= 2\,p m_{//}^*(1/\hbar^2)k_B T\cdot\ln(1+\exp((E_f-E_x)/(k_B T))) \end{aligned} \tag{2-18}$$

Similarly, the summation of f' over k_y and k_z (refer to Eq (2-13)) can be obtained, and has the same expression as Eq (2-18) except that E_f is replaced by $E_{f'}$. Substituting them into Eq (2-13), the net tunneling current density can be rewritten as

$$qn_v m_{//} * (1/(2\pi^2\hbar^3))k_B T \sum_{E_x=0}^{\infty} D\{\ln(1+\exp((E_f - E_x)/(k_B T))) - \ln(1+\exp((E_{f'} - E_x)/(k_B T)))\} \quad (2\text{-}19)$$

This is just the Tsu-Esaki equation [2.19].

The probability $D(E_X)$ that an electron can penetrate a potential barrier height V(x) could be given by the well-known WKB approximation[2.20]:

$$D(E_x) = \exp\{-2\int_{x_0}^{x_s} dx(\sqrt{2m*(V(x)-E_x)/\hbar^2})\} \quad (2\text{-}20)$$

where m^* is the isotropic effective mass inside the potential barrier, E_X is the energy component of the incident electron in the x direction, and x_0 and x_S are the classical turning points. WKB approximation considers only the barrier between x_0 and x_S, and the WKB tunneling probability of a trapezoidal potential barrier is therefore a monotonically decreasing function of applied voltage.[2.21-2.25]

2.3.2 Simulated and measured results

In Fig 2.8, we known that the source/drain tunneling current is treated as the conduction(valance) band electron(hole) tunneling current in n-MOSFET(p-MOOSFET). In Fig. 2.9 and Fig. 2.10, we find that the simulation results of the I_{sd}-V_g in the inversion region are good agreement with the measurement data in n-MOSFET and p-MOSFET with the same device parameters as in section 2.2. In other words, we can use the same set of parameters to fit the measured I-V reasonably well. The barrier height of the conduction (valance) band is set to be 3.05 (4.17) eV and the image lowering effect is neglected. In the next section, we

will consider the valence band tunneling to complete the gate tunneling current simulation. Moreover, since the valence band electrons do not have surface quantization effect, it will become relatively simpler to calculate the valence band tunneling current.

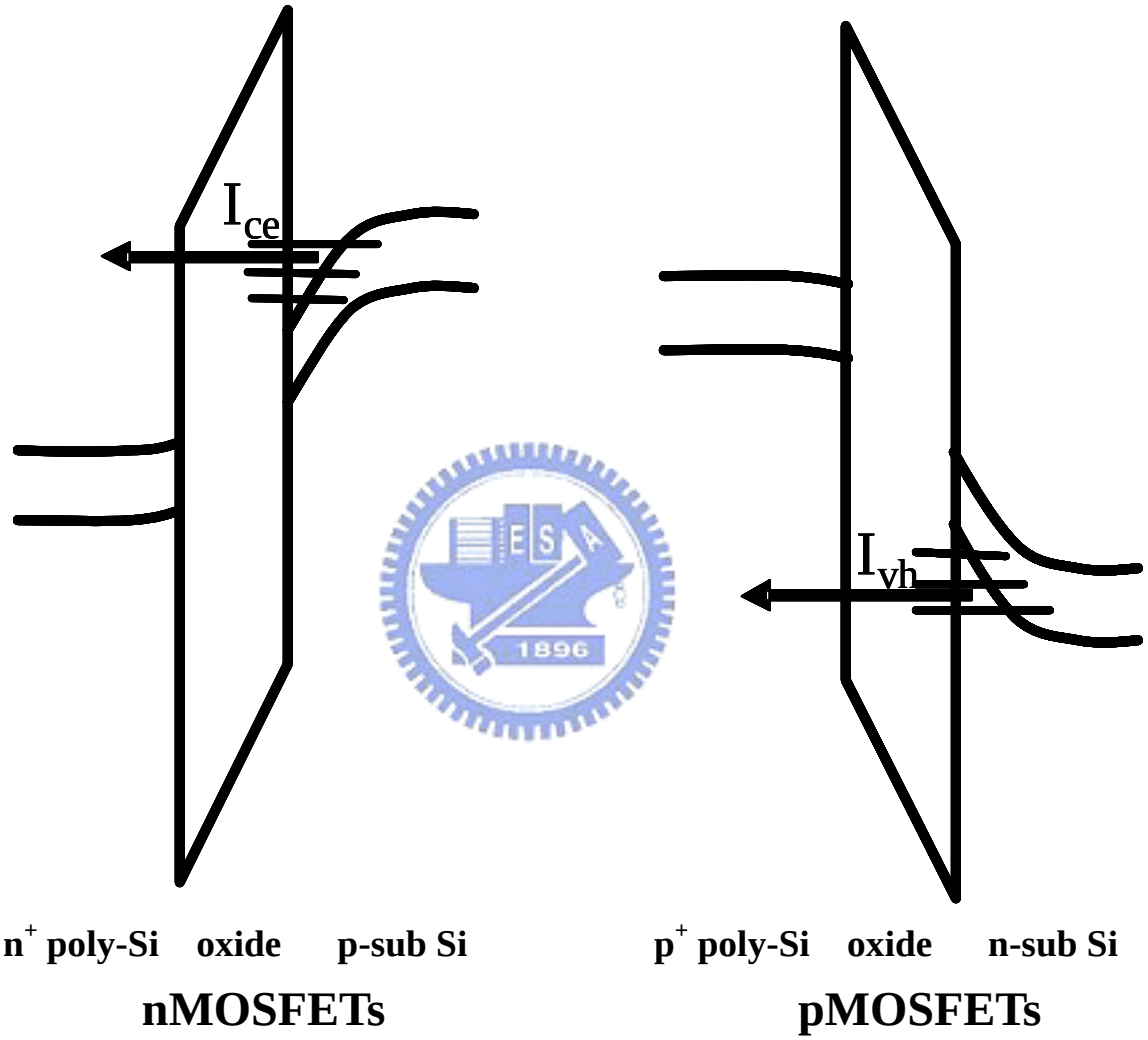

Fig.2.8 Illustration of source/drain tunneling current components in MOSFET's in strong inversion condition.

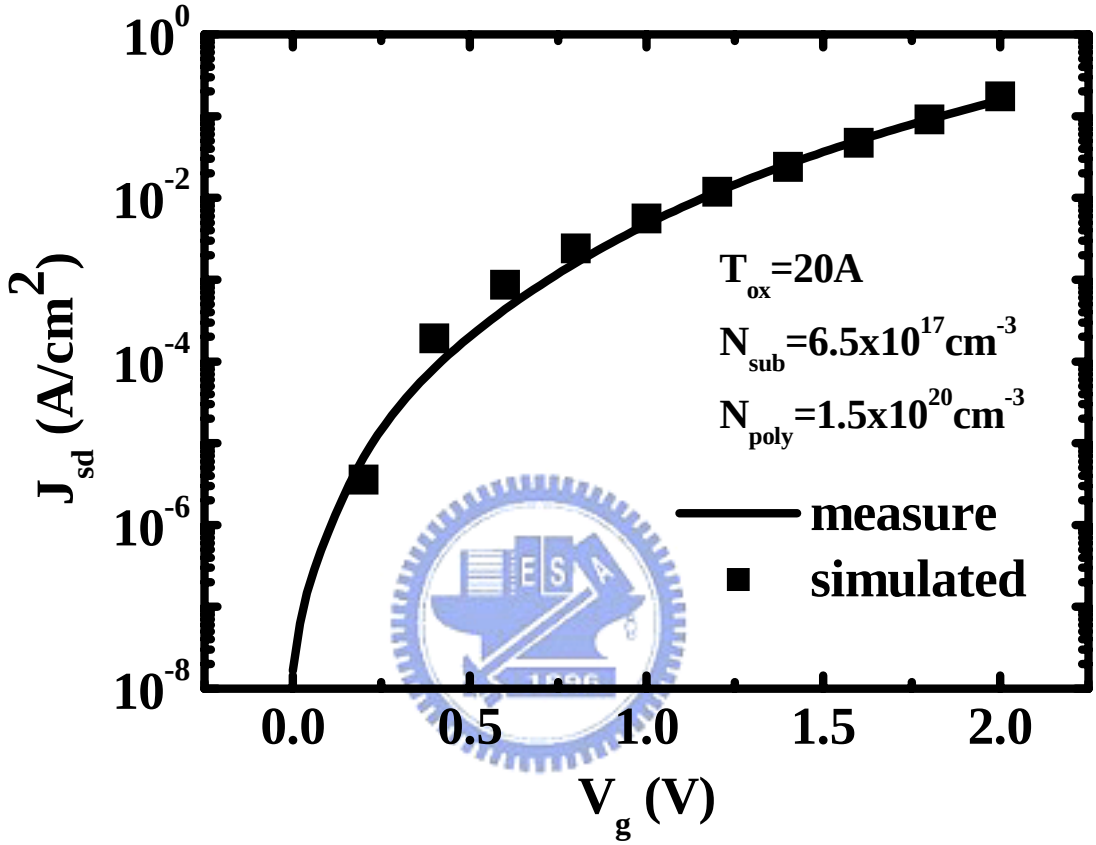

Fig.2.9 Measured and simulated I_{sd}-V_g curves of an n-MOSFET device.

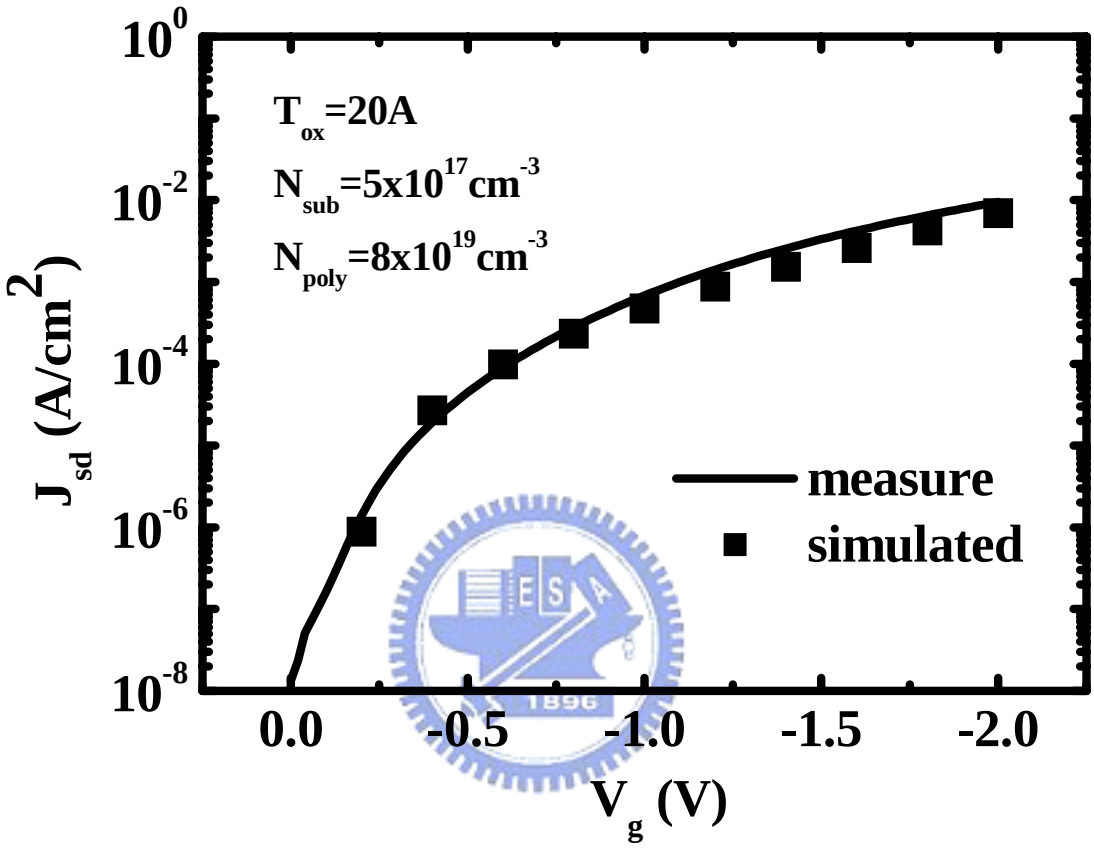

Fig.2.10 Measured and simulated I_{sd}-V_g curves of a p-MOSFET device.

2.4 Substrate Tunneling Current Modeling

In this section, the valance band tunneling current model will be derived. At a positive gate bias in an nMOSFET, the valence band tunneling current accounts for the substrate tunneling leakage current. At a negative gate bias in a pMOSFET, the valence band tunneling constitutes the substrate current. The simulated and measured results of the valence band tunneling in n- and p-MOSFETs will be compared and discussed.

2.4.1 Transport of Valence Band Electrons

The valance band tunneling model is similar to the conduction band tunneling model except that the valence band tunneling current is obtained from the integral of Eq (2-9) over the entire energy range in the valence band. This is because the energy state in the valence band can be considered as continuous states, as opposed to the sub-band structure for electrons in the conduction band. So the valance band electron tunneling current density from the substrate to the gate can be written as follows

$$j_{si\to poly} = qnv_x = q(((dk_x dk_y dk_z)/(2\pi)^3)\cdot 2\cdot f\cdot D\cdot(1-f'))v_x \qquad (2\text{-}21)$$

The valance band electron tunneling current density from the gate to the substrate is below

$$j_{poly\to si} = q/(4\pi^3\hbar)\int_0^\infty dE_x \int_{k_y}\int_{k_z} D' f'(1-f)dk_z dk_y \qquad (2\text{-}22)$$

E_X is measured from the valance band-edge of the substrate. Similarly, the net tunneling current has the following form

$$j = q/(4\pi^3\hbar)\int_0^\infty dE_x \int_{k_y}\int_{k_z} D'(f - f')dk_z dk_y \tag{2-23}$$

Substituting Eq (2-15) into Eq (2-23), the net valance band electron tunneling current density can be written as

$$j = q/(4\pi^3\hbar)\int_0^\infty dE_x \int_0^{E_x} \frac{dE_{//} m_{//}^*}{\hbar^2} 2\pi D'(f - f') \tag{2-24}$$

So the valance band electron tunneling current density is

$$\begin{aligned} qm_{//}^*(1/(2\pi^2\hbar^3))\int_0^\infty dE_x \int_0^{E_x} dE_{//} D(E_{//})\{1/(1+\exp((E_x - E_f)/(k_B T))) \\ -1/(1+\exp((E_x - E_{f'})/(k_B T)))\} \end{aligned} \tag{2-25}$$

the definition of the parameters in the above equations are the same as in previous sections.

2.4.2 Simulated and Measured Result

In Fig. 2.11, we know that in inversion region the valence band electrons tunnel from the substrate (gate) to the gate (substrate). The electrons flow out (into) the substrate for n-MOSFET (p-MOSFET). So, the number of electrons tunneling from the substrate into the gate in the valence band should be the same as the number of holes flowing to the substrate contact. Thus, the measured substrate current is composed of the valence band tunneling current in an nMOSFET. So, we can use Eq (2-25) to simulate the substrate tunneling current. In Fig. 2.12 and Fig. 2.13, it is found that the simulation results of I_b-V_g in inversion region can fit the measurement result well with the same set of device parameters in section 2.2.

2.5 Summary

In this chapter, a quantum-mechanical treatment of the accumulated and inverted silicon layers and the gate tunneling current in ultra-thin gate oxides are presented. The gate tunneling current is treated as the summation of the source/drain tunneling current and substrate tunneling current. Using the QM calculation and a modified WKB method, we have demonstrated that the source/drain current and the substrate current can be simulated well in ultra-thin gate oxides.

Specifically the model can be used to model the tunneling currents from the substrate inversion layer of an MOS device, especially for ultra thin oxides about 2.0 nm where accurate modeling at low bias levels is critical. The tunneling current at the low bias is particularly important since for future generation of MOS devices with ultra thin gate oxides, the off-state currents due to the gate tunneling currents become a dominant factor. Thus, the present model may provide a simple tool to access the effects of the low bias gate tunneling currents for MOSFETs in the off state condition. These tunneling current models will help us to understand the reliability concerns of ultra-thin oxide devices.

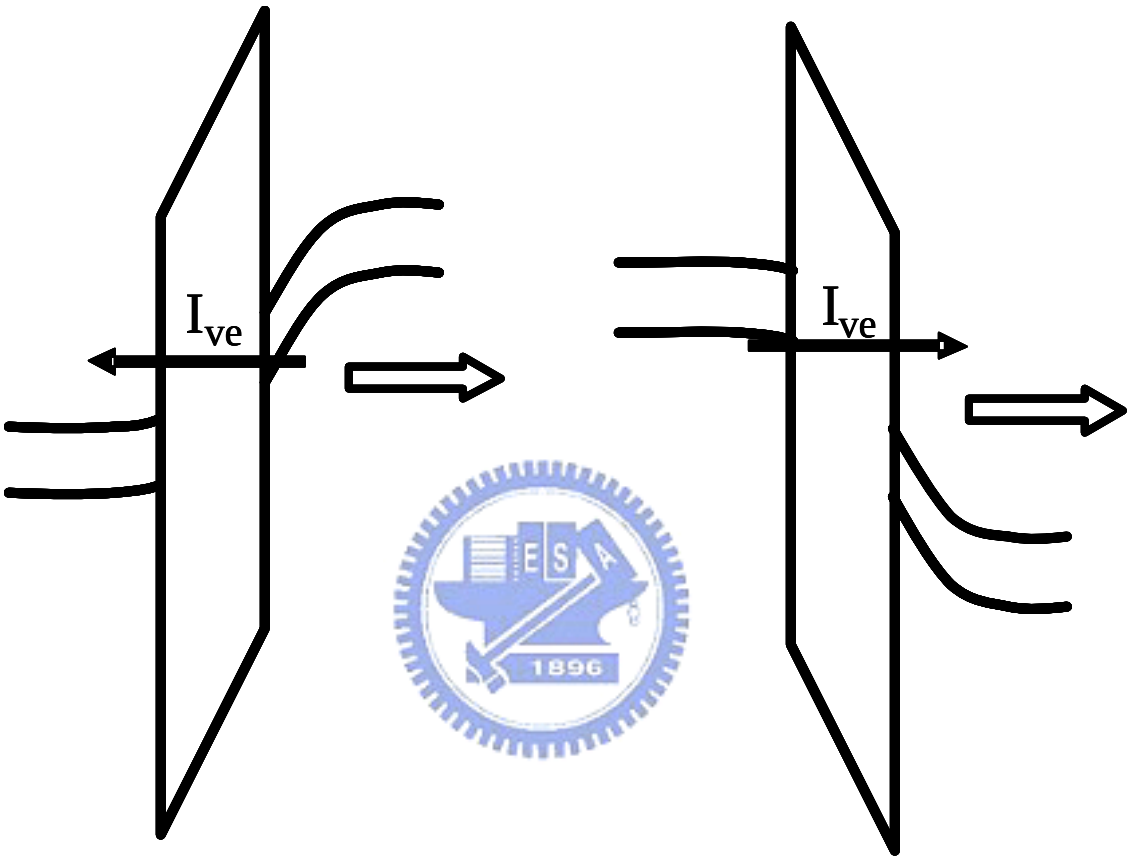

Fig.2.11 Illustration of substrate current transport in MOSFET's in strong inversion condition.

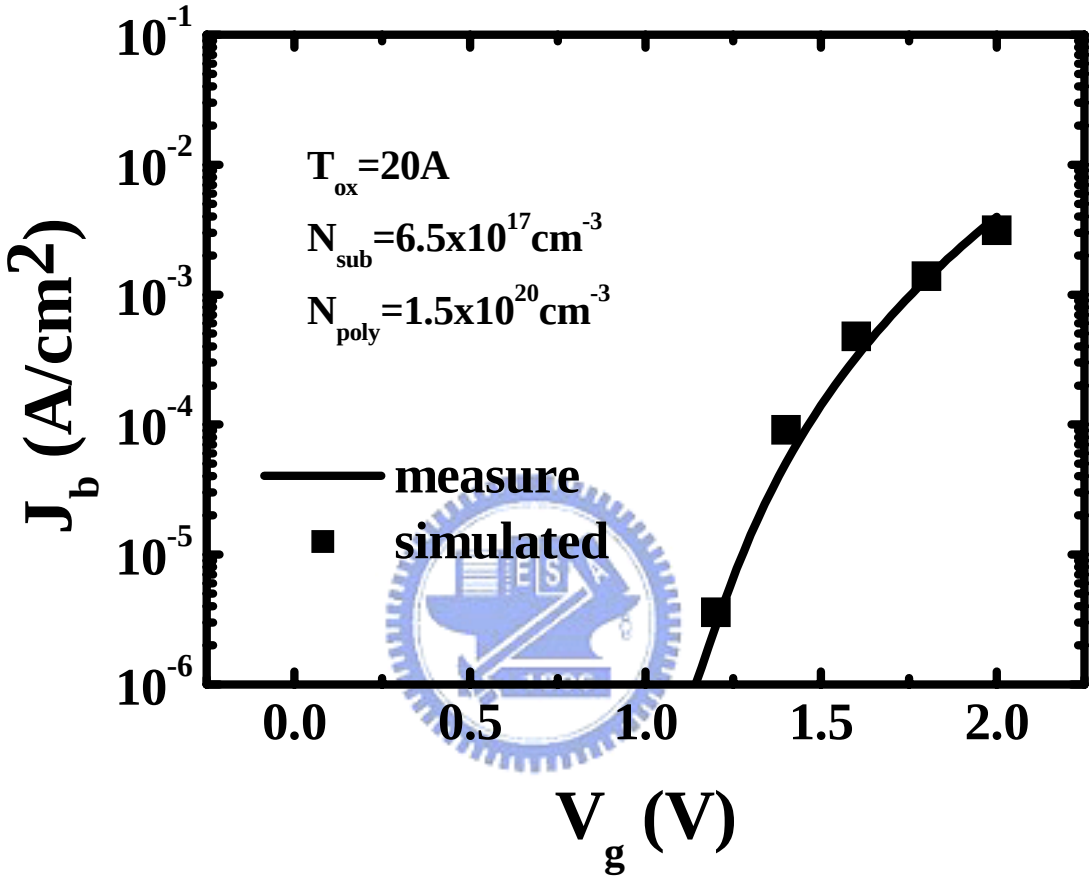

Fig.2.12 Measured and simulated I_b-V_g curves of an n-MOSFET device.

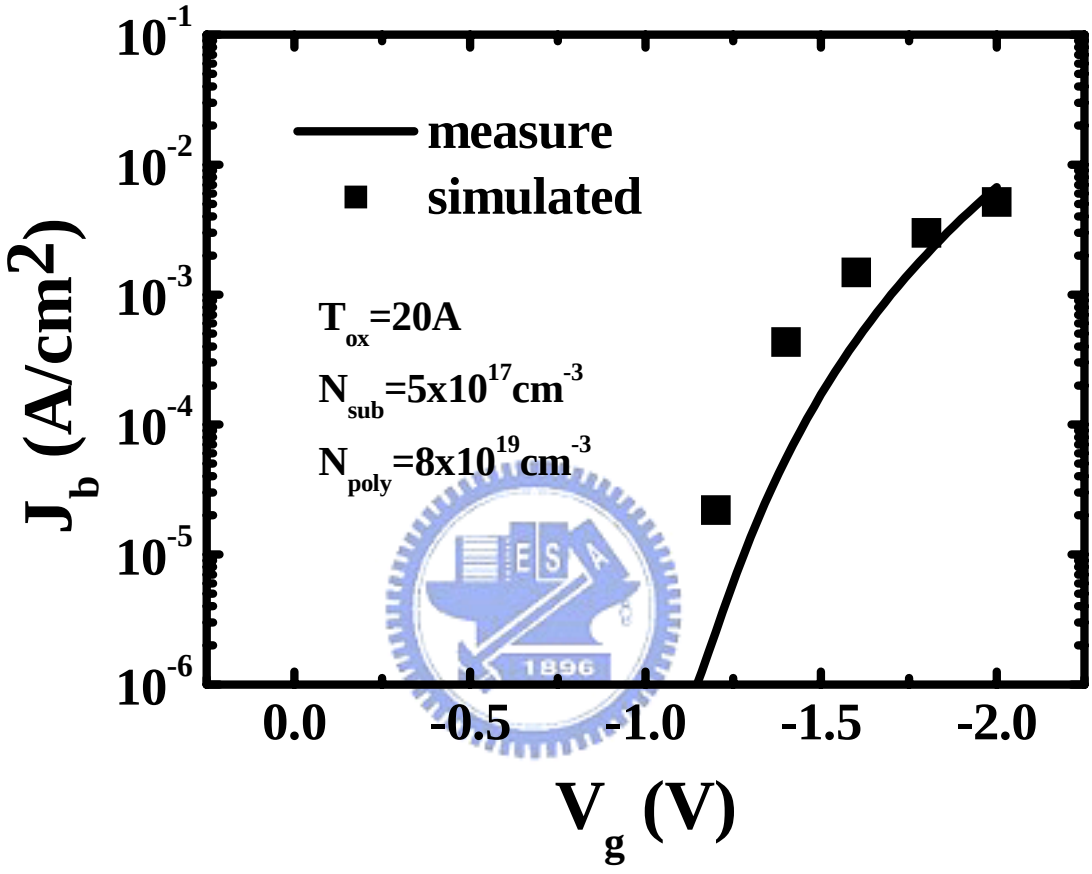

Fig.2.13 Measured and simulated I_b-V_g curves of a p-MOSFET device.

Chapter 3
Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI MOSFETs

3.1 Introduction

Silicon-on-insulator (SOI) technology has emerged as a promising technology for system-on-a-chip applications, which require high-performance complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs), low power, embedded memory, and bipolar devices. The primary feature of a MOSFET with SOI configuration is that the local substrate of the device is floating electrically, and thus the substrate-source bias (V_{BS}) is not fixed. As V_{BS} changes, the device threshold voltage (V_t) will change due to the body effect. This "instability" in V_t resulting from floating body configuration becomes one of the most challenging tasks in bringing SOI devices into mainstream applications.[3.1-3.4] One manifestation of the V_t variation is the hysteresis effect. The V_t hysteresis as a result of various floating body charging/discharging mechanisms has been widely investigated.[3.2-3.4] In this work, the influence of gate oxide breakdown position on hysteresis effects in ultra-thin oxide partially-depleted (PD) SOI MOSFETs will be explored.

Several causes of V_t hysteresis in PD SOI MOSFETs have been proposed.[3.5-3.8] Boudou et al [3.5] reported that V_t hysteresis could be caused by positive feedback of impact ionization due to long time constants associated with body potential charging. Chen et al [3.6] showed that at high drain biases the floating body effect can lead to hysteresis in the sub-threshold I_{ds}-V_{gs} characteristics even when the gate is biased well below its threshold voltage. Fung et al [3.7] found that in ultra thin gate oxide devices the gate-to-body tunneling current modulates the body voltage and induces a hysteresis effect. All the above works investigate the hysteresis phenomenon in PD SOI MOSFETs without considering gate oxide

soft breakdown (SBD). Recent studies [3.9-3.13] showed that in bulk CMOS the impact of gate oxide SBD is only manifested in a noticeable increase in gate leakage current without degrading other device characteristics in operation. Crupi et al [3.14] showed that at high gate voltages the substrate current steeply increases after SBD due to localized effective thinning of gate oxide. Chan et al [3.15] presented that in thinner oxides the post-SBD gate induced drain leakage (GIDL) current increases significantly because of the enhancement of band-to-band tunneling. Although the dependence of these excess substrate currents on the location of a SBD spot was widely explored, the influence of SBD location on V_t hysteresis in SOI devices has been rarely investigated.

3.2 Device Structure and Characterization

The devices in this work were made with a 0.13μm standard CMOS process on p-type PD SOI substrate. The gate oxide was grown with rapid plasma nitridation (RPN) process. The gate length is 0.13μm, the gate width is 10μm and the oxide thickness is 1.6nm. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this chapter, all devices were stressed at high constant gate voltage with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10μA. After breakdown, the device on-state characteristics were checked and no difference was observed.

The breakdown position was examined by using the method proposed by Degraeve et al.[3.16] Table 3.1 shows the ratio of I_d to (I_s+I_d) before and after SBD in four SOI devices. The measurement is in accumulation region and $|V_g|$=1.5V and $V_d=V_s$=0V. A significant increase of $I_d/(I_s+I_d)$ in device B and device D indicates that breakdown is located at the drain edge, while in device A and device C the moderate change in $I_d/(I_s+I_d)$ implies that the SBD position is in the channel. Aside from $I_d/(I_s+I_d)$, $I_b/(I_s+I_d)$ was measured (also shown in Table

3.1). In the channel SBD (c-SBD) devices, the valence band tunneling leakage in the channel region (I_b) was enhanced, resulting in a larger $I_b/(I_s+I_d)$. In the case of edge SBD (e-SBD), the breakdown was above the drain edge. As a result, the tunneling leakage current in the channel region remains almost the same as in pre-SBD, and the increased edge leakage current makes I_s+I_d larger and thus a smaller $I_b/(I_s+I_d)$. In short, the results in Table 3.1 shows that we can use the change of $I_d/(I_s+I_d)$ or $I_b/(I_s+I_d)$ to determine the breakdown location in the channel or in the drain edge region.

By utilizing the above technique, the device electrical behaviors in c-SBD and e-SBD devices were characterized. In Fig. 3.1, the gate current and the substrate current as a function of V_g in a fresh, a c-SBD, and an e-SBD nMOSFET were compared. The result shows that the substrate current increases drastically after c-SBD, but has little change after e-SBD. The substrate current at a positive gate bias is attributed to valence electron tunneling from the channel to the gate. The generated holes left behind in the channel then flow to the substrate. This tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band-gap of the n^+ poly-gate. Thus, I_b is enhanced significantly at a positive gate bias in a c-SBD device due to localized effective oxide thinning [3.14, 3.17-3.18] while I_b in an e-SBD device is nearly unchanged. Fig. 3.2 shows the drain bias dependence of the GIDL current before and after SBD. The substrate current has an apparent increase after edge SBD. This is because at a high drain bias the I_b comes from electron band-to-band tunneling in the drain depletion region and the generated holes flow to the substrate. Since the electrical field in the drain region becomes stronger after e-SBD due to effectively oxide thinning, the GIDL (I_b) in an e-SBD device is enhanced. The same phenomena in p-MOSFETs are also observed and the result is shown in Fig. 3.3.

acc. region	nMOSFET		pMOSFET	
	device A (c-SBD)	device B (e-SBD)	device C (c-SBD)	device D (e-SBD)
I_d/I_s+I_d before SBD	0.5078	0.5297	0.5174	0.5251
I_d/I_s+I_d after SBD	**0.4482**	**0.9957**	**0.1368**	**0.9387**
I_b/I_s+I_d before SBD	0.0287	0.0178	0.3202	0.1163
I_b/I_s+I_d after SBD	**0.1426**	**0.0001**	**10.8680**	**0.0102**

Table 3.1 The ratio of $I_d/(I_s+I_d)$ and $I_b/(I_s+I_d)$ before and after soft breakdown in four SOI MOSFETs. The measurement is in the accumulation region and V_g= |1.5V|, $V_d=V_s$=0V.

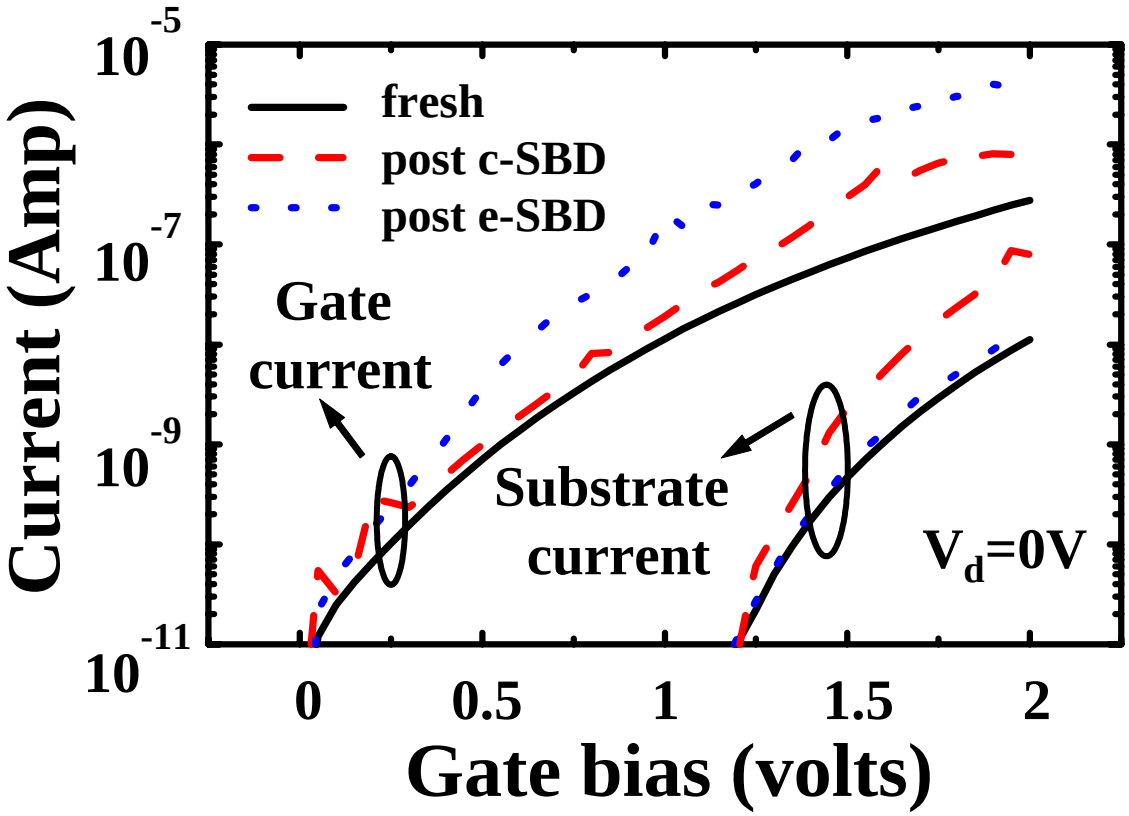

Fig.3.1 Gate current and substrate current versus gate bias in nMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

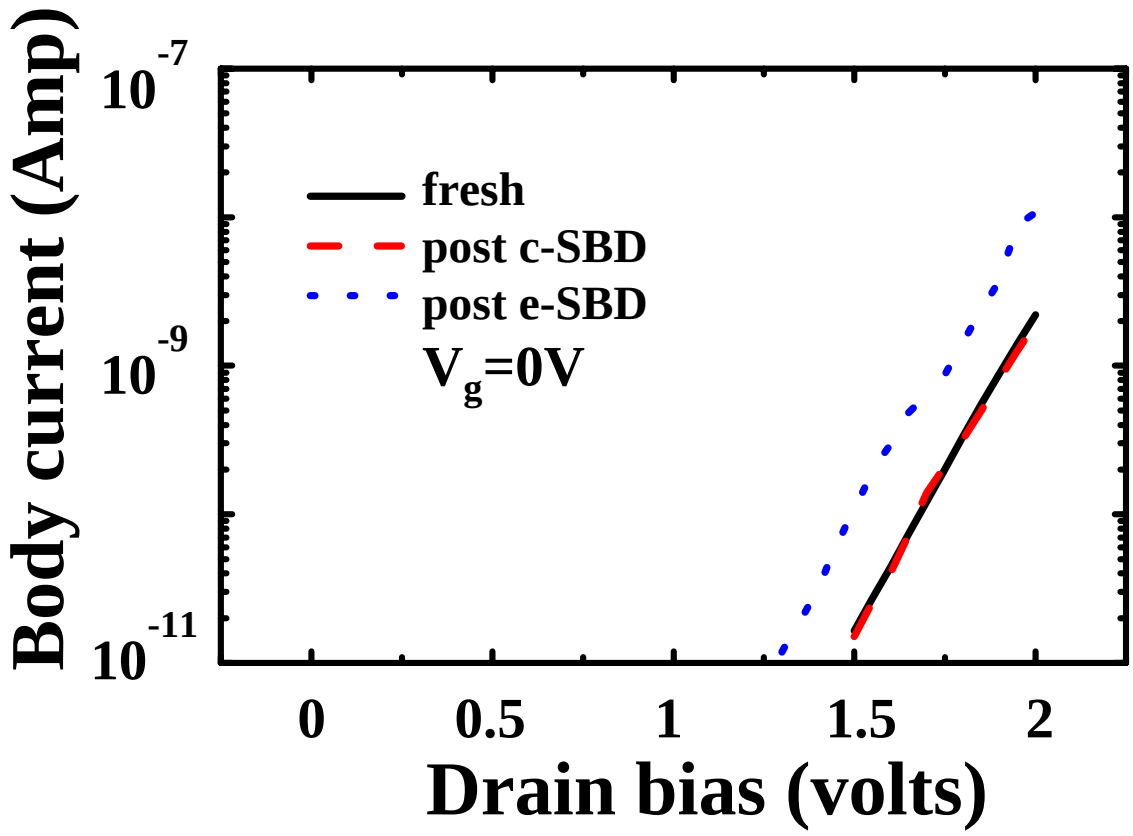

Fig.3.2 Body current versus drain bias in nMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

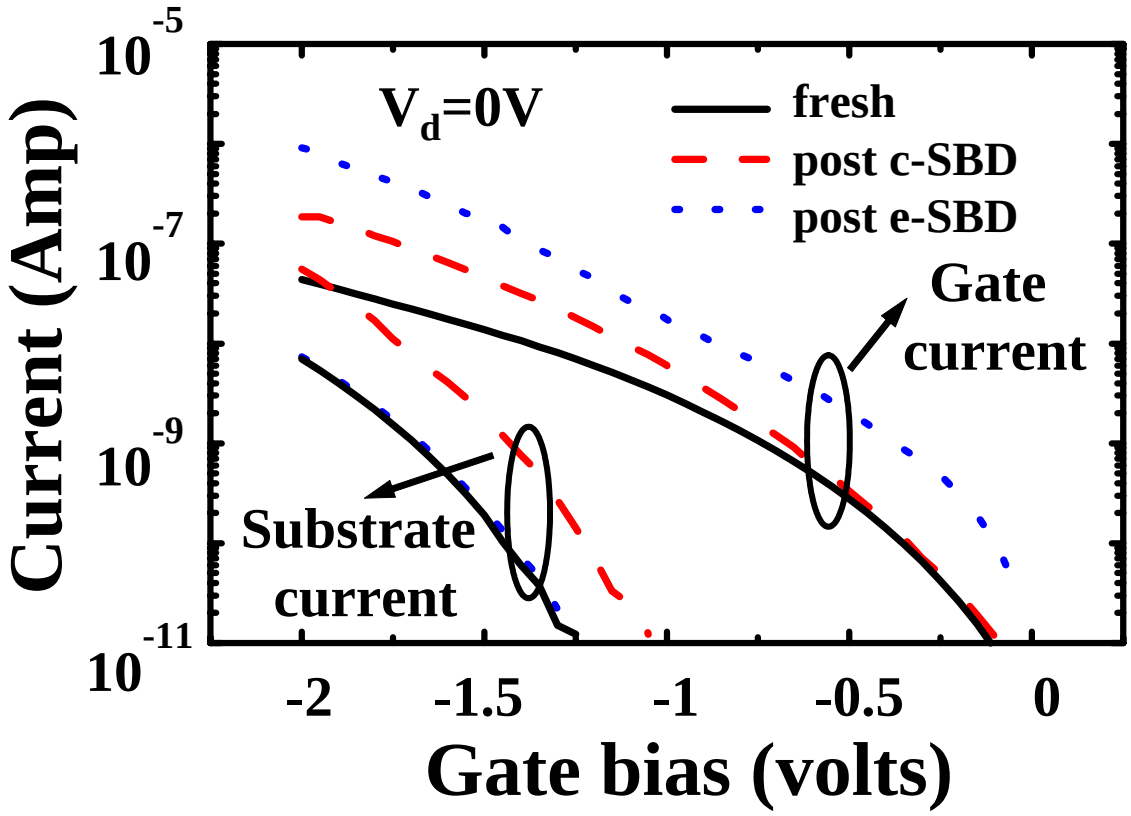

Fig.3.3 Gate current and substrate current versus gate bias in pMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

3.3 Modes of SBD Enhanced Hysteresis

Two modes of SBD enhanced body potential alteration are proposed. Fig. 3.4 illustrates two floating-body charging processes in c-SBD and in e-SBD SOI nMOSFETs.[3.19-3.20] In a c-SBD device with a positive gate bias (Fig. 3.4(a)), valence band electron tunneling from the channel to the gate is increased after SBD. The generated holes flow to the body and raise the body potential. Fig. 3.4(b) shows the drain-induced floating-body charging in an e-SBD nMOSFET. Since the breakdown path is in the drain edge, the GIDL current increases due to a stronger band bending in the n^+ drain region, thus raising the body potential at a high drain bias. On the contrary, the GIDL current does not change in a c-SBD device. Likewise, Fig. 3.5 shows two possible floating-body charging processes in pMOSFETs. Due to the above two charging processes, we conclude that the body potential of both nMOSFET and pMOSFET can be modified either during gate switching or during drain switching depending on the location of a SBD spot.

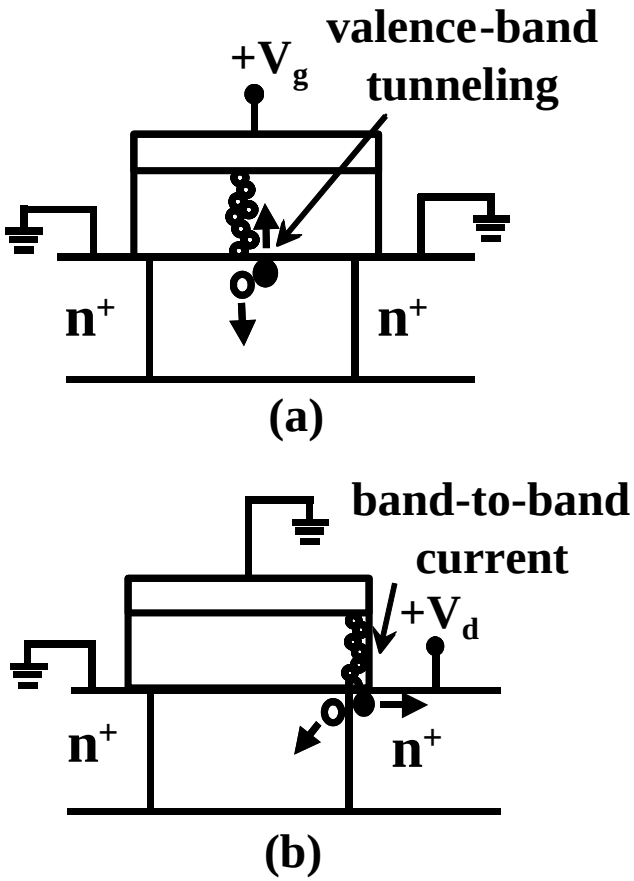

Fig.3.4 Illustration of two soft-breakdown enhanced floating-body charging processes in SOI nMOSFETs. (a) soft breakdown in the channel region and hole creation due to valence band electron tunneling; (b) soft breakdown in the drain region and enhanced GIDL current.

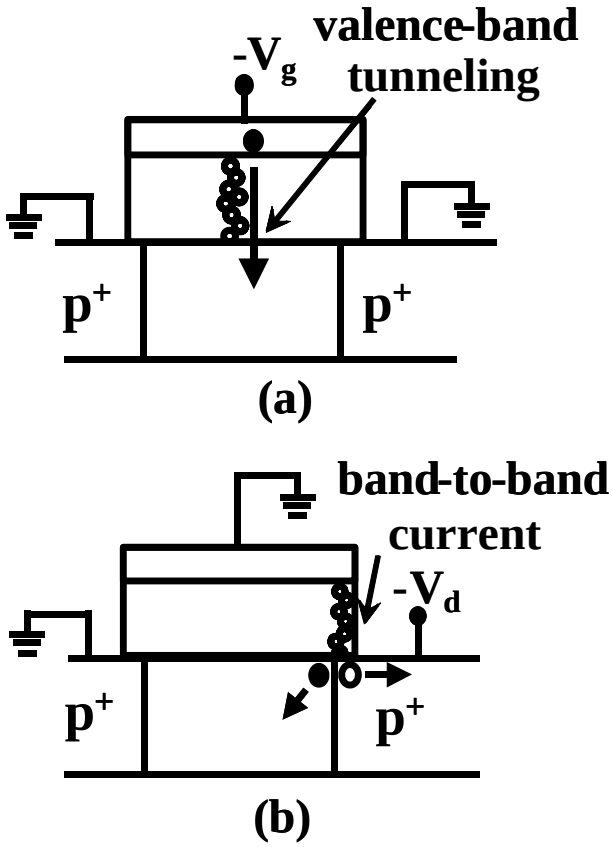

Fig.3.5 Illustration of two soft-breakdown enhanced floating-body charging processes in SOI pMOSFETs. (a) soft breakdown in the channel region and valence band electron tunneling from poly-gate to the floating body; (b) soft breakdown in the drain region and enhanced GIDL current.

3.4 Results and Discussion

Fig. 3.6 shows the I_{ds}-V_{gs} hysteresis in a PD SOI nMOSFET before and after c-SBD. The measurement drain bias is 0.1V. The gate bias is swept from 0V to 1.3V and then is reversely swept from 1.3 to 0V. Note that (i) the sub-threshold hysteresis before SBD is insignificant and (ii) the post-SBD hysteresis is induced by gate bias sweep in this device. The corresponding body potential fluctuation in gate bias sweep is shown in Fig. 3.6. The arrow in the figure indicates the direction of bias sweep. After c-SBD, the body potential begins to rise when the V_g amplitude is above 0.8V. The gate switching induced body potential variation can be as large as 0.3V in this case. The pre-SBD body potential hysteresis at the same switching amplitude is less than a few tens of milli-volts. The c-SBD induced V_t hysteresis is also observed in a pMOSFET. The measurement data are not shown here.

In an e-SBD device, although gate enhanced hysteresis is not observed, drain sweep induced hysteresis in sub-threshold leakage current is remarkable (Fig. 3.7). In this figure, the measurement V_{gs} is 0V and the drain bias is swept from 0V to 1.3V and then reversely swept back. The body potential variation is shown in Fig. 3.7, too. The e-SBD enhanced hysteresis effect is clearly shown in this figure. It should be noted these breakdown-induced hysteresis effects occurs in off-state rather than in on-state where hot carrier impact ionization has been reported as a responsible charging mechanism.[3.5]

The relationship between the magnitude of sweep voltage and the body potential hysteresis in the two SBD modes is investigated. In nMOSFETs, the degree of hysteresis in terms of the body potential variation versus the amplitude of the sweep voltage is shown in Fig. 3.8 for gate bias sweep and in Fig. 3.9 for drain bias sweep. The hysteresis voltage is defined as the maximum substrate charging voltage during the sweep. In gate bias sweep (Fig. 3.8), the c-SBD device shows an increased hysteresis voltage while the hysteresis voltage of the e-SBD device is almost unchanged. In contrast, the e-SBD device shows a larger hysteresis voltage in drain bias sweep (Fig. 3.9). Similar results in pMOSFETs are presented

in Fig. 3.10 for gate bias sweep and in Fig. 3.11 for drain bias sweep. From our characterization, we found SBD induced hysteresis effect may become appreciable even when the supply voltage is below 0.8V.

The impact of SBD enhanced body charging effect in CMOS operation is described as follows. Fig. 3.12 illustrates the dominant V_t hysteresis modes in a SOI CMOS inverter. Hot carrier (HC) induced floating body charging occurs in on state [3.1,3.5] and it is dominant only when the inverter is during switching. On the other hand, floating body charging takes place in c-SBD (e-SBD) nMOSFETs and e-SBD (c-SBD) pMOSFETs when the input signal is at high (low) state. Since the soft breakdown induced body charging is in the off state, the time for charging can be much longer than the on-state HC caused body charging. Our study reveals that SBD in PD SOI MOSFETs not only increases leakage current but also affects circuit stability.

3.5 Summary

The significance of soft breakdown position to V_t hysteresis in PD SOI CMOS devices has been evaluated. Two SBD enhanced hysteresis modes in off-state CMOS are identified. The dominant floating body charging mechanism is valence band tunneling in c-SBD devices and band-to-band tunneling in e-SBD devices. The SBD enhanced hysteresis effect may occur even with supply voltage less than 1.0V and would be a serious reliability concern in ultra-thin oxide PD SOI circuits.

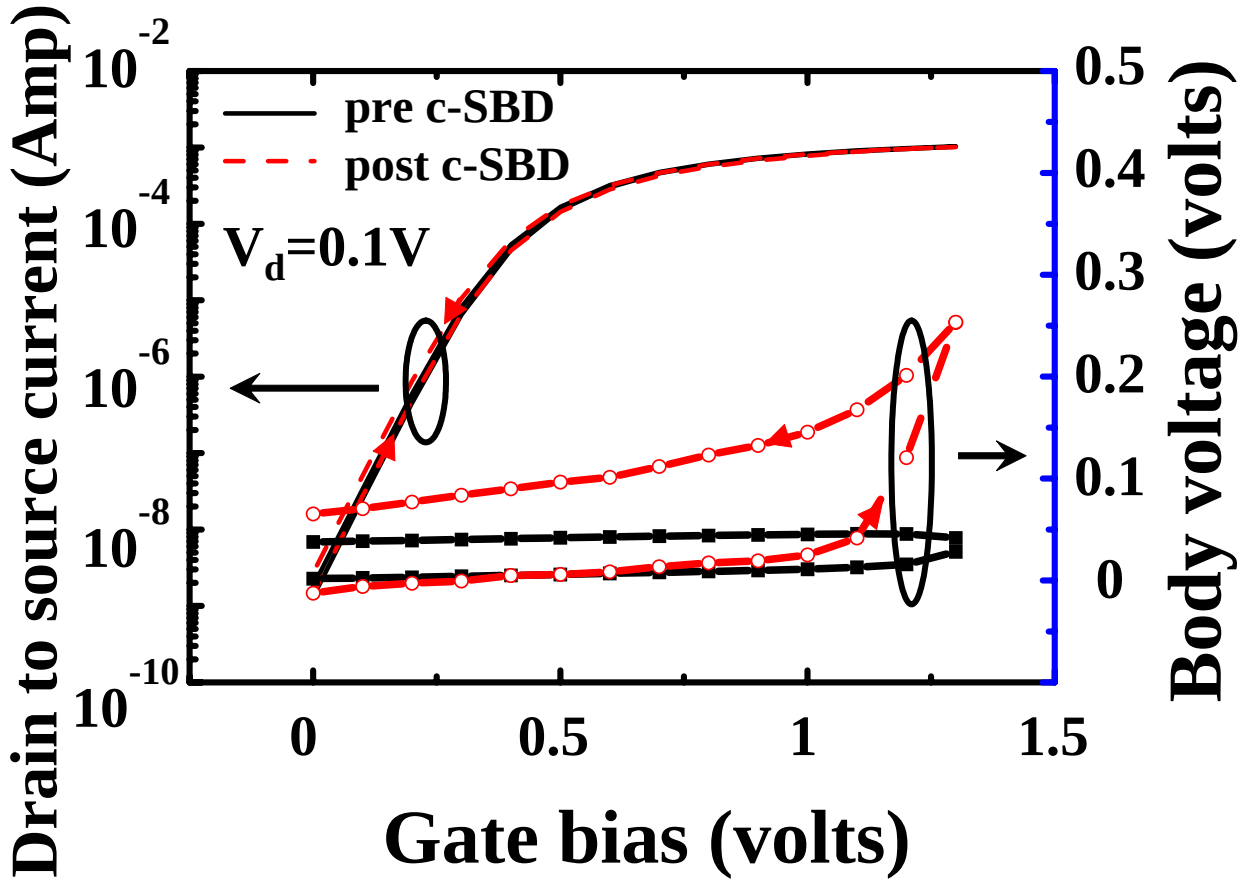

Fig.3.6 Hysteresis in I_{ds} and corresponding floating-body potential versus V_g in a c-SBD SOI nMOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0V to 1.3V.

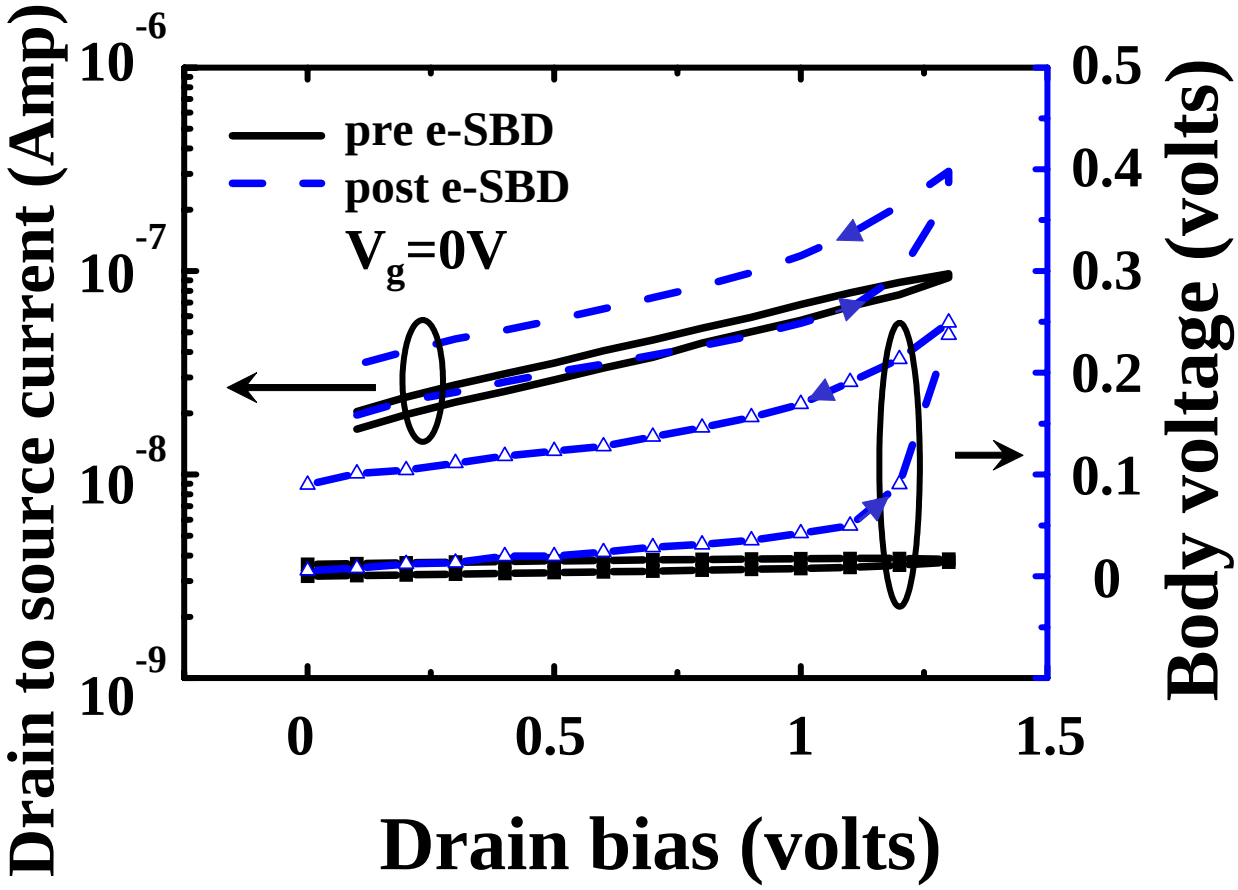

Fig.3.7 Hysteresis in sub-threshold current and corresponding floating-body potential in an e-SBD SOI nMOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0V to 1.3V.

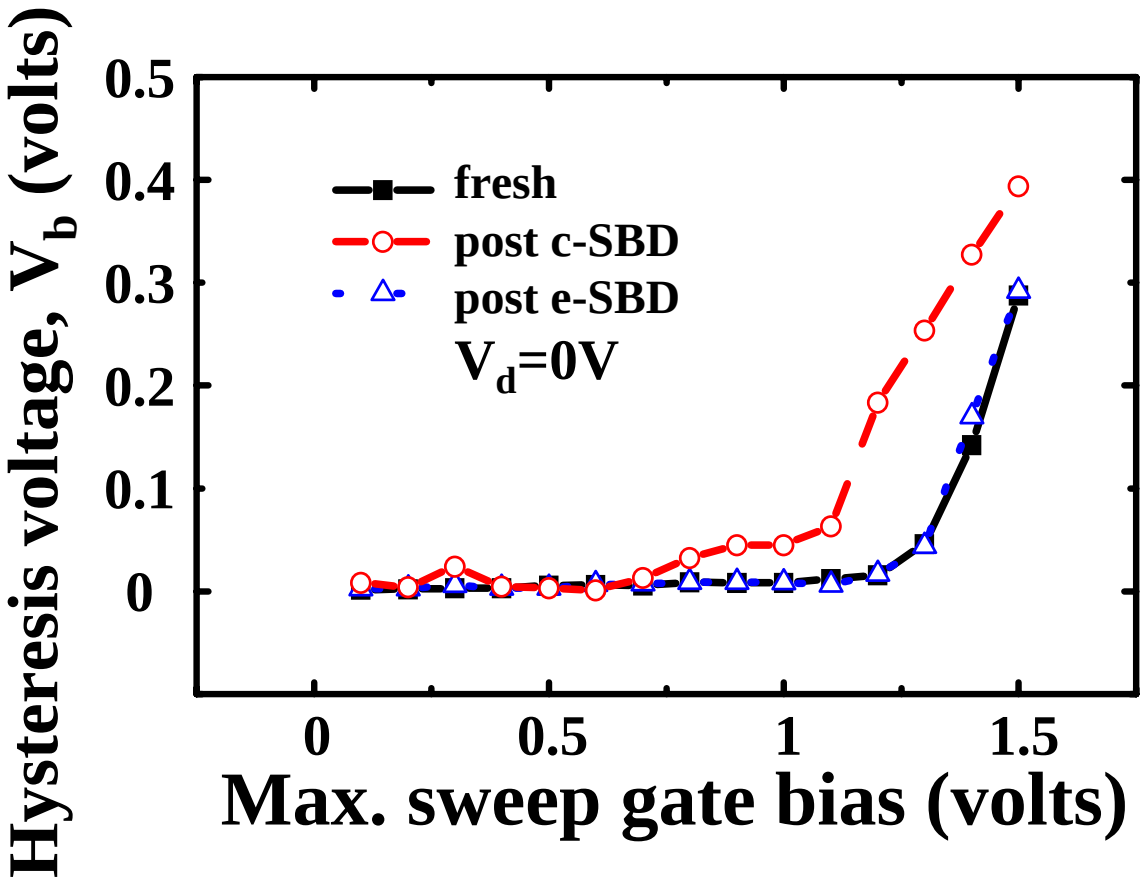

Fig.3.8 The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI nMOSFETs. V_d=0V.

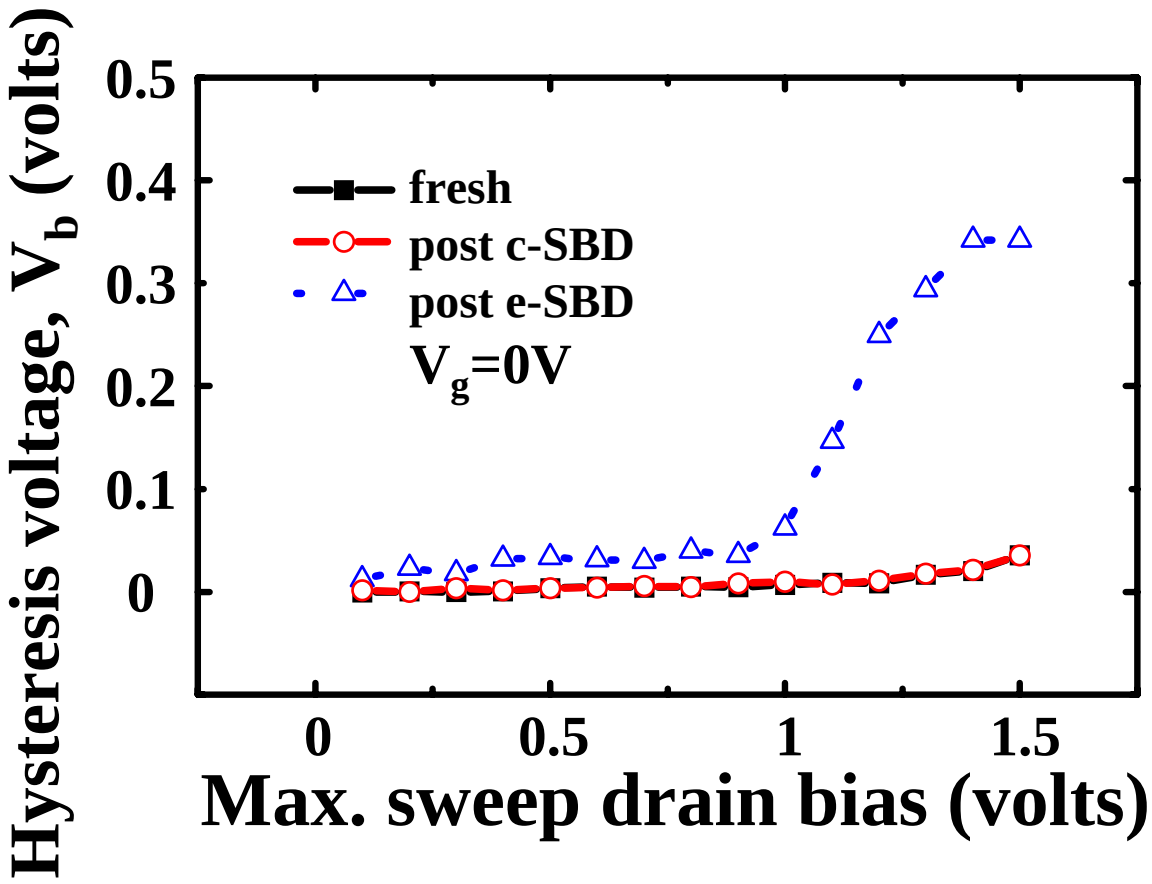

Fig.3.9 The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI nMOSFETs. V_g=0V.

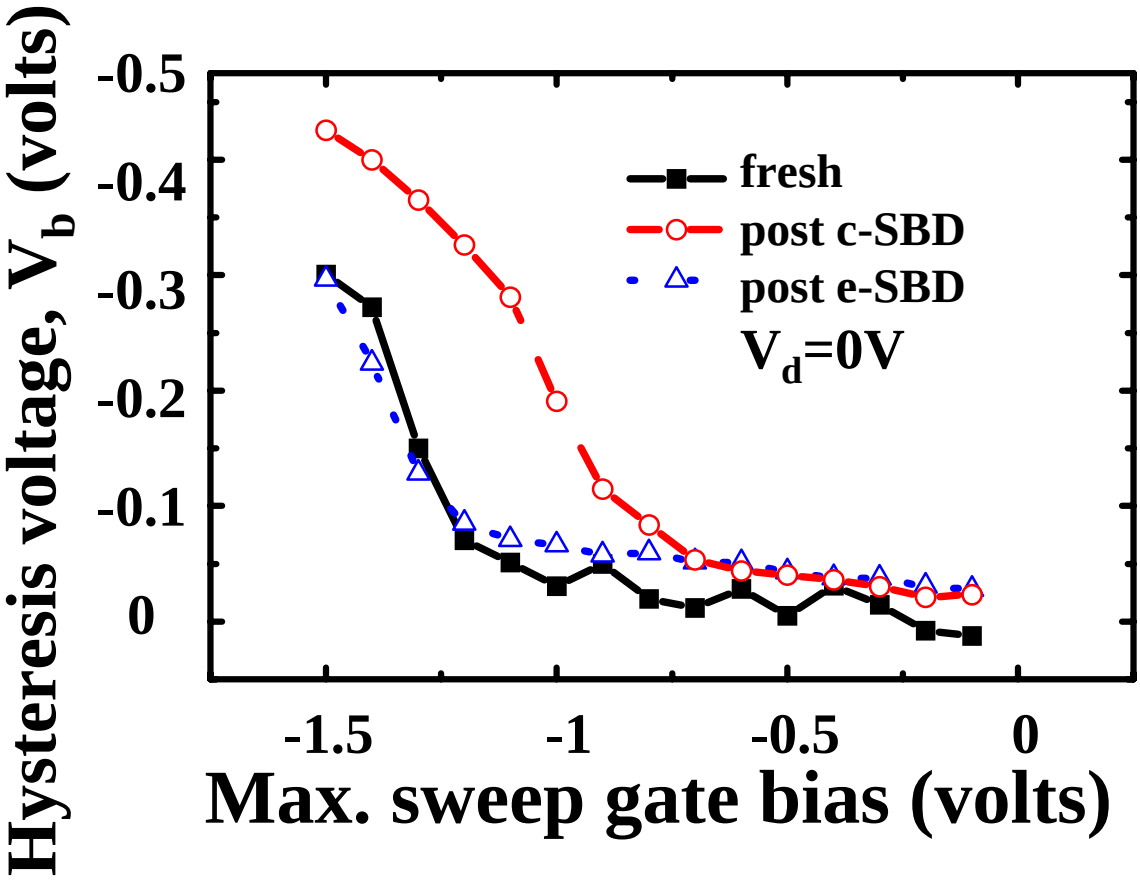

Fig.3.10 The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI pMOSFETs. V_d=0V.

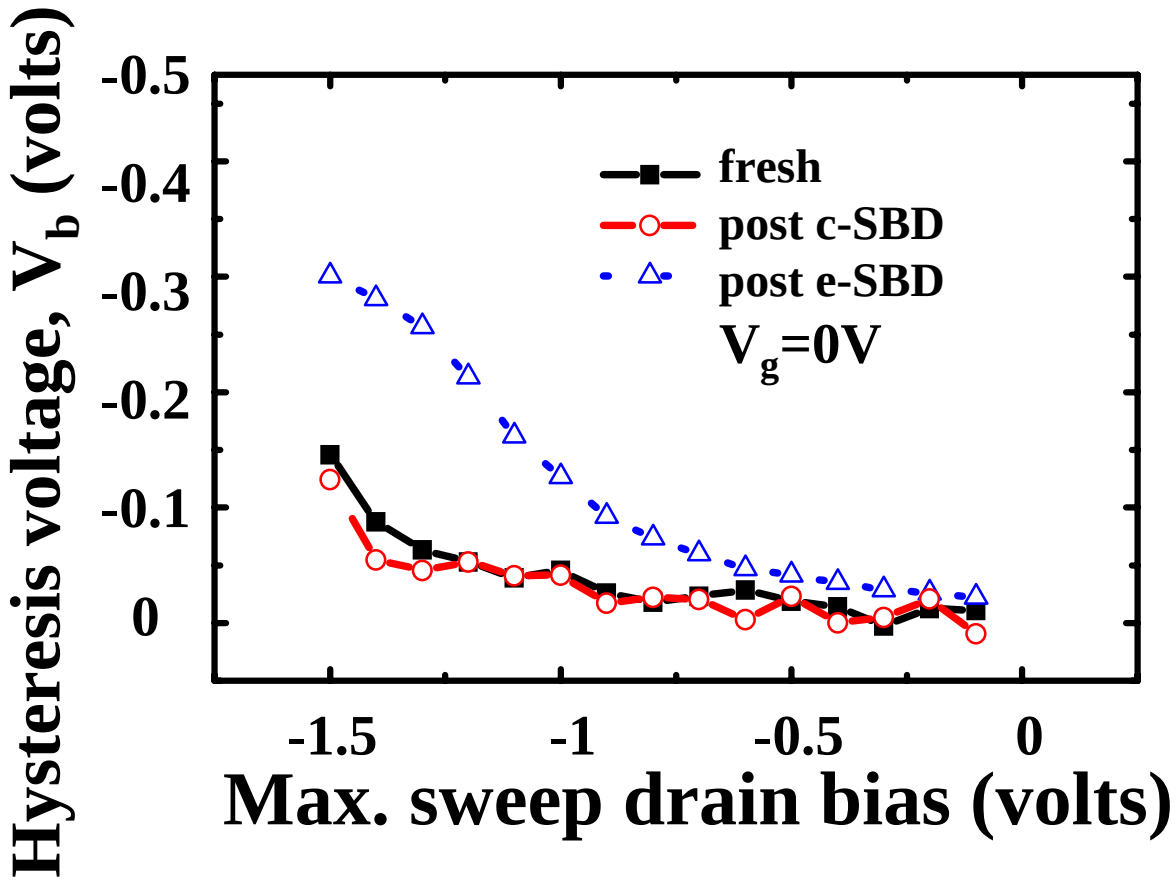

Fig.3.11 The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI pMOSFETs. V_g=0V.

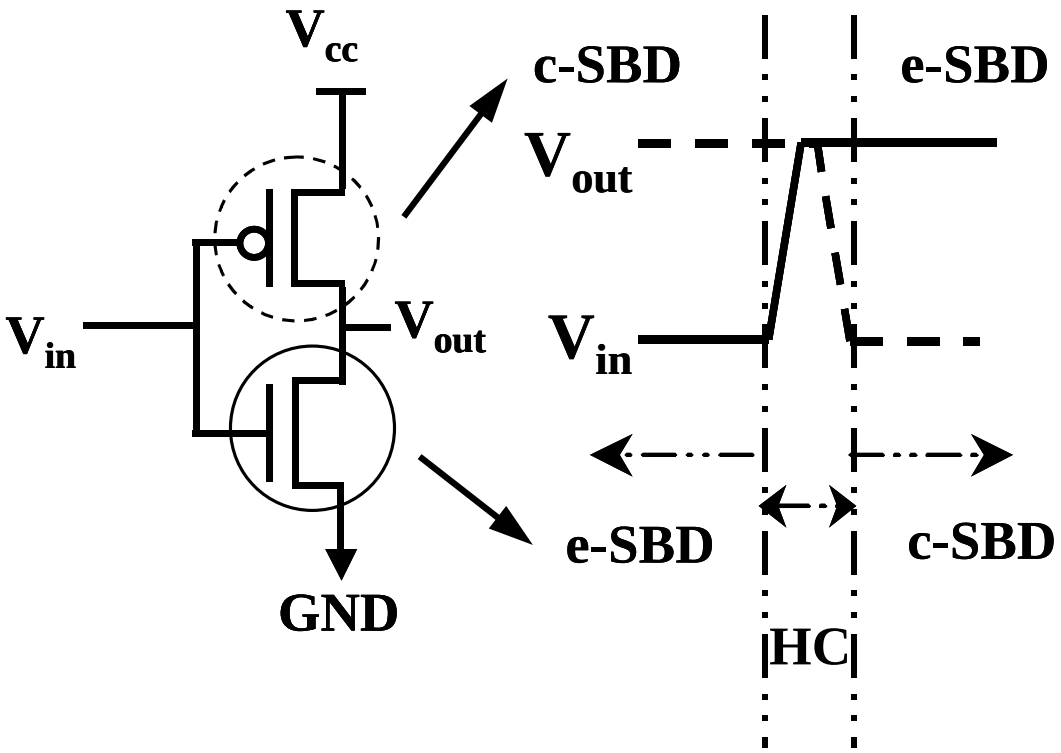

Fig.3.12 Illustration of dominant V_t hysteresis modes in the switching of an SOI CMOS inverter.

Chapter 4
Soft Breakdown Enhanced Excess Low-Frequency Noise in Ultra-Thin Oxide SOI n-MOSFETs

4.1 Introduction

Silicon-on-insulator (SOI) technology also has regarded as a hopeful technology for system-on-a-chip applications, which require high-performance, low power, fully integrated RF, and mixed-signal circuits.[4.1-4.5] However, the troublesome floating-body effect (FBE) in PD SOI MOSFETs leads to kink in drain current characteristics as well as some undesirable transient effects.[4.1-4.4] FBE also gives rise to excess low-frequency noise with a Lorentzian-like spectrum in floating body PD SOI devices, posing a serious problem for base band signal processing system.[4.6-4.9] The observed Lorentzian shaped noise is caused by white thermal noise (Nyquist or shot) sources associated with the generation and removal of body charge.[4.6] The Lorentzian signature is obtained through the trans-impedances coupling these internal white noise sources to the terminals of the SOI device.[4.7] Several causes of the Lorentzian-like spectrum in SOI MOSFETs have been proposed. The origin of these floating body noises could be related to high drain bias induced impact ionization current and large gate bias induced valance band electron tunneling through the ultra-thin gate oxide.[4.9-4.10] Chapter 3 has pointed out that soft breakdown enhanced substrate tunneling current would induce threshold voltage (V_t) hysteresis effects in PD SOI MOSFETS.[4.11] The aim of this chapter is to describe the impact of soft breakdown location on the excess low-frequency noise for SOI devices with floating body configuration.

In the beginning, the excess noise model in PD SOI MOSFETs is introduced. Then, the kink effect in ultra-thin oxide floating body SOI n-MOSFETs is studied, which would induce excess low frequency noise. After that**,** the impact of soft breakdown location on drain current noise in ultra-thin oxide SOI n-MOSFETs is investigated. In a channel breakdown device, a

noise overshoot phenomenon is observed in the ohmic regime. It is characterized by a peak in current noise spectral density versus the operation gate voltage, whereby the peak amplitude can be about one order of magnitude higher than the background flicker noise. The origin of this excess noise is believed due to soft breakdown (SBD) enhanced valance-band electron tunneling and thus induced floating body effect. The findings indicate that channel SBD enhanced drain current noise can be a reliability issue in PD analog SOI CMOS circuit.

4.2 Excess Low-Frequency Noise Model in SOI MOSFETs

The major noise sources of an SOI MOSFETs operating in strong inversion are shown in Fig. 4.1. There are two noise sources associated with the conducting channel. One is flicker (1/f) noise which contributes to the low-frequency noise, the other is thermal noise which dominates at high frequency. In addition to the noise in the channel, there are two shot noise sources associated with the floating-body, which are due to the impact ionization current and the body-source diode current, respectively. In bulk MOSFET, only 1/f noise can be observed at low-frequency. However, excess noise is found in floating-body PD SOI MOSFET. The excess noise originates in the two shot noises. Although the shot noises are small in magnitude compared with flicker noise, they are amplified by FBE and give rise to the excess low-frequency noise in PD SOI MOSFET. The low-frequency noise in floating-body PD SOI MOSFET's includes white noise, flicker noise and the FBE-induced excess noise.

A. White Noise

The white noise component originates from thermal random motion of carriers in the channel.

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B. Flicker Noise

Flicker noise is a fluctuation in conductance with a power spectral density proportional to

$1/f^{\beta}$, where β is close to unity so that flicker is normally called 1/f noise. There is no consensus to the origin of the 1/f noise, it is very likely that there exist more than one mechanism giving rise to the same noise characteristics. According to McWhorter's number fluctuation theory [4.12], 1/f noise is attributed to the trapping and de-trapping processes of the charges in the oxide traps close to the Si–SiO_2 interface. Hooge's empirical model [4.13], however, considers the 1/f noise as a result of carrier mobility fluctuation due to lattice scattering. It has been reported that both the carrier number fluctuation and the mobility fluctuation are possible mechanisms which lead to the 1/f noise in MOSFET's [4.14-4.15]. Hence, for the 1/f noise, a correlated noise model [4.14] which incorporates both mechanisms is applied

$$S_{id-1/f} = \frac{kTqI_{ds}\mu_{eff}}{\gamma f L_{eff}^{\ 2}} \int_0^{V_{ds}} \frac{N_t(E_f)}{N} (1+\alpha\mu_{eff} N)^2 \, dV \tag{4.1}$$

where

$S_{id-1/f}$	1/f noise current spectral density;
I_{ds}	drain current;
μ_{eff}	effective mobility;
γ	attenuation coefficient of the electron wave function in the oxide;
L_{eff}	effective channel length of the device;
V_{ds}	drain bias;
$N_t(E_f)$	oxide trap concentration around the quasi-Fermi level along the channel;
N	carrier concentration along the channel;
α	lattice scattering coefficient.

C. Excess Low Frequency Noise

The excess low-frequency noise is specific to PD SOI MOSFET's associated with the floating-body effect (FBE). The noise small-signal equivalent circuit shown in Fig. 4.2(a) can explain the mechanism underlying the excess low-frequency noise [4.6]. The shot noise results from the impact ionization current (I_{ii}):

$$S_{ib1} = M \cdot 2qI_{ii} \tag{4.2}$$

where **M** is a multiplication factor [4.16]. Impact ionization current exhibits shot noise because only the carriers with sufficient kinetic energy can generate electron-hole pairs. The second noise source is associated with the body-source diode current ($\mathbf{I_{bs}}$) where carriers have to overcome the built-in potential barrier:

$$S_{ib2} = 2qI_{bs} \tag{4.3}$$

The two noise current flow through the body-ground impedance (c_{eq} and r_{eq}), leading to a fluctuation in body potential:

$$S_{vb} = S_{ib} \cdot |z_b|^2 = S_{ib} \cdot |(\frac{1}{r_{eq}} + j\omega c_{eq})^{-1}|^2$$

$$= S_{ib} \cdot \frac{r_{eq}^{\ 2}}{1+(\frac{f}{f_c})^2} \tag{4.4}$$

where

$$S_{ib} = S_{ib1} + S_{ib2} \quad \text{and} \quad f_c = \frac{1}{2\pi \cdot r_{eq} c_{eq}}$$

The equivalent body-ground resistance r_{eq} is equal to the small-signal resistance of the body-source junction. The equivalent body-ground capacitance c_{eq} can be modeled as the sum of all the capacitance seen from the body. The schematic for r_{eq} and c_{eq} is shown in Fig. 4.2(b). And, the fluctuation in the body potential modulates the threshold voltage of the device:

$$S_{vth} = S_{vb} \cdot (\frac{\partial V_{th}}{\partial V_{bs}})^2 \tag{4.5}$$

Due to the fluctuation in $\mathbf{V_{th}}$, the excess drain current noise is given by:

$$S_{id-excess} = S_{vth} \cdot (\frac{\partial I_{ds}}{\partial V_{th}})^2 = \frac{(M+1) \cdot 2qI_{ii} g_{mb}^{\ 2} r_{eq}^{\ 2}}{1+(\frac{f}{f_c})^2} \tag{4.6}$$

where $\mathbf{g_{mb}}$ is the body trans-conductance. The excess noise shows a Lorentzian power spectrum, which is characterized by a constant plateau at low frequency and a $1/f^2$ roll-off at higher frequencies.

Since white noise, 1/f noise and excess noise are uncorrelated, the total spectrum density of low-frequency drain current noise is the sum of the three components (Fig 4.3):

$$S_{id-total} = S_{id-1/f} + S_{id-excess} + S_{id-white} \tag{4.7}$$

To verify the proposed low-frequency noise model, the noise measurement is conducted according to the setup shown in Fig. 4.4. The DC bias to the DUT is supplied by the Berkeley Technology Associate BTA9603 Noise Analyzer, which eliminates the residual noise in the bias voltages generated by HP4155C Semiconductor Parameter Analyzer. The noise current of the DUT is amplified by the low-noise amplifiers in BTA9603 before being applied to the Stanford Research SR780 Network Signal Analyzer (bandwidth: dc to 100 kHz) for FFT (fast Fourier transform). A computer installed with Noise Pro is used to automatically control the whole measurement.

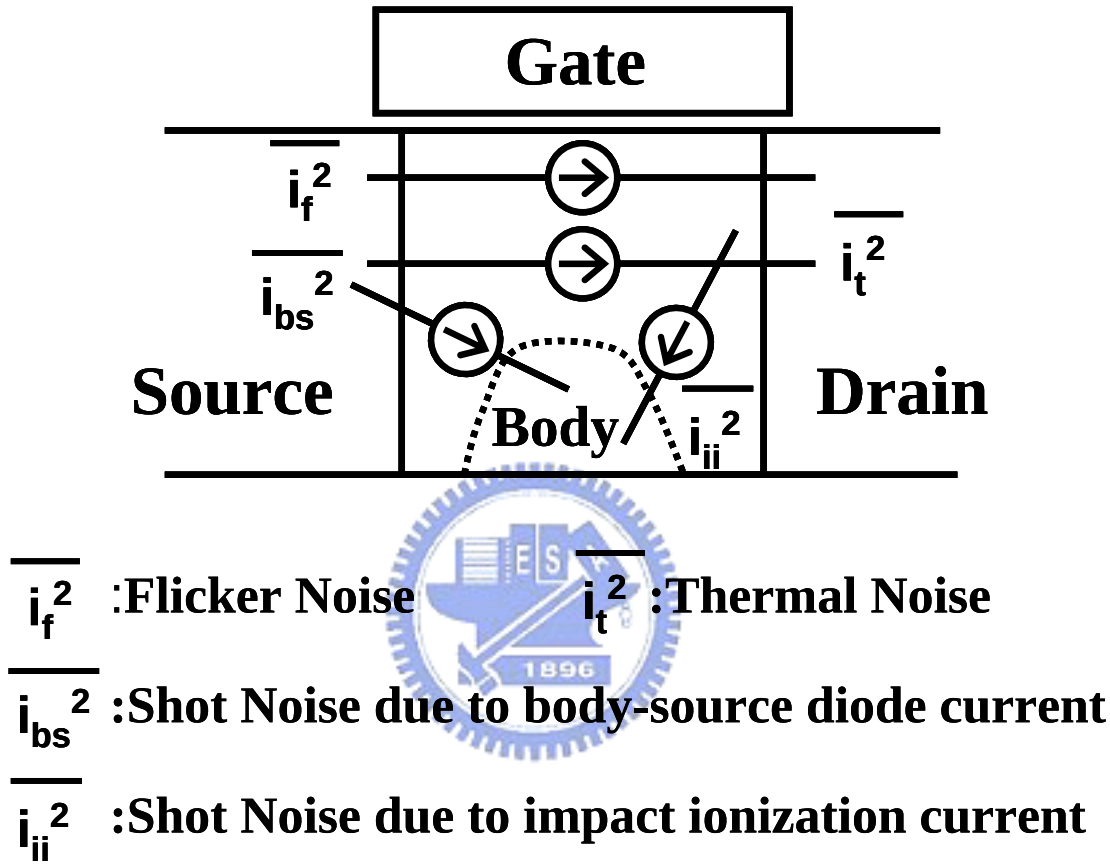

Fig.4.1 Noise sources in an SOI MOSFET.

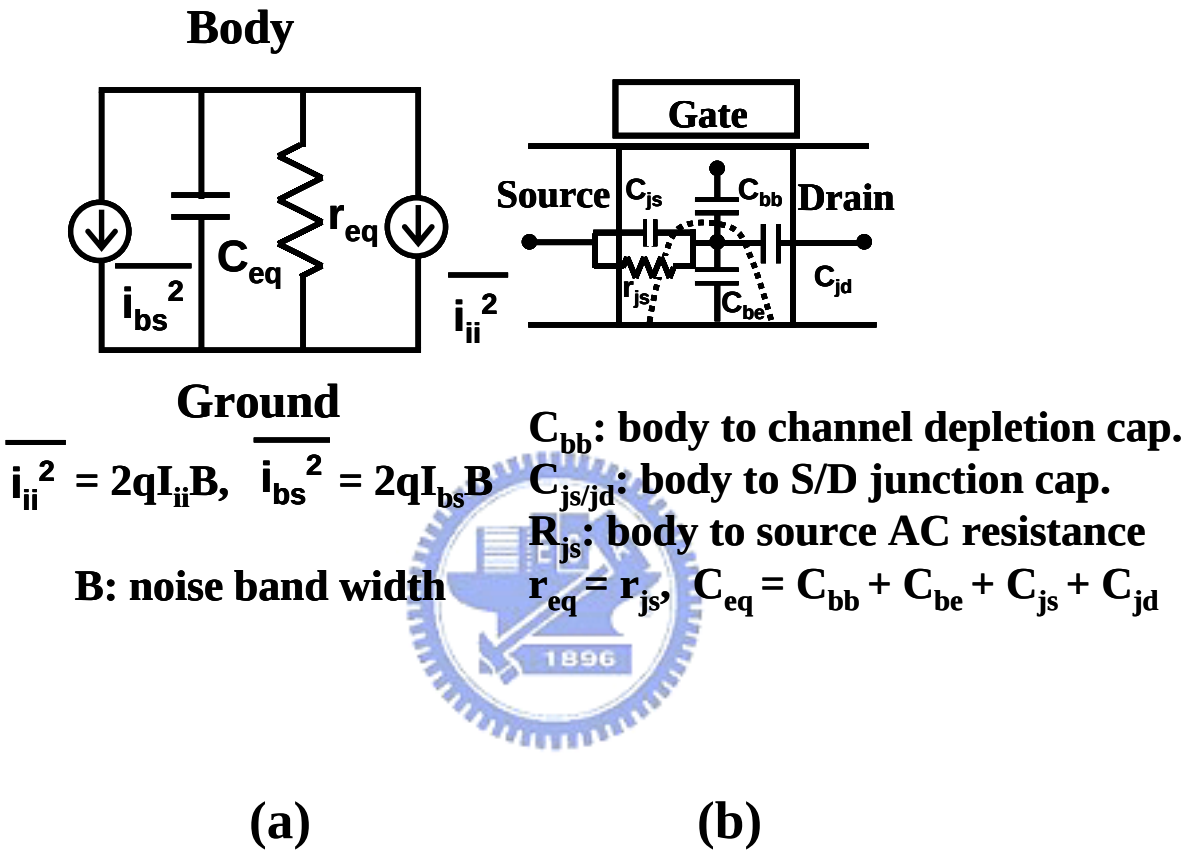

Fig.4.2 (a) Noise small-signal equivalent circuit for the floating-body and (b) schematic for the r_{eq} and C_{eq} network.

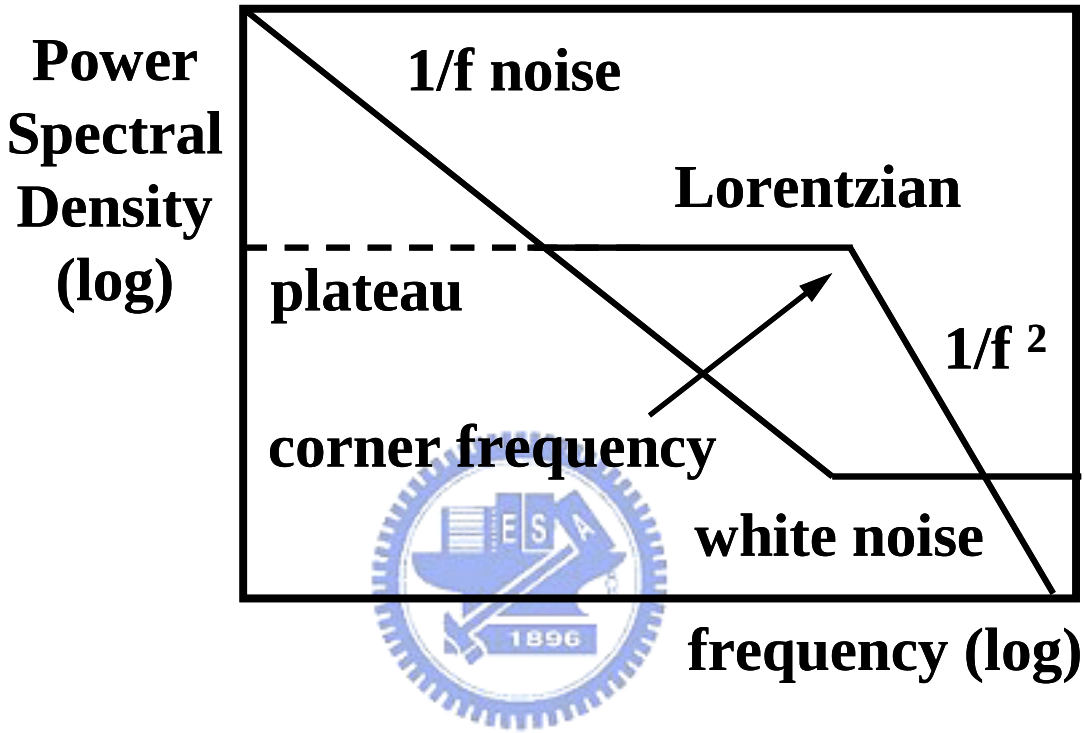

Fig.4.3 Typical input-referred low-frequency noise spectrum.

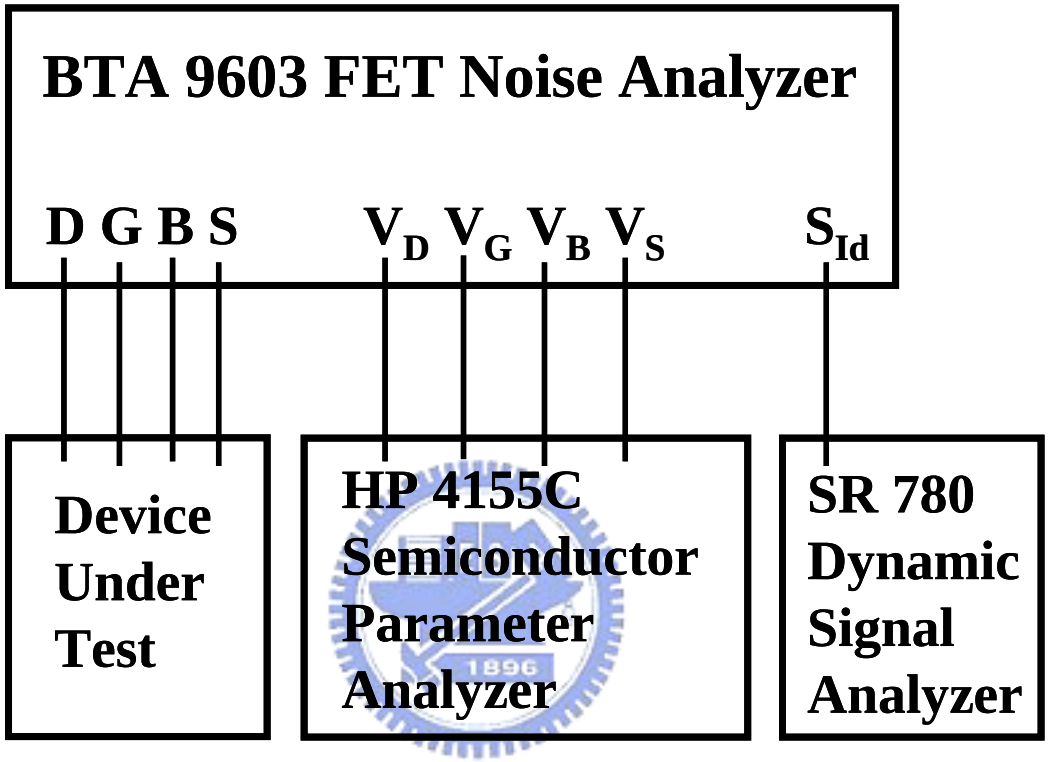

Fig.4.4 Low-frequency noise measurement setup.

4.3 Kink Effect Induced Excess Low-Frequency Noise

The SOI devices in this chapter were made with a 0.13μm standard CMOS process on p-type silicon substrate. Fig. 4.5 shows ours measured I_d-V_d characteristics of SOI n-MOSFETs (W/L = 10 μm/0.18 μm) with floating body and grounding body. Gate is biased at 0.9V. The kink effect is obviously observed in a floating body n-MOSFET and not in an n-MOSFET with body grounded. Due to the impact ionization current, electron-hole pairs are created at the drain end. Then, the holes go to the floating body, which induce the variation of body potential. At the kink point where the body potential sufficiently increases, threshold voltage drops and thus causes an increase of the drain current. The phenomenon in the floating body n-MOSFET consists with others results in PD SOI MOSFETs.[4.6] The excess noise is also found in floating body PD SOI MOSFET as the drain bias is above the kink voltage.

In Fig. 4.6, normalized noise power spectrum density in an n-MOSFET with body floated is measured at gate biased 0.9 V, and drain biased 0.5V、1.0V、1.2V、1.3V、1.4V、1.6V. Fig. 4.6 shows that the excess noise is not observable in the curve corresponding to the linear regime operation. As drain biases is above the kink onset voltage, the normalized noise power spectrum exhibits a plateau up to the characteristic frequency $f_c = 1/(2\pi \cdot r_{eq} c_{eq})$ before a $1/f^2$ roll-ff sets in. Furthermore, a typical Lorentzian shift to lower plateau and higher cut-off frequency is observed due to the increase of impact ionization current with the drain bias. Because the r_{eq} decreases with increasing drain voltage, a larger drain bias gives rise to a higher f_c but a smaller noise magnitude.

Additionally, Fig. 4.7 shows that normalized noise power spectrum density in an n-MOSFET with body grounded. Fig. 4.7 manifests that only flicker noise is exhibited at drain biased from linear regime to saturation regime. That is, the excess noise can be effectively eliminated, as body contact is grounded. Fig. 4.8 illustrates that the normalized drain current noise initially increases with the drain voltage and reaches a peak when the kink

point appears for a given frequency. This is when the device switches from linear operation regime to the regime around the kink point with the increase of the drain voltage.

The low-frequency noise in floating-body PD SOI MOSFETs is composed of 1/f noise and shot noise-induced excess noise. High drain bias gives rise to impact ionization current which flows through the floating-body to the source terminal. The shot noise causes fluctuation of body potential and threshold voltage, and consequently leads to excess noise in drain current. The RC network of the body in floating-body PD SOI MOSFETs amplifies and filters the shot noise, giving rise to a Lorentzian-like spectral density in noise. The noise peaks around the kink onset voltage for a given frequency. These experimental results consisted with previous mentioned noise model.

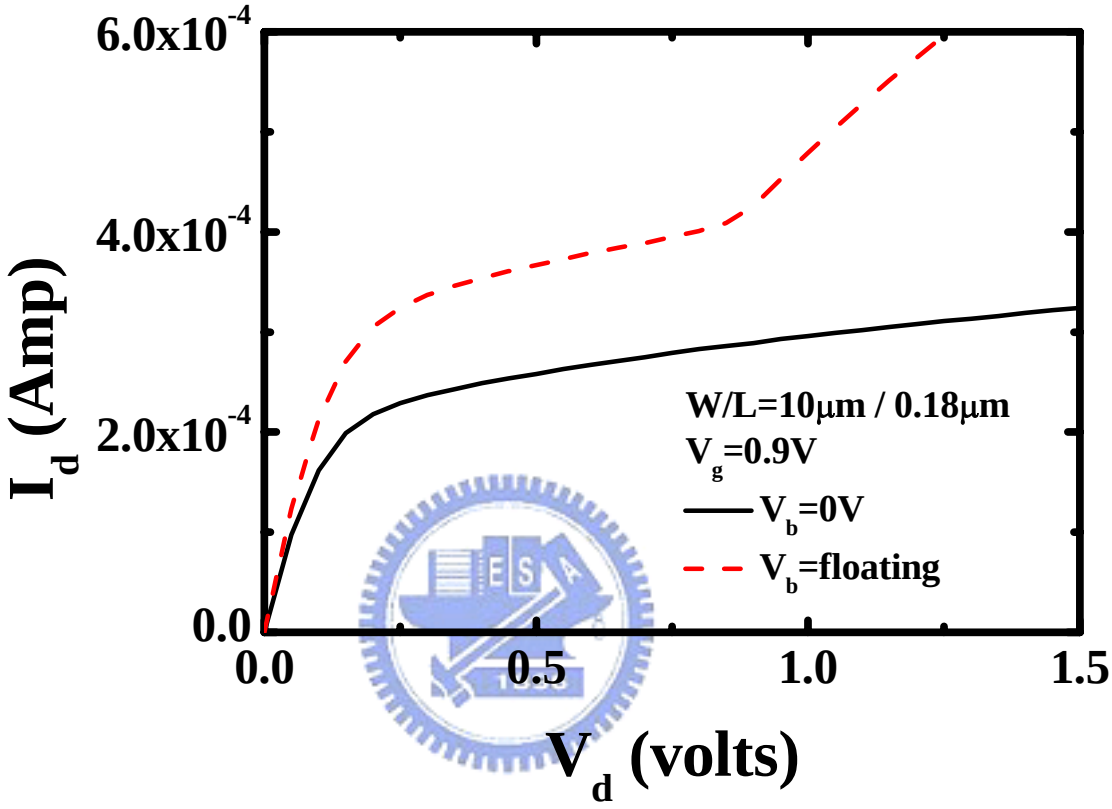

Fig.4.5 The I_d-V_d characteristics in nMOS SOI devices with floating body and grounding body when gate is biased at 0.9V.

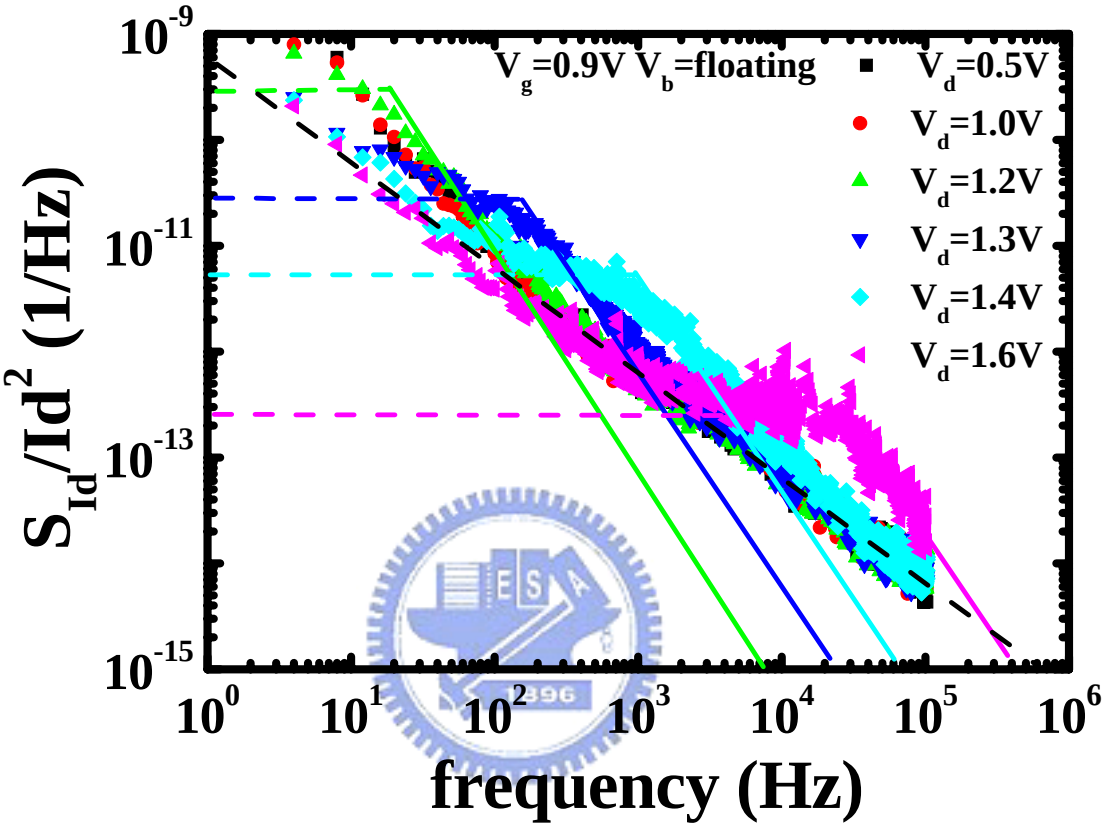

Fig.4.6 Normalization noise power spectral density in floating body nMOS SOI devices under different drain voltage when gate is biased at 0.9V.

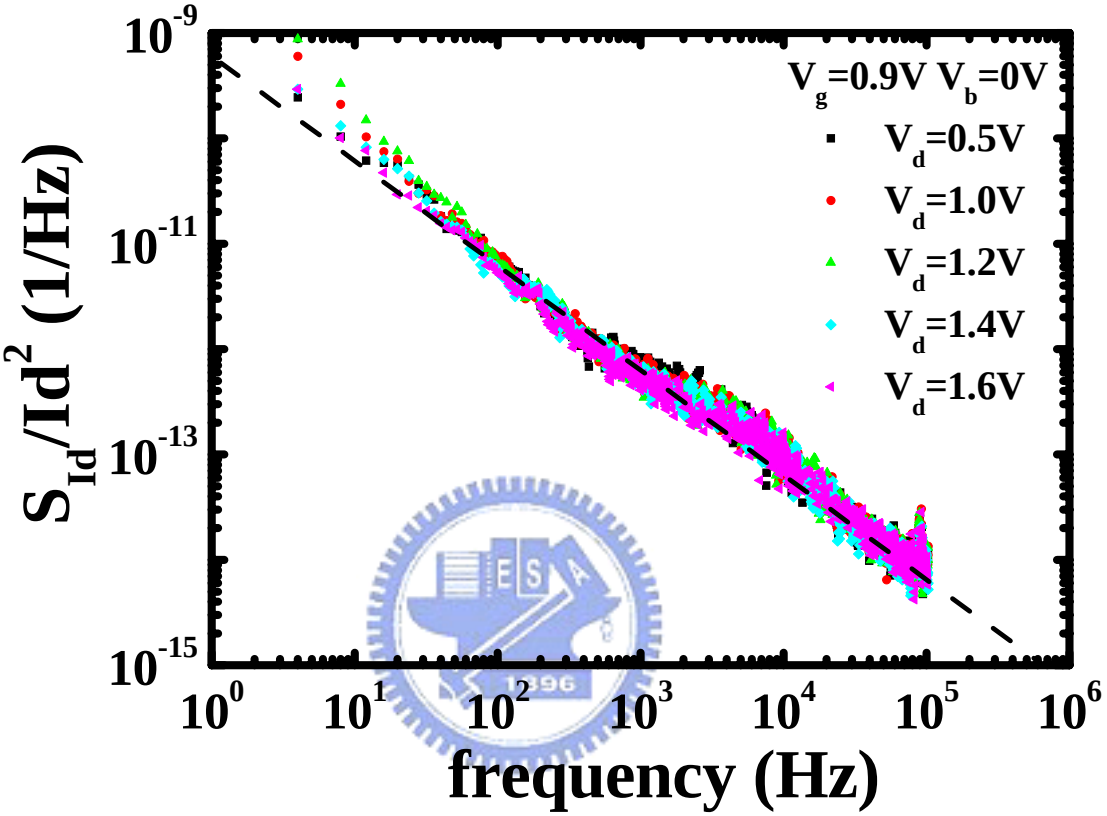

Fig.4.7 Normalization noise power spectral density in grounding body nMOS SOI devices under different drain voltage when gate is biased at 0.9V.

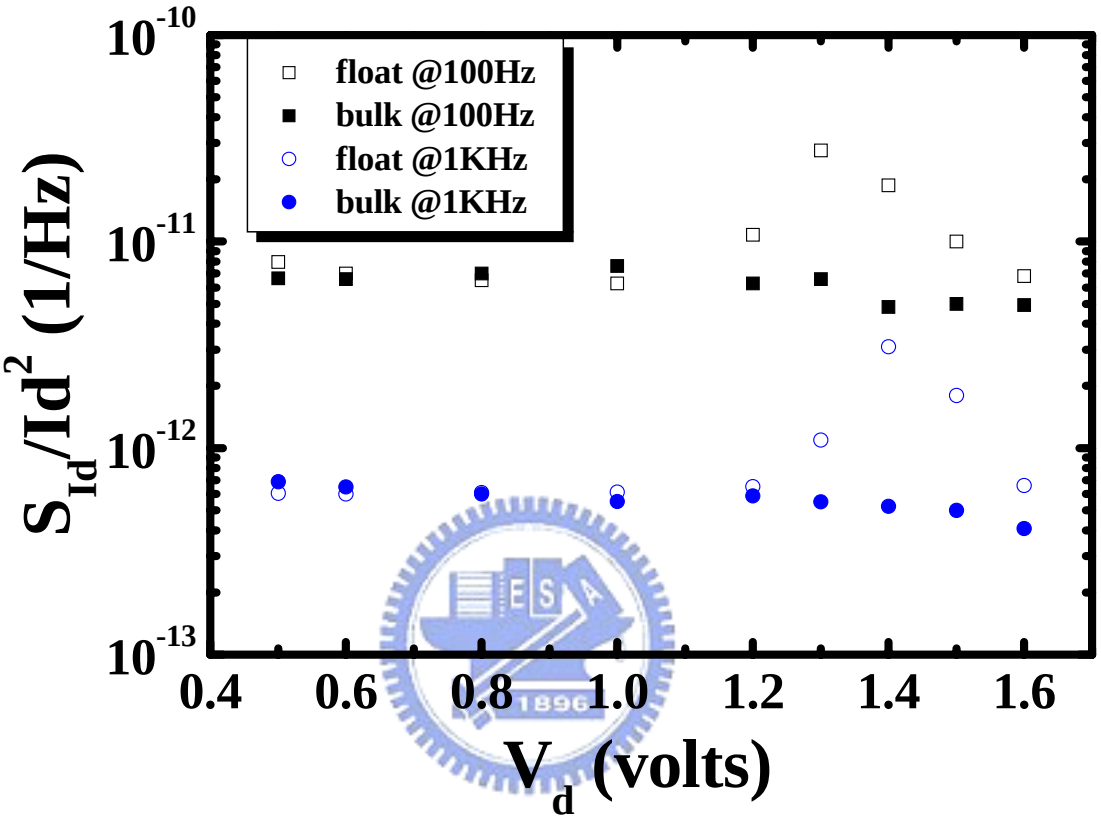

Fig.4.8 Comparison of normalization noise power spectral density under different drain bias in floating body SOI devices and grounding body SOI devices for given frequency.

4.4 Channel Soft Breakdown Enhanced Excess Low-Frequency Noise

The gate length of this section is 0.13μm, the gate width is 10μm and the oxide thickness is 1.6nm. All devices were stressed at high constant gate voltages with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10μA. After breakdown, the device on-state characteristics were checked and no difference was observed. Similarly, from others' study, [4.17-4.21] the impact of the gate oxide SBD is only a noticeable increase in leakage current without degrading any on-state device performance in operation.

The breakdown position was examined by using the method given in Chapter 3.[4.22] The measurement gate bias is V_g=-1.5V and V_d=V_s=0V in the accumulation region. A significant increase of I_d/I_s+I_d in device indicates that breakdown is located at the drain edge, while the moderate change in I_d/I_s+I_d implies that SBD position is in the channel. By utilizing the aforementioned technique of examining the breakdown location, the device electrical behaviors before and after various soft breakdown modes could be characterized. In Fig. 4.9, the gate current and substrate current as a function of V_g in fresh, channel-SBD, and edge-SBD n-MOSFETs were compared.

This comparison indicates that the substrate current increased drastically in channel-SBD devices, but the change in edge-SBD devices was negligible. The substrate current at a positive gate bias is attributed to channel hole creation resulting from valence-band electron tunneling from Si substrate to the conduction band of the poly gate. The tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band-gap of the n^+ poly-gate. Thus, these findings support the viewpoint that the post c-SBD I_b is enhanced largely at a positive gate bias due to a localized effective oxide thinning [4.23-4.25] while I_b is nearly unchanged after e-SBD. The results provide direct experimental evidence that channel soft breakdown may induce a substrate leakage current increase in device operation, especially at a high gate bias.

According to the above results, c-SBD enhanced substrate tunneling current in PD SOI MOSFETs is proposed as a new body-charging mode.[4.11,4.26-4.27] To further illustrate this point; the low frequency drain noise spectrums of SOI nMOSFET before and after both SBD modes are shown in Fig. 4.10. The measurement drain bias is 0.1V and the gate bias is 1.2V. The pre-BD noise characteristics of 1.6 nm gate oxide nMOSFET were dominated by a 1/f-like flicker noise component without other noise component of linear kink effect.[4.28] Suitable channel engineer process can eliminate the excess floating body noise of SOI device in advanced 0.13μm generation SOI technologies.[4.8,4.10] An additional Lorentizian-like spectrum appears only when both channel soft breakdown occurs and body contact is floated. As body contact is grounded, the excess noise can be effectively eliminated. The excess noise is also not observable in e-SBD devices. It indicates that the additional body charge injection of c-SBD devices not only enhances the V_t hysteresis effect but also degrades the LF noise spectrum.

Now, we would further investigate the gate bias dependence of the c-SBD induced excess floating body noise. Fig. 4.11 shows the normalized noise spectra of a floating body c-SBD SOI nMOSFETs under different gate biases. We observed a typical Lorentzian shift to lower plateau and higher cut-off frequency due to the valance band electron current increase with the gate bias. At V_g=1.6V, only 1/f noise is observed. In fact, we believe there is still a Lorentzian in this case but shifted to lower frequency, below our measurement capability. Note that the normalized 1/f noise remains almost constant over measurement gate bias in this ohmic region. This could be associated with the number fluctuation dominated in this measurement.[4.29-4.30] The excess noise of a c-SBD SOI devices with floating body shows similar behaviors to the excess noise induced by the kink effect in section 4.3.

Fig. 4.12 illustrates that for a given frequency, the normalized drain current noise of c-SBD floating body SOI devices initially increases with V_g and reaches a peak when gate bias is 1V. This phenomenon is consistent with other research claiming that the RC network of

the body in floating-body PD SOI nMOSFET's amplifies and filters the shot noise of substrate current, giving rise to a Lorentzian-like spectral density in noise.[4.6-4.9] It can be explained that with an increase in gate voltage, c-SBD induces more substrate current as a result of valance band electron tunneling. Further increase in gate bias leads to a low amplification gain by the floating-body to the shot noise, because the equivalent substrate resistance decreases with the substrate current increase, thus the noise magnitude decreases.[4.7]

4.5 Summary

The significance of soft breakdown position to the low frequency drain current noise in floating body PD SOI nMOSFETs has been evaluated. The excess floating body noise of nMOSFETs would be enhanced if a breakdown path occurs at the channel. The enhanced noise correlates with channel soft breakdown induced large substrate current of valance band electron tunneling. This noise sources origins from the amplification by small white noise of the substrate current. The c-SBD enhanced excess noise may occur even with supply voltage less than 1.0V and would be a serious reliability concern in ultra-thin oxide analog SOI devices.

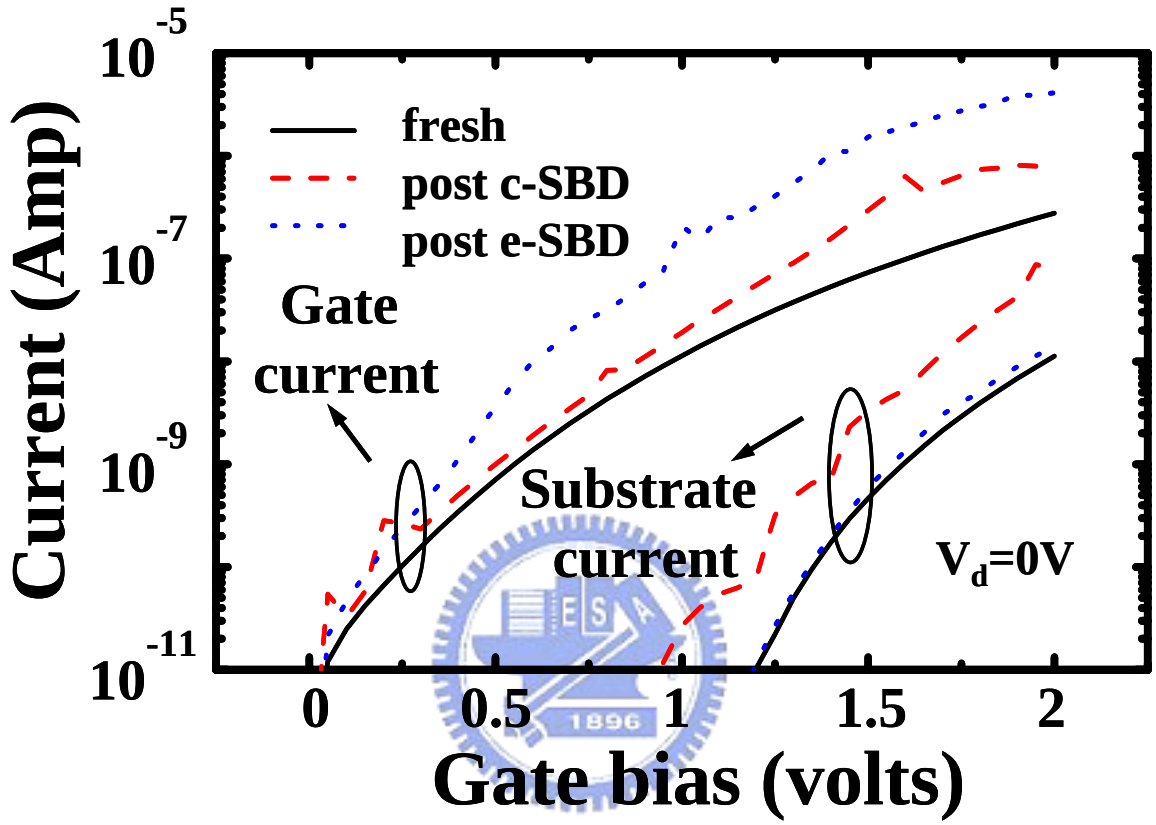

Fig.4.9 The gate current and substrate current as a function of V_g in fresh, channel SBD, and edge SBD n-MOSFETs were compared.

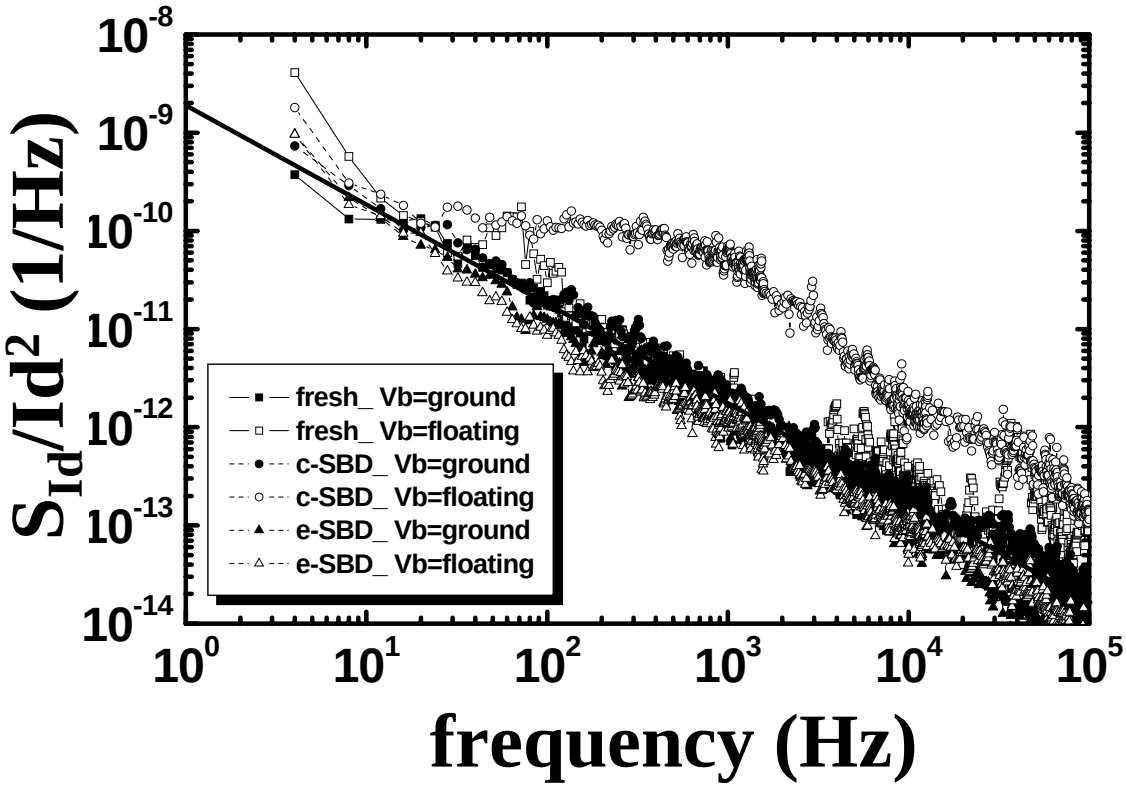

Fig.4.10 The low frequency drain noise spectrums of n-MOSFET before and after two SBD modes. The measurement drain bias is 0.1V and the gate bias is 1.2V.

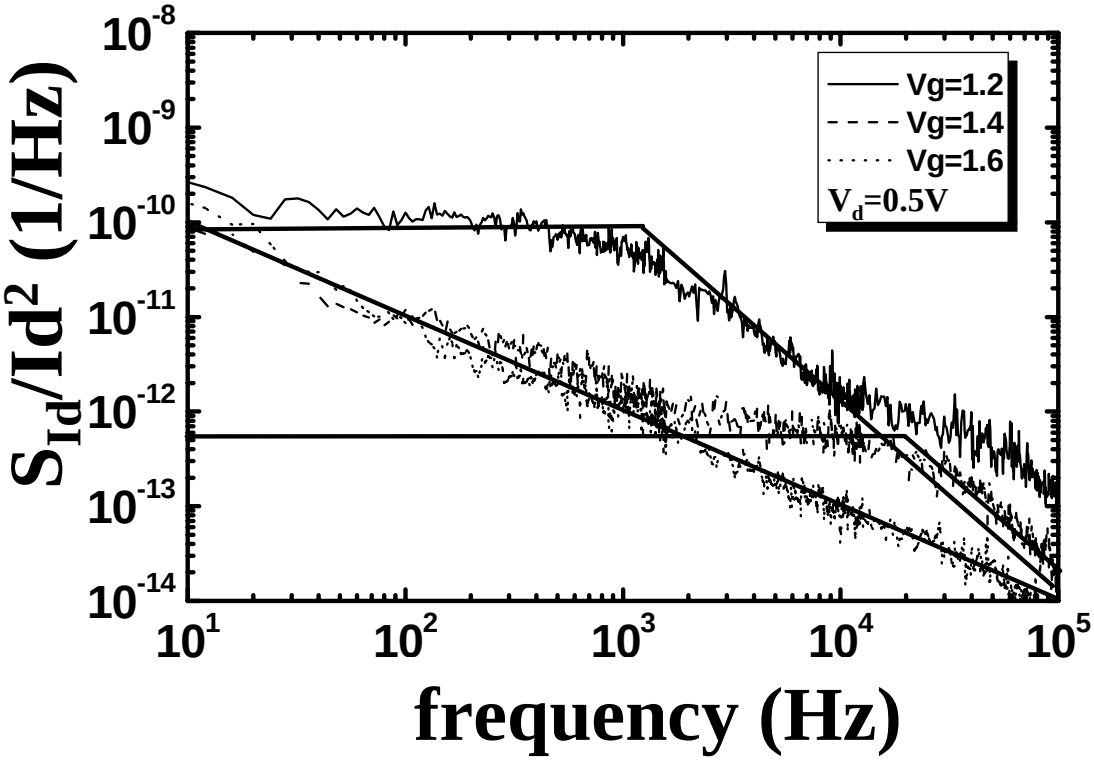

Fig.4.11 The normalized noise power spectrum of a c-SBD nMOS SOI device with floating body under different gate biases.

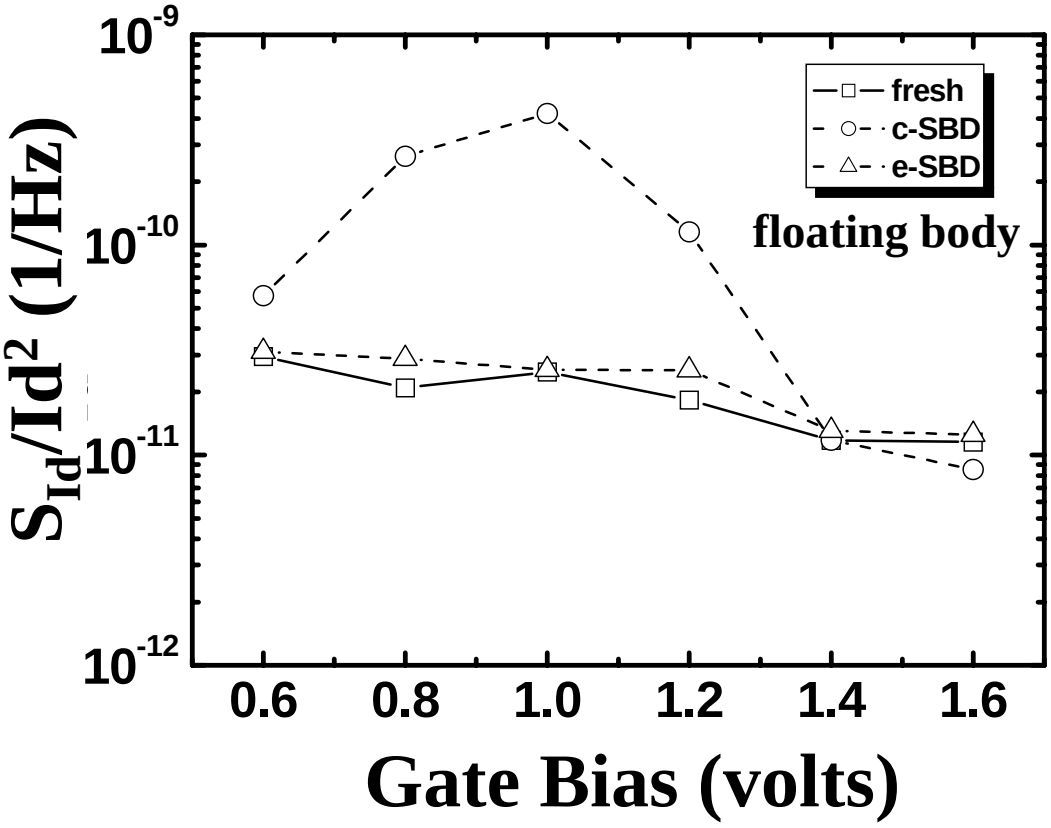

Fig.4.12 Comparison of normalized noise power spectral density with floating body under different gate bias in a fresh device, c-SBD device and e-SBD device at f=100Hz.

Chapter 5
Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI p-MOSFETs

5.1 Introduction

The aggressive scaling of advanced complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs) has pushed the gate oxide thickness towards its limit in terms of reliability.[5.1-5.4] In ultra-thin gate oxide MOSFETs, oxide breakdown (BD) has been shown to evolve in a continuous manner from initial stages to final shorting.[5.5-5.7] Previous study has shown that a small increase in gate leakage due to oxide BD does not disrupt circuit operation, and the failure criterion should be changed to a higher level of gate leakage.[5.8-5.9] Therefore, the oxide failure time is determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate. Presently, the silicon-on-insulator (SOI) technology has emerged to be a candidate for advanced CMOS technology for its higher performance. The BD progression in conventional bulk CMOS devices [5.10-5.12] has been widely investigated. In this chapter, we will investigate the influence of floating body effect on BD progression in partially depleted (PD) p-type SOI MOSFETs.

Several concerns of hard breakdown evolution in ultra-thin oxides have been proposed.[5.7-5.14] Monsieur et al [5.7] reported that for low gate stress bias, the defect generation rate being very low, the degradation of the BD conduction path becomes macroscopic and can last thousands of seconds even in the case of accelerated test. Linder et al [5.9] showed that the growth of BD current could be exponentially dependent on gate bias, oxide thickness, and any other parasitics, such as inversion layer resistances, altering the observed growth rate drastically. Alam et al [5.13] indicated that circuits do continue to operate after the first soft breakdown (SBD), and suggested that the standard reliability

specification is too restrictive, and should be redefined, particularly for pMOS devices. In ultra-thin oxide pMOSFETs, enhanced gate oxide BD growth rate was observed with a negative substrate bias.[5.14] Furthermore, the floating body configuration of partially depleted SOI CMOS may result in a non-zero body voltage due to various body charging mechanisms [5.15-5.18] and thus affects oxide BD evolution. The objective of this chapter is therefore to investigate floating body effect on BD progression rate. A model based on breakdown induced channel carrier heating will be proposed to explain the observed phenomenon.

5.2 Devices and Experiment

The devices in this work were made with an optimized 0.13μm CMOS process on p-type SOI wafer and have a gate length of 0.5μm, a gate width of 2μm and an oxide thickness of 1.6nm. The gate oxide was grown with rapid plasma nitridation (RPN) process. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this chapter, all devices were stressed at constant gate voltage with the source and drain grounded. Fig. 5.1 shows typical BD evolution in a 1.4nm oxide and a 2.5nm oxide bulk pMOSFETs. In the 1.4nm gate oxide pMOSFET, oxide BD is evolved in a progressive way, and the gate leakage current increases gradually with stress time. As a contrast, the 2.5nm oxide pMOSFET exhibits an abrupt jump in gate leakage current after BD. Since a slight gate leakage increase due to oxide BD is considered to be nondestructive for circuit operation [5.8], we define oxide breakdown time (t_{BD}) and device fail time (t_{fail}) as the time when the gate leakage current reaches 1.5 times and 15 times its pre-stress value, respectively.

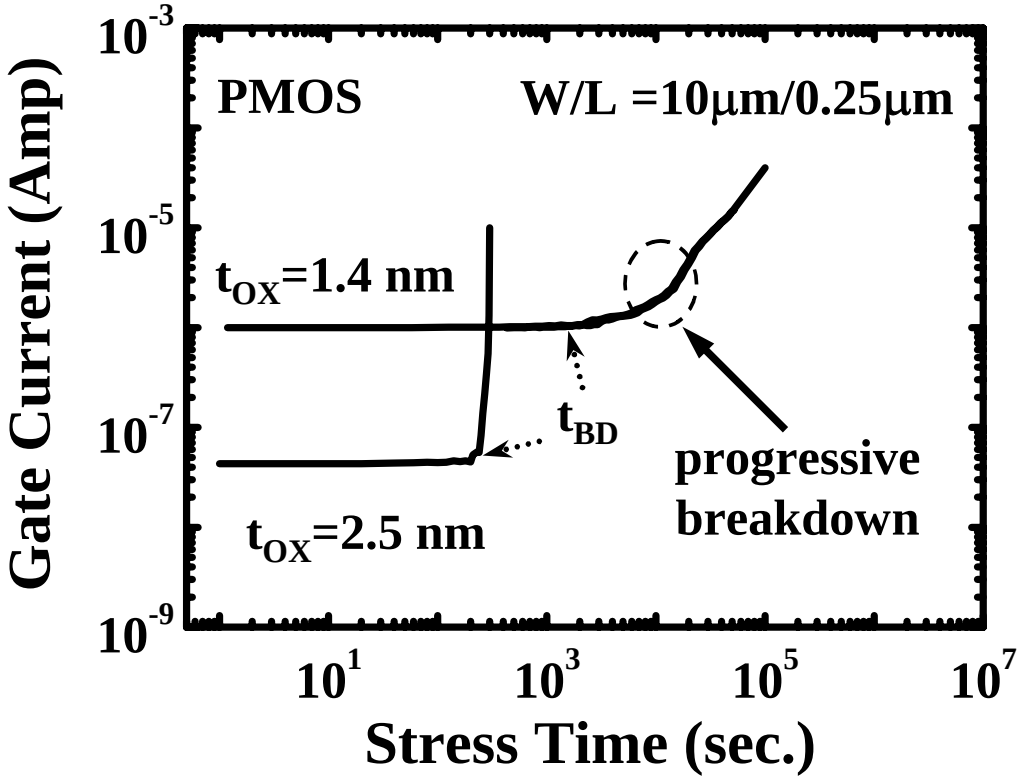

Fig.5.1 Comparsion of breakdown behavior in a 1.4nm oxide pMOSFETand in a 2.5nm oxide pMOSFET. The stress gate voltage is –3V for the 1.4nm oxide and –4.5V for the 2.5nm oxide. t_{BD} denotes the onset time of oxide breakdown.

5.3 Result and Discussion

5.3.1 A Shorter t_{fail} in SOI pMOSFETs

Fig. 5.2 shows the gate leakage current evolution with stress time at a stress gate voltage of V_g=-2.9V for various applied substrate biases (V_b) in pMOSFETs. The oxide t_{BD} is almost the same for different substrate biases. This can be understood because oxide defect generation rate is dependent on injected charge energy and fluence during stress [5.19-5.22], regardless of applied substrate bias. After the onset of BD, the BD growth rate exhibits an apparent dependence on substrate bias. A forward substrate bias can significantly enhance BD growth rate. It should be noted that the SOI device with floating body configuration has the worst BD progression rate in Fig. 5.2. The statistic Weibull distributions of oxide t_{BD} and t_{fail} for SOI (floating substrate) and bulk (grounding substrate) pMOSFETs are plotted in Fig. 5.3. Although the floating substrate configuration does not affect t_{BD}, it does cause a 2 times shorter t_{fail} than in bulk pMOSFETs.

5.3.2 Mechanism of Enhanced BD Progression in SOI

The floating body configuration of SOI devices may result in a small forward body voltage due to various body charging processes. In an ultra-thin oxide pMOSFET, the gate stress current may have comparable electron and hole components at a negative gate bias. To analyze the polarity of dominant stress current in a pMOSFET, a charge separation technique is utilized to measure electron stress current and hole stress current. The inset of Fig. 5.4 illustrates the carrier flow at a negative gate bias, I_b denotes electron current and comes from valance-band electron tunneling from the gate electrode. I_{sd} stands for hole tunneling current from the inverted channel. The substrate bias dependence of electron current and hole current before and after t_{BD} is shown in Fig. 5.4. Note that the electron and hole currents in a fresh device are independent of substrate bias. Interestingly, the post-t_{BD} hole current, unlike the pre-BD I_b and I_{sd}, exhibits a significant V_b dependence. Furthermore, Fig. 5.5 reveals that the

V_b dependence of the post-t_{BD} hole current increases with BD evolution. Since the hole stress current dominates gate stress during BD evolution and increases with a forward body bias, the enhanced BD progression in a floating body configuration can be understood.

5.3.3 BD Caused Carrier Heating

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 5.4), the possibility that the V_b dependence of the post-t_{BD} hole current is caused by the variation of effective gate-to-channel voltage resulting from V_b modulated channel resistance can be excluded. Otherwise, the post-t_{BD} I_b should have the same V_b effect as the post-t_{BD} I_{sd}. Moreover, substrate impact ionization and negative bias-temperature instability effects are also excluded because the trend of the V_b dependence is opposite.

To further investigate the origin of the V_b dependence of the post-t_{BD} hole current, we measured the spectral distribution of hot carrier light emission before and after t_{BD} (Fig. 5.6). The light intensity is greatly increased after oxide BD. The high-energy tail of the post-t_{BD} spectral distribution indicates the rise of the carrier temperature. Similar finding was also reported by other groups.[5.23] The extracted carrier temperature from the high-energy tail of the spectrum is around 1300^{o} K (Fig. 5.6(b)). There are two possible theories to explain the rise of channel carrier temperature at a BD spot. First, based on the model proposed by Rasras et al [5.23], the gate voltage may penetrate into the substrate after BD and causes lateral field heating of channel carriers. However, this process is unlikely here since the post-t_{BD} electron current and hole current have distinctly different V_b dependence. The second possible reason is that high-dissipated energy, released by valence electrons tunneling from the gate through the BD path, will locally produce a rise of hole temperature. A temperature range of 1000^{o} K to 2000^{o} K was estimated in Ref. [5.24]. Electron-hole scattering or Auger recombination is suspected to be the responsible energy transfer process.

To show that the rise of hole temperature may account for the observed V_b dependence,

we calculate the hole tunneling current with hole temperature at 300°K and 1300°K. In our calculation, we solve the coupled Poisson and Schrodinger equations to obtain the sub-band structure for the inversion holes (Fig. 5.7). A simple one-band effective mass approximation is used for simplicity. The hole tunneling current density is calculated according to the Tsu-Esaki formula [5.25]

$$J_{sd} = qm^*_{//}\left(\frac{1}{2\pi^2\hbar^3}\right)k_BT\sum_n D_n\{\ln(1+\exp((E_n - E_f)/k_BT))) - \ln(1+\exp((E_n - E_{f'})/k_BT)))\} \quad (5\text{-}1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the n-th sub-band. m^* is the hole effective mass in Si. Other variables have their usual definitions. It should be emphasized that it is not our intention to consider detailed trap-assisted charge transport in the BD path. It is also not our intension to calculate the precise current value before and after oxide BD, since the BD area and BD caused effective oxide thinning cannot be easily determined. Instead, our purpose is to investigate the effect of hole temperature on the inversion hole distribution in different sub-bands and the corresponding substrate bias effect on hole tunneling current. Therefore, a simple WKB formula for direct tunneling is employed for D_n.

Our result in Fig. 5.8 clearly shows that the hole tunneling current exhibits a larger V_b dependence at 1300 °K. The simulation can well interpret the measured V_b dependence of the post-t_{BD} I_{sd} by simply using an elevated hole temperature. The trend in Fig. 5.8 is similar to the measured V_b dependence in Fig. 5.5. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three sub-bands is given in Table. 5.1. At T=300 °K, channel holes mostly reside in the first sub-band no matter of V_b. At T=1300 °K, a large part of holes are thermally excited to higher sub-bands at a

forward body voltage (-0.5V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at negative body voltages.

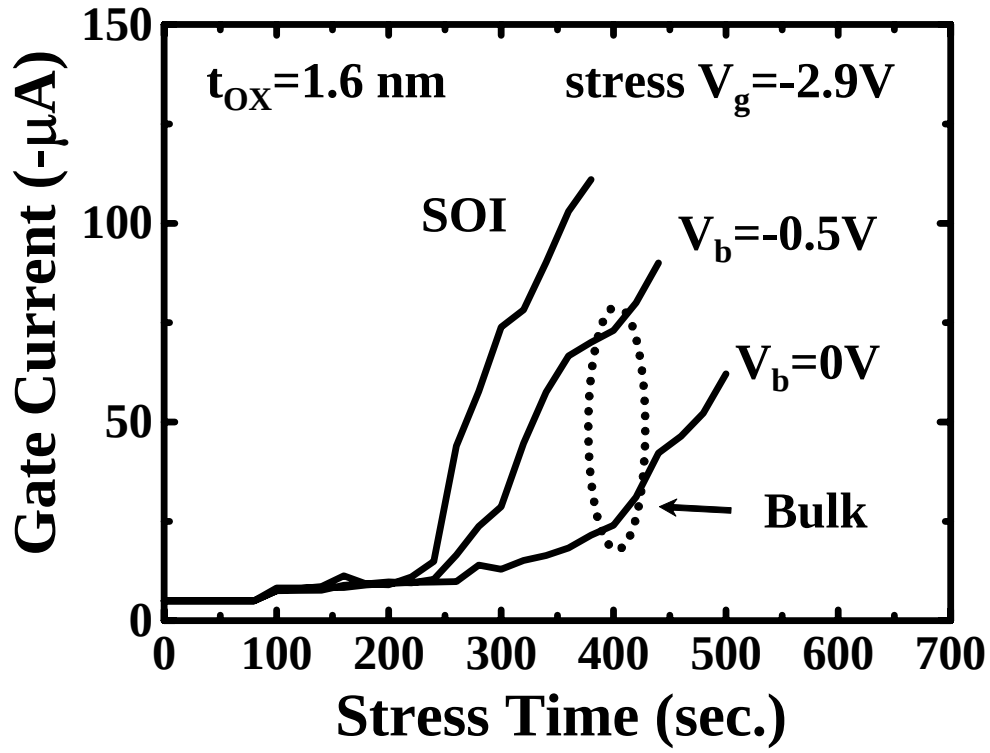

Fig.5.2 Oxide breakdown progression in bulk and SOI pMOSFETs. The stress gate bias is –2.9V and temperature is 125^{o} C.

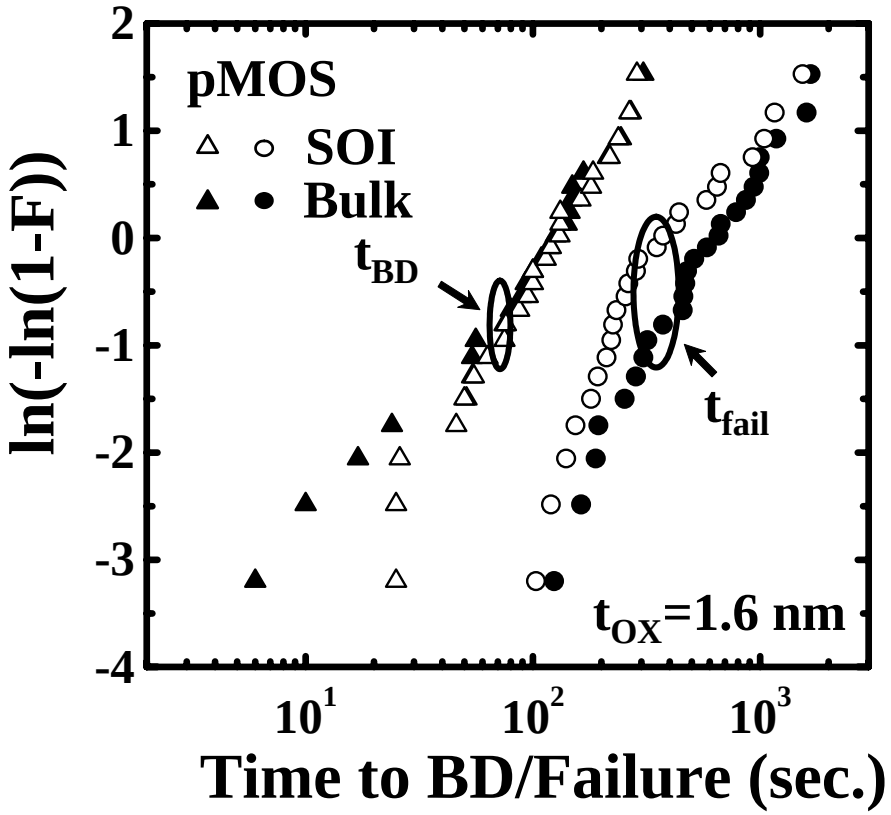

Fig.5.3 The Weibull plots of t_{BD} and t_{fail} distribution for 1.6nm oxide SOI and bulk pMOSFETs. The stress gate bias is –2.9V and the temperature is 125^{o}C. t_{BD} and t_{fail} are defined as the time for gate current to reach 1.5 times and 15 times its pre-stress value, respectively.

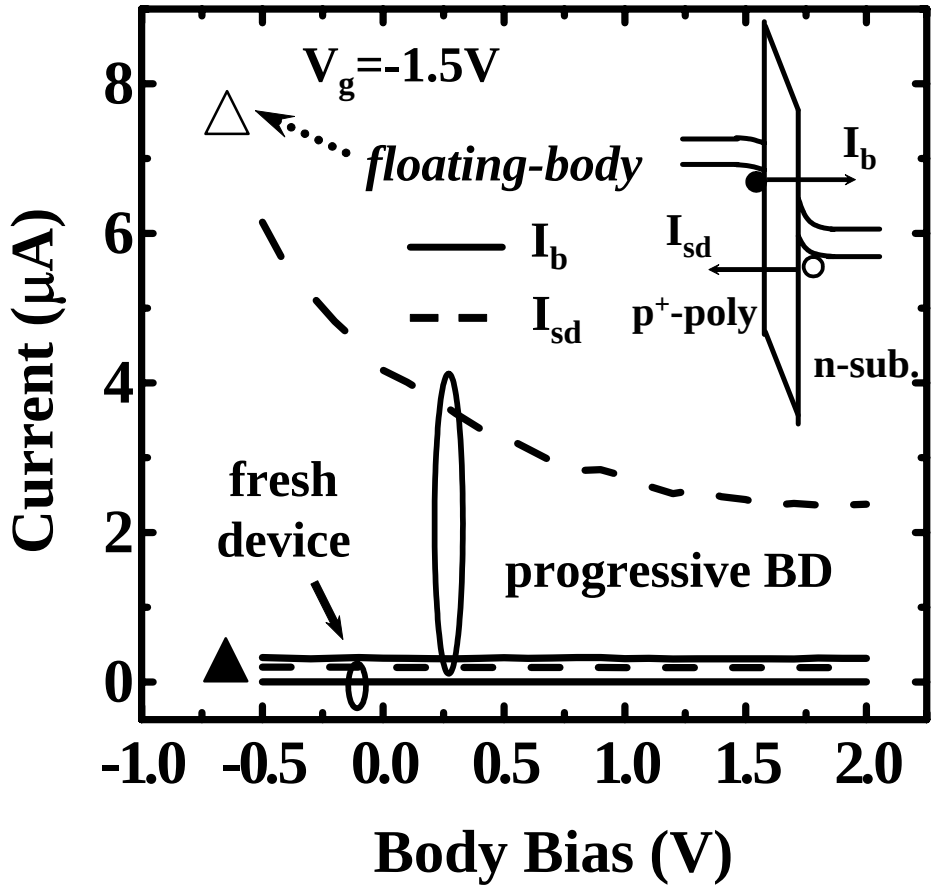

Fig.5.4 The V_b dependence of pre-BD and post-BD electron currents (I_b) and hole currents (I_{sd}) at V_g=-1.5V. Distinct V_b dependence of the post-t_{BD} I_{sd} is noted. The floating body configuration corresponds to a body voltage of approximately -0.65V. The inset illustrates carrier flow in a pMOSFET at a negative gate bias.

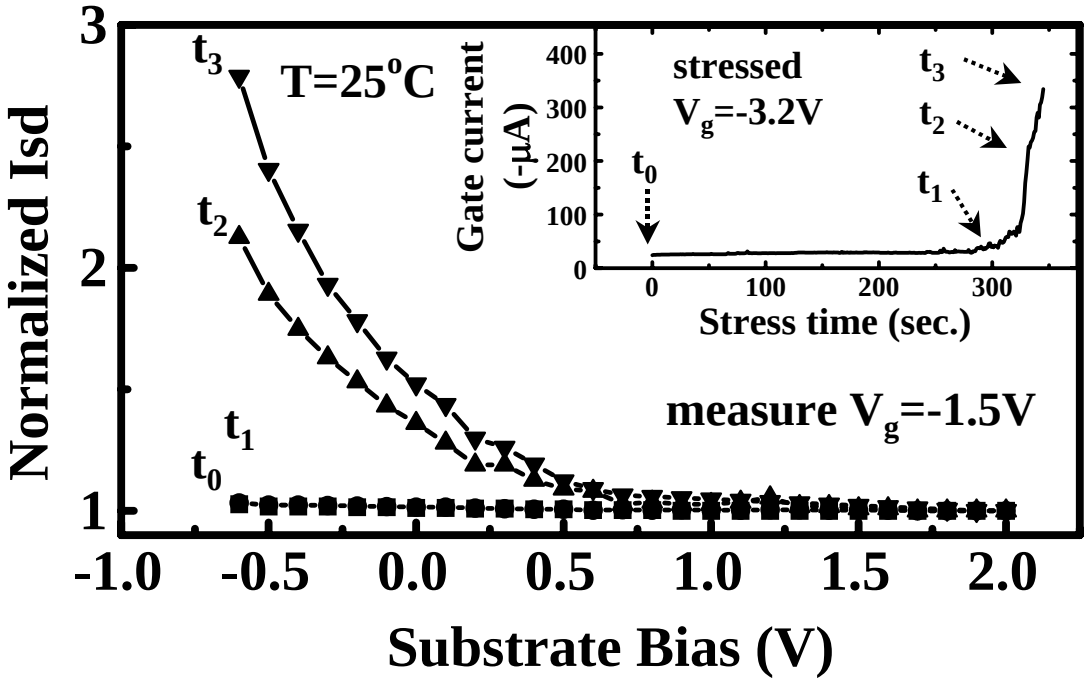

Fig.5.5 The V_b dependence of the hole current I_{sd} at different stress times, t_0, t_1, t_2 and t_3. I_{sd} is normalized to its value at V_b=2V. Gate current vs. stress time in a stress condition of V_g=-3.2V and T=25° C is shown in the inset.

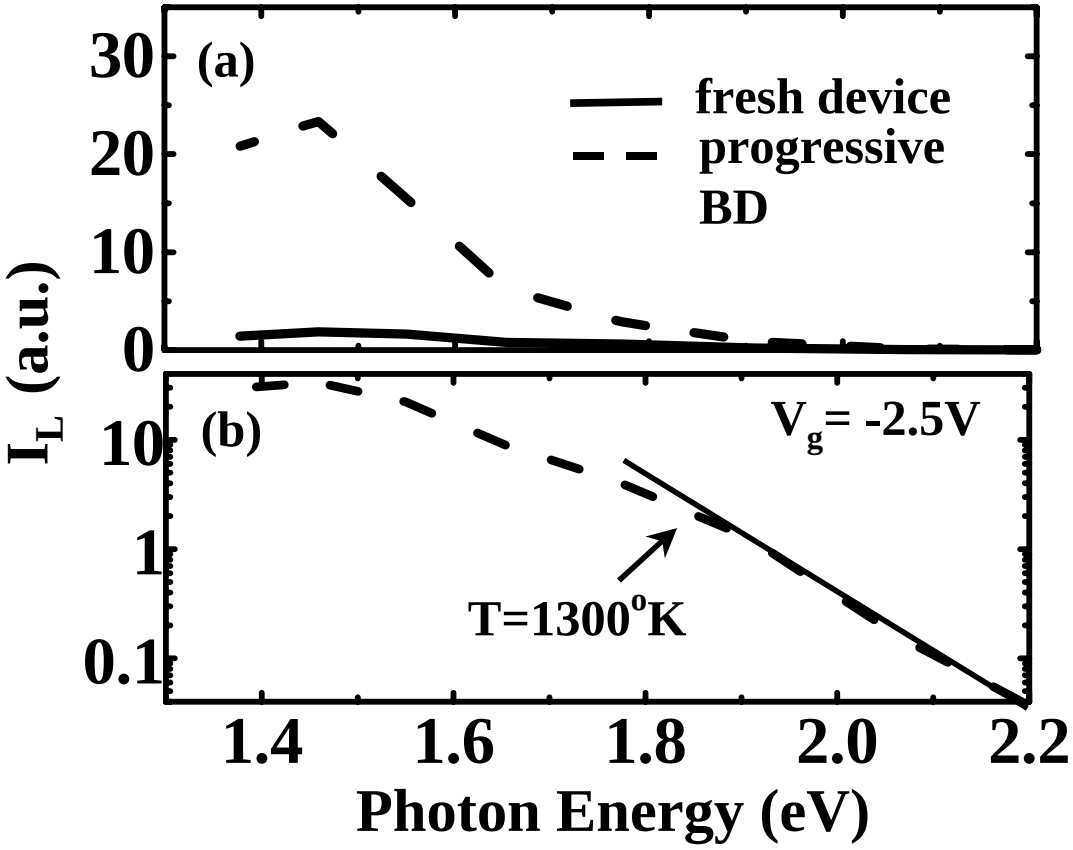

Fig.5.6 Spectral distribution of light emission in a 1.4nm oxide pMOSFET at V_g=-2.5V. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 ^{o} K.

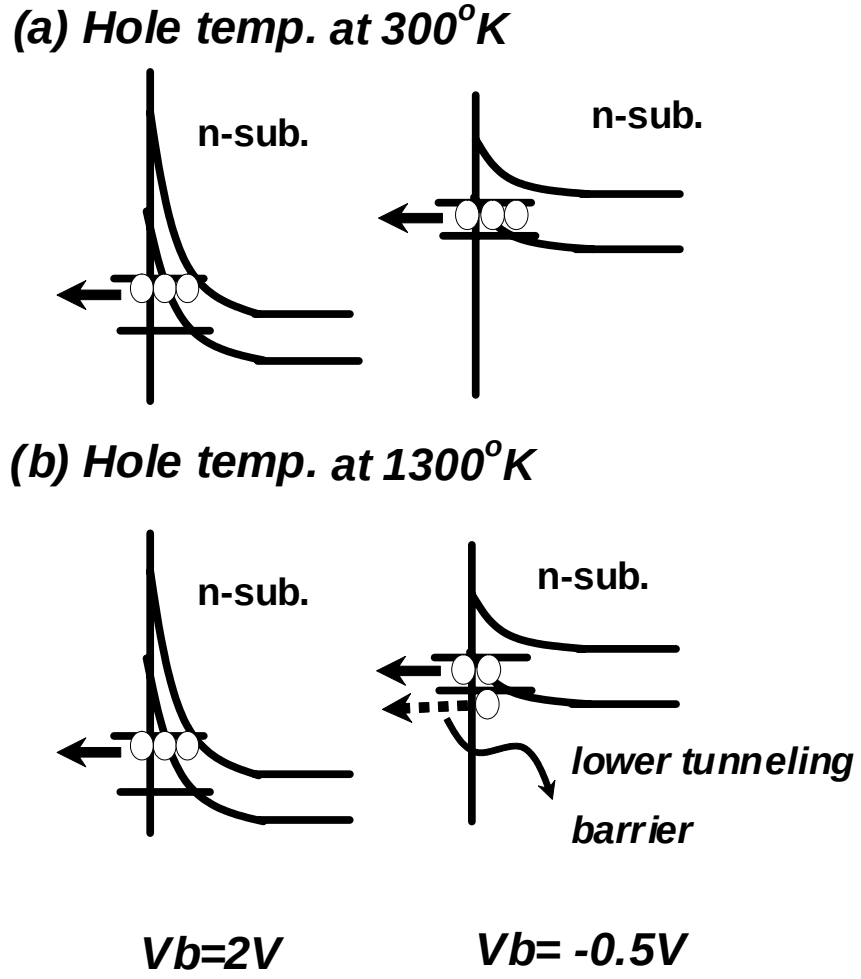

Fig.5.7 Illustration of hole distribution in sub-bands at a hole temperature of 300 ^{o} K and 1300 ^{o} K. Higher carrier temperature results in a larger V_b effect.

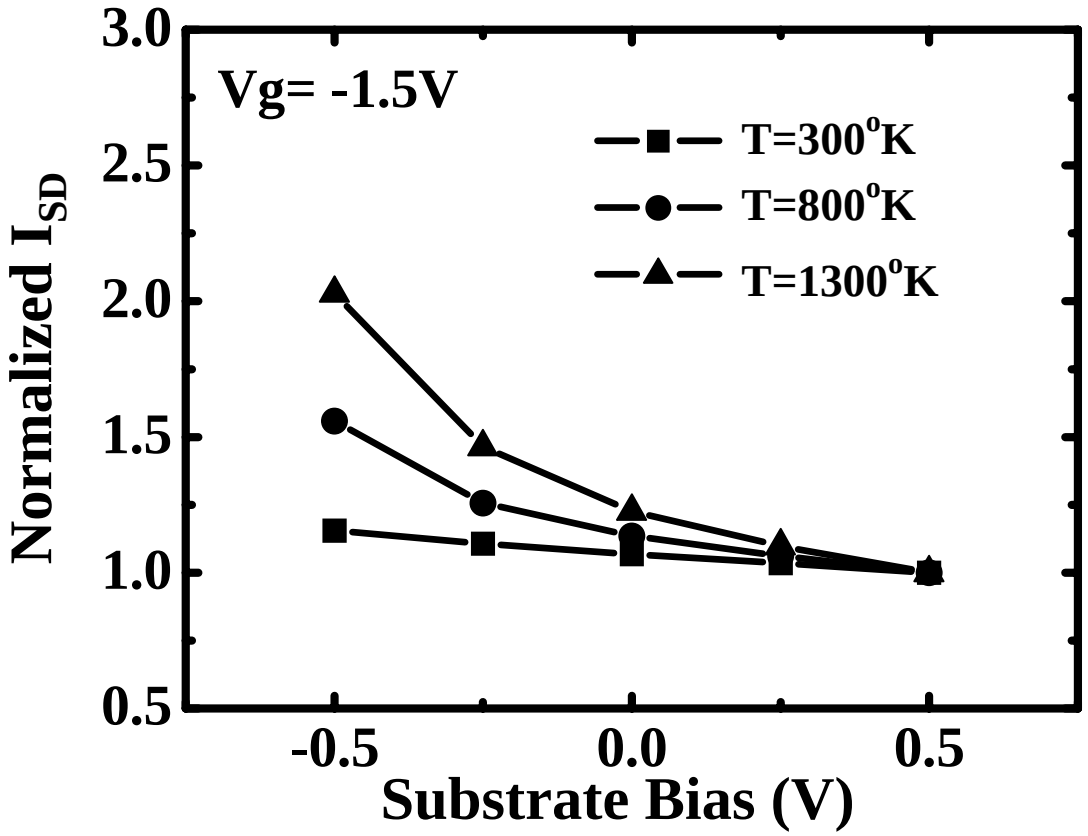

Fig.5.8 Simulated substrate bias effect on hole tunneling current in a 1.6nm oxide pMOSFET. I_{sd} is normalized to its value at V_b=2V. Simulated V_g=-1.5V.

cond. / sub-band	channel hole dist. (%)			
	300°K		**1300°K**	
	V_b=-0.5	V_b=2	V_b=-0.5	V_b=2
1st	96.6%	99.5%	39.8%	99.4%
2nd	3%	0.5%	18%	0.6%
3rd	0.3%	0%	11.6%	0%

Table 5.1 Calculated distributions of channel holes in the lowest three sub-bands. The gate bias in simulation is –1.5V. The parameters used in simulation is m*(Si) = $0.67m_0$, m*(SiO_2) = $0.55m_0$, ϕ_h (hole barrier height at SiO_2 interface) = 4.25eV, t_{ox} = 1.6nm, and N_B (substrate doping) = $1x10^{18}cm^{-3}$.

5.4 The Impact of Gate Stress Bias

From previous discussion, the V_b dependence of hole stress current was identified to be the origin of the floating-body enhanced BD progression. Now, the impact of gate stress bias scaling on the enhanced BD progression is explored. Fig. 5.9 shows the V_b dependence of BD current at various measurement gate biases. The V_b dependence is more distinguished at a smaller gate bias. Fig. 5.10 shows the range of the gate stress bias where hole current is dominant. The hole current dominates gate stress at small gate biases (less than ~3.0V) and the hole component of the stress current increases during BD evolution. This result is consistent with the findings in Fig. 5.9 that a large V_b dependence of the post-BD stress current is obtained at smaller gate voltages. Fig. 5.11 compares the 63% time-to-failure in SOI and bulk pMOSFETs at various gate stress biases. Accelerated BD progression is noticed in SOI samples and the trend becomes more apparent at lower gate stress biases. Fig. 5.12 shows the range of oxide thickness and stress gate voltage where the hole current component is dominant in a fresh device and after breakdown. For example, for an oxide thickness of 1.6nm, hole current is dominant in stress for V_g<2.5V in a fresh device and for V_g <3.0V after BD. High-energy electron impact ionization does not need to be considered until V_g is above 3.5V. Fig. 5.12 also reveals that the hole current dominant region increases not only with BD progression but with decreasing oxide thickness. It implies that the floating body enhanced BD progression will become more significant as oxide thickness scales down.

5.5 Summary

In ultra-thin oxide SOI pMOSFETs, breakdown progression is aggravated by a forward body bias. An enhanced post-t_{BD} gate current is observed in SOI devices due to the charging of the floating body. Numerical analysis shows that the V_b enhanced hole stress current can be explained by the increase of hole temperature at the breakdown spot. The V_b accelerated BD progression is more significant at a lower stress gate bias and for a thinner oxide.

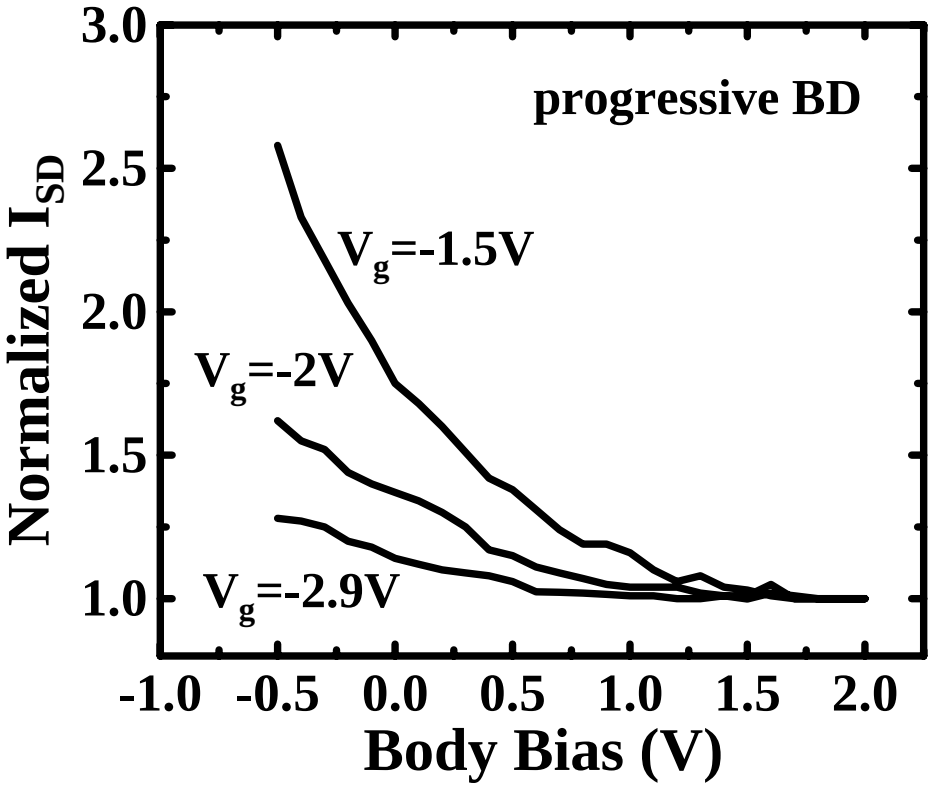

Fig.5.9 Substrate bias dependence of the post-BD hole current at various gate biases. I_{sd} is normalized to its value at V_b=2V.

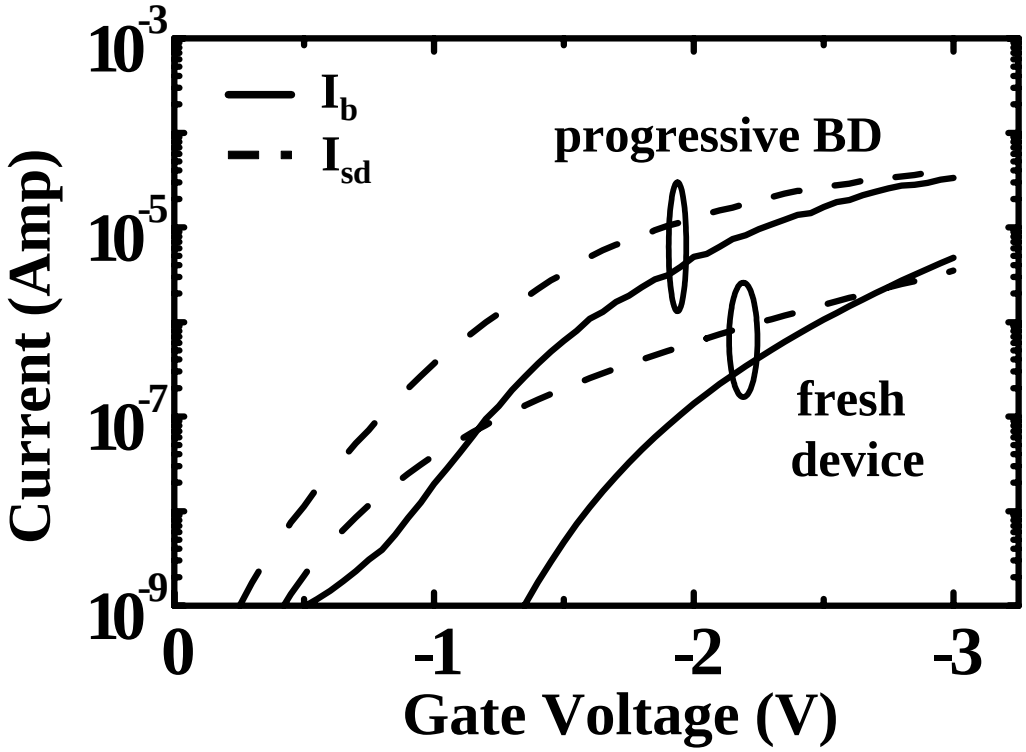

Fig.5.10 Gate bias dependence of electron current and hole current in a fresh pMOSFET and during progressive BD.

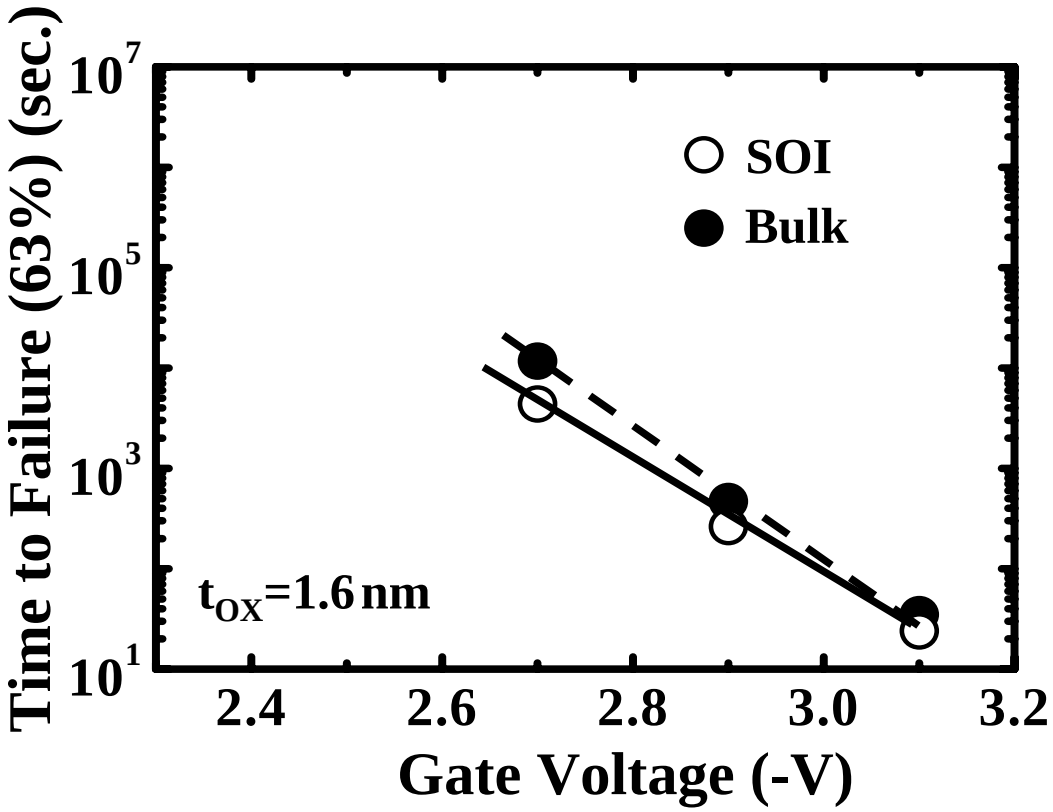

Fig.5.11 t_{fail} (63%) vs. gate stress bias for SOI and bulk pMOS devices.

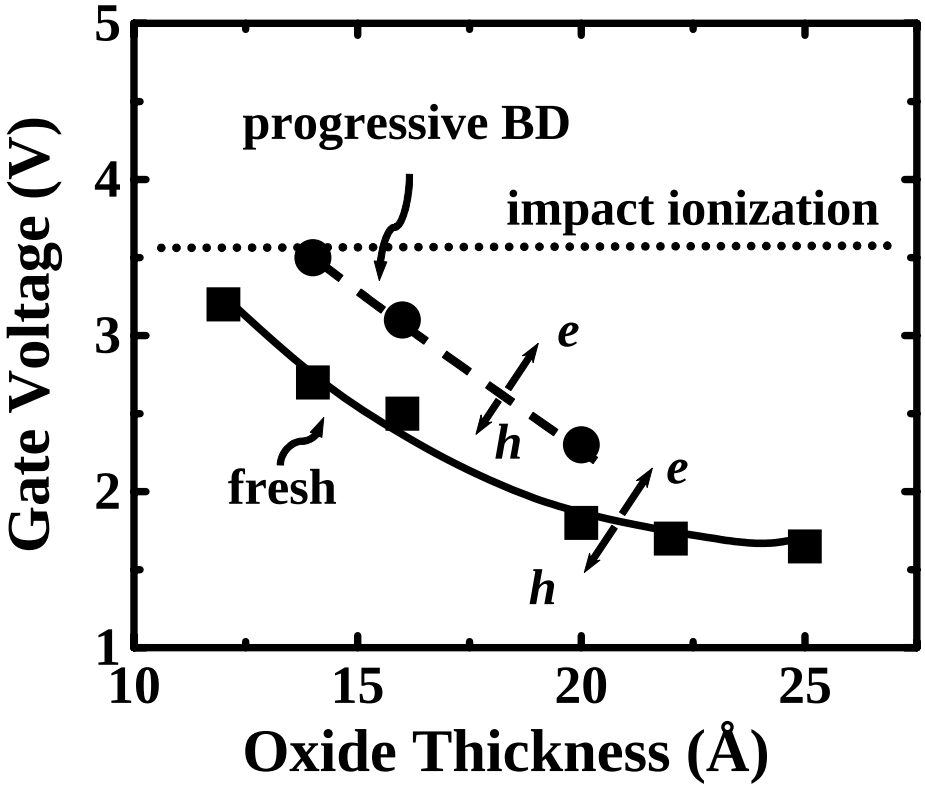

Fig.5.12 The range of oxide thickness and stress gate voltage where the hole current component is dominant in a fresh device and after breakdown. *h* or *e* represents hole current or electron current dominant regime, respectively.

Chapter 6
Conclusions

In short, this dissertation has discussed major SBD induced reliability issues in SOI CMOS with gate oxide in direct tunneling domain, among them the V_t hysteresis effects, excess low frequency noise, and breakdown hardness. Major contributions of each subject in this work are summarized as follows.

First, we have calculated the gate tunneling leakage current in ultra-thin oxide MOSFETs. Two charge transport modes attributed to gate tunneling current is proposed. The gate tunneling current includes both source/drain tunneling current and substrate tunneling current. A quantum charge transport mechanism is developed to study the I_{sd} of the inversed carrier tunneling processes, and a classical charge transport mechanism is built to explore the I_b of the valance band electron tunneling processes. In addition, the combined Poisson and Schrodinger equations are solved self-consistently to simulate the accurate oxide electric field. The C-V curve of ultra-thin gate oxide capacitance also can be calculated from the simulated results. The measured C-V and I-V of ultra-thin oxide can be fitted well by our proposed models.

Next, we reported the impact of breakdown position on hysteresis effects for ultra-thin oxide PD SOI MOSFETs. The excess substrate tunneling current of SBD PD SOI devices will modulate the substrate bias in specific operation conditions. As input signal is switching, the hysteresis effect of c-SBD PD SOI devices is enhanced. The dominant floating-body charging mechanism is valance band tunneling due to applied gate voltage. While output signal is changing, the hysteresis effect of e-SBD PD SOI devices is aggravated. The dominant floating-body charging mechanism is band-to-band tunneling when drain bias is large. Two SBD enhanced hysteresis modes in off-state CMOS have been evaluated and would be a serious reliability concern in ultra-thin oxide PD SOI circuits.

Then, the significance of soft breakdown position to the low frequency drain current noise in PD SOI nMOS devices has been identified. In high gate bias, the excess floating body noise would be enhanced if a breakdown path occurs at the channel. Large substrate leakage current of valance band electron tunneling in c-SBD not only affects the V_t hysteresis effect but also generates excess low frequency drain current noise source. This noise source correlates with the amplification by small white noise of substrate tunneling currents. The c-SBD enhanced excess noise would become an important reliability subject in ultra-thin oxide analog SOI devices.

Finally, in ultra-thin oxide pMOS, hole current instead of electron current is found to dominate breakdown progression. Enhanced breakdown hardness is observed with floating body. The enhanced breakdown evolution can be explained by the heating of channel holes and thus increased hole stress current during breakdown progression. The temperature rise of channel holes after oxide breakdown is caused by the valance electron tunneling through the BD path and the following electron-hole energy transfer process. Higher carrier temperature can produce a larger substrate bias effect on hole tunneling current by thermal excitation of holes into higher sub-bands. Numerical analysis of substrate bias effect on hole tunneling current is performed to support the proposed theory. The floating-body enhanced BD progression has large impact on the failure time of ultra-thin oxide SOI pMOS devices. All of these findings make SBD not just increase the tunneling leakage current but become a challenge of reliability issues in ultra-thin oxide PD SOI MOSFETs.

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Investigation of Soft Breakdown Induced Reliability Issues in Ultra-Thin Oxide SOI Devices

Publication Lists

(a) Journal Papers

(1) C. W. Tsai, M. C. Chen, S. H. Gu and T. Wang, “Auger recombination enhanced hot carrier degradation in nMOSFETs with a forward substrate bias,” in *IEEE Trans. Electron Devices (TED)*, pp. 1022-1026, 2003.

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五、著作總點數： 7 (依新法記點)