Chapter 1

Introduction

1.1 General Background

With the trend of scaling down for integrated circuits, the linewidth and spacing between metal interconnections become smaller. Moreover, the length of interconnection lines will increase due to the larger chip size, which is the result of getting profitable and excellent IC performances. Therefore, a larger part of the total circuit propagation delay (RC delay) is contributed more from the characteristics of the interconnections than that of the scaling of devices [1-3] (Fig. 1-1). In the medium 1990's, the National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials to meet the projected overall technology requirements [4]. Thereafter, there were many new interconnect materials and structures extensively studied in the industrial and academic committees [5-8]. However, when the dimensions are scaled below 100 nm beyond 2004, the back-ended-of-line (BEOL) interconnection (Fig. 1-2) will become more complexity and functionality. As a result, this will cause more integration challenges such as the packing density, reliability, and manufacture compatibility, etc. [9].

In addition, the dimension scaling of interconnection will lead to the fact that not only does the propagation RC delay increase, but also does the power consumption and cross-talk noise between metal signal lines arise [10-12]. In order to understand these issues, we assuming that the minimum metal pitch equaling twice the metal width and the dielectric thickness is the same as that of the metal line in between (Fig.

1-3). In a simple first-order model, time delay τ and power consumption P can be estimated by the following equations:

$$\tau = RC = 2\rho\varepsilon\left(\frac{L_m^2}{W^2} + \frac{L_m^2}{t_m^2}\right) \quad (1)$$

$$P \propto 2\pi f V^2 \varepsilon \tan(\delta) \propto 2\pi f V^2 C \quad (2)$$

where

$$R = \rho \frac{L_m}{W\ t_m}, \quad C = 2(C_L + C_v) = 2\varepsilon\left(\frac{L_m t_m}{W} + \frac{L_m W}{t_m}\right)$$

in which ρ is the resistivity, Lm is the interconnect line length, W is the line width, ε is the permittivity, tm is the thickness of the metal, f, V and tanδ are frequency, applied voltage and dielectric low, respectively. Therefore, since the RC delay and power consumption issues is unlikely to be resolved by changing interconnection geometry, the most effective approach is to introduce low-dielectric constant (low-k) and low-resistivity materials into the interconnect architecture.

For the low-resistivity materials, Cu conductive metal has been recognized to apply to 130 nm technology node and beyond due to its low resistivity (1.67 μΩ-cm for bulk materials) and high electromigration resistance [13-17]. Moreover, using Cu as the conductive metal instead of traditional Al interconnections can effectively reduce the number of metal levels in ultra-large-scale-integrated (ULSI) circuits [18-20]. Although the copper interconnections can improve the ICs performance by fewer metal levels and its excellent intrinsic properties, the introduction of low-k dielectrics is essential to obtain more advanced circuits on chip [21-22]. Thus, the investigation of low-k materials on its physical, chemical and electrical properties is very important for the progress of semiconductor technology. In order to correspond with the IC fabrication demands, the requirement of low-k materials are summarized in Table 1-1. Generally, the permittivity of low-k materials is contributed by electronic (frequency $\geq 10^{15}$), atomic (frequency $\leq 10^{13}$) and permanent dipolar (frequency $\leq 10^{9}$) within the

materials. These contributions can be evaluated by spectroscopic ellipsometry, infrared spectroscopy and C-V measurement with 100 Hz to 1 MHz [23-24]. In light of the degree of polarization in films will significantly affect the dielectric constant of materials, lower polarization of materials can cause lower dielectric constant. For instance, some organic polymers consist of symmetrical molecular structure, which has a small dipole polarization, resulting in a lower dielectric constant [25-26].

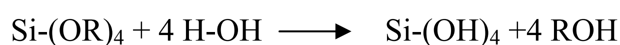
There are two principal methods to form low-k films. One is the chemical vapor deposition (CVD), and the other is the Spin-on deposition (SOD). The conventional IMD material was CVD deposited oxide whose dielectric constant is about 3.9. In order to reduce the dielectric constant of SiO_2 film, semiconductor industries have adopted the fluorinated oxide (FSG) as the IMD dielectrics [27-28]. Moreover, it is easily compatible to the standard semiconductor processes. Although relatively minor in variation from silicon dioxide, there are issues of fluorine mobility, reactivity with refractory barrier layers, adhesion and moisture sensitivity required to develop a truly robust process [29]. In addition to FSG film, several low-k ($k < 3.0$) materials can be deposited by CVD technique such as fluorinated amorphous carbon, parylenes and diamond-like carbon, etc. [30-32].

The other technique of forming low-k materials is spin-on deposition (SOD). This method is using a liquid precursor deposited on a wafer by spin-coating method. Then, the as-spun wafer is subjected to a series of baking. Finally, a furnace curing is performed to achieve the network low-k structure. In general, most of SOD low-k materials can be divided into two categories. One is organic polymer, and the other one is inorganic silica-based materials. There have been many organic polymers, such as fluorinated polyimide (FPI), poly arylene ether (PAE), benzocyclobutene (BCB), and aromatic polyether polymers, including FLARE and SiLK, extensively developed by materials venders [33-37]. Although so many organic materials were proposed for

IMD dielectric, most of them were not available due to low-thermal stability, softness, and incompatible with SiO_2-based technology. Therefore, it is believed that the integration of organic polymers still have large challenges for interconnect application. Besides, inorganic silica-based materials have also been developed widely. These materials include Hydeogen Silsesquioxane (HSQ), Methysilsesquioxane (MSQ), Hybrid-Organic-Siloxane-Polymer (HOSP), and Methysilsesquiazane (MSZ), etc. [38-41]. This type of low-k materials possesses the features of good gap filling, local planarization and low dielectric constant. Furthermore, their low-k properties can be achieved if the density of functional groups (such as Si-H, Si-R, etc) can be maintained in high level [42].

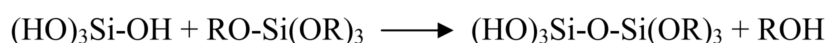
In addition, for the sake of conforming to the requirement of higher performance ICs in future, ultra low dielectric constant materials (k<2.2) will need to be investigated extensively. The dielectric constant below 2.2 can be achieved by incorporation of voids within the matrix materials [43-44]. Generally, there are two approaches to form ultra low-k materials, which is sol-gel and nanoform processes. As for sol-gel method [45-47], a liquid solution consisting of colloidal particle, which is called as “sol”, is spun on the substrate. Then, a wet-gel film can be achieved by an aging process. The aging process can be achieved through hydrolysis and poly-condensation reactions, which is described as follows:

Hydrolysis:

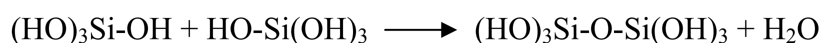


$$Si\text{-}(OR)_4 + 4\ H\text{-}OH \longrightarrow Si\text{-}(OH)_4 + 4\ ROH$$

Poly-condensation:



$$(HO)_3Si\text{-}OH + RO\text{-}Si(OR)_3 \longrightarrow (HO)_3Si\text{-}O\text{-}Si(OR)_3 + ROH$$



$$(HO)_3Si\text{-}OH + HO\text{-}Si(OH)_3 \longrightarrow (HO)_3Si\text{-}O\text{-}Si(OH)_3 + H_2O$$

Then, the residual liquid in film can be removed by either supercritical drying or thermal evaporation. The material formed by the former method is termed “aerogel”

[48] and by the latter one is called as “xerogel” [49]. Generally, the pore structure of porous low-k material formed by sol-gel method will be affected by three factors: (1) the size and structure of primary polymer in the condensation process, (2) the organization of these polymers, and (3) the type of gel drying method. In addition, porous low-k materials can also be synthesized by nanofoam process [50]. This process is to form a nano-porous material by utilizing a block copolymer precursor which consists of thermally stable matrix and thermally labile blocks. After suitable thermal anneal, the labile blocks will decompose, leaving pores in the matrix (Fig. 1-4). Therefore, the porous low-k materials can be achieved by this method. However, it is noted that the content of labile blocks should be controlled below 30 % otherwise the collapsed structure would take place [51-52]. There are some basic properties of several low-k materials listed in Table 1-2.

Although the low-k materials have been developed for about 10 years up to now, there are still a lot of problems with the properties or integration of new low-k materials. Especially, after Cu conductive metal was introduced into IC fabrication in the late 1990s, integration and reliability issues between Cu and low-k materials persecute semiconductor industries throughout. These issues include (1) thermally and mechanical induced cracking and adhesion loss, (2) poor mechanical strength, (3) moisture absorption, (4) time-dependent behavior, (5) chemical interaction (e. g. PR removal, etch/clean and deposition), (6) low-electrical breakdown, (7) poor thermal conductivity, and so on [53]. These challenges have made the implementation of low-k inter-level dielectric (ILD) materials delay beyond 2004 (Table1-3). According to the long-term MPU interconnect technology of International Technology Roadmap for Semiconductors (ITRS) in 2003 [54], the introduction of ultra low-k materials (k<2.2) even delay to 2013 (Table1-4). For such a reason, more effort of technology developing on the integration between Cu and new low-k materials should be kept in

mind for relative persons of advanced IC fabrication.

In order to integrate Cu and low-k materials into nano technology (<100nm) regime to meet the requirement of future IC products, the nurture of global planarization process and next generation lithography is significantly important among many integration challenges on Cu interconnect technology. Moreover, the damascene structure is the only method to realize the Cu interconnection due to the difficulty on Cu etching process through dry etching technology during Cu metallization. However, many low-k materials were subjected to chemical mechanical polishing (CMP) issues (such as degradation of low-k properties after CMP, dielectric peeling in damascene structure after CMP, and so on) during fabrication of damascene structure [55]. In addition, many literatures have indicated that the properties of low-k materials are easily damaged during the photoresist stripping process [39, 56]. Therefore, in this dissertation, I will investigate the impact of CMP process on the dielectric properties of various low-k materials. Besides, a novel technology, the electron beam (e-beam) direct patterning method to form damascene structure, is also proposed to avoid the retrogression of low-k dielectrics during photoresist stripping process.

1.1.1 The impact of CMP process on the low-k materials

Recently, planarization has become an inevitable step for interconnect technology. Two main reasons for the requirement of palanrization are lithography limitation and step coverage improvement. For the lithography limitation, depth of focus (DOF) is one significant factor to affect the pattern resolution. In addition, unplaned surface will result in step coverage issues of metal thinning on sidewall of via, which cause the reliability problems. Among many planarization technologies,

chemical mechanical polishing (CMP) is the only one process to achieve global planarization [57]. This process combines chemical reaction and mechanical interaction between CMP slurry and polished materials. Besides, Cu CMP process is the most critical technology for Cu damascene interconnection. This is attributed to the difficulty of Cu etching process through dry etching technology. Moreover, the process of damascene structure is simpler and more cost down than that of traditional subtractive Al structure [58] (Figure 1-5). In the middle 1980s, the corporation IBM firstly developed the dielectric CMP planarization technology. When reaching middle 1990s, the CMP process has replaced the reactive ionic etching (RIE) etch-back technology for planarization process such as poly-Si etch-back process during DRAM fabrication, inter metal dielectric (IMD) CMP, and tungsten plug etch-back process etc. The requirement of Cu damascene interconnection for advanced ICs has made the development of Cu CMP process more important in late 1990s. Therefore, the impact of CMP on advanced interconnection of IC should be investigated extensively for semiconductor technology. During the manufacture of IC products, metal CMP and dielectric CMP steps are two main functions of CMP technology. The polishing mechanism of oxide is the formation of Si-O-Si bonds between abrasive and film due to the hydration reaction [59]. Then, the molecular bonding is removed by mechanical polishing. On the other hand, the polishing mechanism of metal is using oxidant in slurry to oxidize the surface of metal, and then removing the oxidized layer by mechanical polishing [60]. In order to achieve the requirement of smooth planarization surface, high polishing rate, excellent polishing uniformity, and successful integration of Cu and low-k materials into multilevel interconnection, a number of studies have been investigated by many experts in the world. For example, the suitable control of abrasive size and pH value of slurry in hard pad can result in smooth planarization surface of interlayer dielectric [61]. High Cu removal rate can

be attained by utilizing low down-force pressure, abrasive-free slurry and orbital CMP equipment [62]. The using of dummy pattern in wafer was proposed to avoid the issues of dishing and erosion of polished material which result in the problems of open circuit in interconnection. As for the integration of Cu and low-k materials, several reports indicated that two steps of Cu CMP methodology would be a good alternative for the fabrication of Cu/ultra-low-k materials damascene structure [62-63]. This process can be described below. Firstly, High selectivity Cu slurry is used to remove most Cu layer. Then, the barrier metal is removed by using low selectivity barrier slurry sequentially. Although many relative studies have been focused on the improvement of topography planarization of interconnect layers, little attention has been given on the electrical properties of post-polished films. As a result of the electrical properties of polished layers significantly affecting the performance of interconnection, more efforts should be made on this field. In addition, according to the description of ITRS roadmap, low thermal budget is the trend of ICs fabrication, especially for the deposition of pre-metal dielectric (PMD) [54]. Furthermore, as the scale of device continues to shrink below 65 nm, the planarization of PMD becomes more important for lithography. Based on the above two reason, the CMP process of PMD dielectric will be one of chief technologies for fabrication of future IC products. Moreover, in order to reduce the cross talk of local interconnection of device, the introduction of low-k materials into PMD would be possible in the future. Therefore, the CMP of low-k materials as a PMD layer would be a critical process for IC production in future (Figure 1-6). In addition, in virtue of the difficulty of end-point detection during CMP processes, the IMD materials would be subjected to over polishing. This will probably affect the dielectric properties of IMD. Therefore, in this dissertation, the characteristics of various low-k materials after CMP process were investigated in detail.

1.1.2 Electron beam direct patterning technology on low-k materials

In the early 1970s, the optical lithography technology has been used to manufacture integrated circuits. To date, this technology has made the progress of ICs follow the Moore's law for over thirties years. However, beyond the 2003, lithography technologies are confronted with two set of challenges. The first is a consequence of the difficulties inherent in extending optical lithography to physical limits. The second is the need to develop entirely new, next general lithography (NGL) technologies to be capable of applied to ICs fabrication. According to the potential solution of lithography of ITRS roadmap [54] (figure 1-7), optical lithography is expected to be the dominate technology through the 65 nm node. The NGL technology possibly appears at the 45 nm node, although it is more likely later. In the leading semiconductor fabrication, the ArF excimer laser (193 nm) lithography has replaced the KrF excimer laser (248 nm) lithography as the exposure source for critical patterning. Significant improvements in 193 nm resists and masks are still needed for future applications, and the F2 gaseous laser (157 nm) lithography is still in early development. However, for the sake of resolving the difficult of the wavelength scaling down of optical light source, many NGL technologies must be explored right now. These technologies include extremely ultraviolet (EUV) lithography, X-ray lithography, ion-beam lithography, immersion lithography, and electron-beam (e-beam) lithography etc. [64-67]. Among these NGL technologies, there are some advantages and disadvantages for the application in manufacture. The EUV lithography is an electromagnetic radiation wave with 1~50 nm wavelength. The possible source is plasma radiation of laser-excited xenon gas. The wavelength of EUV is too short so that no transmissible lens is available. For such a reason, its

lithography system is mirror system. But this system is very complex. The X-ray lithography has been investigated in 1972 [68]. However, its difficulties for IC lithography application are due to the difficult of fabrication of small size mask with 1:1 ratio and a strenuous, stable, parallel, and single frequency X-ray source. The ion-beam lithography is primarily used to modify masks and detect and repair the defect of device. Of course, the low throughput and the fabrication difficult of mask are fatal wound of this lithography. The immersion lithography has attracted much attention among many semiconductor industries recently. This technology can make the wavelength of traditional optical (193 nm) achieve 134 nm by using water medium between optical light and wafer. But it still has some issues needed to be overcome. As for e-beam lithography, it has been used to make mask for many years. The e-beam lithography has been investigated for the production of ICs up to now. However, the major problem of e-beam lithography for ICs production is its low throughput. Nevertheless, a number of improvements on throughput of e-beam lithography were proposed by academic and industrial societies. For example, electron projection lithography (EPL) [69], multi-parallel beam lithography [70], digital electrostatically focused e-beam array direct-write lithography (DEAL) [71] and scattering with angular limitation projection electron-beam lithography (SCALPEL) [72] etc. are all promised technologies to raise the throughput of e-beam lithography. On the other hand, in order to reduce the RC delay of interconnection resulting from the consecutive scaling-down on device, the integration of Cu and low-k materials is an inevitable trend in ICs manufacture. Moreover, the damascene structure is the only architecture for Cu interconnection. However, low-k materials have been reported to be easily degraded during photoresist stripping processes for the fabrication of damascene structure (Figure 1-8). In addition, some literatures have reported that several low-k materials were sensitive to e-beam exposure [73-74].

Based on the above-mentioned reasons, we propose a novel direct patterning technology on low-k materials with e-beam exposure for the fabrication of damascene structure. The procedure of e-beam direct patterning on low-k materials is illustrated in figure 1-9. This technology can not only avoid the damage of low-k materials during photoresist ashing but also simplify the fabrication steps of damascene structure. Besides, the impact of e-beam exposure on the dielectric properties of low-k materials was also investigated in detail in this dissertation so that this technology can be applied to the fabrication of interconnection in future.

1.2 Organization of the dissertation

This dissertation is divided into six chapters. The contents in each chapter are described as follows.

In chapter 1, general background of the application of low-k materials on interconnection is introduced. In addition, the integration issues such as the impact of CMP and photoresist stripping processes on low-k materials are also introduced. Finally, an e-beam direct pattering on low-k materials is proposed.

In chapter 2, the intrinsic properties of low-k Methylsilsesquiazane (MSZ) and the impact of CMP process on MSZ for interconnect applications are investigated. In addition, a new method of improving the polishing rate of low-k MSZ with oxygen plasma treatment is also demonstrated in this chapter.

In chapter 3, the intrinsic properties of ultra low-k material porous-polysilazane (PPSZ) and the effect of CMP on PPSZ are studied. Also, the effect of oxygen plasma treatment on CMP process for PPSZ is also evaluated.

In chapter 4, a novel electron-beam (e-beam) direct patterning on inorganic low-k

HSQ for interconnect application is evaluated. The dielectric properties of e-beam exposed HSQ are also present in this chapter.

In chapter 5, the feasibility of electron-beam direct patterning on organic dense low-k MSZ for interconnect application is investigated.

In chapter 6, the effect of electron beam curing on organic ultra low-k porous organosilicate glass (POSG) material is also presented in this chapter.

Finally, the summarization of all experimental results in this dissertation and the suggestions for the future work are presented in chapter 7.