**Table 1-1 The requirements for low-k dielectrics**

| Requirements for Low-K Dielectrics | |
|---|---|
| **Film Properties**<br><br>1. Dielectric Constant:<br>~ Bulk: k = 2.7 or below<br>~ Effective: k=3.1~3.6<br>~ Extendible to k < 2.4<br>2. Thermal/Dimensional Stability:<br>~ Tg > 400°C<br>~ Decomposition temperature > 450 °C<br>~ Useable temperature > 400 °C<br>~ CTE: 20~70 ppm<br>3. Electrical Properties:<br>~ Leakage current density: $10^{-9}$~$10^{-8}$ A/cm$^2$ at 1 MV/cm<br>~ Breakdown field: 2~5 MV/cm<br>~ Dissipation factor: < 0.01<br>~ Low fix charge<br>4. Film Composition:<br>~ Compatible with Cu metallization materials<br>~ Oxide like film composition<br>~ Low film stress<br>~ >2 μm thick cracking threshold | **Integration Compatibility**<br><br>5. Adhesion:<br>Good adhesion to various metallization and dielectric materials before and after integration,<br>i.e. etch & CMP<br>6. Structure Rigidity:<br>Ability to build > 10 level structures<br>No impact on electromigration<br>7. Moisture Absorption/Permeation:<br>No moisture uptake<br>8. $O_2$ Ash/Solvent Resistance:<br>Compatible with conventional post etch and resist removal processes<br><br>**ESH/Manufacture ability**<br><br>9 . Safety/Green technology<br>10. cost of ownership (COO) stand alone/integrated<br>11. Non Proprietary Chemical<br>12. Particles/Contamination |

*(Ref: Semiconductor International Association)*

## Table 1-2 Basic intrinsic properties of several low-k materials.

| Dielectric | Dielectric constant | Deposition technology | Glass transition temperature ($^oC$) | Refractive index | Stress (Mpa) Pa=N/$m^2$ | Gap filling (um) | Cure temperature ($^oC$) |
|---|---|---|---|---|---|---|---|
| FSG (silicon oxyfluoride) | 3.4~4.1 | CVD | >800 | 1.42 | 130 | <0.35 | No issue |
| Parylene-AF4 (aliphatic tetrafluorinated poly-p-xylyene) | 2.5 | CVD | Tmelt >510 | 1.548ΔRI > 0.09 (ai) | 100 | 0.18 | 420~450 |
| Fluorinated amorphous Carbon (a-F:C) | 2.0~2.6 | CVD | - | 1.49~1.39 | 5~45 | <0.35 | - |
| Diamondlike Carbon | 2.4~2.8 | CVD | - | 1.6~1.75 | 2-10 | <0.18 | - |
| Polyimides | 3.2~3.6 | SOD | >350 | ΔRI > 0.22 (ai) | - | - | - |
| Hybrid-Silsesquioxanes | <3 | SOD | Tmelt > 250 | 1.58 | 30~40 | <0.1 | 450 |
| HSQ (hydrogen silsesquioxane) | 2.9 | SOD | >500 | 1.37 | 70~80 | <0.1 | 350~450 |
| MSQ(Methyl-silsesquioxane) | 2.5~2.7 | SOD | >500 | 1.36 | 60~70 | <0.1 | 400~450 |
| Fluorinated Polyimides | 2.6~2.9 | SOD | >400 | ΔRI > 0.15 (ai) | 2 | <0.5 | 350 |
| Poly(arylene)ethers | 2.4~3.0 | SOD | 290 | - | - | - | 425 |
| Aromatic hydrocarbon | 2.65 | SOD | >490 | 1.628 | 55~60 | <0.05 | 400~450 |
| Bisbenzo(cyclobutene) BCB | 2.6~2.8 | SOD | Tdec > 350 | - | 85 | <1 | 250 |
| Fluorinated Poly(arylene)ethers | 2.4~2.7 | SOD | 175~265 | - | 30~50 | 0.1~0.8 | 450 |
| PTFE (polytetrafluoro-ethylene) | 1.9 | SOD | Tdec > 250~300 | 1.34 | 25~27 | <0.3 | 360~390 |
| Nanoporous Silica | 1.3~2.5 | SOD | >500 | 1.15 | 0 | <0.25 | 400 |
| Xerogels/Aerogels | 1.1~2.5 | SOD | N/A | - | - | 0.1 | 300~400 |

**Table 1-3 MPU interconnect technology requirements –Near-term**

| Year of production | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 |
|---|---|---|---|---|---|---|---|
| DRAM 1/2 Pitch (nm) | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| MPU/ASIC 1/2 Pitch (nm) | 120 | 107 | 95 | 85 | 76 | 67 | 60 |
| MPU Printed Gate Length (nm) | 65 | 53 | 45 | 40 | 35 | 32 | 28 |
| MPU Physical Gate Length (nm | 45 | 37 | 32 | 28 | 25 | 22 | 20 |
| Number of metal levels (minimum) | 9 | 10 | 11 | 11 | 11 | 12 | 12 |
| Total interconnect length ($m/cm^2$) -active wiring only, excluding global levels | 579 | 688 | 907 | 1002 | 1117 | 1401 | 1559 |
| Metal 1 wiring pitch (nm) | 240 | 214 | 190 | 170 | 152 | 134 | 120 |
| Minimum global wiring pitch (nm) | 475 | 410 | 360 | 320 | 290 | 260 | 234 |
| Interconnect RC delay (ps) for 1 mm global Line at minimum pitch | 42 | 55 | 69 | 87 | 92 | 112 | 139 |
| Conductor effective resistivity ($\mu\Omega$-cm) Cu intermediate wiring | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| Barrier/cladding thickness (for Cu global wiring) (nm) | 12 | 10 | 9 | 8 | 7 | 6 | 6 |
| Interlevel metal insulator (minimum expected)-effective dielectric constant (k) | 3.3-3.6 | 3.1-3.6 | 3.1-3.6 | 3.1-3.6 | 2.7-3.0 | 2.7-3.0 | 2.7-3.0 |
| Interlevel metal insulator(minimum expected)-bulk dielectric constant (k) | <3.0 | <2.7 | <2.7 | <2.7 | <2.4 | <2.4 | <2.4 |

(*Ref.: ITRS 2004*)

**Table 1-4 MPU interconnect technology requirements –Long-term**

| Year of production | 2010 | 2012 | 2013 | 2015 | 2016 | 2018 |
|---|---|---|---|---|---|---|
| DRAM 1/2 Pitch (nm) | 45 | 35 | 32 | 25 | 22 | 18 |
| MPU/ASIC 1/2 Pitch (nm) | 54 | 42 | 38 | 30 | 27 | 21 |
| MPU Printed Gate Length (nm) | 25 | 20 | 18 | 14 | 13 | 10 |
| MPU Physical Gate Length (nm | 18 | 14 | 13 | 10 | 9 | 7 |
| Number of metal levels (minimum) | 12 | 12 | 12 | 13 | 14 | 14 |
| Total interconnect length ($m/cm^2$) -active wiring only, excluding global levels | 1784 | 2214 | 2544 | 3544 | 4208 | 5035 |
| Metal 1 wiring pitch (nm) | 108 | 84 | 76 | 60 | 54 | 42 |
| Minimum global wiring pitch (nm) | 205 | 165 | 140 | 117 | 100 | 83 |
| Interconnect RC delay (ps) for 1 mm global Line at minimum pitch | 143 | 220 | 248 | 354 | 452 | 618 |
| Conductor effective resistivity ( $\mu\Omega$-cm) Cu intermediate wiring | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| Barrier/cladding thickness (for Cu global wiring) (nm) | 4.9 | 4 | 3.6 | 2.9 | 2.5 | 2 |
| Interlevel metal insulator (minimum expected)-effective dielectric constant (k) | 2.3-2.6 | 2.3-2.6 | 2.0-2.4 | 2.0-2.4 | <2.0 | <2.0 |
| Interlevel metal insulator(minimum expected)-bulk dielectric constant (k) | <2.1 | <2.1 | <1.9 | <1.9 | <1.7 | <1.7 |

(*Ref.: ITRS 2004*)

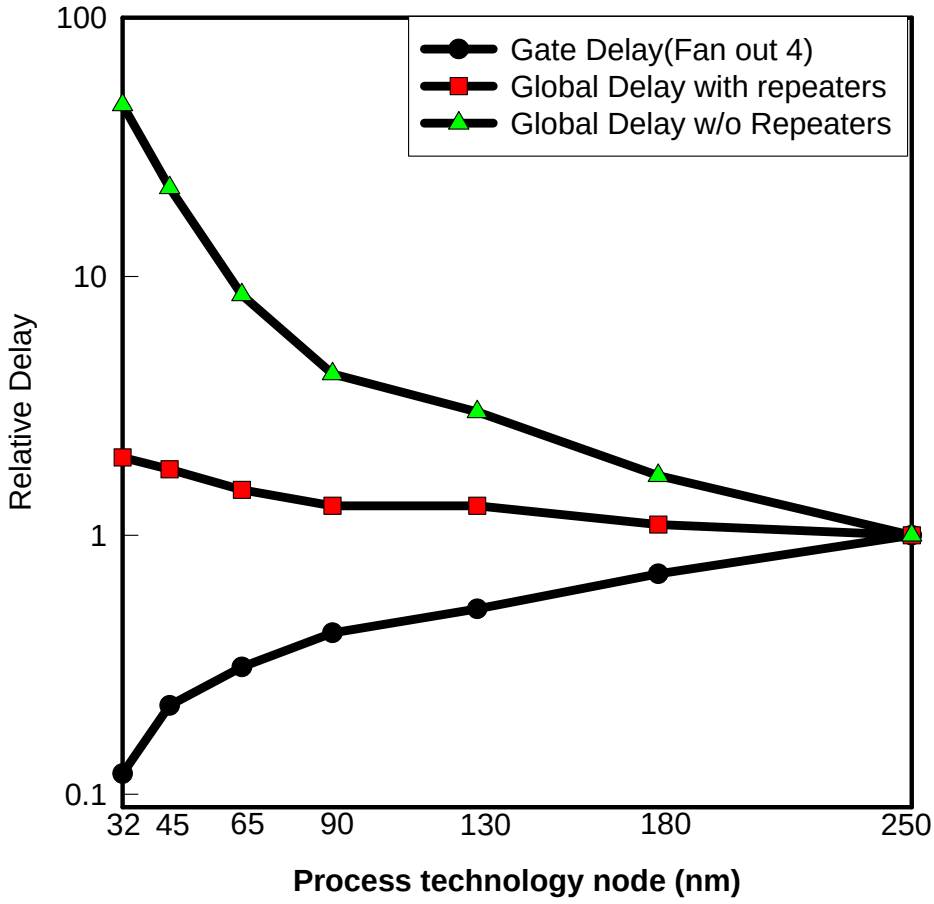
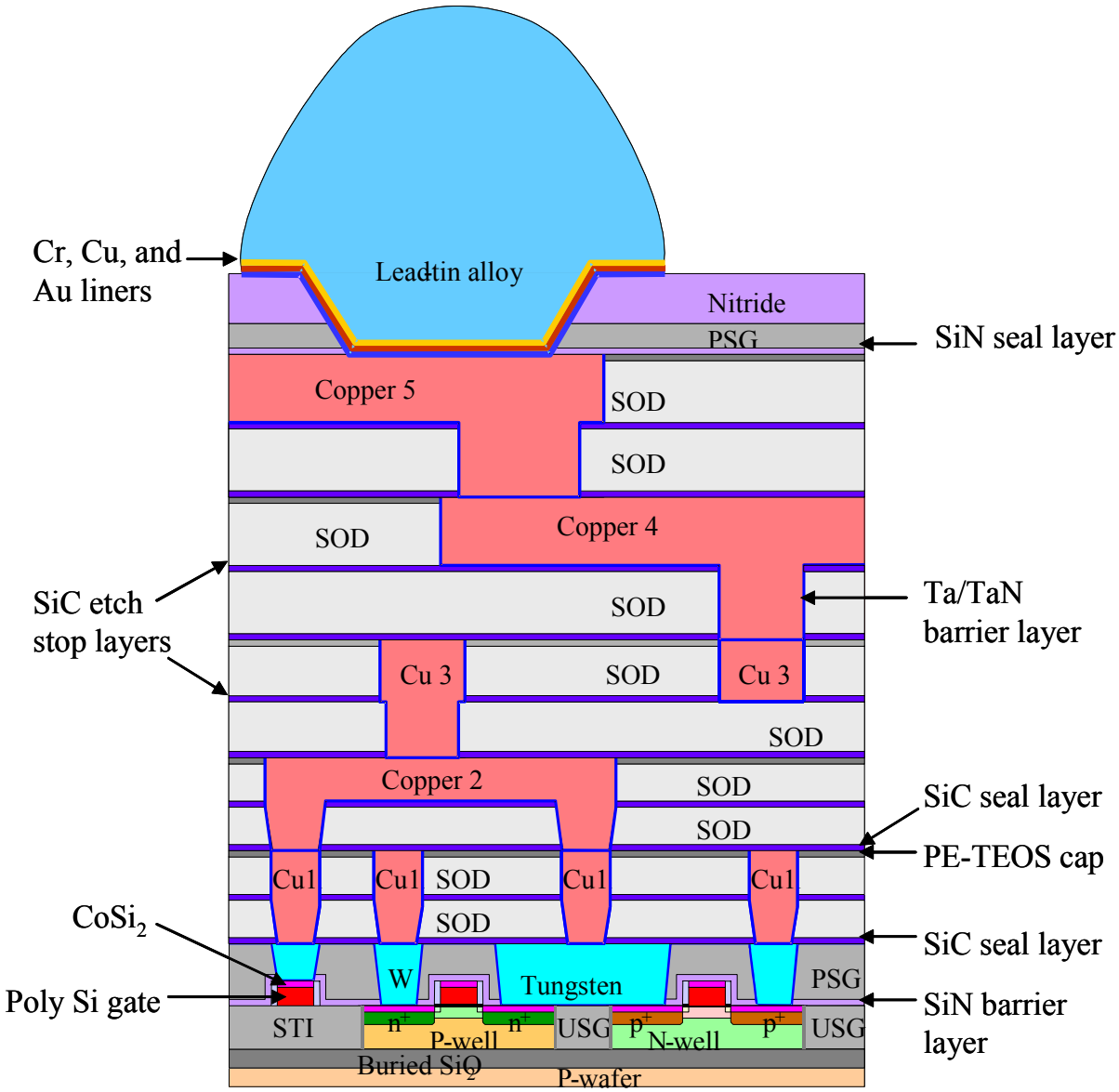



Figure 1-1 The RC delay trend of nano-scaled ULSI circuits. (Source: ITRS 2003)




*(Ref: Introduction to Semiconductor Manufacturing Technology by Hong Xiao, 2001)*

Figure 1-2 The architecture of multilevel interconnect metallization

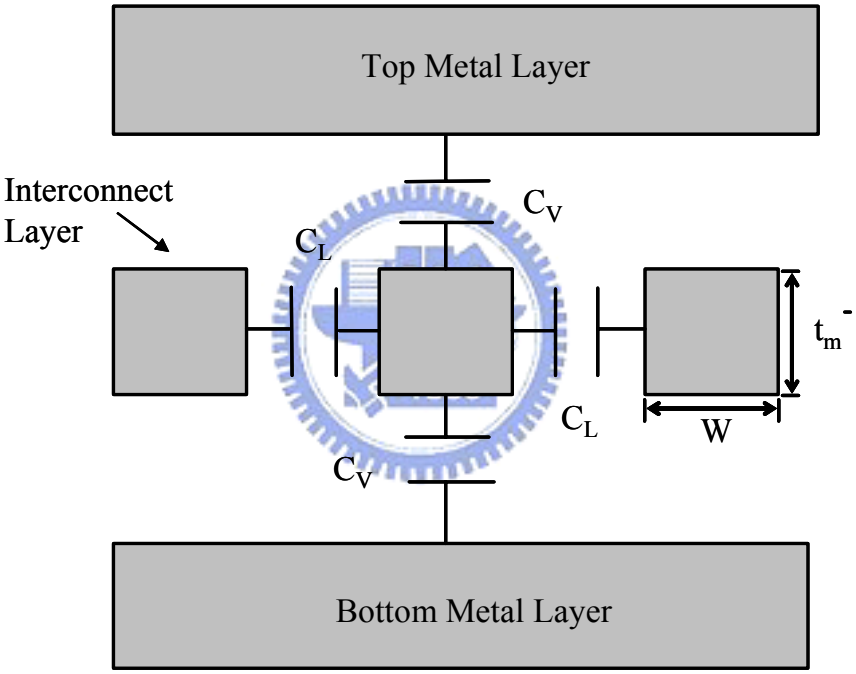



Figure 1-3 The cross-section of interconnect system with parasitic capacitance.

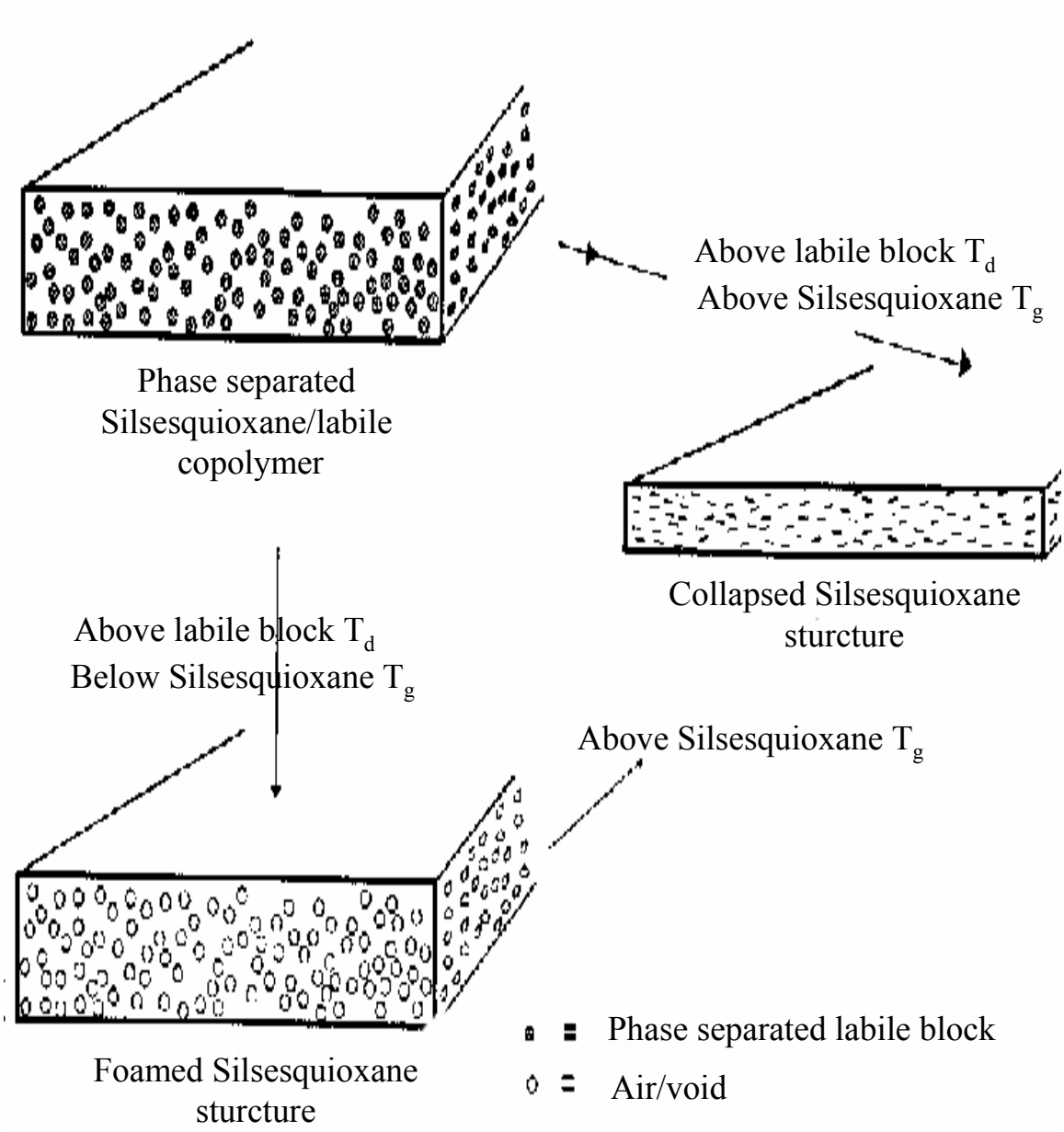



Figure 1-4 Foam Formation Process
(Source: K. R. Carter, IBM Research Division, 1997)

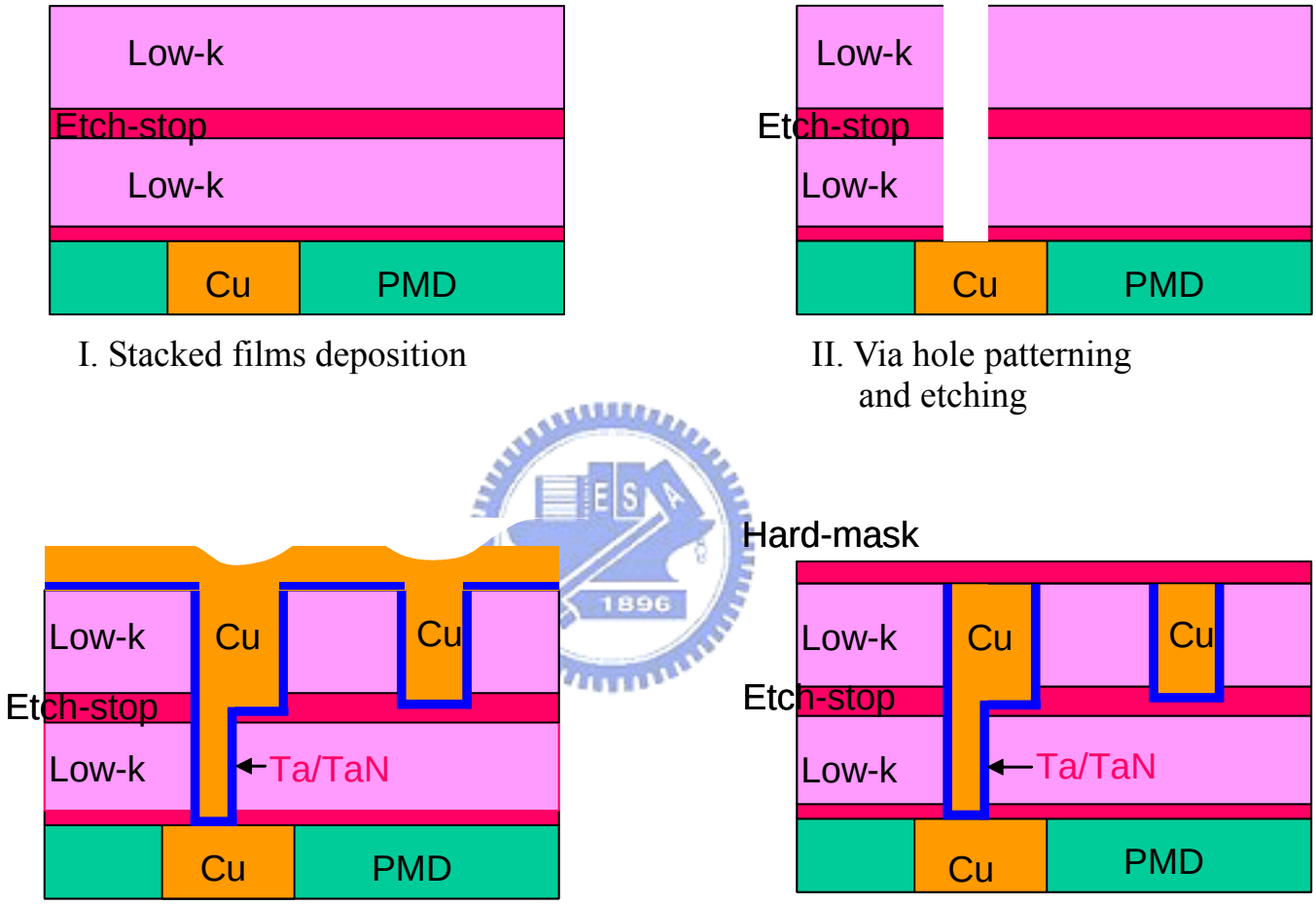



Figure 1-5 Typical process flow of Cu damascene architecture integrated with low-k material.

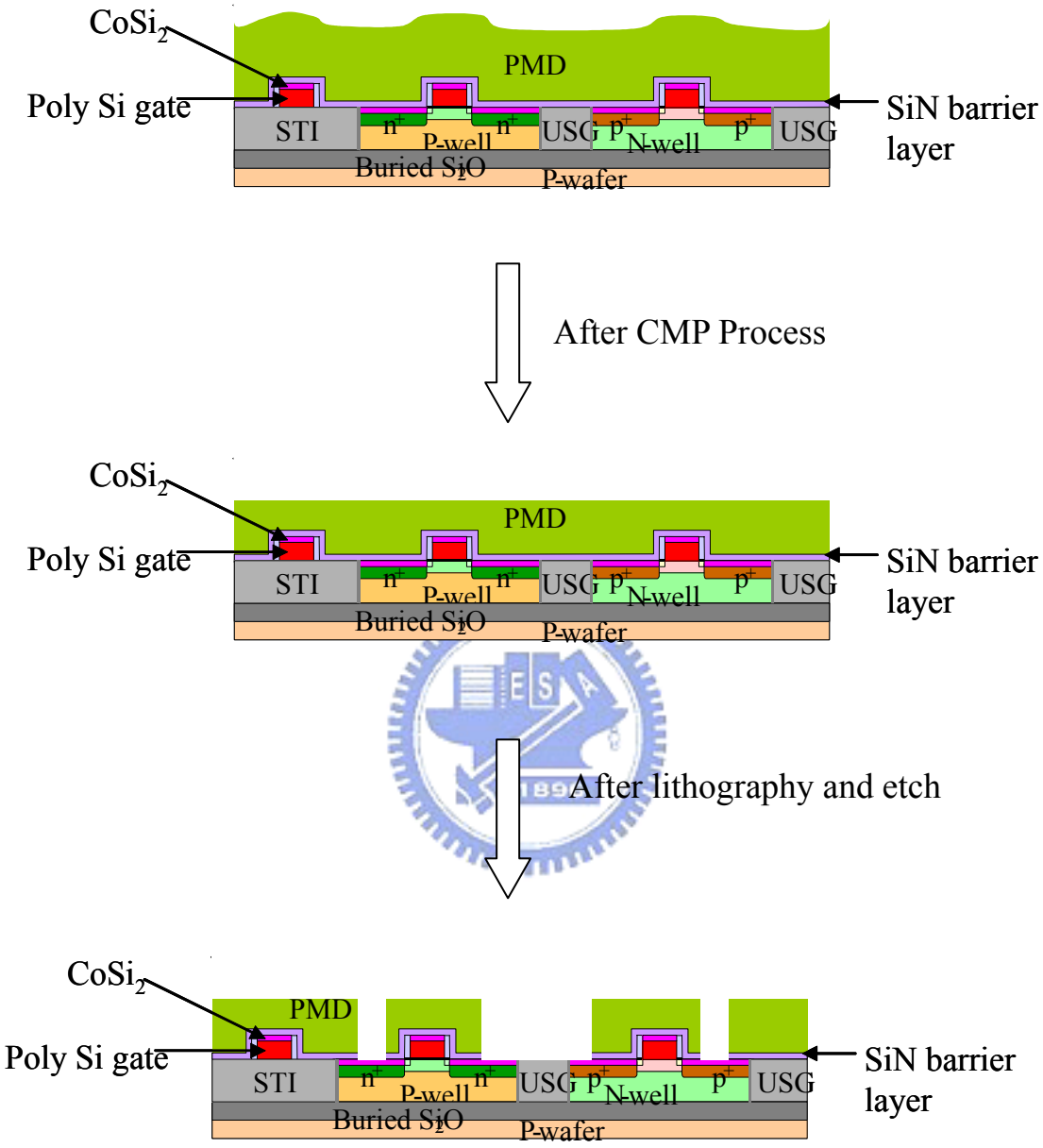
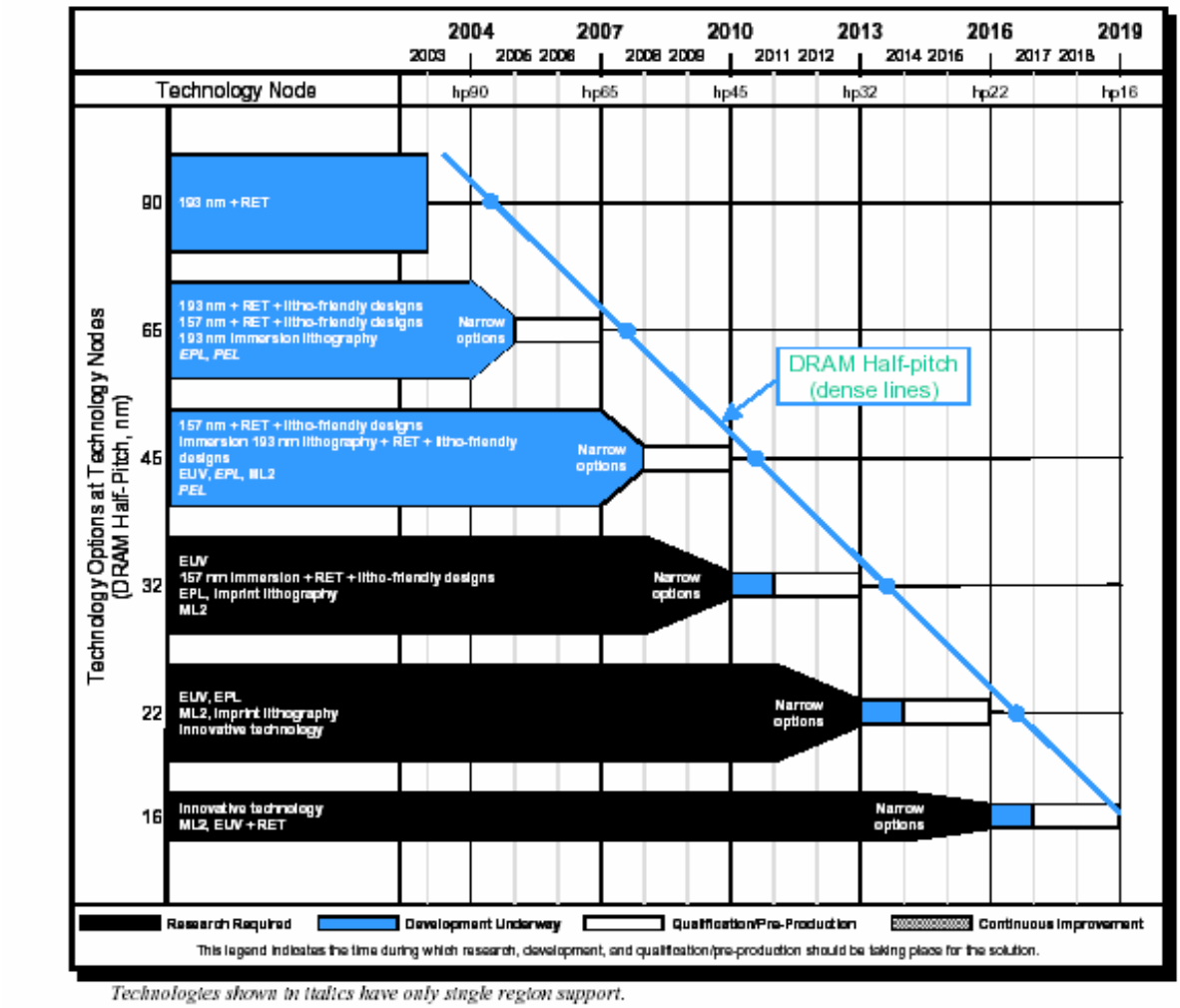



Figure 1-6 The planarization flow of PMD with CMP process




*Technologies shown in italics have only single region support.*
*RET—resolution enhancement technology EUV—extreme ultraviolet EPL—electron projection lithography*
*ML2—maskless lithography PEL—proximity electron lithography*

(*Ref.: ITRS 2003*)

Figure 1-7 Lithography Exposure Tool Potential Solutions

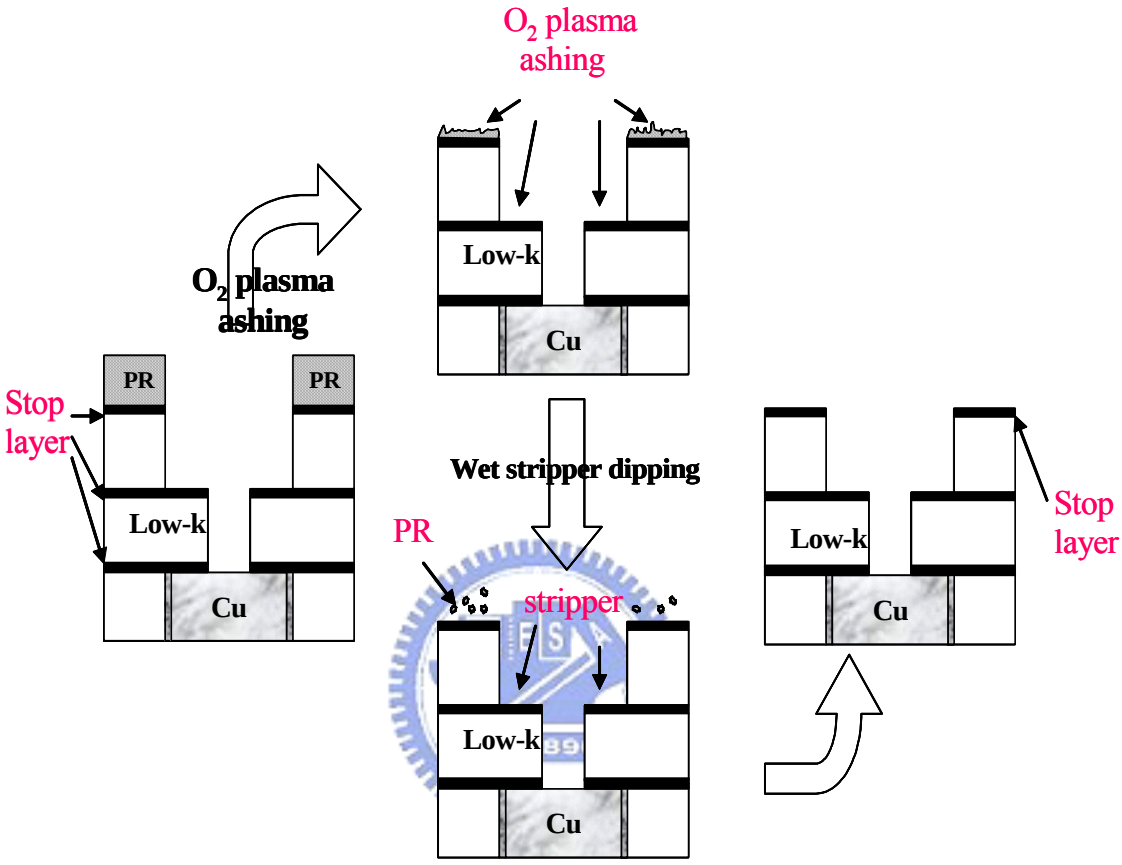



Figure 1-8 Photoresist stripping processes during the fabrication of damascene structure

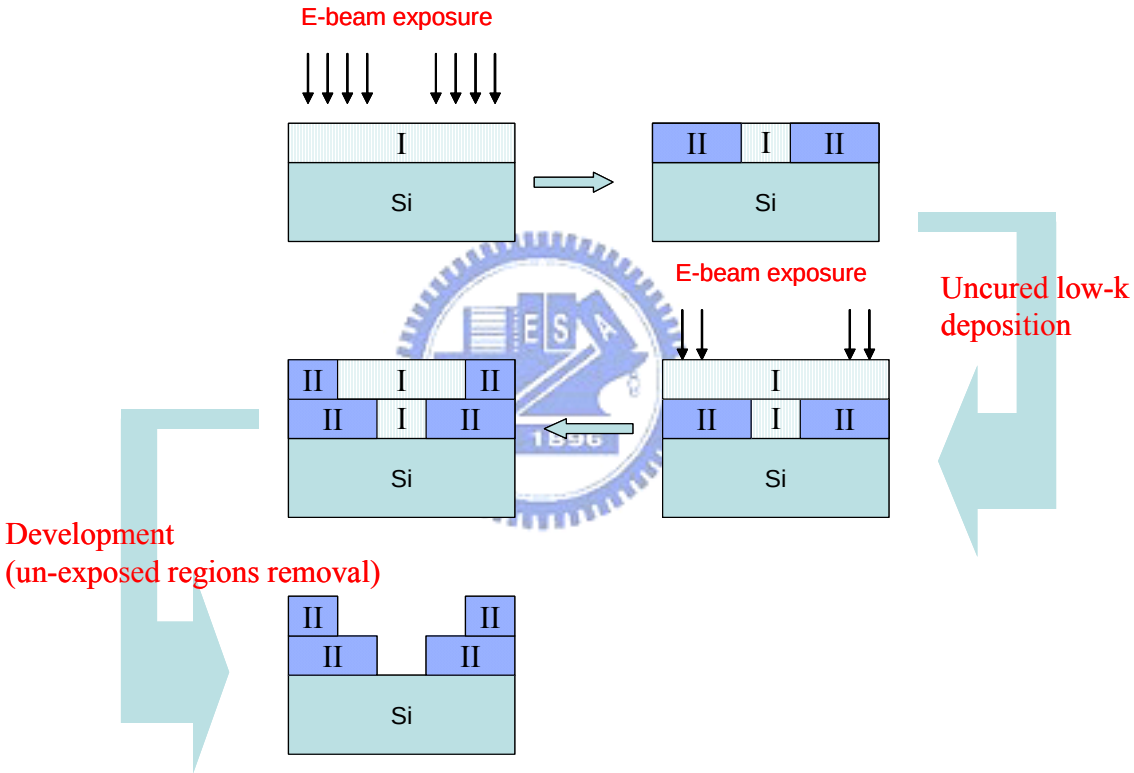



Figure 1-9 Scheme of e-beam direct patterning of low-k dielectrics for the manufacture of dual damascene structure.
Regions I are uncured low-k materials in a gel-like state and regions II are crossed-linked state after e-beam exposure.