國 立 交 通 大 學

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博 士 論 文

新穎雙功函數金屬閘極製程技術之研發

Investigation of Novel Dual Work Function Metal Gate Technologies

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摘要

本論文的研究方向，主要為研發新穎之雙功函數金屬閘極製程技術。元件尺寸的微縮雖可以改善元件之操作特性，然而傳統的多晶矽閘極本質上的缺點，對元件特性的負面影響也將更加顯著。另一方面，隨著元件尺寸的微縮，閘極氧化層的厚度變薄也將導致閘極漏電流大幅上揚，為了有效降低閘極漏電流，近年來以高介電材質取代傳統二氧化矽的相關研究也被投注大量心力。然而多晶矽閘極搭配高介電材質，已被發現會有熱穩定性不佳的缺點，同時介面也存在著費米能階夾止效應，因此，金屬閘極製程的研發不僅可以克服上述多晶矽的本質缺點，對於與高介電材質間的熱穩定性、費米能階夾止效應等方面，也提供了可能的解答。此外，金屬閘極的低阻抗，對於元件的高頻操作特性亦有改善之效。

對於金屬閘極的製程技術與材料選擇有以下幾項基本要求，首先它必須能夠在閘極介電層介面提供正確適當的功函數值，同時與閘極

介電層間需有良好的熱穩定性以確保在元件製程中可以保有穩定的特性，另外也必須可相容、整合於傳統的製程技術中。本論文中，我們提出了兩種新穎的雙功函數金屬閘極製程技術，一是利用金屬混合以形成雙元合金，二是以金屬矽化反應以形成金屬矽化物。應用了此等金屬功函數調變法後，早期被提出的雙功函數金屬閘極製程技術中，閘極介電層因金屬蝕刻導致厚度的不均勻性以及可靠度退化的現象將可被避免。在雙元合金的實驗中，我們先以同時性濺鍍的物理沈積法沈積鉿鉬雙元合金，藉以觀察其電性、化性。藉由改變各靶材的濺鍍功率可調變鉿鉬合金的組成，進而得到近乎線性且連續的功函數調變，其調變範圍可介於 3.93eV（純金屬鉿）與 4.93eV（純金屬鉬）之間。我們也發現鉿鉬合金在二氧化矽上的熱穩定性，雖然會隨著鉿含量的增加而變差，但至少都可達 400℃以上。

基於製程整合上的考量，我們進一步驗證了沈積鉿、鉬兩金屬層並經熱處理使其混合的方式以形成鉿鉬雙元合金，並藉此提出一雙功函數金屬閘極製程技術。由於達到完全的金屬混合以形成雙元合金所需的熱預算取決於兩金屬層的厚度總和 T_M ($T_M = T_{Hf} + T_{Mo}$)，我們提出了一個概念：根據金屬沈積後製程所需經過的總熱處理預算，選用適當的金屬層總厚度，則可以避免掉對金屬閘極材質本身熱穩定性的要求。此外，我們也驗證了藉由改變鉿、鉬兩金屬層的厚度比例 T_R ($T_R = T_{Hf} / T_{Mo}$)，可以精確地控制所形成的雙元合金的組成以及功函數值。上述的技術對於具有先進結構的元件諸如：FinFET、UTB-MOSFET 將相當具有吸引力，因為先進元件通常具有較薄的基板厚度，且基板的雜質摻雜濃度對元件臨界電壓的調變效果也大幅降低。此外，先進元件所需的閘極功函數值會隨基板厚度與閘極數目的

不同而有所差異，因此準確的功函數調變將會益形重要。

論文中所提出的第二種雙功函數金屬閘極製程技術則是應用了金屬的矽化反應。我們選擇在具有良好熱穩定性的金屬鉭上沈積了適當厚度的非晶矽，再藉由熱處理過程使其經由矽化反應生成矽化鉭，並藉此提出使用金屬鉭與矽化鉭作為閘極組合的雙功函數金屬閘極製程技術。在二氧化矽上，金屬鉭-矽化鉭之閘極組合所提供的功函數組合可適用於具有先進結構的元件，且矽化鉭亦被驗證具有良好的熱穩定性。另外我們發現在矽化反應之前，如果於非晶矽中佈植摻雜入雜質砷，則可進一步降低所生成矽化鉭的功函數值，進而拉大金屬鉭-矽化鉭之間的功函數差，將所提出的雙功函數金屬閘極製程技術之應用範圍擴大到傳統的本體元件。值得一提的是，此提出的新穎製程技術是利用金屬本身搭配本質或 *n* 型金屬矽化物來提供功函數差，有別於近期被廣泛研究的 FUSI 技術中利用 *p* 型與 *n* 型金屬矽化物來提供功函數差。由於避免了 *p* 型金屬矽化物的使用，因此可以消除硼穿透可能帶來的缺點。

我們同時也驗證了金屬鉭-矽化鉭之閘極組合在高介電材質上的特性。我們發現金屬鉭與矽化鉭在二氧化鉿的高介電閘極介電層上所得到的功函數值都分別略低於在二氧化矽上所得到的值，然而兩者間的功函數差值卻可維持。同時，矽化反應之前，於非晶矽中雜質砷的佈植仍然可以有效降低所形成矽化鉭在二氧化鉿上的功函數值，克服了 FUSI 技術在二氧化鉿高介電閘極介電層上，*p* 型與 *n* 型金屬矽化物幾乎無功函數差的致命缺點。相較於 FUSI 技術，雖然同樣運用到金屬的矽化反應，然而我們的實驗結果卻顯示出費米能階夾止效應被

有效壓抑。對此我們猜測其原因是：我們所提出的金屬鉬-矽化鉬雙功函數金屬閘極製程技術，其結構有效避免了非晶矽層在沈積過程以及矽化反應之前與高介電閘極介電層的直接接觸。

Investigation of Novel Dual Work Function Metal Gate Technologies

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Abstract

Two novel dual work function metal gate technologies are investigated and proposed. With the down-scaling of the device geometry for performance improvement, inherent drawbacks of conventional polysilicon gate electrodes lead to increasingly significant negative influence. In addition, the high-k gate dielectrics have been introduced to replace the conventional silicon dioxide. Consequently, under the same effective oxide thickness, the gate leakage current can be effectively reduced. Unfortunately, polysilicon gates have been reported to be thermodynamically unstable on many high-k materials and lead to Fermi-level pinning effect at the polysilicon/high-k interface. Therefore, metal gates are expected to provide a turning point in possessing a better thermal stability and a retardation of the Fermi-level pinning effect. In addition, metal gates can possess a lower gate resistance and enhance the device performance at higher frequency.

The basic requirements for a novel metal gate technology include providing

suitable work function values at the gate dielectric interface, the good enough thermal stability with the underlying gate dielectrics and a compatible device integration process. Two novel metal gate technologies are proposed in this dissertation. One is based on the metal intermixing technique, and the other is based on the silicidation technique. We firstly investigate the electrical and chemical characteristics of Hf-Mo binary alloys deposited by co-sputtering technique. A continuous and almost linear work function adjustment using $Hf_xMo_{(1-x)}$ is demonstrated for the first time. The work function value of Hf-Mo binary alloy ranges from 3.93eV (Φ_m of pure Hf) to 4.93eV (Φ_m of pure Mo) and depends on the sputtering power ratio of each target. The thermal stabilities of Hf-Mo binary alloy on SiO_2 are found to degrade with the increase of Hf atomic fraction, but all of the Hf-Mo binary alloys possess thermal stabilities at least higher than 400℃. The Hf-Mo binary alloys can be appropriate for a gate-last SiO_2 CMOS process.

The practicable integration of Hf-Mo binary alloys into the dual metal gate process is also proposed. $Hf_xMo_{(1-x)}$ formed by metal intermixing of the Hf/Mo stack is firstly evaluated, and a novel dual work function metal gate technology is then proposed and demonstrated. A precise control over the work function of the Hf-Mo binary alloy by adjusting the composite metal thickness ratio T_R ($T_R = T_{Hf} / T_{Mo}$) is demonstrated. Besides, the required thermal budget for a complete metal intermixing is demonstrated to depend on the total metal thickness, T_M ($T_M = T_{Hf} + T_{Mo}$). Therefore, one can be allowed to get around the thermal stability issue by using an appropriate T_M value. This technique is not only attractive but especially important for devices with advanced transistor structures, such as FinFET and/or UTB-MOSFET devices, since the substrate doping modulation may not be an efficient way to adjust the threshold voltages of devices with advanced transistor structures.

The other novel dual metal gate technology proposed in this dissertation is based on using the silicidation technique. The α-Si/Mo stack was fabricated and thermal annealed to form $MoSi_x$. The work function of $MoSi_x$ is found to be lower than that of Mo, and the thermal stability of $MoSi_x$ is evaluated to be higher than 950℃. Combining $MoSi_x$ with the pure Mo gate, a practical integration into the dual metal gate technology is then proposed. On the SiO_2 gate dielectric, the combination of Mo-$MoSi_x$ possesses a work function shift appropriate for devices with advanced transistor structures. Furthermore, the additional arsenic pre-implantation into the α-Si layer prior to the silicidation annealing is demonstrated to effectively lower the work function of $MoSi_x$. Consequently, the application of the proposed novel dual metal gate technology can be expanded to the conventional bulk devices. Besides, the new structure along with the ruling out of *p*-type metal silicide is also demonstrated to eliminate the boron penetration problem encountered with the reported FUSI method.

On high-k gate dielectric materials, the maintenance of the considerable work function shift is also demonstrated. The extracted Φ_m value of pure Mo or $MoSi_2$ gate on HfO_2 is slightly lower than that on SiO_2, but the Φ_m difference between Mo and $MoSi_x$ is almost the same regardless of the underlying gate dielectric materials. The arsenic pre-implantation still has effect upon the modulation of Φ_m of metal silicide on HfO_2, even though the modulation range is a little smaller than that on SiO_2. The influence of Fermi-level pinning effect, which has been reported to be responsible for the high threshold voltages of FUSI gated devices with the high-k gate dielectric, is also discussed. The Fermi-level pinning effect seems to be retarded in the proposed Mo-$MoSi_x$ dual metal gate technology. We speculate that the improvement may be attributed to the separation of silicon layer from the high-k gate dielectrics.

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李宗霖

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Introduction

1.1 EVOLUTION OF GATE ELECTRODE CANDIDATES

Before the mid-1970s, the doping technique was accomplished by the diffusion process in high-temperature furnaces. After the source/drain (S/D) diffusion, the thin gate oxide is grown and the metal gate is deposited. If the gate mask is misaligned with the S/D mask, the transistor will not work properly as shown in fig. 1.1. Oversized gate electrodes are required to ensure the complete gate coverage over the S/D. The gate misalignment issue leads to a great challenge especially when devices are scaled down.

The application of ion implantation solved the gate alignment problem by using the so-called self-aligned S/D doping process as shown in fig. 1.2. In this case, the gate oxide is grown followed with the deposition, patterning, and etching of gate electrodes. The ion implantation is used to form the S/D region and a high temperature annealing process is required to repair the damage due to the implantation process and to activate the implanted dopant. Since the required annealing temperature is usually higher than the melting point of aluminum (Al), a different gate electrode candidate has to be introduced. Polysilicon and silicide/polysilicon stack (polycide) have been used as the gate materials for several device generations.

In the late-1980s, the need to reduce the power consumption of the integrated circuit (IC) was one of the major driving forces for complementary MOS (CMOS) devices development. Early CMOS based ICs used n^+-polysilicon as gate electrodes for both *n*-MOS and *p*-MOS devices as shown in fig. 1.3. To suppress the punch through in *p*-MOS devices, the substrate doping concentration will need to be increased. Along with the use of lower Fermi energy n^+-polysilicon as gate electrode, the threshold voltage of *p*-MOS will be too negative to be acceptable. A thin sheet of negative charges must therefore be placed at the Si/SiO_2 interface in *p*-MOS devices. This can be accomplished by implanting a shallow layer of boron atoms. The boron dose must be heavy enough to compensate the *n*-surface so that a thin *p*-region is formed and shifts the threshold voltage of *p*-MOS toward more positive value.

However, this technology (n^+-polysilicon for both *n*-MOS and *p*-MOS) will lead to a buried-channel *p*-MOS device which will exhibit enhanced susceptibility to short-channel effects. Solutions involving the use of gate electrodes other than n^+-polysilicon must therefore be explored. One alternative is to use n^+-polysilicon and p^+-polysilicon for *n*-MOS and *p*-MOS devices, respectively, as shown in fig. 1.4. Such a so-called dual-doped poly approach, however, introduces other problems. One drawback is the poor threshold voltage control in the *p*-MOS devices due to penetration of the boron atoms into the oxide or further into the silicon substrate, as shown in fig. 1.5, especially when a thin gate oxide is used [1]. It has also been found that the presence of fluorine in the gate oxide worsens the boron penetration problem [2, 3]. Such fluorine can be introduced into the gate oxide if the *p*-MOS S/D regions are formed using BF_2 implantation which is suggested for shallow junction formation.

Another problem encountered with conventional polysilicon gates is the

so-called poly depletion effect as shown in fig. 1.6 [4]. If the polysilicon gate is not doped heavily enough, problems will arise from the depletion of the gate itself. Gate depletion results in an additional capacitance in series with the gate oxide capacitance, which in turn leads to a reduced inversion-layer charge density and degradation of the MOSFET transconductance. It is worth to note that the boron penetration and poly depletion effect in *p*-MOS devices will influence each other. Heavily boron concentration is needed for p^+-polysilicon to suppress the poly depletion effect in PMOS while it potentially makes the boron penetration problem more pronounced.

It is also worth to note that the shrinkage of oxide thickness can improve the device short channel performance, however, the increasing leakage current leads to the noticeable standby power. Replacing the conventional silicon dioxide gate stack with the novel high-k gate dielectric material draws more and more attention in the last several years. The use of the high-k gate dielectric can possesses larger physical oxide thickness under the same electrical oxide thickness and results in effective leakage current reduction. Several high-k materials have been investigated as new gate dielectric candidates such as TiO_2, Ta_2O_3, Al_2O_3, ZrO_2, HfO_2, La_2O_3, Y_2O_3 and Pr_2O_3. Among these candidates, HfO_2 not only has relatively high dielectric constant and bandgap but also exhibits the impressive thermal stability with the silicon substrate. The polysilicon/HfO_2 interface, however, will lead to the so-called Fermi-level pinning effect which is believed to have been caused by Si-Hf interaction and leads to high threshold voltages of MOSFET devices. Moreover, polysilicon gates are found to be thermodynamically unstable on many high-k materials [5, 6] so that metals are expected to provide a turning point in possessing a better thermal stability.

1.2 BASIC REQUIREMENTS FOR METAL GATES

The use of metal/high-k structure, however, will introduce several new challenges such as the choice of metal candidates, the development of a compatible process and the thermal stability issue between metal and high-k gate dielectric.

The work function value of the introduced metal candidate will significantly influence threshold voltages of fabricated devices. High performance CMOS technology generally requires two separate gate work function values for *n*-MOS and *p*-MOS devices. Providing appropriate work function values at the gate dielectric interface, one can achieve low and symmetric threshold voltages for *n*- and *p*-channel devices without high dosage channel implantation which potentially leads to the threshold voltage non-uniformity and the carrier mobility degradation. Metals with midgap work function, such as W and TiN, have been firstly adopted as gate candidates for symmetric threshold voltage values. However, the magnitude of resulted threshold voltages for both *n*- and *p*-channel devices would be too large to be acceptable [7, 8]. To avoid applying heavily counter channel doping, the dual work function metal gate technology has been proposed [9-11]. The major concept is similar to the dual-doped polysilicon technology where different gate materials with suitable work function values are served as gate candidates for *n*- and *p*-channel devices. The chosen metal candidates should provide suitable work function (Φ_m) values at the dielectric interface. For instance, metal gates should possess work function values of about 4eV and 5eV to replace the conventional n^+- and p^+-polysilicon gates, respectively, for surface-channel bulk devices. Moreover, several

advanced devices with new transistor structures, such as FinFET and ultra-thin-body (UTB) MOSFET, have been developed recently [12-19]. These advanced devices have better gate-to-channel controllability. Consequently, the required gate work function values for low and symmetric threshold voltages will be different from those in bulk devices. Moreover, the adjustment of the substrate doping is no longer an effective way of threshold voltage control in advanced devices. Choosing metal gate candidates with suitable work function values becomes a more and more importance topic. The reported simulation results show that the required gate work function for *n*- and *p*-channel advanced devices are about 4.4~4.6eV and 4.8~5.0eV, respectively.

In addition, the chosen metal candidates should be able to possess good thermal stability with the underlying gate dielectric material. Consequently, the undesired interaction at metal/gate dielectric interface during the device fabrication process can be avoided, and the process induced Φ_m and/or the equivalent oxide thickness (EOT) variations can be suppressed. Although the recently developed gate-last (also called replacement gate) technique can provide a new chance of using low thermal stable materials as gate electrodes [20-26], the fabrication process will become more complex and lead to new challenges such as dummy gate removal and metal polish.

The development of suitable process integration is also an important issue to avoid the possible process-induced performance degradation. Several metal gate technologies have been widely investigated in the last decade. The firstly proposed dual work function metal gate technology exhibits a straightforward fabrication process [9, 10]. Although the used Ti and Mo have suitable work function values for *n*- and *p*-channel devices, respectively, the proposed integration process inherently makes the gate dielectric material exposed to the metal etchant and leads to an

undesired reliability problem and oxide thickness non-uniformity.

To overcome this phenomenon, a novel dual work function metal gate technology using Ni-Ti interdiffusion has been proposed [27, 28]. Although this approach is quite material-dependent, it provides a lot of suggestions and recommendations on the dual metal gate technologies. Furthermore, a novel metal work function adjustment technique using nitrogen implantation has been proposed [29-32]. This approach is good at the ease of process integration but the modulated range of work function may not be large enough and the process stability will be a challenge.

Recently, a so-called fully silicidation (FUSI) method has been proposed to apply for implement of dual work function metal gate technology [33-38]. The front-end process is the same with the traditional dual-doped polysilicon gates CMOS technology while the conventional salicide process is modified. A metal layer thicker than that required for conventional salicide process is required to allow for full silicidation of the existed polysilicon gates. And dopants in the polysilicon are demonstrated to be able to modify the work function value of the formed metal silicide (MeSi) gates.

Several metal candidates, metal nitrides and binary alloys have also been widely investigated in the last five years. To sum up, the dual work function metal gate technology is drawing more and more attention.

1.3 METAL WORK FUNCTION EXTRACTION TECHNIQUE

There are several methods for the metal gate work function extraction. One is comparing the flat-band voltage shift of MOSCAP devices between the under test metal gate electrode and that with known work function value such as n^+ poly-silicon. In this case, devices should be subjected to the similar process flow and the same thermal budget. From the known work function of n^+ poly-silicon and flat-band voltage difference between n^+ poly-silicon and the under test metal, the metal work function can be estimated. But the value of the extracted metal work function in this approach would be less precise due to the different gate electrode deposition processes for polysilicon and metal gates. In general, metal gates are deposited using sputtering system, and this physical vapor deposition (PVD) system will inherently result in more oxide charges contributing to flat-band voltage difference.

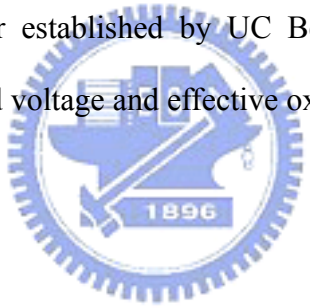
Another approach bases on the expression of the flat-band voltage in a MOS system [29]:

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{C_{ox}} = \Phi_{ms} - \frac{Q_f}{\varepsilon_{ox}} t_{ox} \qquad (1.1)$$

where Q_f is the density of fixed charges in the oxide, ε_{ox} is the permittivity of the dielectric material and t_{ox} is the thickness of the gate dielectric. To decouple the effect of fixed oxide charges, Capacitance-voltage measurements of MOSCAP devices with different oxide thicknesses will be performed to generate the flat-band voltage (V_{FB}) versus the effective oxide thickness (EOT) plot. The intercept of V_{FB} axis corresponds to the value of Φ_{ms}. The value of Φ_s can be calculated according to the information of the electron affinity of silicon substrate, silicon energy bandgap and the potential difference between the intrinsic and doped silicon Fermi level. Work function values obtained in this way, however, would be fair approximations after accounting for

uncertainties in flat-band voltage determination and the contributions of interface trap state.

Notably, it has been reported that the quantum mechanical (QM) effect becomes significant in the oxide thickness extraction as oxide thickness is reduced [39, 40]. Carrier transporting in the channel is confined by a triangular energy well. Consequently, the charge centroid locates further from the surface than that predicted by the classic analysis. This quantum mechanical effect will contribute additional effective oxide thickness and then lead to a deviation in metal work function extraction. Several capacitor-voltage simulators with the consideration of quantum confinement effect, such as QMCV and NCSU-CV, have been proposed. In this thesis, we use the QMCV simulator established by UC Berkeley Device Group for the determinations of the flat-band voltage and effective oxide thickness.



1.4 ORGANIZATION OF THE THESIS

Two novel dual-work function metal gate technologies are proposed and investigated in this dissertation. First, the dual metal gate technology based on the use of Hf-Mo binary alloys is demonstrated. Second, the silicidation technique is used to implement a dual metal gate technology with metal-metal silicide combination.

In chapter 1, an introduction to the gate candidate evolution and a brief review of state-of-the-art metal gate technologies are discussed. Basic requirements of novel metal candidates are also addressed. Moreover, the used work function extraction technique in this dissertation is also mentioned.

In chapter 2, the electrical and chemical characteristics of Hf-Mo binary alloys are investigated. The continuous and almost linear work function adjustment using $Hf_xMo_{(1-x)}$ is demonstrated for the first time. The work function value of Hf-Mo binary alloy deposited by co-sputtering ranges from 3.93eV (Φ_m of pure Hf) to 4.93eV (Φ_m of pure Mo) and depends on the sputtering power ratio of each target. The thermal stabilities of Hf-Mo binary alloys on SiO_2 degrade with the increase of Hf atomic fraction, but all of them possess thermal stabilities at least higher than 400℃. The Hf-Mo binary alloys can still be suitable for the gate-last SiO_2 CMOS process.

In chapter 3, the integration of Hf-Mo binary alloys into dual metal gate technology is proposed. For the ease of process integration, $Hf_xMo_{(1-x)}$ formed by metal intermixing is evaluated, and a novel dual work function metal gate technology is proposed and demonstrated. One can be allowed to get around the thermal stability issue by using an appropriate metal thickness, and possess precise controllability of metal work function by adjusting the composite metal thickness ratio. This technique is not only attractive but especially important for FinFET and/or UTB-MOSFET applications.

In chapter 4, a novel dual metal gate technology based on silicidation technique is proposed. The α-Si/Mo stack was fabricated and thermal annealed to allow for the formation of $MoSi_x$. Combining $MoSi_x$ with the pure Mo, a practical integration of Mo-$MoSi_x$ gate combination into dual metal gate technology is also proposed. On the SiO_2 gate dielectric, Mo-$MoSi_x$ combination can possess considerable work function shift and be suitable for devices with advanced transistor structures. The thermal stabilities of pure Mo and $MoSi_x$ on SiO_2 are evaluated to be higher than 950℃. Moreover, the additional arsenic pre-implantation into the amorphous silicon layer

prior to silicidation annealing is demonstrated to make the application of the proposed novel dual metal gate technology also suitable for the conventional bulk devices. The new structure along with the ruling out of *p*-type metal silicides can effectively eliminate the boron penetration problem encountered with the FUSI method.

In chapter 5, the proposed dual metal gate technology gated by Mo and $MoSi_x$ is demonstrated to keep providing the considerable work function shift on the high-k gate dielectric materials. The extracted Φ_m value of pure Mo or $MoSi_2$ gate on HfO_2 is slightly lower than that on SiO_2, but the Φ_m difference between Mo and $MoSi_x$ is almost the same with that on SiO_2 regardless of the underlying gate dielectric materials. The use of arsenic pre-implantation for the modulation of Φ_m of metal silicide on HfO_2 is also demonstrated, even though the modulation range is a little smaller than that on SiO_2.

In chapter 6, we conclude our results and summarize the main contributions in this dissertation. Suggestions for further studies are also discussed.

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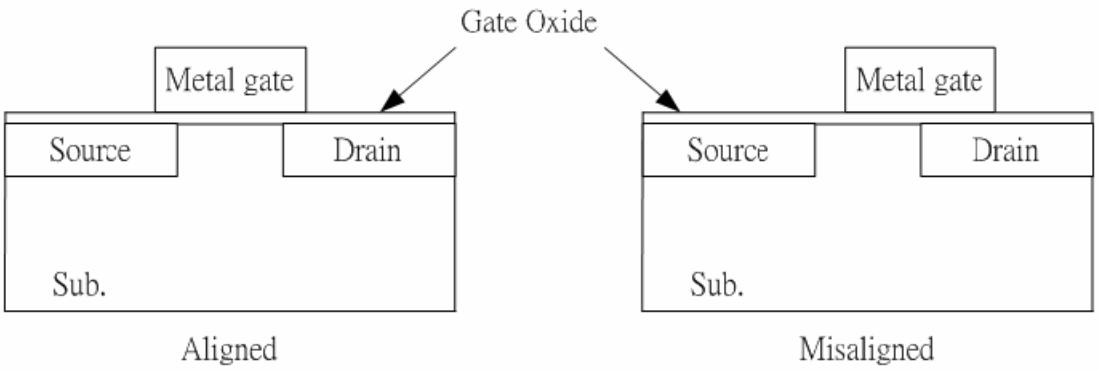

Fig. 1.1 Illustration of gate misalignment.

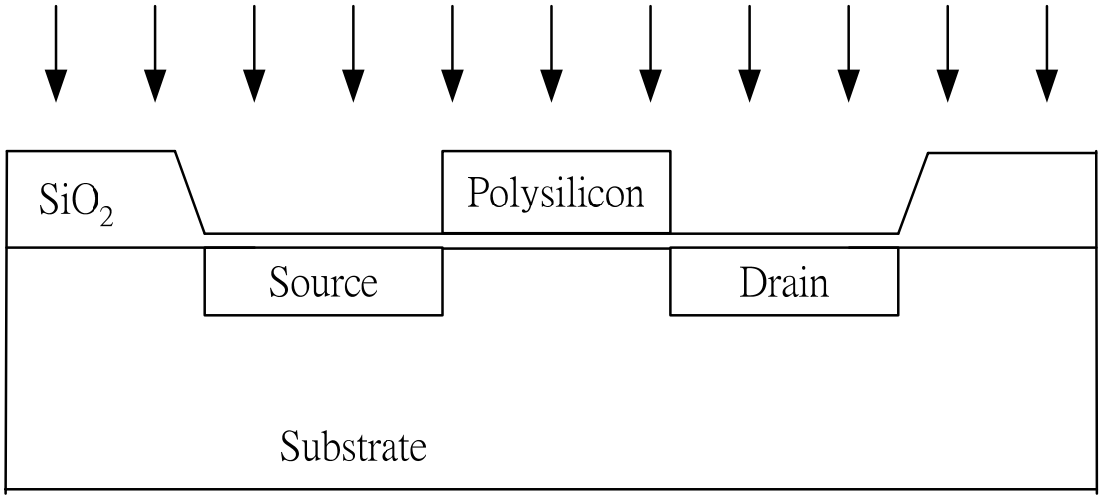

Fig. 1.2 Illustration of self-aligned process.

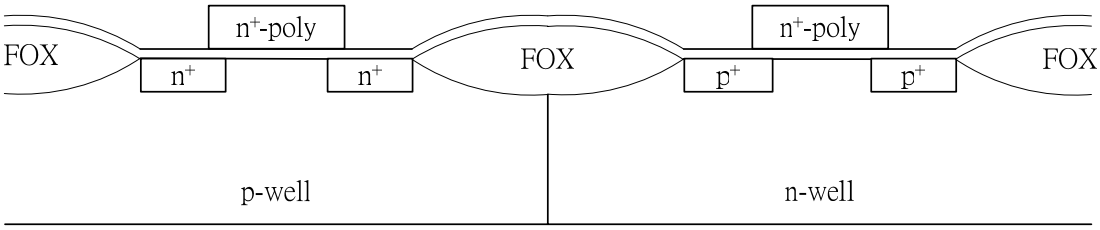

Fig. 1.3 Illustration of polysilicon gate technology using only n^+-poly for both *n*- and *p*-channel devices.

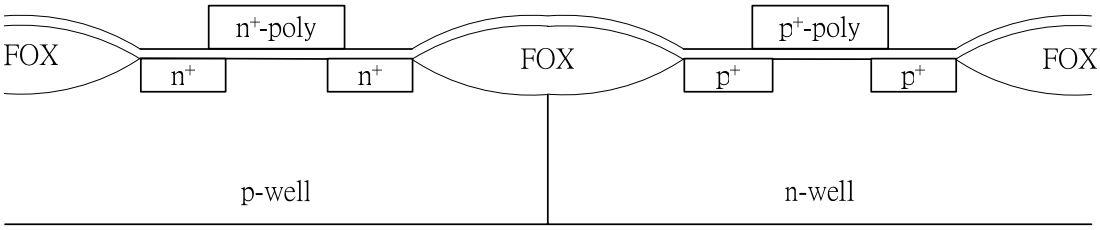

Fig. 1.4 Illustration of dual-doped polysilicon gate technology.

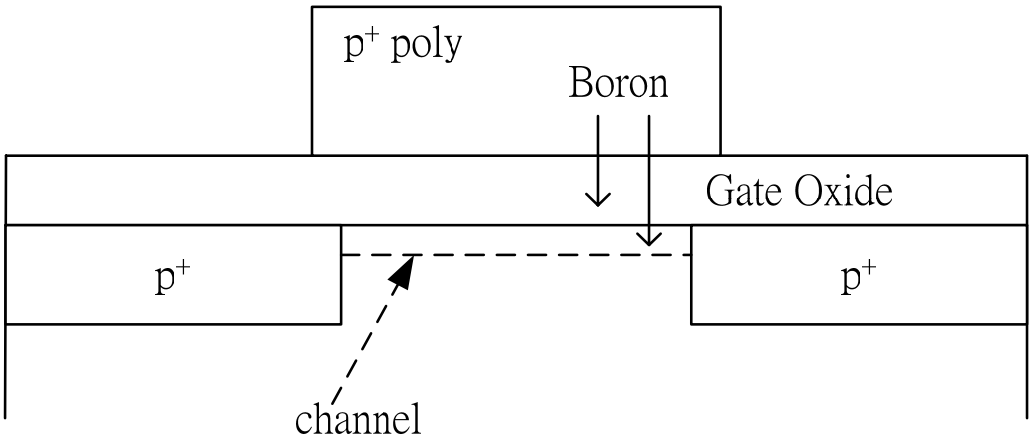

Fig. 1.5 Illustration of the boron penetration.

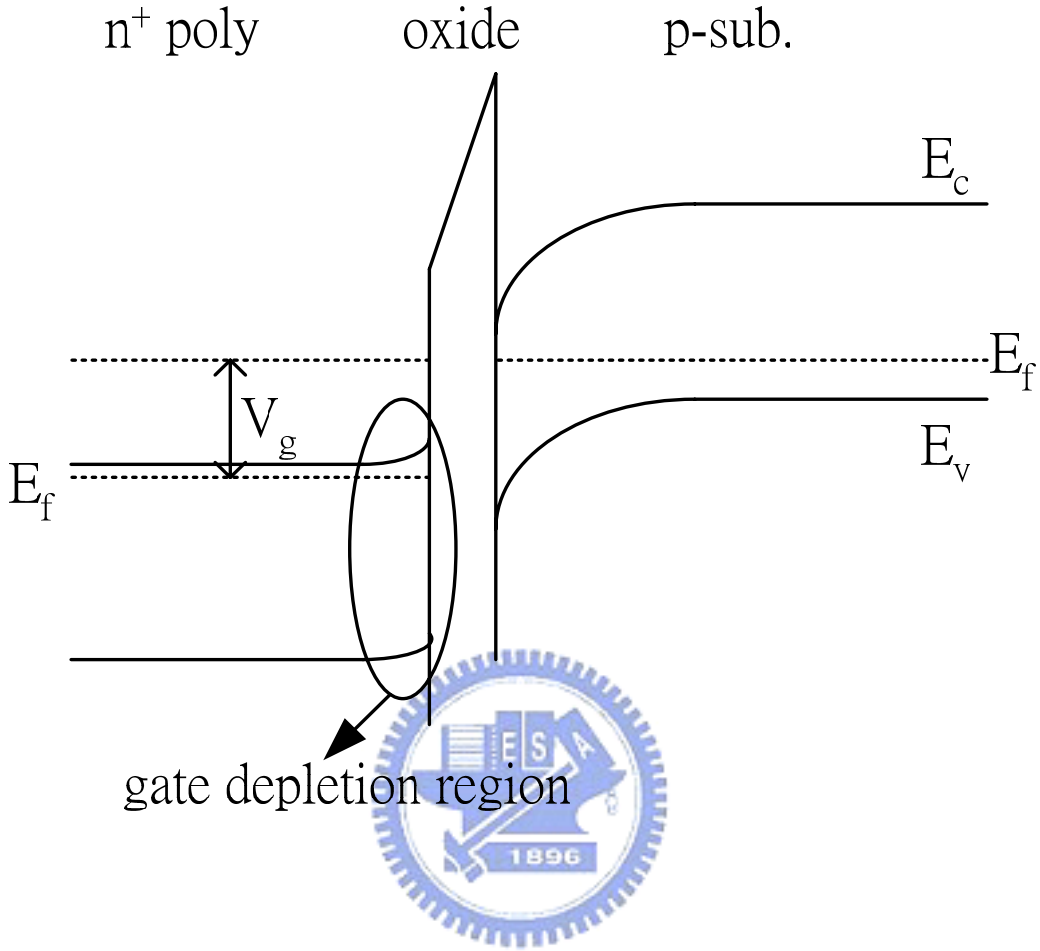

Fig. 1.6 Illustration of the poly depletion effect.

Chapter 2

Investigation of $Hf_xMo_{(1-x)}$ Binary Alloys

2.1 BACKGROUNDS AND MOTIVATION

With the sustained scaling of CMOS technology for device performance improvement, the conventional polysilicon/SiO_2 structure keeps suffering a variety of challenges. Novel metal/high-k gate stack has been extensively investigated as a potential solution. The introduction of high-k gate dielectric can effectively reduce the tunneling leakage current due to its larger physical thickness under the same electrical thickness [1, 2]. On the other hand, the inherent drawbacks of polysilicon gates such as poly depletion effect and boron penetration which will lead to an undesired increase of EOT [3] and degrade device performance [4] can be eliminated. In addition, polysilicon gates have been reported to be thermodynamically unstable on many high-k materials [5, 6] so that metals are expected to provide a turning point in possessing better thermal stability and a lower gate resistance for the enhancement of device performance at high frequency.

The major superiority of the traditional polysilicon gate electrode is the ability of Fermi-level adjustment by either donor or acceptor implantation. By contrast, the adjustment of the metal work function is not easily achievable. For bulk devices, the required metal work functions for replacing the conventional n^+- and p^+- polysilicon gates are about 4eV and 5eV, respectively. On the other hand, for FinFET and/or

ultra-thin-body (UTB) MOSFET devices, the gate-over-channel controllability is enhanced so that the required gate work function for *n*-channel (*p*-channel) devices have been increased (reduced) to 4.4~4.6eV (4.8~5.0eV) compared with conventional bulk devices [7]. Since the required work function values for *n*- and *p*-channel devices are different in both cases, the dual metal gate technology with suitably chosen metal work function values has been proposed. However, the process integration will lead to the unwanted gate dielectric integrity degradation [8] due to the direct removal of metal from the dielectric surface. It is worth to note that, the adjustment of the substrate doping is no longer an effective way of threshold voltage control in FinFET and/or UTB-MOSFET devices so that the importance of metal gate work function engineering will be more pronounced.

Recently, several metal work function modulation techniques have been widely investigated. The Ru-Ta alloy proposed by H. Zhong et al. can possess the superior thermal stability and a wide work function tuning range [9, 10]. However, the modulation of work function seems not to be continuous. The work function values with interest for advanced transistor structures (4.4-5eV) would be unachievable. Moreover, the Pt-Ta alloy proposed by B-Y. Tsui et al. has been demonstrated to possess a wide and continuous work function modulation [11], but the issue of gate dielectric integrity degradation mentioned in [8] would be problematic due to the lack of suitable integration methods. Similarly, S. H. Bae et al. proposed that the laminated metal gate stacks HfN/Ti/TaN and Ti/Ta can possess *p*- and *n*-MOS compatible work function values (5.1eV and 4.35eV) [12]. However, the process integration of these two distinct laminated metal stacks into dual metal gate CMOS process are still problematic [8]. Otherwise, a novel work function modulation using nitrogen implanted Mo has been proposed by P. Ranade et al. [13]. The major advantage of this

method is the ease of process integration, while the Φ_m value strongly depends on the implantation parameters and subsequent annealing conditions. A precise work function modulation would not be easily achievable.

In this chapter, the continuous and almost linear work function adjustment using Hf-Mo binary alloys deposited by co-sputtering is demonstrated for the first time. The work function value of Hf-Mo binary alloy deposited by co-sputtering ranges from 3.93eV (Φ_m of pure Hf) to 4.93eV (Φ_m of pure Mo). Moreover, thermal stabilities of Hf-Mo binary alloys on SiO_2 gate dielectric are also evaluated. Although the thermal stability of $Hf_xMo_{(1-x)}$ on SiO_2 degrades with the increase of Hf atomic fraction, $Hf_xMo_{(1-x)}$ can still be appropriate for the gate-last SiO_2 CMOS process.

2.2 EXPERIMENT

MOSCAP devices were fabricated on *p*-type (100) 6-in Si wafers and high frequency (1MHz) capacitance-voltage characteristics were measured using an Agilent 4284A precision LCR meter. After LOCOS isolation, SiO_2 with different thicknesses were thermally grown at 950℃ to serve as the gate dielectric. $Hf_xMo_{(1-x)}$ (~50nm) alloys were then deposited by co-sputtering in Ar ambient. The sputtering power of each target was varied as listed in Table 2.1 to modulate the composition of the deposited binary alloy. The $Hf_xMo_{(1-x)}$ gate electrodes were then patterned by reactive ion etching (RIE) using Cl_2-based chemistry. All samples were then subjected to 400℃ annealing in N_2 ambient. The flat-band voltage (V_{FB}) and effective oxide thickness (EOT) of each capacitor were extracted from the measured C-V curve using the quantum mechanical C-V (QMCV) simulator so that one can avoid overestimating

the EOT as well as the metal work function value [14].

2.3 RESULTS AND DISCUSSION

The as-deposited high frequency (1MHz) C-V characteristics of capacitors gated by Hf-Mo binary alloys, pure Mo, and pure Hf films are shown in Fig. 2.1. The negative flat-band voltage shift with the increase of Hf power ratio can be observed. To eliminate the contribution of oxide fixed charges, C-V measurements of MOSCAP devices with several oxide thicknesses were performed to generate the V_{FB} versus EOT plot as shown in Fig. 2.2. All samples exhibit linear relationships from which work function values of binary alloys can be extracted as listed in Table 2.1.

Figure 2.3 exhibits the (110) morphology for the pure Mo film. The extracted work function value (4.93eV) of the (110) oriented Mo is closely consistent with previous reports [13]. However, the as-deposited Mo with (110) orientation is different from the previous report [15], and this would be attributed to the different deposition conditions. Figure 2.4 exhibits the small the hysteresis for the 50% Hf power ratio co-sputtering sample, which is believed to suffer from the most series sputtering damage. Accordingly, the good process quality can be demonstrated.

The C-V curves of as-deposited and post-400℃ sintering pure Hf gated capacitor are shown in Fig. 2.5. Obvious EOT variation along with the V_{FB} shift after annealing illustrates the poor thermal stability of Hf on SiO_2 and exclude Hf from gate candidates even in the gate last process [16]. By contrast, $Hf_xMo_{(1-x)}$ gated capacitors exhibit better thermal stability on SiO_2 as shown in Fig. 2.6. The dependence of Φ_m

and EOT variation on annealing conditions for $Hf_xMo_{(1-x)}$ also indicates that the thermal stability of all alloy samples can be at least higher than 400℃ as shown in Fig. 2.7.

In Fig. 2.7, the decreases of EOT at certain temperature for alloy samples, except for the one with 25% Hf power ratio, are similar to that for the pure Hf sample. The noticeable EOT decrease and the corresponding work function variation might be attributed to that partial SiO_2 gate dielectric was transformed into high-k materials, such as HfO_2 or $HfSi_xO_y$, due to the Hf-SiO_2 interaction. For the 25% alloy sample, the abnormal EOT increase along with relative small work function variation can be observed. We speculate that the lower Hf concentration might make the effect of Hf-SiO_2 interaction be masked by the extra Si-substrate oxidation due to the oxygen contamination. In the case of sample gated by pure Mo, the small amount of Φ_m increase (18meV) and the negligible EOT variation (0.08nm) after 950℃ RTA demonstrate the superior thermal stability of Mo on SiO_2 gate dielectric. Although the thermal stability seems to be degraded with the increasing of the Hf atomic fraction in the Hf-Mo binary alloy, $Hf_xMo_{(1-x)}$ still can be adopted as gate material in a gate-last SiO_2 CMOS process. It is worth to note that, alloy samples with Hf power ratio lower than 50% can possess work function value suitable for advanced devices and exhibit thermal stability up to 700℃. In comparison with other reported candidates, the thermal stability of Hf-Mo alloy is lower than that for Ru-Ta alloy [9], but higher than that for Pt-Ta alloy [11].

In 1974, Gelatt and Ehrenreich proposed that the work function of an $A_xB_{(1-x)}$ alloy can be approximately expressed as [17] :

$$\Phi_m(x) = x\Phi_{m,A} + (1-x)\Phi_{m,B} + x(1-x)\frac{(\Phi_{m,A} - \Phi_{m,B})(\rho_A/\rho_B - 1)}{x \cdot \rho_A/\rho_B + (1-x)} \quad (1.1)$$

In this equation, $\Phi_{m,A}$ and $\Phi_{m,B}$ are work function values of pure element A and B, respectively. ρ_A and ρ_B are effective density of states in Fermi level for pure element A and B, respectively. In this equation, the first two terms represent that the work function of the binary alloy is a linear combination of that of each pure element. On the other hand, the last term will lead to a deviation from the linear relationship. According to the theory of heat capacity of metal, the observable Sommerfeld factor γ of a metal is directly proportional to its density of state in Fermi level ρ [18].

The calculated results of eq. (1) are shown in fig. 2.8 where several γ ratios are used and values of $\Phi_{m,A}$ and $\Phi_{m,B}$ are set to be 3.93 and 4.93, respectively, for convenience. As expected, the work function modulation will deviate from the linear behavior with the difference in γ values between two metals. For a non-linear behavior, work function modulation can be roughly divided into the flat and sharp regime. In the flatter regime, the alloy system would be less susceptible to the composition and process variation, but the Φ_m modulation efficiency will be lower. On the other hand, the alloy system will be more sensitive to the process variation but possess higher Φ_m modulation efficiency in the sharper regime. By contrast, the linear work function modulation can provide a compromise between the modulation efficiency and immunity to the process variation throughout the whole modulation range.

According to the binary alloy phase diagram of Hf-Mo system [19] shown in fig. 2.9, an abrupt work function modulation can be excluded since no specific compound will be formed under 1000℃. Moreover, the Sommerfeld factors for Hf and Mo are

2.16 and 2.0, respectively [18]. Therefore, a continuous and almost linear work function modulation using the $Hf_xMo_{(1-x)}$ solid solution can be expected. The calculated and experimental results of work functions of $Hf_xMo_{(1-x)}$ alloys are shown in fig. 2.10. Compared with the experimental data, a good consistency with only a mildly shift in the lower Hf power ratio regime can be observed. This deviation may be attributed to the difference between the Hf power ratio and the Hf atomic fraction due to a relatively lower deposition rate of Mo in this work.

The XRD spectra and AES depth profile of the co-sputtering sample are shown in fig. 2.11 and fig. 2.12, respectively. An amorphous film with uniform composition and abrupt interface is observed. It is worth to note that the relatively lower composition of Mo compared to that of Hf in the co-sputtering sample as shown in fig. 2.12 also demonstrates our speculation about the deviation observed in Fig. 2.10.

2.4 SUMMARY

The continuous and almost linear work function adjustment using $Hf_xMo_{(1-x)}$ is demonstrated for the first time. The work function value of Hf-Mo binary alloy deposited by co-sputtering ranges from 3.93eV (Φ_m of pure Hf) to 4.93eV (Φ_m of pure Mo) and depends on the sputtering power ratio of each target. The thermal stabilities of Hf-Mo binary alloys on SiO_2 degrade with the increase of Hf atomic fraction, but all Hf-Mo binary alloys still possess thermal stabilities at least higher than 400℃. The Hf-Mo binary alloys can be used in a gate-last SiO_2 CMOS process.

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Sample	Hf power (W)	Mo power (W)	Hf power ratio (%)	Φ_m (eV)
ctrl.	0	150	0 (pure Mo)	4.932
1-1	22	150	12.8	4.727
1-2	50	150	25	4.597
1-3	90	150	37.5	4.492
1-4	150	150	50	4.350
1-5	150	90	62.5	4.213
1-6	150	50	75	4.150
1-7	150	22	87.5	4.062
ctrl.	150	0	100 (pure Hf)	3.930

Table 2.1. Sample conditions and extracted Φ_m of co-sputtering experiment. (alloy samples : 400℃, 30s；control samples : as-deposited)

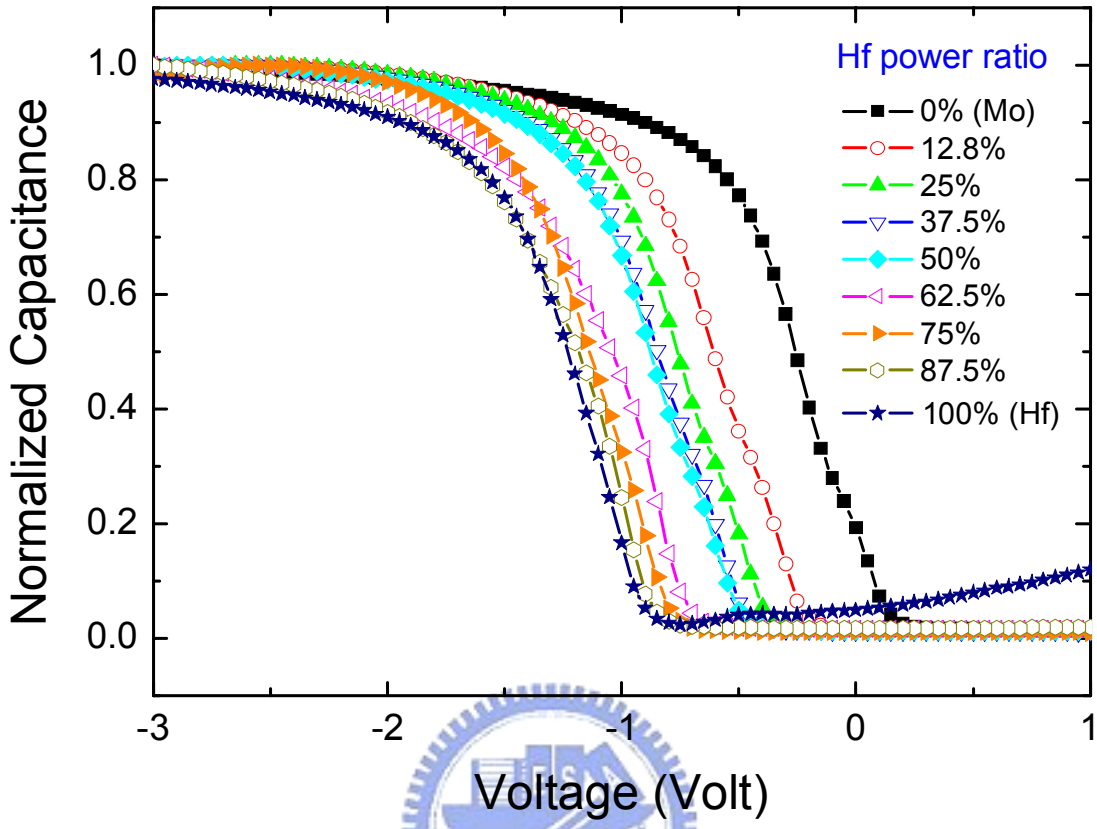

Fig. 2.1. C-V curves of as-deposited co-sputtering samples. Wide-ranging flat band voltage shift can be observed.

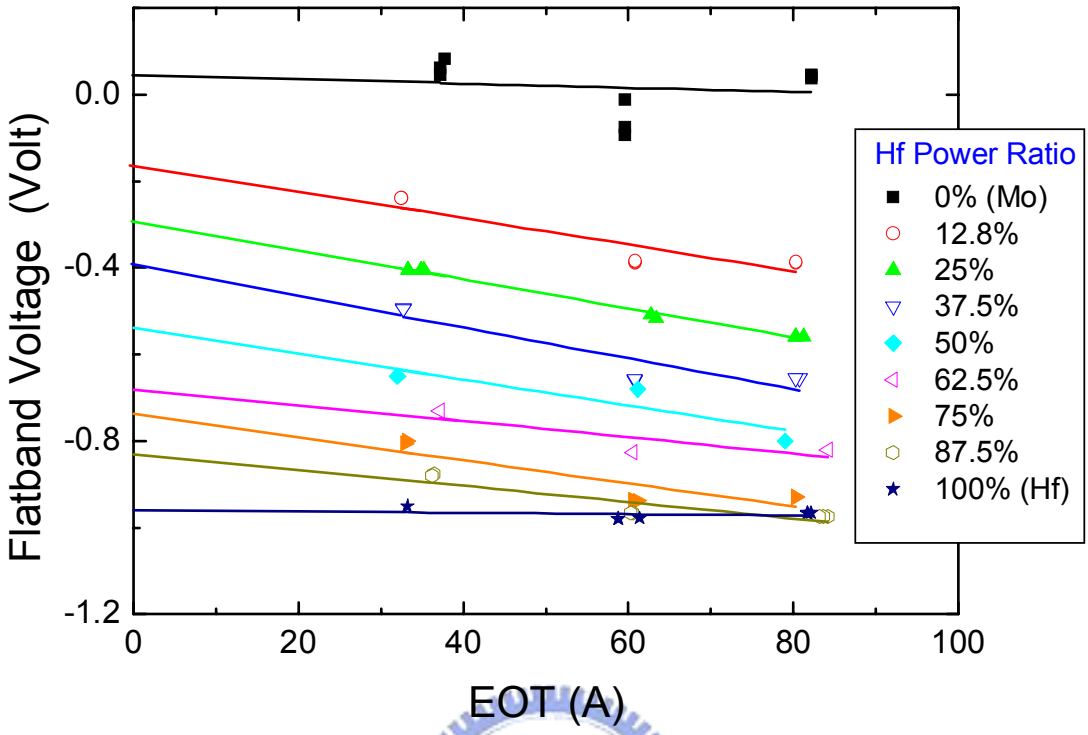

Fig. 2.2. All samples (Table I.) exhibited linear behavior in V_{FB} vs. EOT curves from which work function of each alloy could be extracted. (alloy samples : 400℃, 30s ; control samples : as-deposited)

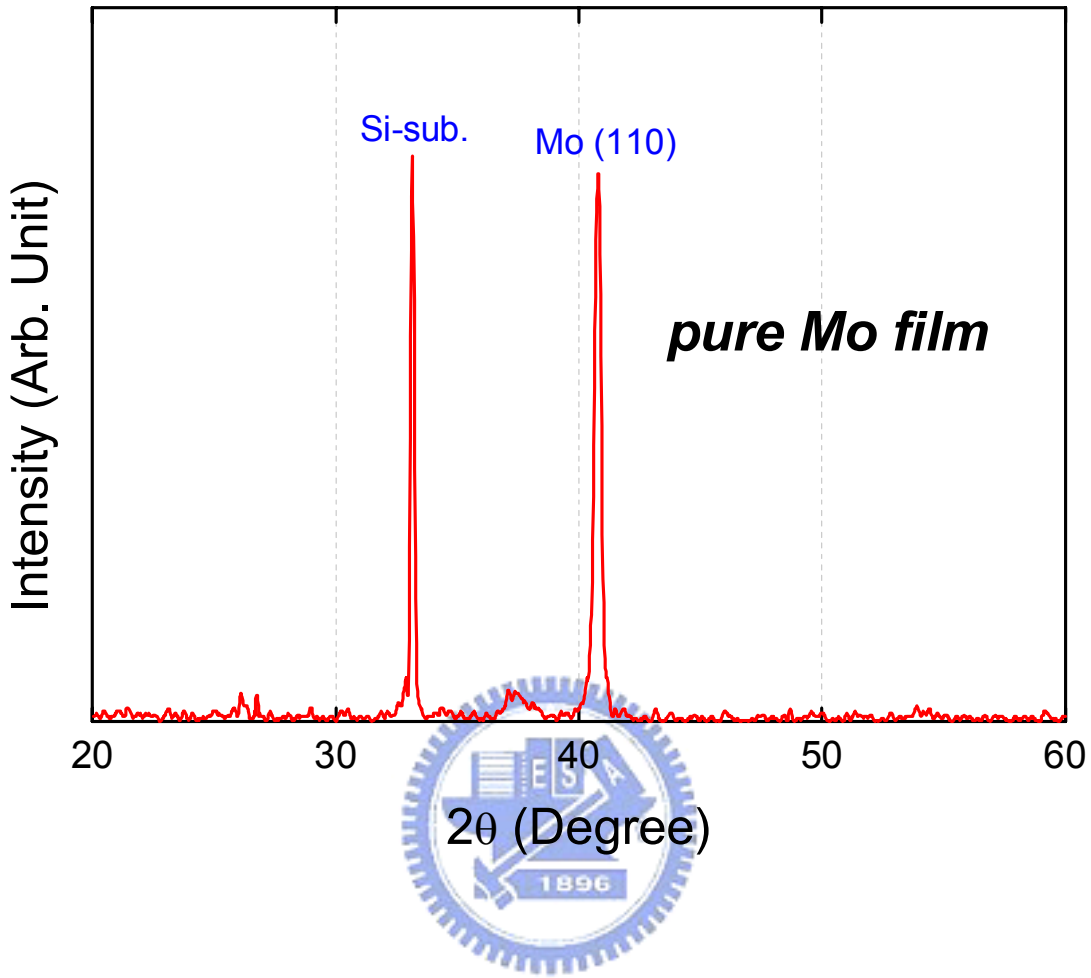

Fig. 2.3. The as-deposited pure Mo film is found to have (110) orientation.

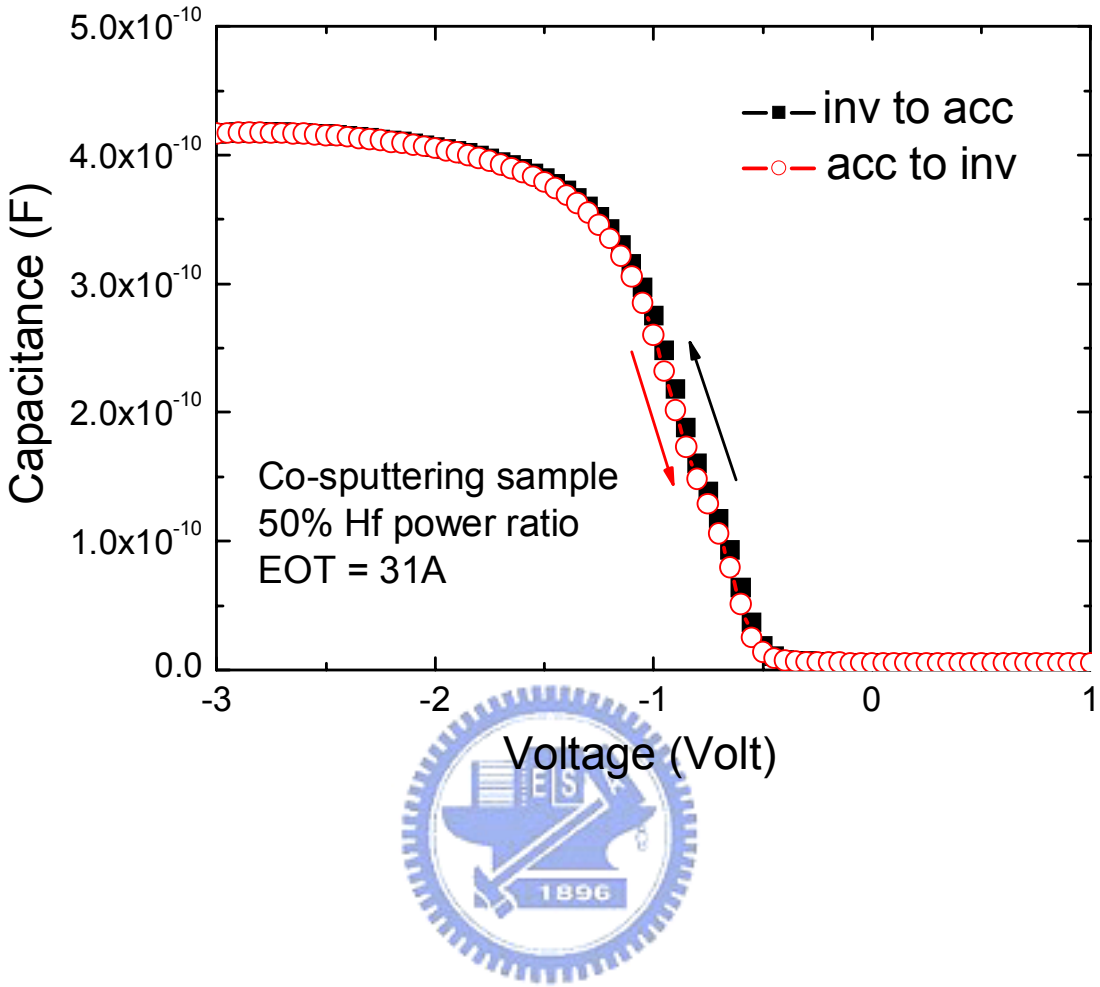

Fig. 2.4. Process quality was demonstrated, since the 50% Hf power ratio sample suffering maximum power summation during metal deposition still exhibited negligible hysteresis.

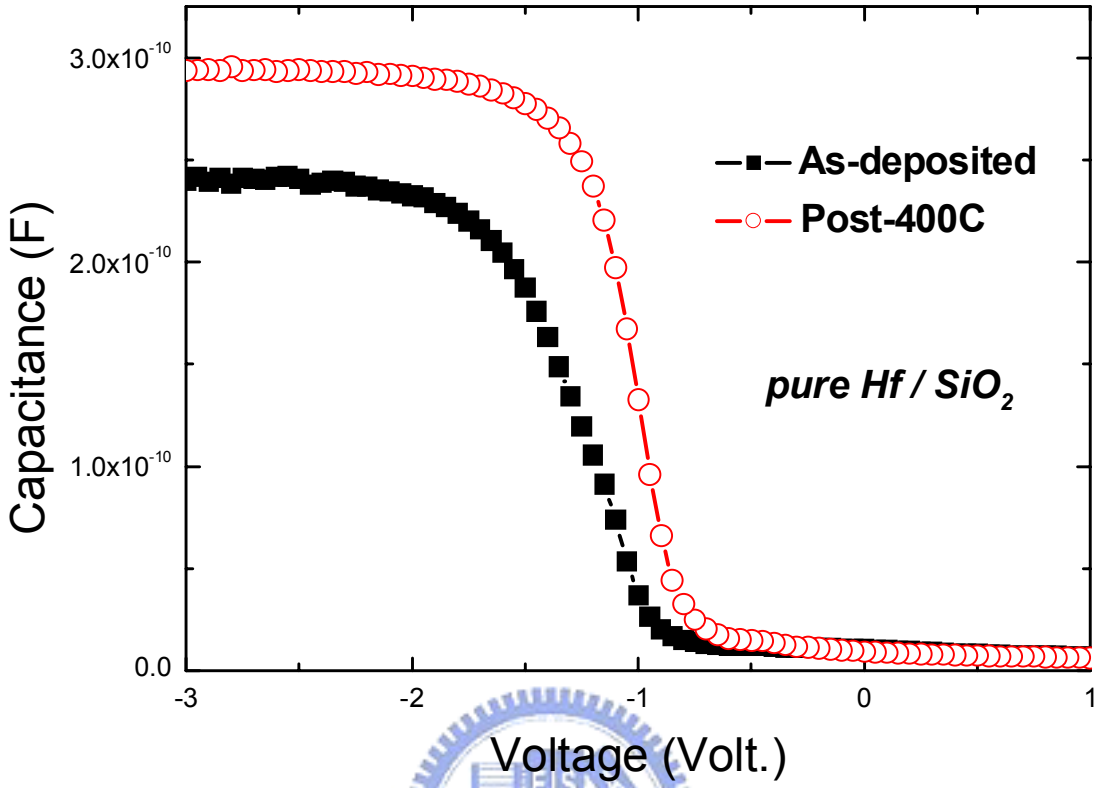

Fig. 2.5. C-V curve of post-400℃ annealing Hf gated capacitor shows noticeable EOT variation and flatband voltage shift.

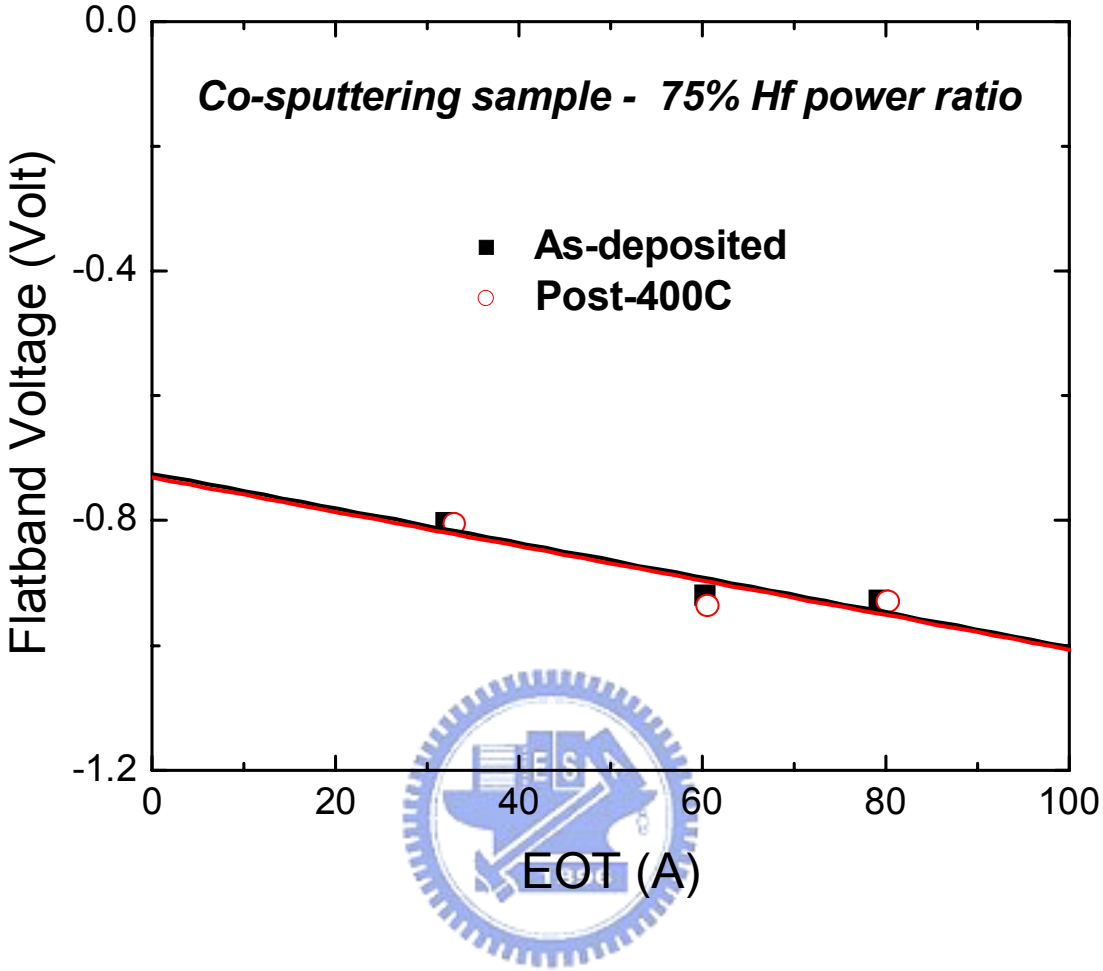

Fig. 2.6. Post-400℃ annealing co-sputtering sample shows negligible work function variation.

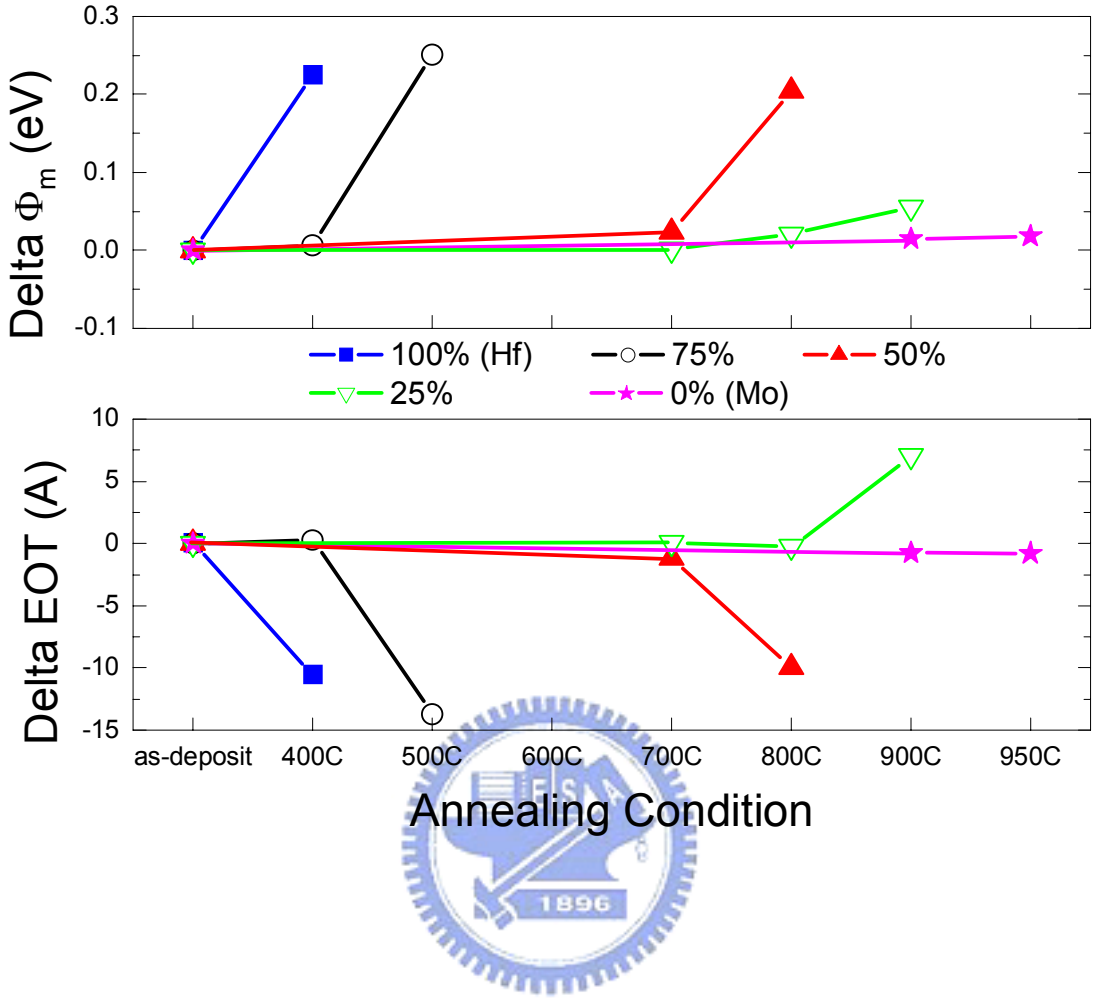

Fig. 2.7. The dependence of Φ_m and EOT variation on annealing temperature show that the thermal stability of alloy samples can be at least higher than 400℃.

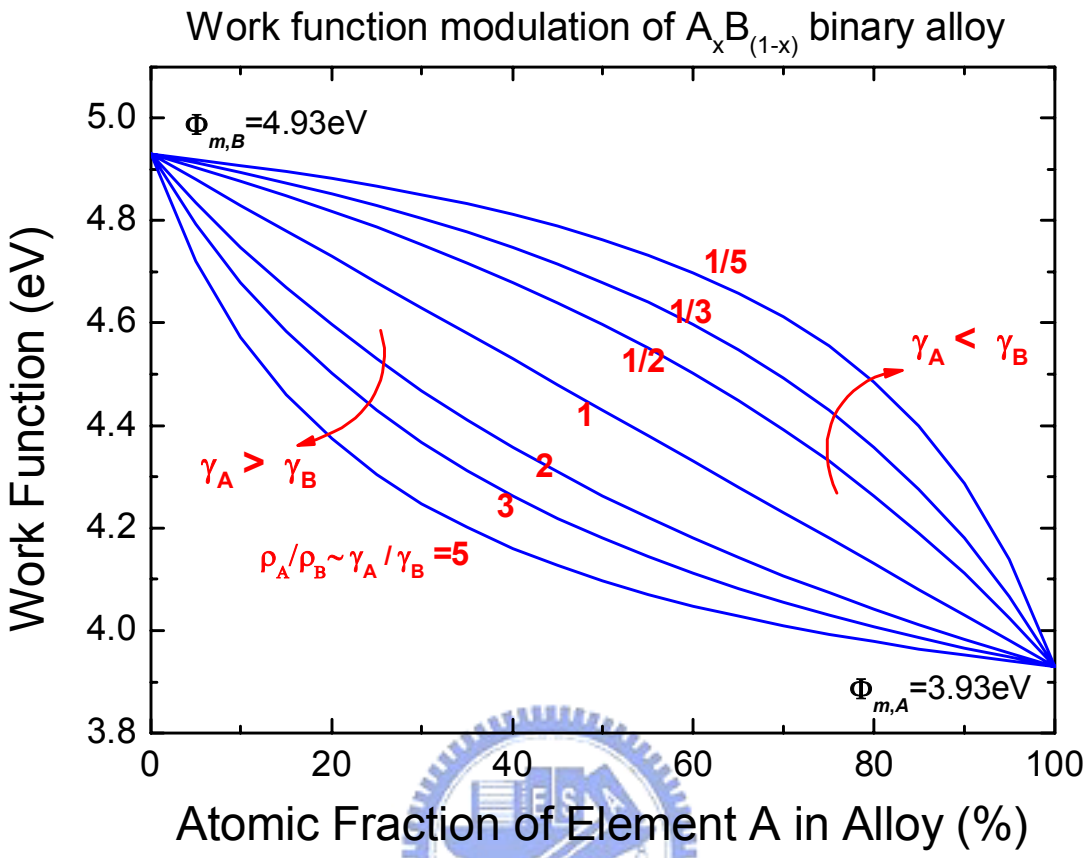

Fig. 2.8. Calculated work function value versus atomic fraction in binary alloy as a function of γ ratio. Metals with similar γ (Sommerfeld factor) will lead to a linear work function modulation which is a compromise between modulation efficiency and immunity to process variation. ($\Phi_{m.A}$ and $\Phi_{m.B}$ are set to be 3.93 and 4.93eV for convenience)

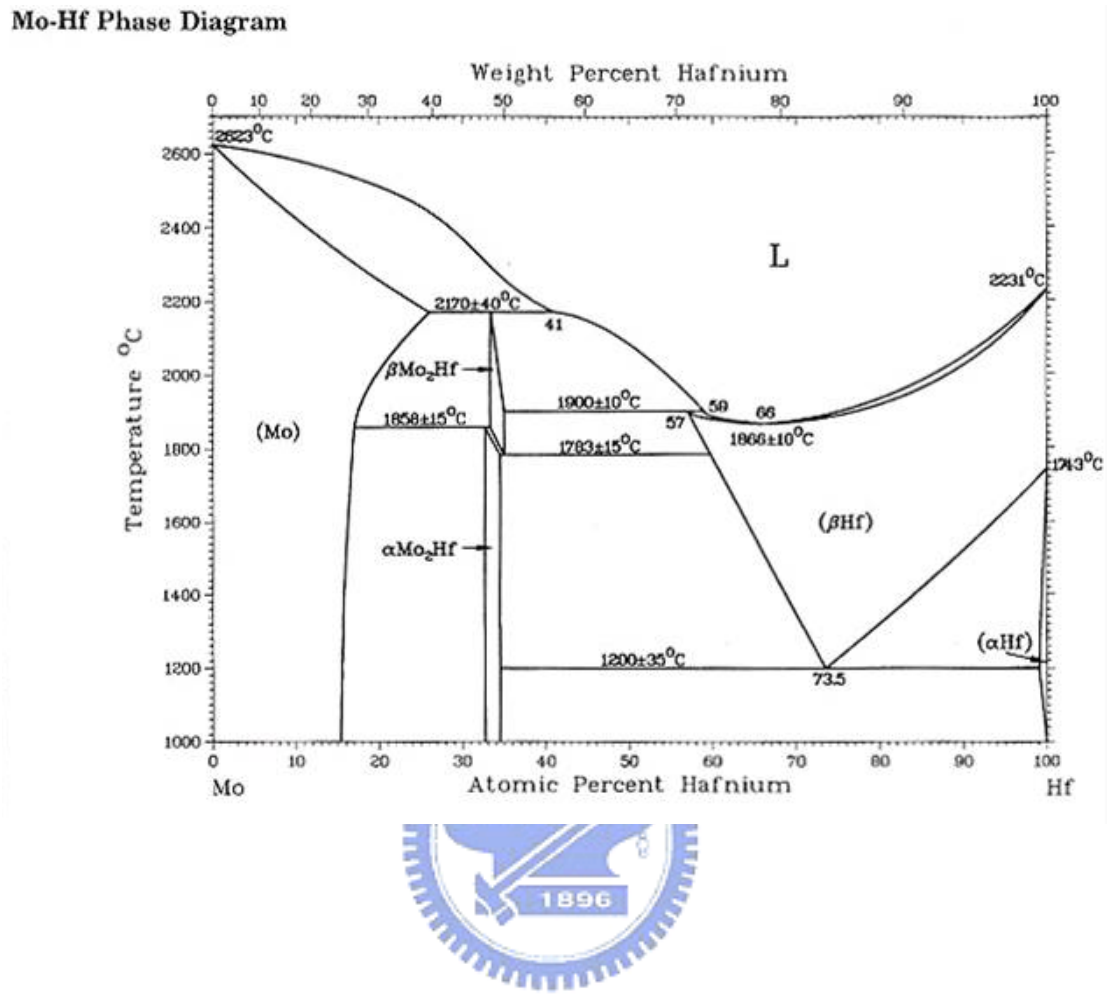

Fig. 2.9. The phase diagram of Mo-Hf system.

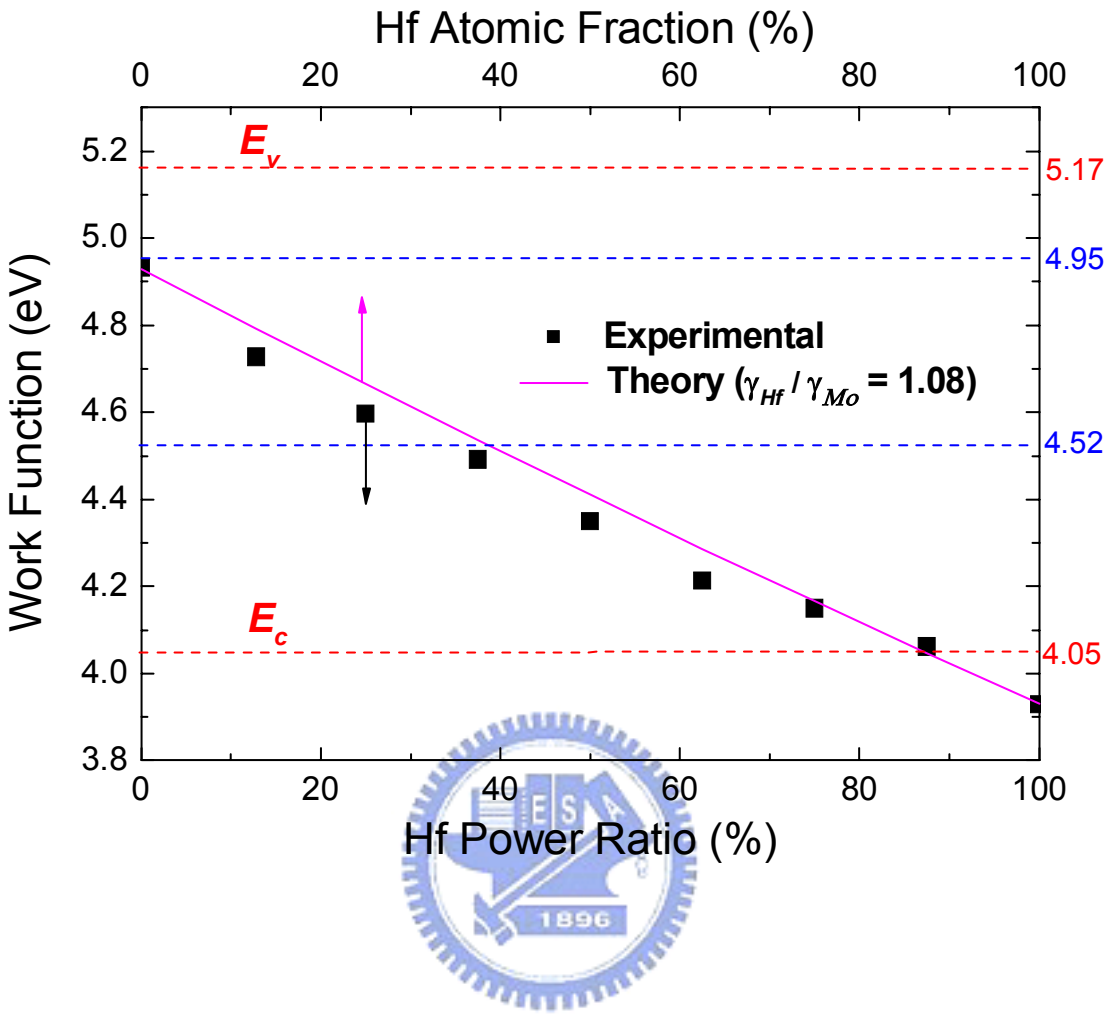

Fig. 2.10. Comparison between experimental (Table I.) and theoretical work function values. A slightly deviation in lower Hf power ratio regime may be attributed to different sputtering rate between Hf and Mo. (γ_{Hf} = 2.16, γ_{Mo} = 2.0 are used for calculation)

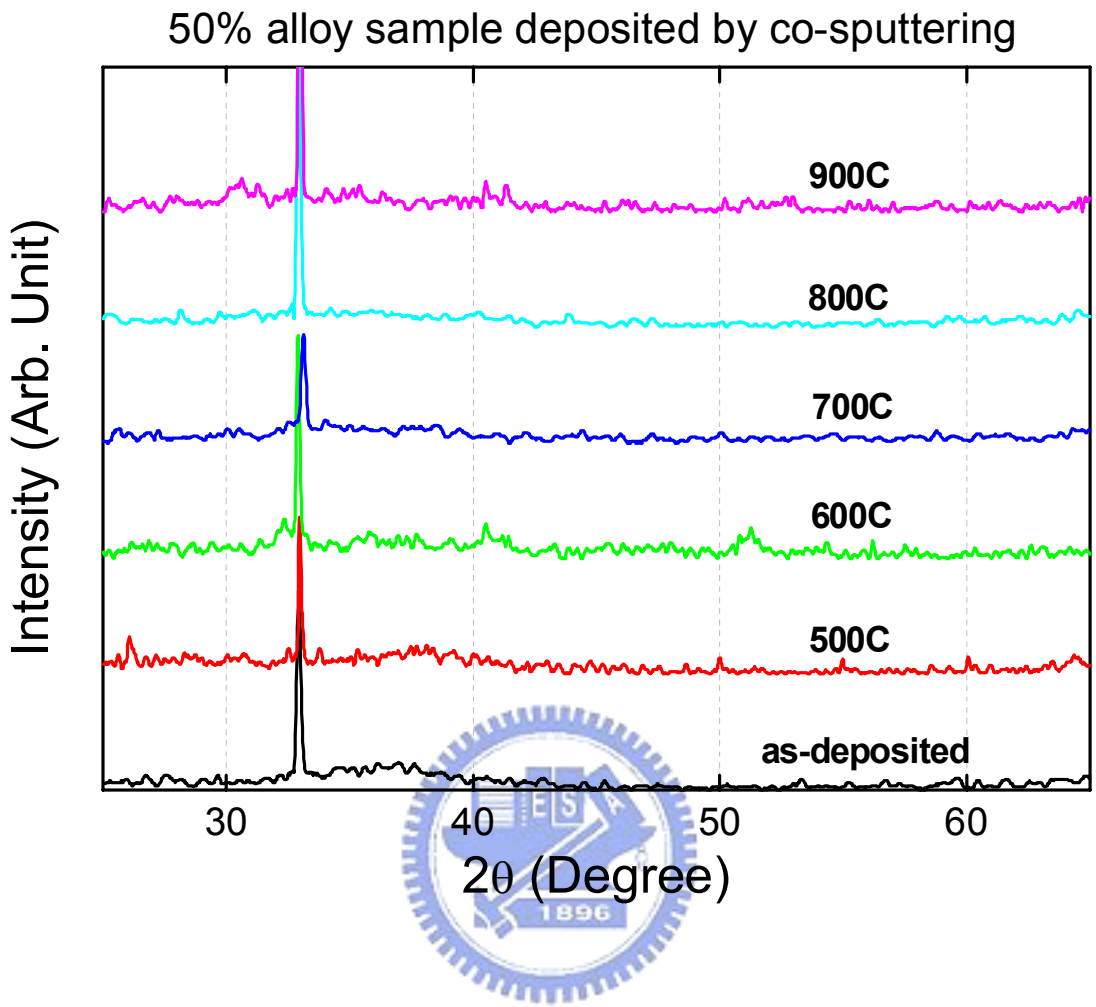

Fig. 2.11. XRD spectra of 50% Hf power ratio co-sputtering sample exhibited an amorphous film structure and only the *c*-Si was featuring.

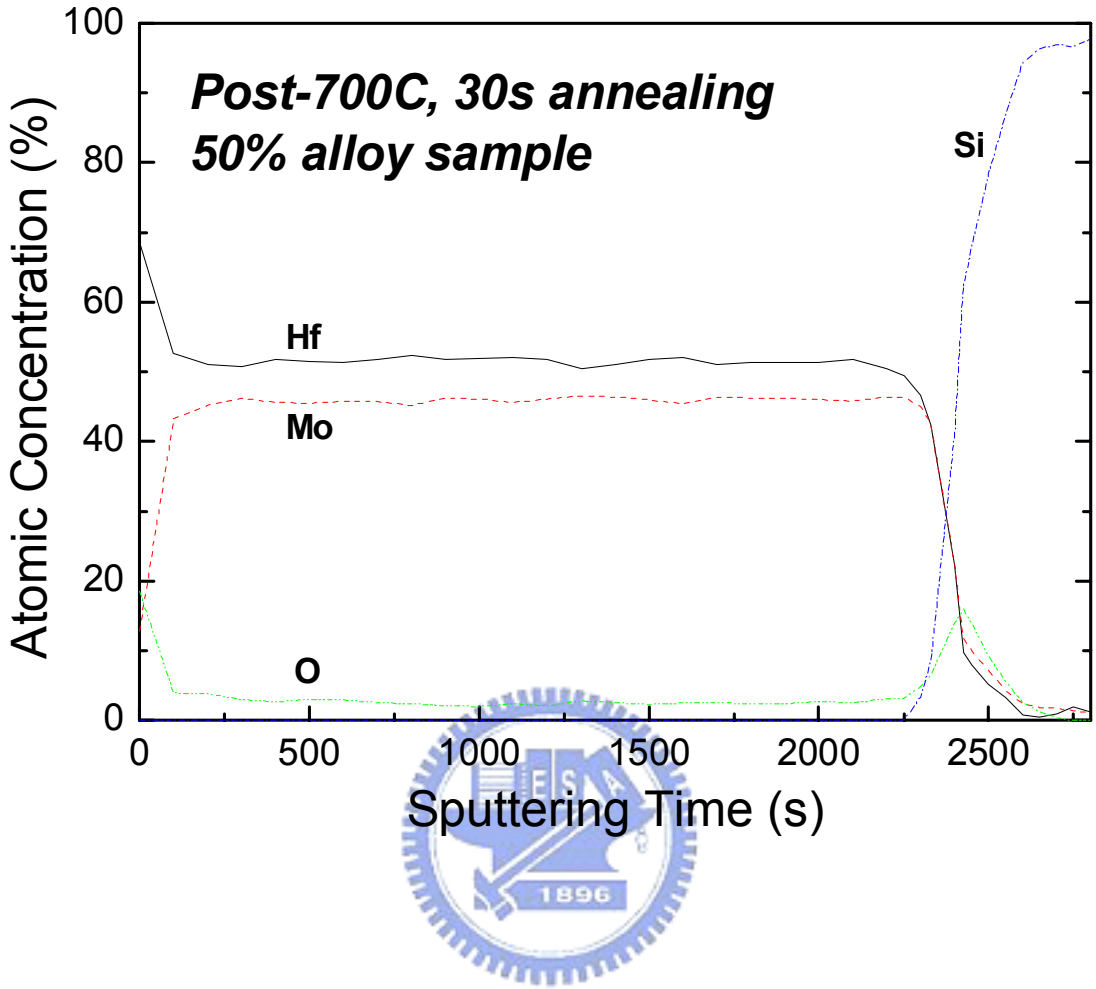

Fig. 2.12. AES profile of post-annealing 50% Hf power ratio co-sputtering sample. A uniform composition and abrupt interface can be observed.

Chapter 3

Integratable Dual Metal Gate Technology Using $Hf_xMo_{(1-x)}$ Binary Alloys

3.1 BACKGROUNDS AND MOTIVATION

In the previous chapter, the almost linear and continuous work function modulation behavior of Hf-Mo binary alloys is demonstrated. In the view of process integration, a suitable integration technique should be introduced to avoid the process induced gate dielectric integrity degradation.

Here we propose a dual metal gate technology which employs Mo and $Hf_xMo_{(1-x)}$ as gate electrodes for *p*- and *n*-channel devices, respectively. In this case, the $Hf_xMo_{(1-x)}$ electrode in the proposed dual metal gate technology is formed by metal intermixing. Metals need not to be removed from the dielectric interface so that the uniformity and integrity of gate dielectric can be preserved. Furthermore, a parameter called the optimal annealing temperature, $T_{A,opt}$, is expected to provide a prospective work function modulation without causing the EOT variation. The value of $T_{A,opt}$ will strongly affect the application of the proposed technique.

Moreover, since the phenomenon of metal intermixing is based on solid diffusion, we demonstrate that the optimal annealing temperature, $T_{A,opt}$, can be raised by increasing the total metal thickness ($T_M = T_{Hf} + T_{Mo}$). Consequently, it is likely to

overcome the thermal stability issue in conventional CMOS process by using an appropriate metal thickness. In addition, the composition and work function of $Hf_xMo_{(1-x)}$ are demonstrated to depend on the thickness combination of metal layers. At the top surface of the gate electrode, the oxidation of Hf which will lead to an extra Hf consumption was observed. A modified multilayer structure (TiN/Mo/Hf/Mo) was fabricated and verified to improve the immunity to metal oxidation. In addition, a quadratic equation relating the work function (Φ_m) to composite metal thickness ratio ($T_R = T_{Hf} / T_{Mo}$) is also derived. Good consistency with the experimental data assures the possibility of precise metal work function adjustment.

3.2 EXPERIMENT

Figure 3.1 shows a practicable fabrication process for the proposed dual metal gate technology that uses Mo and $Hf_xMo_{(1-x)}$ as gate electrodes. After LOCOS isolation and the gate dielectric deposition, the first layer metal Mo and the second layer metal Hf are deposited over the entire wafer. A non-critical lithography step is performed and the second layer metal Hf is then selectively removed from the PMOS side. After gate electrodes patterning and S/D implantation, the thermal annealing is performed for dopant activation and metal intermixing at the NMOS side simultaneously.

To demonstrate this technique, MOSCAP devices were fabricated. The process flow is similar to that of co-sputtering experiment, except that Mo and Hf are deposited in sequence. The Mo gate has been reported to possess high thermal stability (> 1000℃) on SiO_2 gate dielectric [1]. Moreover, the work function value of

Mo film varies with the bulk metal microstructure and consequently depends on deposition and annealing conditions [2]. The Mo film with (110) orientation has been reported to maintain possessing high work function value suitable for p-channel devices up to 900℃ [3]. By contrast, the poor thermal stability of pure Hf gate on SiO_2 has been reported [4]. Therefore, Mo is used as the first layer metal to retard the unwanted interaction between metal and SiO_2 during the subsequent thermal treatment. The composition of binary alloy is modulated by varying the thickness of each metal layer as listed in Table 3.1. The Hf atomic fraction in each $Hf_xMo_{(1-x)}$ alloy is approximately predicted by

$$x / (1-x) = 9.38\ T_{Hf} / 13.44\ T_{Mo} \qquad (2.1)$$

In eq. (2.1), factors of 13.44 and 9.38 are the molar volume of Hf and Mo, respectively. After gate electrode patterning, samples were then subjected to different rapid thermal annealing conditions in N_2 ambient to lead to metal intermixing for alloy formation and simulate the possible thermal cycle in the conventional CMOS process.

3.3 RESULTS AND DISCUSSION

Figure 3.2 shows the C-V characteristics of an MOSCAP gated by Hf/Mo metal stack before and after the rapid thermal annealing. The C-V results shows that the nearly optimal annealing temperature ($T_{A,opt}$) for the 50% sample is 600℃. A sufficient and prospective metal work function modulation can be achieved without the noticeable EOT variation. By contrast, smaller flat band voltage shift for

annealing temperature lower than 600℃ may be due to the insufficient thermal budget needed for expected Hf concentration diffusion to the dielectric interface. As for annealing temperature higher than 600℃, a noticeable capacitance decrease which is different with the observation in co-sputtering experiment can be observed. The abnormal increase in EOT might be attributed to the contribution of series capacitance due to metal oxidation and should be verified further.

In view of process integration, lower $T_{A,opt}$ will restrict the proposed technique to the gate-last process where high temperature annealing for S/D dopant activation will be performed prior to the deposition of gate dielectric and gate electrode. It should be noted that the summation of metal thickness is kept constant (500Å) for each sample as listed in Table 3.1. Since the phenomenon of metal intermixing is based on solid diffusion, the increase of first-layer metal thickness as well as the total metal thickness ($T_M = T_{Hf} + T_{Mo}$) under the same thickness ratio can be expected to raise the required thermal budget for prospective work function modulation. An investigation about the influence of the total metal thickness, T_M, on the optimal annealing temperature, $T_{A,opt}$, is shown in Fig. 3.3. Although the result for sample with total metal thickness of 1500Å is not optimized yet, a positive correlation can be observed. When the total metal thickness is increased from 500Å to 1500Å, the optimal annealing temperature for the 50% sample is raised from 600℃ to 900℃ substantially. Consequently, one can possibly get around the thermal stability issue by using an appropriate total metal thickness corresponding to the total thermal budget subsequent to the gate electrode deposition.

According to the ITRS roadmap, however, the thickness of the gate electrode must be reduced with the miniaturization of MOSFET devices. To use thicker metal

thickness, an additional etch-back of the gate electrode would be required after the finish of metal intermixing. The gate electrode thin-down process without serious increase of the process complexity can be possible. For instance, one can employ the interlevel dielectric (ILD) CMP for gate electrode etch-back, and only the polish-time control is needed to achieve a prospective gate electrode thickness as shown in fig. 3.4. Compared to the gate-last process [5], the dummy gate removal, gate electrode re-deposition and the gate electrode CMP are not required.

The work functions of $Hf_xMo_{(1-x)}$ formed by metal intermixing are listed in Table 3.1 (optimal annealing temperature: 700℃, 30s for sample 2-1 and 2-2; 600℃, 30s for samples 2-3 and 2-4). The dependence of work function value on the thickness combination of the two metal layers can be observed. Figure 3.5 shows the dependence of post-annealing capacitor-voltage characteristics on the Hf atomic fraction calculated by eq. (2). Figure 3.6 shows the dependence of extracted work function values on the Hf atomic fraction. A parallel shift of post-annealing work functions from the calculated values can be observed. This may be attributed to the extra consumption of Hf (~3%) due to surface oxidation. In Fig. 3.7, the XRD result exhibits the HfO_2 peak and demonstrates the speculation. With eq. (1.1) and eq. (2.1), one can obtain the following quadratic equation:

$$(1.053\Phi_m - 4.136)\ T_R^2 + (2.904\Phi_m - 12.808)\ T_R + (2\Phi_m - 9.86) = 0 \quad (2.2)$$

Here T_R is the thickness ratio of Hf to Mo ($T_R = T_{Hf} / T_{Mo}$). If the extra consumption of Hf (~3%) due to surface oxidation is taken into account, the eq. (2.2) becomes:

$$(1.05\Phi_m - 4.156)\ T_R^2 + (2.897\Phi_m - 12.864)\ T_R + (1.995\Phi_m - 9.89) = 0 \quad (2.3)$$

Figure 3.8 shows the dependence of the work function on the thickness ratio. Also shown are the calculated results of eq. (2.2) and eq. (2.3). A strong consistency assures the possibility of precise work function tuning since the T_R value required for an expected Φ_m can be precisely determined. Furthermore, to overcome the surface oxidation of Hf, MOS capacitors with triple layer metal stack (Mo/Hf/Mo) capped by TiN (20nm) were also fabricated and subjected to the same annealing conditions in the two-layer experiments. The extracted work function values are labeled in fig. 3.6 and fig.3.8. In the multilayer experiments, the thickness of Mo in the two-layer experiment is split into 10nm as first-layer metal and the remnant Mo is deposited atop Hf. Using the multilayer structure, the immunity against surface oxidation can be improved effectively. The extracted work functions will be recovered to the prospective values and can be described accurately by eq. (2.2).

3.4 SUMMARY

For the ease of process integration, $Hf_xMo_{(1-x)}$ formed by metal intermixing is evaluated, and a novel dual work function metal gate technology is proposed and demonstrated. One can be allowed to get around the thermal stability issue by using an appropriate metal thickness (T_M) and possess precise controllability of metal work function by adjusting the composite metal thickness ratio (T_R). This technique is not only attractive but especially important for FinFET and/or UTB-MOSFET devices application.

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Sample	T_{Mo} (Å)	T_{Hf} (Å)	Hf atomic fraction (%)	Φ_m (eV)
ctrl.	500	0	0 (pure Mo)	4.93
2-1	406	94	14	4.81
2-2	294	206	33	4.63
2-3	256	244	40	4.55
2-4	205	295	50	4.43

Table 3.1.Sample conditions and extracted Φ_m of metal intermixing experiment. (700 ℃, 30s for sample 2-1 and 2-2；600℃, 30s for samples 2-3 and 2-4)

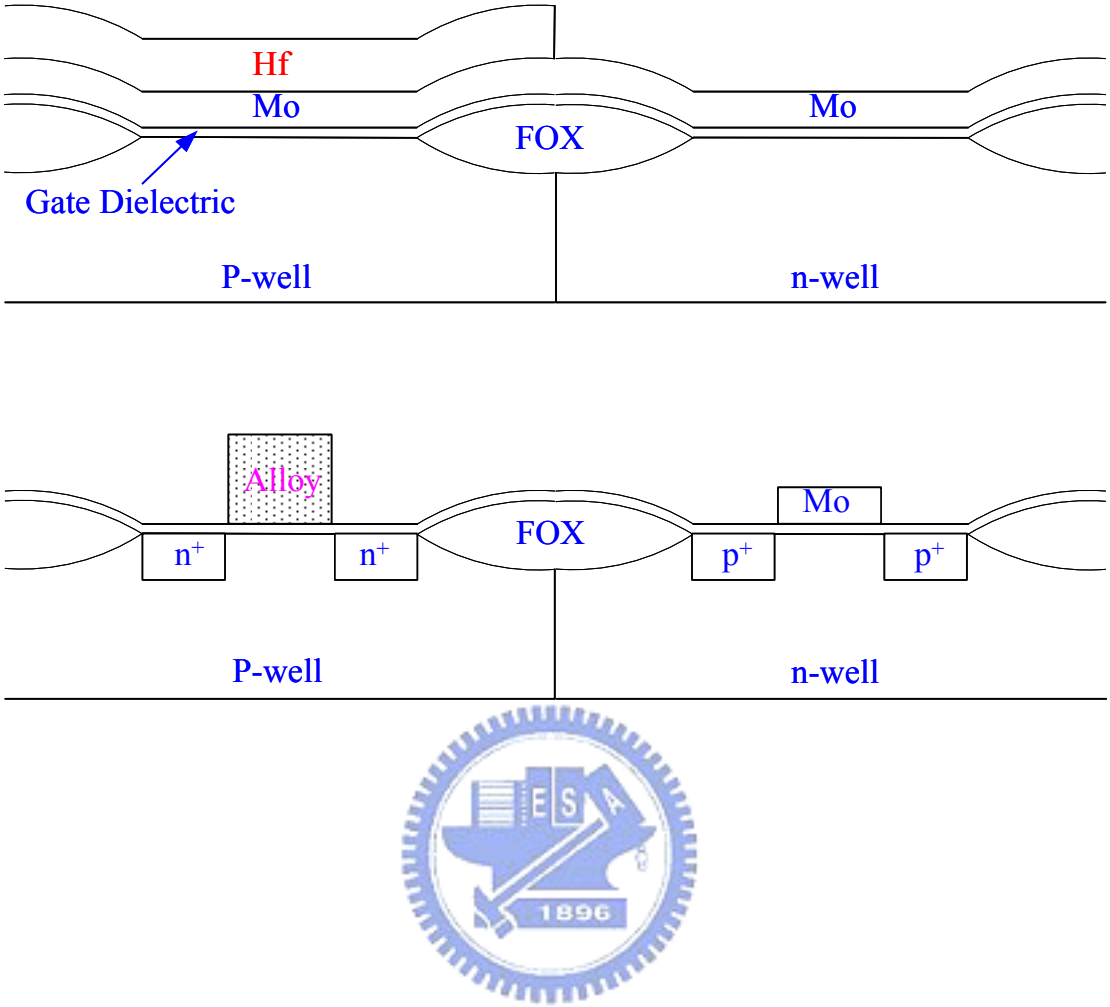


Fig. 3.1. Schematics of dual metal gate technology using metal and alloy formed by metal intermixing. Metals need not to be etched away from the dielectric surface so the uniformity and integrity of gate dielectric can be preserved.

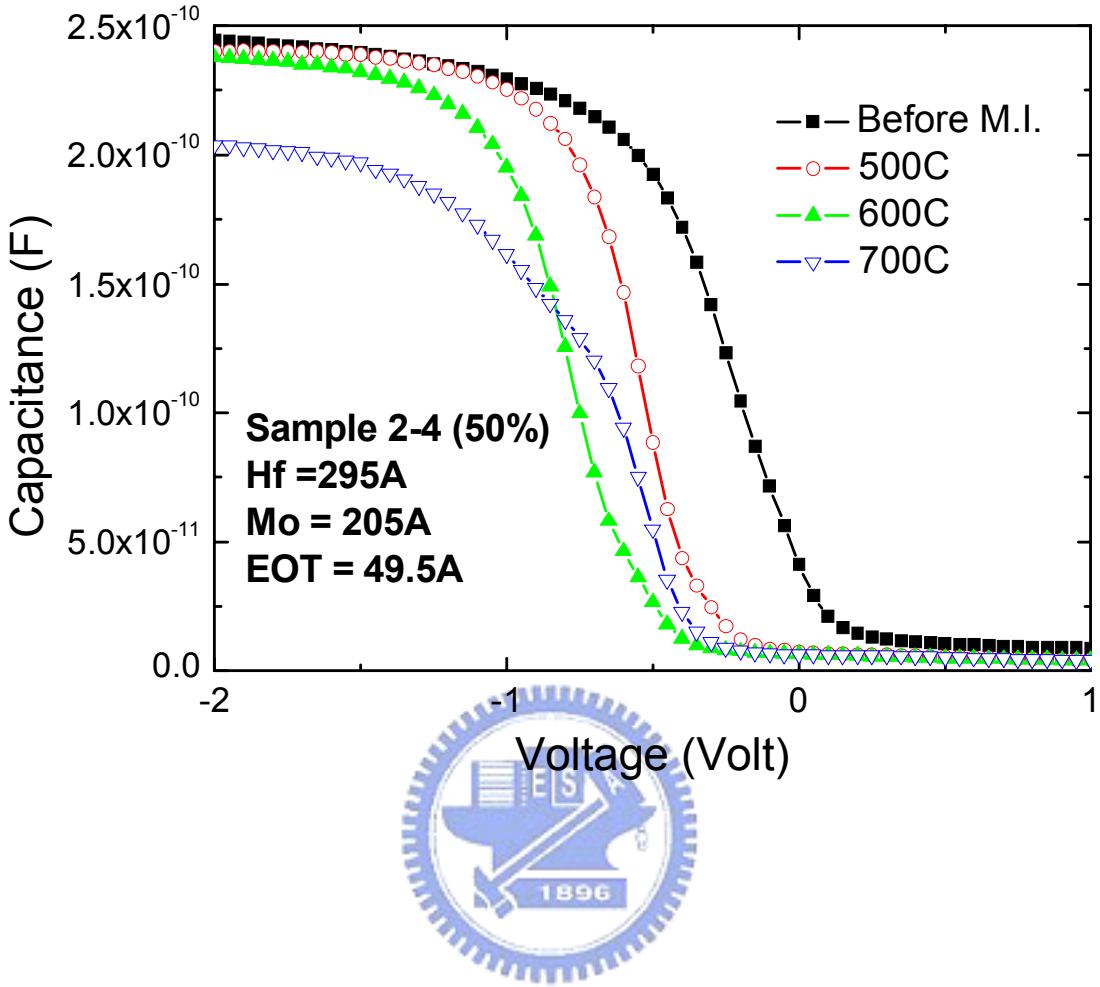


Fig. 3.2. C-V curves of Hf-295Å/Mo-205Å/SiO_2 capacitor before and after thermal annealing. The optimal annealing temperature for this sample was found to be 600℃.

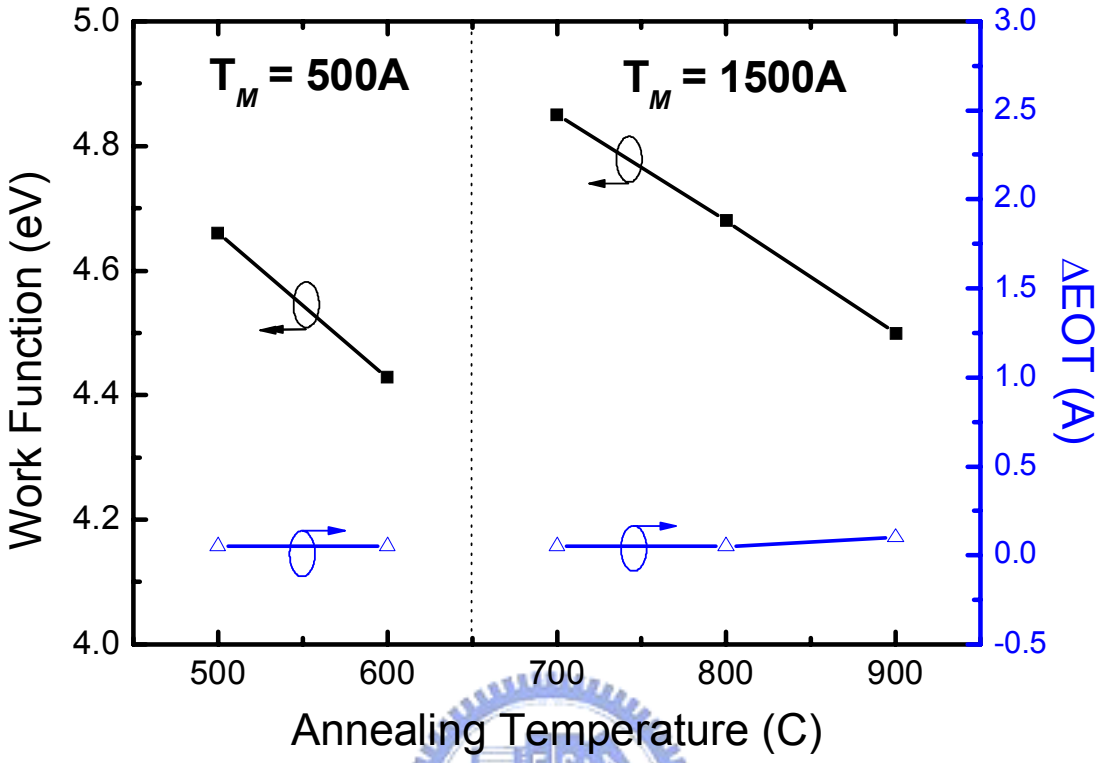


Fig. 3.3. The increase of total metal thickness under the same composite metal thickness ratio can effectively rise the optimal annealing temperature.

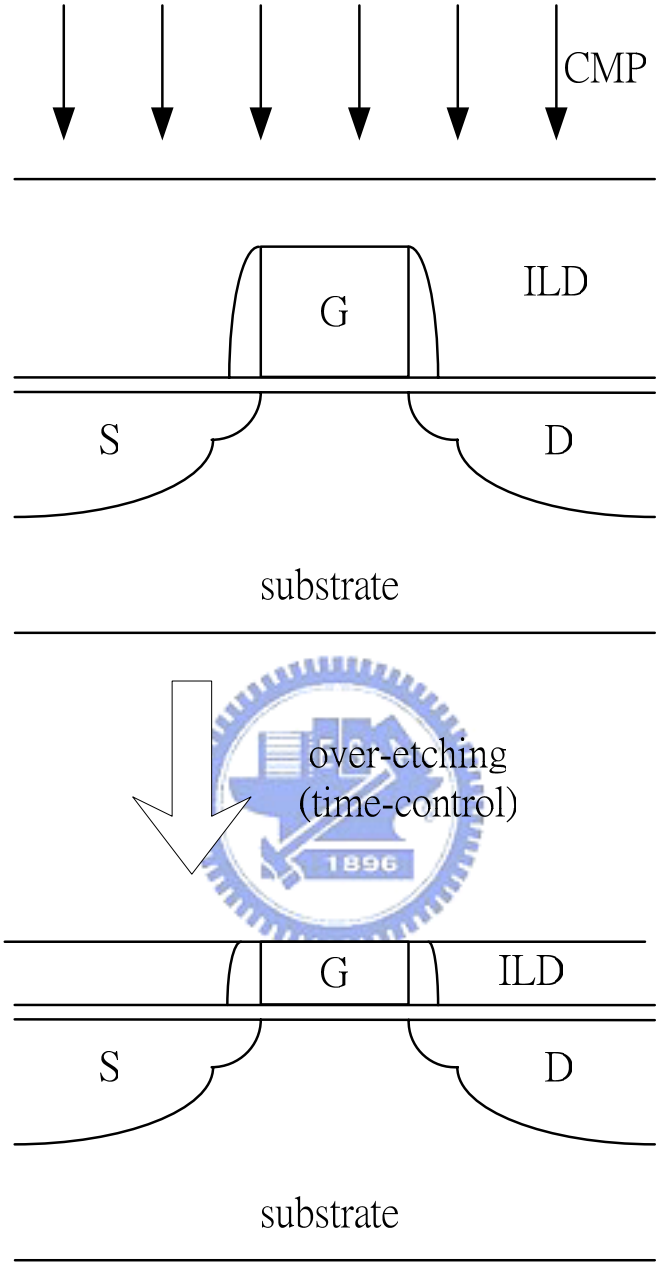


Fig. 3.4. Illustration of thinning down of the gate electrode using ILD CMP.

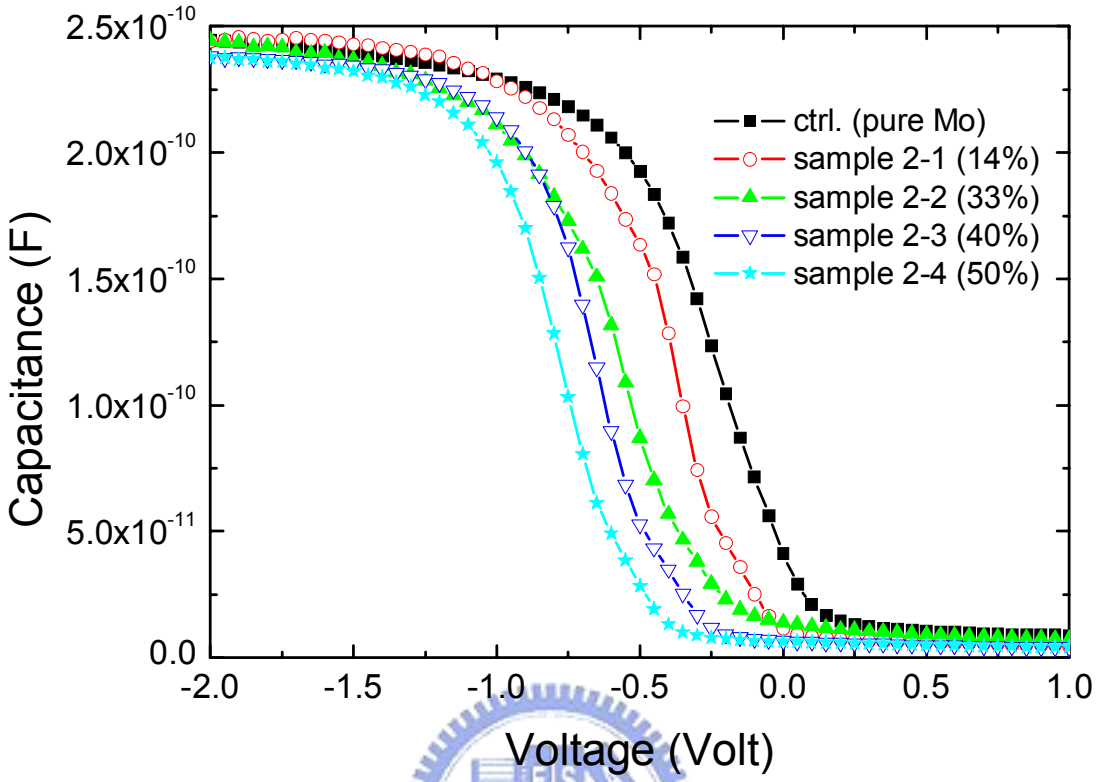


Fig. 3.5. C-V curves of post-annealing Hf/Mo/SiO_2 capacitors as a function of Hf atomic fraction.

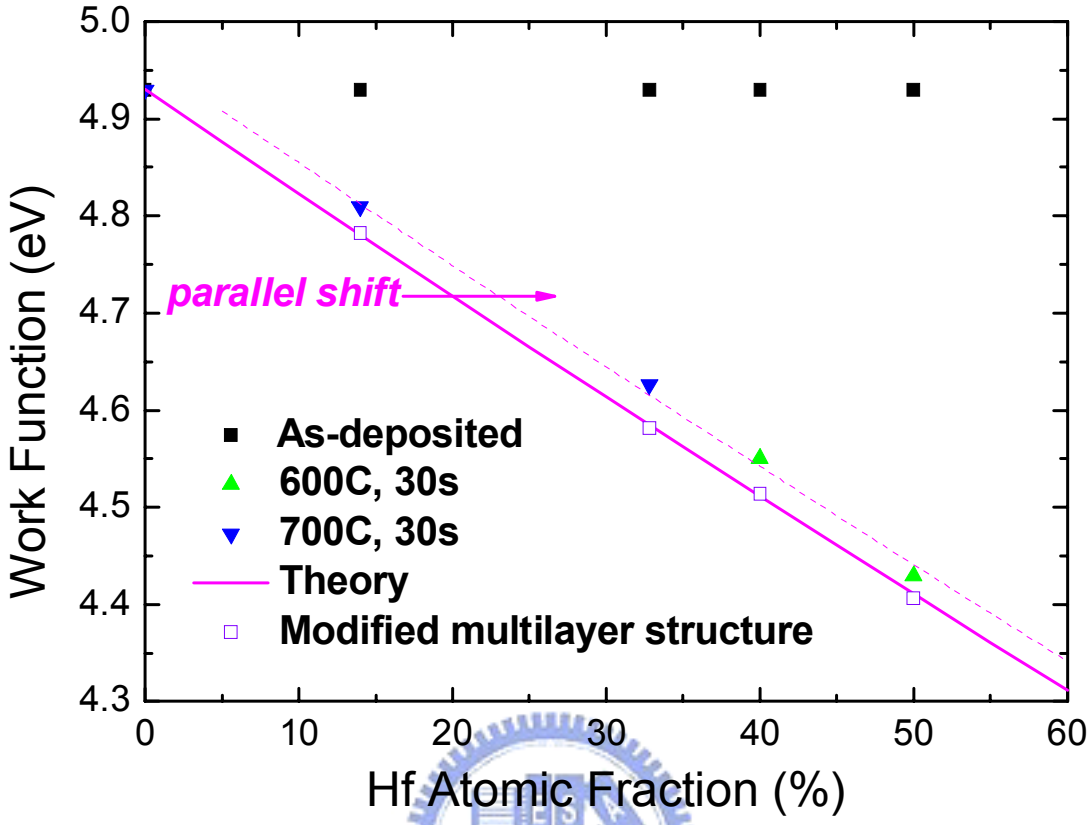


Fig. 3.6. Comparison between experimental (Table II.) and theoretical results. A parallel shift may be attributed to the extra Hf consumption (~3%) due to surface oxidation. Also shown as open symbols are experimental results of multilayer (TiN/Mo/Hf/Mo) gated devices, good agreement on theoretical results can be achieved.

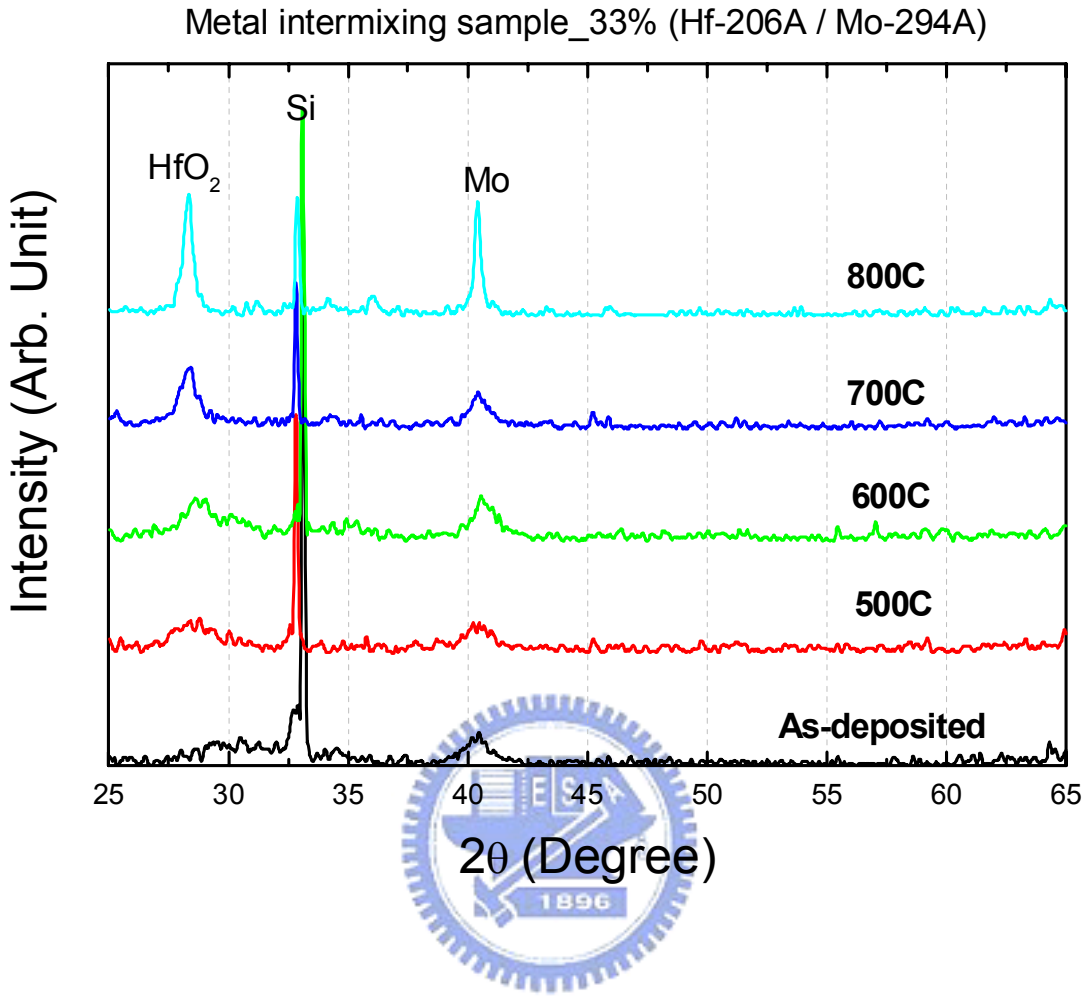


Fig. 3.7 XRD spectra of metal intermixing sample (Hf-206Å/Mo-294Å/SiO_2) exhibited HfO_2 peak as a result of oxidation of Hf at the top surface after thermal treatment.

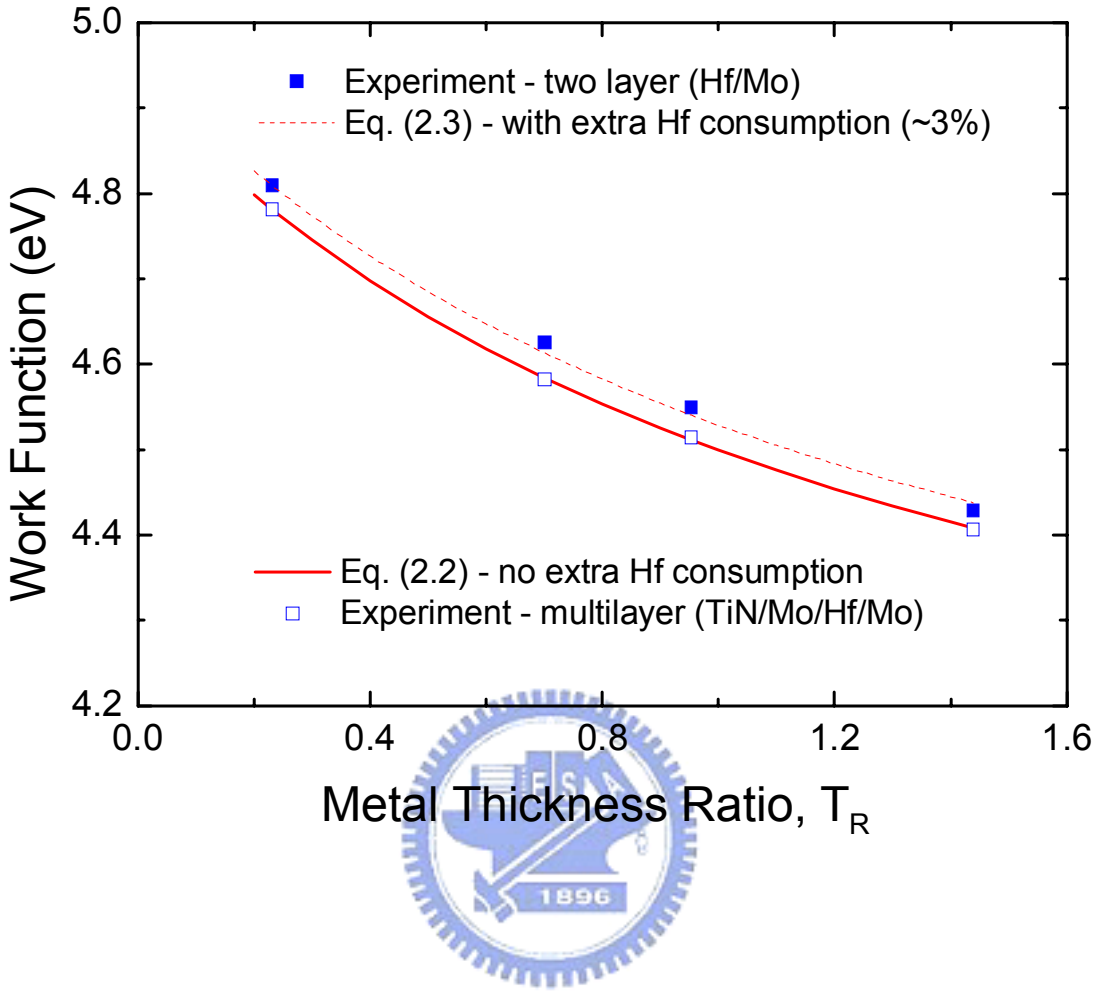


Fig. 3.8 Post-annealing work functions extracted from two-layer (Hf/Mo) and multilayer (TiN/Mo/Hf/Mo) gated MOSCAP versus the composite metal thickness ratio ($T_R = T_{Hf} / T_{Mo}$). Also shown are calculated results of derived quadratic equations with and without taking extra Hf consumption into account.

Chapter 4

Novel Dual Metal Gate Technology Using $MoSi_x$ Films

4.1 BACKGROUNDS AND MOTIVATION

According to the ITRS roadmap [1], the introduction of high-k gate dielectric materials and dual metal gate electrodes with appropriate work functions will be required in the near future to reduce gate leakage current [2]-[4] and eliminate boron penetration and poly depletion effect [4], [5]. For conventional bulk devices, the required work functions (Φ_m) of *n*- and *p*-channel devices are about 4eV and 5eV, respectively. However, the required Φ_m values for *n*- and *p*-channel devices with advanced transistor structures, such as FinFET or ultra-thin-body (UTB) MOSFETs, are about 4.4-4.6eV and 4.8-5.0eV, respectively [6]. Since the work function of the metals cannot easily be modulated, a straightforward dual metal gate CMOS process has been proposed, but it degrades the integrity of the gate dielectric by exposing it to the metal etchant [7].

To preserve the gate dielectric integrity, the first layer metal which is deposited atop the gate dielectric should not be etched away so that the gate dielectric can be protected without exposing to the metal etchant. In this case, the work function of the deposited first layer metal in either NMOS side or PMOS side should be modulated to accomplish the dual work function metal gate technology and provide low and

symmetric threshold voltages for CMOS devices. In addition to the alloy formation mentioned in the previous chapter, the silicidation process may also possess a possibility of metal work function modulation. The straightforward dual work function metal gate technology based on silicides is shown in fig. 4.1. Atop the polysilicon gates, different metals are deposited followed with high temperature annealing to form silicides. The work function values of formed silicides depend on the chosen metal candidates. Unfortunately, most metal silicides are found to possess midgap work function values so that it is difficult to possess large enough work function difference using this approach.

A novel dual metal gate technology based on the full silicidation (FUSI) of polysilicon gates has also been reported [8]-[10] as shown in fig. 4.2. The front end process is the same with the traditional dual-doped polysilicon gates CMOS technology while the conventional salicide process is modified. The metal layer thicker than required for conventional salicide process will be deposited to allow for full silicidation of the polysilicon gates. In this case, dopants in the polysilicon are believed to be responsible for providing the difference between the work functions of *n*- and *p*-type metal-silicide (MeSi) gates [11], [12]. Both the source/drain dopant activation annealing and the silicidation anneaing contribute to the dopant redistribution. The major advantage of the FUSI method is the ease of process integration. Moreover, since the source/drain dopant activation annealing will be performed prior to silicide formation, the requirement for the thermal stability of MeSi can be alleviated. Thermal treatment prior to silicidation process, however, results in the incomplete elimination of boron penetration in *p*-channel devices [13]. A noticeable boron penetration will take place during the high temperature annealing for S/D activation.

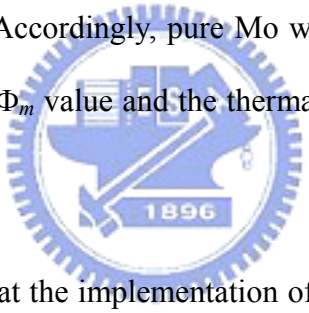
This work proposes the use of a combination of Mo-$MoSi_x$ gate electrodes for dual metal gate technology. In view of process integration, the $MoSi_x$ gate was formed by the full silicidation of the α-Si/Mo/gate dielectric stack to prevent the exposure of the gate dielectric in the channel region to metal etchant. Extracted Φ_m values for $MoSi_x$ and as-deposited pure Mo gates on SiO_2 are appropriate for devices with advanced transistor structures. The small increase in Φ_m and the negligible variation in EOT after RTA at 950℃ demonstrate the superior thermal stabilities of Mo and $MoSi_x$ on SiO_2. To expand the application of our proposed novel dual metal gate technology, the introduction of *n*-type metal silicide was also investigated. An additional arsenic pre-implantation prior to silicidation annealing was used for *n*-type metal silicide formation. Extracted Φ_m values for *n*-type $MoSi_x$ and as-deposited pure Mo gates on SiO_2 are found to be suitable for conventional bulk devices. The use of Mo-$MoSi_x$ gate electrodes combination effectively solves the problems encountered in the FUSI method, and the possessed work function combination can be suitable for devices with advanced transistor structures and conventional bulk devices if additional arsenic pre-implantation prior to silicide annealing was performed.

4.2 EXPERIMENT

Fig. 4.3 schematically depicts the proposed novel dual metal gate technology that combines metal and metal silicide. The first layer metal and α-Si are deposited over the entire wafer in sequence on the gate dielectric. A non-critical lithography step is performed and an appropriate wet etching recipe should be investigated to remove selectively the α-Si from the *p*-MOS side. Since only Mo remains in the *p*-MOS region, it solely determines the work function of the *p*-MOS gate electrode. The

remaining α-Si/Mo stack in the *n*-MOS region will be subsequently transformed into molybdenum silicide and determine the work function of the *n*-MOS gate electrode. In this process, the gate dielectric in the channel region will not be exposed to the metal etchant so the side-effects encountered in the straightforward dual metal gate technology [7] can be prevented.

It is worth to note that the thermal stability of the selected metal film on the gate dielectric should be sufficiently high to ensure that no interaction occurs between metal and the gate dielectric during the silicidation and following high temperature processes. The (110) Mo gate has been reported to have a work function that is appropriate for *p*-channel device [14], and exhibit high thermal stability (1000℃) on the SiO_2 gate dielectric [15]. Accordingly, pure Mo will be adopted as the first layer metal in this work so that the Φ_m value and the thermal stability of the formed $MoSi_x$ become the main issue.



It is also worth to note that the implementation of the proposed novel dual metal gate technology will be more complex than the schematic illustration shown in fig. 4.3. For instance, the re-deposition of Mo in the *p*-MOS region is needed after the selective removal of α-Si, to equalize the thickness of the gate electrode across the entire wafer. Consequently, potential gate patterning and spacer formation challenges can be prevented. For this reason, a more practical integration process is also proposed as shown in fig. 4.4.

To evaluate the proposed concept, the electrical characteristics of Mo and $MoSi_x$ gates were extensively investigated. MOS capacitors with Mo/SiO_2/*n*-Si and α-Si/Mo/SiO_2/*n*-Si structures were fabricated on 6-in Si wafers. After LOCOS isolation, thermal SiO_2 (3nm, 6nm, 9nm) was deposited as the gate dielectric.

According to the ITRS roadmap, the thickness of the gate electrode must be reduced as the MOSFET devices are miniaturized. To meet this criterion, a thin (10nm) layer of Mo was sputter-deposited on top of the gate dielectrics for all samples. Some samples were followed by sputter-deposition of α-Si (25nm). Gate electrodes were then patterned by reactive ion etching (RIE) using Cl_2-based chemistry. Following gate electrode patterning, some of the samples with an α-Si/Mo/SiO_2 stack were then subjected to arsenic implantation ($1x10^{15}$, $5x10^{15}cm^{-2}$). The low implantation energy (10KeV), corresponding to a projected implant range (R_p) value of one half of the thickness of the α-Si layer, was employed to avoid the direct implantation of dopants into the channel region. Samples with an α-Si/Mo/SiO_2 stack were then subjected to successive rapid thermal annealing (600℃, 1 min. + 700℃, 1 min. + 800℃, 1 min.) in N_2 ambient for $MoSi_x$ formation. All samples were then subjected to 950℃ RTA for 30s to evaluate the thermal stabilities of gate electrodes. The flat band voltage (V_{FB}) and equivalent oxide thickness (EOT) were extracted from the measured C-V curve using the quantum mechanical C-V (QMCV) simulator [16]. The Φ_m values of the gate electrodes were then extrapolated from the V_{FB}—EOT plots by setting the electron affinity (χ) of the Si substrate to 4.05eV.

4.3 RESULTS AND DISCUSSION

Before executing the major experiment, a test run for silicidation conditions was performed. MOS capacitors with α-Si/Mo/SiO_2/n-Si structures were fabricated on dummy wafers. The thickness of first layer Mo was kept constant as 10nm and the thickness of capped α-Si layer was split into 15nm and 25nm. The successive rapid

thermal annealing (RTA) was performed for silicidation of Mo layer. The result shows that samples with 15nm α-Si layer can not lead to noticeable flat band voltage shift, this may be attributed to insufficient silicon for full silicidation of Mo layer. On the other hand, samples with 25nm α-Si layer can exhibit negative flat band voltage shift under the same annealing condition as shown in fig. 4.5. This noticeable negatively flat band voltage shift may be attributed to the full silicidation of the Mo layer. Based on the above information, the thickness combination of α-Si/Mo stack used in the following experiment was decided. It is also worth to note that, similar experimental result can be obtained under the constant temperature RTA at 600℃ for longer than 30min in N_2 ambient, however, such a long annealing duration makes this silicidation condition not attractive.

Fig. 4.6 shows the C-V characteristics of MOSCAP devices gated by α-Si/Mo/SiO_2 stack before and after silicidation annealing. A negative post-silicidation flat-band voltage shift without EOT variation can be observed. The change in the work function of the gate electrode and the reduction of the fixed charge can contribute to the flat-band voltage shift.

Fig. 4.7 reveals that both as-deposited Mo/SiO_2 and post-silicidation α-Si/Mo/SiO_2 samples exhibit linear behavior in V_{FB}—EOT plots. The large fixed oxide charge density in the as-deposited Mo/SiO_2 sample may be caused by the damage done by sputtering and can be reduced by high-temperature annealing. The Φ_m values of the as-deposited pure Mo film and the formed $MoSi_x$ on SiO_2 are extracted to be 4.94eV and 4.38eV, respectively, so the Φ_m difference is 0.56eV. The possessed Φ_m value combination is suitable for devices with advanced structures.

For pure Mo gated MOSCAP devices, the dependences of the EOT variation and

the extracted work function value on annealing conditions are shown in fig. 4.8 and fig. 4.9, respectively. Similarly, the dependences of the EOT variation and the extracted work function value on annealing conditions for MOSCAP device with α-Si/Mo/SiO_2 structure are shown in fig. 4.10 and fig. 4.11, respectively. The small increase in Φ_m (Mo: 10meV; $MoSi_x$: 20meV) along with the negligible EOT variation (Mo: 0.08nm; $MoSi_x$: 0.06nm) after RTA at 950℃ demonstrate the excellent thermal stabilities of Mo and $MoSi_x$ films on SiO_2.

The constant voltage stressing (CVS) method was employed to generate the 10-year lifetime projections of Mo/SiO_2 (2.3nm) and post-silicidation α-Si/Mo/SiO_2 (2.4nm) devices at room temperature for oxide integrity evaluation. Figure 4.12 and 4.13 show that pure Mo and $MoSi_x$ gates have superior TDDB characteristics, respectively, after 950℃ RTA for 30s. Figure 4.14 compares the accumulation leakage current densities of Mo/SiO_2/*n*-Si and post-silicidation α-Si/Mo/SiO_2 devices to investigate further the possible metal interdiffusion into the oxide or channel region following high-temperature annealing. Both devices were annealed by 950℃ RTA for 30s, and $MoSi_x$/SiO_2 device exhibited slightly higher leakage current density than Mo/SiO_2 device. This increase in leakage current may be caused by the additional thermal budget required for the formation of metal silicide. Notably, pure Mo has been demonstrated as a p^+-polysilicon-compatible gate candidate for PMOS with negligible metal contamination and metal diffusion [17]. The comparable TDDB characteristics and leakage current densities of pure Mo and $MoSi_x$ gated devices also reveal that the silicidation process required for the formation of $MoSi_x$ will not severely degrade the device performance or oxide integrity.

$MoSi_2$ has been reported to be likely the only silicide phase observed for the

Mo:Si=1:2 stacked samples annealed at a temperature of higher than 600℃ [18]. MOSCAP devices gated by the sputtering deposition of $MoSi_2$ using the $MoSi_2$ target were also fabricated. The V_{FB} versus EOT plots of $MoSi_2/SiO_2/n$-Si and $MoSi_2/SiO_2/p$-Si structures yielded the work function of $MoSi_2$ film that was sputter-deposited on SiO_2 using the $MoSi_2$ target at 4.41eV, regardless of the dopant of the substrate, as shown in Fig. 4.15. Moreover, the x-ray photoelectron spectroscopy (XPS) analysis was also performed to estimate the chemical condition of the silicided film. Figure 4.16 and 4.17 compare the Si 2p and Mo 3d spectra of silicided films with those of pure Si and pure Mo, respectively. The binding energies that correspond to the Si 2p spectrum of pure Si and the silicided film obtained in this work were 99.4eV and 99.0eV, respectively. Similarly, the binding energies that correspond to the Mo 3d spectrum of pure Mo and the silicided film were 228.2eV and 228.0eV, respectively. Both the binding energy that corresponds to the Si 2p spectrum of the pure Si film and that which corresponds to the Mo 3d spectrum of the pure Mo film are strongly consistent with the reported handbook data [19]. Furthermore, a downward shift in binding energy of 0.4eV for silicided films is observed from the Si 2p spectra. The magnitude of this shift is close to the value previously reported for $MoSi_2$ (-0.3eV) [20]. Similarly, a downward shift in binding energy of 0.2eV for silicided films is observed from Mo 3d spectra, and the magnitude of the binding energy shift corresponds closely to previously reported values (-0.2eV) [21]. Accordingly, we speculate that $MoSi_2$ is the main constituent of the $MoSi_x$ film formed in this work and the full silicidation of the Mo layer is responsible for the large shift in the work function after silicidation annealing.

Fig. 4.18 indicates that post-silicidation α-Si/Mo/SiO_2 with and without arsenic pre-implantation exhibit linear V_{FB} versus EOT plots. A parallel shift in V_{FB} versus

EOT plot is observed. Evidently, the incorporation of low-energy arsenic pre-implantation indeed leads to the modulation of the work function, rather than the channel dopant-induced adjustment in the threshold voltage. Figure 4.19 summarizes the effect of the arsenic pre-implantation dosage upon the magnitude of the work function modulation. The extracted Φ_m values of $MoSi_x$ on SiO_2 with the pre-implantation of $1x10^{15}$ and $5x10^{15}$ cm^{-2} doses of arsenic are 4.19eV and 4.07eV, respectively. Although the introduction of arsenic impurities has been demonstrated to expand the difference between the Φ_m of $MoSi_x$ and pure Mo, and to extend the range of applications of the proposed approach from devices with advanced structures to conventional bulk devices, the exact mechanism of the modulation of work function by the pre-implantation of As is still under investigation.

The thermal stability of $MoSi_x$ with arsenic pre-implantation of $5x10^{15}$ cm^{-2} doses on SiO_2 are also evaluated at 950℃ for 30s. The dependences of the EOT variation and the extracted work function value on annealing conditions are shown in fig. 4.20 and fig. 4.21, respectively. The small decrease in Φ_m (42meV) along with the negligible EOT variation (0.02nm) after RTA at 950℃ for 30s demonstrates that the thermal stability of $MoSi_x$ on SiO_2 will not be degraded by the introduction of arsenic pre-implantation.

4.4 SUMMARY

A novel dual metal gate technology gated by Mo and $MoSi_x$ was proposed. On SiO_2 gate dielectric, Mo-$MoSi_x$ combination can be suitable for devices with advanced transistor structures. The thermal stabilities of pure Mo and $MoSi_x$ on SiO_2

also have been evaluated to be higher than 950℃. On the other hand, an additional arsenic pre-implantation prior to silicidation annealing can be used to expand the application of the proposed novel dual metal gate technology to the conventional bulk devices. The new structure along with the ruling out of *p*-type metal silicide can effectively eliminate the boron penetration encountered in the FUSI method.

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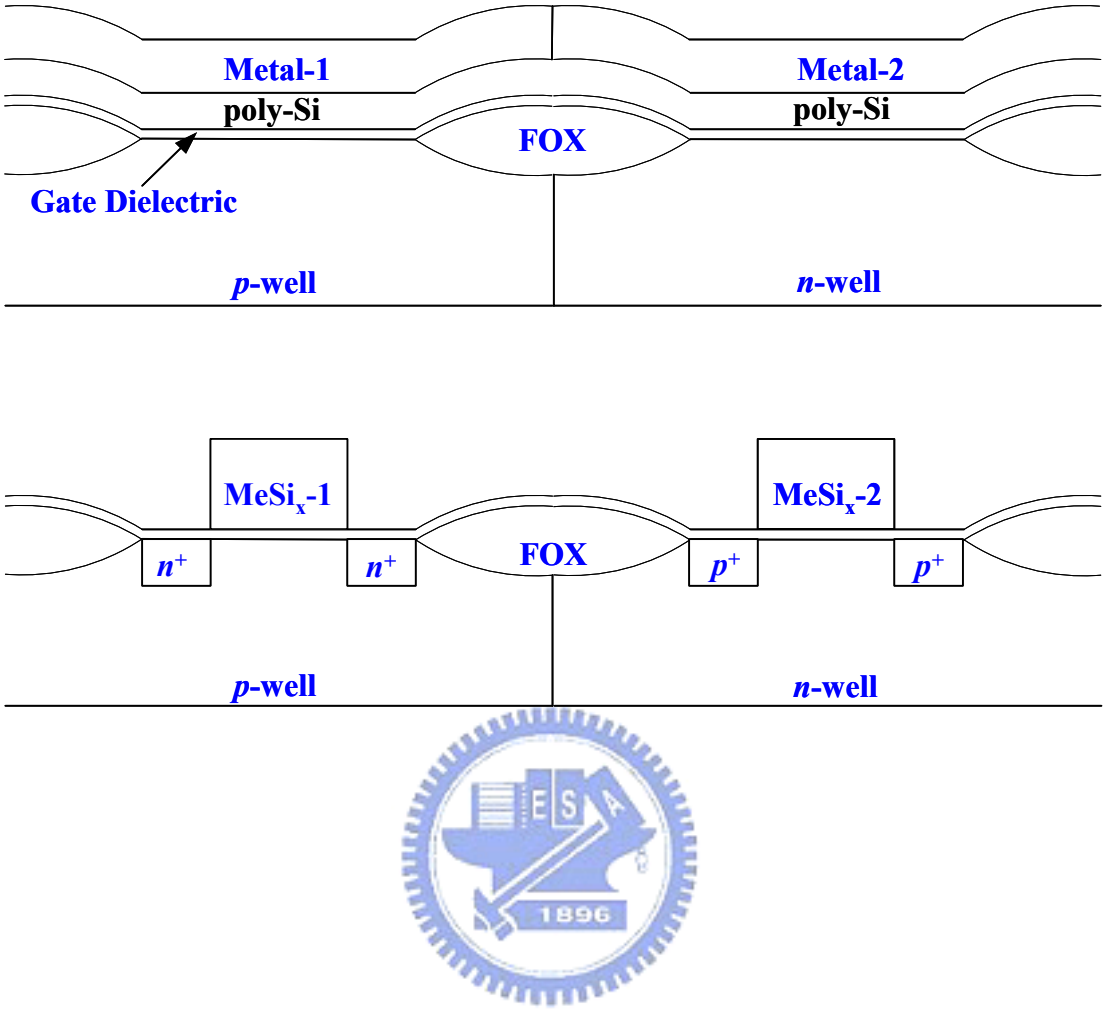

Fig. 4.1. The schematic illustration of dual metal gate technology gated by the combination of different metal silicides.

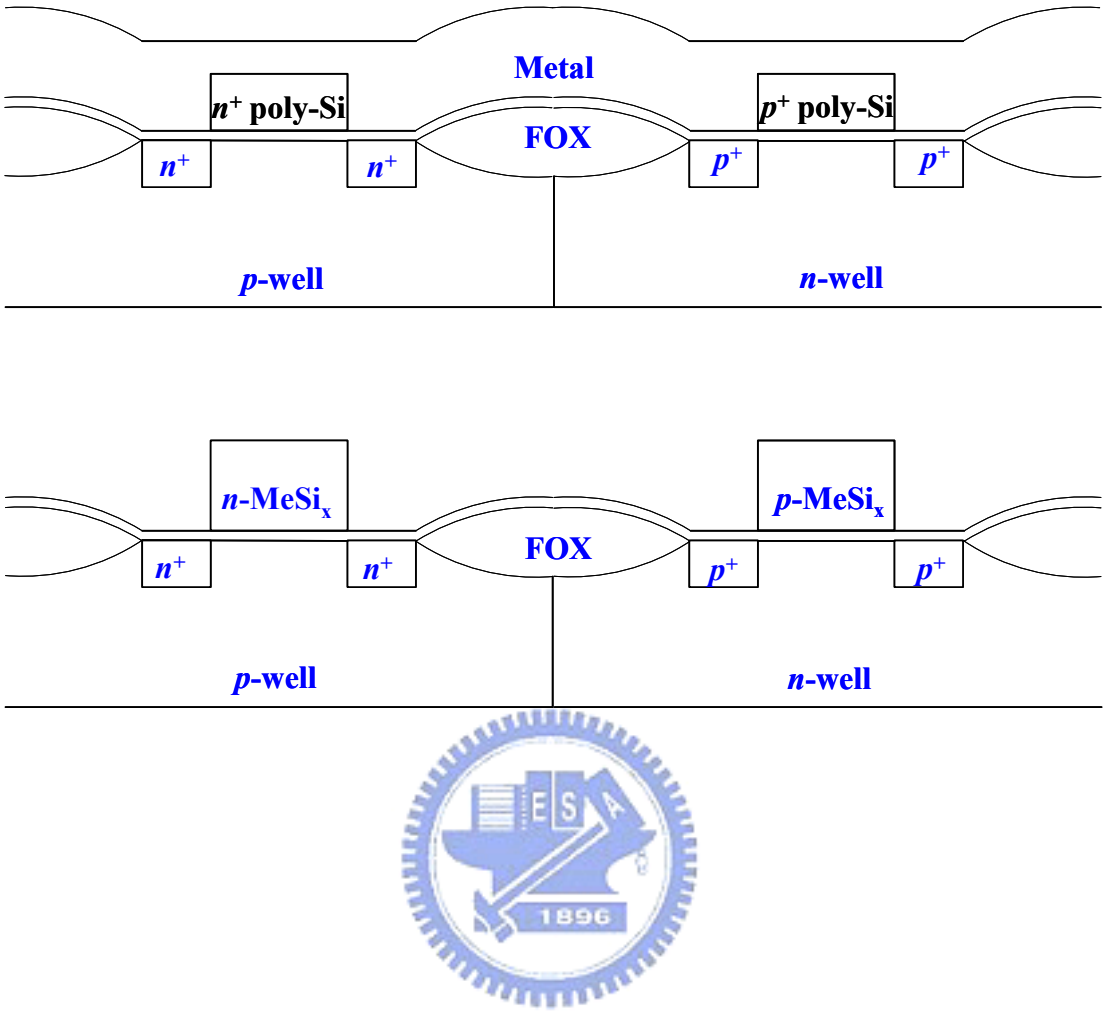

Fig. 4.2. The schematic illustration of the reported dual metal gate technology using FUSI method.

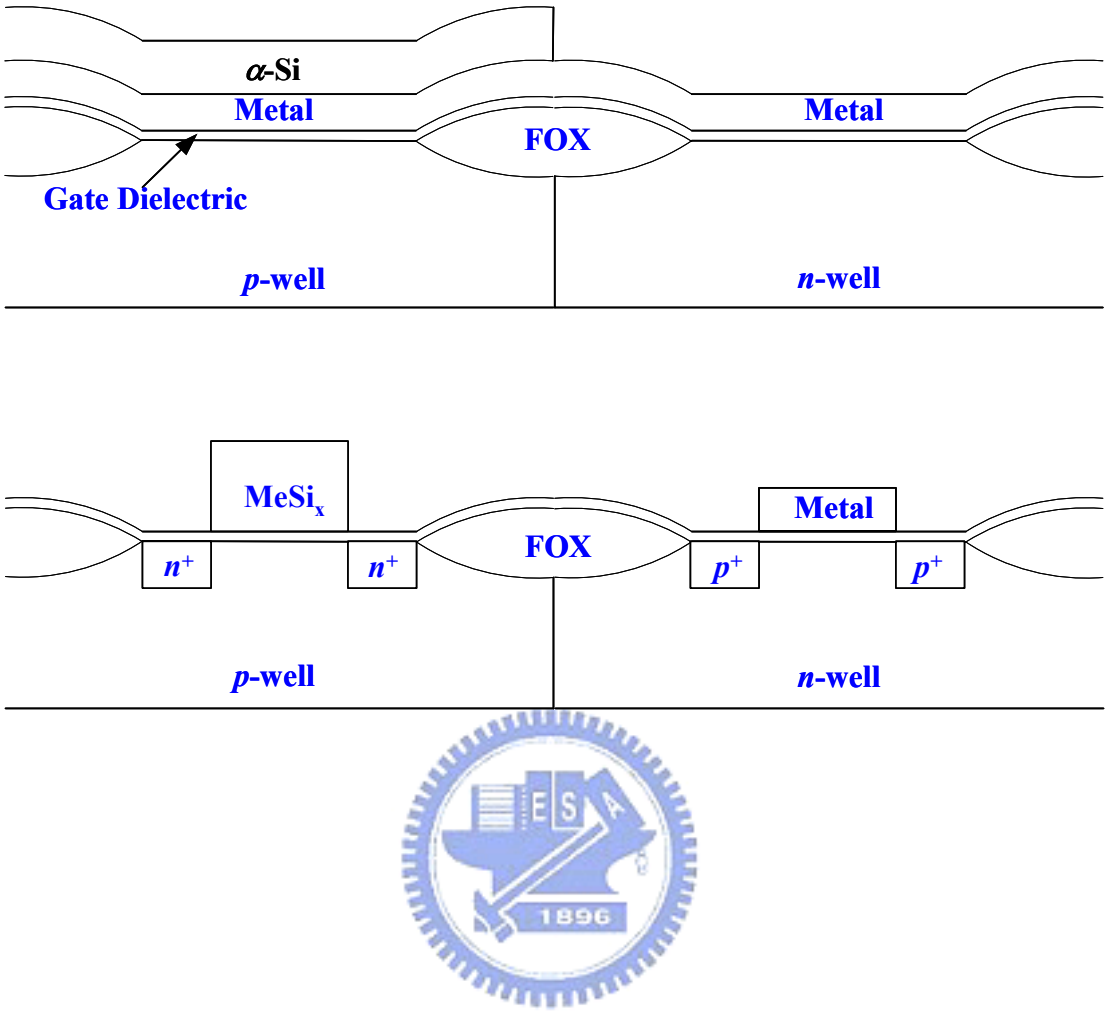

Fig. 4.3. The schematic illustration of the proposed novel dual metal gate technology gated by the combination of metal and metal silicide.

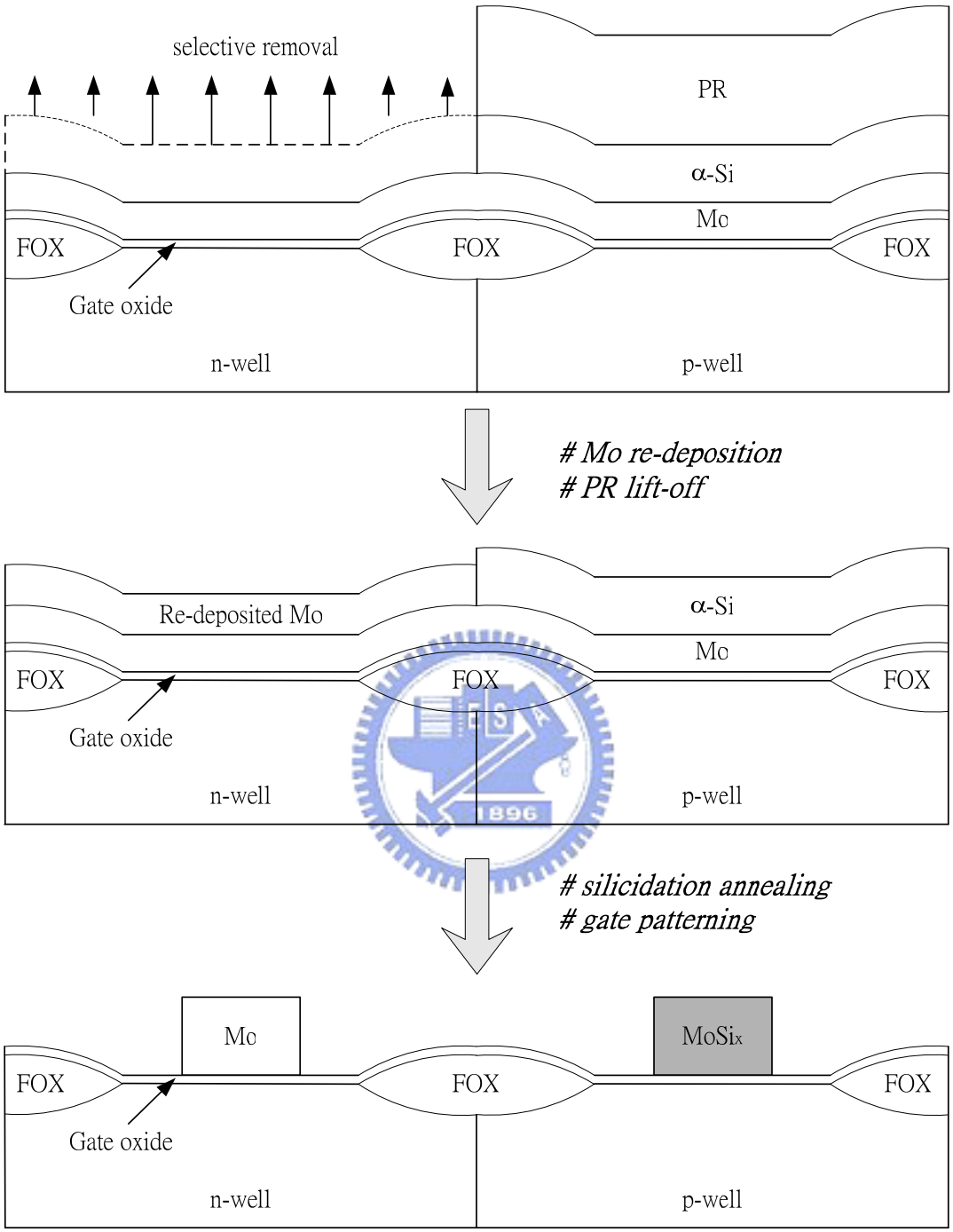

Fig. 4.4. The practical integration of the proposed novel dual metal gate technology gated by the combination of metal (Mo) and metal silicide ($MoSi_x$).

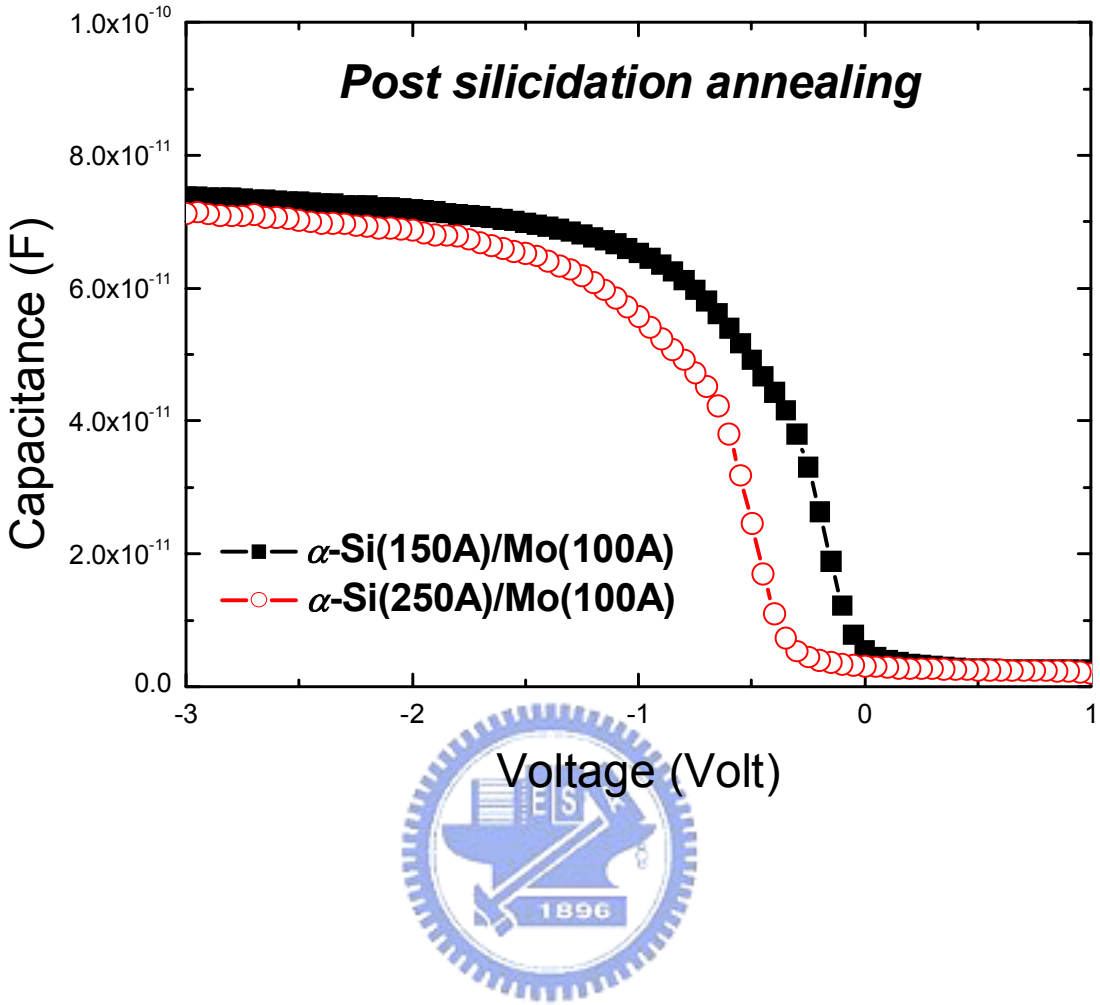

Fig. 4.5. Capacitance-voltage curves of post-silicidation α-Si/Mo/SiO_2/p-Si MOSCAP as a function of the thickness of α-Si.

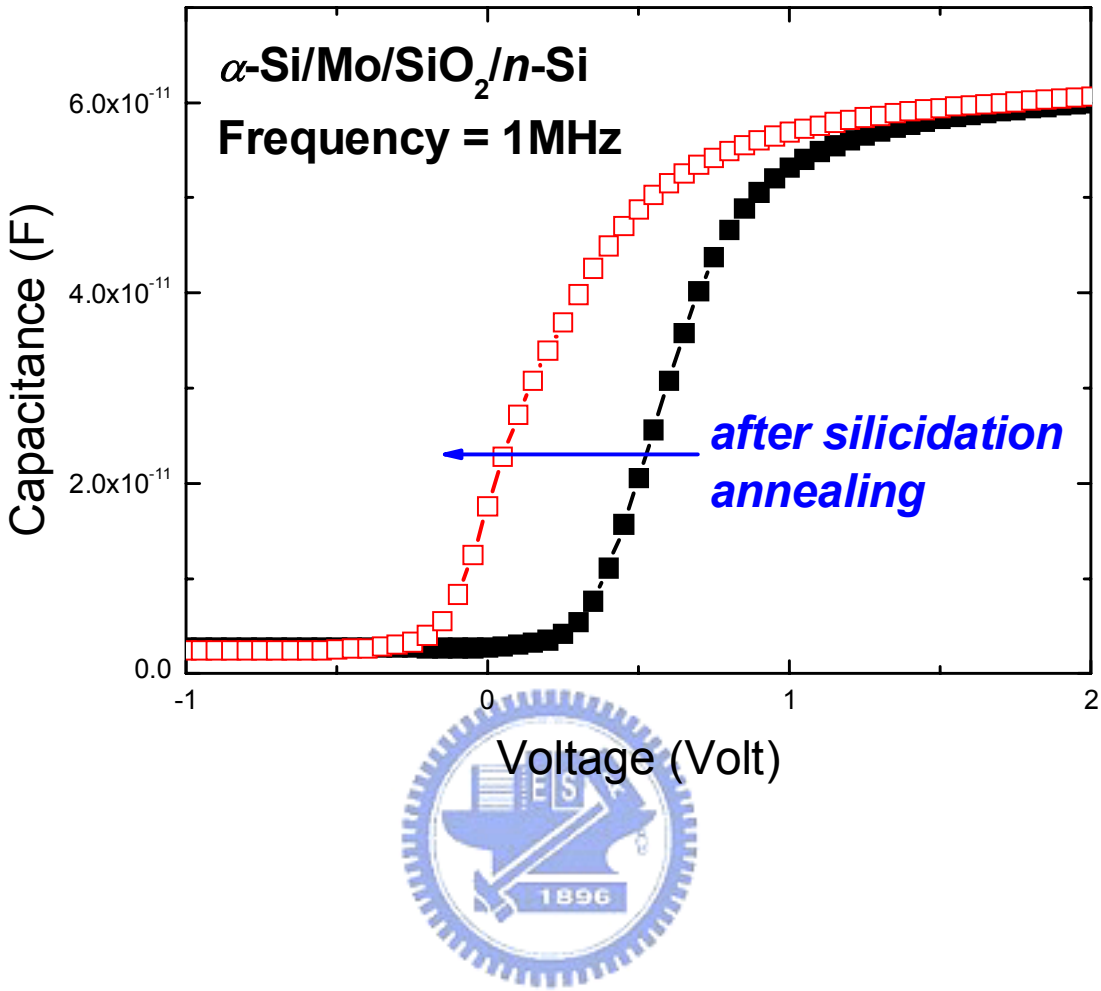

Fig. 4.6. Capacitance-voltage characteristics of MOSCAP devices with α-Si/Mo/SiO_2/n-Si structure before and after silicidation annealing.

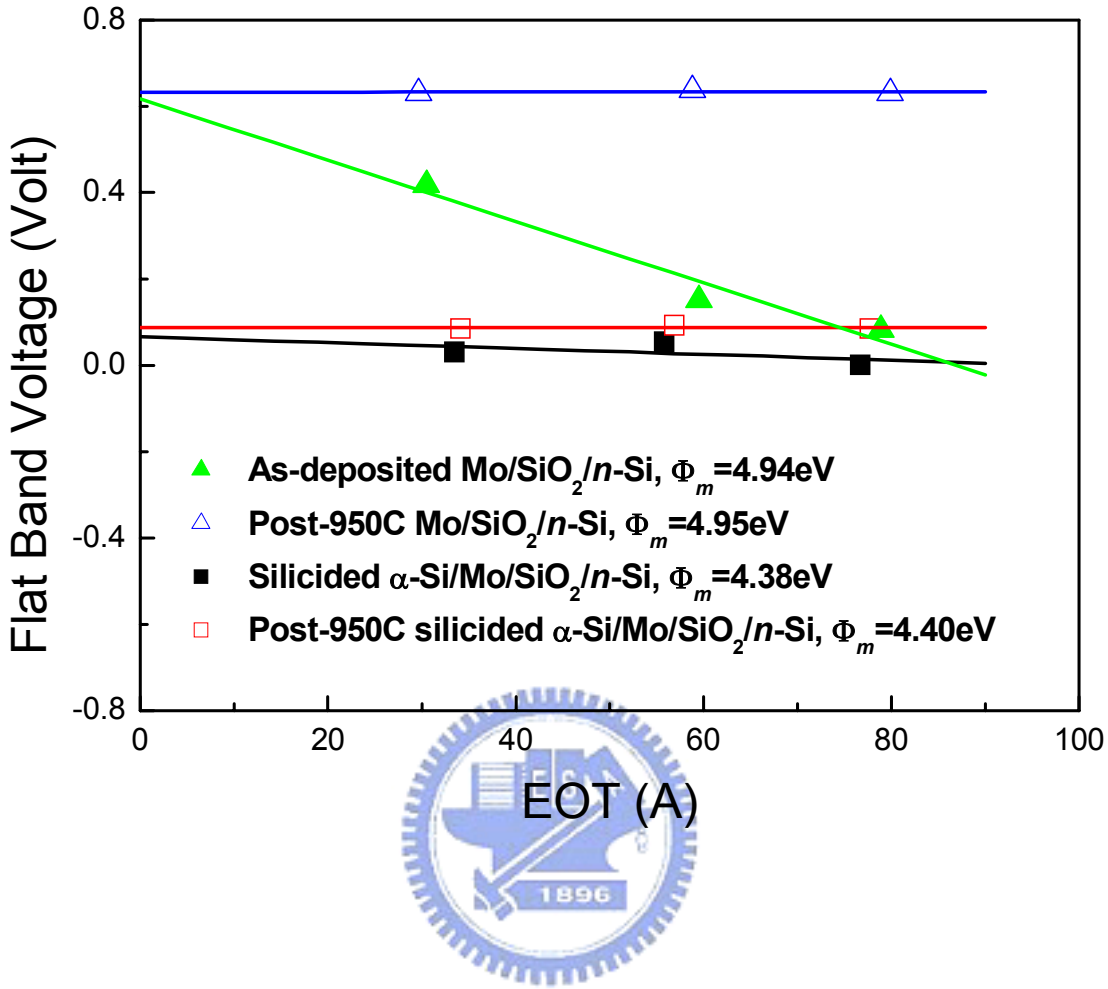

Fig. 4.7. The V_{FB} versus EOT plots of Mo and $MoSi_x$ gated MOSCAP devices before and after 950℃ RTA for thermal stability evaluation.

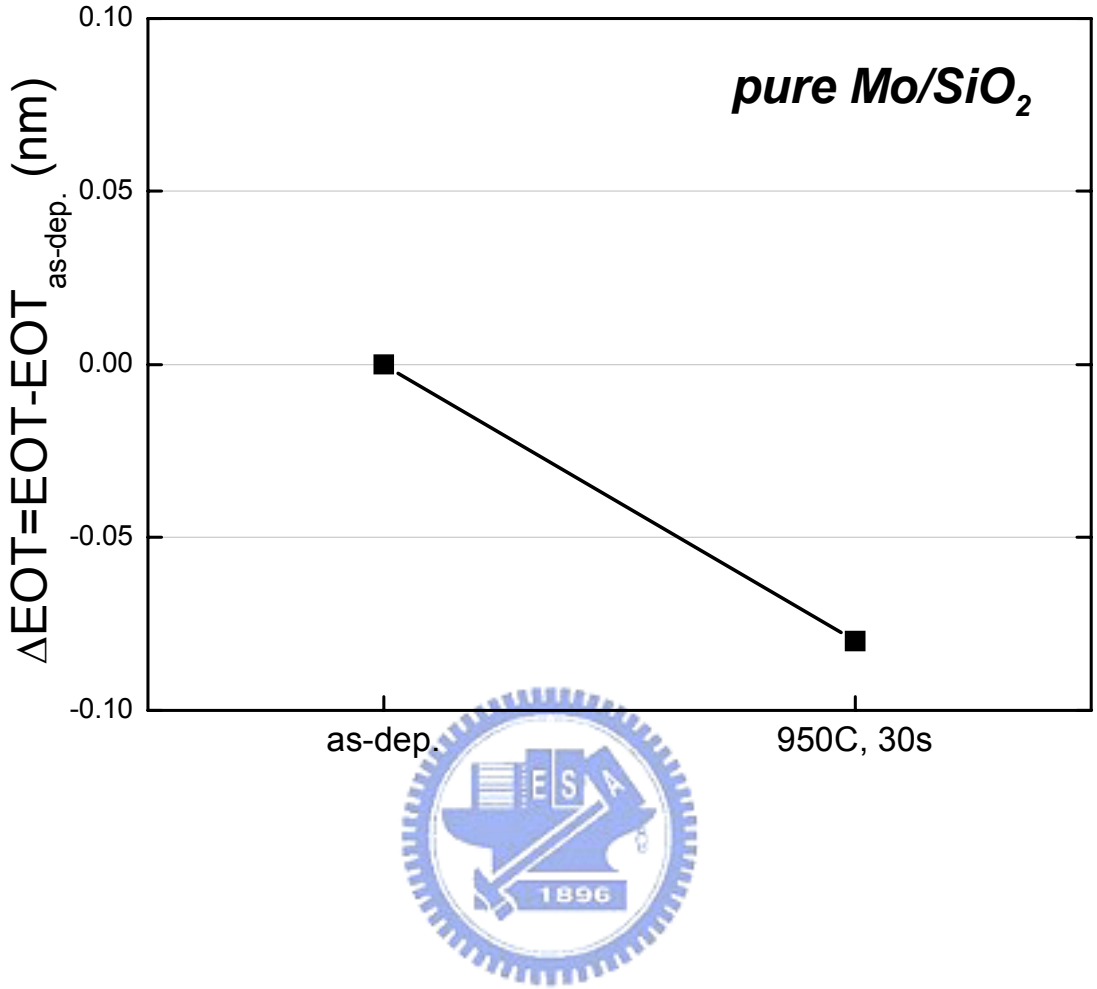

Fig. 4.8. The dependence of the EOT variation on annealing conditions for MOSCAP devices with Mo/SiO_2/*n*-Si structure.

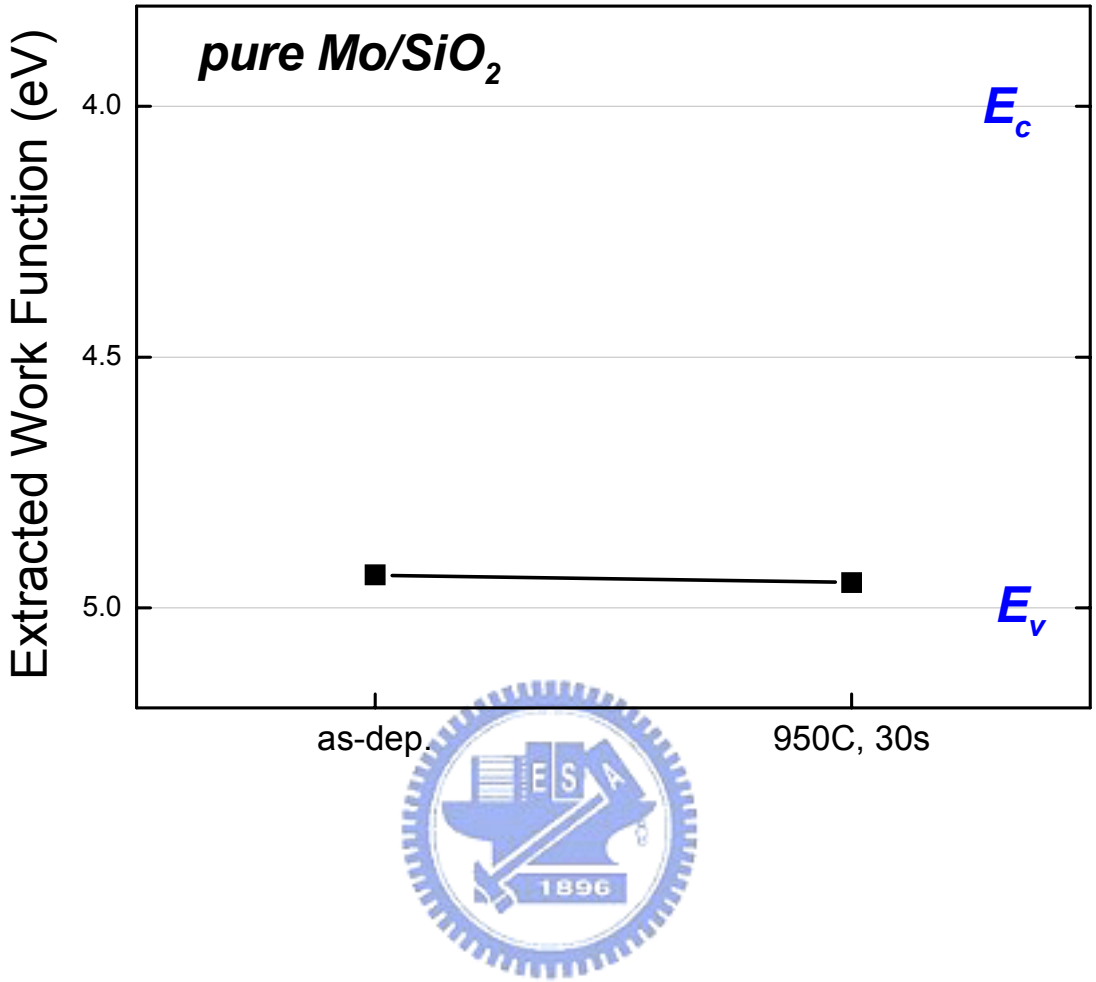

Fig. 4.9. The dependence of the extracted work function value on annealing condition for MOSCAP devices with Mo/SiO_2/*n*-Si structure.

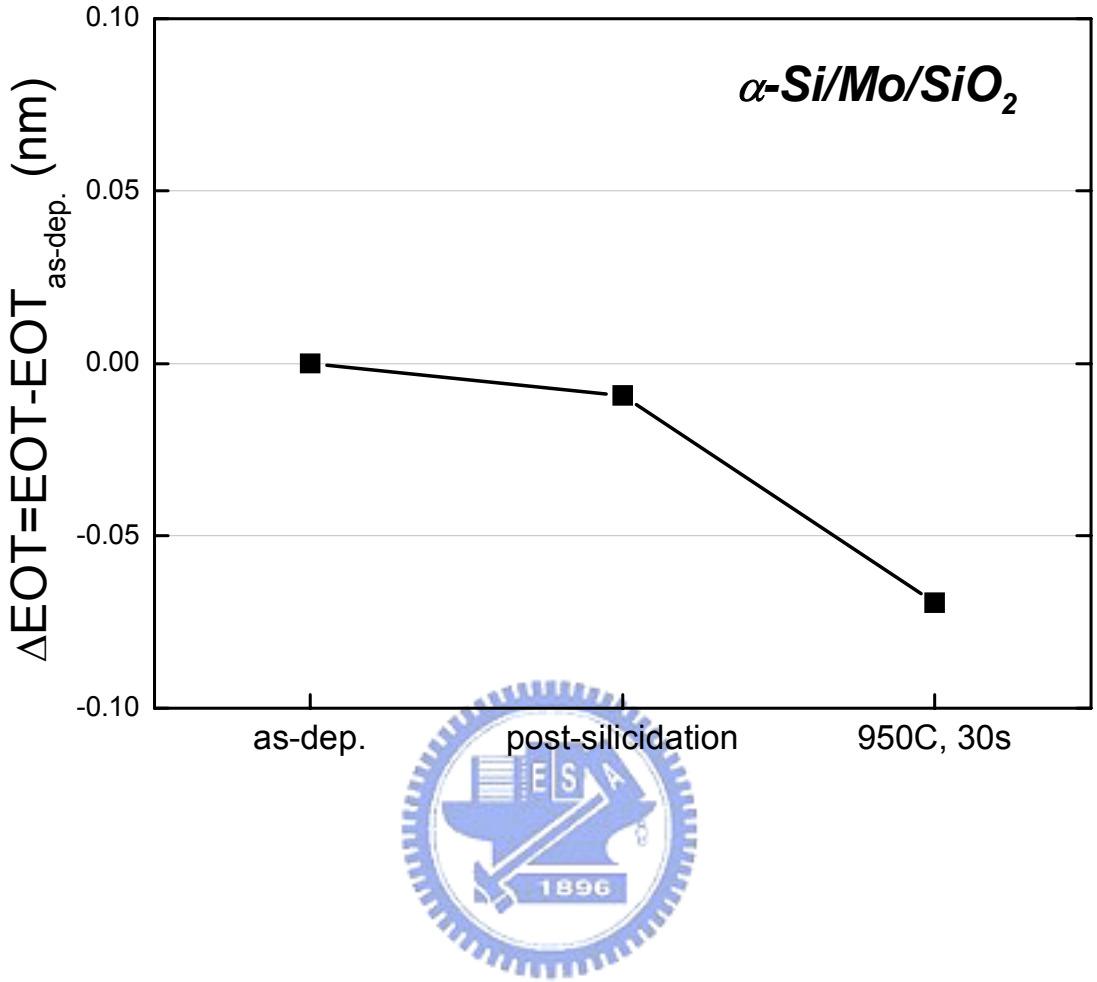

Fig. 4.10. The dependence of the EOT variation on annealing conditions for MOSCAP devices with α-Si/Mo/SiO_2/*n*-Si structure.

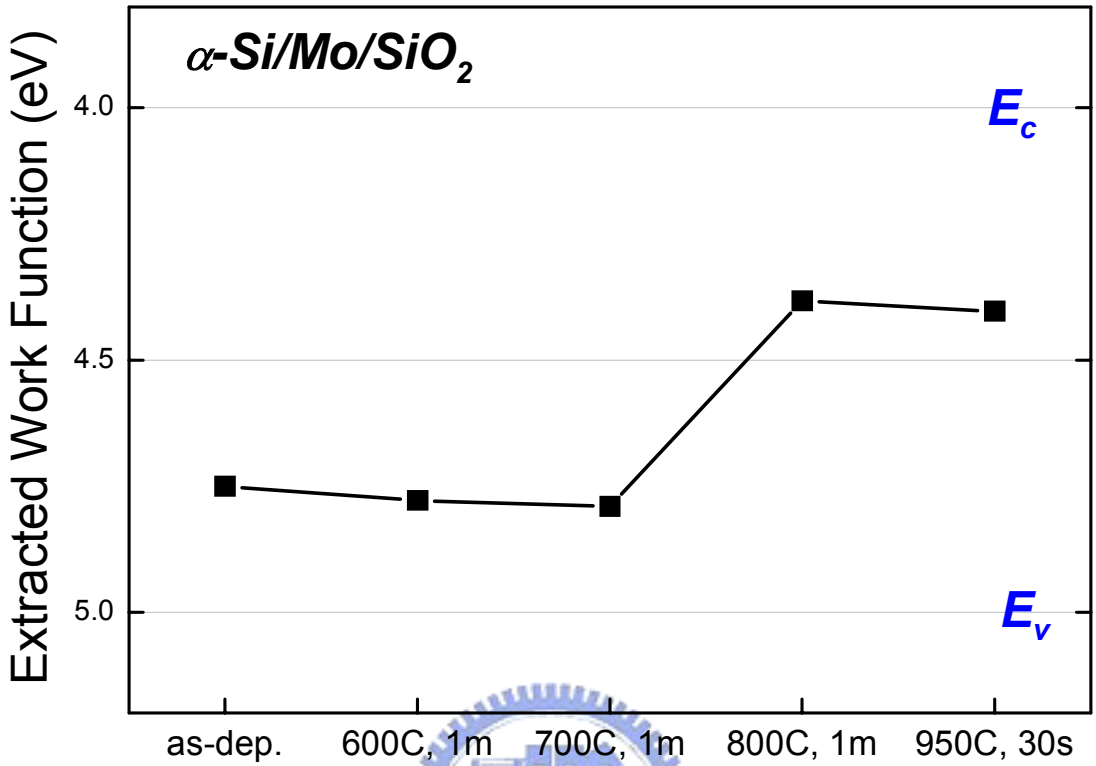

Fig. 4.11. The dependence of the extracted work function value on annealing temperature for MOSCAP devices withg α-Si/Mo/SiO_2/*n*-Si structure.

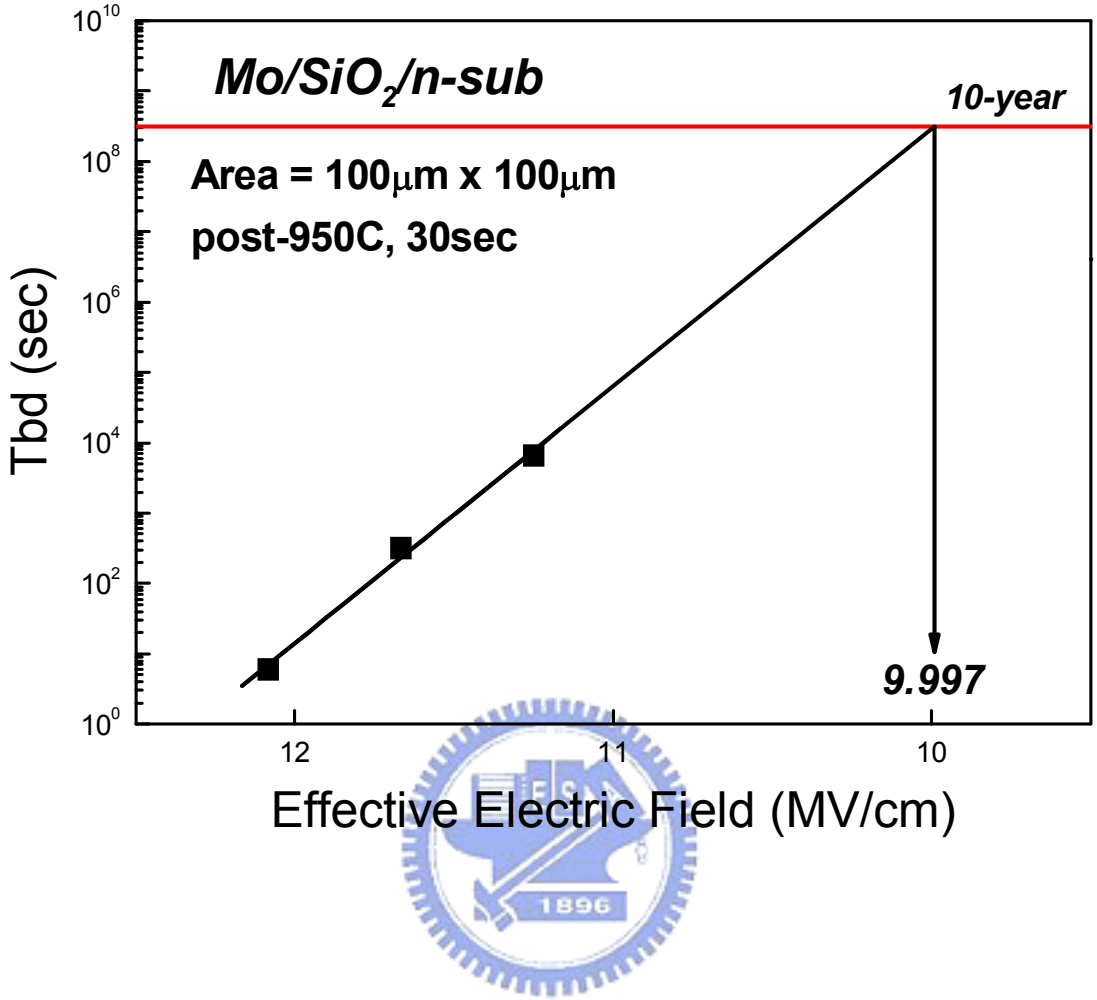

Fig. 4.12. The TDDB lifetime projection of the Mo/SiO_2 device. Superior TDDB characteristic for pure Mo gate annealed by 950℃ RTA for 30s is demonstrated.

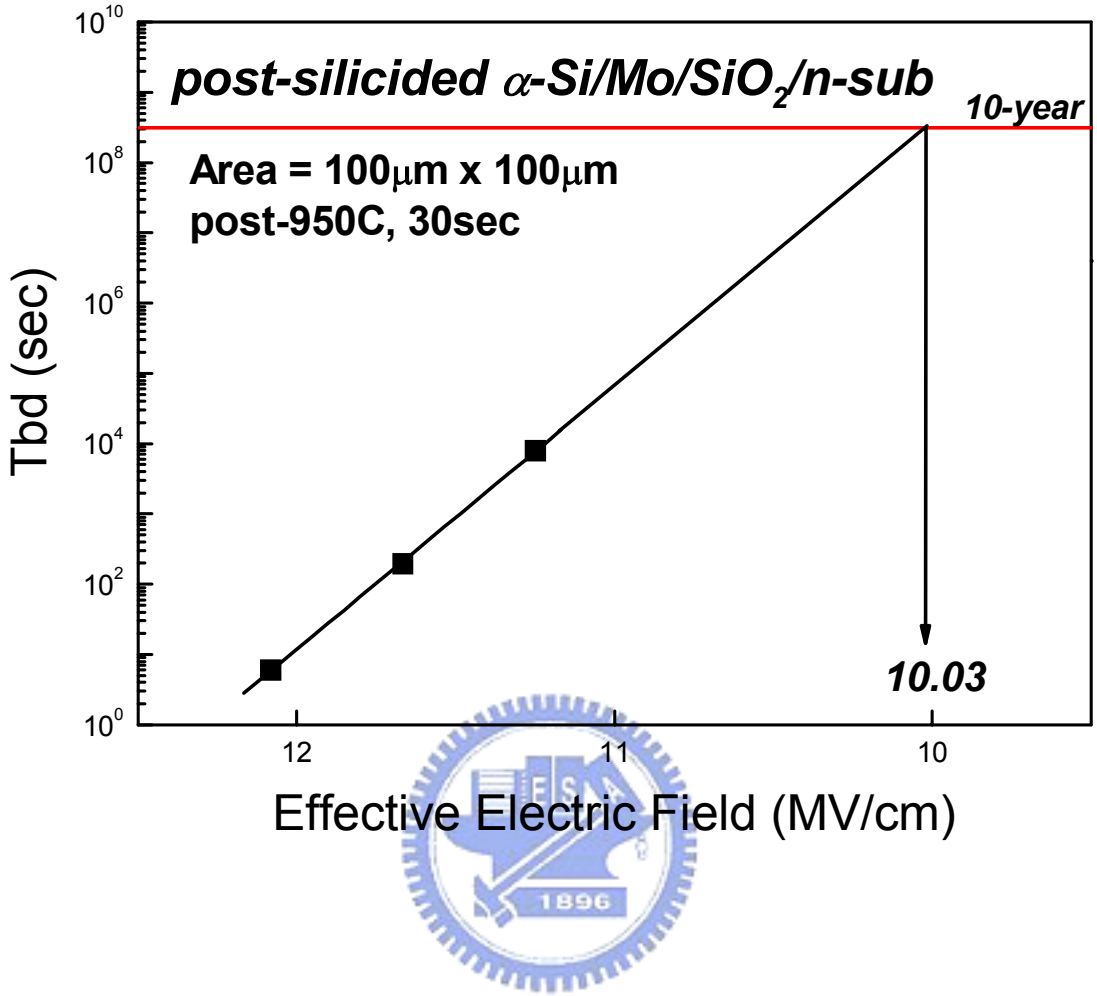

Fig. 4.13. The TDDB lifetime projection of the post-silicidation α-Si/Mo/SiO_2 device. Superior TDDB characteristic for $MoSi_x$ gate annealed by 950℃ RTA for 30s is demonstrated.

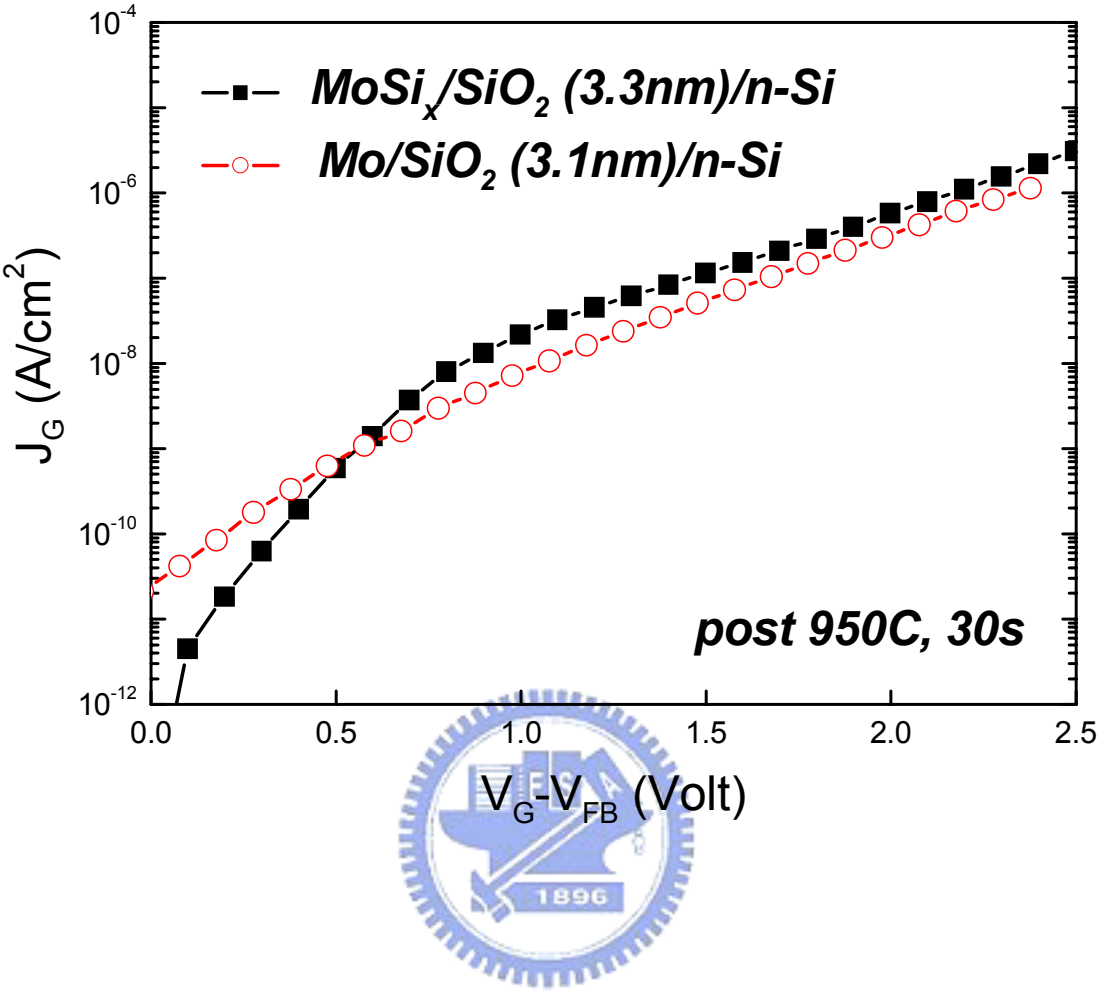

Fig. 4.14. The accumulation leakage current densities of Mo/SiO_2/*n*-Si and $MoSi_x$/SiO_2/*n*-Si devices annealed by 950℃ for 30s.

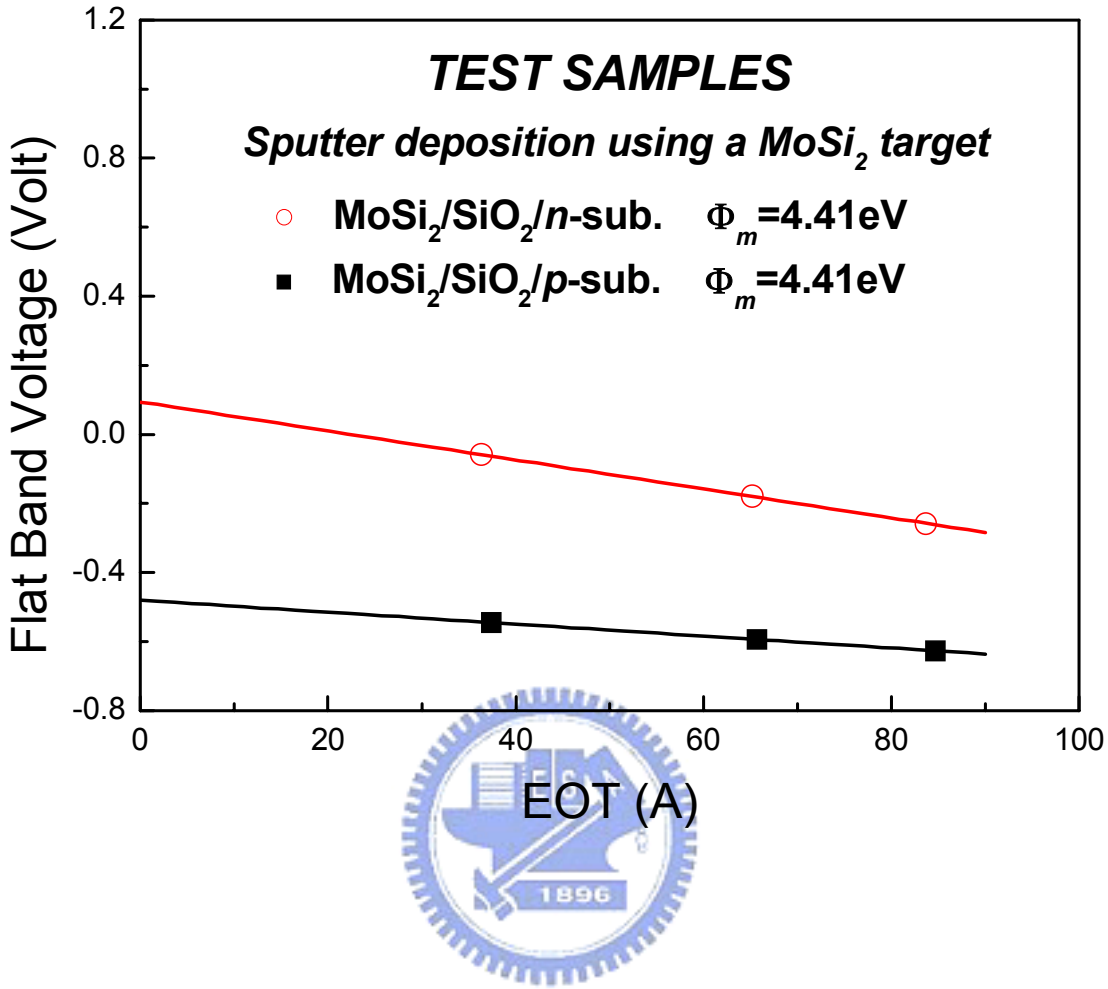

Fig. 4.15. Work function extraction of $MoSi_2$ on SiO_2. In this case, the $MoSi_2$ is sputtering-deposited using the $MoSi_2$ target.

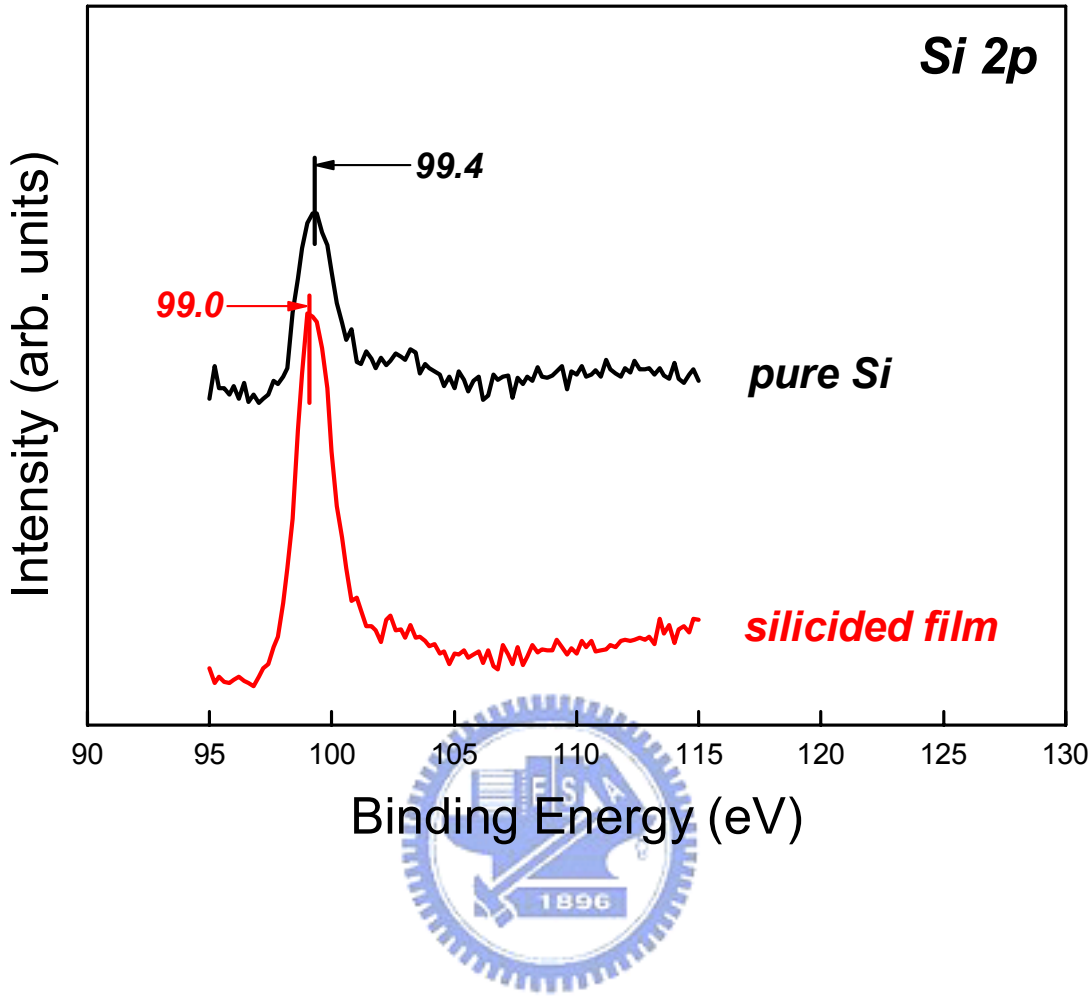

Fig. 4.16. The x-ray photoelectron spectroscopy (XPS) analysis shows that the binding energy corresponding to the Si 2p spectra of silicided films is 0.4eV lower than that of pure Si.

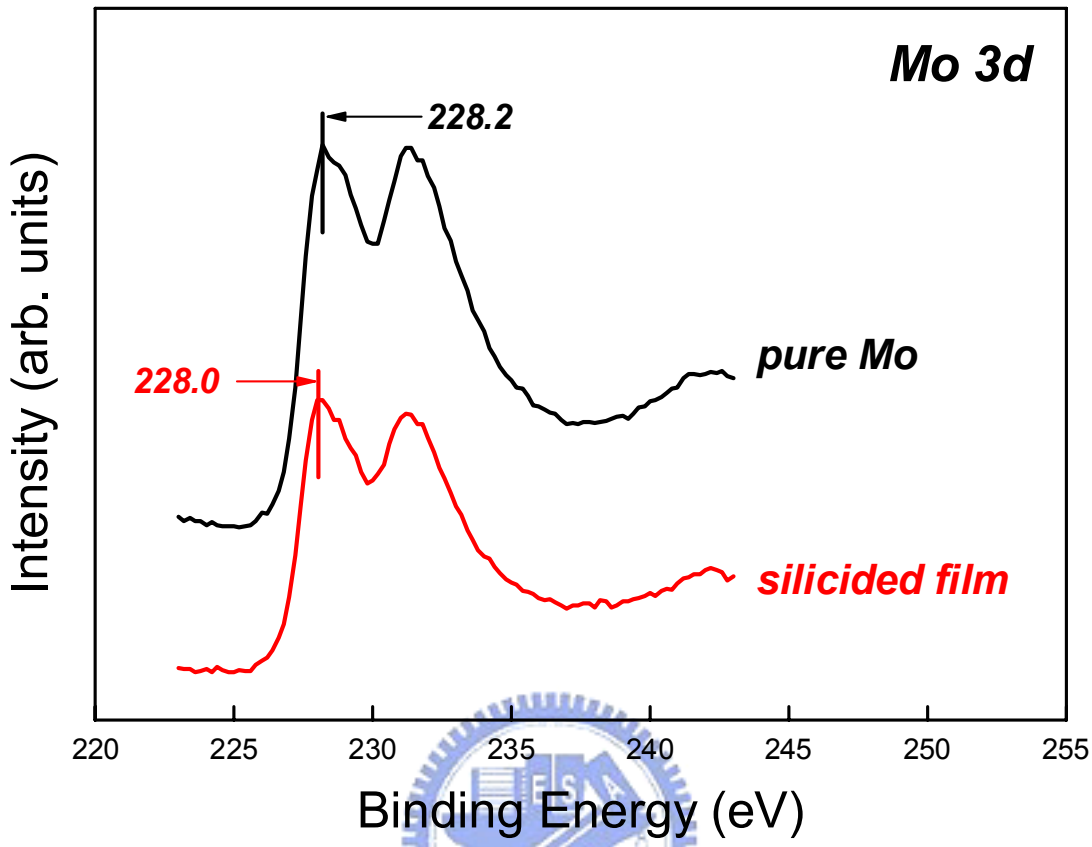

Fig. 4.17. The x-ray photoelectron spectroscopy (XPS) analysis shows that the binding energy corresponding to the Mo 3d spectra of silicided films is 0.2eV lower than that of pure Mo.

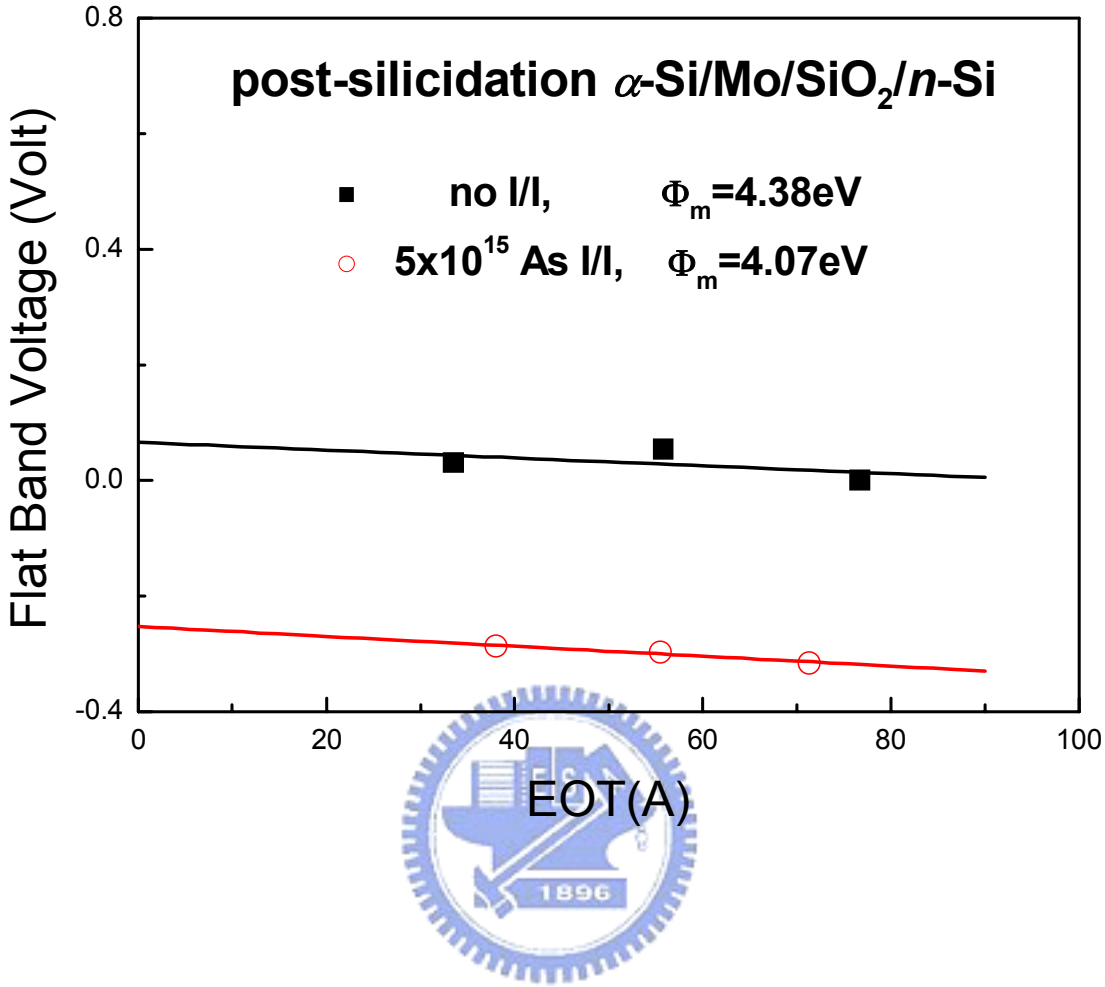

Fig. 4.18. The V_{FB} versus EOT plots of post-silicidation α-Si/Mo gated MOSCAP devices with ($5x10^{15}cm^{-2}$) and without arsenic pre-implantation dosage.

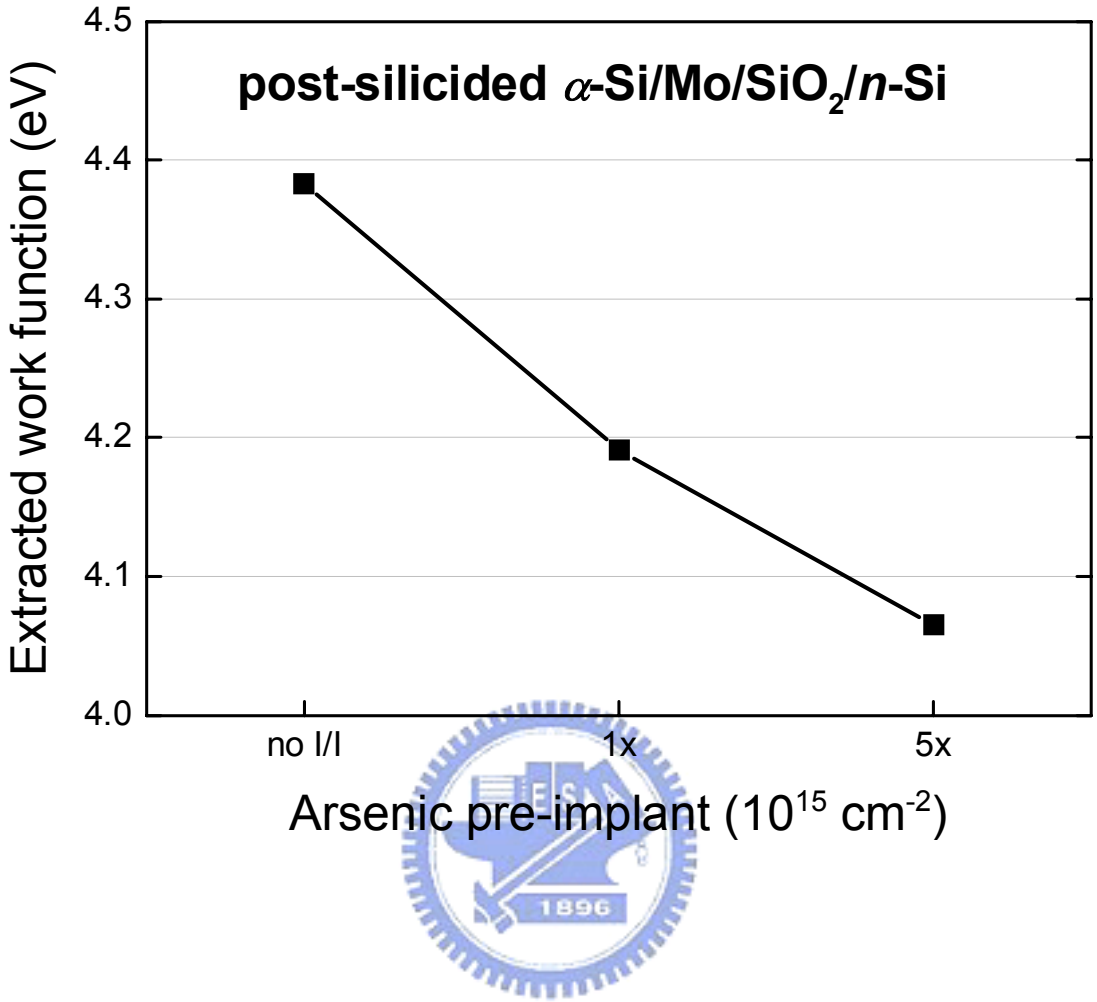

Fig. 4.19. The dependence of Φ_m values on the doses of arsenic pre-implantation.

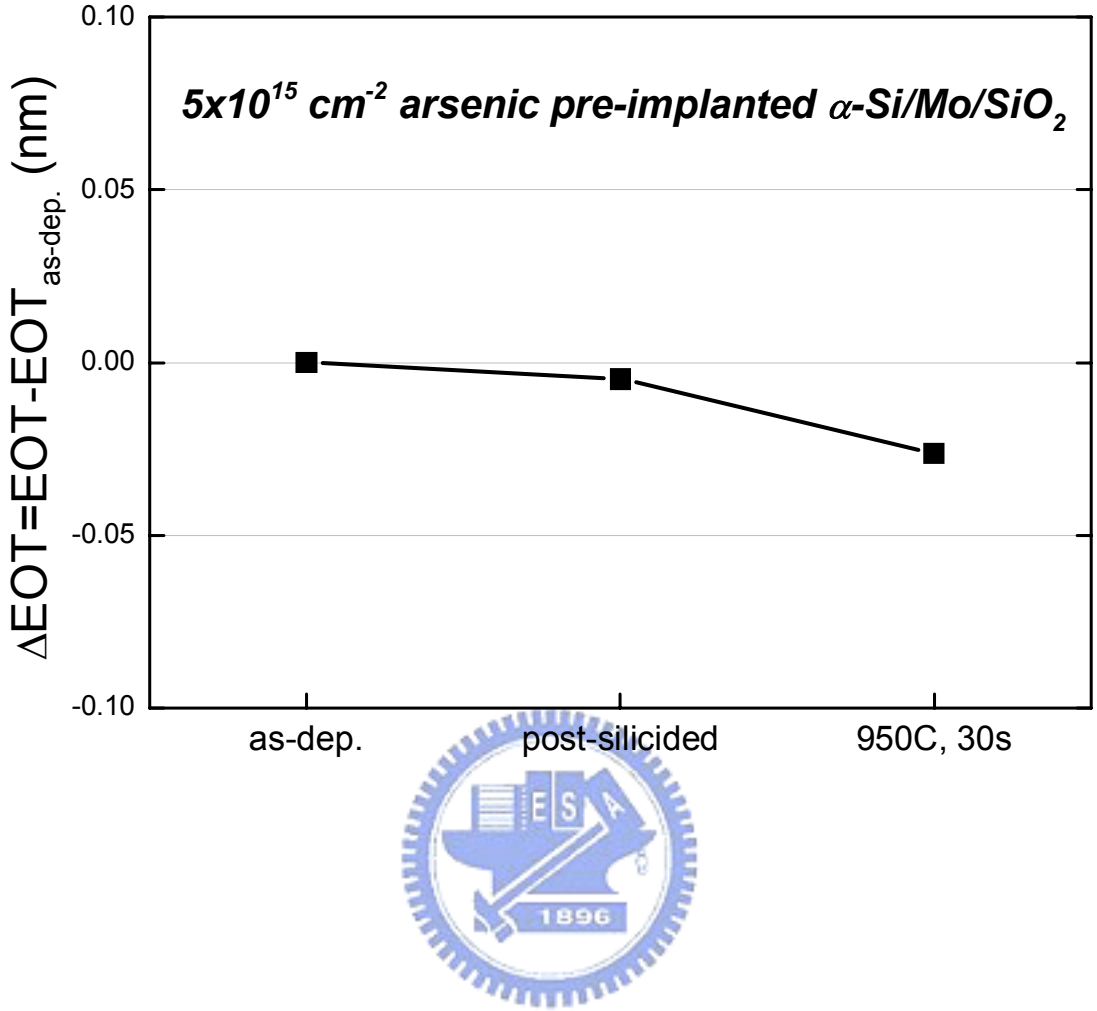

Fig. 4.20. The dependence of the EOT variation on annealing conditions for MOSCAP devices with α-Si/Mo/SiO_2/*n*-Si structure with 5x10^{15} cm^{-2} arsenic pre-implantation.

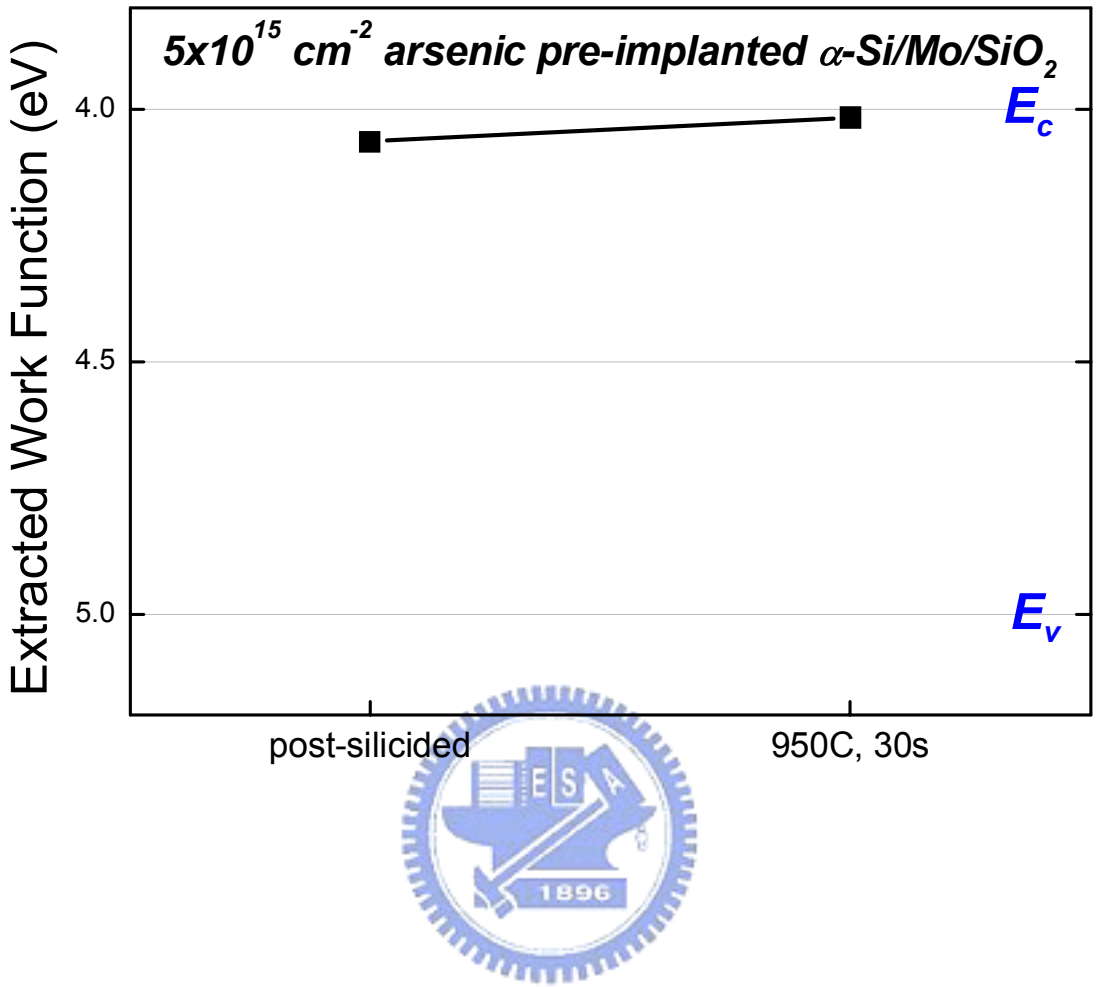

Fig. 4.21. The dependence of the extracted work function value on annealing conditions for MOSCAP devices with α-Si/Mo/SiO_2/*n*-Si structure with $5x10^{15}$ cm^{-2} arsenic pre-implantation.

Chapter 5

Investigation of $MoSi_x$ Based Dual Metal Gate Technology on the High-k Gate Dielectric

5.1 BACKGROUNDS AND MOTIVATION

The introduction of high-k gate dielectric can effectively reduce the gate tunneling leakage current because of its larger physical thickness under the same electrical thickness [1], [2]. In addition, traditional polysilicon gates have been found to be thermodynamically unstable on many high-k gate dielectric materials [3], [4] so that metals are expected to provide a turning point in possessing better thermal stability.

In the case of FUSI method, dopants in the polysilicon are believed to be responsible for providing work function difference between *n*- and *p*-type metal silicide (MeSi) gates [5], [6]. Both the source/drain dopant activation annealing and the silicidation anneaing contribute to the dopant redistribution. This phenomenon also suggests us a way to expand the work function shift in our proposed novel dual metal gate technology using Me-$MeSi_x$ combination and has been demonstrated in the previous chapter.

However, the impurity doping dose has been reported not to help modulate the

Φ_m of FUSI-MeSi, such as NiSi and PtSi, on HfON high-k gate dielectric because of the Fermi-level pinning effect [7]. Consequently, the undoped, *n*-type, and *p*-type metal silicide (MeSi) gates on high-k gate dielectric materials tend to possess almost the same effective work function values. The FUSI gate on high-k gate dielectric becomes single work function metal gate candidate and its application is strictly limited.

Based on this phenomenon, T. Nabatame *et al*. presented a partial silicides technology that uses n^+-polysilicon and *n*-type MeSi as gate electrodes for *n*- and *p*-channel devices, respectively, as shown in fig. 5.1. In this case, the phenomenon that *n*- and *p*-type metal silicides on the high-k gate dielectric possess almost the same effective work function values was applied. This approach, however, suffers from the poly depletion effect in *n*-channel devices.

The Hf-Si bond has been suggested to be responsible for the pinning effect and the large device threshold voltages observed in polysilicon and FUSI gates with an Hf-based gate dielectric [8]. The Hf-Si bond is likely to have been formed during the deposition of polysilicon and may not be eliminated by subsequent annealing or silicidation process [9]. The amount of Hf-Si bonds, which strongly depends on the type and quality of the gate/dielectric interface, becomes the key parameter in controlling the Fermi-level pinning effect. The suppression of the pinning effect by replacing HfO_2 with Si-rich Hf-silicates [9]-[12] or Al-incorporating HfAlON [13], [14] has been proposed. Also, the use of capping layer such as SiO_2 [12] or Al_2O_3 [9] on the high-k gate dielectric has been reported to reduce effectively the Hf-Si interaction. These improvements, however, come at the expense of a large EOT, a reduced average dielectric constant and poor scalability. In addition to the use of the

capping layer and the modulation of the Hf concentration in Hf-based high-k gate dielectric, a novel retardation of the pinning effect has been proposed using phase-controlled FUSI (PC-FUSI) gates [15], [16]. Although a negligible Φ_m difference between NiSi and Ni_3Si can be obtained on SiO_2, a small (about 0.25-0.33eV) Φ_m difference can be achieved on Hf-based high-k gate dielectric, and is believed to be caused by Fermi-pinning relaxation associated with the metal-rich silicide (Ni_3Si), which reduces the number of Hf-Si bonds at the gate dielectric interface.

In the FUSI method, conventional polysilicon gates will be directly deposited on top of the high-k gate dielectrics and the S/D dopant activation annealing will be performed prior to the formation of silicides. The FUSI method potentially enhances the susceptibility to Fermi-level pinning effect. By contrast, the proposed dual metal gate technology uses Mo as the first layer gate electrode, which can separate the silicon layer required for the formation of silicides from the underlying high-k gate dielectrics. The Fermi-level pinning effect caused by Hs-Si bond formation can be suppressed so that the modulation of work function using impurity dopant may be preserved on high-k gate dielectrics.

In this chapter, we demonstrate that combination of Mo-$MoSi_x$ gate electrodes can possess a considerable work function shift on high-k gate dielectrics. Moreover, *n*-type $MoSi_x$ still has a lower Φ_m value than undoped $MoSi_x$ on HfO_2, even though the modulation range provided by arsenic pre-implantation is smaller than that on SiO_2.

5.2 EXPERIMENT

MOS capacitors with Mo/HfO_2/*n*-Si and α-Si/Mo/HfO_2/*n*-Si structures were fabricated on 6-in Si wafers. After LOCOS isolation, MOCVD HfO_2 (physical thickness: 5nm, 7.5nm, and 10nm) was deposited as the gate dielectric. For all samples, a thin (10nm) layer of Mo was sputter-deposited on top of the gate dielectric. Some samples were followed by sputter-deposition of α-Si (25nm). Gate electrodes were then patterned by reactive ion etching (RIE) using Cl_2-based chemistry. Following gate electrode patterning, some of the samples with an α-Si/Mo/ HfO_2 stack were then subjected to arsenic implantation (10KeV, $1x10^{15}$-$5x10^{15}cm^{-2}$). Samples with an α-Si/Mo/HfO_2 stack were then subjected to successive rapid thermal annealing (600℃, 1 min. + 700℃, 1 min. + 800℃, 1 min.) in N_2 ambient for $MoSi_x$ formation. The flat band voltage (V_{FB}) and equivalent oxide thickness (EOT) were extracted from the measured C-V curve using the quantum mechanical C-V (QMCV) simulator [17]. The effective Φ_m values of the gate electrodes on MOCVD HfO_2 gate dielectric were then extrapolated from the V_{FB}—EOT plots by setting the electron affinity (χ) of the Si substrate to 4.05eV.

5.3 RESULTS AND DISCUSSION

Fig. 5.2 shows the C-V characteristics of MOSCAP devices gated by α-Si/Mo/HfO_2 stack before and after silicidation annealing. Similar C-V behavior to the case on SiO_2 gate dielectric can be observed. A negative post-silicidation flat-band voltage shift without EOT variation can be obtained. The flat-band voltage shift can

be contributed from the change of gate electrode work function and the reduction of fixed charge.

Fig. 5.3 shows the C-V characteristics of MOSCAP devices gated by pure Mo/HfO_2 stack after RTP at 950℃ for 30s. The MOSCAP devices on MOCVD HfO_2 still exhibit normal and smooth C-V characteristics. The V_{FB} versus EOT plots were also generated for metal work function extraction. The effective Φ_m values of as-deposited pure Mo film and $MoSi_x$ on HfO_2 are extracted to be 4.89eV and 4.34eV, respectively, providing an Φ_m difference of 0.55eV. The possessed work function combination can be suitable for devices with advanced transistor structures. As expected, the proposed novel dual metal gate technology using Me-$MeSi_x$ combination exhibits the superiority over the FUSI technology since a considerable work function shift can be remained on high-k gate dielectrics.

The dependences of Φ_m values on gate dielectric materials are shown in fig. 5.4. Effective Φ_m values of pure Mo or $MoSi_x$ gate on HfO_2 are slightly lower than that on SiO_2, while the provided Φ_m shift seems to be regardless of the underlying gate dielectric materials. This observation consists with the results reported by J. H. Lee *et al.* [18]. The developed novel dual metal gate technology successfully overcomes the problem encountered in the FUSI method on high-k gate dielectric materials. Our proposed approach acts as a dual metal gate approach on high-k gate dielectrics.

Furthermore, the arsenic pre-implantation can still lower the effective Φ_m value of $MoSi_2$ on HfO_2 gate dielectric as shown in fig. 5.5. The effective Φ_m value of $MoSi_x$ on HfO_2 with implantation of $5x10^{15}$ cm^{-2} ($1x10^{15}$ cm^{-2}) arsenic doses is 4.06eV (4.16eV), which is 0.28eV (0.18eV) lower than that for the sample without arsenic pre-implantation. As mentioned above, pre-implantation of impurities does not

help to modulate the Φ_m of FUSI gates on the HfO_2 gate dielectric because of the Fermi-level pinning effect [7]. By contrast, the possibility of Φ_m modulation using dopant pre-implantation is still maintained herein. With $5x10^{15}$ cm^{-2} arsenic pre-implantation, the impurity-induced Φ_m lowering on SiO_2 gate dielectric is 0.31eV, while that on HfO_2 is 0.28eV. The small reduction (0.03eV) in the modulation range may be partially due to the process variation caused by dopant implantation. This improvement may be attributed to the use of Mo as the first layer metal, which effectively separates most Si atoms from the gate/HfO_2 interface prior to its participation in silicidation as shown in fig. 5.6. The formation of Hf-Si bonds during α-Si deposition or silicidation annealing is noticeably mitigated and the pinning effect, believed to be caused by Hf-Si interaction, can be less pronounced.

5.4 SUMMARY

We demonstrate the proposed dual metal gate technology gated by Mo and $MoSi_x$ can provide a considerable effective work function shift on high-k gate dielectric materials. The effective Φ_m value of pure Mo or $MoSi_2$ gate on HfO_2 is slightly lower than that on SiO_2, but the Φ_m difference between Mo and $MoSi_x$ is almost the same regardless of the underlying gate dielectric materials. The arsenic pre-implantation still has effect upon Φ_m modulation of metal silicide on HfO_2, even though the modulation range is a little smaller than that on SiO_2.

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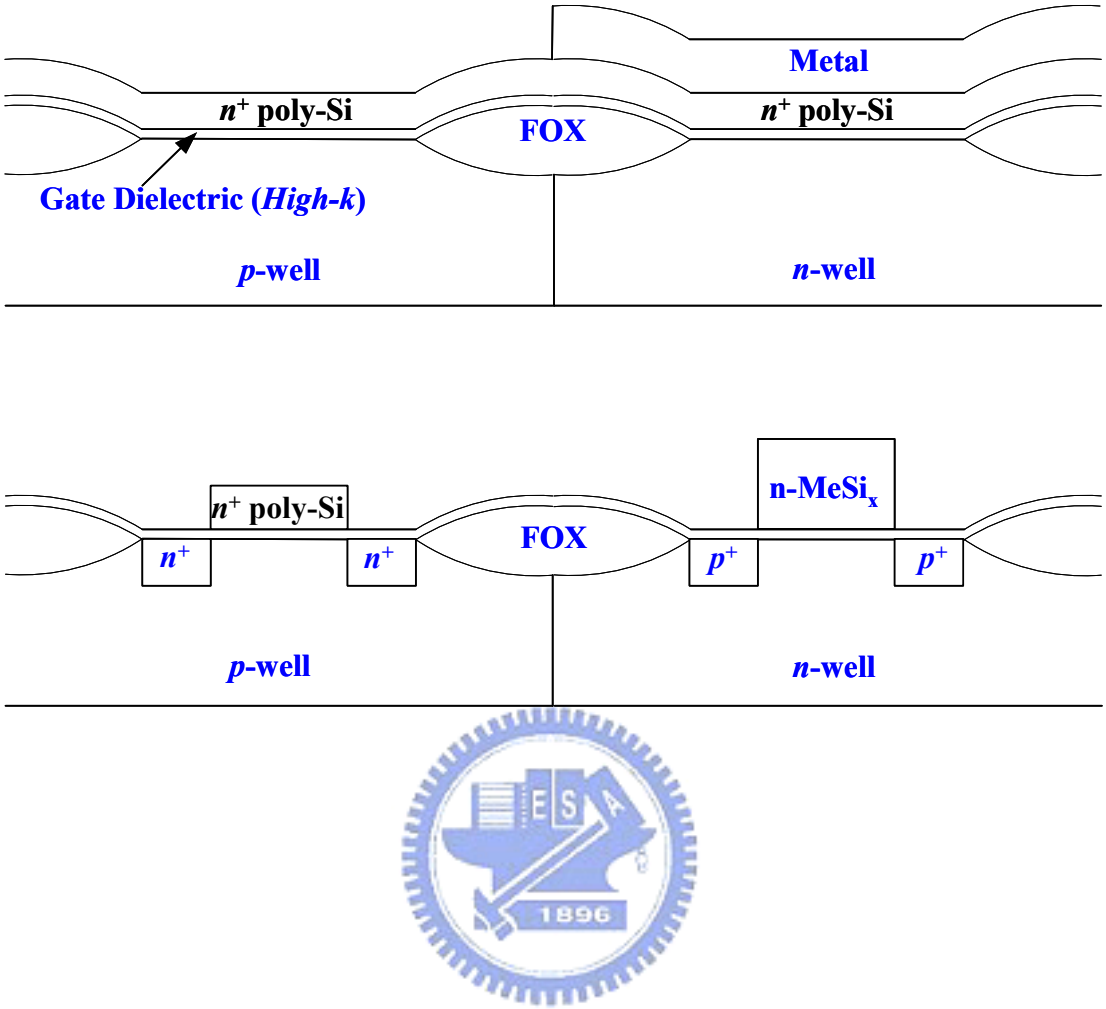

Fig. 5.1. The schematic illustration of dual metal gate technology gated by the combination of polysilicon and metal silicide.

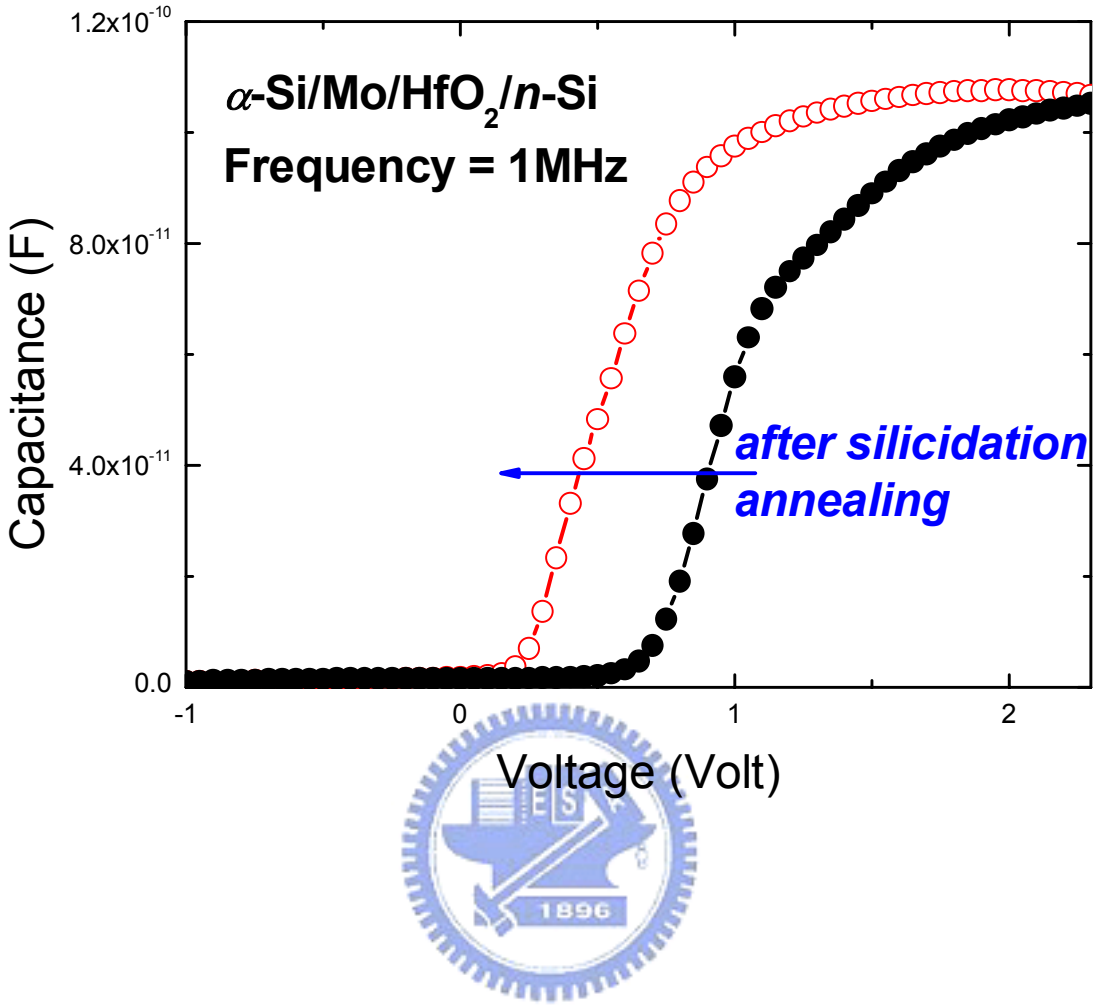

Fig. 5.2. The capacitance-voltage characteristics of MOSCAP devices with α-Si/Mo/HfO_2/n-Si structure before and after silicidation annealing.

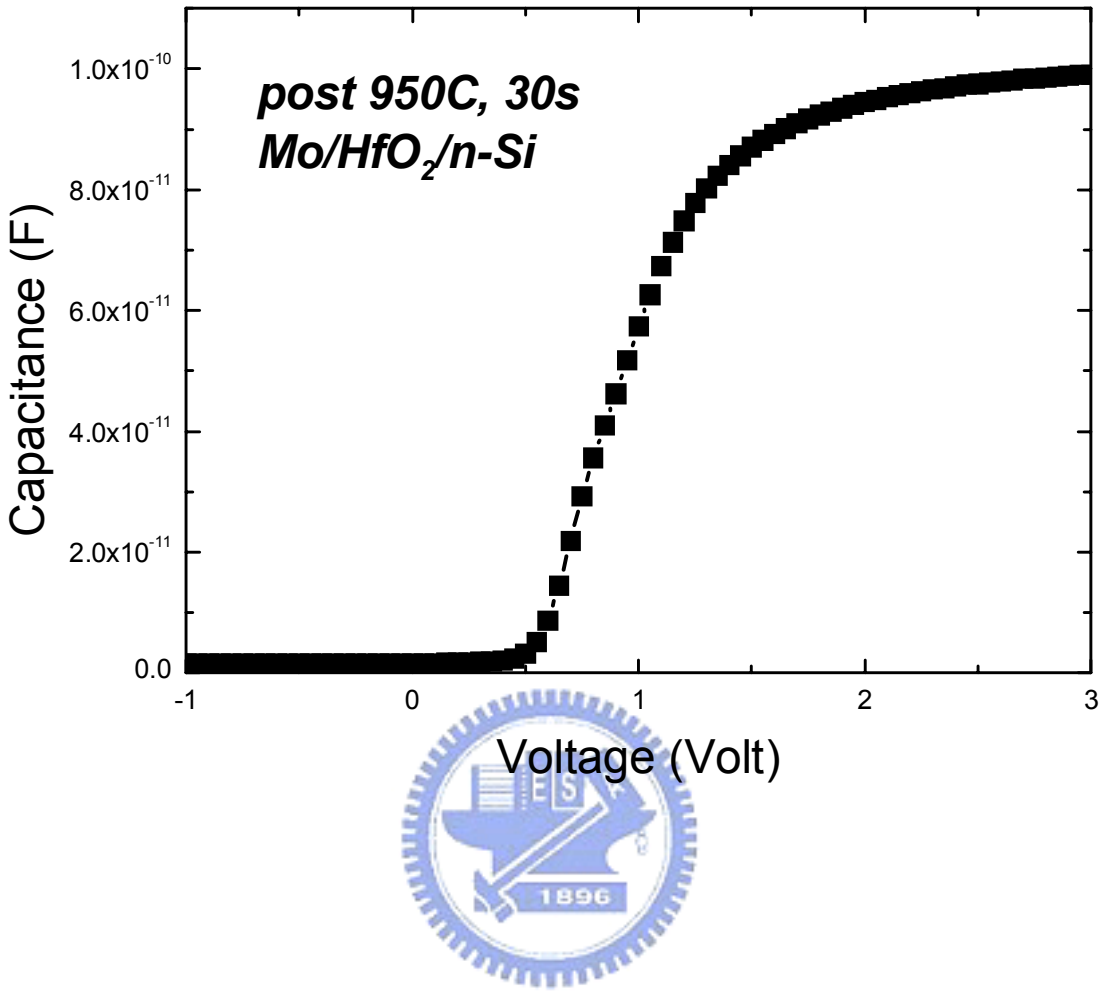

Fig. 5.3. The capacitance-voltage characteristics of pure Mo gated MOSCAP devices on the HfO_2 gate dielectric after RTA at 950℃ for 30s.

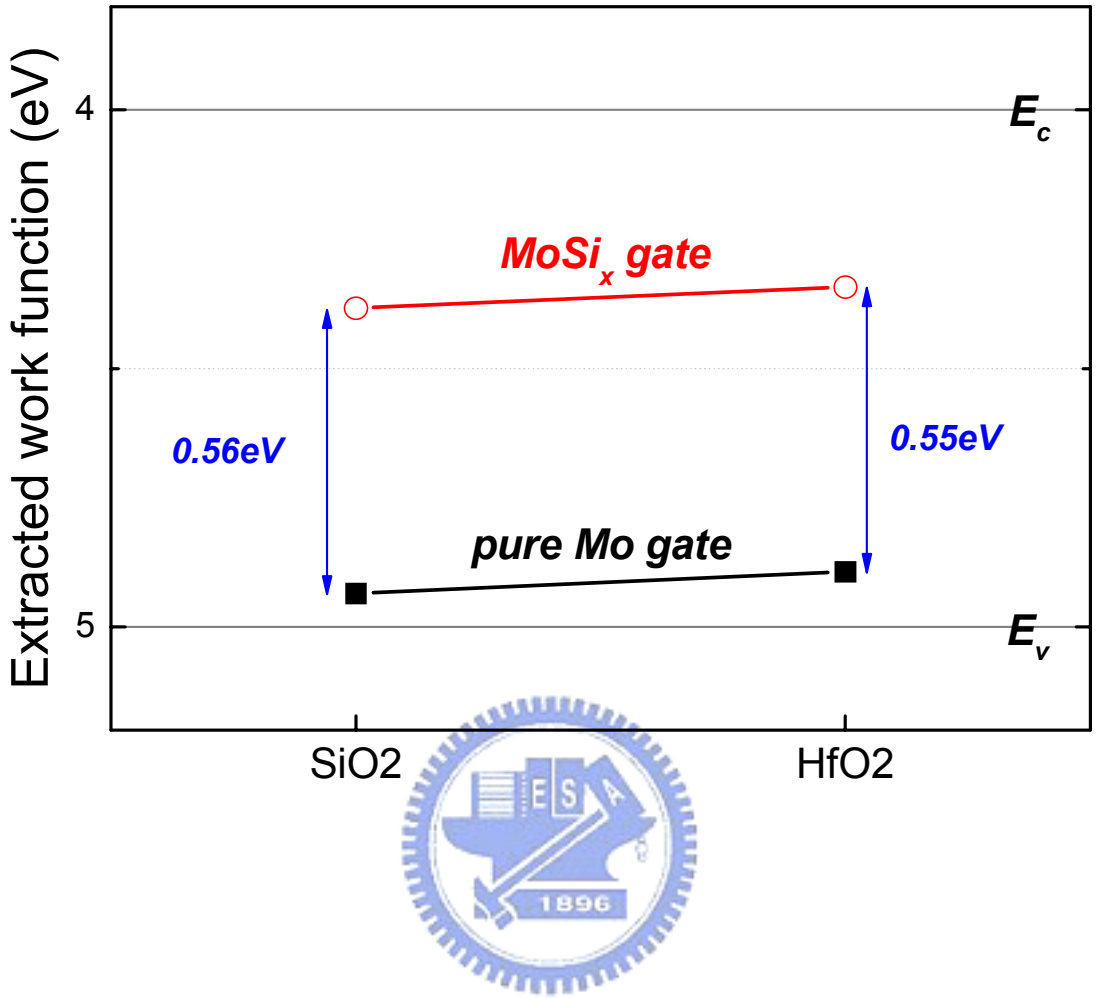

Fig. 5.4. The dependence of Φ_m values on gate dielectric materials for pure Mo and $MoSi_x$ gate electrodes.

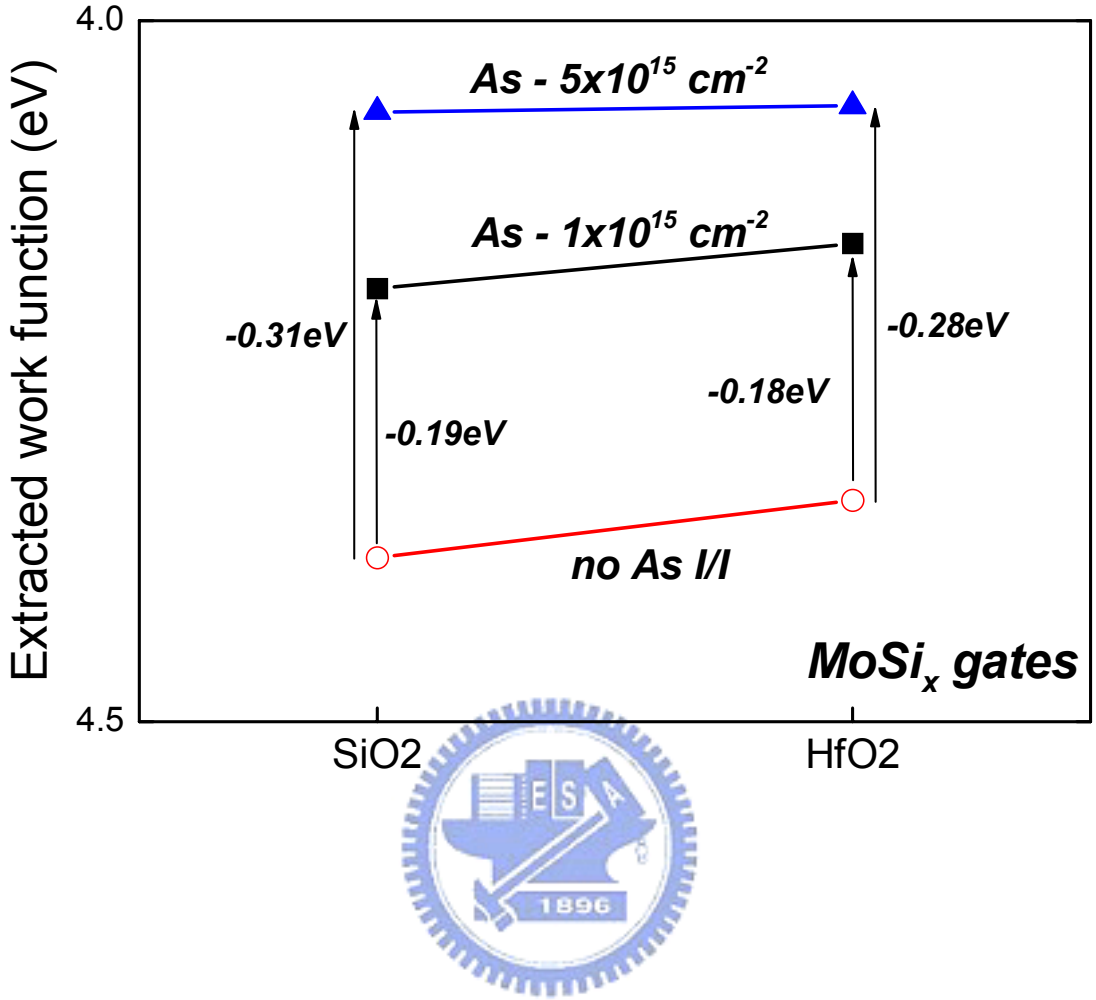

Fig. 5.5. The dependence of Φ_m values on gate dielectric materials for $MoSi_x$ gate electrodes with and without arsenic pre-implantation.

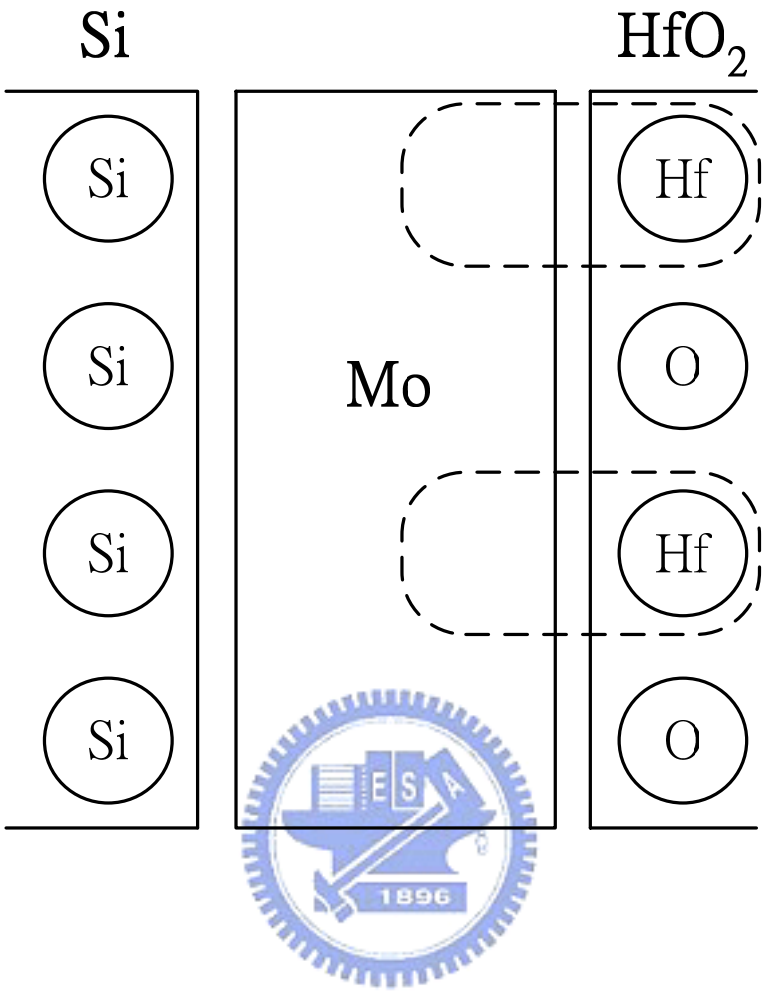

Fig. 5.6. Schematic explanation of the machenism of Fermi-level pinning effect relaxation in the proposed novel approach.

Chapter 6

Conclusions and Suggestions for Future Work

6.1 CONTRIBUTIONS OF THIS STUDY

We would like to point out major contributions in this dissertation.

1. In chapter 2, we have extracted work function values and evaluated thermal stabilities of sputter-deposited Hf-Mo binary alloys. The almost linear and continuous work function adjustment with Hf atomic fraction in the sputter-deposited Hf-Mo binary alloy has been demonstrated. This approach shows a great potential in the work function engineering. The thermal stability of Hf-Mo binary alloy on SiO_2 also depends on the Hf atomic fraction. The Hf-Mo binary alloy with larger Hf atomic fraction possesses lower work function value but poorer thermal stability.

2. In chapter 3, we have investigated the formation of Hf-Mo binary alloy using the Hf/Mo gate stack. It has been demonstrated that the modulation of Hf atomic fraction in Hf-Mo binary alloy can be achieved by varying the thickness ratio of Hf to Mo. Also, the required thermal budget for prospective Hf-Mo intermixing has been demonstrated to depend on the total metal thickness. Consequently, depositing an Hf/Mo gate stack with an appropriate total thickness and a

required thickness ratio, a precise gate-work-function engineering can be achieved. Moreover, the use of the Hf/Mo gate stack for the formation of Hf-Mo binary alloy can prevent the process integration from leading to the degradation of gate dielectric integrity, since no metal needs to be removed from the gate dielectric interface directly.

3. In chapter 4, we have investigated the formation of molybdenum silicide using the α-Si/Mo gate stack. According to the chemical bond analysis, $MoSi_2$ is speculated to be the main constituent of the formed $MoSi_x$. The work function of formed $MoSi_x$ gate is lower than that of the pure Mo gate. The pure Mo and $MoSi_x$ gates can provide work function values appropriate for *p*- and *n*-channel devices with advanced transistor structures, respectively. Moreover, thermal stabilities of the pure Mo and $MoSi_x$ gates on SiO_2 also have been evaluated to be higher than 950℃. The pre-implantation of arsenic dosage into the α-Si layer also has been demonstrated to lower the work function of formed $MoSi_x$ effectively. Consequently, the pure Mo and $MoSi_x$ gates can provide work function values appropriate for *p*- and *n*-channel bulk devices, respectively.

4. In chapter 5, we have evaluated the properties of pure Mo and $MoSi_x$ gates on the MOCVD HfO_2 gate dielectric. The work function values of pure Mo and $MoSi_x$ on HfO_2 are slightly lower than those on the SiO_2 gate dielectric, but the work function difference between these two gates is independent of the gate dielectric material. The Fermi-level pinning effect, which can be observed in the reported FUSI gates, seems to be either retarded or masked in the $MoSi_x$ gate. To further investigate the pinning effect in the $MoSi_x$ gate, the work function modulation using the pre-implantation of arsenic dosage also has been evaluated.

On the HfO_2 gate dielectric, the work function value of *n*-type $MoSi_x$ has been demonstrated to be lower than that of the undoped $MoSi_x$. The preservation of impurity effect on the work function modulation confirms the retardation of the pinning effect. We speculate that the use of Mo as the first-layer gate electrode can separate the Si atoms from the underlying HfO_2 gate dielectric and effectively avoid the formation of Hf-Si bonds which has been reported to be responsible for the cause of the Fermi-level pinning effect.

6.2 SUGGESTIONS FOR FUTURE WORK

There are some more topics which are valuable for further researches.

1. In Chapter 3, the appropriate wet-etching recipe for selective removal of Hf from Mo should be developed for the device fabrication. Consequently, the proposed dual work function metal gate approach can be further demonstrated by CMOS transistors fabrication.

2. In Chapter 3, the demonstration of the proposed gate-electrode-thin-down process should be investigated further to demonstrate the feasibility of the idea that uses a thicker gate electrode for getting around the thermal stability issue.

3. In Chapter 4, the appropriate wet-etching recipe for selective removal of amorphous Si from Mo should be developed for device fabrication. Consequently, the proposed dual work function metal gate approach can be further demonstrated by CMOS transistors fabrication.

4. In Chapters 4 and 5, the exact mechanism of the work function modulation of $MoSi_x$ by the pre-implantation of arsenic should be investigated to make the whole picture clearer. The SIMS profile can provide more insights about what is really responsible for the flat band voltage shift observed in the arsenic pre-implanted samples.

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Publication List

A. International Journal

1. **Tzung-Lin Li**, Chia-Hsin Hu, Wu-Lin Ho, Howard C.-H. Wang, and Chun-Yen Chang, "Continuous and Precise Work Function Adjustment for Integratable Dual Metal Gate CMOS Technology Using Hf-Mo Binary Alloys," ***IEEE Transactions on Electron Devices***, vol.52, no.6, pp.1172-1179, June 2005.

2. **Tzung-Lin Li**, Wu-Lin Ho, Hung-Bin Chen, Howard C.-H. Wang, Chun-Yen Chang, and Chenming Hu, "Novel Dual Metal Gate Technology Using Mo-$MoSi_x$ Combination," ***IEEE Transactions on Electron Devices***, vol.53, no.6, pp.1420-1426, June 2006.

B. International Conference

1. **Tzung-Lin Li**, Wu-Lin Ho, Howard C.-H. Wang, and Chun-Yen Chang, "Novel Dual Metal Gate Technology Using Mo-$MoSi_x$ for Advanced MOS Device Applications," ***Electrochemical Society Proceeding***, PV. 2005-05, pp.383-388, 2005.

C. Patent

1. Chih-Hao Wang, **Tzung-Lin Li**, Yen-Ping Wang, and Chun-Yen Chang, "Dual Work Function Gate Electrodes," United State Patent (No. 7,018,883).