國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

高介電常數閘極介電質熱氧化氧化鋁在金氧半電晶體的電性及應用

The Electrical Characteristics and Application in MOSFETs of High k Gate Dielectric Al_2O_3 Formed by Aluminum Oxidation

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摘要

由於矽積體電路元件尺寸的縮微，導致不斷的減少閘極氧化層的厚度。然而，隨之而來的高閘極漏電流卻使電晶體的特性變差，並且使元件消耗的功率變大。一個解決的辦法是以高介電常數介電質材料取代傳統熱氧化層，如此可以增加元件的密度而不需要更進一步減少閘極氧化層厚度。雖然高介電常數介電質的使用能有效的減少閘極漏電流，但仍然有一些相關新的問題必須解決。我們發展出一種簡單的沈積介電質的方法，為了避免任何製程在氧化鋁上引起缺陷，先利用物理氣相沈積的方式蒸鍍金屬薄膜，再將其氧化及退火。在我們研究中，我們將氧化鋁沈積在矽基版上，並製作成金氧半電容和電晶體。為了瞭解其被應用為閘極介電質的特性，我們量測了元件參數，閘極漏電流、遷移率和電晶體特性，量測結果顯示，氧化鋁運用在金氧半電容上其漏電流遠低於相同等效厚度的二氧化矽介電質，電子遷移率可比的上文獻發表的熱氧化二氧化矽數據。由電容電壓特性曲線顯示氧化鋁的高介電常數。量測介電質崩潰電壓、定電流應力、定電壓應力和應力產生的漏電流的可靠性測試，根據可靠性分析證實氧化鋁的高品質。

為了研究偏壓溫度不穩定性的影響，將 10MV/cm 的電場和 85°C 溫度應力加在氧化鋁閘極介電質電晶體上量測臨界電壓的改變，在高電場和高溫應力下，由臨界電壓的改變可以推斷 10 年壽命下所能承受的最大閘極電壓僅達到 1 伏特操作下 10% 的安全邊緣。此外，我們分別量測氧化鋁和二氧化矽介電質的閘極漏電流、電荷對介電質的崩潰以及應力產生的漏電流在銅污染下的影響。結果顯示，氧化鋁閘極介電質有強大的銅污染阻隔能力。因此，我們使用的這項製程方法，可以將氧化鋁應用在金氧半電晶體所使用的閘極介電質，此外它同時具有簡單，並且與現有超大型積體電路製程技術相容的優點。

The Electrical Characteristics and Application in MOSFETs of High-k Gate Dielectric Al_2O_3 Formed by Aluminum Oxidation

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Abstract

The scaling-down of silicon integrated circuits has lead to a constant reduction of the thickness of gate oxide. However, the high gate leakage current degrades the performance of transistors and enlarges the power consumption of the devices. A solution is to replace SiO_2 by high dielectric constant insulators, thus allowing an increase of the packing density without a further reduction of gate oxide thickness. Although utilizing high-k dielectrics reduced the gate leakage current effectively, there are still some issues that we have to overcome. We have developed an approach to deposit high-k dielectric. We deposited the ultra thin Al film on Si substrate using PVD followed by oxidation and annealing. The MOS transistor and capacitor devices with Al_2O_3 dielectrics were fabricated. To investigate the characteristics of Al_2O_3 used as gate dielectric, we measured the leakage current, mobility and transistor performance. The result indicates that the leakage current of Al_2O_3 as dielectric of MOS-capacitor is already better than that of SiO_2 and the electron mobility is

comparable to published mobility data from thermal SiO_2. Capacitance-Voltage (C-V) curve shows its higher dielectric constant (k). We also show the high quality of Al_2O_3 dielectric according to its reliability analysis. Reliability tests were carried out by measuring breakdown voltage, constant current stress, constant voltage stress and stress induced leakage current (SILC) effect. To investigate the Bias-Temperature Instability (BTI) effects on Al_2O_3 CMOSFETs, the ΔV_t changes have measured after 10MV/cm and 85°C stress. The 10 years lifetime $V_{max\text{-}10years}$ is from the extrapolation of ΔV_t changes at high gate voltage and high temperature that can barely meet the required 1 V operation with 10% safety margin. Furthermore, to characteristics the Cu contamination effect on Al_2O_3 gate dielectric, we measured the gate dielectric leakage current, charge-to-breakdown and stress-induced leakage current on Al_2O_3 and SiO_2, respectively. The results show the Al_2O_3 gate dielectric has strong Cu contamination resistance. Therefore, using this approach, we can fabricate Al_2O_3 high-k dielectric that is suitable in MOSFETs application. More important, this approach is simple and fully compatible with current VLSI technology.

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***This thesis is dedicated to my family*.**

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Chapter 1

Chapter 1

Introduction

1.1 Background and Motivation of Al_2O_3 High-k Dielectric

Continual the scaling-down of MOS devices has to a constant reduction of the thickness of the gate dielectrics. For sub-0.13 um gate length technologies, an equivalent SiO_2 thickness lower than 15 Å is required. MOS transistor with gate oxide thickness of 15 Å and 13 Å has been demonstrated, respectively [1.1], [1.2]. Nevertheless, silicon dioxide does not satisfy all criteria for an ideal technological insulator, such a low thickness would subjected to several problems for conventional dielectrics, such as silicon oxide, silicon nitride or oxynitride films, in terms of leakage current density and resistance to impurity diffusion. Thereby reducing the thickness with lower leakage current and high resistance to impurity diffusion plays an important role. A solution is to replace these materials by high dielectric constant (high-k) insulators, thus allowing an increase of the packing density without a further reduction of the insulator thickness. Fig. 1-1 shows ITRS projections for low power gate leakage. Actually, novel high-k gate dielectric has been identified in future R & D plan [1.3] as one of the most important factors for deca-nano CMOS technology.

According to the roadmap of ITRS as shown in Table 1-1 and Fig. 1-1, the thickness of gate oxide have be below 13 Å after 2005, and the use high constant dielectrics as insulator to replace SiO_2 has become so widespread in the future gate dielectric. It would seem almost unchangeable [1.4]. Since the leakage current is related to the physical thickness, the increasing thickness can reduce the gate leakage current of the devices. Although high-k dielectric films exhibit smaller band gap, weak bond, and charge trapping than SiO_2. The high-k dielectric films with the same effective oxide thickness (EOT) with SiO_2 provide sufficient gate control with reduce gate leakage. That is the reason why high-k dielectrics have drawn much attention for future gate dielectrics.

Recently, many high-k dielectric candidate materials have widely investigated and the characteristics and issues of those materials have also been reported. Table 1-2 shows the physical properties for various high-k materials. The high-k dielectrics show good performances are always accompanied by other drawbacks. Finding out the most suitable high-k dielectric for device and altering the device structure or process to meet the requirement of the high speed device are significant tasks to implant high-k dielectrics to the next VLSI generation. Many alternatives to SiO_2 have been proposed. Silicon nitride (Si_3N_4) is an attractive candidate for this purpose due to its higher dielectric constant (~7). However, Si_3N_4 has a poor interface with silicon to cause MOSFET's surface mobility degradation and is leaky due to a high trap density in the film. Therefore, it is not an attractive candidate for a future gate dielectric for ULSI [1.5].

Among the high-k simple metal oxide, such as Tantalum oxide (Ta_2O_5) and Titanium oxide (TiO_2) are seriously considered as candidates for advanced CMOS gate dielectric applications. Because of they exhibit the merits including the better capacitance linearity than that SiO_2, the lower process temperature and the larger band gap (4.65eV) than that of the other high-k dielectrics and high reliability [1.6], [1.7]. However, Ta_2O_5 and TiO_2 are not thermally stability when directly contacted to Si substrate [1.8]. They react with Si and form an interfacial low-k dielectric layer. Additional barrier layer has been used to prevent the reaction, but it increases equivalent oxide thickness (EOT) and process complexity [1.9]. In addition, crystallization will cause from post implant RTA.

Recently, HfO_2 and ZrO_2 have attracted much attention due to their thermal stability with poly or TiN and TaN [1.10], [1.11], [1.12]. In addition, they also exhibits suitable dielectric constant (25~30) and energy band gap, for the use of MOSFET in sub-micron generation. However, HfO_2 is poor barrier to oxygen diffusion, oxygen tends to diffuse though HfO_2 and form oxide interlayer after high temperature process and it becomes difficult to achieve the effective oxide thickness below 15 Å. Furthermore, it exists an important issue for the integration of HfO_2 and ZrO_2. The boron penetration effect is severe when single HfO_2 serves as gate dielectric of transistors, while ZrO_2 reacts with poly silicon to form Zr silicide after post implant annealing. This Zr-silicide defects increase the leakage current and degrade the reliability. Besides, both HfO_2 and ZrO_2 will crystallize at the temperature higher than 500^{o}C. After source/drain activation, this property increases the leakage current and power dissipation of the device.

The use of aluminum oxide (Al_2O_3) has attracted much attention because it has some advantage over silicon dioxide (SiO_2) which makes it promising; lower leakage current, greater resistance to ionic motion, greater radiation hardness, the possibility of obtaining low threshold voltage MOSFETs, and possibility of use in nonvolatile memory devices. Balk [1.13] has proposed a set of criteria to be employed in the selection of insulators either instead of, or in conjunction with silicon dioxide (SiO_2) : (1) high dielectric constant, (2) high breakdown strength, (3) an effective barrier against contaminants such as alkali ions, copper and moisture, (4) etchable in liquid etchants at or near room temperature, (5) stable electrical properties when used as gate dielectric in MOSFET, (6) controllable electrical properties when used as nonvolatile memory elements. Al_2O_3 fulfills many of these requirements very well. Al_2O_3 is believed to be more resistant to ion penetration than silicon dioxide (SiO_2). Besides, its very high dielectric constant (~10) that can be used for next generation MOSFETs and memory application.

1.2 The Formation of Al_2O_3 High-k Dielectric

Many methods to deposit ultra thin high-k dielectrics on substrates have been proposed in recent years and various methods exhibit the merits as well as some other issues that have to be solved.

In this study, we used the advance deposition method to fabricate Al_2O_3 high-k dielectrics. We utilized the self-limit property of Al_2O_3 to prevent from the formation of interface oxide and have the effect of aluminum doping at the same time. The pre-cleaned wafer was loaded in the chamber under high vacuum condition, and then aluminum layer was deposited in evaporation on Si Substrate. Because extremely high quality is required for gate dielectric, we have used thermally grown Al_2O_3 from oxidized Al on Si-substrate. In comparison, sputtering and oxygen plasma have been used in the past to deposit aluminum oxide. However, high defects can be expected from Ar-ion bombardment and oxygen plasma respectively [1.14]. The MOS transistor and capacitor devices with Al_2O_3 dielectrics are fabricated and measured. It is found in our study that the self-limiting oxidation mechanism is one of the important merits of Al_2O_3 for either reproducibility or uniformity control. We have first characterized the electrical property of Al_2O_3 as dielectric of MOS-capacitor to figure out if this material can be used as a gate dielectric of a MOSFET. Then we applied it to be gate dielectric of a MOSFET and characterized its electrical properties.

1.3 The Measurement of the Devices

To investigate the electrical characteristics of MOSFETs, we measured the leakage current, stress induced leakage current and V_t degradation using HP4156C semiconductor parameter analyzer with high temperature chuck. Besides, HP4284A precision LCR meter was used to evaluate the capacitance at a high frequency 100KHz and a quasi-static frequency 10Hz. The thickness of the aluminum oxide film was measured by a single wavelength ellipsometer. We assumed the oxide layer was homogeneous with a refractive index n=1.76 (typical of bulk aluminum oxide). The structure and atomic composition of capacitor samples were investigated by micro analyses, such as secondary ion mass spectrometry (SIMS). For the SIMS analysis, we can determine the oxide and aluminum diffusion profile into silicon. The leakage current of 48 Å Al_2O_3 as dielectric of MOS-capacitor is already better than that of SiO_2 with the same equivalent thickness of 13 Å. Capacitance-Voltage (C-V) curve shows its higher dielectric constant (k). Besides, the effective mobility of Al_2O_3 gate MOSFETs is closed to the effective mobility of traditional SiO_2 gate MOSFETs. The interface trap density was calculated from high-low capacitance method. We also show the high quality of Al_2O_3 dielectric according to its reliability analysis. Capacitor reliability tests were carried out by measuring constant current stress, constant voltage stress and SILC (Stress Induced Leakage Current) effect. To investigate the Bias-Temperature Instability (BTI) effects on fully silicided-gate/Al_2O_3 CMOSFETs. The ΔV_t changes have measured after 10MV/cm and 85°C stress. The 10 years lifetime $V_{max\text{-}10years}$ is from the extrapolation of ΔV_t changes at high gate voltage and high temperature. Furthermore, to characteristics the Cu contamination effect on Al_2O_3 gate dielectric, we measured the gate dielectric leakage current, charge-to-breakdown and stress-induced leakage current on Al_2O_3 and SiO_2, respectively. These results suggest the possible application of aluminum oxide (Al_2O_3) to the next generation of VLSI.

1.4 Thesis Outline

In this thesis, we performed a high-k dielectric Al_2O_3 for the MOSFETs device by thermal oxidizing the thin Al and than studied the electrical properties and mechanism of Al_2O_3 dielectric. Moreover, we have studied the Bias-Temperature Instability (NBTI) on fully Nickel silicide (NiSi) and germanided (NiGe) gate on high-k Al_2O_3 nMOSFETs and pMOSFETs, respectively. Finally, the Cu contamination on Al_2O_3 gate dielectric was characterized.

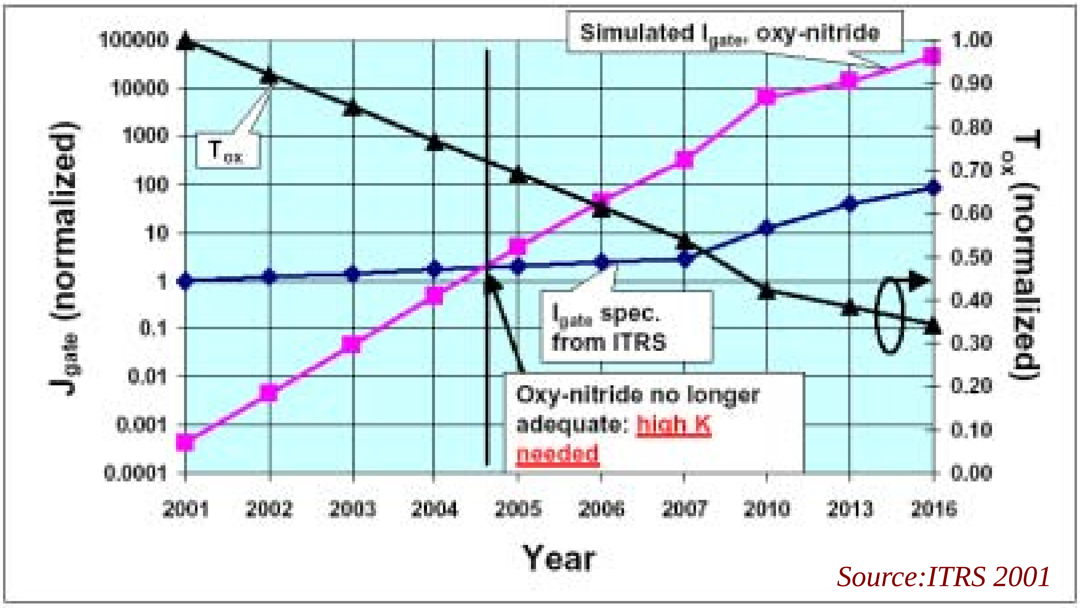
In Chapter 2, we have studied the Al_2O_3 to use as an alternative gate dielectric. To ensure good quality, Al_2O_3 is thermally oxidized from MBE-grown AlAs or Al on Si-substrates. Experimental results indicate that the leakage current from oxidized AlAs is larger than that from directly oxidized Al, which may be due to the weak As_2O_3 inside Al_2O_3. The leakage current of a 53 Å Al_2O_3 is already lower than that of SiO_2 with an equivalent oxide thickness of 21 Å.

In Chapter 3, firstly we have reported a very simple process to fabricate Al_2O_3 gate dielectric with k (9.0 to 9.8) greater than Si_3N_4. Al_2O_3 is formed by direct oxidation from thermally evaporated Al. The 48 Å Al_2O_3 has ~6 orders lower leakage current than equivalent 13 Å SiO_2. Good Al_2O_3/Si interface was evidenced by the low interface density of $1x10^{11}$ $eVcm^{-2}$ and compatible electron mobility with thermal SiO_2. Good reliability is measured from the small SILC after 2.5 V stress for 10,000s. Secondly high quality La_2O_3 was fabricated with EOT of 9.6 Å, leakage current of 0.4 A/cm^2 and D_{it} of both $3x10^{10}$ eV^{-1}/cm^2. The high-k is further evidenced from high MOSFET's I_d and g_m with low I_{off}. Good SILC and Q_{BD} are obtained and comparable with SiO_2. The low EOT is due to the high thermodynamic stability in contact with Si and stable after H_2 annealing up to 550°C.

In Chapter 4, we have studied the Bias-Temperature Instability (BTI) on fully Nickel silicided (NiSi) and germanided (NiGe) gate on high-k Al_2O_3 nMOSFETs and pMOSFETs, respectively. At an equivalent-oxide thickness (EOT) of 17 Å, the NiSi/Al_2O_3 pMOSFETs and NiGe/Al_2O_3 nMOSFETs have comparable threshold voltage (V_t) change of -34 and 33 mV at 85°C and 10 MV/cm stress for 1 hour. This result is quite different from the more severe native BTI (NBTI) degradation measured in oxynitride pMOSFET than positive BTI (PBTI) in nMOSFET. The extrapolated maximum voltage for 10 years lifetime is 1.16 and -1.12 V from NiSi-NiGe/Al_2O_3 CMOSFETs that can barely meet the required 1 V operation with 10% safety margin. However, further improvement is still required since the 18 Å oxynitride CMOSFETs have higher 10 years lifetime operation voltage of 2.48 and -1.52 V for PBTI and NBTI, respectively.

In Chapter 5, we have studied the Cu contamination effect on 42 Å thick Al_2O_3 MOS capacitors with an equivalent-oxide thickness (EOT) of 19 Å. In contrast to the large degradation of gate oxide integrity of control 30 Å SiO_2 MOS capacitors contaminated by Cu, the 19 Å EOT Al_2O_3 MOS devices have good Cu contamination resistance with only small degradation of gate dielectric leakage current, charge-to-breakdown and stress-induced leakage current. This strong Cu contamination resistance is similar to oxynitride (with high nitrogen content) but the Al_2O_3 gate dielectric has the advantage of higher-k value and lower gate dielectric leakage current.

Finally, conclusions and the future prospects were given in Chapter 6.



Source:ITRS 2001

Fig. 1-1 ITRS projections for low power gate leakage.

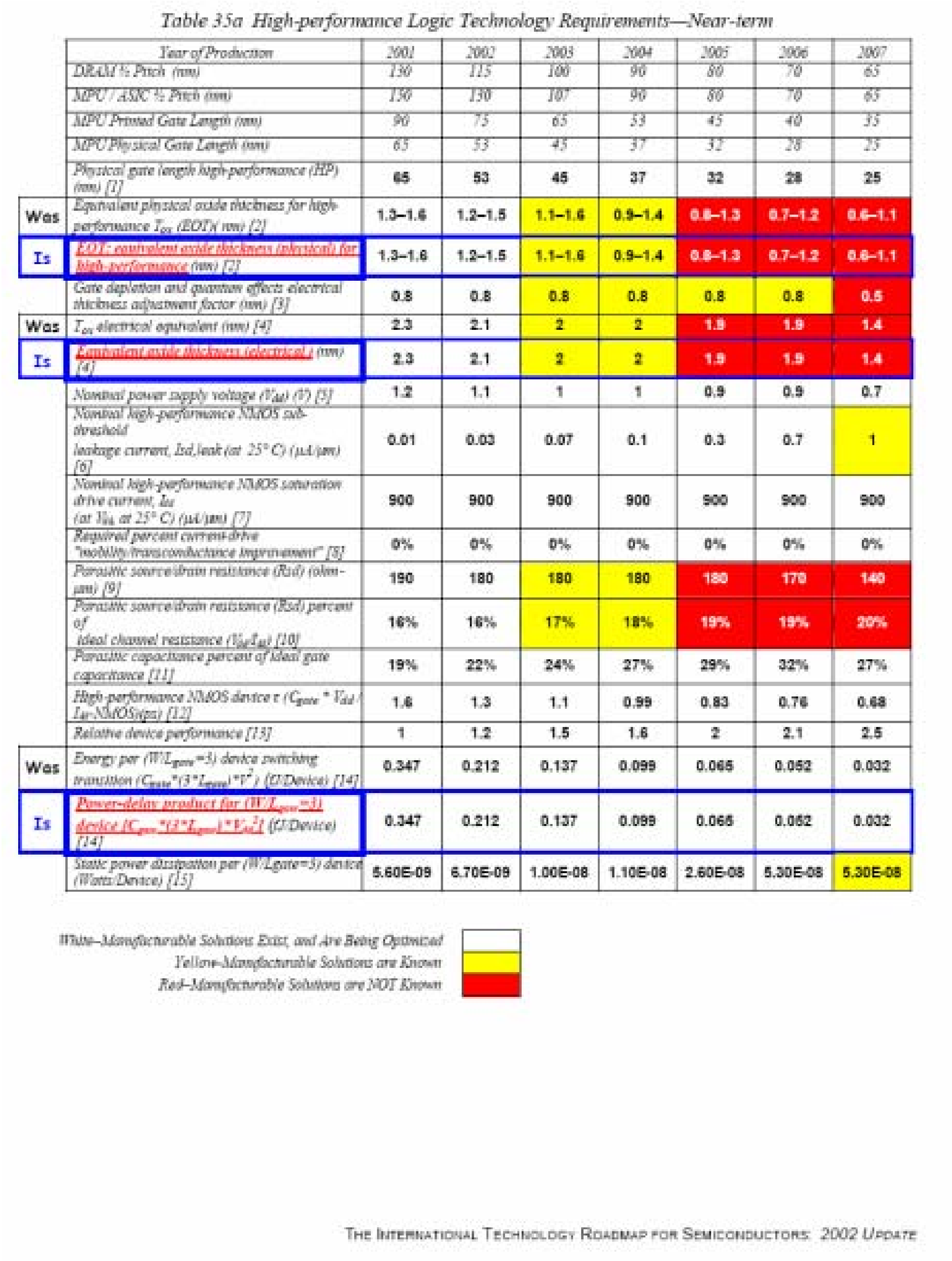


Table 35a High-performance Logic Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Physical gate length high-performance (HP) (nm) [1]	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Was	Equivalent physical oxide thickness for high-performance T_{ox} (EOT)(nm) [2]	**1.3–1.6**	**1.2–1.5**	**1.1–1.6**	**0.9–1.4**	**0.8–1.3**	**0.7–1.2**	**0.6–1.1**
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	**1.3–1.6**	**1.2–1.5**	**1.1–1.6**	**0.9–1.4**	**0.8–1.3**	**0.7–1.2**	**0.6–1.1**
	Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.5**
Was	T_{ox} electrical equivalent (nm) [4]	**2.3**	**2.1**	**2**	**2**	**1.9**	**1.9**	**1.4**
Is	Equivalent oxide thickness (electrical) (nm) [4]	**2.3**	**2.1**	**2**	**2**	**1.9**	**1.9**	**1.4**
	Nominal power supply voltage (V_{dd}) (V) [5]	**1.2**	**1.1**	**1**	**1**	**0.9**	**0.9**	**0.7**
	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25° C) (μA/μm) [6]	**0.01**	**0.03**	**0.07**	**0.1**	**0.3**	**0.7**	**1**
	Nominal high-performance NMOS saturation drive current, I_{dd} (at V_{dd}, at 25° C) (μA/μm) [7]	**900**	**900**	**900**	**900**	**900**	**900**	**900**
	Required percent current-drive "mobility/transconductance improvement" [8]	**0%**	**0%**	**0%**	**0%**	**0%**	**0%**	**0%**
	Parasitic source/drain resistance (Rsd) (ohm-μm) [9]	**190**	**180**	**180**	**180**	**180**	**170**	**140**
	Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	**16%**	**16%**	**17%**	**18%**	**19%**	**19%**	**20%**
	Parasitic capacitance percent of ideal gate capacitance [11]	**19%**	**22%**	**24%**	**27%**	**29%**	**32%**	**27%**
	High-performance NMOS device τ (C_{gate} * V_{dd} / I_{d}-NMOS)(ps) [12]	**1.6**	**1.3**	**1.1**	**0.99**	**0.83**	**0.76**	**0.68**
	Relative device performance [13]	**1**	**1.2**	**1.5**	**1.6**	**2**	**2.1**	**2.5**
Was	Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (J/Device) [14]	**0.347**	**0.212**	**0.137**	**0.099**	**0.065**	**0.052**	**0.032**
Is	Power-delay product for (W/L_{gate}=3) device (C_{gate}*(3*L_{gate})*V_{dd}^2) (J/Device) [14]	**0.347**	**0.212**	**0.137**	**0.099**	**0.065**	**0.052**	**0.032**
	Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	**5.60E-09**	**6.70E-09**	**1.00E-08**	**1.10E-08**	**2.60E-08**	**5.30E-08**	**5.30E-08**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: *2002 UPDATE*

Table 1-1 The International Technology Roadmap of ITRS for Semiconductor 2002.

Material	**Dielectric constant (k)**	**Band gap Eg(eV)**	**ΔEc (eV) to Si**	**Contact stability with Si (KJ/mole) Si+Mox--> M+ SiO**	**Crystal structure**
SiO_2	3.9	8.9	3.2	Stable	Amorphous
Al_2O_3	9	8.7	2.8	63.4	Amorphous
La_2O_3	30	4.3	2.3	98.5	Amorphous
HfO_2	25	5.7	1.5	47.6	Crystal T>700C
ZrO_2	25	7.8	1.4	42.3	Crystal T>400~800C
TiO_2	80	3.5	1.2	-	Tetragonal

Table 1-2 Physical properties for various high-k materials.

Chapter 2

Electrical characterization of Al_2O_3 on Si from thermally oxidized AlAs and Al

2.1 Introduction

It has been shown that the practical scaling limit for gate oxide is due to the leakage current by direct-tunneling process [2.1], although 11-15 Å direct-tunneling gate oxide has already been demonstrated [2.2], [2.3]. The thickness of thermally grown gate oxide is scaled down to 35-40 Å for the 0.18-µm VLSI generation, and further scaling down below 15 Å is required within a few years [2.4]. Unfortunately the large direct-tunneling current precludes the use of silicon dioxide (SiO_2) below 15-20 Å thickness. However, continuously scaling down the gate oxide is necessary to increase the current drive capability of MOSFETs and the operation speed of ICs. The relationship of drive current and gate oxide thickness is shown in equation (1):

$$I_{Dsat} = \frac{1}{2}\,\bar{\mu}_n \frac{W}{L} \frac{\varepsilon_0 K A}{t_{ox}} (V_G - V_T)^2 \qquad (1)$$

where I_{Dsat} is the device saturation current, V_G is the applied gate voltage and k is the dielectric constant of gate capacitor. The only solution to overcome this difficulty and to continuously scale down the gate dielectric is to use a thicker dielectric with a higher k value. Therefore novel high-k gate dielectric has been identified as one of the most important R & D plans [2.4] for deca-nano CMOS technology. Unfortunately, because of the stringent requirements for device quality gate dielectric, no satisfactory alternatives to SiO_2 has so far been found. Recently, aluminum oxide (Al_2O_3) has attracted much attention because of its very high dielectric constant (~10) that can be used for next generation DRAM and Flash memory application [2.5]. Moreover, Al_2O_3 has also been treated as a gate barrier in InAlAs/InGaAs MESFET using plasma oxidation of deposited Al [2.6]. In this study, we have first characterized the electrical property of Al_2O_3 to use as an alternative gate dielectric of MOSFETs. Because extremely high quality is required for gate dielectric, we have used thermally grown Al_2O_3 from oxidized AlAs or Al that were grown in an ultra-high vacuum molecular beam epitaxy (MBE) system. In comparison, sputtering deposition and O_2 plasma oxidation have been used in the past to deposit Al_2O_3; however high defects can be expected from Ar^+ bombardment and plasma damage, respectively. In this work, the leakage current of a 53 Å Al_2O_3 from direct oxidized Al is already better than that of SiO_2 with the equivalent thickness of 21 Å [2.2]. This result suggests the possible application of Al_2O_3 to VLSI.

2.2 Experimental

P-type 4-inch [100] Si wafers with typical resistivity of 10 ohm-cm are used in this study. After modified RCA cleaning, HF dipping, rinsing in DI water and spun dry, the wafer was treated by HF-vapor passivation and immediately loading into the MBE chamber. The HF-vapor passivation has been used to reduce thermal budget to desorb the native oxide [2.7]. Then 40-80 Å AlAs or 40-55 Å Al were grown by MBE at 500°C. The oxidation process was performed in a standard furnace at 500°C for 90 min., and the dielectric thickness was measured by an ellipsometer. After oxidation, 3000 Å poly-Si was deposited followed by phosphorus doping using $POCl_3$ at 850°C. The wafers were then received a 30-min. nitrogen anneal at 800°C. This anneal was found to be very effective to reduce dielectric leakage current. Subsequently, 3000 Å Al was deposited and gate electrode was defined by patterning and wet etching. The gate dielectrics were electrically characterized by I-V leakage current using a semiconductor parameter analyzer, and the composition profiles were measured using secondary ion mass spectroscopy (SIMS).

2.3 Results and Discussion

Fig. 2-1 presents the SIMS profiles of oxidized AlAs at 500°C, where O, Al and As are detected within the oxidized layer. The possible AlAs oxidation process is in the following equation:

$$AlAs + 3/2\ O_2 \rightarrow 1/2\ Al_2O_3 + 1/2\ As_2O_3 \tag{2}$$

Therefore both Al_2O_3 and As_2O_3 are formed during AlAs oxidation. As shown in Fig. 2-1, significant Al and As diffusion into Si is observed. The diffused As into Si will behave as a n-type dopant and change the threshold voltage, while the amount of diffused Al is dependent on the solid solubility of Si. However, none of these effects are desirable for MOS devices. The reduced surface concentration of As is due to the out-diffusion into ambient during oxidation.

Fig. 2-2 shows the SIMS profile of oxidized Al. The O_2 concentration decreases to its background value as increasing depth beyond the oxidized layer. This is because the Si oxidation rate is negligibly slow at this temperature. In sharp contrast to AlAs oxidation, the oxidized Al shows a much sharper SIMS profiles. Possible reason may be due to the absence of As-enhanced diffusion during oxidation. Another advantage of direct Al oxidation may be due to the strong bonding energy of Al_2O_3 instead of As_2O_3 from oxidized AlAs. Therefore, the oxidized Al films may provide not only better material quality but also lower diffusion into Si during oxidation.

We have further characterized the electrical behavior of these oxides. Fig. 2-3 shows the typical J-V characteristics of MOS capacitors from oxidized AlAs. The capacitor leakage current reduces with increasing dielectric thickness from 80 to 130 Å. This is a typical behavior because a thicker insulating barrier has lower electric field that can block the electron transport more easily. However, this thicker insulating barrier did not successfully reduce the leakage current at low voltages less than ~0.7 V. Possible reasons may be due to trap-assisted tunneling at low electric field [2.8]. The traps may be generated by the weak bonding strength of As_2O_3 inside Al_2O_3 matrix or vacancies by As out-diffusion.

To investigate the effect of As-related weak As_2O_3 or vacancies, we have studied the electric characteristic of capacitors with directly oxidized Al. In comparison the J-V characteristics of ~ 80 Å oxides in Figs. 2-3 and 2-4, a much lower leakage current is observed at gate voltage below 1 V from directly oxidized Al. This leakage current at low gate electric field is related to the intrinsic defects [2.8] that is similar to stress-induced leakage current (SILC) [2.7], [2.9]. Therefore the As-related weak As_2O_3 or vacancies are responsible to the increased oxide leakage current. The almost same current at high voltages is due to the dominated tunneling mechanism. We have further compared the leakage current of Al_2O_3 with SiO_2 from the published I-V characteristic [2.2]. It is important to note that the leakage current of 53 Å Al_2O_3 is already better than the leakage current of MOS capacitors with the same equivalent thickness of 21 Å thick SiO_2 [2.2].

2.4 Conclusion

We have studied the thermally oxidized AlAs and Al to use as an alternative gate dielectric. The leakage current from AlAs oxidation is larger than that from Al oxidation at low voltages. The leakage current of a 53 Å Al_2O_3 is already lower than SiO_2 with an equivalent oxide thickness of 21 Å. These results suggest that scaling equivalent oxide thickness below 13 Å is possible using the Al_2O_3 films.

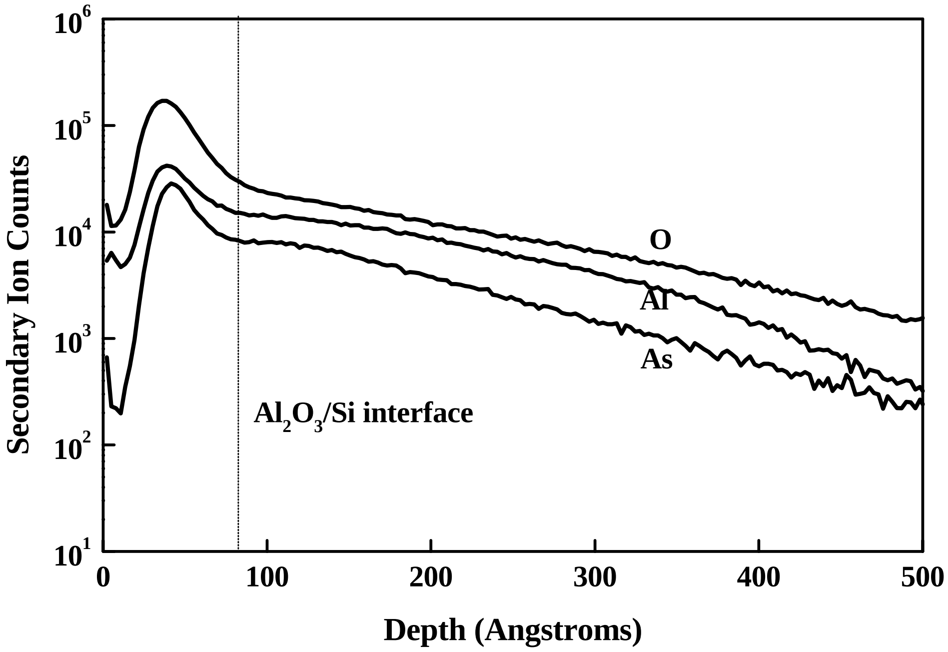


Fig. 2-1 SIMS depth profiles of oxidized AlAs at 500°C.

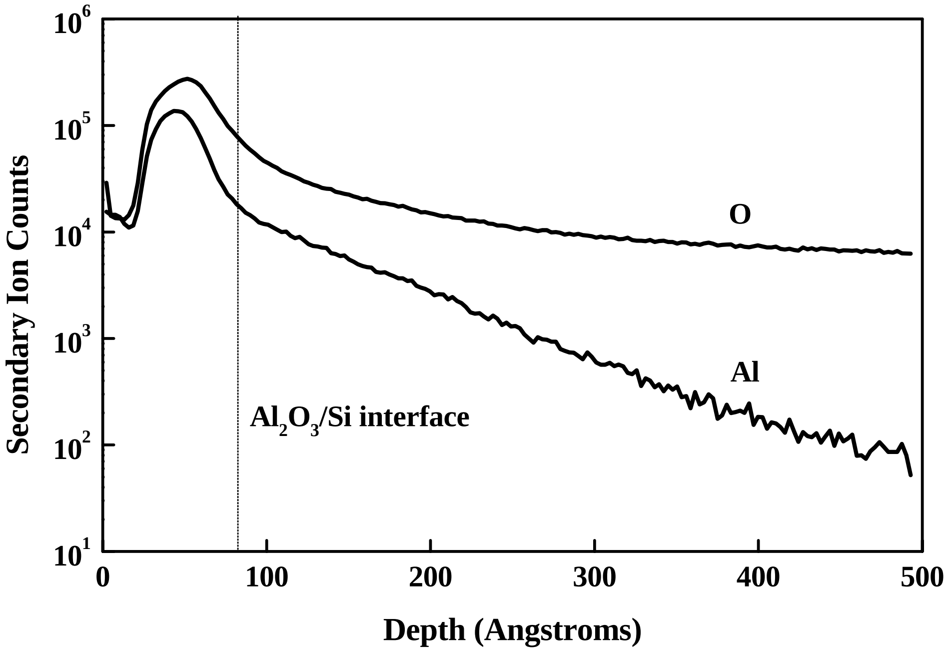


Fig. 2-2 SIMS depth profiles of oxidized Al at 500°C.

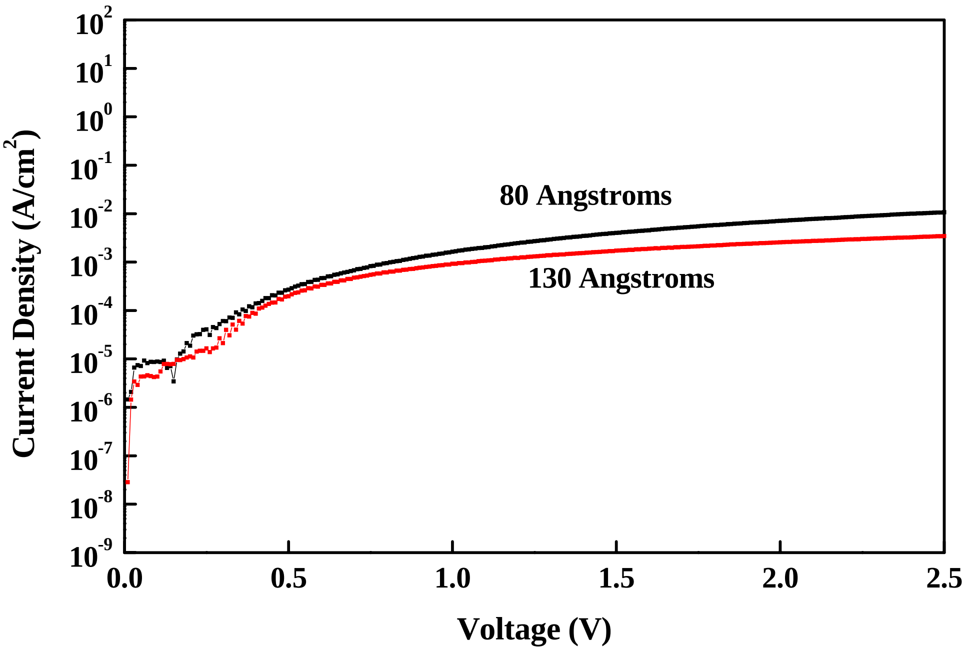


Fig. 2-3 J-V characteristic of MOS capacitors with deposited AlAs oxidized at a temperature of 500°C to form Al_2O_3 dielectric. The capacitor area is 800μm×800μm.

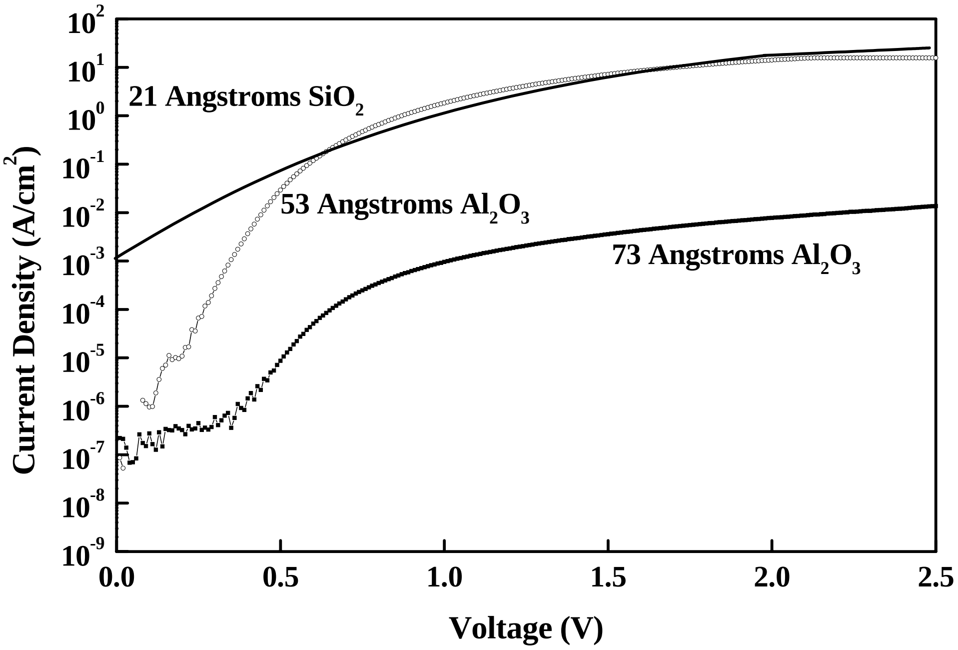


Fig. 2-4 J-V characteristic of MOS capacitors with deposited Al oxidized at a temperature of 500°C to form Al_2O_3 dielectric. The capacitor area is 800μm╳800μm. The J-V characteristic of 21 Å SiO_2 is from reference 2.

Chapter 3

Device and Reliability of High-k Al_2O_3 and La_2O_3 Gate Dielectric with Good Mobility and Low D_{it}

3.1 Introduction

By continuously scaling down the CMOS technology, ultra-thin high-k gate dielectrics with low leakage current are required to replace the direct-tunneling current dominated thermal SiO_2. Recently Si_3N_4 gate dielectric has been studied extensively to replace thermal SiO_2 [3.1]; however, the marginal improvement beyond SiO_2 is due to the relatively lower k and slightly higher leakage current. Although stacked high-k materials have been studied to achieve higher k value than that of Si_3N_4 [3.2], [3.3], it may require complicated process steps and the leakage current is still higher than expected. In this study, we report a very simple process to fabricate Al_2O_3 as an alternative gate dielectric with a k value (9.0 to 9.8) greater than Si_3N_4. To avoid any process related damage, Al_2O_3 gate dielectric is formed by direct oxidation from thermally evaporated Al. In addition to high-k, the 48 Å Al_2O_3 has ~6 orders lower leakage current than equivalent 13 Å SiO_2. Good mobility, interface trap density, and reliability are also achieved using this process.

Although high-k gate dielectrics have attracted much attention recently, further reduction of EOT may be limited by the interface reaction region between high-k material and Si [3.4], [3.5]. Therefore, the search for thermodynamically stable high-k dielectric directly on Si is important to meet future sub-10 Å requirement. Besides the required good electrical properties such as low interface trap density (D_{it}), low leakage current, high breakdown field (E_{BD}) and good reliability, high-k material must also be compatible with existing VLSI process. Thus, good stability with H_2 and high transition temperature from amorphous to crystal [3.5] are necessary to prevent dielectric degradation by H_2 and crystalline structure created defects or dislocations during strain relaxation in process. Previously, we have worked that amorphous Al_2O_3 directly on Si can meet near all the requirements and stable up to 1000^oC [3.6], except that EOT (21 Å) and D_{it} ($1x10^{11}$ eV^{-1}/cm^2) are still high. The high D_{it} is unacceptable for IC because of the increased noise [3.7]. In this study, we have used amorphous La_2O_3 (k~27) to achieve 4.8 Å EOT and reduced Al_2O_3 EOT to 9.6 Å, where La_2O_3 has similar property as Al_2O_3 but with even better thermal stability on Si (Table 1-2). In addition to respective low leakage current of 0.06 and $0.4A/cm^2$ for La_2O_3 and Al_2O_3, both dielectrics now have good D_{it} ($3x10^{10}$ eV^{-1}/cm^2), E_{BD}, SILC, and Q_{BD} as compared with SiO_2.

3.2 Device and Reliability of High-k Al_2O_3 Gate Dielectric

3.2.1 Experimental

To avoid any possible process-related damage in Al_2O_3 gate dielectric [3.8], we have used direct thermal oxidation from thermally evaporated Al on Si. Native oxide is suppressed by a HF-vapor passivation and desorbed *in-situ* inside an ultra-high vacuum MBE environment [3.9], followed by an immediate Al evaporation. Deposited Al was oxidized at a temperature of 400^oC to form Al_2O_3. Then the Al_2O_3 was annealed in nitrogen ambient to reduce defects. Poly-Si gate MOS capacitor and transistor were fabricated to evaluate the electrical characteristics. The suppression of native oxide is important to achieve higher k in Al_2O_3, and we have used similar idea to achieve atomically smooth ultra-thin oxide with good electrical characteristics and reliability [3.10]. For comparison, MOS capacitor and transistor were also fabricated by thermal SiO_2.

3.2.2 Results and Discussion

3.2.2.1 The physical property of Al_2O_3

We have first measured the SIMS profile in Fig. 3-1 to confirm the formation of Al_2O_3. Although Al diffusion into Si can be observed, the concentration reduces rapidly as increasing thickness into Si. Fig. 3-2(a) and 3-2(b) illustrates the TEM photos of Al oxidized at 400^oC and 500^oC, respectively. The crystalline structure is observed in Al_2O_3 bulk oxidized at 500°C. We have also used C-V measurement to determine the Al diffusion and the concentration is lower than 1×10^{16} cm^{-3}. Furthermore, the field-dependent mobility also suggests the low Al diffusion into Si.

3.2.2.2 Gate capacitor

Fig. 3-3 presents the J-V characteristic of a 48 Å Al_2O_3 capacitor. The leakage current is ~6 orders of magnitude lower than that of the equivalent 13 Å thermal SiO_2. In order to obtain an accurate k value, we have also measured the C-V of a thick 110 Å Al_2O_3 capacitor. As shown in Fig. 3-4, a k value of 9.0 is measured that is higher than Si_3N_4. In Fig. 3-5 presents the measured interface trap density with a mid-gap value of 1×10^{11} $eVcm^{-2}$ from this capacitor. This low interface trap density is suitable for MOSFET application.

3.2.2.3 Mobility and transistor performance

To further characterize the Al_2O_3/Si interface, we have fabricated a wide gate MOSFET to measure the electron mobility. Fig. 3-6 shows the effective mobility of an 80 Å Al_2O_3 MOSFET. The electron mobility is comparable to published mobility data from thermal SiO_2. Fig. 3-7 shows the I_d-V_d characteristics of an 80 Å Al_2O_3 MOSFET with a gate length of 10-μm. The higher current drive of Al_2O_3 MOSFET than that of thermal SiO_2 also proves the high-k value in Al_2O_3 MOSFET and a k of 9.8 is obtained.

3.2.2.4 Reliability

Fig. 3-8 and Fig. 3-9 show the 48 Å Al_2O_3 gate dielectric under a 2.5 V constant stress for 10,000 sec, and good reliability is evidenced from the very small current change and stress-induced leakage current (SILC) respectively. Fig. 3-10 and Fig. 3-11 present the same Al_2O_3 gate dielectric under a much higher stress of ~5.4 V with a 0.1 mA/cm^2 constant current density for 1000 sec. The small voltage changes less than 0.04 V and the small SILC also suggest the excellent reliability. Therefore, the Al_2O_3 gate dielectric is suitable for continuously operation at VLSI generations of 2.5 V and beyond.

3.3 Device and Reliability of High-k La_2O_3 Gate Dielectric

3.3.1 Experimental

To avoid any k value reduction, interfacial native oxide is suppressed by HF-vapor passivation and *in-situ* desorption [3.6] followed by an immediate La or Al evaporation. Because La or Al is highly reactive with O_2, low oxidation temperatures

≤ 400°C is used to reduce metal diffusion into Si. The formed oxides were further annealed in N_2 at 900°C. To reduce gate depletion, Al gate is used for MOS capacitor and transistor to evaluate the electrical characteristics. H_2 annealing at 450-550°C is performed to study the stability with H_2. Besides achieved higher k, suppression of native oxide is important to obtain a smooth interface, low D_{it}, and high reliability in our previously achieved atomically smooth ultra-thin oxides.

3.3.2 Results and Discussion

3.3.2.1 Gate capacitor

Fig. 3-12 presents the J-V characteristics of La_2O_3 and Al_2O_3 capacitors. Comparable leakage current for La_2O_3 on Si or $Si_{0.3}Ge_{0.7}$ I s obtained that is important for high mobility PMOS [3.11]. The stacked Al_2O_3/La_2O_3 is used to reduce leakage current for C-V to obtain D_{it}. In order to get accurate k and EOT, the oxide thickness is carefully examined by both ellipsometer and TEM in Fig. 3-13. The very uniform oxide and smooth interface are due to native oxide free surface and high thermal stability in Table 1-2 as contact with Si. Therefore, low EOT can be expected. Fig. 3-14 shows the cumulative values for high-k oxides, and leakage current of 0.06 A/cm^2 for La_2O_3 and 0.4 A/cm^2 for Al_2O_3 are obtained. Fig. 3-15 is the C-V curves and k values of 27 and 8.5 are measured for respective La_2O_3 and Al_2O_3 that gives the low

4.8 Å and 9.6 Å EOT (without QM correction). Small hysterisis of 11 and 22 mV are measured for respective dielectrics that indicates good quality because of applied high annealing temperature without transition to crystal structure [3.5]. Fig. 3-16 shows the measured D_{it} of $3x10^{10}$ eV^{-1}/cm^2 from both capacitors. This low D_{it} close to thermal SiO_2 is extremely important for circuit to lower 1/f noise [3.7].

3.3.2.2 Transistor performance with 4.8 Å EOT

We have further fabricated wide gate MOSFETs with 4.8 Å EOT. Figs. 3-17 shows the device I_d-V_d, and important I_d-V_g and g_m are plotted in Fig. 3-18. The very high current drive and g_m are due to high-k that gives a k of ~27 consistent with C-V measurement. Good device pinch-off $I_{off} < 10^{-10}$ A/μm and small sub-threshold swing of 75 mV/decade are observed, and the small swing also suggests the low D_{it}. The effective mobility is further plotted in Fig. 3-19. The electron mobility is comparable with published universal mobility data for thermal SiO_2 because of low D_{it}.

3.3.2.3 Reliability

Fig. 3-20 shows the gate dielectrics under a -2.5 V constant stress for 1 hour with total Q_{inj} of $1.3x10^3$ and $1.2x10^5 C/cm^2$ for La_2O_3 and Al_2O_3, respectively. No significant charge trapping is occurred during stress, and small SILC for both dielectrics is observed in Fig. 3-21. Good reliability for 4.8 Å EOT La_2O_3 is evidenced from the high Q_{BD} in Fig. 3-22 and comparable with current SiO_2 [3.12]. The good SILC and Q_{BD} may be due to the high lattice energy in Table 1-2. From the 50% failure time, an extrapolated max voltage of 2.3 V is obtained for 10 years lifetime that suggests good reliability for VLSI application with 4.8 Å EOT and small leakage of 0.06 A/cm^2 at 1 V.

3.4 Conclusion

We report a very simple process to fabricate Al_2O_3 gate dielectric with k (9.0 to 9.8) greater than Si_3N_4. Al_2O_3 is formed by direct oxidation from thermally evaporated Al. The 48 Å Al_2O_3 has ~6 orders lower leakage current than equivalent 13 Å SiO_2. Good Al_2O_3/Si interface was evidenced by the low interface density of 1x10^{11} eVcm^{-2} and compatible electron mobility with thermal SiO_2. Good reliability is measured from the small SILC after 2.5 V stress for 10,000 sec.

High quality La_2O_3 and Al_2O_3 are fabricated with EOT of 4.8 and 9.6 Å, leakage current of 0.06 and 0.4 A/cm^2 and D_{it} of both 3x10^{10} eV^{-1}/cm^2, respectively. The high-k is further evidenced from high MOSFET's I_d and g_m with low I_{off}. Good SILC and Q_{BD} are obtained and comparable with SiO_2. The low EOT is due to the high thermodynamic stability in contact with Si and stable after H_2 annealing up to 550°C.

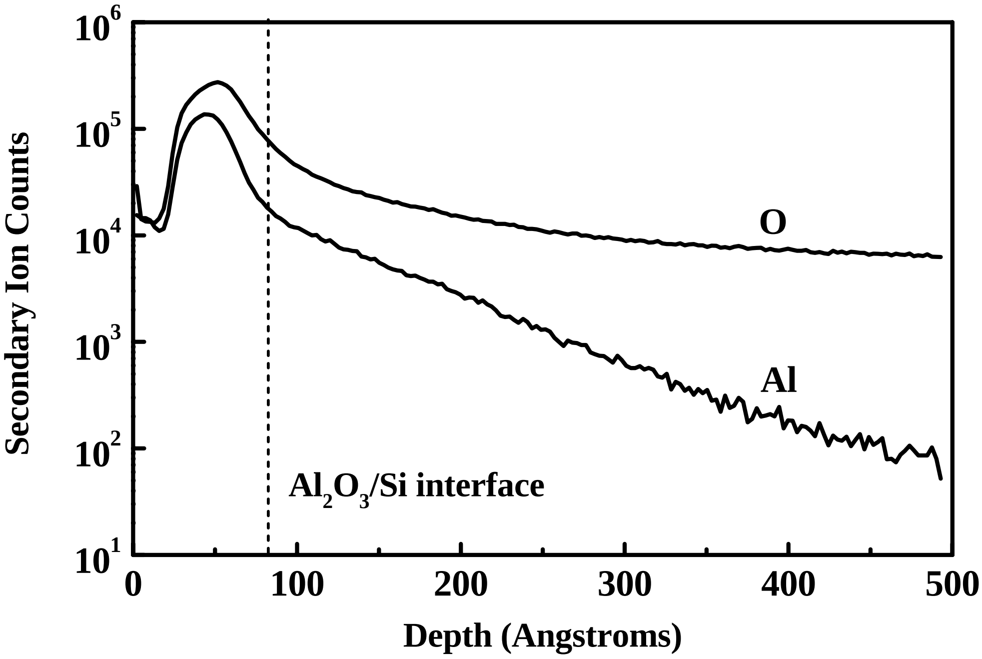
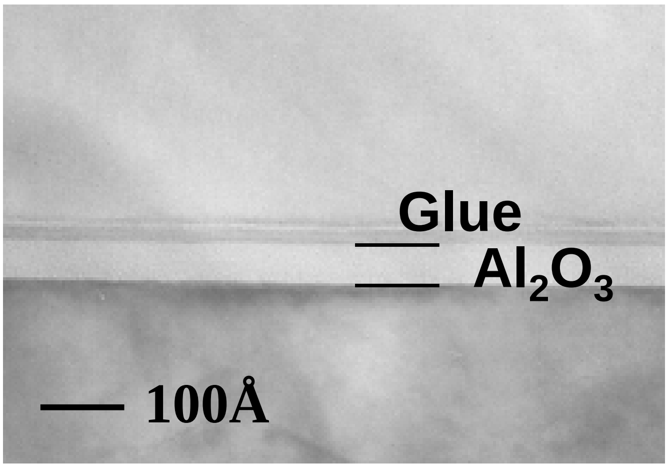
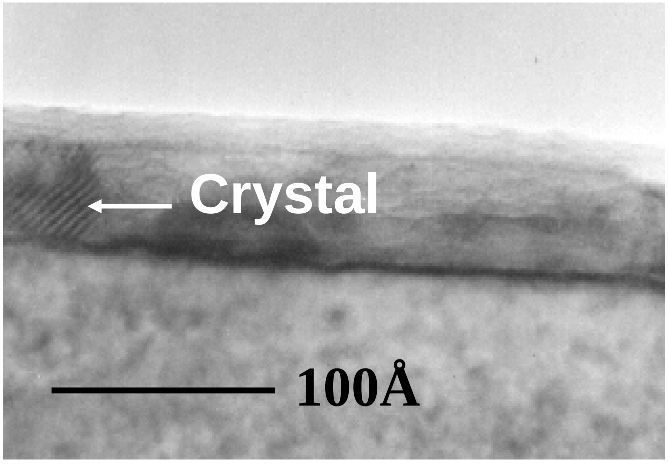


Fig. 4-1 SIMS depth profile of oxidized Al at 500^{o}C. The measured thickness is close to that measured by ellipsometer & cross-sectional TEM.



(a)



(b)

Fig. 3-2 TEM photos of Al oxidized at (a) 400°C and (b) 500°C.

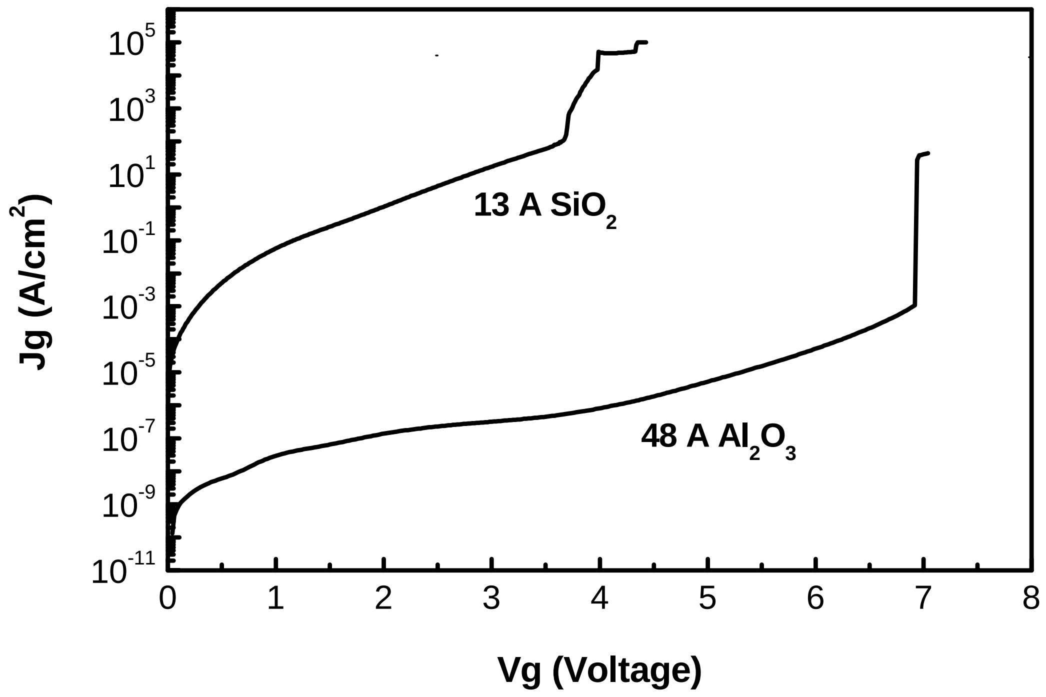


Fig. 4-2 J-V characteristics of the 48 Å Al_2O_3 MOS capacitor.

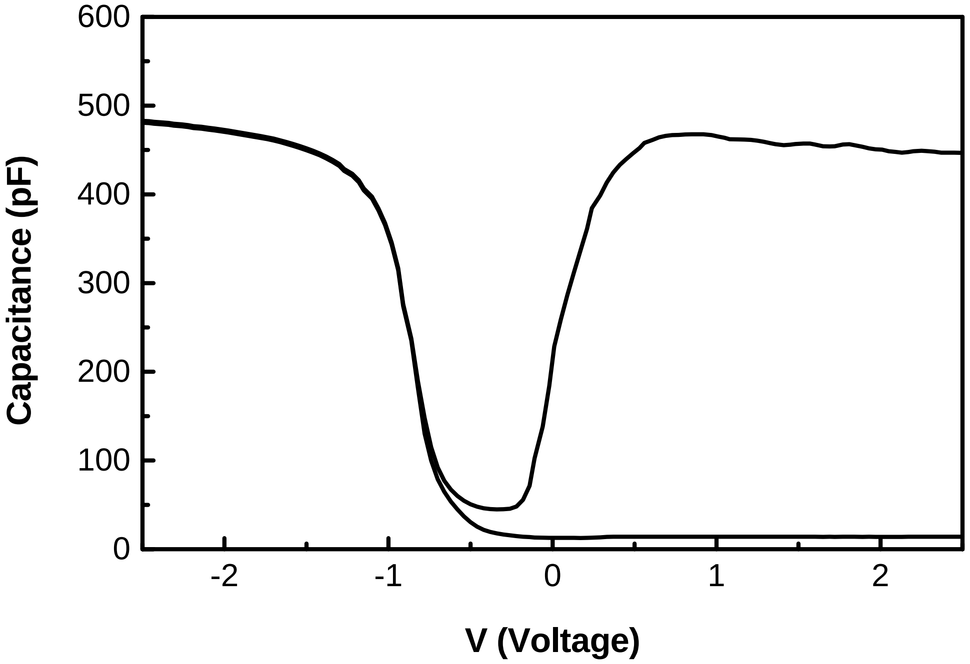


Fig. 3-4 C-V characteristics of 110 Å Al_2O_3 MOS capacitor.

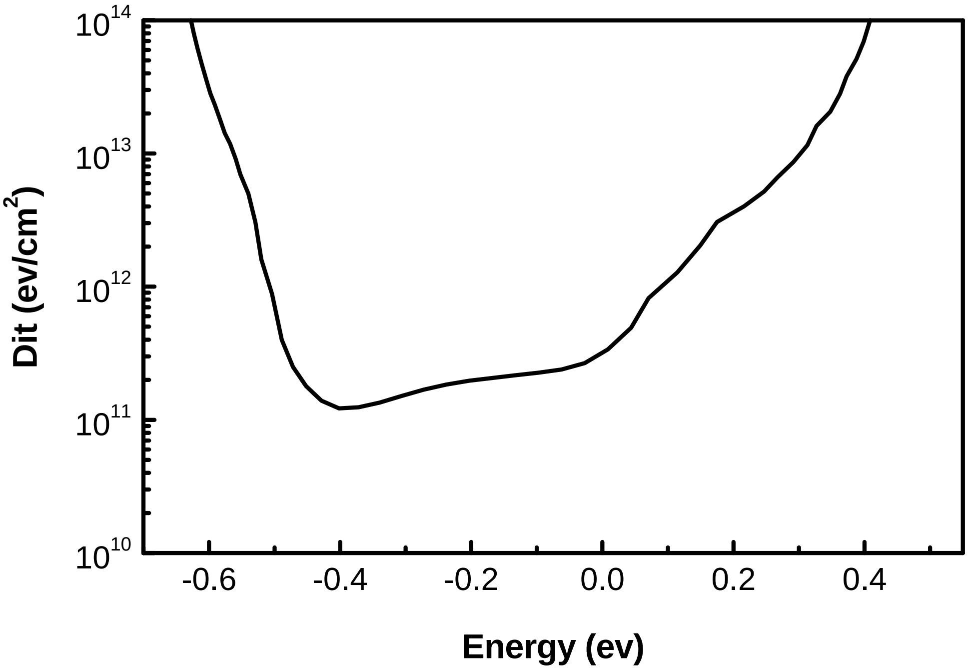


Fig. 3-5 Interface trap density of the Al_2O_3/Si interface.

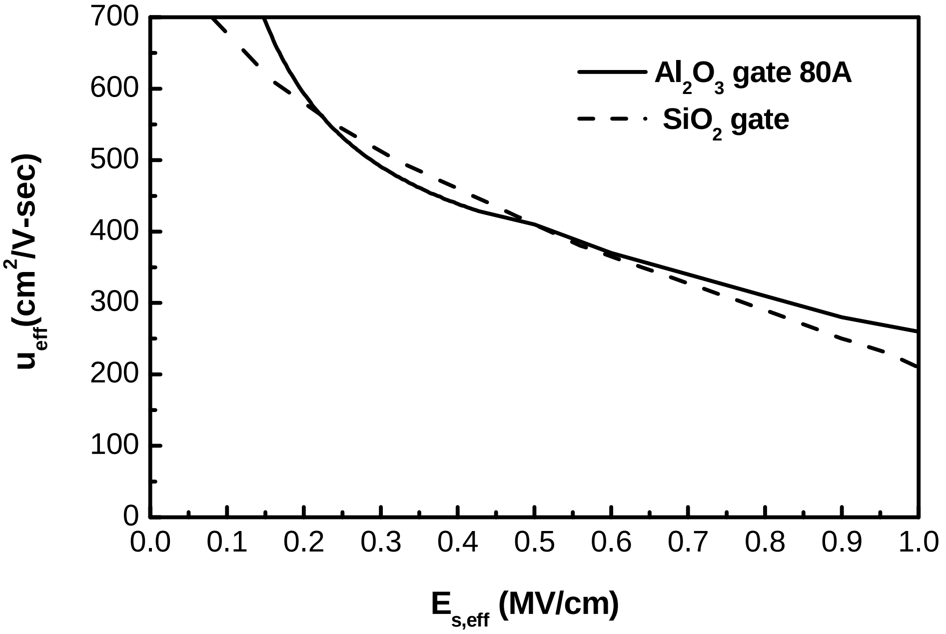


Fig. 3-6 Electron mobilities of MOSFET's with 80 Å Al_2O_3 and conventional SiO_2. (M. S. Liang, J. Y. Choi, P. K. Ko, C. Hu, IEEE TED-33, no. 3, pp. 409-413, 1986.).

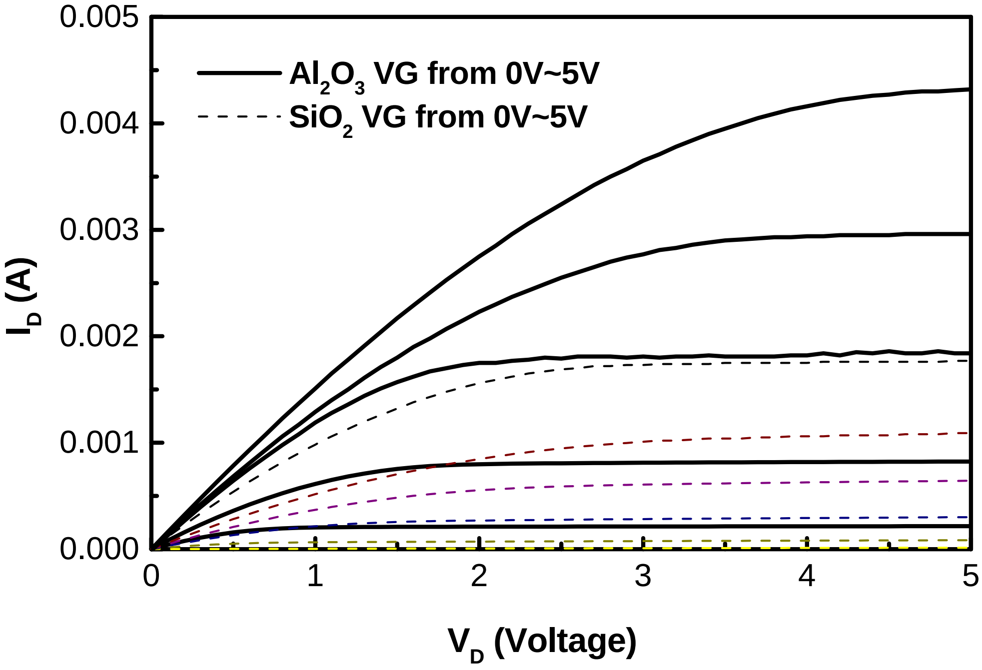


Fig. 3-7 Id-Vd characteristics of an 80 Å Al_2O_3 MOSFET. The high current drive in Al_2O_3 gives a k value of 9.8.

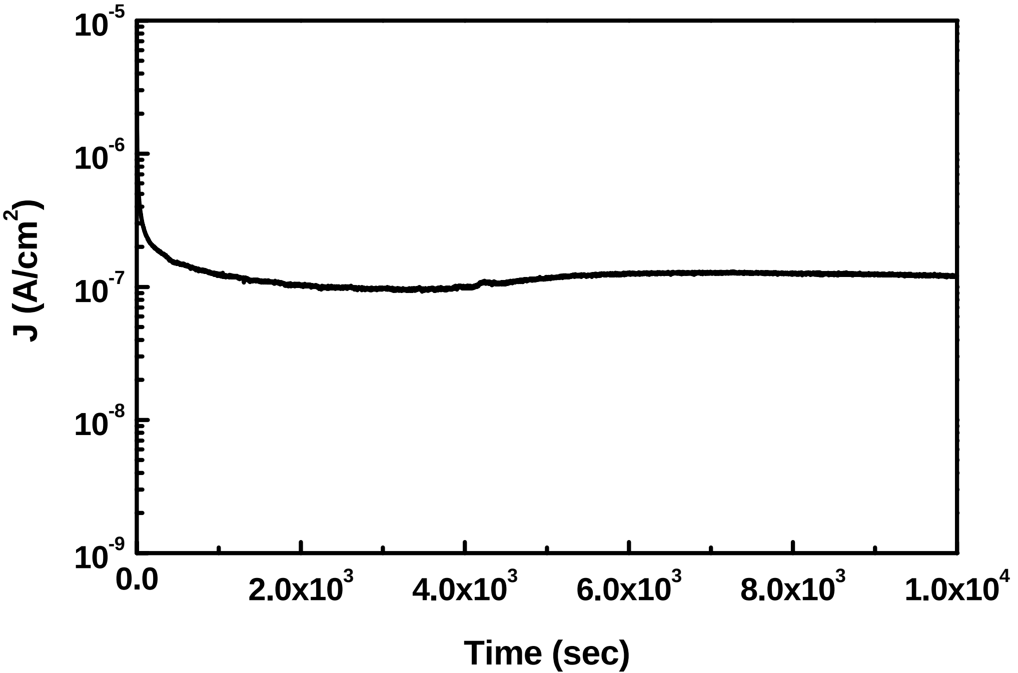


Fig. 3-8 Current density changes of the 48 Å Al_2O_3 MOS capacitor under a constant voltage stress at 2.5 V for 10,000 sec.

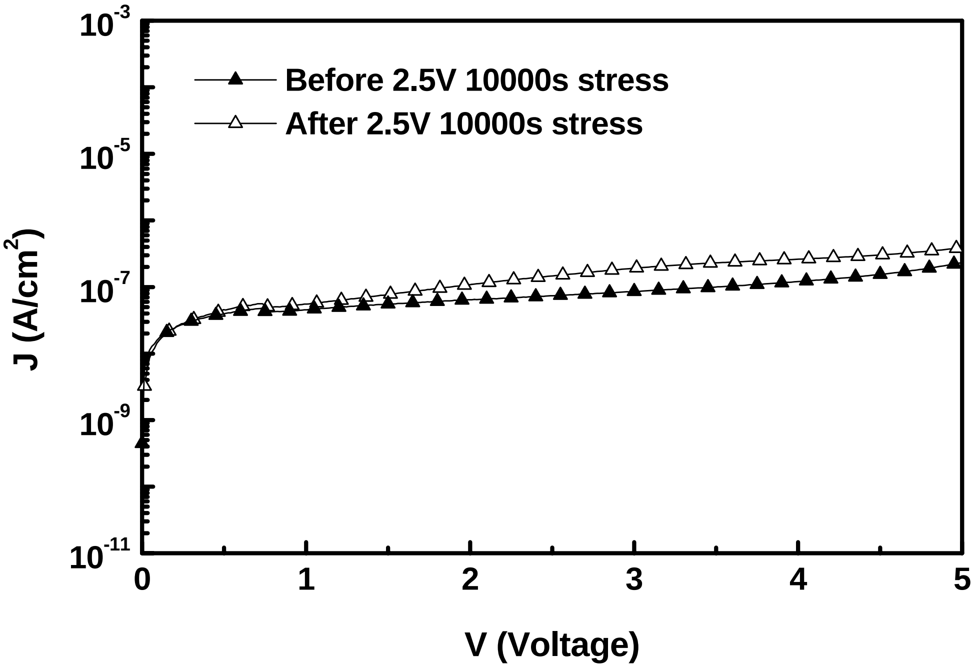


Fig. 3-9 SILC effect of the 48 Å Al_2O_3 MOS capacitor under a constant voltage stress at 2.5 V for 10,000 sec.

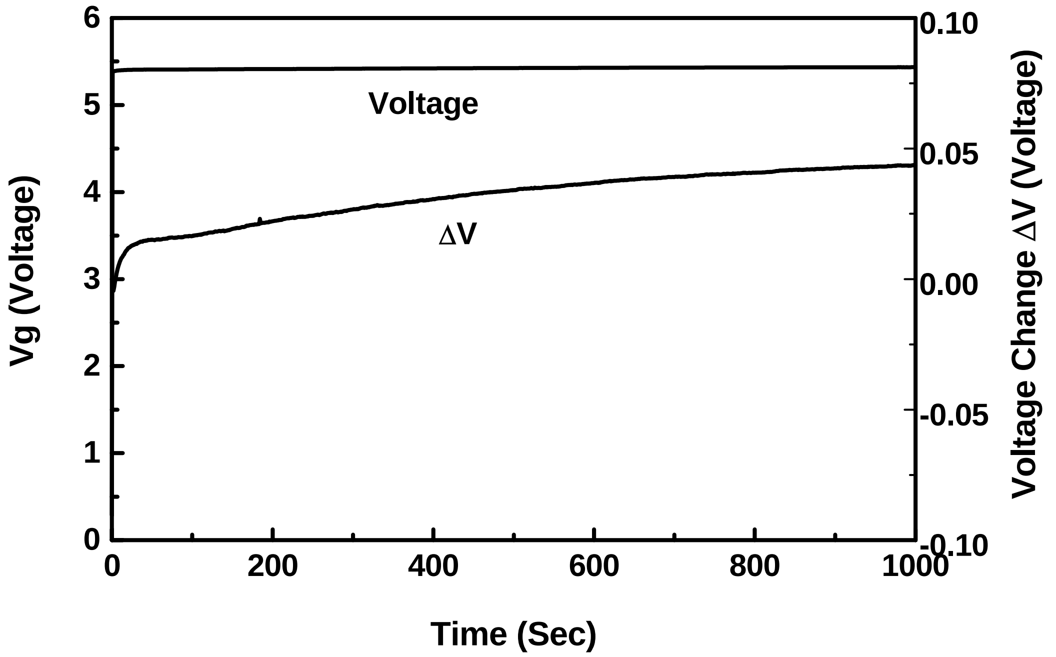


Fig. 3-10 Voltage changes of 48 Å Al_2O_3 MOS capacitor under a 0.1 mA/cm^2 current density stress for 1000 sec.

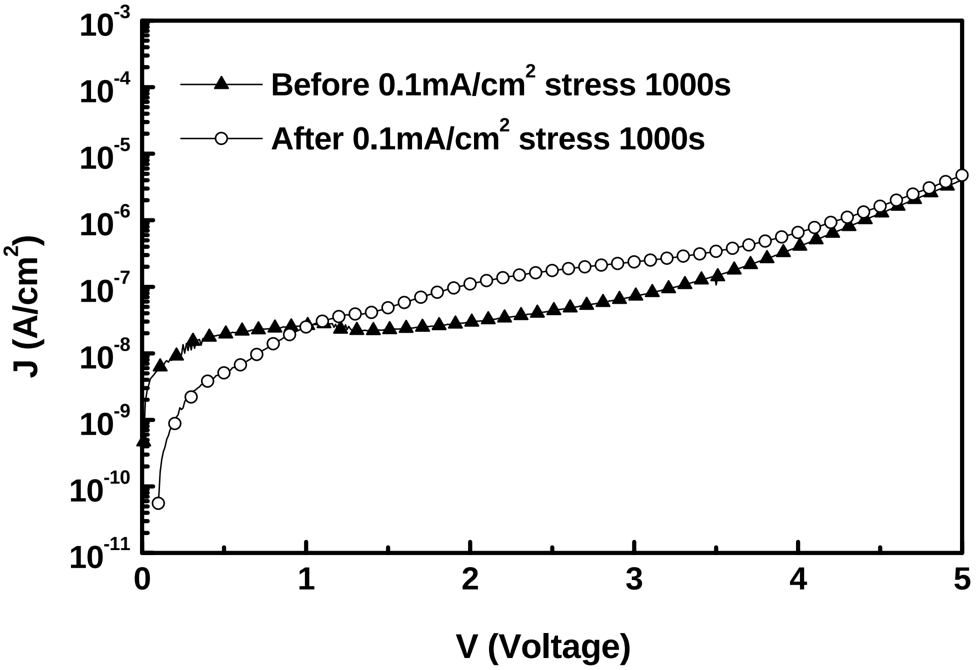


Fig. 3-11 SILC effect of 48 Å Al_2O_3 MOS capacitor under a 0.1 mA/cm^2 current density stress for 1000 sec.

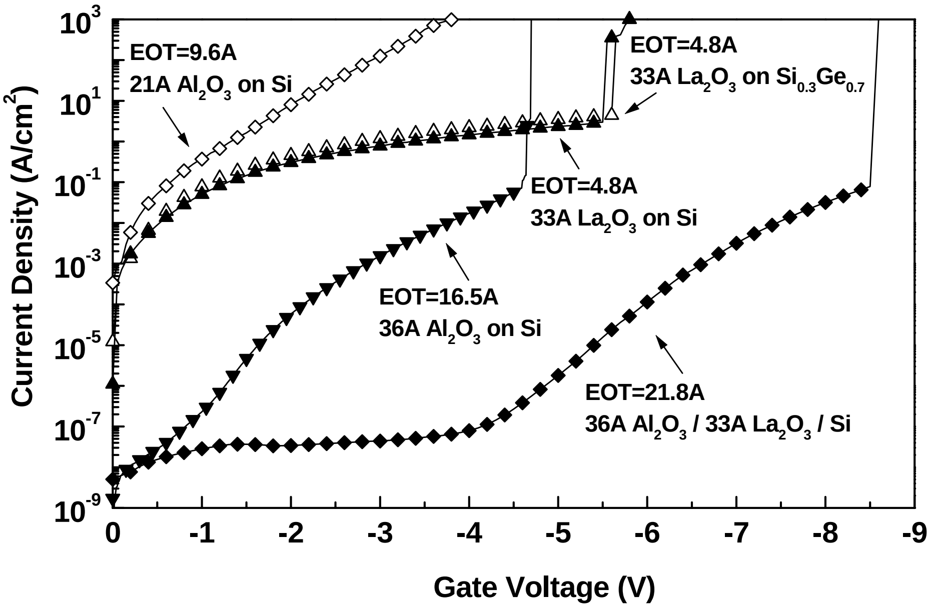


Fig. 3-12 J-V characteristics for Al_2O_3 (9.6 & 16.5 Å EOT) and La_2O_3 (4.8 Å EOT) capacitors. Stacked structure is adopted to reduce leakage current for D_{it} measurement.

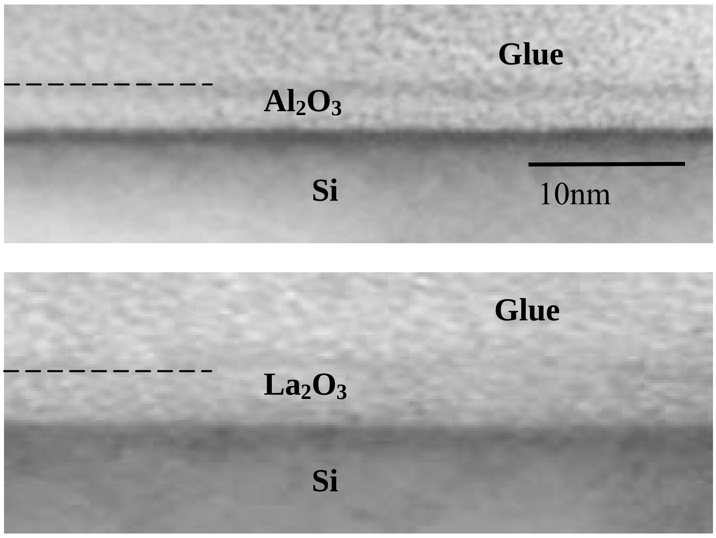


Fig. 3-13 Cross-section TEM of Al_2O_3 and La_2O_3. Very smooth interface is due to the high thermal stability and native oxide free surface. Both dielectrics are amorphous.

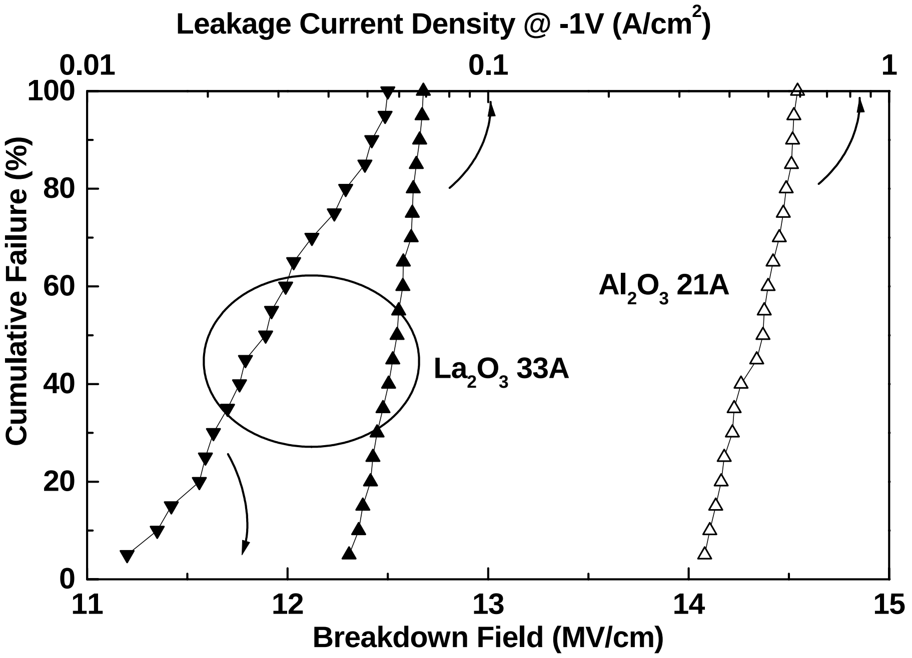


Fig. 3-14 Cumulative distribution of leakage current and breakdown field for Al_2O_3 and La_2O_3 gate dielectrics.

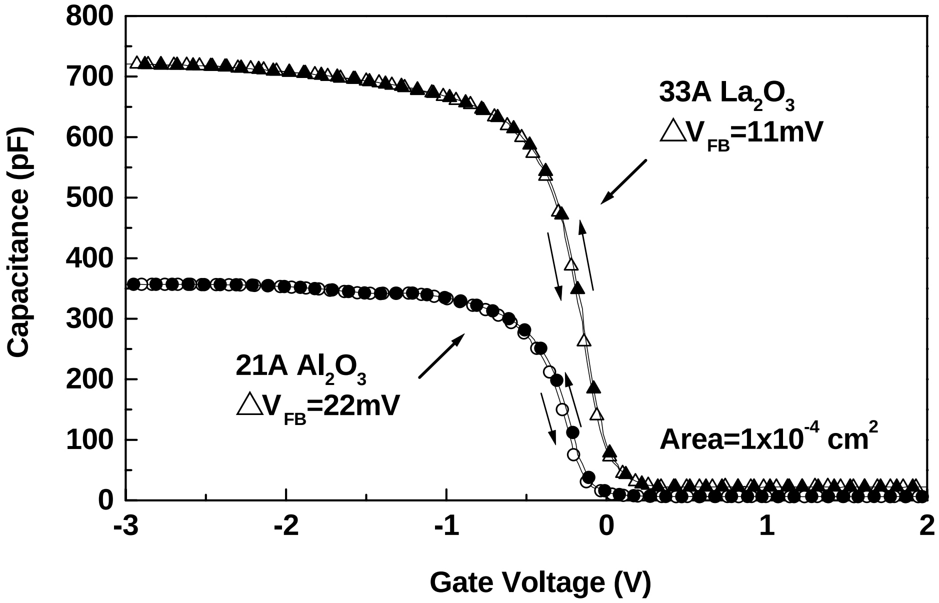


Fig. 3-15 Hysteresis curves for Al_2O_3 and La_2O_3 gate dielectrics.

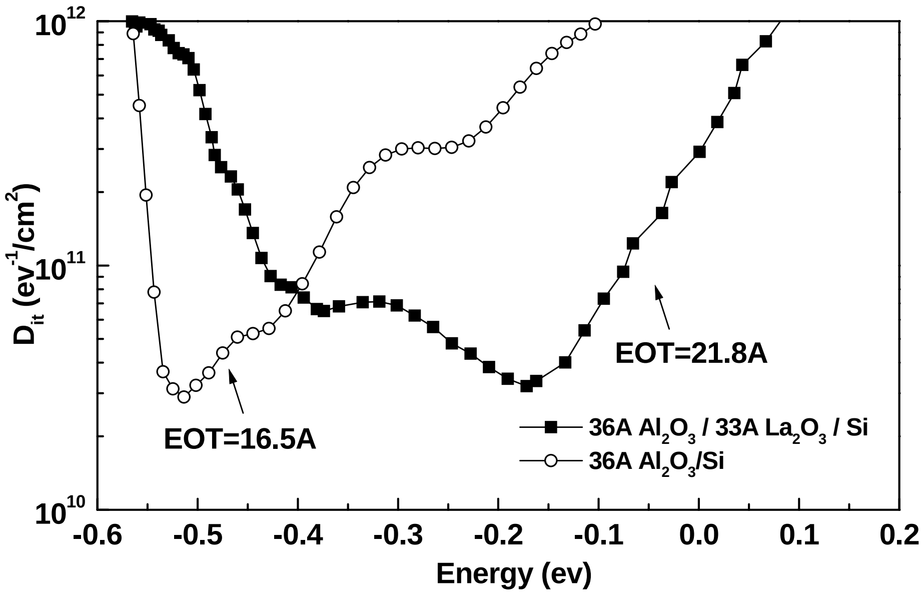


Fig. 3-16 Interface state density of Al_2O_3 and La_2O_3 on Si. Min D_{it} of $3x10^{10}$ eV^{-1}/cm^2 is obtained for both dielectrics and close to SiO_2/Si.

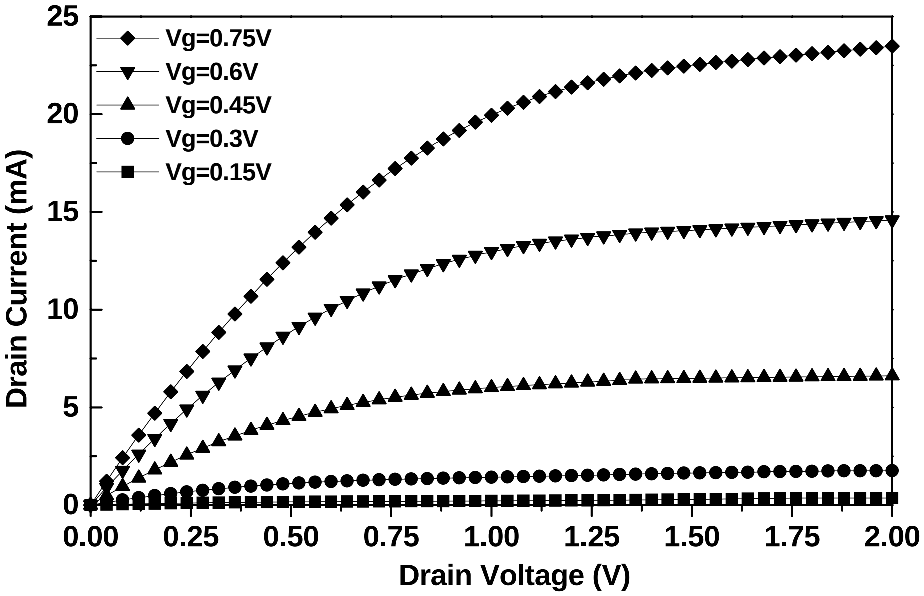


Fig. 3-17 I_d-V_d characteristics of 30 mm x 1200 mm nMOSFETs with 33 Å La_2O_3 gate dielectric.

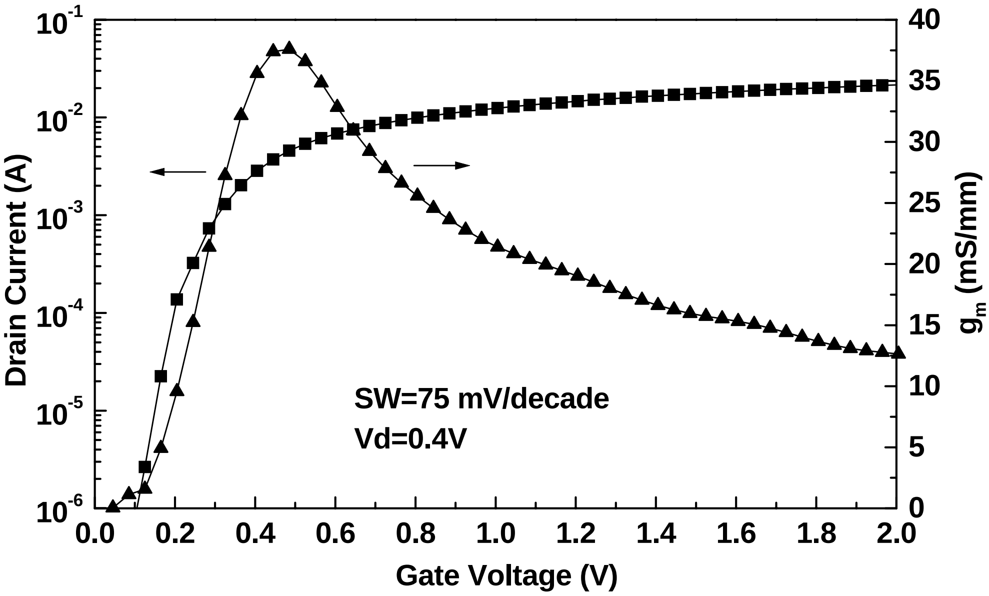


Fig. 3-18 Subthreshold characteristic and transconductance for 33 Å La_2O_3 nMOSFETs as a function of gate bias.

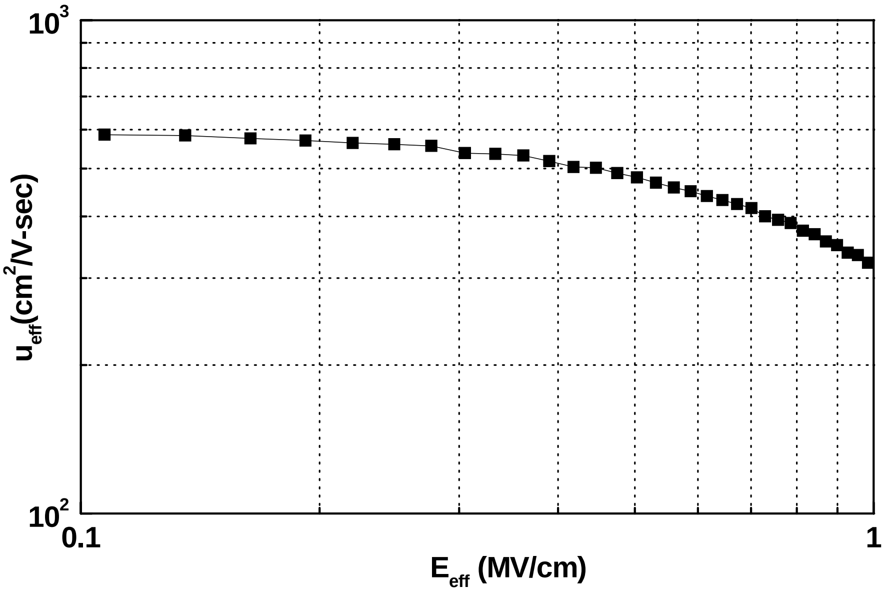


Fig. 3-19 Effective electron mobility versus electrical field for 33 Å La_2O_3 nMOSFET.

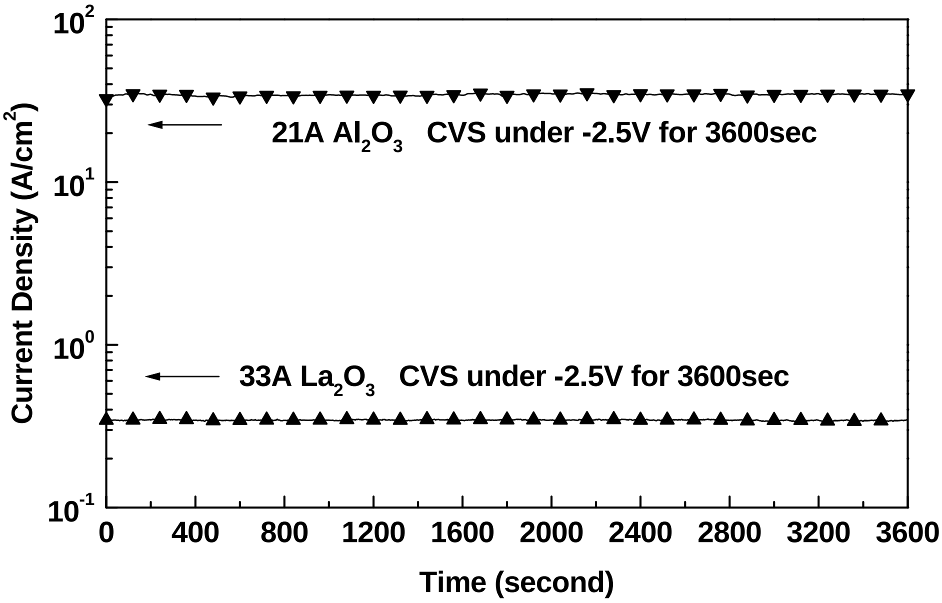


Fig. 3-20 Time evolution of I_g under -2.5 V for 1 hr with Q_{inj} of $1.3x10^3$ and $1.5x10^5$ C/cm^2 for respective La_2O_3 and Al_2O_3.

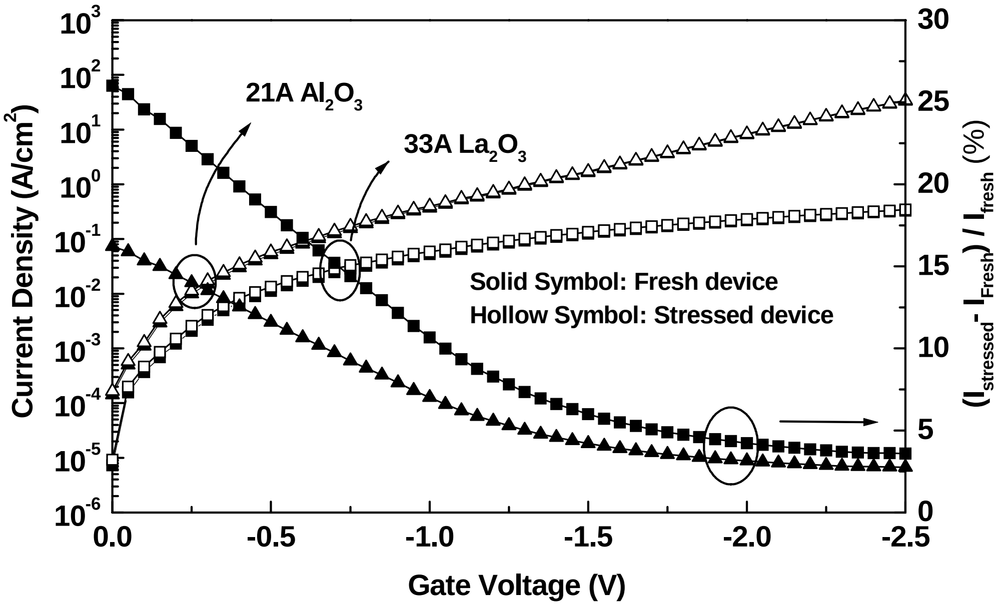


Fig. 3-21 Stress induced leakage current and current variation for Al_2O_3 and La_2O_3 under -2.5 V for 1hr.

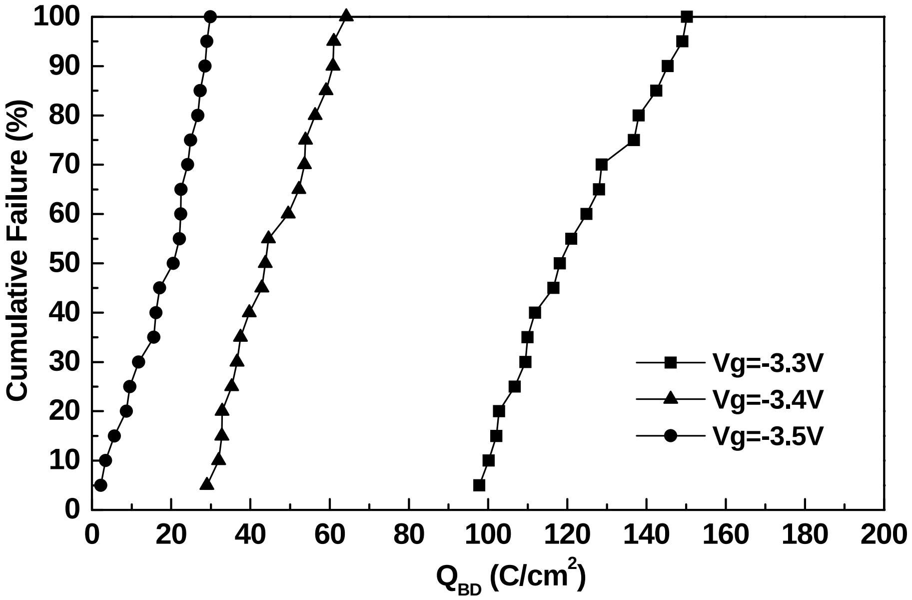


Fig. 3-22 Q_{BD} distribution of La_2O_3 dielectric with different V_g. For 50% MTTF and 10 years lifetime, a max operation voltage of 2.3 V is obtained.

Chapter 4

Bias-Temperature Instability and Charge Trapping on Fully-Silicided-Germanided Gates/High-k Al_2O_3 CMOSFETs

4.1 Introduction

As continuous scaling down the MOSFET devices into sub-100 nm scale, oxynitride or metal-oxide high-k gate dielectric, with ultra-thin equivalent oxide thickness (EOT), is required to replace the conventional SiO_2 to reduce gate dielectric leakage current. To further increase the drive current in MOSFET, metal gate will be integrated with these high-k gate dielectrics [4.1]-[4.5]. However, one of the main concerns of such metal-gate/high-k MOSFETs is the poor Bias-Temperature Instability (BTI) [4.1], [4.6]-[4.8]. In particular, the negative BTI (NBTI) of pMOSFETs is becoming an increasingly serious problem of the CMOS reliability. It is known that the NBTI of oxynitride gate dielectric pMOSFETs is mainly related to nitrogen traps [4.9]-[4.12], hydrogen [4.13]-[4.14], moisture (H_2O) [4.14], and impurity diffusion [4.6] etc. Both the NBTI and positive BTI (PBTI) are even worse in metal-oxide high-k CMOSFETs than oxynitride devices [4.1], [4.6]-[4.8]. In this work, we have studied the BTI effect on fully silicided-germanided (NiSi-NiGe) dual gates on high-k Al_2O_3 CMOSFETs [4.5], [4.15]-[4.19] and compared with a benchmark oxynitride devices. The fully silicided gate has advantage of fully process compatible to current VLSI fabrication technology. The Al_2O_3 gate dielectric has reasonable high-k and good thermal stability with amorphous type up to $1000^{o}C$ [4.5], [4.12], [4.15]-[4.21]. In contrast to the worse NBTI than PBTI in oxynitride devices, close NBTI and PBTI is found in fully NiSi-NiGe gates/Al_2O_3 CMOSFETs. At 17 Å EOT, the extrapolated maximum operation voltage ($V_{max-10years}$) for 10 years lifetime, with 50 mV threshold voltage (V_t) change at $85^{o}C$, is 1.16 V and -1.12 V from PBTI and NBTI, respectively. These results are comparable or better than the reported HfAlON [4.6] and HfSiON data [4.7]. The high $V_{max-10years}$ and close value for both NBTI and PBTI may be due to the process without hydrogen and H_2O that were used during high-k HfAlON and HfSiON deposition by Atomic-Layer Deposition (ALD) using NH_3 and H_2O sources [4.6]. However, the inferior PBTI of NiSi-NiGe/Al_2O_3 CMOSFETs to oxynitride devices suggests that further improving the high-k dielectric quality is required.

4.2 Experimental

Standard n- and p-type (100) Si wafers with a typical resistivity of ~10 Ω-cm were used in this study. After standard cleaning, the device active region was formed by thick field oxide and patterning. The source and drain region were implanted by 35 KeV Phosphorus or 25 KeV Boron for nMOSFETs or pMOSFETs respectively, followed by RTA activation. Then the ~39 Å Al_2O_3 was formed by physical-vapor deposition, 400°C oxidation for 20 min. and 400°C annealing for 20 min. From the C-V measurement, a k value of 8.9 and EOT of 17 Å were obtained. The slightly low-k value than bulk Al_2O_3 (k=10) is due to the oxidation of Si during post deposition annealing. The fully NiSi and NiGe gates were formed by depositing 150 Å amorphous Si or Ge on Al_2O_3, 150 Å Ni for both n- and p-devices, and followed by silicidation and germanidation at 400°C RTA for 30 sec [4.5], [4.15]-[4-19]. For comparison, control oxynitride was formed by decoupled plasma nitridation [4.22] on a 18 Å SiO_2 that was grown by oxygen at 700°C for 12 min. The formed oxynitride has peak N concentration of 9% near poly gate interface, followed by post deposition annealing at 1000°C RTA. The fabricated CMOSFETs were further characterized by C-V I-V, and Bias-Temperature (BT) measurements.

4.3 Results and Discussion

We have first measured the I_{ds}-V_{gs} characteristics to examine the hysteresis effects in Al_2O_3. Fig. 4-1 and Fig. 4-2 show the measured hysteresis on NiSi/Al_2O_3 nMOSFETs and NiGe/Al_2O_3 pMOSFETs, respectively. For fully silicide/high-k nMOSFET, the double sweep of gate voltage from 0 to 1.5 V results in V_t shifted to positive by +10 mV. This result suggests generating negative charge traps in nMOSFET. For pMOSFET, the double sweep of gate voltage from 0.5 to -1.5 V results in V_T shifted to negative by -10 mV, which also indicates the generating positive charge traps in bulk Al_2O_3 and Al_2O_3/Si interface. These amounts of charge trappings may cause NBTI in pMOSFETs and PBTI in nMOSFETs. The poor I_{off} in nMOSFETs is due to the insufficient high temperature annealing (only 950°C RTA) for ion-implanted damage. The limited RTA temperature also gives a relative poor sub-threshold swing because of the insufficient annealing of high-k dielectric defects. Further improving the leakage current and sub-threshold swing can be done by increasing RTA temperature to typical 1000-1050°C or using $LaAlO_3$ high-k dielectric [4.24], [4.25].

We have also used the C-V to measure the hysteresis effects. Fig. 4-3 and Fig. 4-4 show the CV hysteresis characteristics, measured at 500 KHz, on NiSi/Al_2O_3 nMOSFETs and NiGe/Al_2O_3 pMOSFETs respectively, where conventional bi-directional sweeps from inversion to accumulation were applied to these transistors. The double sweeping hysteresis of +10 mV and ~0 mV are measured for nMOS and pMOS capacitors, respectively. The smaller flat band voltage shift of pMOS capacitor than the V_t shifts of I_{ds}-V_{gs} curves in NiGe/Al_2O_3 pMOSFETs may be due to the relative slower and deeper traps that were unable to follow the AC signal [4.23]. Similar effect is also observed in other high-k dielectrics from quasi-static to RF frequency range [4.24]-[4.27].

Figs. 4-5 and Fig. 4-6 shows the NBTI characteristics of I_{ds}-V_{gs} and V_t change (ΔV_t) for NiSi/Al_2O_3 pMOSFETs stressed at 10 MV/cm electric field and 85°C ambient to 1 hour, respectively. This stress condition was chosen to compare with published data in the literature [4.6], [4.7]. For reference and comparison, the ΔV_t of SiON pMOSFETs and the data of TaN/HfAlO [4.6] are also plotted in Fig. 4-6. After the 1 hour stress at 10 MV/cm and 85°C, a ΔV_t of -33 mV is measured suggesting that the NBTI is one of the most serious reliability issues for fully NiSi gate/high-k Al_2O_3 pMOSFETs. The measured ΔV_t changes are comparable or better than the published HfAlON [4.6], HfSiON [4.7] and HfTaO [4.1] where additional Al, N, Si or Ta must be added to HfO_2 for BTI reliability improvement. However, the measured ΔV_t is still larger than that of oxynitride devices with plasma generated N at top poly-Si/oxynitride interface. The possible reason of the inferior NBTI is due to the degraded interface of Al_2O_3/Si and bulk oxide change in Al_2O_3, where oxygen-riched SiN interface on Al_2O_3 will be the possible solution for this important reliability issue [4.10]-[4.12].

Fig. 4-7 and Fig. 4-8 show the PBTI characteristics of I_{ds}-V_{gs} and V_t for

NiGe/Al_2O_3 nMOSFETs stressed at 10 MV/cm electric field and 85°C to 1 hour, respectively. The ΔV_t of SiON nMOSFETs are also added in Fig. 4-8 for comparison. After the 1 hour BT stress, a ΔV_t of 34 mV is measured for PBTI that is close to the $|-33\ \mathrm{mV}|$ value in NBTI. In sharp contrast, the NBTI of only 0.76 mV is measured in poly-Si/oxynitride (9% peak at poly-Si interface) nMOSFETs after the same BT stress that is lower than the 6.6 mV change in oxynitride pMOSFETs. The better PBTI than NBTI is normal for oxynitride MOSFETs where the mechanism is attributed to hole injection to break the H-Si bonds and created interface traps [4.9]-[4.14]. However, the measured NBTI and PBTI value are less than that of HfO_2 [4.7], [4.8], which may be due the strong A-O bond and consistent with the results in HfAlO [4.6]. The close PBTI and NBTI absolute value after BT stress in Al_2O_3 MOSFETs suggesting the higher number of interface and bulk traps, which are normal for high-k gate dielectric, are the main causes and for larger $|\Delta V_t|$ change than oxynitride devices.

We have also measured BTI at other gate electric field for 10 years lifetime projection, where the lifetime at each gate voltage was defined by a $|\Delta V_t|$=50 mV change during stress. Such high gate voltage or electric field is especially required for poly-Si/SiON CMOS due to the excellent reliability. Figs. 4-9 show the time as a function of V_{gs} of nMOSFETs and pMOSFETs, respectively. The 10 years lifetime

$V_{max\text{-}10years}$ is from the extrapolation of measured data at high gate voltage. The extrapolated $V_{max\text{-}10years}$ are 1.16 and -1.12 V for Al_2O_3 nMOSFETs and pMOSFETs, respectively. Theses values can barely meet the BTI requirement at 1 V operation with additional 10% safety margin to 1.1 V. It is important to notice that the degraded PBTI is also reported in HfAlON gate dielectric MOSFETs [4.6] that is even worse than NBTI and attributed to gate impurity diffusion. The close $V_{max\text{-}10years}$ for PBTI and NBTI in Al_2O_3 MOSFETs is simply because no impurity [4.6], nor hydrogen annealing [4.13]-[4.14] or processing water [4.6], [4.14] were added to the fully NiSi-NiGe/Al_2O_3 CMOSFETs. Unfortunately, these values are lower than the 2.48 and -1.52 V of respective PBTI and NBTI extrapolation for oxynitride MOSFETs at close EOT. The main mechanism for NBTI degradation in poly-Si/SiON pMOS is due to the trap generation by energetic holes in bulk oxide and interface. In contrast, the poorer BTI in high-k MOSFETs may be directly related to the existing high bulk and interface traps. Therefore, further technology development to reduce these traps or using an oxygen-riched SiN interface beneath the high-k [4.10]-[4.12] is the key factor for metal-gate/high-k CMOS BTI reliability.

4.4 Conclusion

We have studied the NBTI and PBTI of 17 Å EOT NiSi-NiGe/Al_2O_3

CMOSFETs, with baseline characteristics of 10 mV hysteresis. The comparable V_t change of -34 and 33 mV for respective NBTI and PBTI, after 10 MV/cm and 85°C stress for 1 hour, is probably due to impurity free in NiSi or NiGe gate and no hydrogen or water used in device process. The amount of V_t change and extrapolated $V_{max\text{-}10years}$ of 1.16 and -1.12 V in NiSi-NiGe/Al_2O_3 CMOSFETs are comparable with or better than the reported BTI data of HfSiON and HfAlON that suggesting the good high-k device integrity. Although the $V_{max\text{-}10years}$ of NiSi-NiGe/Al_2O_3 CMOSFETs can barely meet the 1 V operation requirement, better performance is found in oxynitride CMOSFETs with higher $V_{max\text{-}10years}$ of 2.48 and -1.52 V of PBTI and NBTI, respectively. In addition to almost the same NBTI and PBTI values in NiSi-NiGe/Al_2O_3 CMOSFETs, the comparison with oxynitride CMOSFETs suggests the bulk and interface oxide traps in high-k Al_2O_3 dielectric plays the dominant role for BTI. Therefore, further improving the device performance is required for metal-gate/high-k CMOSFETs including BTI and mobility degradation effects.

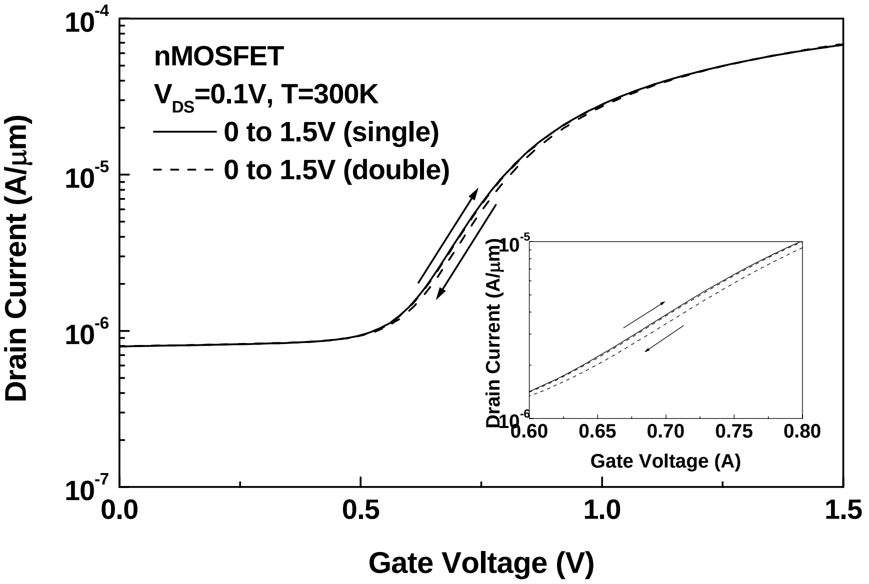


Fig. 4-1 The room temperature I_{ds}-V_{gs} characteristics of NiSi/Al_2O_3 nMOSFETs under double sweep measurements. The inserted figures are the enlarged view to show the hysteresis.

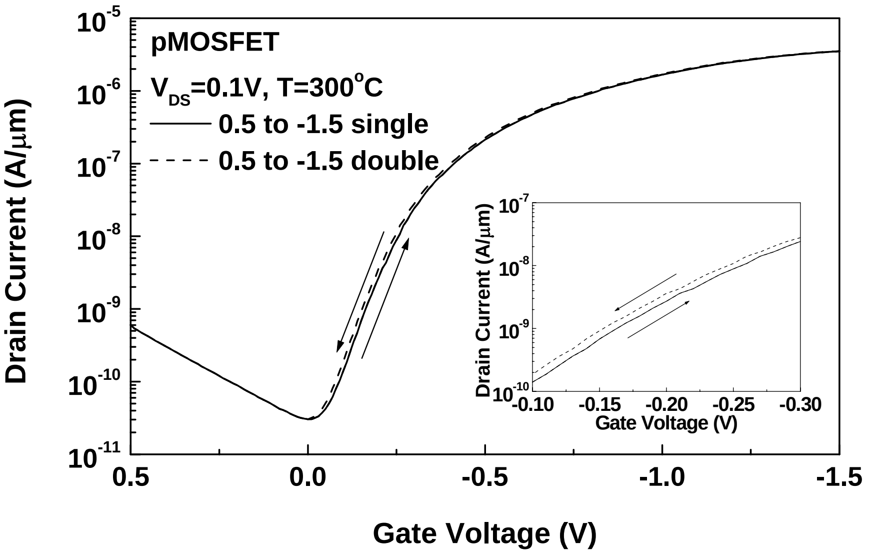


Fig. 4-2 The room temperature I_{ds}-V_{gs} characteristics of NiGe/Al_2O_3 pMOSFETs under double sweep measurements. The inserted figures are the enlarged view to show the hysteresis.

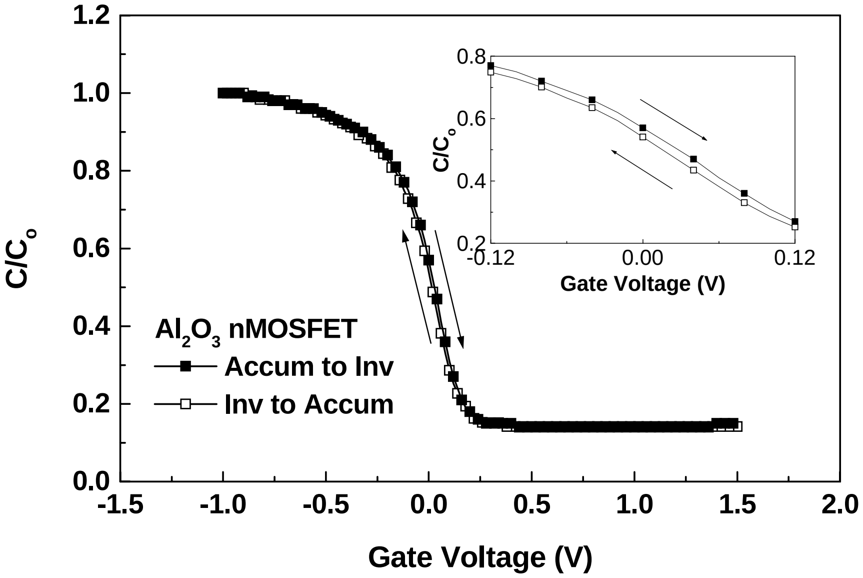


Fig. 4-3 The room temperature C-V characteristics of NiSi/Al_2O_3 nMOS capacitors under double sweep measurements. The inserted figures are the enlarged view to show the hysteresis.

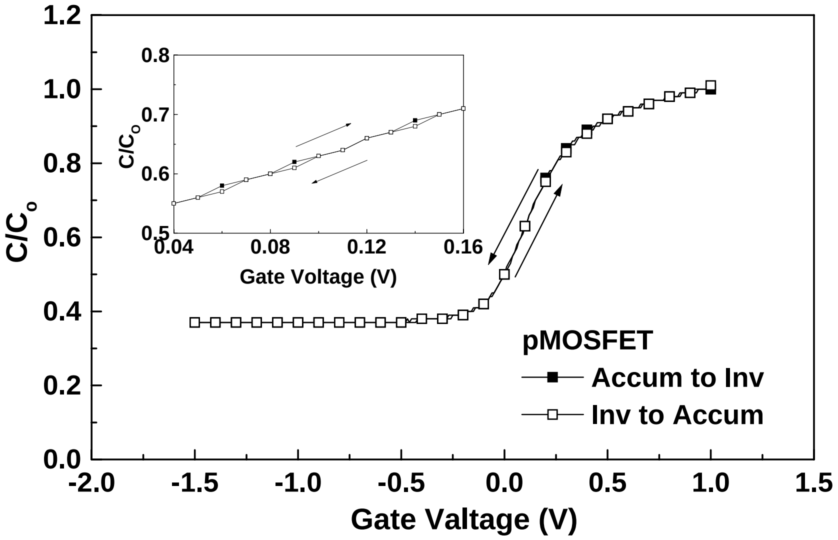


Fig. 4-4 The room temperature C-V characteristics of NiGe/Al_2O_3 pMOS capacitors under double sweep measurements. The inserted figures are the enlarged view to show the hysteresis.

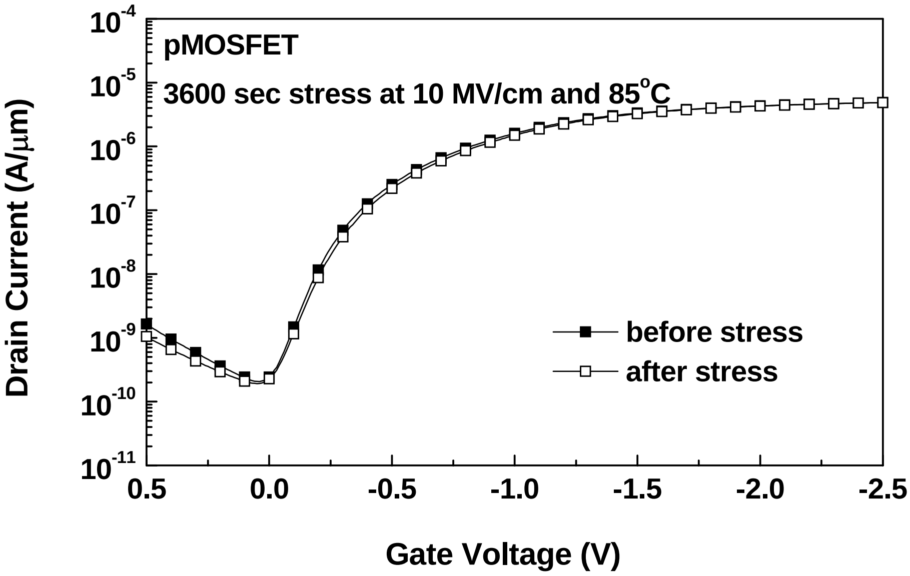


Fig. 4-5 The I_{ds}-V_{gs} changes of NiGe/Al_2O_3 pMOSFETs stressed at 85°C and 10 MV/cm for 1 hour.

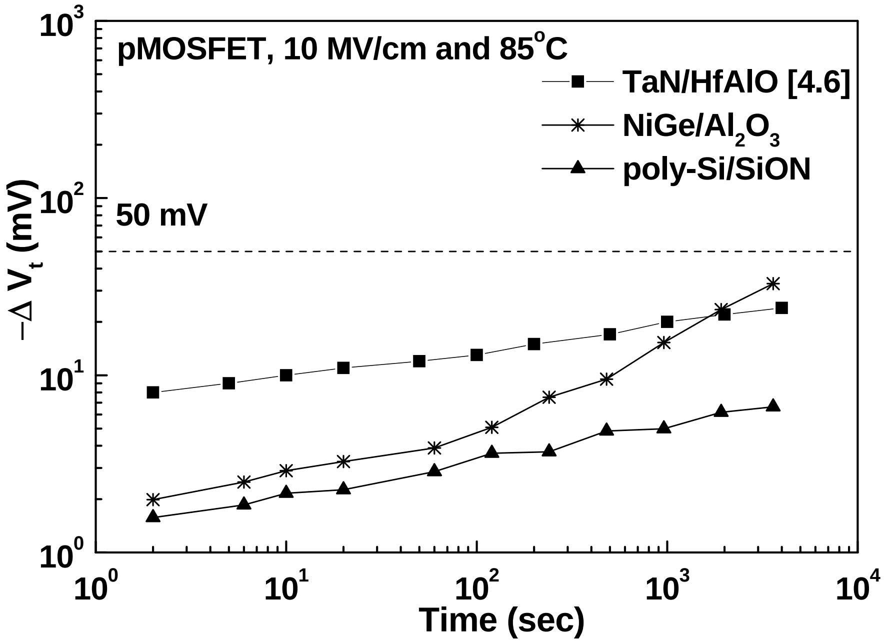


Fig. 4-6 The ΔV_t changes of NiGe/Al_2O_3 pMOSFETs stressed at 85°C and 10 MV/cm for 1 hour. For comparison, the data from poly-Si/SiON and TaN/HfAlO (from reference 6) are also added under the same stress condition.

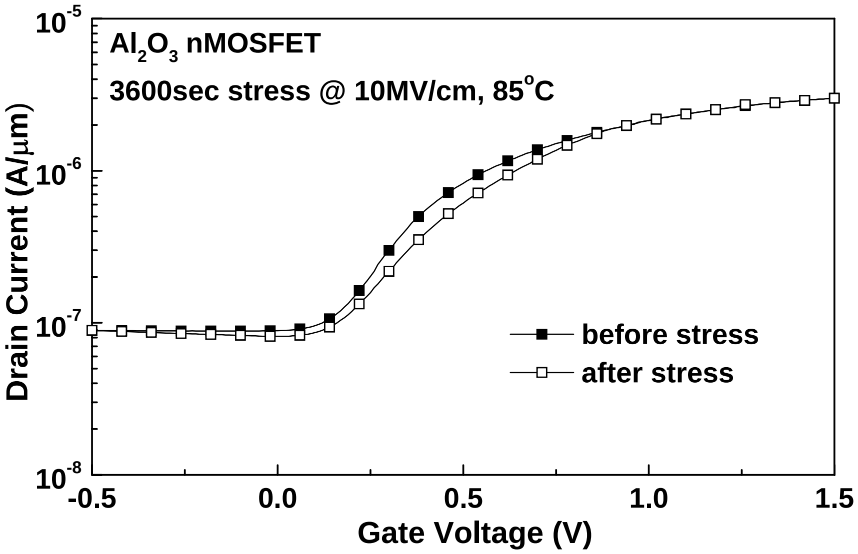


Fig. 4-7 The I_{ds}-V_{gs} change of NiSi/Al_2O_3 nMOSFETs stressed at 85°C and 10 MV/cm for 1 hour.

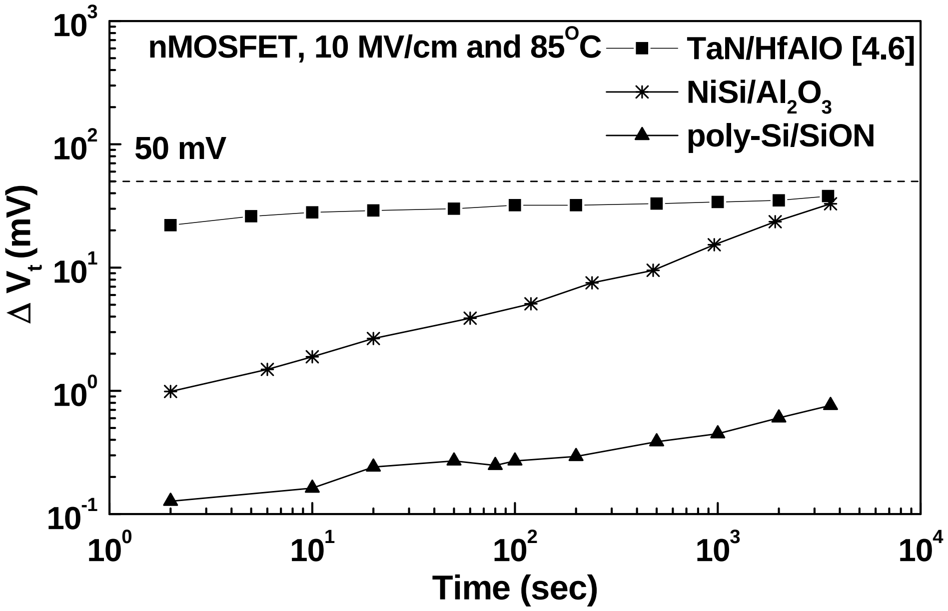


Fig. 4-8 The ΔV_t changes of NiSi/Al$_2$O$_3$ nMOSFETs stressed at 85°C and 10 MV/cm for 1 hour. For comparison, the data from poly-Si/SiON and TaN/HfAlO (from reference 6) are also added under the same stress condition.

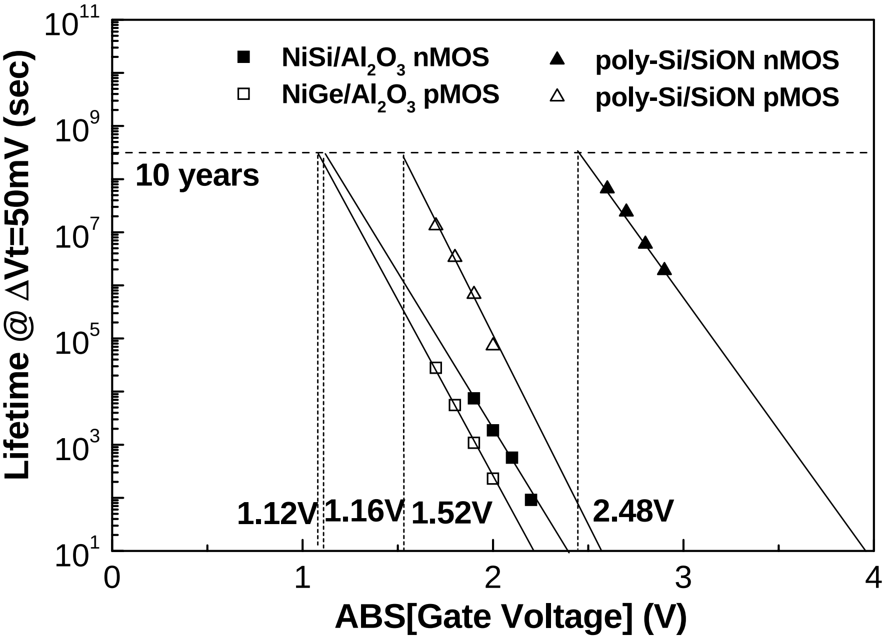


Fig. 4-9 The extrapolated maximum operation voltage for 10 years lifetime of NiSi/Al$_2$O$_3$ nMOSFETs and NiGe/Al$_2$O$_3$ pMOSFETs under failure condition of 50 mV change in V_t at 85°C. The data from oxynitride is also added for comparison.

Chapter 5

The Copper Contamination Effect on Al_2O_3 Gate Dielectric on Si

5.1 Introduction

To reduce the circuit’s RC delay from backend metal lines and parasitic capacitors, Cu and low-k dielectric are required. However, Cu diffusion into low-k and front-end MOSFETs is an important issue [5.1]-[5.12]. The Cu contamination from backend Cu interconnects or the backside wafer surface contaminated by Cu will accumulate at the Si/SiO_2 interface [5.6]-[5.8] or reacts with Si to form silicide. The precipitate Cu at oxide interface will increase the sub-threshold swing of MOSFETs [5.7], [5.9], shift the threshold voltage, and degrade the gate leakage current [5.10]-[5.12]. The Cu silicide will also increase the unwanted leakage current in source-drain junction. To reduce Cu diffusion during backend thermal cycle, barrier metal under Cu and thick SiN between each inter-metal layer (IML) dielectric are usually added. However, the added SiN of typical 500 Å has large k value of 7.5 and will degrade the total k of combined IML dielectric and SiN. The increasing effective k is unfavorable since it will increase the circuit’s backend RC delay. In this paper, we have studied the Cu contamination effect in high-k Al_2O_3 gate dielectric [5.13]-[5.16] with small equivalent-oxide thickness (EOT) of 19 Å, where the high-k gate dielectric is important for continuously scaling down the nm-scale MOSFET. In contrast to the large degradation of gate oxide integrity in 30 Å thermal SiO_2, the smaller 19 Å EOT Al_2O_3 gate dielectric shows much better resistance to Cu contamination related degradation on gate dielectric leakage current, charge-to-breakdown (Q_{BD}) and stress-induced leakage current (SILC). Therefore, the high-k gate dielectric with Al_2O_3 ternary compound such as HfAlO or $LaAlO_3$ should have this additional advantage besides the high-k value. This is the first study of Cu diffusion in high-k Al_2O_3.

5.2 Experimental

Standard four-inch, p-type (100) Si wafers with a typical resistivity of ~10 Ω-cm were used in this study. After standard cleaning, the device active region was formed by thick field oxide and patterning. Then the ~42 Å Al_2O_3 was formed by physical-vapor deposition from an Al_2O_3 sputter source, oxidation at $400^{o}C$ under O_2 ambient for 5 min and annealed at N_2 ambient for 25 min. From the C-V measurement, a k value of 8.5 and EOT of 19 Å were obtained. Then the gate electrode was formed by depositing a 3000 Å thick aluminum by thermal evaporation and patterning, where the fabricated area of MOS capacitors is 100 μm × 100 μm. The Cu contamination to the Al_2O_3 MOS devices was introduced by contacting the front side of devices into a $Cu(NO_3)_2$ solution with 10 ppb or 10 ppm concentration for 1 minute then followed by driving-in at 400°C N_2 annealing. The existence of Cu within gate SiO_2 by this contamination process was confirmed by SIMS measurements reported previously [5.11], where strong Cu accumulation is observed in both poly-Si and SiO_2. More detailed Cu contamination process and the degradation on gate dielectric integrity of SiO_2 and SiON can be found in our previous publications [5.10]-[5.12]. The Cu contamination effect was studied by current-density and voltage (J-V) measurements in high-k Al_2O_3 gate dielectric MOS capacitors.

5.3 Results and Discussion

Fig. 5-1 shows the J-(V_G-V_{FB}) characteristics of Al_2O_3 gate capacitors with ~42 Å physical thickness (19 Å EOT), where the V_{FB} is the flatband voltage obtained from the C-V measurement and quantum mechanical calculation. The V_{FB} of -0.7 V and -0.85 V are obtained for Al_2O_3 and SiO_2 gate dielectric capacitors, respectively. It is important to notice that there is no significant V_{FB} change after Cu contamination. This suggests that the Cu may behave as neutral trap in gate dielectric and consistent with our previous report [5.12]. For comparison, the J-(V_G-V_{FB}) characteristics of 30 Å thick SiO_2 MOS device were also plotted. For samples without Cu contamination, the 19 Å EOT Al_2O_3 gate capacitor has ~one order of magnitude lower leakage current than 30 Å SiO_2, which is the fundamental advantage of high-k gate dielectric. The Cu contamination in 30 Å SiO_2 control devices have significant effect on gate dielectric leakage current that was increased by ~2 orders of magnitude. The 10 ppb and 10 ppm Cu contaminated SiO_2 control devices show almost identical leakage current before breakdown voltage (V_{BD}), although the V_{BD} is lower in 10 ppm contaminated devices than 10 ppb case. Such effect was previously attributed to the Cu trap energy state inside the SiO_2 dielectric [5.11]; the leakage current shows exponential relation with the trap energy in direct tunneling regime with less concentration dependence. In contrast to the large increasing leakage current (2 orders of magnitude) in SiO_2 MOS capacitors contaminated by Cu, negligible leakage current increase in Al_2O_3 MOS capacitors is measured with high 10 ppm Cu contamination. The reason why the Cu contamination has little effect on the Al_2O_3 gate dielectric may be due to the strong diffusion barrier property similar to Si_3N_4, where the Al_2O_3 can even be used as the diffusion barrier for small H_2 molecule [5.17].

Figs. 5-2(a), 5-2(b) and 5-2(c) further compare the cumulative leakage current distributions of the 42 Å Al_2O_3 (19 Å EOT), 30 Å SiO_2, and 36 Å oxynitride with 23% N content (30 Å EOT), respectively. The control gate oxide leakage current of 30

Å SiO_2 MOS device shows an increasing trend by one to two orders of magnitude at 0.5 V and 2.5 V bias with increasing Cu concentration from 10 ppb to 10 ppm. In sharp contrast, only slightly increasing leakage current at lowest 0.5 V bias can be observed in the 42 Å Al_2O_3 (19 Å EOT). This increasing leakage current in pre-tunneling region at low voltage is also previously observed in thick 50 Å SiO_2 and oxynitride with 16% N content [5.10]-[5.12], which is attributed to the trap-assisted tunneling originated by neutral traps formed by Cu inside the oxide matrix. It is noticed that although the degradation of pre-tunneling leakage current is negligible for the 36 Å oxynitride with 23% N, the Al_2O_3 still has strong advantage of much smaller EOT of only 19 Å than the 30 Å EOT oxynitride (23% N). In addition, the k value of 8.5 for Al_2O_3 is also higher than the 4.7 k value for 23% N oxynitride [5.10], which is important for gate dielectric application in nm-scale MOSFET.

Fig. 5-3(a) shows the comparison of Q_{BD} distribution of 42 Å Al_2O_3 gate dielectric (19 Å EOT) with the control 30 Å thermal oxide, with or without the Cu contamination. The good quality of control 30 Å oxide without contamination is evidenced from the high Q_{BD} of ~0.13 C/cm^2 (–4.3 V constant voltage stress) and close to the published data [5.18]. The Cu contamination effect on SiO_2 gate capacitor lowers down the Q_{BD} with a wider distribution, which is consistent with the larger distribution of leakage current shown in Fig. 5-2(b). In sharp contrast, the Cu contamination at both 10 ppb and 10 ppm has only small effects on Q_{BD} distribution of the 19 Å EOT Al_2O_3 gate dielectric and free from the trail Q_{BD} distribution devices. This result is also consistent with the tight gate current distribution shown in Fig. 5-2(a). It is noticed that the Q_{BD} value decreases rapidly with increasing stress voltage, and the mean Q_{BD} of 0.4 C/cm^2 for 42 Å Al_2O_3 gate dielectric, biased at a large voltage of 5.8 V, is also comparable to SiO_2 within in same order [5.18]. This suggests the excellent quality of high-k Al_2O_3 gate dielectric. Fig. 5-3(b) further shows the time to breakdown (t_{BD}) plot stressed at -4V at 150°C. The larger t_{BD} decrease of Cu contaminated SiO_2 than that of Al_2O_3 is due to the larger increase of leakage current in SiO_2 after contamination shown in Fig. 5-1.

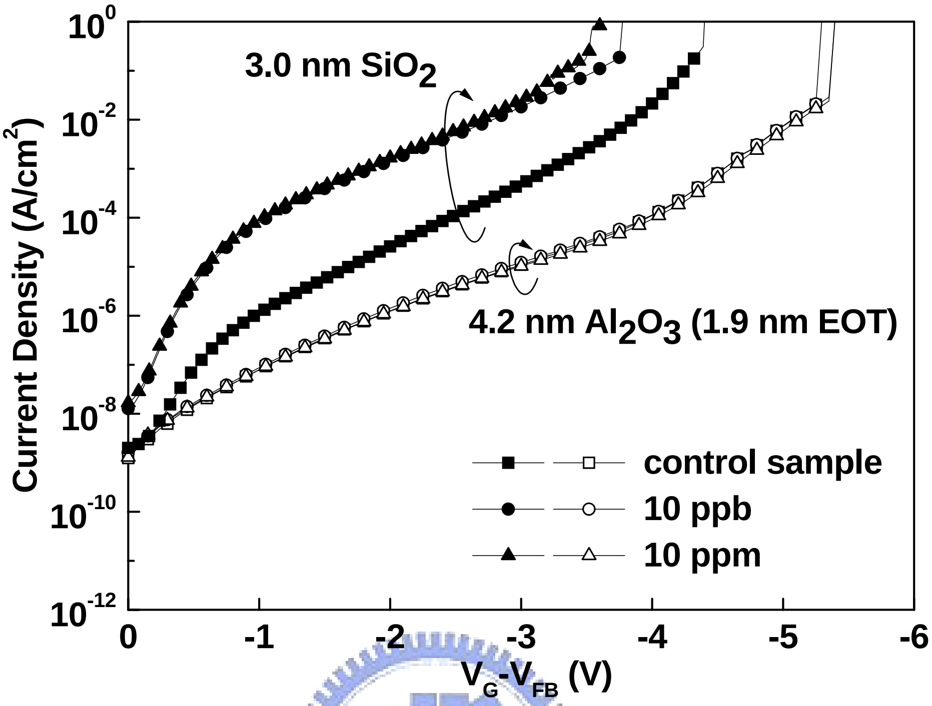
The SILC is another important factor for gate dielectric reliability evaluation. Figs. 5-4(a) and 5-4(b) show the comparison of the stress effect on J-V characteristics for MOS capacitors with 42 Å Al_2O_3 gate dielectric (1.9nm EOT) and 30 Å thermal oxides, respectively, with or without Cu contamination. In both cases, the applied stress condition is at –3.3 V for 10,000 sec. It is noticed that although the amount of injected charges is less for Al_2O_3 dielectric than SiO_2, this is due to the fundamental advantage for high-k gate dielectric with largely improved gate leakage current. Among all the Al_2O_3 and SiO_2 MOS devices with or without Cu contamination, the control 30 Å SiO_2 MOS capacitor has the smallest current change and better than the

42 Å Al_2O_3 MOS device under the same stress condition. This is due to the robustness of thermal SiO_2 where larger bulk oxide and interface defects are usually found in high-k dielectric such as Al_2O_3. The amount of these weak defects will increase under charge injection during constant voltage stress, which causes higher leakage current in MOS capacitors.

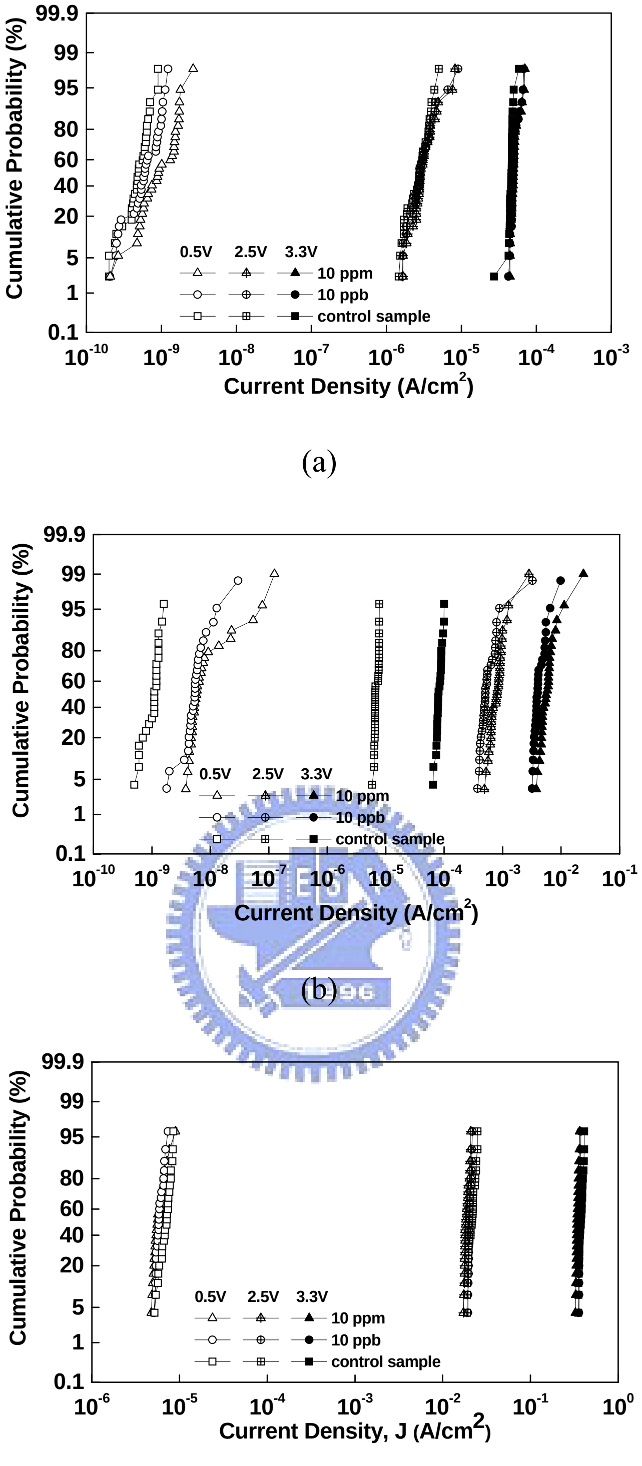
To further analyze the SILC effect, we have plotted the current change $(J_{stressed} - J_0)/J_0$ as a function of bias voltage in Fig. 5-5, which is more sensitive than the $J_{stressed}$-V plot shown in Fig. 5-4. For the un-contaminated Al_2O_3 and SiO_2 MOS devices shown in Figs. 5-5(a) and 5-5(b) respectively, the Al_2O_3 dielectric capacitor has higher SILC current than the SiO_2 devices, even though the dielectric thickness (42 Å) for Al_2O_3 is thicker than the SiO_2 (30 Å). This is due to the higher bulk and interface defects in high-k Al_2O_3 gate dielectric than thermal SiO_2. However, the SILC of $\Delta J/J_0$ increases rapidly in the SiO_2 devices even under the smallest Cu contamination of 10 ppb. The increasing SILC with Cu contamination is previously attributed to the formation of neutral traps inside the oxide and interface [5.12]. In contrast, the $\Delta J/J_0$ only increases slightly at 10 ppb Cu contamination and the amount of increase at 10 ppm Cu is still less than the SiO_2 case. The smaller amount of Cu contamination generated SILC in Al_2O_3 gate dielectric suggests the good diffusion barrier property and also consistent with the smaller degradation on dielectric leakage current and Q_{BD} shown in Figs. 5-1 and 5-3.

5.4 Conclusion

We have studied the Cu contamination effects on gate dielectric integrity of 42 Å Al_2O_3 dielectric. By comparing with the control 30 Å SiO_2 MOS capacitors contaminated by Cu, much smaller degradation of gate dielectric leakage current, Q_{BD} and SILC is found in 19 Å EOT Al_2O_3 MOS devices. The much better resistance of Cu contamination in ultra-thin 19 Å EOT Al_2O_3 MOS capacitor is the strong advantage for high-k Al_2O_3 gate dielectric.



5.4 The J-(V_G-V_{FB}) characteristics of MOS capacitors with 42 Å Al_2O_3 gate dielectric (19 Å EOT) with or without Cu contamination. The MOS devices with 30 Å thermal SiO_2 are also added for comparison. The devices were contaminated by 10 ppb or 10 ppm Cu.

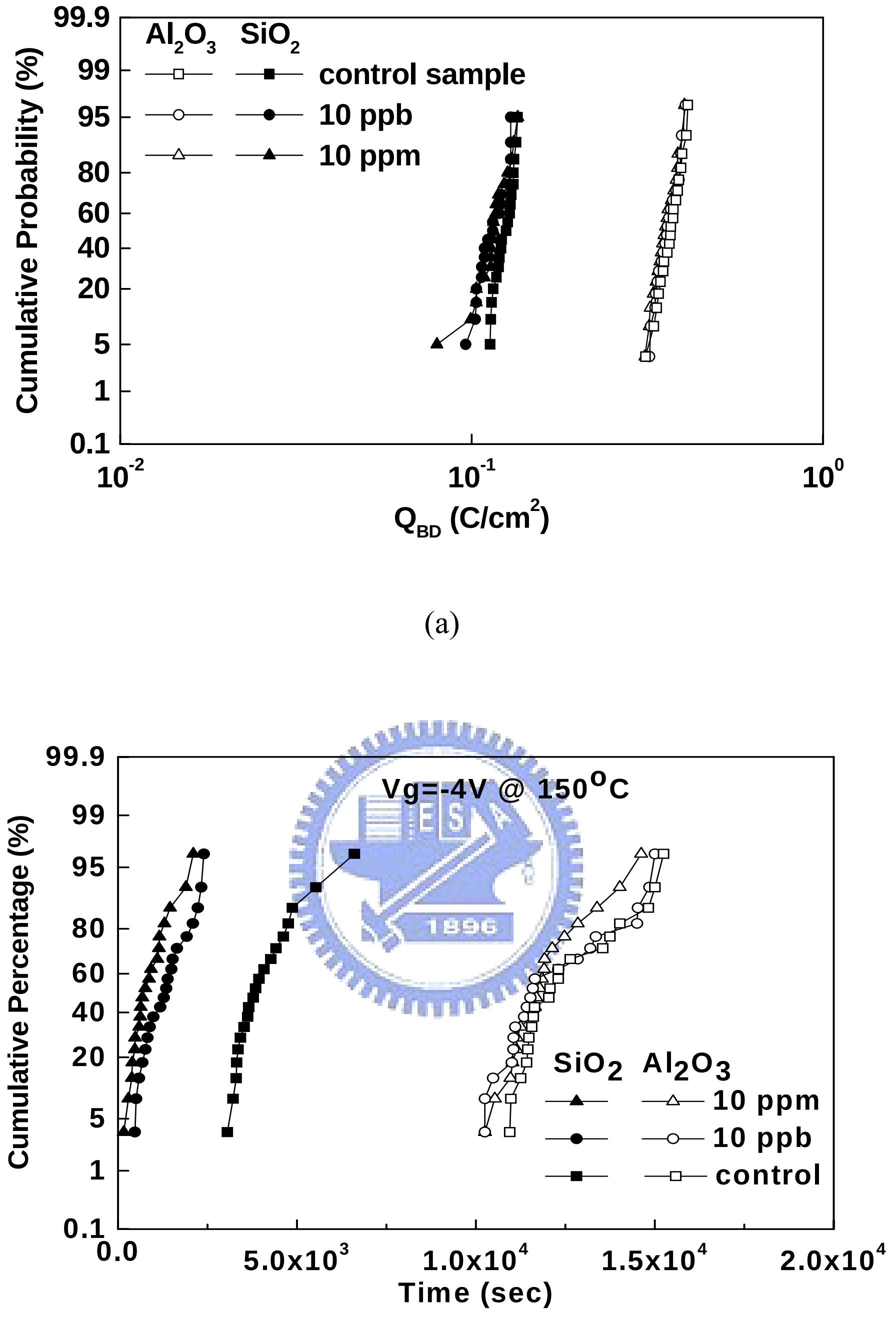


(a)

(b)

(c)

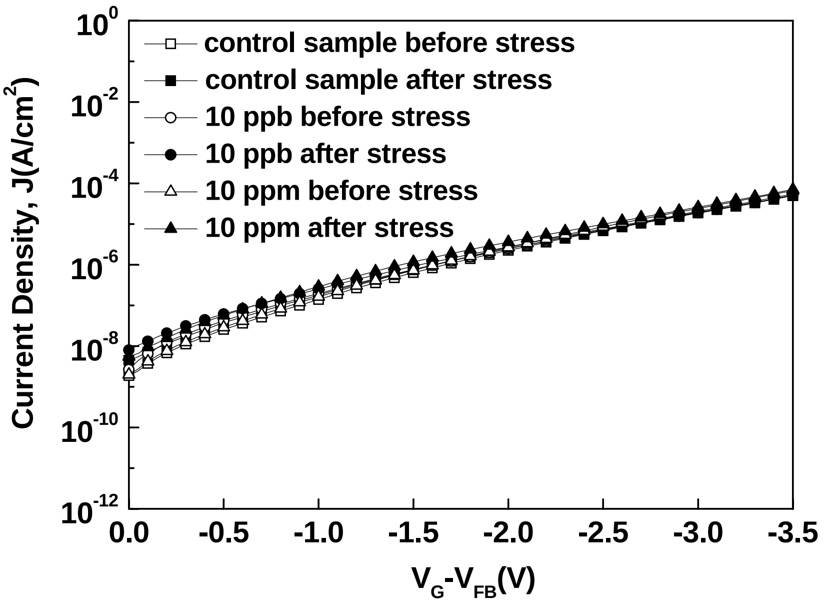
Fig. 5-2 The distribution of leakage current density for (a) 42 Å Al_2O_3 gate dielectric (19 Å EOT), (b) 30 Å thermal SiO_2 and (c) 36 Å SiON with 23%N content (30 Å EOT) gate dielectrics with or without Cu contamination.



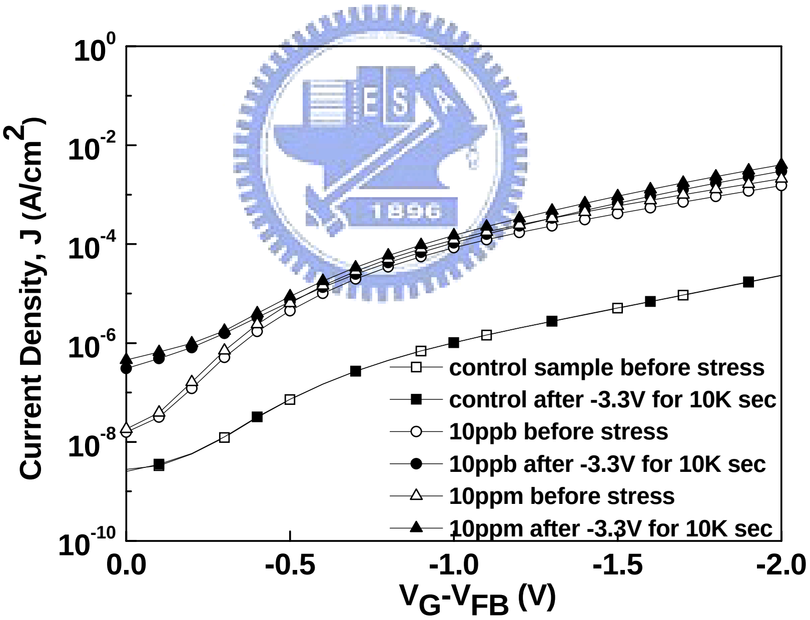
(a)

(b)

Fig. 5-3 The (a) Q_{BD} and (b) t_{BD} distribution of 42 Å Al_2O_3 gate dielectric (19 Å EOT) MOS devices under different Cu contamination level. The distributions of 30 Å SiO_2 MOS capacitors with or without Cu contamination are also added for comparison.

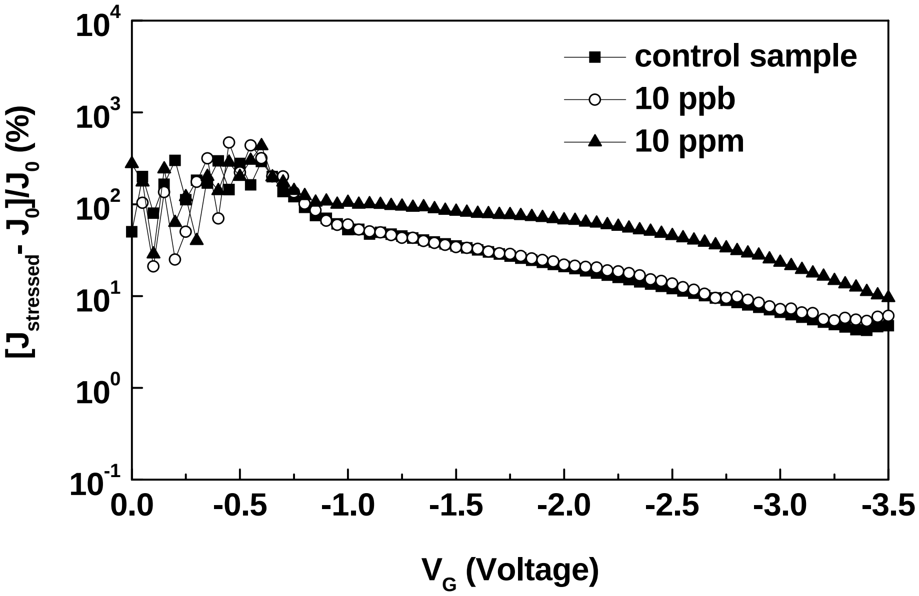


(a)

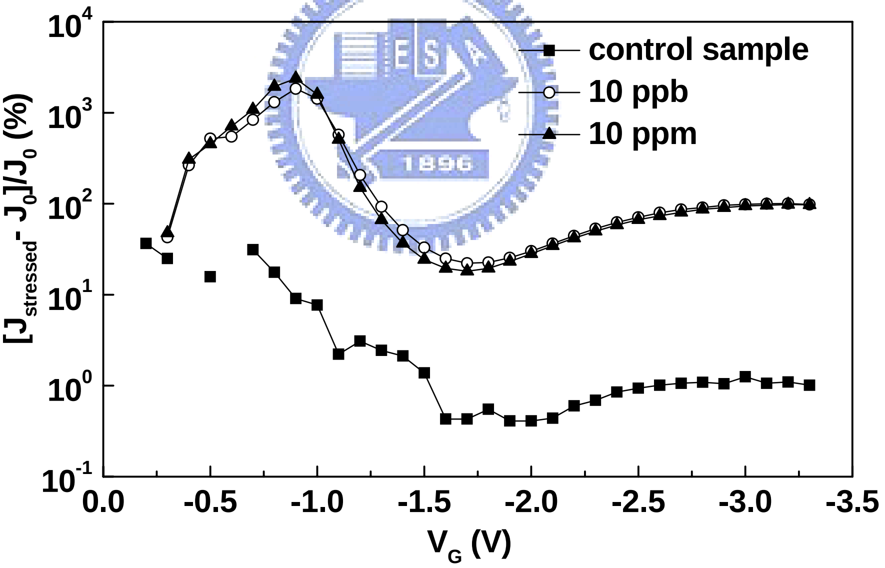


(b)

Fig. 5-4 The stress effect on J-(V_G-V_{FB}) characteristics for MOS capacitors contaminated by Cu with (a) 42 Å Al_2O_3 gate dielectric (19 Å EOT) and (b) 30 Å SiO_2. The applied stress condition is at –3.3 V for 10,000 sec.



(a)



(b)

Fig. 5-5 The stress and Cu contamination effect on ΔJ/J-V characteristics of (a) 42 Å Al_2O_3 gate dielectric (19 Å EOT) and (b) control 30 Å SiO_2 MOS capacitors.

Chapter 6

Conclusion

A new and simple approach has been proposed to deposit high-k dielectrics on Si substrate. Aluminum oxide (Al_2O_3) high-k dielectric is deposited by evaporating the ultra thin metal layer followed by thermal oxidation and annealing. Utilizing the self-limit characteristic of Al_2O_3, the formation of interface oxide in high-k dielectrics can be eliminated effectively. To investigate the performance of Al_2O_3 for the use of MOSFET devices, we have fabricated 48 Å Al_2O_3 films with ~6 orders lower leakage current than 13 Å SiO_2 films and low interface state density at the Al_2O_3/Si interface than Si_3N_4/Si interface. We further successful applied Al_2O_3 as MOSFET insulator and get acceptable performance. So, the lower leakage current characteristics of Al_2O_3 films and mobility of Al_2O_3 MOSFET comparable to published mobility data from thermal SiO_2 do qualify this dielectric for the gate dielectric application.

BTI of MOSFETs has been one of the biggest reliability problems in the high-k gate dielectric. In order to characterize the BTI in Al_2O_3, we have measured the NBTI and PBTI effects on fully silicided-gate/Al_2O_3 CMOSFETs and compared with benchmark poly-Si/oxynitride devices. The fully silicided-gate/Al_2O_3 have merits of simple process and fully compatible to current VLSI process line; the metal-gates may be more suitable for achieving small EOT. Although both the V_t changes and extrapolated operation voltages for 10 years lifetime for fully silicided-gate/Al_2O_3 are worse than benchmark poly-Si/oxynitride devices, the high-k devices can still barely meet the required 1 V operation voltage for 10 year lifetime. Further improvement is still required since the 18 Å oxynitride CMOSFETs have higher 10 years lifetime operation voltage.

We have further characterized the Cu contamination effect on gate dielectric integrity of 42 Å thick Al_2O_3 MOS capacitors with an EOT of 19 Å. The gate dielectric degradation by Cu contamination is greatly reduced in Al_2O_3 dielectric as compared with the control 30 Å thermal SiO_2 MOS capacitors contamination by Cu. The good Cu contamination resistance of Al_2O_3 gate dielectric is attributed to the strong diffusion barrier property of the Al_2O_3 dielectric as observed gate dielectric leakage current, charge-to-breakdown and SILC. This strong Cu contamination resistance is similar to oxynitride but Al_2O_3 gate dielectric has the advantage of higher k-value. This simple technique to deposit high-k Al_2O_3 dielectrics has demonstrated its practicability in device fabrication and its flexibility to develop the suitable high-k dielectrics for the use of gate dielectric in MOSFETs application.

References

Chapter 1

[1.1] H. S. Mormose, M. Ono, T. yodhitomi, T. Ohgure, S-I Nakamura, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *IEEE Trans, Electron Dev.* 43, pp. 1233, 1996.

[1.2] Timp, G.; Agarwal, A.; Baumann, F.H.; Boone, T.; Buonanno, M.; Cirelli, R.; Donnelly, V.; Foad, M.; Grant, D.; Green, M.; Gossmann, H.; Hillenius, S.; Jackson, J.; Jacobson, D.; Kleiman, R.; Komblit, A.; Klemens, F.; Lee, J.T.-C.; Mansfield, W.; Moccio, S.; Murrell, A.; O'Malley, M.; Rosamilia, J.; Sapjeta, J.; Silverman, P.; Sorsch, T.; Tai, W.W.; Tennant, D.; Vuong, H.; Weir, B, " Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm nMOSFETs, " *Int'l Electron Devices Meeting (IEDM) Tech.* pp. 930, 1997.

[1.3] Albert Chin, W. J. Chen, T. Chang, R. H. Kao, B. C. Lin, C. Tsia, and J. C-M. Huang, " Thin Oxides with *in situ* Native Oxide Removal," I*EEE Electron Device Lett.* 18, pp. 417, 1997.

[1.4] The national Technology Roadmap for Semiconductors, 2002.

[1.5] H. –H. Tseng, P. G. Y. Tsui, P. J. Tobin, J. Mogab, M. Khare, X. W. Wang, T. P. Ma, R. Hedge, C. Hobbs, J.Veteran, M. Hartig, G. Kenig, V. Wang, R. Blumenthal, R. Cotton, V. Kaushik, T. Tamagawa, B. L. Halpern, G. J. Cui, and J. J. Schmitt, " Application of JVD Nitride Gate Dielectric to A 0.35 Micron CMOS Process for Reduction of Gate Leakage Current And Boron Penetration," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 647, 1997.

[1.6] D. Park, Qiang Lu, Tsu-Jae King, Chenming Hu, A. Kalnitsky, S. p. Tay, and C. C. Cheng, "SiON/Ta_2O_5/TiN Gate-Stack Transistor with 1.8nm Equivalent SiO_2 Thickness," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 381, 1998.

[1.7] X. Guo, T. P. Ma, T. Tamagaw, and B. L. Halpern. "High Quality Ultra-thin TiO_2/Si_3N_4 Gate Dielectric for Giga Scale MOS Technology," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 377, 1998.

[1.8] K. J. Hubbard and D. G. Schlom, J. Mater. Res. 11, pp. 2757, 1996.

[1.9] B. He, T. Ma, S. A. Campbcll, and W. L. Gladfelter, "A 1.1nm Oxide Equivalent Gate Insulator Formed Using TiO_2 on Nitrided Silicon," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 1038, 1998.

[1.10] C. Hobbs, R. Hegde, B. Maiti, H. Tseng, D. Gilmer, P. Tobin, O. Adetutu, F. Huang, D. Weddington, R. Nagabushnam, D. O'Meara, K. Reid, L. La, L. Grove and M. Rossow, "Sub-quarter micron CMOS process for TiN-gate MOSFETs with TiO_2 gate dielectric formed by titanium oxidation," in *Symp. on VLSI Technology*, , pp.133-134, 1999.

[1.11] H.-J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E.

Dharmarajan and J. C. Lee, "Novel nitrogen profile engineering for improved TaN/HfO_2 Si MOSFET performance," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp.30.2.1-30.2.4, 2001.

[1.12] Y. Abe, T. Oishi, K. Shiozawa, Y. Tokuda and S. Satoh, "Simulation study on comparison between metal gate and polysilicon gate for sub-quartermicron MOSFETs," *IEEE Electron Device Lett.*, 20, pp. 632-634, 1999.

[1.13] S. M. Sze, " Physics of Semiconductor Devices," 2nd Edition, John Wiley and Sons. Inc, 1985, ch. 8.

[1.14] T. Y. Chang, R. E. Behringer, R. E. Howard, A. S. H. Liao, L. D. Jackel, E. A. Caridi, W. J. Skocpol, and R. W. Epworth, *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 356, 1984.

Chapter 2

[2.1] K. F. Schuegraf, C. C. King, and C. Hu, "Ultra-thin silicon dioxide leakage current and scaling limit," *VLSI Technology*, 1992. Digest of Technical Papers. 1992 Symposium on 2-4 June 1992.

[2.2] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nskamura, M. Saito, and H. Iwai, **"**1.5 nm direct-tunneling gate oxide Si MOSFET's, "*IEEE Trans. Electron Devices* 43 (1996) 1233.

[2.3] Chin, W.J. Chen, T. Chang, R.H. Kao, B.C. Lin, C. Tsai, and J.C.M. Huang, "Thin Oxides with in Situ Native Oxide Removal," *IEEE Electron Device Letters* 18, 417-419 (1997).

[2.4] The National Technology Roadmap for Semiconductors (1997), 74.

[2.5] W. H. Lee, J. T. Clemens, R. C. Keller, and L. Manchanda, "A Novel High K Inter-poly Dielectric (IPD), A1/sub-2/O/sub-3/ For Low Voltage/high Speed Flash memories: erasing in msecs at 3.3V," VLSI Technology, 1997. Digest of Technical Papers., 1997 Symposium on , June 10-12, 1997, Pages:117 - 118.

[2.6] T. Y. Chang, R. E. Behringer, R. E. Howard, A. S. H. Liao, L. D. Jackel, E. A. Caridi, W. J. Skocpol, and R. W. Epworth, *Int'l Electron Devices Meeting Tech.* Dig. 356. 1984.

[2.7] A. Chin, B.C. Lin, W.J. Chen, Y.B. Lin, and C. Tsai, "The Effect of Native

Oxide on Thin Gate Oxide Integrity, ” *IEEE Electron Device Lett.*, 19, pp. 426-428, Nov. 1998.

[2.8] T. Liu, A. Ghetti, Y. Ma, G. Alers, C. P. Chang, K. P. Cheung, J. I. Colonell, W. Y. C. Lai, C. S. Pai, R. Liu, H. Vaidya, and J. T. Clemens, “Intrinsic and stress-induced traps in the direct tunneling current of 2.3-3.8 nm oxides and unified characterization methodologies of sub-3 nm oxides,” *Electron Devices Meeting, (1997). Technical Digest., International* , 7-10 Dec. 1997, Pages:85 - 88.

[2.9] B. C. Lin, Y. C. Cheng, A. Chin, T. Wang, and C. Tsai, “The Deuterium Effect on SILC,” *30th Solid State Devices and Materials (SSDM)*, Hiroshima, Japan, Sept. 1998.

Chapter 3

[3.1] S. Song, H. F. Luan, Y. Y. Chen, M. Gardner, J. Fulford, M, Allen and D. L. Kwong, "Ultra Thin (<20 Å) CVD Si_3N_4 Gate Dielectric for Deep-Sub-Micron CMOS Devices," *Int'l Electron Devices Meeting (IEDM) Tech.* Dig., pp. 373, 1998

[3.2] X. Guo, T. P. Ma, T. Tamagawa, and B. L. Halpern, " High Quality Ultra-thin TiO_2/Si_3N_4 Gate Dielectric for Giga Scale MOS Technology," *Int'l Electron Devices Meeting (IEDM*) Tech. Dig., pp.377, 1998

[3.3] D. Park, Qiang Lu, Tsu-Jae King, Chenming Hu, A. Kalnitsky, S. p. Tay, and C. C. Cheng, "$SiON/Ta_2O_5/TiN$ Gate-Stack Transistor with 1.8nm Equivalent SiO_2 Thickness," *Int'l Electron Devices Meeting (IEDM) Tech.*, pp. 381, 1998.

[3.4] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi and J ack C. Lee, "Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," *Int'l Electron Devices Meeting (IEDM) Tech.* Dig., p.133, 1999

[3.5] Y. Ma, Y. Ono, L. Stecker, David R. Evans, and S. T. Hsu, "Zirconium Oxide Based Gate Dielecyrics with Equivalent Oxide Thickness of Less Than 1.0nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process," *Int'l Electron Devices Meeting (IEDM)* Tech. Dig., pp. 149, 1999

[3.6] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, “Device and Reliability of High-K Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it},” *Symp. on VLSI Technology*, pp. 133-134, Japan, June 1999.

[3.7] H. Kimijima, T. Ohguro, B. Evans, B. Acker, J. Bloom, H. Mabuchi, D. L. Kwong, Eiji Morifuji, T. Yoshitomi, H. Sasaki Mornose, M. Kinugawa, Y. Katsumara, and H. Twai “Improvement of 1/f noise using VHP (Vertical High Pressure) oxynitride gate insulator for deep-sub micron RF and analog CMOS,” *Symp. on VLSI Technology*, pp. 119-120, Japan, June 1999.

[3.8] Manchanda, L.; Lee, W.H.; Bower, J.E.; Baumann, F.H.; Brown, W.L.; Case, C.J.; Keller, R.C.; Kim, Y.O.; Laskowski, E.J.; Morris, M.D.; Opila, R.L.; Silverman, P.J.; Sorsch, T.W.; Weber, G.R., “ Gate quality doped high K films for CMOS beyond 100 nm: 3-10 nm Al $_2O_3$ with low leakage and low interface states, ” *Int’l Electron Devices Meeting (IEDM)* Tech. Dig., p.605, 1998

[3.9] C. C. Liao, A. Chin, and C. Tsai, “Electrical Characterization of Al_2O_3 on Si from MBE-grown AlAs and Al,” *10th International Conference on Molecular Beam Epitaxy (MBE),* Cannes, France, August 1998.

[3.10] A. Chin et al., Intl. Reliability Phys. Symp., CA, March 1999.

[3.11] Y. H. Wu and A. Chin, “Gate oxide integrity of thermal oxide grown on high temperature formed $Si_{0.3}Ge_{0.7}$," *IEEE Electron Device Lett.* 21, 113, 2000.

[3.12] Y. Taur & T. H. Ning, Fund. *Modern VLSI Devices*, pp.106, 1998

Chapter 4

[4.1] X. Yu, C. X. Zhu, X. P. Wang, M. F. Li, Albert Chin, A. Du, W. D. Wang, D. L. Kwong, “High Mobility and Excellent Threshold Voltage Stability of NMOSFETs Using HfTaO Gate Dielectrics,” *Symp. on VLSI Technology*, pp.110, US, June 2004.

[4.2] H. Y. Yu, J. F. Kang, J. D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M.-F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du, and D.-L. Kwong, “Thermally Robust High Quality HfN/HfO_2 Gate Stack for Advanced CMOS Devices,” *Int’l Electron Devices Meeting (IEDM) Tech. Dig.*, 99, 2003.

[4.3] C. H. Lee, J. J. Lee, W. P. Bai, S. H. Bae, J. H. Sim, X. Lei, R. D. Clark, Y. Harada, M. Niwa, and D. L. Kwong, “Self-aligned ultra thin HfO/sub-2/CMOS transistors with high quality CVD TaN gate electrode,” *Symp. on VLSI Technology Dig.*, 82, 2002.

[4.4] H. Zhong, S. N. Hong, Y. S. Suh, H. Lazar, G. Heuss and V. Misra, “Properties of Ru-Ta Alloys as Gtae Electrodes For NMOS and PMOS Silicon Devices,” *Int’l Electron Devices Meeting (IEDM) Tech. Dig.*, 467, 2001.

[4.5] C. H. Huang, D. S. Yu, A. Chin, W. J. Chen, C. X. Zhu, M.-F. Li, B. J. Cho, and D. L. Kwong, “Fully Silicided NiSi and Germanided NiGe Dual Gates on SiO2/Si and Al2O3/Ge-On-Insulator MOSFETs,” International Electron

Devices Meeting (IEDM) Tech. Dig., pp. 319-322, Washington DC, Dec. 2003.

[4.6] S. J. Doh, H.-S. Jung, Y.-S. Kim, H.-J. Lim, J. P. Kim, J. H. Lee, J.-H. Lee, N.-I. Lee, H.-K. Kang, K.-P. Suh, S. G. Park, S. B. Kang, G. H. Choi, Y.-S. Chung, H.-S. Baikz, H.-S. Chang, M.-H. Cho, D.-W. Moon, H. B. Park, M. Cho, and C. S. Hwang, "Improvement of NBTI and Electrical Characteristics by Ozone Pre-treatment and PBTI issues in HfAlO(N) High-k Gate Dielectrics," *Int'l Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 943, 2003.

[4.7] A. Shanware, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, J. McPherson, and L. Colombo, "Characterization and Comparison of the Charge Trapping in HfSiON and HfO_2 Gate Dielectrics," *Int'l Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 939, 2003.

[4.8] K. Onishi, C. S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, E. Dharmarajan, and J. C. Lee, "Reliability Characteristics, Including NBTI, of Polysilicon Gate HfO_2 MOSFET's," *Int'l Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 659 2001.

[4.9] T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and D. L. Kwong," Engineering of nitrogen profile in an ultrathin gate insulator to improve transistor performance and NBTI,**"** *IEEE Electron Device Lett.* 24, pp. 150, 2003.

[4.10] J. Yugami, S. Tsujikawa, R. Tsuchiya, S. Saito, Y. Shimamoto, K. Torii, T. Mine, and T. Onai, “Advanced oxynitride gate dielectrics for CMOS applications,” Gate Insulator, 2003. IWGI 2003. Extended Abstracts of International Workshop on, 6-7 Nov. 2003, Pages: 140 - 145.

[4.11] K. Ichinose, T. Saito, Y. Yanagida, Y. Nonaka, K. Torii, H. Saito, S. Wada, K. Mori, and S. Mitani, “A high performance 0.12 μm CMOS with manufacturable 0.18 μm technology,” *Symp. on VLSI Technology Dig.*, pp. 103, 2001.

[4.12] S. Saito, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, D. Hisamoto, T. Mine, K. Torii, J. Yugami, M. Hiratani, T. Onai, and S. Kimura, “Impact of oxygen-enriched SiN interface on Al/sub 2/O/sub 3/ gate stack. An innovative solution to low-power CMOS,” *Symp. on VLSI Technology Dig.*, pp. 145, 2003.

[4.13] E. Morifuji, T. Kumamori, M. Muta, K. Suzuki, M. S. Krishnan, T. Brozek, X. Li, W. Asano, M. Nishigori, N. Yanagiya, S. Yamada, K. Miyamoto, T. Noguchi, and M. Kakumu, “New guideline for hydrogen treatment in advanced system LSI,” *Symp. on VLSI Technology Dig.*, pp. 218, 2002.

[4.14] J. Ushio, K. Kushida-Abdelghafar, and T. Maruizumi, “Interface structures generated by negative-bias temperature instability in Si/SiO_2 and Si/SiO_xN_y

interfaces," Int'l Semiconductor Device Research Symp. (ISDRS) Dig., pp. 158 2001.

[4.15] D. S. Yu, C. H. Wu, C. H. Huang, Albert Chin, W. J. Chen, Chunxiang Zhu, M. F. Li, and Dim-Lee Kwong, "Fully Silicided NiSi and Germanided NiGe Dual Gates on SiO2 n- and p-MOSFETs," IEEE Electron Device Lett. 24, no. 12, pp. 739-741, 2003.

[4.16] C. Y. Lin, M. W. Ma, A. Chin, C. Zhu, M. F. Li, and D. L. Kwong, "Fully silicided NiSi gate on La2O3 MOSFETs," IEEE Electron Device Lett. 24, pp. 348-350, May 2003.

[4.17] D. S. Yu, C. H. Huang, Albert Chin, C. Zhu, M. F. Li, B. J. Cho, and D. L. Kwong, "Al_2O_3/Ge-On-Insulator n- and p-MOSFETs with Fully NiSi and NiGe Dual Gates," IEEE Electron Device Lett. 25, no. 3, pp. 138-140 2004.

[4.18] D. S. Yu, A. Chin, B. F. Hung, W. J. Chen, C. X. Zhu, M.-F. Li, S. Y. Zhu and D. L. Kwong, "Low Workfunction Fully Silicided Gate on SiO2/Si and LaAlO3/GOI n-MOSFETs," 62th Device Research Conference (DRC), pp. 21, Notre Dame, IN, June 2004.

[4.19] D. S. Yu, C. F. Cheng, Albert Chin, C. Zhu, M.-F. Li, and Dim-Lee Kwong, "High Performance fully silicided NiSi:Hf gate on $LaAlO_3$/GOI n-MOSFET with Little Fermi-level Pinning" Int'l Solid-State Devices& Materials Conf.

(SSDM), Sept. 15-17, Tokyo, Japan.

[4.20] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, “Device and Reliability of High-K Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it},” Symp. on VLSI Technology, pp.133-134, Japan, June 1999.

[4.21] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, “High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Oxide Thickness 5-10Å,” *Symp. on VLSI Technology*, pp. 16-17, US, June 2000. (Highlight Section Paper).

[4.22] S. V. Hattangady, R. Kraft, D. T. Grider, M. A. Douglas, G. A. Brown, P. A. Tiner, J. W. Kuehne, P. E. Nicollian, and M. F. Pas, **“**Ultrathin nitrogen-profile engineered gate dielectric films,” *Electron Devices Meeting, 1996., International* , 8-11 Dec. 1996, Pages:495 – 498.

[4.23] M. A. Alam, “A Critical Examination of the Mechanics of Dynamic NBTI for PMOSFETs,” *Int’l Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 345, 2003.

[4.24] S. Datta, G. Dewey, M. Doczy, B. S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick, and R. Chau, “High Mobility Si/SiGe Strained Channel MOS Transistors with HfO_2/TiN Gate Stack,” *Int’l Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 653, 2003.

[4.25] D. S. Yu, Albert Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li^3, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with Novel IrO$_2$(Hf) Dual Gates and High-k Dielectric on 1P6M-0.18 m-CMOS," *International Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 181-184, San Francisco, Dec. 2004.

[4.26] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "RF MIM Capacitors Using High-k Al$_2$O$_3$ and AlTiOx Dielectrics," *IEEE MTT-S International Microwave Symp. Dig.*, vol. 1, pp. 201-204, June 2002.

[4.27] M.Y. Yang, C.H. Huang, A. Chin, C. Zhu, B.J. Cho, M.F. Li, and Dim-Lee Kwong, "Very high density RF MIM capacitors (17fF/μm2) using high-κ Al$_2$O$_3$ doped Ta$_2$O$_5$ dielectrics," *IEEE Microwave & Wireless Components Lett.* 13, pp. 431, 2003.

[4.28] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, M. F. Li, and D. L. Kwong, "High Density MIM Capacitors Using AlTaO$_x$ Dielectrics," *IEEE Electron Device Lett.* 24, pp. 306-308, May 2003.

[4.29] C. H. Huang, M.Y. Yang, A. Chin, C. X. Zhu, M. F. Li, and D. L. Kwong, "High Density RF MIM Capacitors Using High-k AlTaO$_x$ Dielectrics," *IEEE MTT-S International Microwave Symp. Dig.*, vol. 1, pp. 507-510, June 8-13, 2003.

Chapter 5

[5.1] D. A. Ramappa and W. B. Henley, *J. Electrochemical Soc.*, 146, pp. 2258, 1999.

[5.2] B. Vermeire, L. Lee, and H. G. Parks, “The effect of copper contamination on field overlap edges and perimeter junction leakage current,” *IEEE Trans. Semiconductor Manufact.* 11, pp. 232, 1998.

[5.3] P. Motte, J. Torres, J. Palleau, F. Tardif and H. Bernard, *Solid-State Electronics* 43, pp. 1015, 1999.

[5.4] T. Gravier, F. Braud, J. Torres, J. Palleau, A. Chantre, and J. Kirtsch, *Microelectronic Engineering*, 33, pp. 211, 1997.

[5.5] T. Heiser, S. McHugo, H. Hieslmair and E. R. Weber, *Appl. Phys. Lett.* 26, pp. 3576, 1997.

[5.6] Y. Shacham-Diamand, A. Dedhia, D. Hoffstetter, and W. G. Oldham, “Reliability of copper metallization on silicon-dioxide,” *VLSI Multilevel Interconnection Conference, 1991, Proceedings., Eighth International IEEE* , 11-12 June 1991, Pages:109 - 115.

[5.7] K. Hozawa, T. Itoga, S. Isomae, J. Yugami, and M. Ohkura, “Copper distribution behavior near a SiO_2/Si interface by low-temperature (<400°C) annealing and its influence on electrical characteristics of MOS-capacitors,” *Symp. on VLSI Technology*, 24, 2000.

[5.8] A. Correia, D. Ballutaud, and J. L. Naurice, *Jpn. J. Appl. Phys.* 33, 1217 (1994).

[5.9] M. Inohara, H. Sakurai, T. Yamaguchi, H. Tomita, T. Iijima, H. Oyamatsu, T. Nakayama, H. Yoshimura, and Y. Toyoshima, "Copper Contamination Induced Degradation of MOSFET Characteristics and Reliability," *Symp. on VLSI Technology*, pp. 26-27, US, June 2000.

[5.10] Y. H. Lin, F. M. Pan, Y. C. Liao, Y. C. Chen, I. J. Hsieh, and A. Chin, "The Cu contamination effect in oxynitride gate dielectrics," *J. Electrochem. Soc.* 148, G627, 2001.

[5.11] Y. H. Lin, Y. C. Chen, K. T. Chan, F. M. Pan, I. J. Hsieh, and A. Chin, "The strong degradation on 30 Å oxide integrity contaminated by copper," *J. Electrochem. Soc.* 148, F73, 2001.

[5.12] Y. H. Lin, Y. H. Wu, A. Chin, and F. M. Pan "The effect of copper on gate oxide integrity," *J. Electrochem. Soc.* 147, pp. 4305, 2000.

[5.13] C. H. Huang, D. S. Yu, A. Chin, W. J. Chen, C. X. Zhu, M.-F. Li, B. J. Cho, and D. L. Kwong, "Fully Silicided NiSi and Germanided NiGe Dual Gates on SiO_2/Si and Al_2O_3/Ge-On-Insulator MOSFETs," *International Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 319-322, Washington DC, Dec. 2003.

[5.14] H. Hu, C. Zhu, X. Yu, A. Chin, M. F. Li, B. J. Cho, and D. L. Kwong, "MIM Capacitors Using Atomic-Layer-Deposited High-k $(HfO_2)_{1-x}(Al_2O_3)_x$ dielectrics," *IEEE Electron Device Lett.* 24, no. 2, pp. 60-62, 2003.

[5.15] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, "Device and Reliability of High-k Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," *Symp. on VLSI Technology*, p.133-134, Japan, June 1999.

[5.16] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Oxide Thickness 5-10Å," *Symp. on VLSI Technology*, pp. 16-17, US, June 2000. (Highlight Section Paper).

[5.17] D. J. Jung, B. G. Jeon,H. H. Kim, Y. J. Song, B. J. Koo, S. Y. Lee, S. O. Park, Y. W. Park, and K. Kim, "Highly manufacturable 1T1C 4 Mb FRAM with novel sensing scheme," *Int'l Electron Devices Meeting (IEDM) Tech. Dig.*, 279 (1999).

[5.18] Y. Taur and T. K. Ning, *Fundamental Modern VLSI Devices*, p. 106, Cambridge University Press, N.

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Publication list

(A) International Journal:

[1]. D. S. Yu, A. Chin, **C. C. Liao**, C. F. Lee, C. F. Cheng, M. F. Li', Won Jong Yoo, and S. P. McAlister, "3D Metal-Gate/High-k/GOI CMOSFETs on 1-Poly-6-Metal 0.18-um Si Devices," *IEEE Electron Device Lett.* 25, no., pp., 2005.

[2]. **C. C. Liao**, D. S. Yu, C. F. Cheng, K. C. Chiang, and A. Chin, "Bias-Temperature Instability on Fully-Silicided-Germanided Gates/high-K Al_2O_3 CMOSFETs," *J. Electrochem. Soc.* 151, pp., 2005. (accepted)

[3]. C. L. Sun, S. Y. Chen, **C. C. Liao**, and A. Chin, "Low Voltage Lead Titanate/Si One-Transistor Ferroelectric Memory with Good Device Characteristics," *Appl. Phys. Lett.*, vol. 85, no. 20, pp. 4726-4728, Nov. 2004.

[4]. **C. C. Liao**, C. F. Cheng, D. S. Yu and Albert Chin, "The copper contamination effect on Al_2O_3 gate dielectric on Si," *J. Electrochem. Soc.* 151, pp. G693-G696, Oct. 2004. (accepted)

[5]. **C. C. Liao**, A. Chin, and C. Tsai, "Electrical Characterization of Al_2O_3 on Si from MBE-grown AlAs and Al," *J. Crystal Growth*, 201/202, 652, 1999 (special issue of Intl. MBE Conference).

[6]. A. Chin, **C. C. Liao**, and C. Tsai, "$In_{0.52}Al_{0.48}As/InAs/In_xAl_{1-x}As$ Pseudomorphic HEMT's on InP," *IEEE Electron Device Lett.* 18, pp. 157, 1997

[7]. A. Chin, **C. C. Liao**, J. Chu, and S. S. Li, "Investigation of Si-doped p-type AlGaAs/GaAs, AlGaAs/InGaAs quantum well infrared photodetectors and multi-quantum wells grown on (311)A GaAs," *J. Crystal Growth* 176, pp. 999, 1997.

(B). International Conference:

[1]. **C. C. Laio**, D. S. Yu, K. C. Chiang, C. F. Cheng, Albert Chin, W. J. Chen, C. Zhu, M.-F. Li, W. J. Yoo, and D. L. Kwong "BIAS-TEMPERATURE INSTABILITY OF DUAL METAL-GATES/HIGH- CMOSFETS" VLSI-TSA Symposium, 2005. (submitted)

[2]. D. S. Yu, Albert Chin, **C. C. Laio**, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with Novel IrO_2(Hf) Dual Gates and High-κ Dielectric on 1P6M-0.18μm-CMOS," *International Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 181-184, San Francisco, Dec. 2004.

[3]. Albert Chin, D. S. Yu, **C. C. Laio**, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, Y. C. Yeo, W. J. Yoo, and D. L. Kwong, "New VLSI Architecture- High Mobility Metal-Gate/High-κ GOI CMOSFETs and High RF Performance Passive Devices on Si," *3rd International Workshop on New Group IV Semiconductors*, Sendai, Japan, Oct. 12-13, 2004. (Invited)

[4]. A. Chin, H. L. Kao, D. S. Yu, **C. C. Liao**, C. Zhu, M.-F. Li, S. Zhu and Dim-Lee Kwong, "High Performance Metal-Gate/High-κ MOSFETs and GaAs Compatible RF Passive Devices on Ge-On-Insulator Technology" *7th Int'l Conf. on Solid-State and Integrated- Circuit Technology (ICSICT)*, October 18-21, 2004. (Invited).

[5]. **C. C. Liao**, Z. M. Lai, C. F. Lee, J. T. Lin, D. S. Yu and Albert Chin, "Modeling RF Noise of Multi-Fingers 0.18 μm node MOSFETs," *Electrochemical Society (ECS) Intl Semiconductor Technology Conf.*, 2004.

[6]. A. Chin, Y. H. Wu, S. B. Chen, **C. C. Liao**, and W. J. Chen, "High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with Equivalent Oxide Thickness 5-10Å," *Symp. on*

VLSI Technology, pp. 16-17, US, June 2000. (Highlight Section Paper).

[7]. A. Chin, **C. C. Liao**, C. H. Lu, W. J. Chen, and C. Tsai, “Device and Reliability of High-K Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it},” *Symp. on VLSI Technology*, p.133-134, Japan, June 1999.

[8]. **C. C. Liao**, W. J. Chen, C. H. Lu, A. Chin and C. Tsai, “Electrical properties of Al_2O_3 gate dielectric,” *41th Electronic Materials Conference (EMC),* Santa Barbara, CA, June 1999.

[9]. **C. C. Liao**, A. Chin, and C. Tsai, “Electrical Characterization of Al_2O_3 on Si from MBE-grown AlAs and Al ,” *10th International Conference on Molecular Beam Epitaxy (MBE),* Cannes, France, August 1998.

[10]. I. J. Hsieh, **C. C. Liao**, C. Tsai, and A. Chin, “From Strain-Compensated $In_{0.80}Ga_{0.20}As$ /InAlAs to InAs/InAlAs HEMT’s,” *30th Solid State Devices and Materials (SSDM)*, Hiroshima, Japan, Sept. 1998.