國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

適用於高低壓共容輸入輸出介面之積體電路靜電放電防護設計

ESD PROTECTION DESIGNS FOR MIXED-VOLTAGE I/O INTERFACES IN CMOS INTEGRATED CIRCUITS

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中華民國 九十四年一月

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摘要

適用於高低壓共容輸入輸出介面(Mixed-Voltage I/O Interfaces)或具有省電模式(Power-Down-Mode)功能之互補式金氧半積體電路(CMOS ICs)將使得靜電放電(Electrostatic Discharge, ESD)防護設計有更多的限制與困難。適用於高低壓共容輸入輸出介面之積體電路，靜電放電防護設計必需考慮在電路正常操作下，閘極氧化層(Gate Oxide)的可靠度問題與避免額外的漏電流路徑；而具有省電模式功能之積體電路，靜電放電防護設計必需考慮在省電模式操作下，避免額外的漏電流路徑與內部電路誤動作的發生。在靜電放電發生時，靜電放電防護電路必需能夠有效地保護內部電路防止內部電路受到損傷。此外，在高壓互補式金氧半製程技術中，靜電放電防護元件的低持有電壓(Holding Voltage)特性將使得高壓積體電路發生閉鎖效應(Latchup)或類似閉鎖效應(Latchup-Like)的危險。此問題將使得高壓積體電路之靜電放電防護設計更加困難。另一方面，在奈米互補式金氧半製程技術中，如何設計具較快導通速度且較小佈局面積的電源間靜電放電箝制電路(Power-Rail ESD Clamp Circuit)來保護超薄的閘極氧化層以應用在系統單晶片(SOC)將是個挑戰。本論文將針對高低壓共容輸入輸出介面、具有省電模式功能、高壓互補式金氧半製程技術、與奈米互補式金氧半製程技術之積體電路靜電放電防護設計上的限制與困難作討論，並進一步設計出有效的靜電放電防護電路在各相關應用之積體電路晶片。

為了提供有效的靜電放電防護於高低壓共容輸入輸出電路，本論文提出利用基體觸發(Substrate Triggered)技術來提昇堆疊電晶體(Stacked-NMOS)的靜電放電防護能力。利用基體觸發技術可使得堆疊電晶體的觸發電壓(Trigger Voltage)降低，如此更能有效地保護高低壓共容輸入輸出電路。這種利用基體觸發技術所設計靜電放電防護電路其製程步驟完全相容於一般互補式金氧半導體的製程，且不需要使用厚的閘極氧化層。適用於 2.5V/3.3V 共容高低壓輸入輸出電路的靜電放電防護電路已在 0.25 微米互補式金氧半製程中實際被製作與驗證。實驗結果顯示利用基體觸發技術所設計靜電放電防護電路可使得堆疊電晶體的觸發電壓從 8.5 V 降低到 5.3 V；而高低壓共容輸入輸出電路在 240 微米總寬度的堆疊電晶體條件下，其人體放電模式(Human-Body-Model, HBM)的靜電放電耐受能力可以從原來的 3.4 kV 提昇到 5.6 kV。

為了提供有效的靜電放電防護於具有省電模式功能之積體電路晶片，本論文提出新型的靜電放電防護電路架構。此靜電放電防護電路架構包括一靜電放電匯流排(ESD Bus)與數個二極體(Diode)，使得積體電路進入省電模式操作下，可避免從輸入輸出焊墊(I/O Pad)到 VDD 電源線間的漏電流路徑及內部電路誤動作的發生。當積體電路在正常操作下，此設計具有極低的漏電流且不會影響到內部電路的正常工作。在此靜電放電防護電路架構中，VDD 到 VSS 電源間以及靜電放電匯流排到 VSS 電源間，各有一組靜電放電箝制電路以達到全晶片靜電放電防護設計的目的。在 0.35 微米互補式金氧半製程中，此設計可達到 7.5 kV 的人體放電模式靜電放電耐受能力。此外，在此靜電放電防護電路架構中，本論文也提出了改善輸出端電壓準位的電路，使得內部電路在正常操作下輸出端的最高電壓可以達到 VDD 的電壓準位。

在高壓互補式金氧半製程技術中，金氧半場效電晶體(MOSFET)、矽控整流器(SCR)或者是雙載子電晶體(BJT)，被廣泛的用作靜電放電防護元件。但是這些靜電放電防護元件在驟回崩潰(Snapback Breakdown)狀態下的持有電壓都遠小於高壓 Vcc 電源的電壓。此低持有電壓的元件特性將使得在實際系統應用下，高壓積體電路發生閉鎖效應或類似閉鎖效應的危

險，尤其是將這些元件用作電源間靜電放電箝制元件。本論文針對此問題作深入的研究，並進一步提出新型的電源間靜電放電箝制電路以避免高壓積體電路發生閉鎖效應或類似閉鎖效應的危險。此設計是藉由調整堆疊元件的數目，使得堆疊元件結構在驟迴崩潰狀態下的箝制電壓超過高壓 Vcc 電源的電壓。如此，在不需要增加或改變製程步驟下，便可以達到避免高壓積體電路發生閉鎖效應或類似閉鎖效應的目的。利用此概念設計的堆疊場氧化層電晶體結構(Stacked Field-Oxide Structure)用在電源間靜電放電箝制電路已經在供應電壓為 40 V 的 0.25 微米互補式金氧半製程中驗證，其能有效地防止高壓積體電路發生閉鎖效應或類似閉鎖效應的危險。

為了在奈米金氧半製程技術中實現具較高靜電放電耐受能力且較小佈局面積的輸入輸出單元(I/O Cell)，本論文在 0.13 微米互補式金氧半製程中，提出使用電源間寄生矽控整流器來作為電源間靜電放電箝制元件的輸入輸出單元。本論文共提出兩種寄生矽控整流器結構，其在電路正常操作下並沒有閉鎖效應的問題。在佈局上，此寄生矽控整流器結構是放置於輸入輸出單元的輸入(或輸出)P 型電晶體與 N 型電晶體之間。此外，寄生矽控整流器的導通速度可經由基體觸發技術而明顯的提昇。在 0.13 微米互補式金氧半製程中，此設計可達到 5 kV 的人體放電模式靜電放電耐受能力。此設計讓每個輸入輸出單元都具有一個快導通速度且高靜電放電耐受能力的電源間靜電放電箝制元件，因此在單一的輸入輸出單元便可以提供全晶片靜電放電防護所需之放電路徑。利用此設計，晶片可在較小的佈局面積下具有更高的靜電放電耐受能力。

在本博士論文中，已經針對高低壓共容輸入輸出介面、具有省電模式功能、高壓互補式金氧半製程技術、與奈米互補式金氧半製程技術等應用之積體電路設計出高效能的靜電放電防護電路。所設計的靜電放電防護電路均已在實際晶片上成功驗證，並有相對應的國際期刊論文發表與專利申請。

ESD PROTECTION DESIGNS FOR MIXED-VOLTAGE I/O INTERFACES IN CMOS INTEGRATED CIRCUITS

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ABSTRACT

For the CMOS integrated circuits (ICs) with the mixed-voltage I/O interfaces or power-down-mode application, the on-chip electrostatic discharge (ESD) protection circuits will meet more design constraints and difficulties. The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths during normal circuit operating operation, whereas that for IC with power-down-mode operation should avoid the undesired leakage current paths and malfunction during power-down-mode operation. During ESD stress condition, the on-chip ESD protection circuit should provide effective ESD protection for the internal circuits. In high-voltage CMOS technology, the low-holding-voltage characteristic of ESD protection devices has been found to cause the high-voltage CMOS ICs susceptible to latchup or latchup-like danger during normal circuit operating condition. How to avoid the latchup or latchup-like failure in high-voltage CMOS ICs will be an important challenge to on-chip ESD protection design for high-voltage CMOS IC products. In nanoscale CMOS technology, how to realize the turn-on-efficient and area-efficient power-rail ESD clamp circuit to protect the ultra-thin gate oxide will be an important challenge to system-on-a-chip (SOC) applications with a much larger chip size. In this thesis, the ESD design constraints in mixed-voltage I/O interfaces, power-down-mode application, high-voltage CMOS technology, and nanoscale

CMOS technology are presented. Furthermore, the novel on-chip ESD protection circuits have been developed to overcome the design constraints in such applications.

To provide effective ESD protection in the mixed-voltage I/O interfaces, a new ESD protection design, by using the substrate-triggered stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs. The substrate-triggered technique is applied to reduce the trigger voltage of the stacked-nMOS device for ensuring effective ESD protection for the mixed-voltage I/O circuits. The proposed ESD protection circuit with the substrate-triggered technique is fully compatible to general CMOS process without causing the gate-oxide reliability problem. Without using the thick gate oxide, the new proposed design has been fabricated and verified for 2.5V/3.3V-tolerant mixed-voltage I/O circuit in a 0.25-μm salicided CMOS process. By using this substrate-triggered design, the trigger voltage of the stacked-nMOS device can be reduced from the original 8.5V to become 5.3V to ensure effective protection for the mixed-voltage I/O circuits. The human-body-model (HBM) ESD level of the mixed-voltage I/O buffer with a stacked-nMOS of 240-μm channel width can be improved from the original 3.4 kV up to 5.6 kV by this substrate-triggered circuit.

To provide effective ESD protection for power-down-mode application, a new design on the ESD protection schemes for CMOS IC operating in power-down-mode condition is proposed. By using an additional ESD bus and diodes, the new proposed ESD protection schemes can block the leakage current from I/O pad to VDD power line to avoid malfunction during power-down-mode operating condition. During normal circuit operating condition, the new proposed ESD protection schemes have no leakage path to interfere with the normal circuit functions. The whole-chip ESD protection design can be achieved by insertion of ESD clamp circuits between VSS power line and both VDD power line and VDD ESD bus line. Experimental results have verified that the HBM ESD level of the new schemes can be greater than 7.5kV in a 0.35-μm silicided CMOS process. Furthermore, the output signal of the proposed ESD protection schemes can be successfully pulled up to VDD again by the output-swing improvement circuit under normal circuit operating condition.

In high-voltage CMOS technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, and bipolar junction transistors have been widely used as on-chip ESD protection devices. The double snapback characteristic in the high-voltage nMOSFETs has been investigated and analyzed by both measured and simulation results. Furthermore, the holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the high-voltage power supply voltage. Such characteristics will

cause the high-voltage CMOS ICs susceptible to the latchup or latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuits between the high-voltage power lines. In this thesis, the latchup or latchup-like issues in high-voltage CMOS ICs have been investigated in details. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the high-voltage supply voltage without using extra process modification in the high-voltage CMOS technology. A new latchup-free design on the high-voltage power-rail ESD clamp circuit with stacked field-oxide structure is proposed and successfully verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level. Therefore, latchup or latchup-like issues can be avoided by stacked field-oxide structures for the IC applications with power supply of 40V.

In order to realize the high-ESD-robust and high-area-efficient I/O cells in nanoscale CMOS technology, a new ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in a 130-nm CMOS process is proposed. Two new embedded SCR structures without latchup danger are proposed to be placed between the input (or output) pMOS and nMOS devices of the I/O cells. Furthermore, the turn-on efficiency of embedded SCR can be significantly increased by substrate-triggered technique. Experimental results have verified that the HBM ESD level of this new proposed I/O cells can be greater than 5kV in a 130-nm fully salicided CMOS process. By including the efficient power-rail ESD clamp device into each I/O cell, whole-chip ESD protection scheme can be successfully achieved within a small silicon area of I/O cell. Such I/O cells are very suitable for SOC applications in nanoscale CMOS technology.

In summary, the novel ESD protection designs have been successfully developed for mixed-voltage I/O interfaces, power-down-mode application, high-voltage CMOS technology, and nanoscale CMOS technology with high ESD robustness. Each of the proposed ESD protection circuits has been practically verified in the silicon testchips.

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林　　昆　　賢
謹誌於竹塹交大
九十四年　一月

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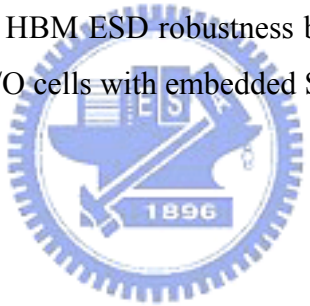

FIGURE CAPTIONS

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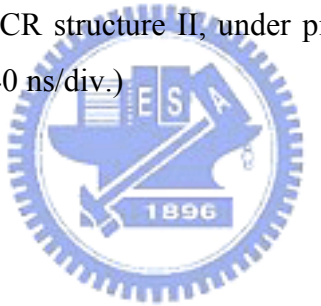


CHAPTER 1

INTRODUCTION

1.1 Background

Electrostatic Discharge (ESD) has become the main reliability concern on semiconductor products, especially for the system-on-a-chip (SOC) implementation in nanoscale CMOS processes. The ESD specifications of commercial IC products are generally required to be higher than 2kV in human-body-model (HBM) [1] ESD stress. Therefore, on-chip ESD protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS integrated circuits (ICs) [2]-[4]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Figs. 1.1(a) ~ 1.1(d), respectively. The typical design of on-chip ESD protection circuits in a CMOS IC is illustrated in Fig. 1.2. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [5]-[7], the turn-on-efficient power-rail ESD clamp circuit was placed between VDD and VSS power lines [8]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [8].

1.1.1 Issue of Mixed-Voltage I/O Interface

To improve circuit operating speed and performance, the device dimension of MOSFET has been shrunk in the advanced CMOS ICs. With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mix semiconductor chips fabricated in different CMOS technologies. Therefore, the microelectronic systems often require the interfaces between

semiconductor chips or sub-systems which have different internal power supply voltages. With the different power supply voltages in a microelectronic system, chip-to-chip I/O interface circuits must be designed to avoid electrical overstress across the gate oxide [9], to avoid hot-carrier degradation [10] on the output devices, and to prevent the undesired leakage current paths between the chips [11], [12]. For example, a 3.3-V I/O interface is generally required by the ICs realized in CMOS processes with the normal internal power-supply voltage of 2.5V or 1.8V. The traditional CMOS I/O buffer with VDD of 2.5V is shown in Fig. 1.3(a) with both output and input stages. When an external 3.3-V signal is applied to the I/O pad, the channel of the output pMOS and the parasitic drain-to-well junction diode in the output pMOS cause the leakage current paths from the I/O pad to VDD, as the dashed lines shown in Fig. 1.3(a). Moreover, the gate oxides of the output nMOS, the gate-grounded nMOS for input electrostatic discharge (ESD) protection, and the input inverter stage are over-stressed by the 3.3-V input signal to suffer the gate-oxide reliability issue. By using the additional thick gate-oxide process (or called as dual gate-oxide CMOS process [13], [14]), the gate-oxide reliability issue can be avoided. However, the process complexity and fabrication cost are increased.

To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-MOS configuration has been widely used in the mixed-voltage I/O circuits [15]-[21]. The typical 2.5V/3.3V-tolerant mixed-voltage I/O circuit is shown in Fig. 1.3(b) [16]. The independent control on the top and bottom gates of stacked-nMOS device allows the devices to meet reliability limitations during normal circuit operation. The gate of top nMOS in the stacked-nMOS device is biased at VDD (e.g. 2.5V in a 2.5V/3.3V mixed-voltage I/O interface). The gate of bottom nMOS is biased at VSS by the pre-driver circuit to avoid leakage current through the stacked-nMOS structure, when the I/O circuit has a high-voltage input signal. With a high-voltage input signal at the pad (e.g. 3.3V in a 2.5V/3.3V mixed-voltage I/O interface), the common node between the top nMOS and bottom nMOS in the stacked-nMOS structure has approximately a voltage level of VDD-Vth (~ 1.9V), where Vth (~ 0.6V) is the threshold voltage of nMOS device. Therefore, the stacked-nMOS can be operated within the safe range for both dielectric and hot-carrier reliability limitations. The pull-up pMOS, connected from the I/O pad to the VDD power line, has the gate tracking circuits for tracking the gate voltage and the n-well self-biased circuits for tracking n-well voltage, which are designed to ensure that the pull-up pMOS does not

conduct current when the 3.3-V input signals enter the I/O pad. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit is shown in Fig. 1.4(a), where a PS-mode ESD pulse is applied to the I/O pad. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD and the VDD-to-VSS ESD clamp circuit to ground. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to VDD power line in the mixed-voltage I/O circuits. Without the diode connected from the I/O pad to VDD in the mixed-voltage I/O circuits, the ESD current at I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to VDD power line, and cannot be discharged through the additional VDD-to-VSS ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. The ESD current path in the mixed-voltage I/O circuits with power-rail ESD clamp circuit under PS-mode ESD stress in illustrated in Fig. 1.4(b). Such ESD current at the I/O pad is mainly discharged through the stacked-nMOS by snapback breakdown. However, the nMOS in stacked configuration has a higher trigger voltage and a higher snapback holding voltage, but a lower secondary breakdown current (It2), as compared to that of the single nMOS [22], [23]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD level for under PS-mode ESD stress, as compared to the traditional I/O circuits with a single nMOS [22]. In addition, without the diode connected from the I/O pad to VDD, the mixed-voltage I/O circuit also has a lower ESD level for I/O pad under PD-mode ESD stress. The absence of the diode between I/O pad and VDD power line in the mixed-voltage I/O circuits will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses. By using extra process modification such as ESD implantation, the ESD robustness of stacked-nMOS device can be further improved [24], [25], but the process complexity and fabrication cost are increased. In addition, the induced high voltage on the gate of top nMOS transistor under ESD stress will cause high-current crowding effect in the channel region to seriously degrade ESD robustness of stacked-nMOS device in the mixed-voltage I/O circuits [26]. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes. In this thesis, the substrate-triggered stacked-nMOS device, which combines the substrate-triggered technique with the stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of

CMOS ICs [27].

1.1.2 Issue of Power-Down Application

Nowadays power-down-mode feature plays an important role in portable and mobile SOC products that require effective power saving. In order to achieve IC power-down-mode operation, modifications on I/O circuits and ESD protection circuits have been studied [12], [28]. An example of two chips connected in an electronic system is shown in Fig. 1.5, where the output pad (O/P) of the chip_1 is connected to the input pad (I/P) of the chip_2. When the chip_2 goes into the power-down-mode operation, two situations are explained as follows. First, if VDD2 power line is grounded, a large leakage current may be induced from the input pad to the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the voltage level at the output pin of chip_1 is high. Second, if the VDD2 power line is floating, the internal circuits of chip_2 may be triggered to cause malfunction by charging the VDD2 power line through the parasitic diode of pMOS connected between the input pad and VDD2 power line, when the voltage level at the output pin of chip_1 is high. Therefore, the parasitic diode of pMOS connected between the input pad and VDD2 power line must be removed to avoid leakage current or malfunction, when the chip_2 goes into the power-down-mode operation in this typical example. In the traditional I/O circuits, ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. However, the absence of the diode between I/O pad and VDD power line for power-down-mode application will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses. To solve the ESD protection and leakage issue for IC with power-down-mode operation, some modified designs have also been reported [29], [30]. The gate-grounded nMOS has been used to replace the diode between the I/O pad and VDD power line [29]. In [30], the design was focused on improving the ESD robustness of the ESD protection circuit between the I/O pad and VSS power line. However, the turn-on efficiency of the ESD protection device [29] or the complicated ESD protection circuit [30] is the concern to implement the approach. In this thesis, three new ESD protection designs for IC with power-down-mode operation [31]-[33] are proposed. The new proposed designs can overcome the leakage issue and have a very high ESD level for IC with power-down-mode operation.

1.1.3 Issue of High-Voltage CMOS ICs

High-voltage transistors in smart power technologies have been extensively used for display driver ICs, power supplies, power management, and automotive electronics. The ESD reliability is an important issue for high-voltage transistors with applications in these products. In smart power technology, high-voltage MOSFET, silicon-controlled rectifier (SCR) device, and bipolar junction transistor (BJT) have been used as on-chip ESD protection devices [34]-[39]. Those earlier works focused on analyzing and improving ESD robustness of the ESD protection devices in high-voltage CMOS processes [34]-[39]. However, the latchup or latchup-like failure from such ESD protection devices under normal circuit operating condition was not considered, especially while the devices are used in the power-rail ESD clamp circuit. Fig. 1.6 shows the typical ESD protection scheme for LCD driver ICs (typically, gate driver with 40V, and source driver with 12V, for 14.1-inch notebook LCD panel). The output buffers (Mp and Mn) are controlled by the input control circuits through the level-shifter circuits. The diodes D1~D4 are used as on-chip ESD protection devices for input and output pads. The ESD current at the output pad under positive-to-VSS ESD stress can be discharged through the diode D1 to the VDD_HV power line, and then through the power-rail ESD clamp circuit from the VDD_HV power line to the grounded VSS power line, as the dashed line shown in Fig. 1.6. When the ESD protection device is used in the power-rail ESD clamp circuit, the device is expected to be kept off in normal circuit operating condition. During ESD stress conditions, the ESD protection device should be triggered on to discharge ESD current. If the holding voltage of the ESD protection device in power-rail ESD clamp circuit is smaller than the power supply voltage, the ESD device may be triggered on by the system-level electromagnetic compatibility (EMC)/ESD transient pulses to cause a very serious “latchup” or “latchup-like” failure in CMOS ICs. This phenomenon often leads to IC function failure or even destruction by burning out [40], [41]. The system-level EMC/ESD reliability of LCD panel has been requested up to 20kV of ESD stress in the air-discharge mode. The system-level EMC/ESD test on LCD panel of notebook by an ESD gun (Standard IEC 61000-4-2 [42]) is shown in Fig. 1.7(a). During the system-level ESD stress, the power lines of driver ICs in the LCD panel of notebook can be coupled with an overshooting/undershooting voltage up to several hundred volts [43], as that shown in Fig. 1.7(b). Especially, the driver ICs with tape carrier package (TCP) are directly attached to the LCD panel. No room is available for the driver ICs with on-board de-coupling discrete components to shunt the ESD-zapping transient voltage away from the driver ICs. So,

the transient voltage seen by the circuits in the driver ICs is quite large during such system-level EMC/ESD zapping. In this thesis, the holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the power supply voltage [44]-[46]. Such characteristics will cause the high-voltage CMOS ICs susceptible to the latchup or latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuit. Furthermore, a new latchup-free power-rail ESD clamp circuit in high-voltage CMOS process [45], [46] is proposed in this thesis.

1.1.4 Issue of Nanoscale CMOS Technology

To provide efficient ESD protection for CMOS ICs, the on-chip ESD protection circuits have to be designed and placed around the input, output, and power pads. In Fig. 1.2, the pMOS and nMOS are used as on-chip ESD protection devices for input and output pads. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. However, due to the parasitic resistance and capacitance along the VDD and VSS power lines, ESD protection efficiency is dependent on the pin location in a chip. To quickly bypass the ESD current during ESD-stress condition, the efficient VDD-to-VSS ESD clamp circuits are repeatedly inserted between VDD and VSS power lines in the appropriate distance to provide a low-impedance path between the VDD and VSS power lines [8]. Therefore, how to realize the area-efficient and turn-on-efficient power-rail ESD clamp circuits will be an important challenge to SOC applications with a much larger chip size but a reduced cell pitch for I/O cell. For CMOS IC applications, SCR can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [47]-[50], which can even provide efficient ESD protection to the ultra-thin gate oxide in nanoscale CMOS process [51]. However, SCR device was susceptible to latchup danger under normal circuit operating condition [52]. Because of the low holding voltage, such SCR devices could be accidentally triggered on by the noise pulses, when ICs are in normal circuit operating conditions. In the traditional I/O cells, double guard rings have been often inserted between input (or output) pMOS and nMOS devices to avoid the latchup issue [53]. The layout view and device structures of the traditional I/O cell are shown in Figs. 1.8(a) and 1.8(b), respectively. However, with the scaled-down device dimension in nanoscale CMOS technology, the power

supply voltage is also scaled down to meet the circuit requirement and gate-oxide reliability. The maximum supply voltage is only 1.2V in a 130-nm CMOS technology with the thin gate oxide of 20Å. If the holding voltage of parasitic SCR device is greater than the power supply voltage, latchup issue will not occur in such nanoscale CMOS process. Therefore, the SCR or parasitic SCR device can be used as on-chip ESD protection device without latchup concern in nanoscale CMOS process. A new ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device is proposed for nanoscale CMOS process [54], [55] in this thesis. Whole-chip ESD protection scheme can be successfully achieved within a small silicon area of I/O cell by this design.

1.2 ESD Protection Designs for Mixed-Voltage I/O Interfaces

1.2.1 Substrate-Triggered Stacked-NMOS Device

To improve the turn-on uniformity among the multiple fingers of CMOS output buffer, the substrate-triggered designs [56]-[58] have been reported to increase ESD robustness of the large-device-dimension nMOS. With the substrate-triggered technique, the substrate-triggered stacked-nMOS device [27] for mixed-voltage I/O interfaces is proposed and verified in Chapter 2 in this thesis. The ESD robustness of mixed-voltage I/O circuits can be effectively improved by this design without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

1.2.2 Extra ESD Device between I/O pad and VSS

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VSS power line [59], [60]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be directly discharged through this additional ESD device to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through this ESD device to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD.

One ESD protection design with the additional substrate-triggered lateral n-p-n BJT device has been used to protect the mixed-voltage I/O circuits in a fully salicided, 0.35-μm, thin-epi CMOS process [59]. The ESD protection design with substrate-triggered circuit and

the lateral n-p-n BJT device for the mixed-voltage I/O circuits is re-drawn in Fig. 1.9(a). The substrate-triggered circuit should meet the design constraints for providing effective ESD protection to the mixed-voltage I/O circuits, but without suffering the gate-oxide reliability issue. In this design, the substrate-triggered circuit is mainly composed of the diode string and a pMOS Mp1 to provide the substrate current for triggering on the lateral n-p-n BJT during ESD stress. A positive feedback network is formed with Mp2, Mn1, and R1, which maintains Mp1 in a highly conductive state to provide the substrate current during ESD stress. Moreover, to improve the turn-on efficiency of lateral n-p-n BJT device in a thin-epi CMOS process with much smaller substrate resistance (Rsub), the device structure of lateral n-p-n BJT is specifically designed in Fig. 1.9(b). The lateral n-p-n BJT device consists of an n+ diffusion (emitter), an n-well (collector), and a p+ diffusion as its base. A dummy gate is formed between the p+ base and n+ emitter regions. The collector n-well encloses a portion of the p+ base region. In this design, the HBM ESD level of the mixed-voltage I/O circuits has been verified greater than 2kV in a fully-salicided thin-epi CMOS process.

Another ESD protection design, by using the additional stacked-nMOS triggered silicon controlled rectifier (SNTSCR), has been reported to protect the mixed-voltage I/O circuits [60]. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 1.10(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 1.10(b). The ESD detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the Mn3 in Fig. 1.10(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2 and Mn4. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the Mp1 is turned on but Mn3 is off since the initial voltage level on the floating VDD line is ~0V. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage of nMOS to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced,

so the SNTSCR can be quickly triggered on to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating n-well of the pull-up pMOS in the mixed-voltage I/O circuit, the SNTSCR device can have a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. From the experimental results in a 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8kV, as compared with that (~2kV) of the original mixed-voltage I/O circuits with only stacked nMOS device.

1.2.3 Extra ESD Device between I/O pad and VDD

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and VDD power line [61]-[63]. The ESD current at the I/O pad under PS-mode ESD stress is designed to be discharged through this additional ESD device to VDD power line, and then through the power-rail ESD clamp circuit to the grounded VSS. The ESD current at the I/O pad under the PD-mode ESD stress can be directly discharged through this additional ESD device to the grounded VDD.

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [61], [62], or used to realize the power-rail ESD clamp circuit [64]. The ESD protection design with the diode string connected between the I/O pad and VDD power line for the mixed-voltage I/O circuits is shown in Fig. 1.11. The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the VDD supply voltage. To reduce the turn-on resistance from I/O pad to VDD during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in the mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to VDD through the stacked diodes could trigger on the parasitic vertical p-n-p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p-n-p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 1.11, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [61], [62].

Another ESD protection design, by using the gated p-n-p BJT as the additional ESD

device connected between I/O pad and VDD, has been designed to protect the mixed-voltage I/O circuits [63], as that shown in Fig. 1.12. In this ESD protection design, the pMOS Mp1 acting as ESD clamp device should be kept off to avoid the leakage current path during normal circuit operating condition. Under PD-mode ESD stress condition, the parasitic lateral p-n-p BJT in the device structure of Mp1 is turned on to discharge ESD current. In the 3.6V/5V mixed-voltage IC application, when the input voltage at I/O pad is 0V, the n-well voltage and gate voltage of Mp1 is clamped at VDD (3.6V) through the turn-on of Mp2 and Mp4. When the input voltage at I/O pad is 5V, the n-well voltage of Mp1 is maintained at 5-Vd (where Vd is the cut-in voltage of the parasitic drain-to-well diode), and the gate voltage of Mp1 is clamped at 5V through the turn-on of Mp3. Therefore, this design can meet the gate-oxide reliability constraints without leakage current path from I/O pad to VDD during normal circuit operating condition. Under ESD stress condition, the parasitic lateral p-n-p BJT in Mp1 is turned on to discharge ESD current by avalanche breakdown. Such a gated p-n-p BJT should be designed to effectively clamp the overstress ESD pulse without causing ESD damage in the mixed-voltage I/O circuits.

1.2.4 ESD Protection Design with ESD Bus

The whole-chip ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application is proposed in Chapter 3 in this thesis [31]-[33]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 1.13. The additional ESD bus line is realized by a wide metal line in CMOS IC [65]. The ESD bus is not directly connected to an external power pin, but biased to VDD through the diode D1 in Fig. 1.13. The diode D1 connected between the VDD power line and ESD bus is also used to block the leakage current path from the I/O pad to VDD during normal circuit operating condition with a high-voltage input signal. The diode Dp is connected between I/O pad and ESD bus, whereas the diode Dn is connected between VSS power line and I/O pad. One (the first) power-rail ESD clamp circuit is connected between VDD power line and VSS power line. Another (the second) power-rail ESD clamp circuit is connected between the ESD bus and VSS power line. The second power-rail ESD clamp circuit connected between ESD bus and VSS power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode Dp to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded VSS.

The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode Dp to the ESD bus, the second power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded VDD. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus.

1.2.5 Special Applications

One of the mixed-voltage circuit applications, such as the interface in ADSL, has the input signals with voltage level higher than VDD and lower than VSS. This application limits the ESD diodes connected between the input pad and VDD/VSS power lines. To meet such mixed-voltage I/O interface, the SCR device with floating p-well structure in an n-substrate CMOS process has been used as on-chip ESD protection device [66]. However, the SCR device with a floating well structure is very sensitive to latchup [53], [67]. The mixed-voltage I/O interfaces in the system applications often meet serious overshooting or undershooting signal transition, which could trigger on the SCR device in the ESD protection circuit of I/O pad to induce latchup troubles to the chip [66]. A new ESD protection design, by using the low-voltage-triggered p-n-p (LVTPNP) device, has been proposed to protect such I/O interfaces with input voltage level higher than VDD and lower than VSS [68], as shown in Fig. 1.14. Comparing to the traditional p-n-p device in CMOS process, the LVTPNP device with a lower breakdown voltage by avalanche breakdown across the p+/n-well or n+/p-sub junctions provides effective discharging path to protect the mixed-voltage I/O interfaces against ESD stresses. During normal circuit operation condition, the LVTPNP device is kept off without causing any leakage current path. In cooperating with the power-rail ESD clamp circuit, the ESD current is discharged through the LVTPNP device by avalanche breakdown under four modes of ESD stresses. The ESD robustness of the LVTPNP device can be further improved by layout optimization.

For high-frequency and analog circuit applications, the high-voltage-tolerant ESD protection design should meet the constraint of low parasitic capacitance. The traditional analog ESD protection with double diodes connected between I/O pad and VDD/VSS power lines [69] cannot meet the high-voltage tolerant requirement. A high-voltage-tolerant ESD protection design, by using the forward-biased diode in series with the stacked-nMOS device, has been reported for analog ESD protection to reduce the input parasitic capacitance [70], as shown in Fig. 1.15. The equivalent capacitance of analog pin in this design is approximate the

junction capacitance of D1 plus the junction capacitance of D2. The diodes D1 and D2 can be drawn with small layout area, because the ESD current is discharged through these diodes under forward-biased condition. Therefore, the total parasitic input capacitance seen by the analog pin was reduced. The gates of Mn1 and Mn3 are connected to VDD to meet the gate-oxide reliability. The gates of Mn2 and Mn4 are grounded by the dynamic-floating-gate technique [71] to improve turn-on uniformity among the multiple fingers of the stacked nMOS device. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked nMOS (Mn3 and Mn4) to the grounded VSS. The ESD current at the I/O pad under PD-mode ESD stress can be discharged through the diode D1 and the parasitic n-p-n BJT of stacked nMOS (Mn1 and Mn2) to the grounded VDD. Because the ESD current is discharged through the stacked-nMOS device by snapback breakdown in this design, the turn-on efficiency and ESD robustness of stacked-nMOS devices (Mn1 ~ Mn4) need to be further improved by the additional ESD-implantation process [72].

1.3 Thesis Organization

To overcome the ESD design constraints in mixed-voltage I/O interfaces, power-down-mode application, high-voltage CMOS process, and nanoscale CMOS technology, the novel on-chip ESD protection circuits are developed and verified in this thesis. This thesis contains six chapters. Chapter 1 presents an overview on the design concept and circuit implementations of the ESD protection designs for mixed-voltage I/O interfaces without using the additional thick gate-oxide process. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and needs to prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current.

In chapter 2, the substrate-triggered stacked-nMOS device, which combines the substrate-triggered technique with the stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs. The proposed ESD protection circuit with the

substrate-triggered technique is fully compatible to general CMOS process without causing the gate-oxide reliability problem. Without using the thick gate oxide, the new proposed design has been fabricated and verified for 2.5V/3.3V tolerant mixed-voltage I/O circuit in a 0.25-μm salicided CMOS process. The HBM ESD level of the mixed-voltage I/O buffer can be improved from the original 3.4kV up to 5.6kV by the substrate-triggered circuit. By using this substrate-triggered design, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells.

In chapter 3, three new ESD protection designs for CMOS IC with power-down-mode operation are proposed. By using the additional ESD bus and diodes, the ESD protection design can block the leakage current from I/O pin to VDD and avoid the malfunction during power-down-mode operating condition. During normal circuit operating condition, the ESD protection design has no leakage path to interfere with the normal circuit functions. The whole-chip ESD protection design can be achieved by insertion of ESD clamp circuits between VSS power line and both VDD power line and ESD bus. Experimental results have verified that the HBM ESD level of the new proposed designs can be greater than 7.5kV in a 0.35-μm silicided CMOS process. Furthermore, output-swing improvement circuit is proposed to achieve the full swing of output voltage level during normal circuit operating condition.

In chapter 4, the double snapback characteristic in the high-voltage nMOSFETs has been found and analyzed. Furthermore, the holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristic will cause the high-voltage CMOS ICs susceptible to the latchup or latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuit. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and successfully verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level. The total holding voltage of the stacked-field-oxide structure in snapback breakdown condition can be larger than the power supply voltage. Therefore, latchup or latchup-like issues can be avoided by stacked-field-oxide structures for the IC applications with power supply of 40V.

In chapter 5, a new ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in a 130-nm CMOS process is proposed. Two new embedded SCR structures without latchup danger are proposed to be placed between the input (or output)

pMOS and nMOS devices of the I/O cells. Furthermore, the turn-on efficiency of embedded SCR can be significantly increased by substrate-triggered technique. Experimental results have verified that the HBM ESD level of this new proposed I/O cells can be greater than 5kV in a 130-nm fully salicided CMOS process. By including the efficient power-rail ESD clamp device into each I/O cell, whole-chip ESD protection scheme can be successfully achieved within a small silicon area of I/O cell.

Finally, the main results of this thesis are summarized in chapter 6. Some suggestions for the future works are also addressed in this chapter.

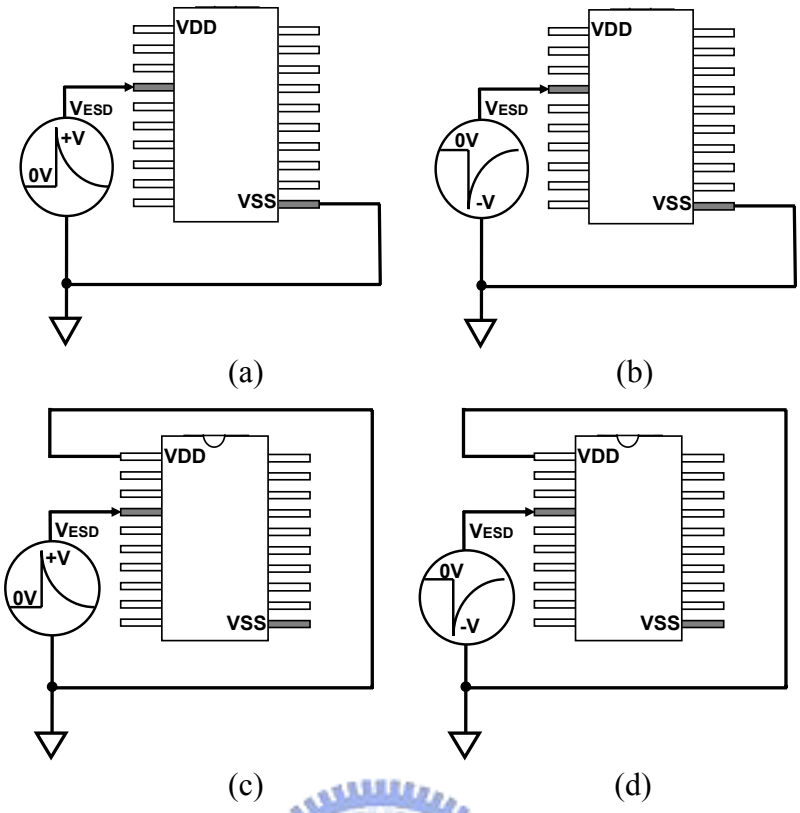


Fig. 1.1 The four pin-combination modes for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

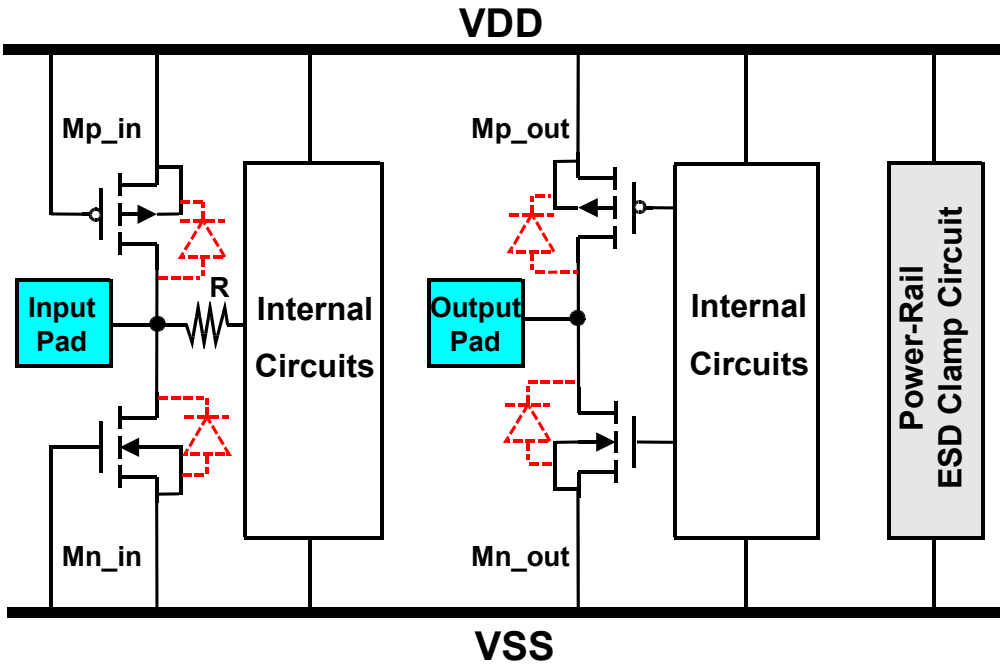
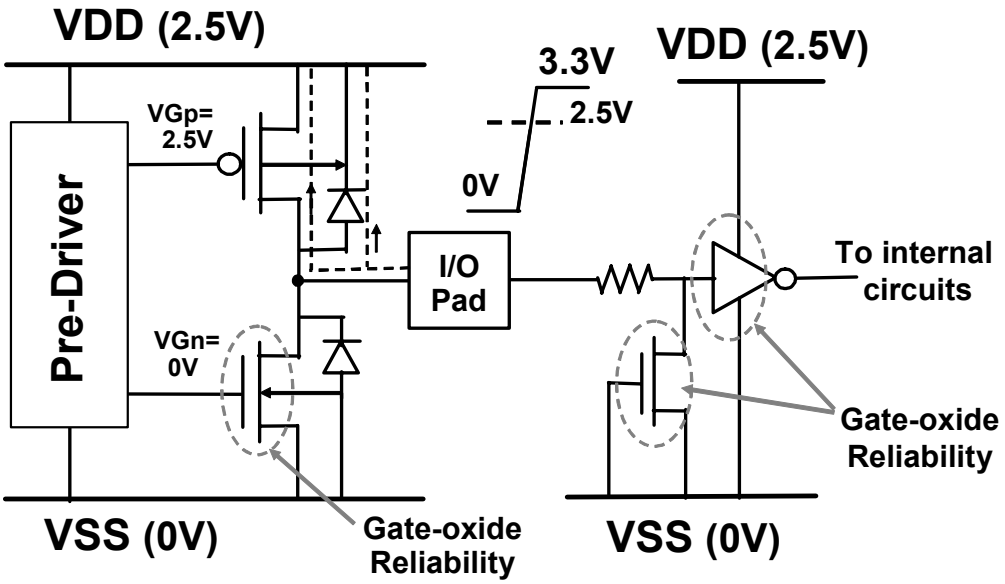
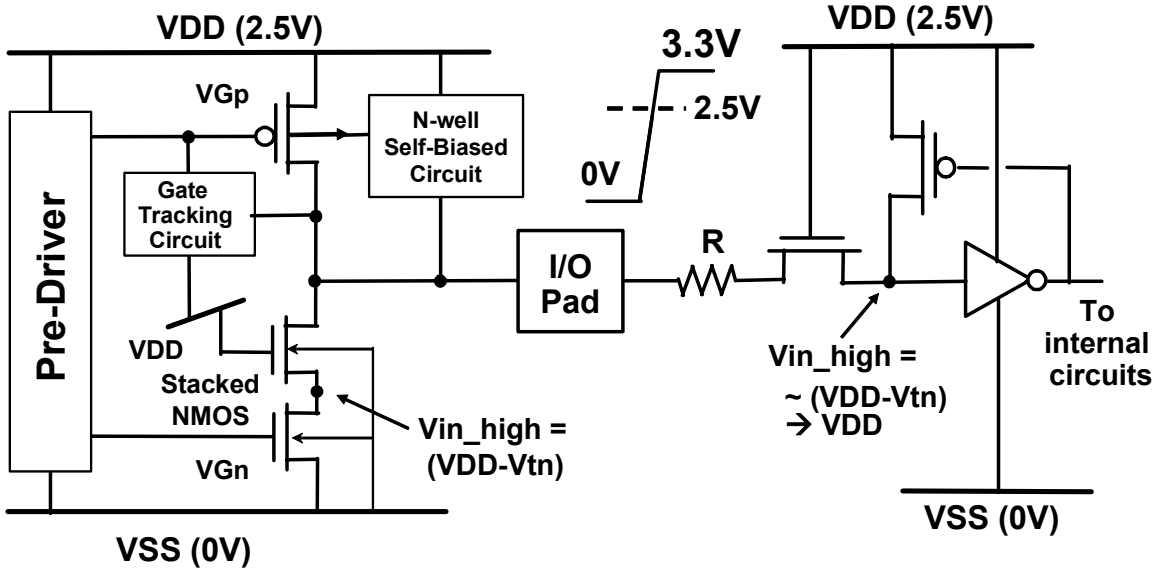


Fig. 1.2 Typical on-chip ESD protection circuits in a CMOS IC.

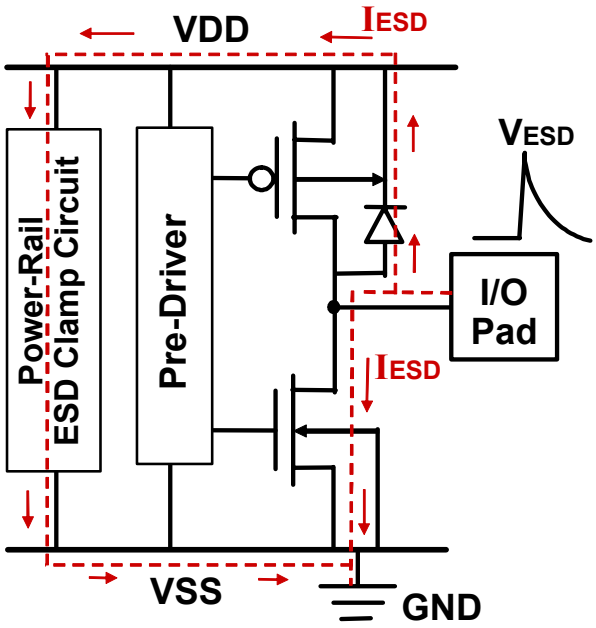


(a)

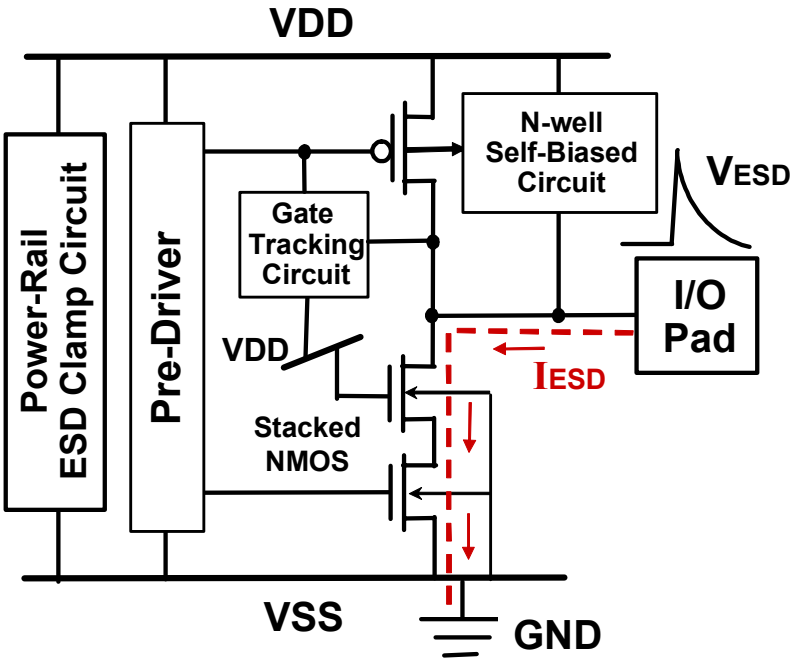


(b)

Fig. 1.3 Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-nMOS and the N-well self-biased pMOS.



(a)



(b)

Fig. 1.4 The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

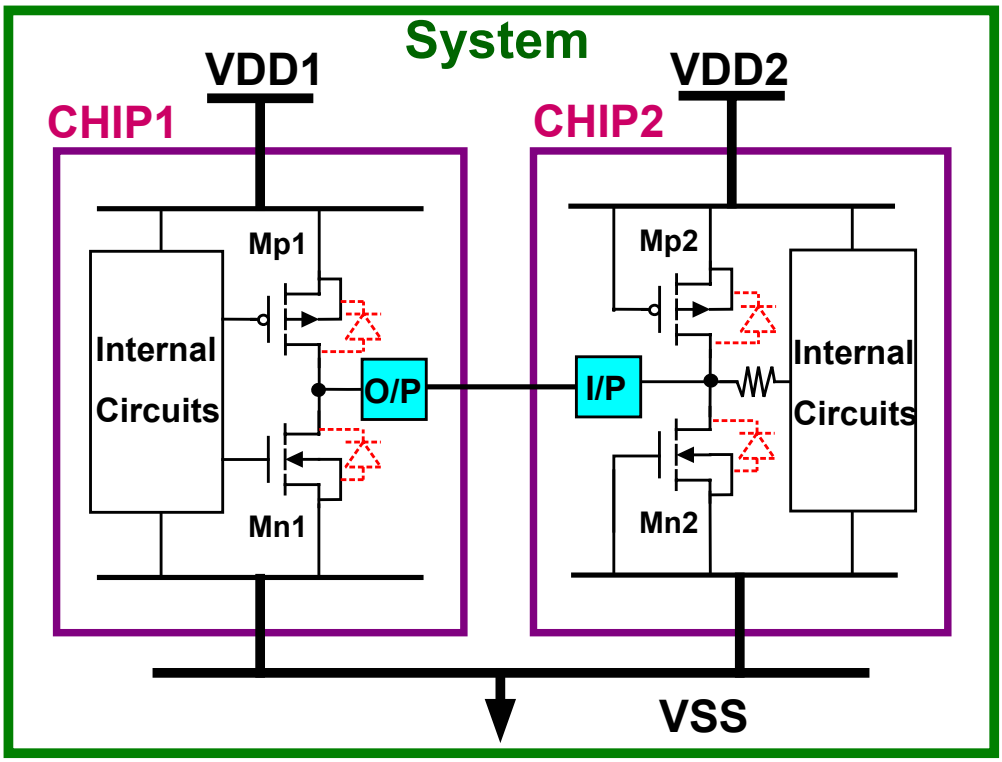


Fig. 1.5 An example to show the power-down-mode operation issue on a system with two chips, which are biased with separated VDD1 and VDD2 power supplies.

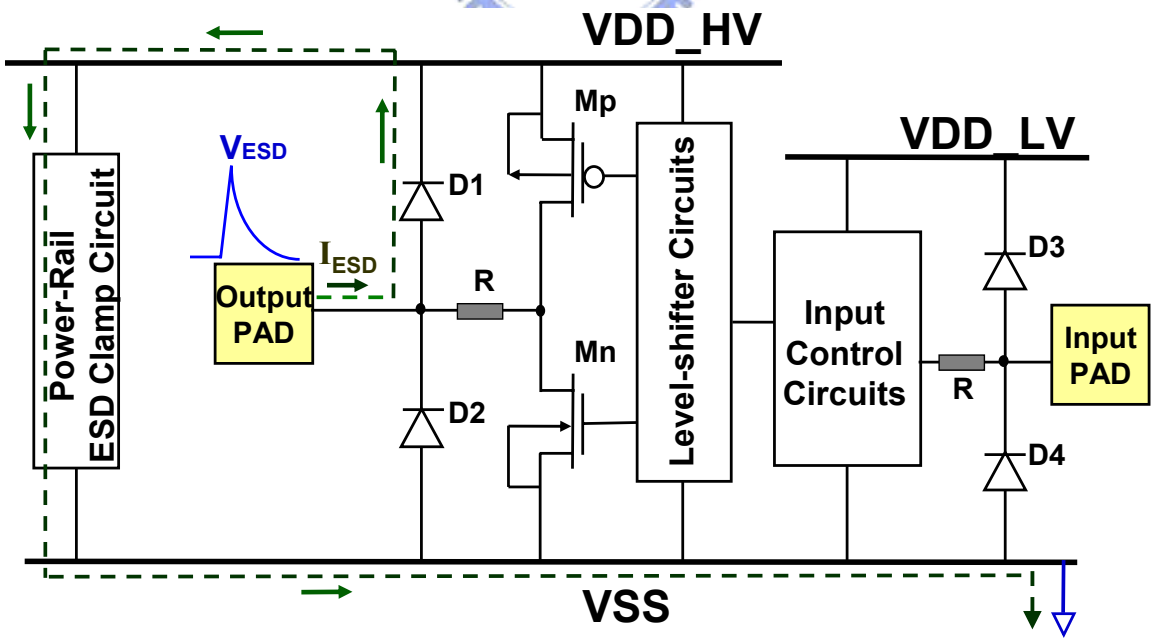
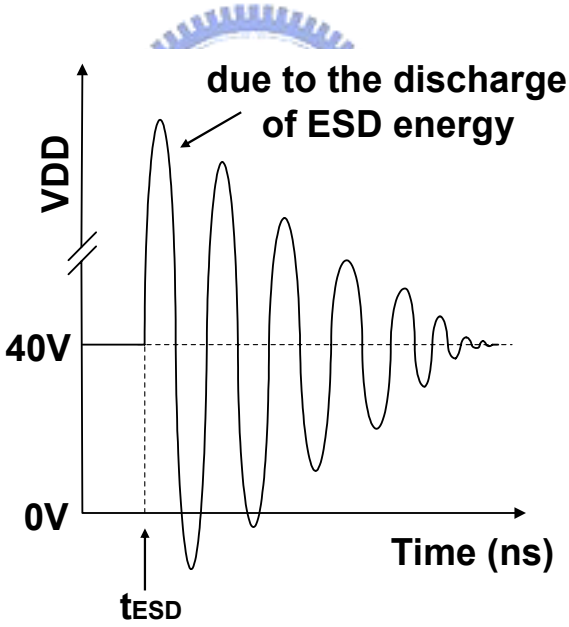


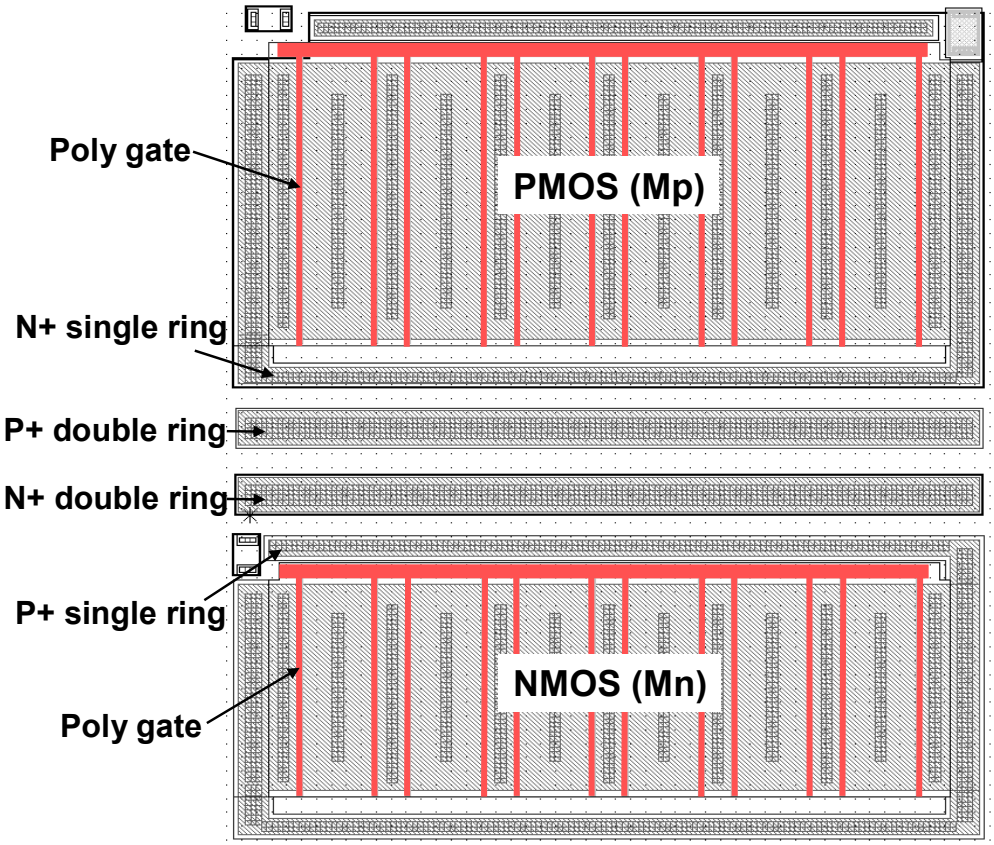
Fig. 1.6 The typical ESD protection scheme for LCD driver ICs.

(a)

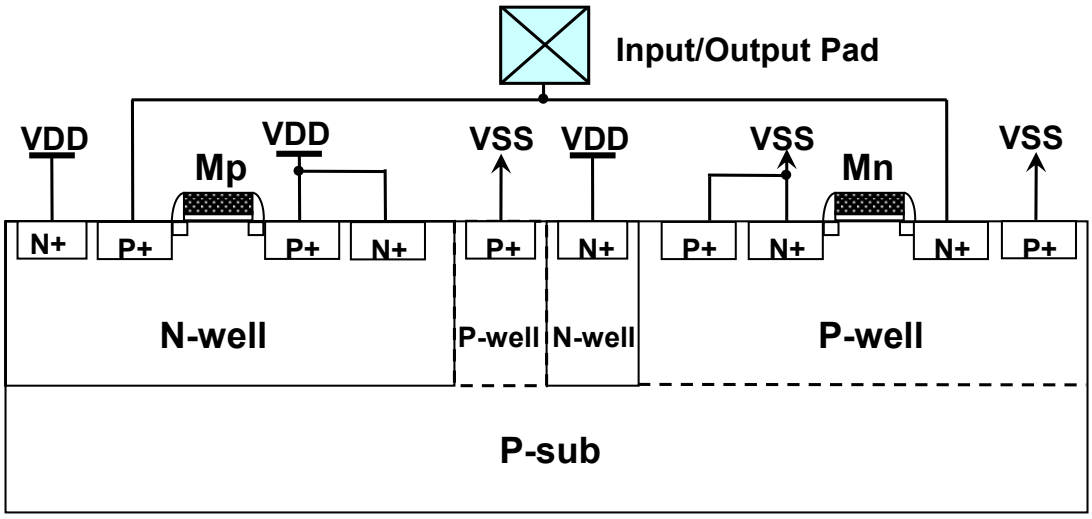


(b)

Fig. 1.7 (a) The system-level EMC/ESD test on LCD panel of notebook by an ESD gun. (b) The transient overshooting/ undershooting voltage waveform on the VDD pin of the driver ICs during system-level EMC/ESD test.

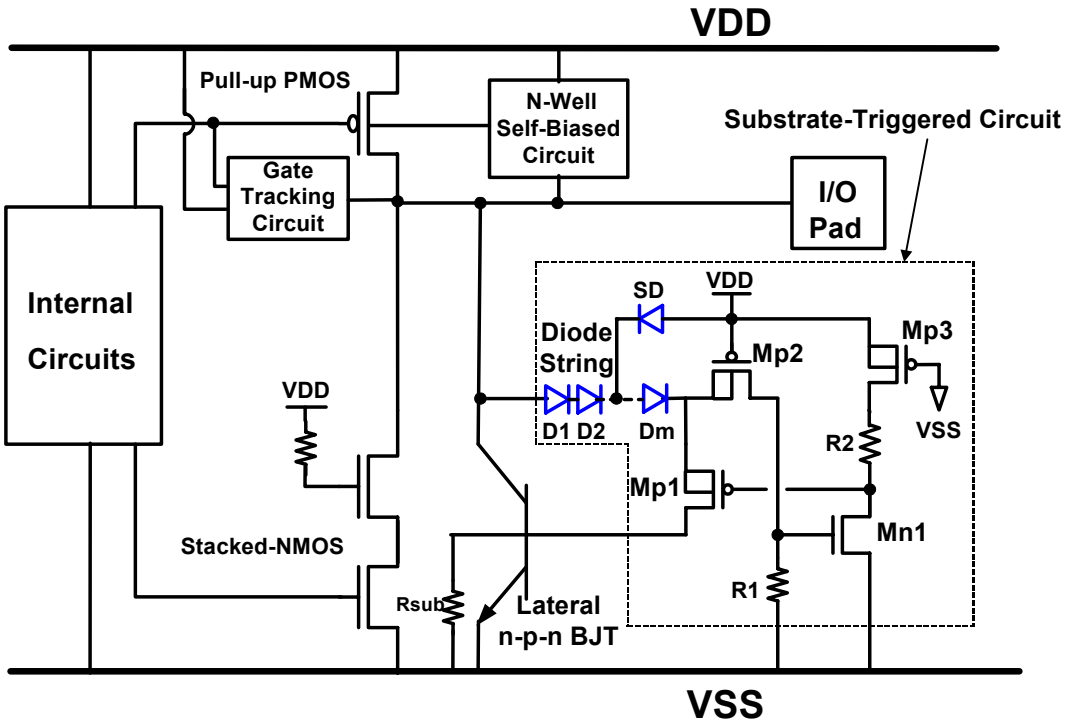


(a)

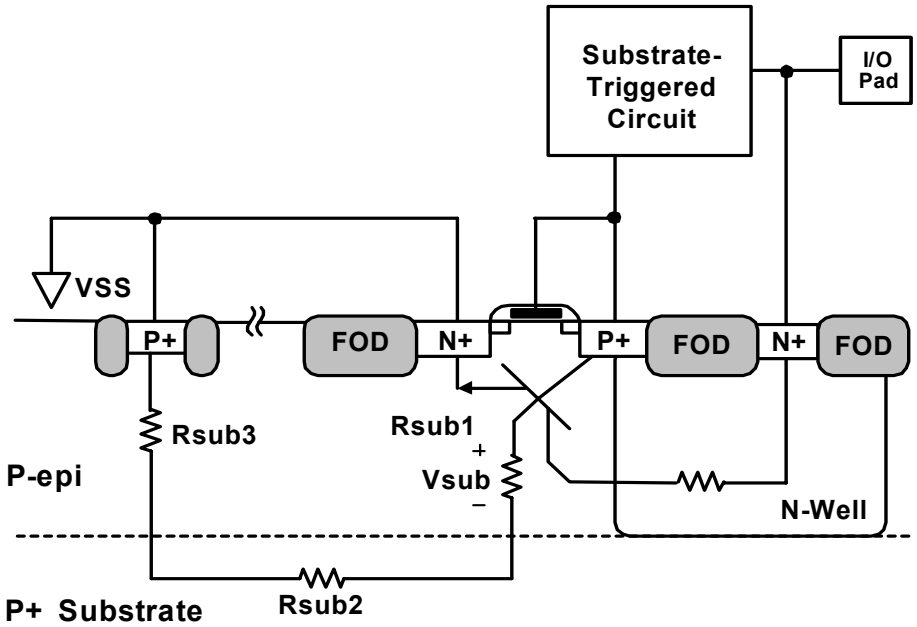


(b)

Fig. 1.8 (a) Layout view and (b) device structures of the traditional I/O cell with double guard rings inserted between input (or output) pMOS and nMOS devices.

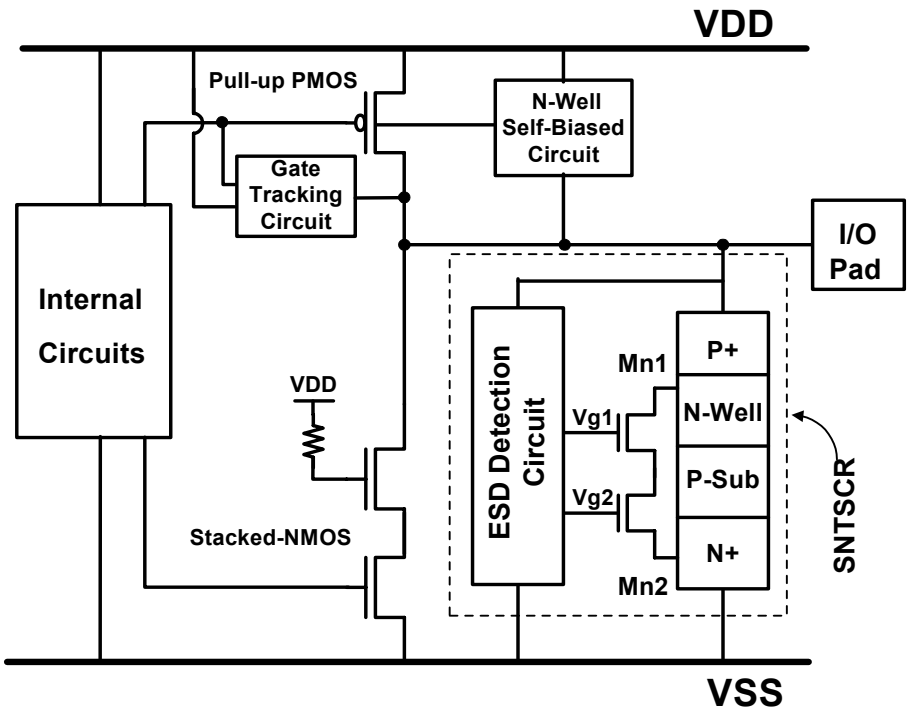


(a)

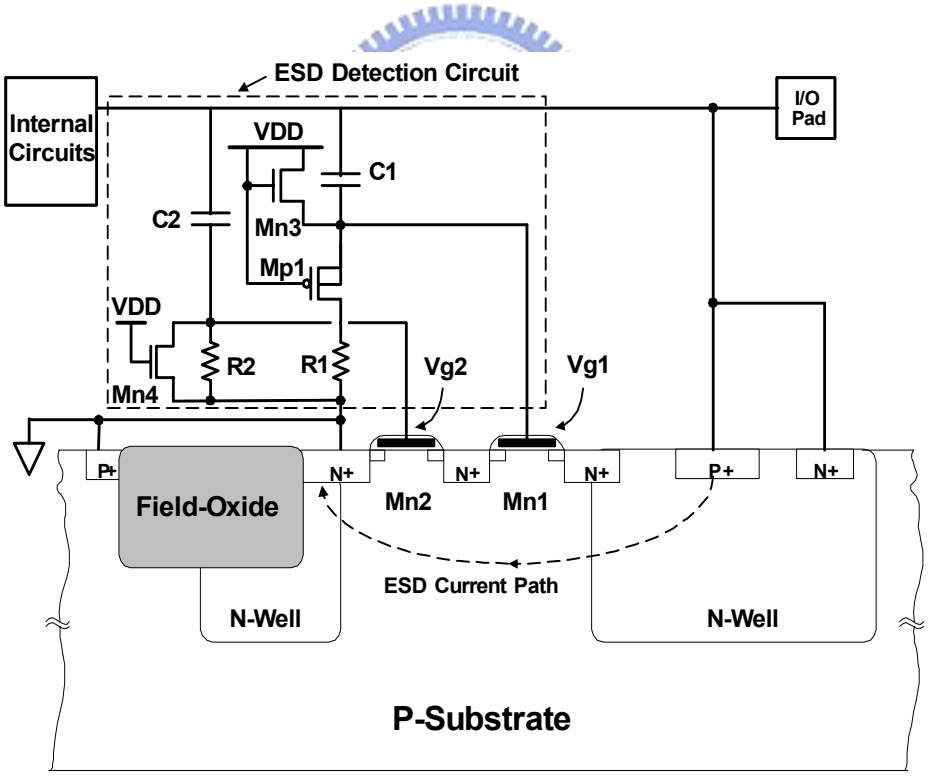


(b)

Fig. 1.9 (a) ESD protection design with substrate-triggered lateral n-p-n BJT device to protect the mixed-voltage I/O circuits. (b) Cross-sectional view of the lateral n-p-n BJT device in a thin-epi CMOS process.



(a)



(b)

Fig. 1.10 (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

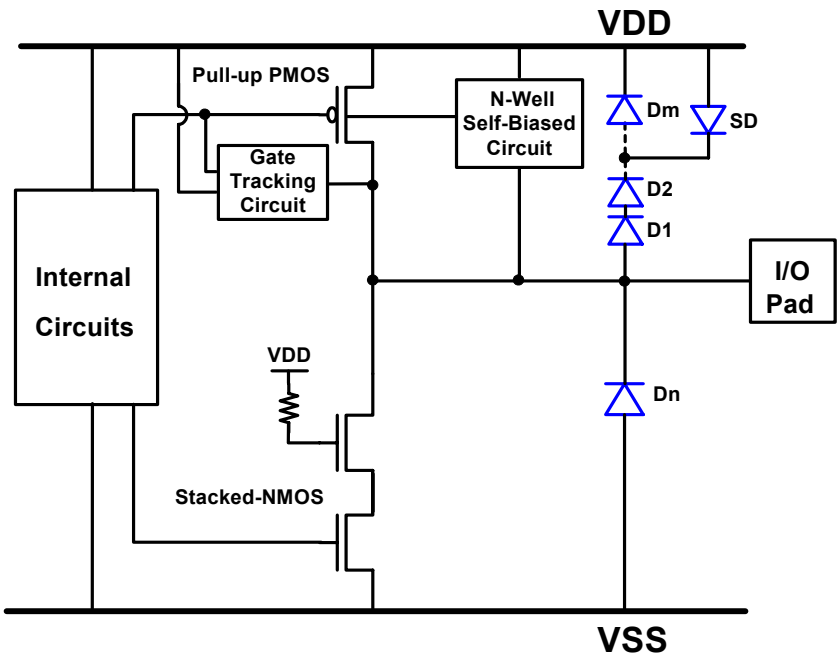


Fig. 1.11 ESD protection design with the diode string connected between the I/O pad and VDD power line to protect the mixed-voltage I/O circuits. An additional snubber diode (SD) is used to reduce the leakage current of the diode string due to the Darlington amplification.

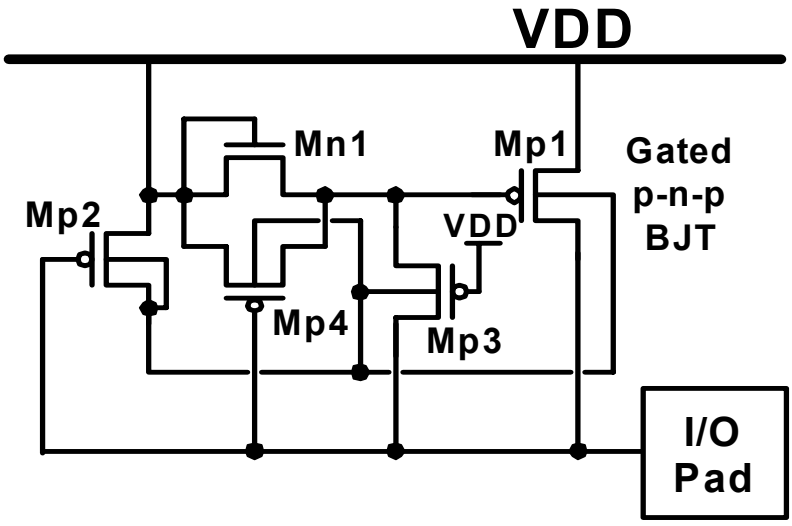


Fig. 1.12 ESD protection design with gated p-n-p BJT as the ESD clamp device connected between I/O pad and VDD to protect the mixed-voltage I/O circuits.

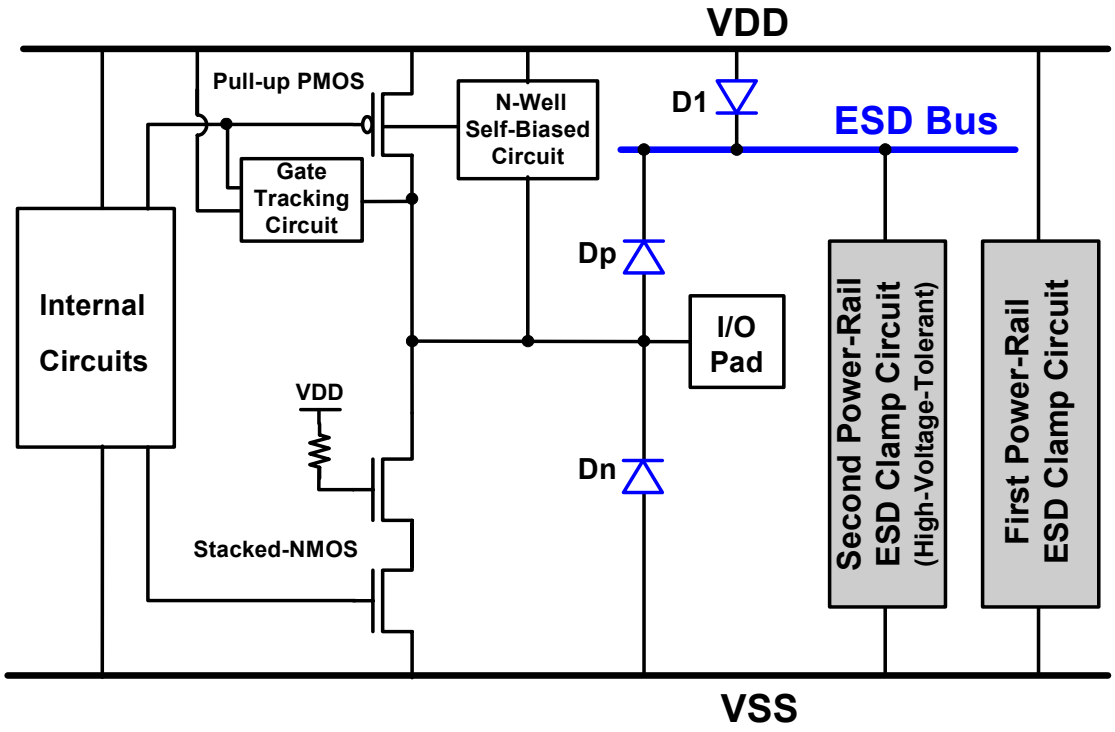


Fig. 1.13 The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between ESD bus line and VSS power line.

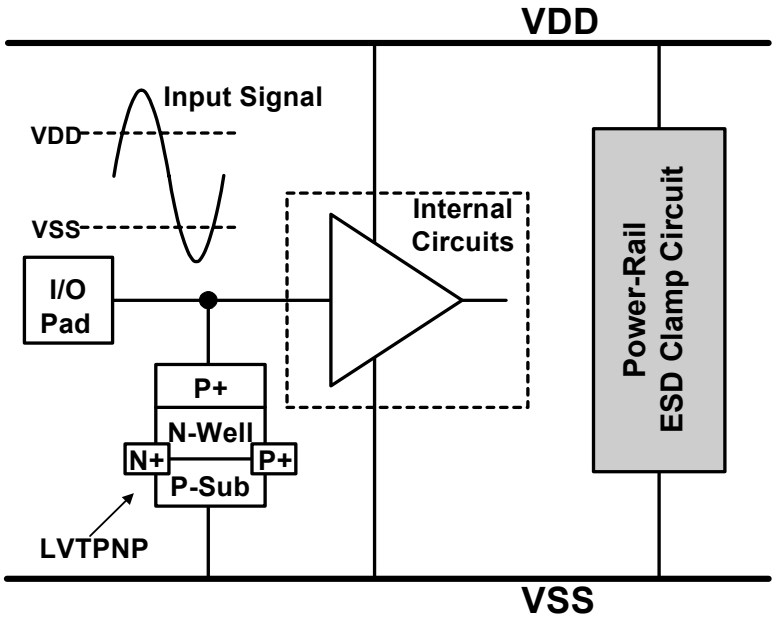


Fig. 1.14 ESD protection design with low-voltage-triggered p-n-p (LVTPNP) device for the I/O interfaces with input voltage level higher than VDD or lower than VSS.

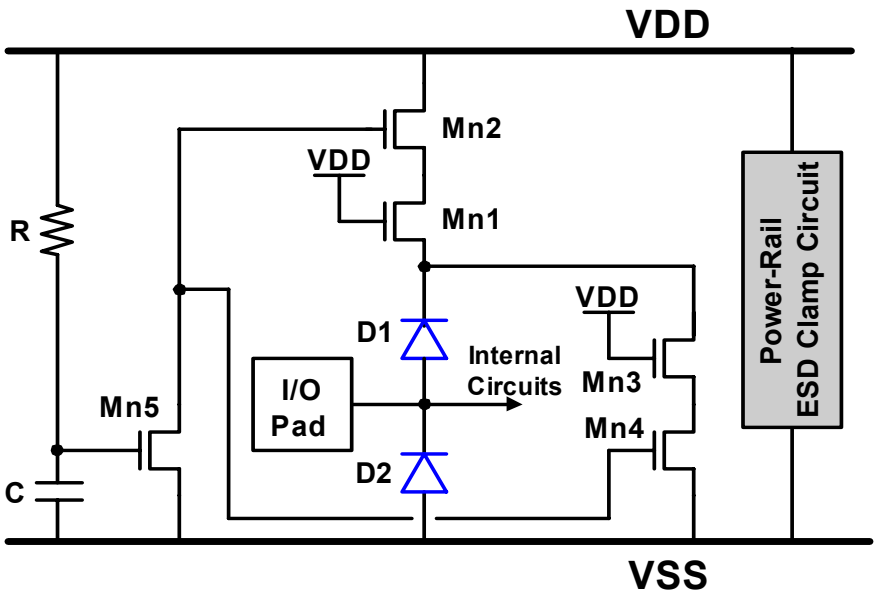


Fig. 1.15 High-voltage-tolerant ESD protection design with the forward-biased diode in series with one stacked nMOS for analog ESD protection to reduce the input parasitic capacitance.

CHAPTER 2

ESD PROTECTION DESIGN FOR MIXED-VOLTAGE I/O CIRCUITS

In this chapter, a new ESD protection design, by using the substrate-triggered stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs. The substrate-triggered technique is applied to lower the trigger voltage of the stacked-nMOS device to ensure effective ESD protection for the mixed-voltage I/O circuits. The substrate-triggered circuit for providing the trigger current should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough current to effectively improve the turn-on efficiency of parasitic n-p-n BJT in stacked-nMOS device. The substrate-triggered circuit should meet above constraints for providing effective ESD protection to the mixed-voltage I/O interfaces. By using this substrate-triggered design, the gates of stacked-nMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n-p-n BJT in the stacked-nMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the I/O cells. Without using the thick gate oxide, this new design has been fabricated and verified for 2.5V/3.3V tolerant mixed-voltage I/O circuit in a 0.25-μm salicided CMOS process [31].

2.1 Stacked-NMOS Device

The finger-type layout pattern and the corresponding cross-sectional view of stacked-nMOS device in mixed-voltage I/O circuits are shown in Figs. 2.1(a) and 2.1(b), respectively. The stacked-nMOS device can be used as both of the pull-down device and ESD protection device in the mixed-voltage I/O circuits. The stacked-nMOS structure includes a

first transistor (top nMOS), having a drain connected to an I/O pad, and a gate (V_{G1}) connected to the VDD power supply. A second transistor (bottom nMOS) is merged into the same active area of the first transistor, having a gate (V_{G2}) connected to the pre-driver of the mixed-voltage I/O circuits. The source of the top nMOS and the drain of the bottom nMOS are constructed together by sharing the common n+ diffusion region.

Under the PS-mode ESD stress condition, the stacked-nMOS is operated in snapback breakdown, with the bipolar effect taking place between the drain of the top nMOS and the source of the bottom nMOS. These two diffusions are acted as bipolar emitter and collector, respectively. Their spacing determines the base width and turn-on efficiency of the lateral bipolar transistor. The snapback mechanism of stacked-nMOS for conducting large amount of ESD current involves both avalanche breakdown and turn-on of the parasitic lateral bipolar transistor. The hole current (Isub) generated from drain avalanche breakdown, drifting through the effective substrate resistance (Rsub) to ground, may elevate the substrate potential (Vsub) of the emitter-base junction in the lateral bipolar transistor. The voltage level, which the local substrate potential is elevated, depends on the relative proximity to the avalanching junction. When the emitter-base junction of bipolar transistor begins to weakly forward bias due to the increase of local substrate potential, additional electron current through the bipolar device is acted as "seed current" to drive a significant increase in the multiplication rate and avalanche current generation at the collector-base junction of the lateral bipolar transistor. Therefore, a "snapback" is seen, and the lateral bipolar transistor enters strong bipolar conduction to discharge ESD current.

The dependences of HBM ESD level on the device channel width and poly-to-poly spacing (common n+ diffusion spacing) of stacked-nMOS device in a 0.25-μm CMOS process are shown in Fig. 2.2. In Fig. 2.2(a), the HBM ESD level of the stacked-nMOS device is increased while the device channel width is increased. Moreover, the stacked-nMOS device with silicide-blocking process can sustain higher ESD level than that with fully silicided process. The non-uniform turn-on issue of the parasitic n-p-n BJT in stacked-nMOS device can be improved by the silicide-blocking process. In Fig. 2.2(b), the HBM ESD level of stacked-nMOS device with fully silicided process is decreased obviously while the poly-to-poly spacing is increased. However, the HBM ESD level of stacked-nMOS device with silicide-blocking process is only decreased slightly. The turn-on efficiency and performance of the parasitic n-p-n BJT in stacked-nMOS device can be improved by reducing the poly-to-poly spacing. Therefore, the ESD robustness of stacked-nMOS device can be

somewhat improved by layout optimization.

2.2 Stacked-NMOS with Substrate-Triggered Technique

2.2.1 Substrate-Triggered Stacked-NMOS Device

The snapback operation of stacked-nMOS device depends on the substrate current (Isub), which is created at the reverse-biased drain/substrate junction, to forward bias the source/substrate junction. Hence, the substrate resistance (Rsub) and substrate current (Isub) are the important design parameters for ESD protection [73], [74]. However, the substrate-triggered technique [56]-[58] can be used to generate the substrate current. With the substrate-triggered current, the trigger voltage of the stacked-nMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection. In this work, the substrate-triggered stacked-nMOS device, which combines the substrate-triggered technique with the stacked-nMOS device, is proposed to protect the mixed-voltage I/O circuits of CMOS ICs.

The finger-type layout pattern and the corresponding cross-sectional view of the new proposed substrate-triggered stacked-nMOS device are shown in Fig. 2.3(a) and Fig. 2.3(b), respectively. As shown in Fig. 2.3, an additional p+ diffusion is inserted into the center drain region of stacked-nMOS device as the substrate-triggered point. The trigger current (Itrig) is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance for improving turn-on efficiency of the parasitic lateral bipolar transistor in the stacked-nMOS device.

2.2.2 ESD Protection Circuit

The ESD protection design, which includes the substrate-triggered stacked-nMOS device and the substrate-triggered circuit for the mixed-voltage I/O circuits, is shown in Fig. 2.4. The substrate-triggered circuit is composed of the diode string, a pMOS Mp1, and an nMOS Mn1, to provide the substrate current for triggering on the parasitic lateral bipolar transistor in the stacked-nMOS device while the ESD voltage is applied on the I/O pad. The anode of the diode string in the substrate-triggered circuit and the collector of the parasitic bipolar transistor in the stacked-nMOS device are connected to I/O pad. The cathode of the diode

string is connected to the source of Mp1. The emitter (the base) of the lateral bipolar transistor is connected to the VSS power line (the drain of Mp1). The nMOS Mn1 is connected between the base of the lateral bipolar transistor and the VSS power line. The gates of Mp1 and Mn1 are connected together to the VDD power line through a resistor. The resistor is realized by an n+ diffusion with a parasitic n+/p-sub diode to avoid the antenna effect during the CMOS process fabrication. The diode string including in the substrate-triggered circuit is composed of individual diodes formed by using P+ diffusion in the separated n-well structure. The total voltage drop across the diode string can be expressed as [64]:

$$V_{string}(I) = mV_D(I) - nV_T[\frac{m(m-1)}{2}] \times \ell n(\beta + 1), \quad (1)$$

where

$V_{string}(I)$ = total voltage drop across the m diodes,

m= the number of diodes in the diode string,

n= ideality factor, and

β = the beta gain of the parasitic vertical pnp bipolar transistor in the diode structure.

During the ESD stress condition, the Mp1 is used in conjunction with the diode string to provide the substrate current to trigger the parasitic lateral bipolar transistor in the stacked-nMOS device. Once the lateral bipolar transistor in the stacked-nMOS device has been turned on, the ESD current is discharged from the I/O pad to VSS.

2.2.3 Operating Principles

Fig. 2.5 shows the cross-sectional view of the substrate-triggered stacked-nMOS device with the substrate-triggered circuit for protecting mixed-voltage I/O circuits. In the normal circuit operating condition, the substrate-triggered circuit should remain in a non-conductive state, so that it does not interfere with the voltage levels on the I/O pad. For the 2.5V/3.3V mixed-voltage IC application, 3.3V tolerance was desired for normal circuit operation with a 2.5-V VDD supply in the chip. The turn-on voltage of the substrate-triggered circuit roughly equals to Vpad $\geqq$ $V_{string}(I)$+|Vtp|+VDD, where the Vtp is the threshold voltage of the pMOS Mp1. The turn-on voltage can be adjusted by varying the numbers of the diodes in the diode string. To satisfy the requirement in the 2.5V/3.3V mixed-voltage application, the number of

the diodes in the diode string should be adjusted to let the turn-on voltage greater than 3.3V. When the I/O pad is applied with a high input voltage of 3.3V, Mp1 is still kept off, and the local substrate of the stacked-nMOS is biased at VSS by the turned-on Mn1. With the diode string to block the 3.3V input voltage on the I/O pad, the Mp1 with thin gate oxide has no gate-oxide reliability issue during the normal circuit operating condition.

The choice of a particular diode string is also determined by the specified pin leakage current at a given temperature. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Since the diode string is not the main ESD current discharge path, its perimeter can be adjusted with less impact on ESD performance. The leakage current problem of the diode string comes from the parasitic vertical pnp bipolar transistor of each diode formed by the P+ diffusion in an n-well. The Mp1 in conjunction with a diode string is used to reduce the leakage current at the I/O pad in the normal operating condition. Moreover, the Mn1 with its gate biased at VDD is always turned on to bypass any leakage current, which may trigger on the lateral npn bipolar transistor in the normal circuit operating condition.

Under the PS-mode ESD stress condition, the gate of the Mp1 has an initial voltage level of ~0V, while the VSS pin is grounded but the VDD pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the Mp1 into the p-substrate, when Vpad $\geqq$ $V_{string}(I)$ + |Vtp|. For a given Rsub, the substrate-triggered circuit must supply an enough trigger current (Itrig) to raise up the local substrate potential, so that V_{BE} (= Isub x Rsub) > 0.6V for triggering on the parasitic lateral n-p-n bipolar transistor in the stacked-nMOS device. Once the lateral bipolar transistor is turned on, the ESD current is discharged from the I/O pad through the lateral bipolar transistor to the grounded VSS. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of Mp1. With an appropriate trigger current, the substrate potential is raised up to trigger on the lateral bipolar transistor and to reduce the trigger voltage of the ESD protection circuit. Therefore, ESD robustness of the mixed-voltage I/O circuits with the stacked-nMOS device can be effectively improved by this new proposed substrate-triggered design. It is important to note that the device size of Mp1 should be large enough than that of Mn1 to provide efficient trigger current into the p-substrate for triggering parasitic lateral n-p-n bipolar transistor. Partial trigger current could be flowed through the Mn1 into VSS power line due to the transient coupling voltage on the gate of Mn1 during PS-mode ESD stress condition. In this work, the device ratio of Mp1 to Mn1 is 5.

A modified connection on the ESD protection design with the substrate-triggered stacked-nMOS device to protect the mixed-voltage I/O circuits is shown in Fig. 2.6. The substrate-triggered circuit is connected from the self-biased n-well of the pull-up pMOS, where the parasitic drain-well diode Dp between the I/O pad and the n-well essentially exists in the pMOS device structure. Under the PS-mode ESD stress condition, the trigger current flows through the parasitic diode Dp and the substrate-triggered circuit to raise the local substrate potential for triggering on the lateral bipolar transistor in the stacked-nMOS device. The main purpose of this modified connection on the ESD protection circuit is to provide the mixed-voltage I/O buffer with a higher ESD robustness but no extra additional capacitance (generating from the ESD detection circuit) to the I/O pad. This modified design is more suitable for high-speed I/O applications, which often require a lower input loading capacitance to the I/O pad.

2.3 Experimental Results

2.3.1 Characteristics of the Substrate-Triggered Stacked-NMOS Device

The measured I-V characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (measured by a Tek370A curve tracer) are shown in Fig. 2.7(a). The relation between the trigger voltage and the substrate-triggered current (Itrig) is summarized in Fig. 2.7(b). As shown in Fig. 2.7, the trigger voltage of the parasitic lateral bipolar transistor in the stacked-nMOS device is decreased while the substrate-triggered current is increased. The trigger voltage of the stacked-nMOS device without the substrate-triggered current is 8.5V (by junction breakdown). However, the trigger voltage can be reduced to only 5.3V when the substrate-triggered current is 8mA.

To investigate the turn-on behavior of the stacked-nMOS device during high ESD current stress, transmission line pulse (TLP) generator with a pulse width of 100ns is used to measure the second breakdown current (It2) of the device [75]. The TLP-measured I-V curves of the stacked-nMOS device with different substrate-triggered currents are shown in Fig. 2.8. The TLP-measured results are consistent with the measured I-V characteristics shown in Fig. 2.7. The trigger voltage of the stacked-nMOS device is decreased when the substrate-triggered current is increased. The dependence of It2 level on the substrate-triggered current (Itrig) under the different channel widths of substrate-triggered stacked-nMOS device is shown in

Fig. 2.9. The It2 level of the substrate-triggered stacked-nMOS device can be improved while the substrate-triggered current is increased. For example, the It2 level is increased from 2.5A to 3.4A for the stacked-nMOS device with a channel width of 240μm, when the substrate-triggered current is increased from 0mA to 2mA. The It2 level of the substrate-triggered stacked-nMOS device is saturated when the substrate-triggered current is high enough to fully trigger on the parasitic bipolar transistor in the stacked-nMOS device.

Based on the experimental results, the ESD protection circuit can be designed with the special substrate-triggered circuit to generate the substrate current to reduce the trigger voltage and to further increase ESD robustness of the stacked-nMOS device in the mixed-voltage I/O buffers.

2.3.2 Leakage Current

The leakage current under normal circuit operating condition is a concern for an ESD protection device connected to an I/O pin. The leakage currents of the fabricated mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit are measured and compared in Fig. 2.10. The leakage current is measured (using a HP4155) by applying a voltage ramp from 0 to 3.3 V to the I/O pad under the bias condition of 2.5-V VDD and 0-V VSS at a room temperature of 25ºC. In Fig. 2.10, the maximum leakage current of the mixed-voltage I/O buffer with (without) the substrate-triggered circuit under 3.3-V bias at the I/O pad is only 1.1nA (0.2nA), which is acceptable for general I/O applications. The mixed-voltage I/O buffer in this measurement has a channel width of 240μm in the stacked nMOS and a channel width of 480 μm in the pull-up pMOS. The leakage currents of the mixed-voltage I/O buffer with or without the substrate-triggered circuit, under the 3.3-V voltage bias at the I/O pad at different temperatures are shown in Fig. 2.11. The leakage current of the mixed-voltage I/O buffer is increased while the temperature is increased. In Fig. 2.11, the leakage current of the mixed-voltage I/O buffer with the substrate-triggered circuit at the temperature of 25ºC (125ºC) is 1.1nA (0.2μA). The diode string of the substrate-triggered circuit in this investigation includes 6 diodes. More diodes can be added into the diode string to further reduce the leakage current of the mixed-voltage I/O buffer with the substrate-triggered circuit.

2.3.3 ESD Level

The PS-mode HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit are measured and compared in Fig. 2.12. The failure criterion is defined as the leakage current of the circuits after ESD zapping is greater than 1μA under the normal operating voltage of 3.3V. The mixed-voltage I/O buffers with different stacked-nMOS channel widths are also tested as a reference. As seen in Fig. 2.12, the HBM ESD level of the mixed-voltage I/O buffers with the substrate-triggered circuit is almost linearly increased while the stacked-nMOS channel width is increased. It implies that the parasitic lateral bipolar transistor in the stacked nMOS can be uniformly turned on to discharge ESD current by the substrate-triggered circuit. The HBM ESD level of the mixed-voltage I/O buffer (with stacked-nMOS channel width of 240 μm) can be obviously improved from the original 3.4kV up to 5.6kV (an increase of ~65%) by using the substrate-triggered technique.

The HBM ESD robustness of the mixed-voltage I/O buffer, with or without the substrate-triggered circuit, under the four pin-combination modes of ESD stress on the I/O pad, is listed in Table 2.1. The stacked nMOS of the mixed-voltage I/O buffer in this ESD test has a W/L of 120μm/0.5μm, and the pull-up pMOS of the mixed-voltage I/O buffer has a W/L of 240μm/0.5μm. As shown in Table I, the PS-mode ESD level of the mixed-voltage I/O buffer is worst among four ESD-zapping modes. The PS-mode ESD level for the mixed-voltage I/O buffer with substrate-triggered circuit can be obviously improved from the original 2.1kV up to 3kV. The experimental result has verified the effectiveness of the substrate-triggered design to improve ESD level of mixed-voltage I/O circuits.

2.4 Summary

To improve ESD robustness of the stacked-nMOS device in the mixed-voltage I/O circuit, the stacked-nMOS device with new proposed substrate-triggered circuit, has been designed and successfully verified in a 0.25-μm salicided CMOS process. The I-V characteristics of stacked-nMOS device with substrate-triggered technique have been measured to verify its effectiveness. By using this substrate-triggered design, the trigger voltage of the stacked-nMOS device can be reduced from the original 8.5V to become 5.3V to ensure effective protection for the mixed-voltage I/O circuits. The HBM ESD level of the

mixed-voltage I/O buffer with a stacked-nMOS of 240-μm channel width can be improved from the original 3.4kV up to 5.6kV by the substrate-triggered circuit. Without using the thick gate oxide, this new proposed ESD protection design is very useful in the sub-quarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins.

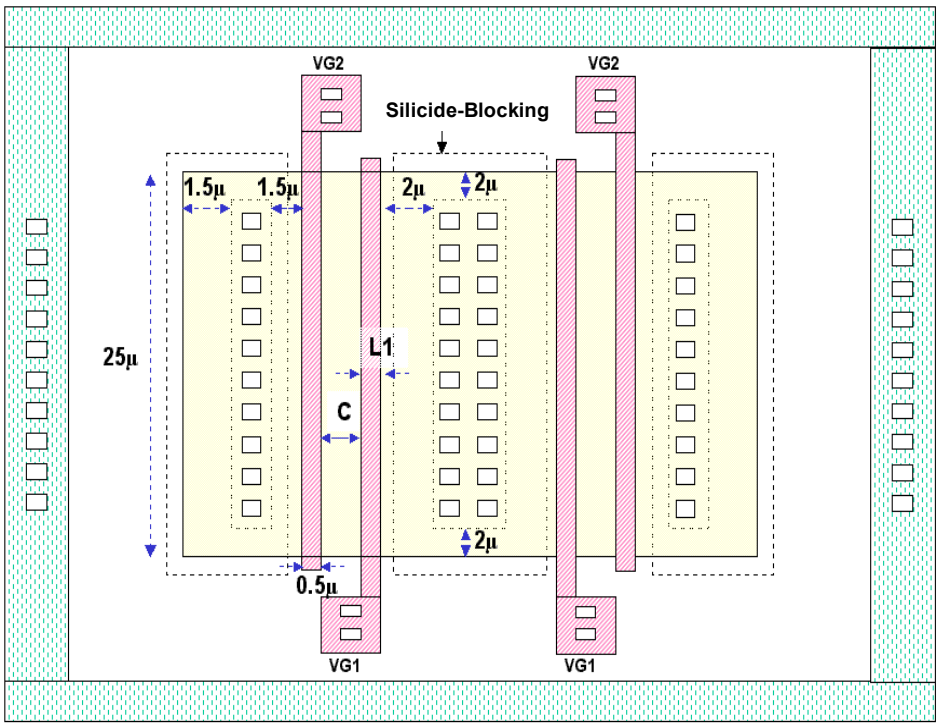
TABLE 2.1

HBM ESD robustness of the mixed-voltage I/O buffers

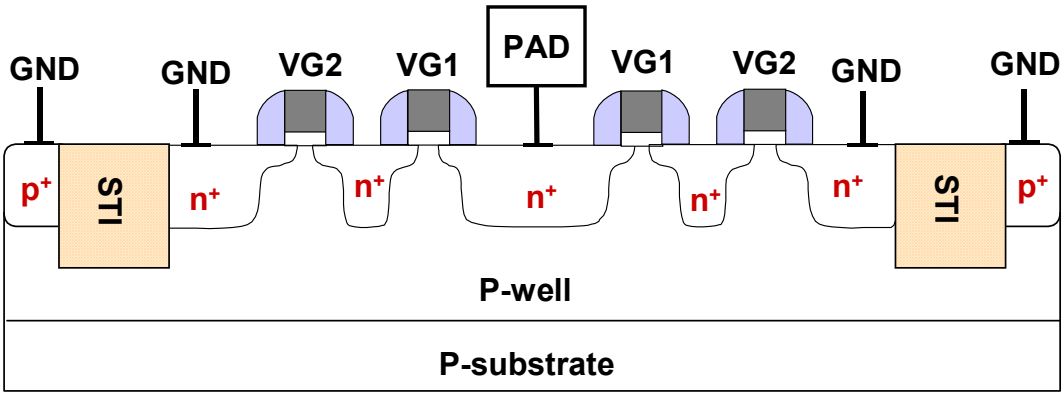
with or without the proposed substrate-triggered circuit under a fixed device dimension.

HBM ESD Stress / I/O Circuits	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD (+)	ND-Mode VDD (-)
Original Mixed-Voltage I/O Buffer	2.1kV	6.4kV	3.1kV	3.9kV
Mixed-Voltage I/O Buffer + Substrate-Triggered Circuit	3kV	6.4kV	3.3kV	4kV

Pull-up PMOS W/L = 240/0.5 (μm) **Stacked-NMOS W/L = 120/0.5 (μm)**
with Silicide-Blocking

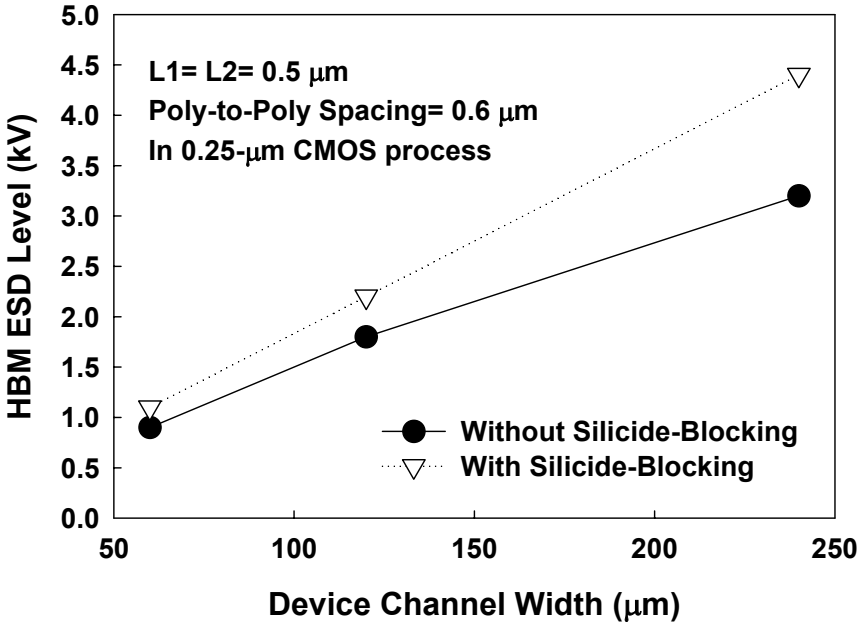


(a)

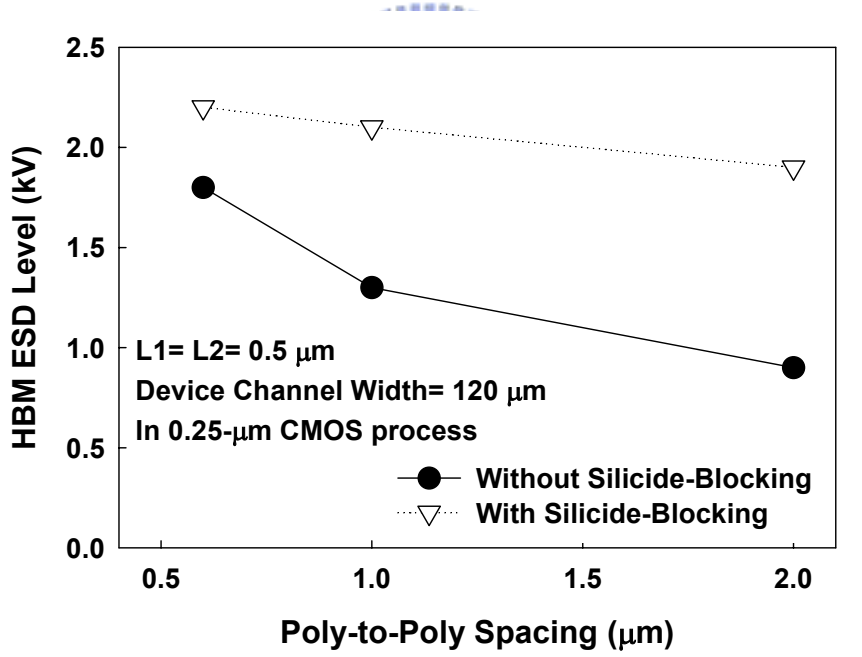


(b)

Fig. 2.1 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the stacked-nMOS device for mixed-voltage I/O circuit in a p-substrate CMOS process.

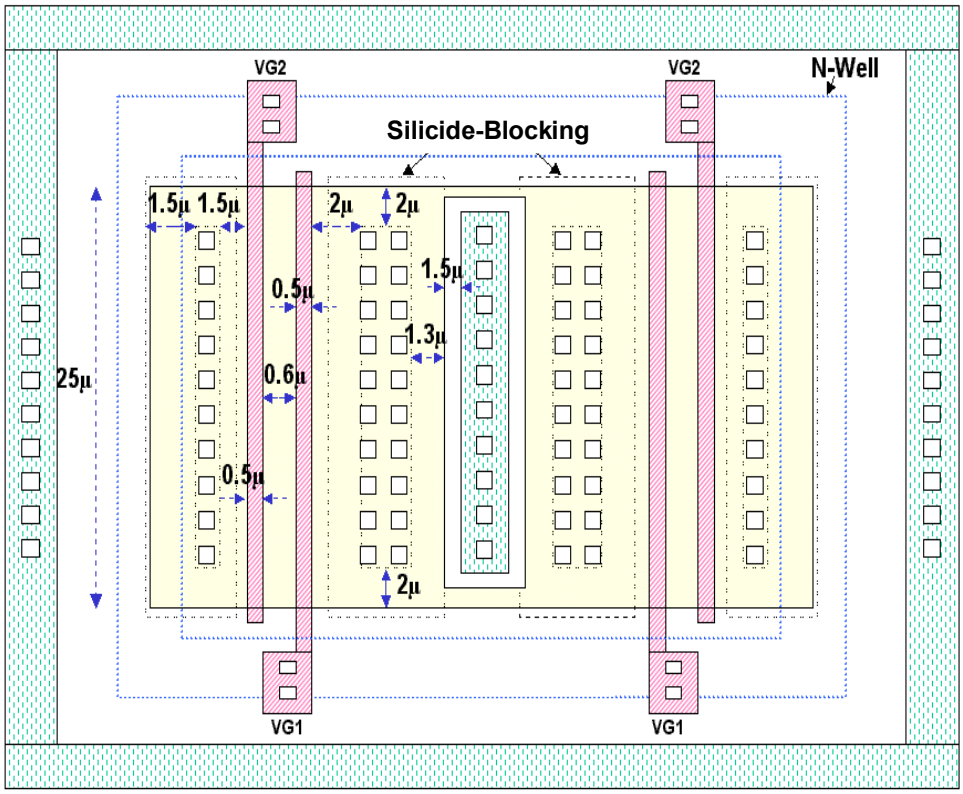


(a)

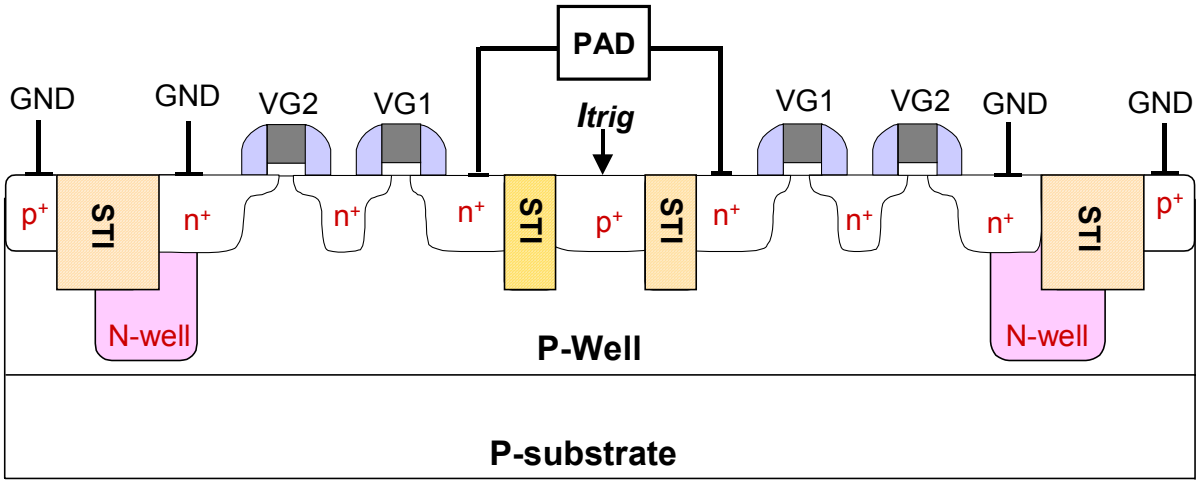


(b)

Fig. 2.2 Comparisons of HBM ESD robustness of the stacked-nMOS device with or without the silicide-blocking process, under (a) different channel widths, and (b) different poly-to-poly spacings, of the stacked-nMOS device fabricated in a 0.25-μm CMOS process.



(a)



(b)

Fig. 2.3 (a) The finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-nMOS device for mixed-voltage I/O circuit in a p-substrate CMOS process.

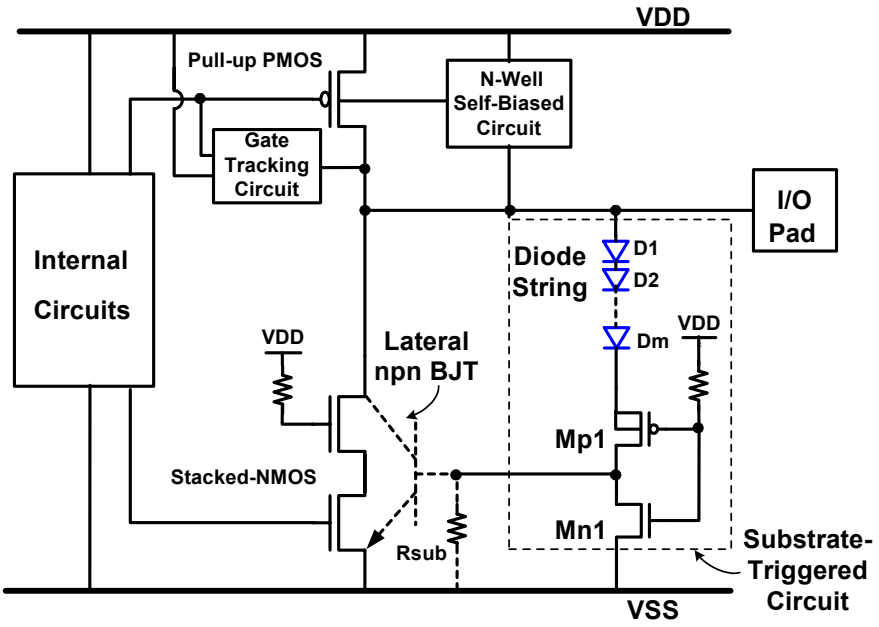


Fig. 2.4 The schematic circuit diagram of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits.

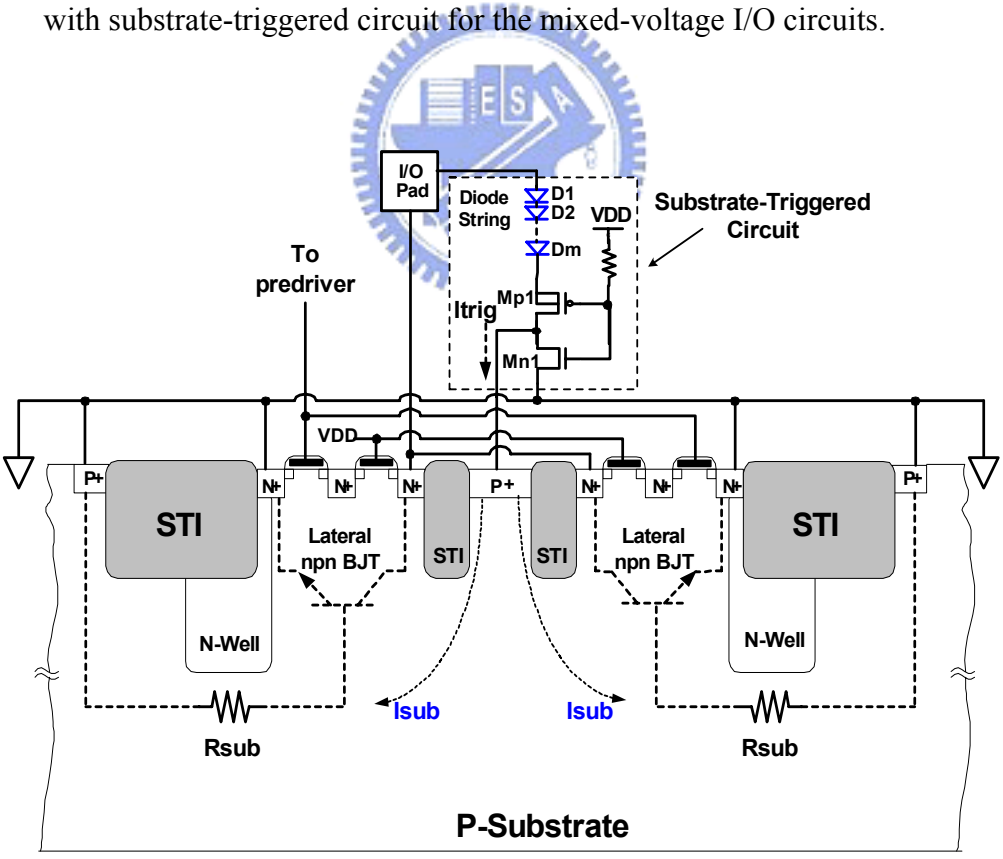


Fig. 2.5 The cross-sectional view of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits.

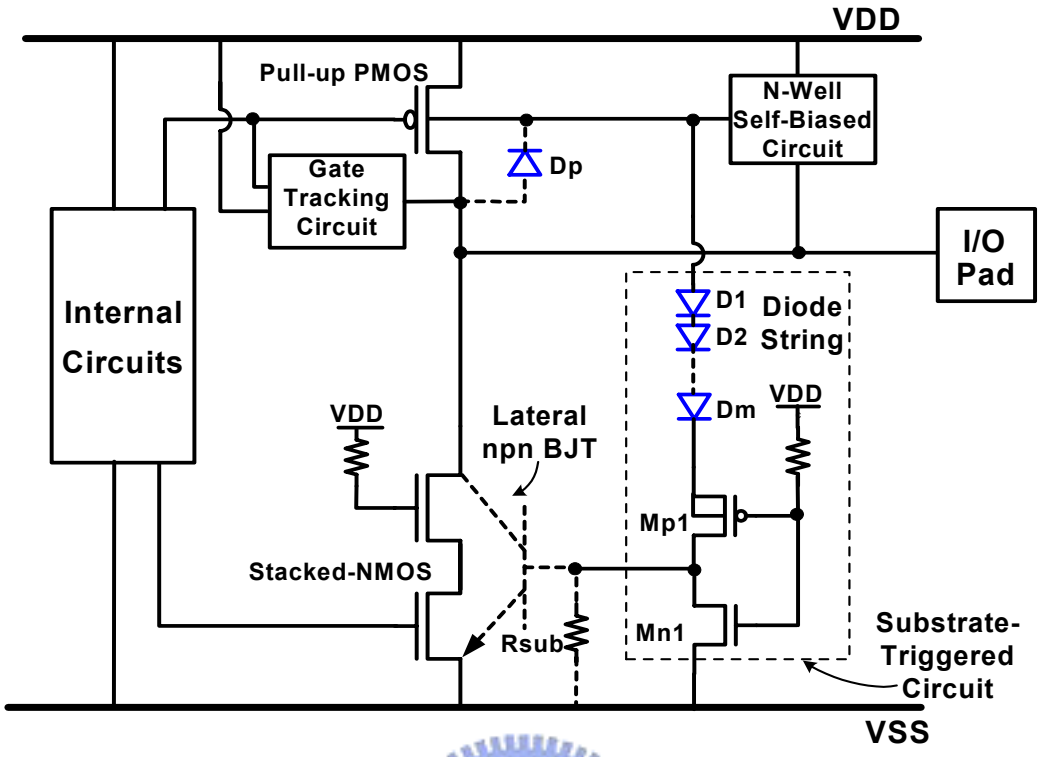
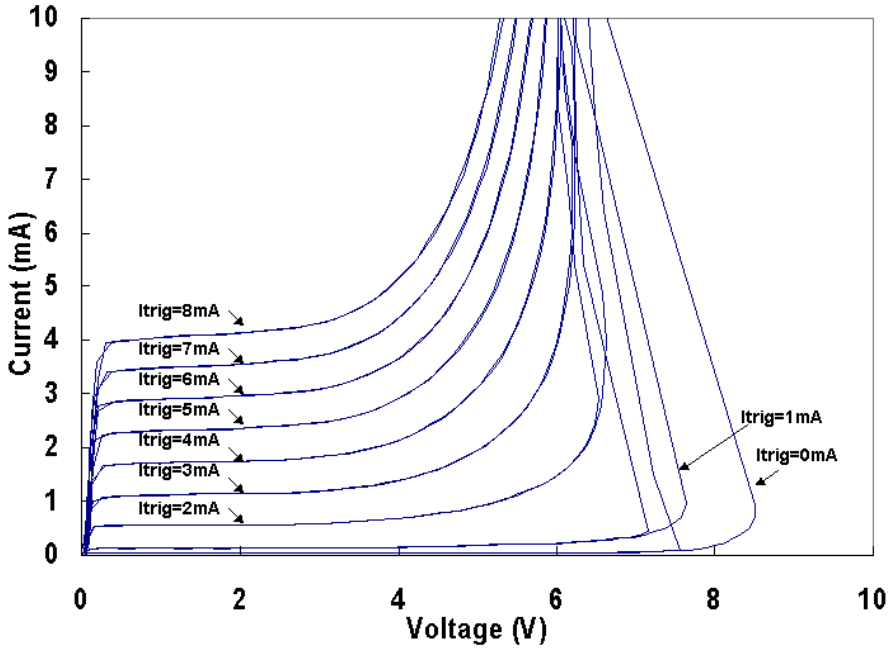
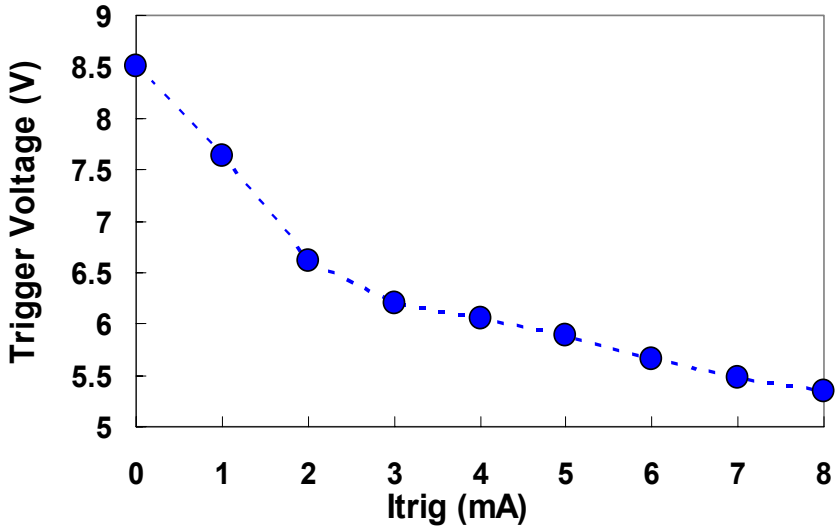


Fig. 2.6 The modified design of the substrate-triggered stacked-nMOS device with substrate-triggered circuit for the mixed-voltage I/O circuits without generating extra additional capacitance to the I/O pad.



(a)



(b)

Fig. 2.7 (a) The measured I-V characteristics of the substrate-triggered stacked-nMOS device with different substrate-triggered currents (Itrig). (b) The relation between the trigger voltage of the stacked-nMOS device and the substrate-triggered current (Itrig).

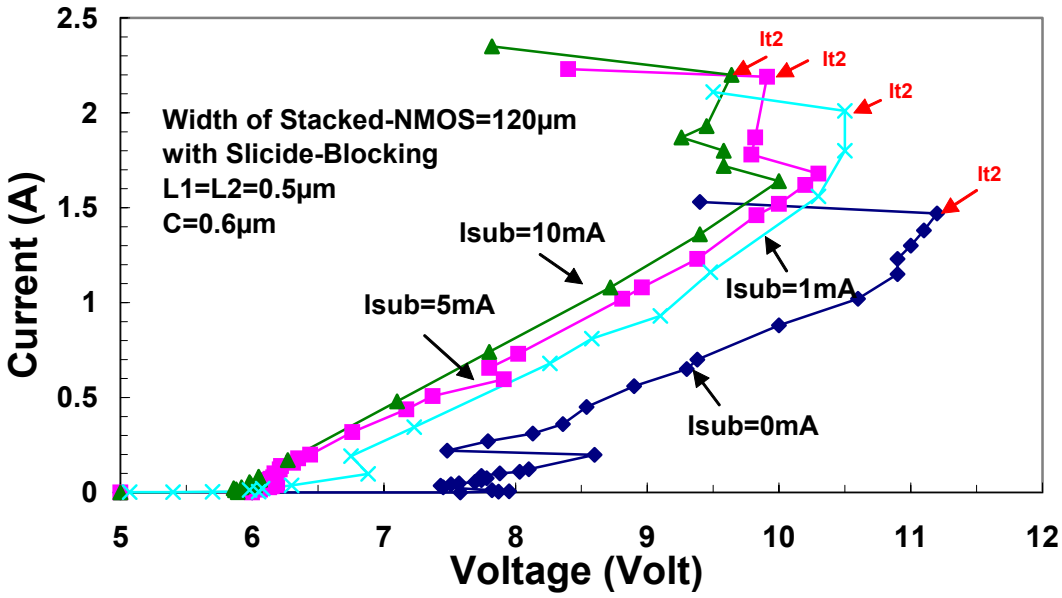


Fig. 2.8 The TLP-measured I-V curves of the stacked-nMOS device with different substrate-triggered currents.

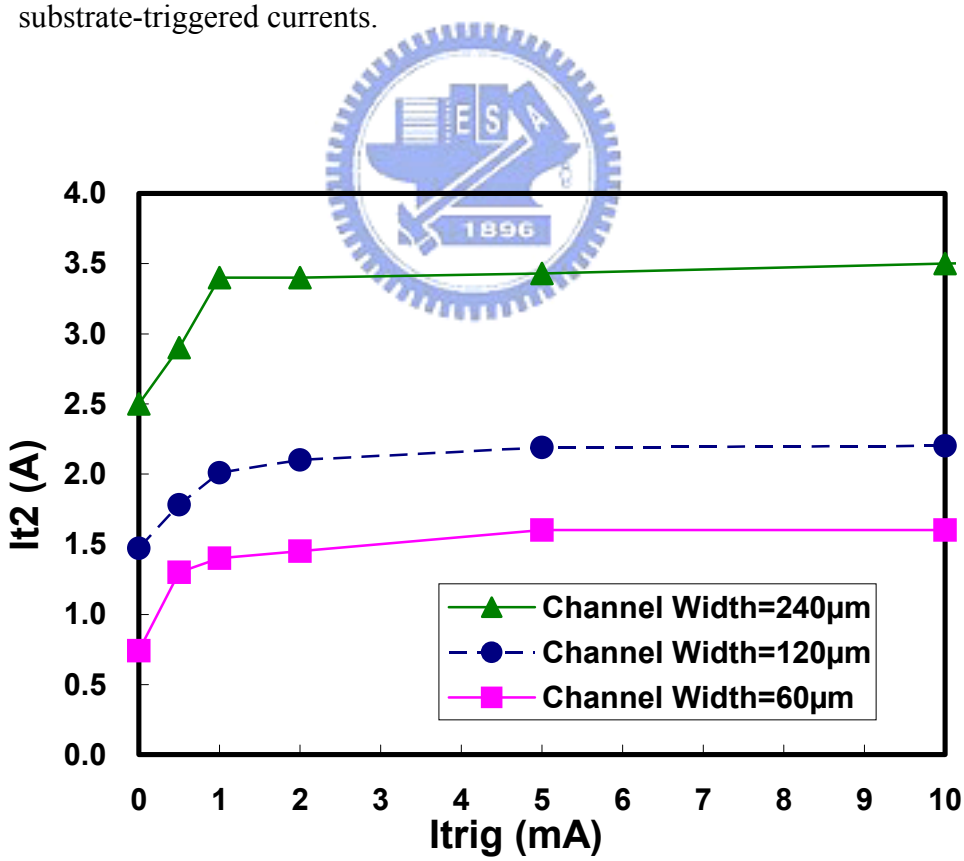


Fig. 2.9 The dependence of It2 level on the substrate-triggered current (Itrig) under the different channel widths of substrate-triggered stacked-nMOS device.

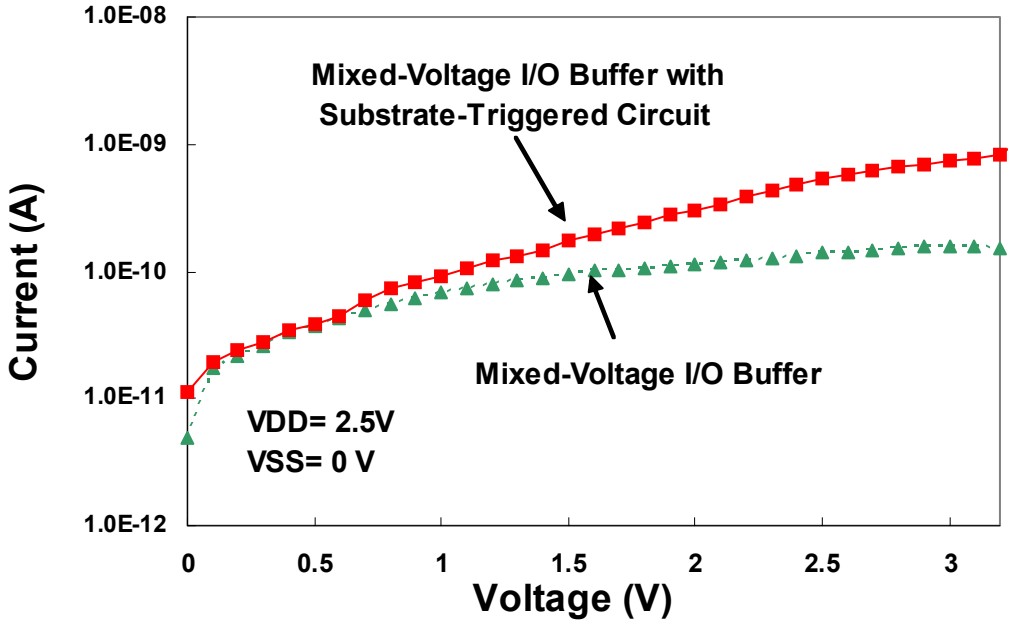


Fig. 2.10 Comparison of the leakage currents of the mixed-voltage I/O buffers with or without the proposed substrate-triggered circuit. The mixed-voltage I/O buffer in this measurement has a channel width of 240 μm in the stacked nMOS and a channel width of 480 μm in the pull-up pMOS.

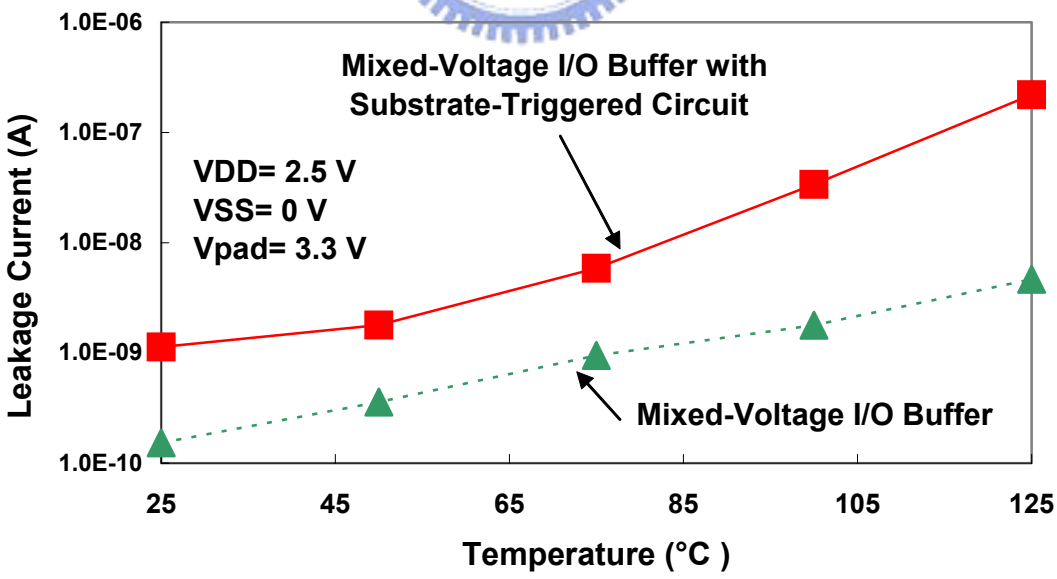


Fig. 2.11 The leakage currents of the mixed-voltage I/O buffers with or without the substrate-triggered circuit under different temperatures.

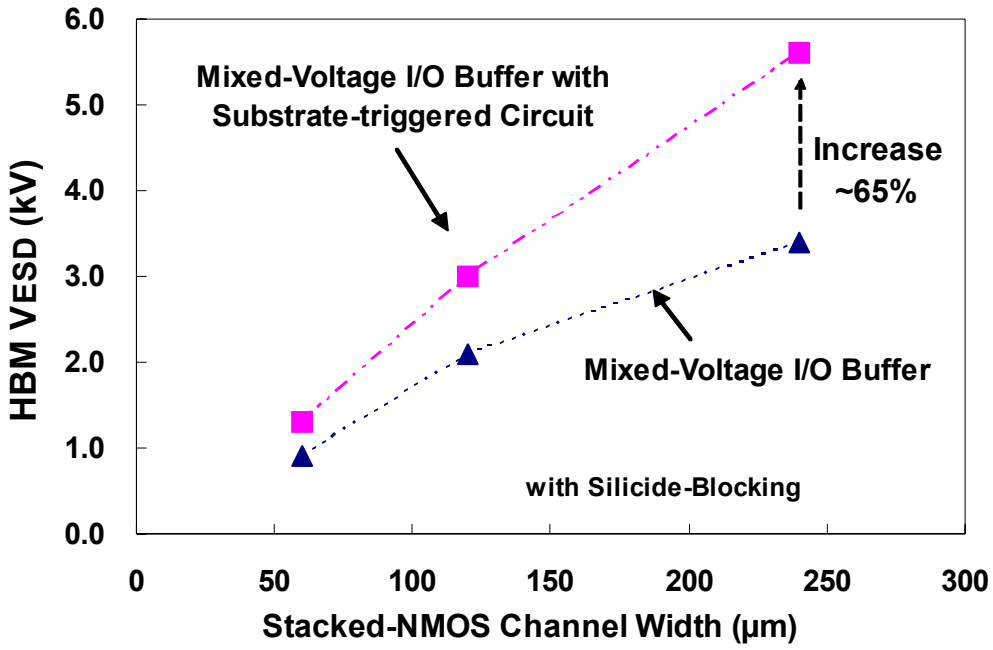


Fig. 2.12 The positive-to-VSS (PS-mode) HBM ESD levels of the mixed-voltage I/O buffers with or without the substrate-triggered circuit, realized in a 0.25-μm CMOS process with silicide-blocking process.

CHAPTER 3

ESD PROTECTION DESIGN FOR IC WITH POWER-DOWN-MODE OPERATION

For IC with power-down-mode operation, the on-chip ESD protection circuits will meet more design constraints and difficulties. In this chapter, three new ESD protection schemes for CMOS IC with power-down-mode operation are proposed. By adding a VDD ESD bus line and diodes, the ESD protection design can block the leakage current from I/O pin to VDD power line to avoid malfunction during power-down-mode operating condition. During normal circuit operating condition, the ESD protection design has no leakage path to interfere with the normal circuit functions. The whole-chip ESD protection design can be achieved by insertion of ESD clamp circuits between VSS power line and both VDD power line and VDD ESD bus line. These new ESD protection designs for IC with power-down-mode operation has been successfully designed and verified in a 0.35-μm silicided CMOS process [31]-[33]. Furthermore, output-swing improvement circuit is proposed to achieve the full swing of output voltage level during normal circuit operating condition [33].

3.1 New ESD Protection Schemes for IC with Power-Down-Mode Operation

3.1.1 ESD Protection Scheme I

The proposed ESD protection scheme I for the IC with power-down-mode operation is shown in Fig. 3.1 with the additional ESD bus line (VDD_ESD), which is realized by wide metal line in CMOS IC. The VDD_ESD bus line is not directly connected to an external power supply pin. The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input pad to VDD when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of output pMOS (Mp_out) to block the leakage current path from the output pad to VDD when the

power of VDD is off. The VDD_ESD bus line is not connected to the source of Mp_out in this scheme, because Mp_out may be turned on. The gate voltage of Mp_out will be dropped down and induces leakage current between I/O pads when the power of VDD is off. With the new proposed ESD protection scheme, the leakage current or malfunction issues for the IC with power-down-mode operation can be avoided. The diode D3 is connected between the output pad and VDD_ESD bus line for ESD protection purpose. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between VDD_ESD bus line and VSS power line.

In the typical mixed-voltage I/O buffer, the output pMOS, connected from the I/O pad to the VDD power line, has self-biased circuits for tracking its gate and n-well voltages to avoid the leakage current path from the I/O pad to VDD when an over-VDD external signal is applied to the I/O pad [16]. However, during the power-down-mode operation, the tracking circuits will not function because the power of VDD is off. The channel of output pMOS cannot be kept off when the external voltage level on the output pad is high; therefore the leakage current may be induced from the output pad to VDD when the power of VDD is off. By using the new proposed ESD protection scheme, the leakage current path from the I/O pad to VDD can be completely blocked by the diode D2 during the power-down-mode operation. Although the output signal cannot be pulled up to VDD (kept at VDD-Vd, where Vd is the cut-in voltage of the diode D2) during normal circuit operating condition, it can be further improved with additional output-swing improvement circuit.

The ESD current discharging paths of the input pad under PS-mode ESD stress condition, the output pad under PS-mode ESD stress condition, the input pad under PD-mode ESD stress condition, and the output pad under PD-mode ESD stress condition are shown in Figs. 3.2(a) ~ 3.2(d), respectively. The ESD current at the input (or output) pad under PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or the diode D3) to the VDD_ESD bus, and then through the ESD clamp circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress can be discharged through the parasitic diode of Mp_in (or the diode D3) to VDD_ESD bus line, the ESD clamp circuit to VSS power line, and then through the parasitic diode of ESD clamp circuit to the grounded VDD power line. The negative ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The negative ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or

Mn_out) to VSS power line, and then discharged through the VDD-to-VSS ESD clamp circuit to the grounded VDD power line. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed ESD protection scheme.

3.1.2 ESD Protection Scheme II

The proposed ESD protection scheme II for the IC with power-down-mode operation is shown in Fig. 3.3. The design concept is similar to that of the ESD protection scheme I. In ESD protection scheme II, the VDD_ESD bus line is separated into input stage and output stage by the diode D3. The VDD ESD bus line of output stage is connected to the source of output pMOS (Mp_out). The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input pad to VDD when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of Mp_out to block the leakage current path from the output pad to VDD when the power of VDD is off. The gate voltage of Mp_out will be dropped down to induce leakage current between I/O pads when the power of VDD is off. The diode of D3 is used to block the leakage current between the I/O pads. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between VDD_ESD bus line and VSS power line.

The ESD current at the input (or output) pad under PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to the VDD_ESD bus, (the diode of D3,) and then discharged through the power-rail ESD clamp circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress can be discharged through the parasitic diode of Mp_in (or Mp_out) to VDD_ESD bus line, (the diode of D3,) the power-rail ESD clamp circuit to VSS power line, and then through the parasitic diode of power-rail ESD clamp circuit to the grounded VDD power line. The negative ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The negative ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to VSS power line, and then discharged through the power-rail ESD clamp circuit to the grounded VDD power line. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed ESD protection scheme.

3.1.3 ESD Protection Scheme III

The proposed ESD protection scheme III for the IC with power-down-mode operation is shown in Fig. 3.4. The design concept is similar to that of the ESD protection scheme I. The diode D1 is connected between the VDD power line and VDD ESD bus line to block the leakage current path from the input or output pad to VDD, when the power of VDD is off. The diode D3 in scheme II is replaced by the Mp1 in scheme III to block the leakage current between the I/O pads when the power of VDD is off. The gate of Mp1 is connected to the VDD power line. Therefore, Mp1 is turned off under the normal circuit operating condition. Under power-down-mode operating condition, Mp1 is turned on to keep the Mp_out off. In addition, the power line of the pre-driver internal circuits which controlled the gate of Mp_out is connected to the VDD ESD bus line to avoid the leakage current from the pre-driver internal circuits to VDD power line, when the power of VDD is off. The ESD current at the input (or output) pad under PS-mode ESD stress condition can be discharged through the parasitic diode of Mp_in (or Mp_out) and the power-rail ESD clamp circuit between the VDD ESD bus line and the VSS power line to ground. The ESD current at the input (or output) pad under the PD-mode ESD stress condition can be discharged through the parasitic diode of Mp_in (or Mp_out) to VDD ESD bus line, the power-rail ESD clamp circuit to VSS power line, and then the parasitic diode of ESD clamp circuit to the grounded VDD power line. The negative ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The negative ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to VSS power line, and then discharged through the power-rail ESD clamp circuit to the grounded VDD power line. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed ESD protection scheme.

Therefore, with the new proposed ESD protection schemes, the leakage current or malfunction issues for the IC with power-down-mode operation can be avoided. The internal circuits of CMOS IC can be fully protected against ESD damage by the new proposed ESD protection schemes.

3.1.4 Layout Consideration

For saving the layout area, the VDD_ESD bus line in the proposed ESD protection schemes can be realized by the different parallel metal layer, which overlaps the VDD power

line. The junction perimeter of the diodes (D1, D2, and D3) in the proposed ESD protection schemes can be drawn with small layout area, because the ESD current is discharged through these diodes with the forward-diode path. The device dimension of Mp1 in scheme II can be adjusted with less impact on ESD performance. In addition, it's important to note that the location of power-rail ESD clamp circuit connected between VDD_ESD bus line and VSS power line is an important factor to implement the ESD protection scheme II. Because the ESD bus line is separated into input stage and output stage by the diode D3, the power-rail ESD clamp circuit must be placed in the input stage to provide the ESD current discharging path for input pad under ESD stress.

3.2 Experimental Results

The testchip with traditional and new proposed ESD protection schemes had been fabricated in a 0.35-μm silicided CMOS process. Fig. 3.5 shows the layout view of the new proposed ESD protection scheme I. Some inverters are connected from the input pad to the output pad, being served as the internal circuits for function verification of this testchip. The input ESD protection devices are realized by the gate-connected-to-source pMOS and gate-grounded nMOS with both the device dimensions (W/L) of 490/0.5 (μm/μm). The output ESD protection devices are realized by the output buffer of pMOS and nMOS with the same device dimensions. The layout parameters of ESD protection devices and output buffers are drawn according to the foundry's ESD rules with the silicide-blocking mask. In the proposed ESD protection schemes, the junction perimeter of the diodes (D1, D2, and D3) is drawn as 50μm. In the proposed ESD protection scheme III, the device dimension (W/L) of Mp1 is drawn as 20/0.5 (μm/μm). The power-rail ESD clamp circuit is realized by the substrate-triggering field-oxide device (STFOD) [76], [77] to have high enough ESD level in a limited layout area, as shown in Fig. 3.6. The device dimensions for the power-rail ESD clamp circuit are drawn as R=55.3kΩ, C=14.2pF, W/L of Mp=100μm/1.2μm, W/L of Mn=20μm/1.2μm, and W/L of STFOD=232.8μm/1μm.

3.2.1 Leakage Current

The leakage currents at the input pad of the traditional and new proposed ESD protection schemes under normal circuit operating condition are compared in Fig. 3.7(a). The leakage

current is measured by applying a voltage ramp from 0 to 3.3V to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In Fig. 3.7(a), the leakage currents at the input pad of traditional ESD protection scheme, new proposed ESD protection schemes I, II, and III are 109pA, 134pA, 132pA, and 122pA, respectively, with a 3.3-V signal applying to the input pad. From the measured results, the new proposed ESD protection schemes do not induce any extra leakage current under normal circuit operating condition.

The leakage currents at input pad and output pad of the traditional and new proposed ESD protection schemes under power-down-mode operating condition are measured and compared in Figs. 3.7(b) and 3.7(c), respectively. The leakage current is measured by applying a voltage ramp from 0 to 3.3V to the input or output pad under the bias condition of 0-V VDD and 0-V VSS. From the measured results, the leakage currents at the input pads (output pads) of the new proposed ESD protection schemes are only ~130pA in Fig. 3.7(b) (~300pA in Fig. 3.7(c)), when a 3.3-V signal is applied to the input pad (output pad). On the contrary, the traditional ESD protection scheme has a very high leakage current of up to several mA when the input or output voltage is only increased to 0.7V. The leakage current in the new proposed ESD protection scheme has been successfully blocked by the diode of D1 or D2. The experimental results have verified that the new proposed ESD protection schemes can avoid the leakage current from the I/O pin to VDD power line under the power-down-mode operating condition.

3.2.2 Function Verification

The measurement setup to verify the function of I/O cells with the new proposed ESD protection schemes, or the traditional ESD protection scheme, under normal circuit operating condition and power-down-mode operating condition is shown in Fig. 3.8. To verify the function among the different designs under normal circuit operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 3.3-V VDD and 0-V VSS. In addition, to verify the function among the different designs under power-down-mode operating condition, a 0-to-3.3 V voltage pulse with a rise time of 20 ns is applied to the input pad under the bias condition of 0-V VSS but VDD is floating.

Figs. 3.9(a) and 3.9(b) show the voltage waveforms on the input/output pad of the I/O cells with the traditional ESD protection scheme under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 3.9(a), the I/O cells with traditional ESD protection circuits can be operated normally under normal circuit

operating condition. However, under the power-down-mode condition, the voltage waveform on the output pad is dropped to a voltage level of ~1.4V, when the input voltage level is 0V, as that shown in Fig. 3.9(b). It implies that the internal circuits are triggered by the input voltage waveform under power-down-mode operating condition, although the circuits are expected to be off. With the wrong voltage waveform at the I/O pads, the system could be malfunction.

Figs. 3.10(a) and 3.10(b) show the voltage waveforms on the input/output pad of the I/O cells with the new proposed ESD protection scheme I under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 3.10(a), the I/O cells with the new proposed ESD protection scheme I can be operated normally under normal circuit operating condition. The high voltage level on the output pad is kept at ~2.7V (VDD-Vd, where Vd is the cut-in voltage of the diode D2). In Fig. 3.10(b), the voltage level on the output pad is always kept at ~ 0V under power-down-mode operating condition. This result has verified that the internal circuits can be really kept inactive by the new proposed ESD protection scheme I under power-down-mode operating condition. In addition, the measured voltage waveforms on the input/output pad of I/O cells with the proposed ESD protection scheme II or ESD protection scheme III have the same results as those shown in Figs. 3.10(a) and 3.10(b) under normal circuit operating condition and power-down-mode operating condition, respectively. The experimental results have verified that the I/O cells with the proposed ESD protection scheme II or ESD protection scheme III can be normally operated under normal circuit operating condition, as well as the internal circuits can be really kept inactive under power-down-mode operating condition.

3.2.3 ESD Robustness

The HBM ESD robustness of I/O pads with the traditional or new proposed ESD protection schemes under different pin combinations is listed in Table 3.1. The failure criterion is defined as the leakage current of the circuits after ESD stress is greater than 1μA under the normal operating voltage of 3.3V. With the traditional ESD protection scheme, the ESD level of the I/O pads is 5kV, which is dominated by the I/O pad under the ND-mode ESD stress or positive VDD-to-VSS ESD stress. However, with the new proposed ESD protection scheme I, II and III, the ESD level of the I/O pads is 7.5kV, which is dominated by the I/O pad under the PS-mode or PD-mode ESD stress. The ESD level of I/O pad under the ND-mode ESD stress or VDD-to-VSS ESD stress is improved by the extra ESD current path

in the new proposed ESD protection scheme, which is discharged through the diode D1 and power-rail ESD clamp circuit between the VDD ESD bus line and VSS power line. As a result, ESD level of the whole chip can be efficiently improved by the new proposed ESD protection schemes for IC with power-down-mode operation.

3.3 Output-Swing Improvement Circuit

Although the output signal of the new proposed ESD protection scheme was not pulled up to full-VDD voltage swing during normal circuit operating condition, it can be further improved with additional output-swing improvement circuit. This circuit block connecting between the VDD power line and VDD_ESD bus line in the ESD protection scheme II is shown in Fig. 3.11(a). The circuit diagram of output-swing improvement circuit is shown in Fig. 3.11(b). In this circuit, Mp1 is used as a pull-up device to achieve the full-VDD voltage swing of output signal. During normal circuit operating condition, Mp1 is always turned on. Thus, the output signal can be pulled up to VDD by the turn-on of Mp_out controlled by the pre-driver circuits. Therefore, the device size of Mp1 is determined by the driving current of the output cell in a CMOS IC. During power-down-mode operating condition, Mp1 is turned off to avoid the leakage current path from the output pad to VDD. The Mn1 and Mp2 in this circuit are used to control the gate of Mp1 during normal circuit operating condition and power-down-mode operating condition, respectively. The gates of Mn1 and Mp2 are connected to the VDD power line. Therefore, Mp2 is turned off, and Mn1 is turned on to keep the gate voltage of Mp1 at ~0V under normal circuit operating condition. With the turn-on of Mp1, the output signal can be pulled up to full-VDD voltage swing under normal circuit operating condition. Under power-down-mode operating condition with the bias condition of 0-V VDD, Mn1 is turned off, and Mp2 is turned on to keep the Mp1 off. The bodies (n-well) of Mp1 and Mp2 are connected to the VDD_ESD bus line to avoid the leakage path of the parasitic diode under power-down-mode operating condition. Therefore, no extra leakage current will be induced under the power-down-mode operating condition. This output-swing improvement circuit has been fabrication with the new proposed ESD protection scheme in a 0.35-μm CMOS process to verify its effectiveness.

The leakage currents at I/O pads of new proposed ESD protection scheme II with output-swing improvement circuit under normal circuit operating condition and

power-down-mode operating condition are measured in Fig. 3.12. From the measured results, no extra leakage current is induced by adding output-swing improvement circuit in the new proposed ESD protection scheme under both normal circuit operating condition and power-down-mode operating condition.

Figs. 3.13(a) and 3.13(b) show the voltage waveforms on the input/output pad of the new proposed ESD protection scheme II with the output-swing improvement circuit under normal circuit operating condition and power-down-mode operating condition, respectively. As shown in Fig. 3.13(a), the output signal has been really pulled up to full-VDD voltage swing under normal circuit operating condition, when the input voltage level is 0V. In Fig. 3.13(b), the internal circuits can be really kept off under power-down-mode operating condition. Therefore, the output signal of the proposed ESD protection scheme can be pulled up to VDD by the output-swing improvement circuit under normal circuit operating condition, without increasing any leakage current.

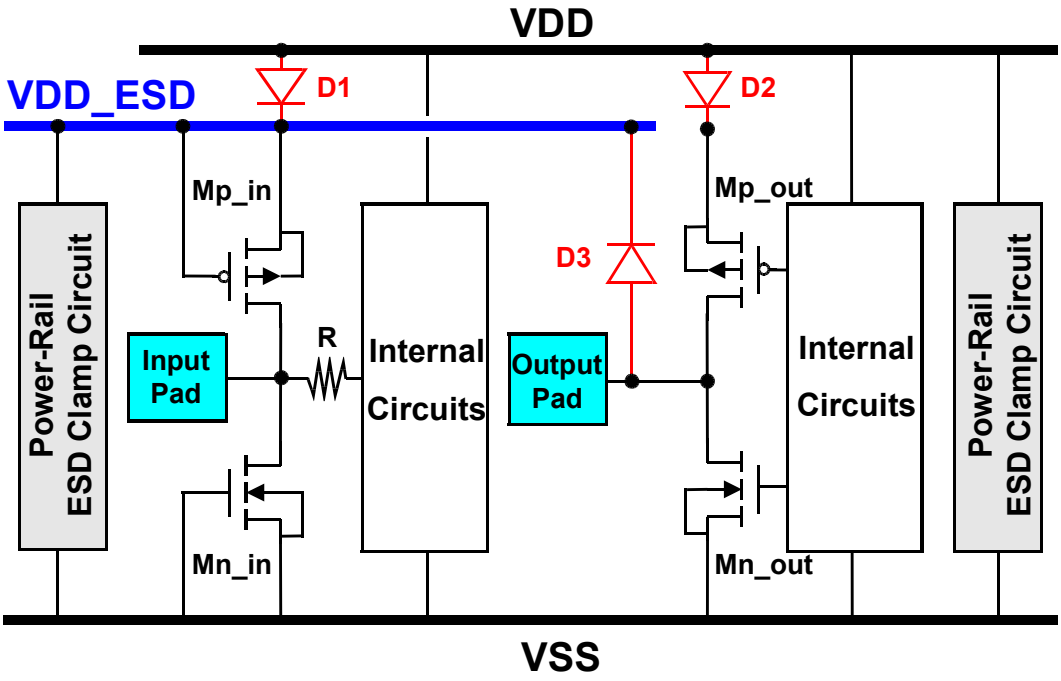
3.4 Summary

Three new ESD protection schemes without leakage current path for CMOS IC operating in power-down-mode condition has been successfully designed and verified in a 0.35-μm silicided CMOS process. Under the normal circuit operating condition, the I/O cells with the new proposed ESD protection schemes can be operated normally. Under the power-down-mode operating condition, the new proposed ESD protection schemes can provide the I/O pad without leakage path, and avoid triggering the internal circuits those should be “off”. High ESD robustness has been practically achieved in the testchip with these new proposed ESD protection schemes to sustain HBM ESD stress of up to 7.5kV in a 0.35-μm silicided CMOS process. Furthermore, the output signal of the new modified ESD protection schemes can be successfully pulled up to VDD again by the output-swing improvement circuit under normal circuit operating condition.

TABLE 3.1

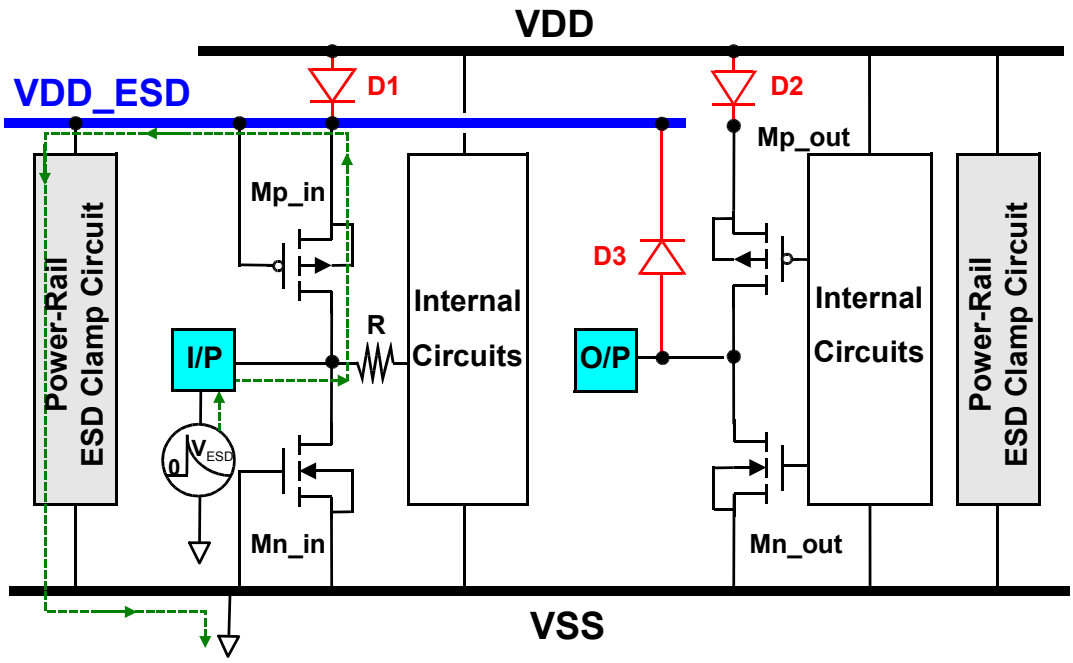
HBM ESD robustness of the traditional ESD protection scheme and the new proposed ESD protection schemes.

ESD Protection Scheme \ HBM ESD Stress	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VSS(+)	ND-Mode VSS(-)	VDD-to-VSS(+)	VDD-to-VSS(-)
Traditional Scheme (Input Pin)	7.5kV	>8kV	>8kV	5kV	5kV	>8kV
Traditional Scheme (Output Pin)	7.5kV	>8kV	>8kV	5kV		
New Proposed Scheme I (Input Pin)	7.5kV	>8kV	7.5kV	>8kV	>8kV	>8kV
New Proposed Scheme I (Output Pin)	>8kV	>8kV	>8kV	>8kV		
New Proposed Scheme II (Input Pin)	7.5kV	>8kV	7.5kV	>8kV	>8kV	>8kV
New Proposed Scheme II (Output Pin)	7.75kV	>8kV	7.75kV	>8kV		
New Proposed Scheme III (Input Pin)	7.75kV	>8kV	7.75kV	>8kV	>8kV	>8kV
New Proposed Scheme III (Output Pin)	7.5kV	>8kV	>8kV	>8kV		

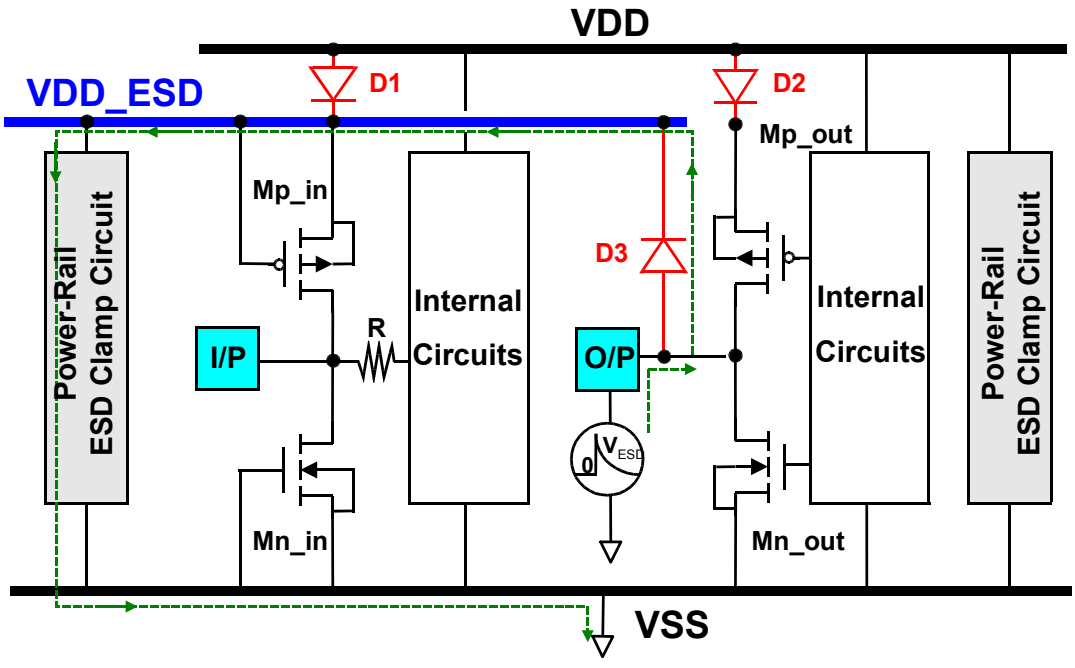


(b)

Fig. 3.1 The new proposed ESD protection scheme I for the IC with power-down-mode operation.

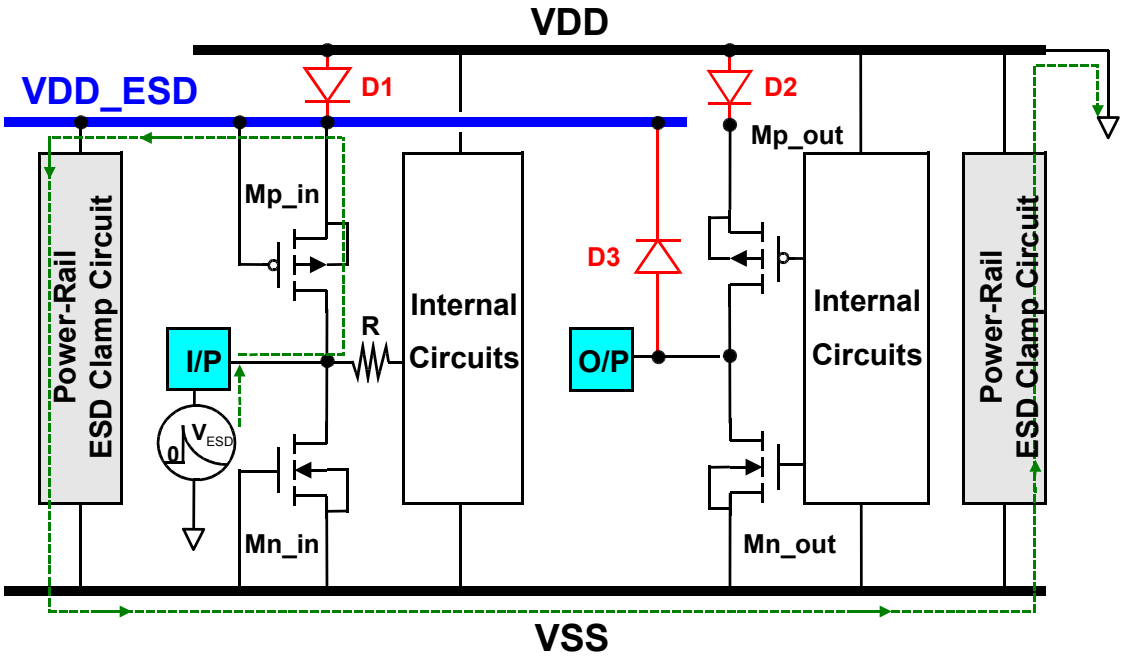


(a)

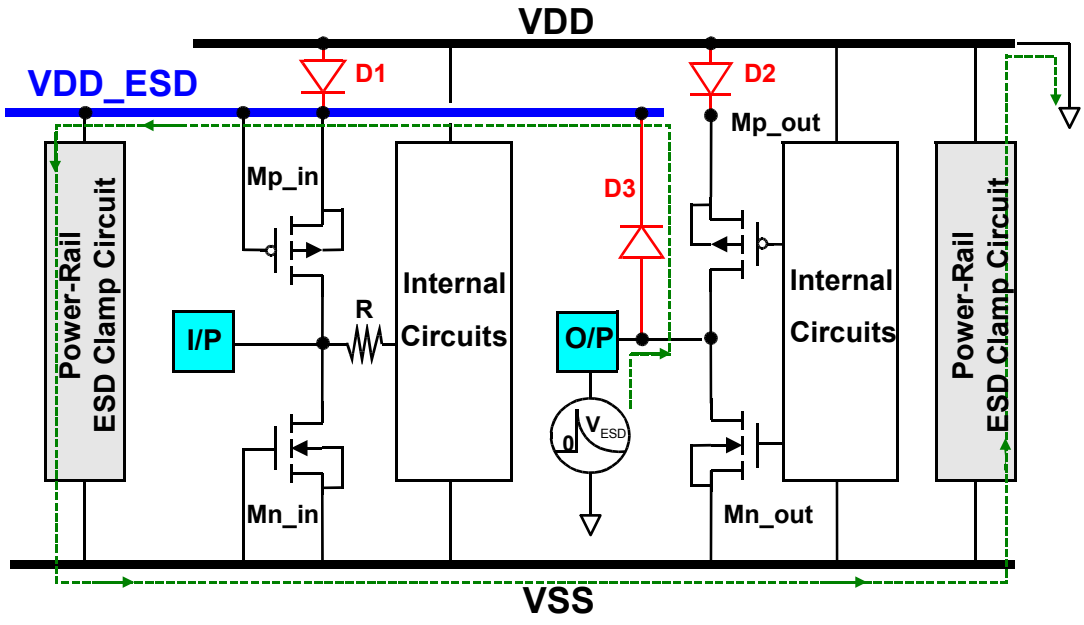


(b)

(continue to next page, **Fig. 3.2**)



(c)



(d)

Fig. 3.2 The ESD current discharging paths of (a) the input pad under PS-mode ESD stress condition, (b) the output pad under PS-mode ESD stress condition, (c) the input pad under PD-mode ESD stress condition, and (d) the output pad under PD-mode ESD stress condition.

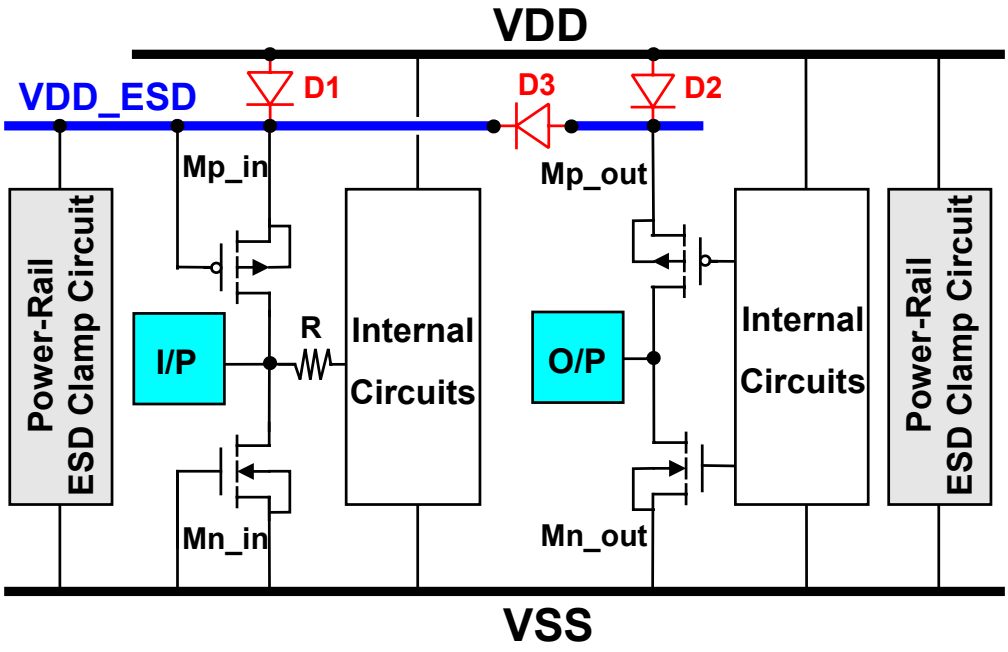


Fig. 3.3 The new proposed ESD protection scheme II for the IC with power-down-mode operation.

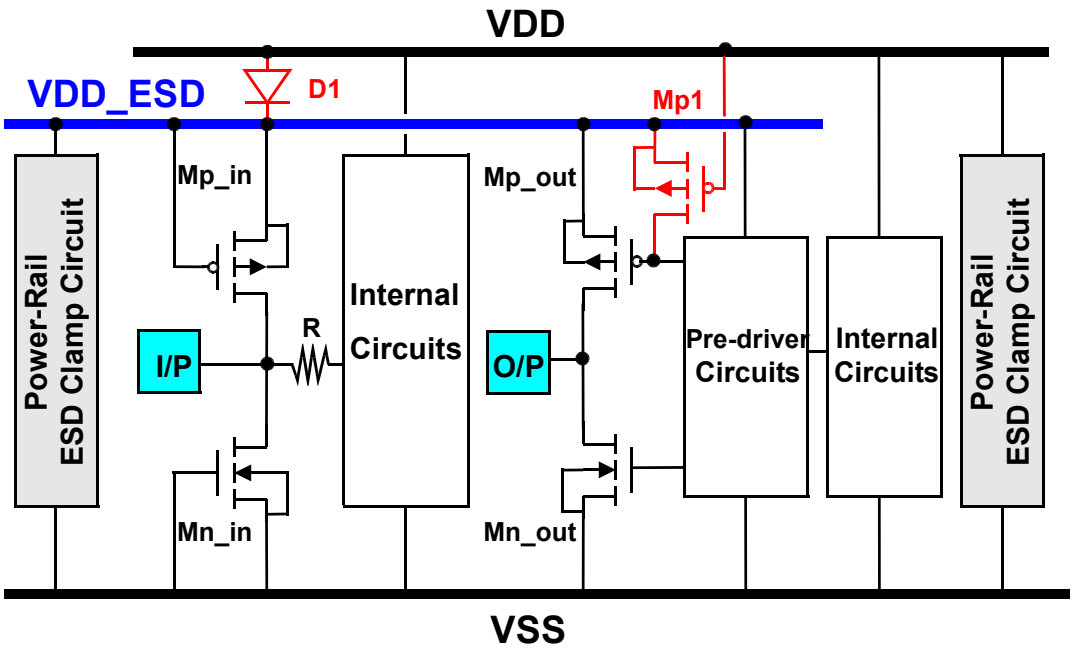


Fig. 3.4 The new proposed ESD protection scheme III for the IC with power-down-mode operation.

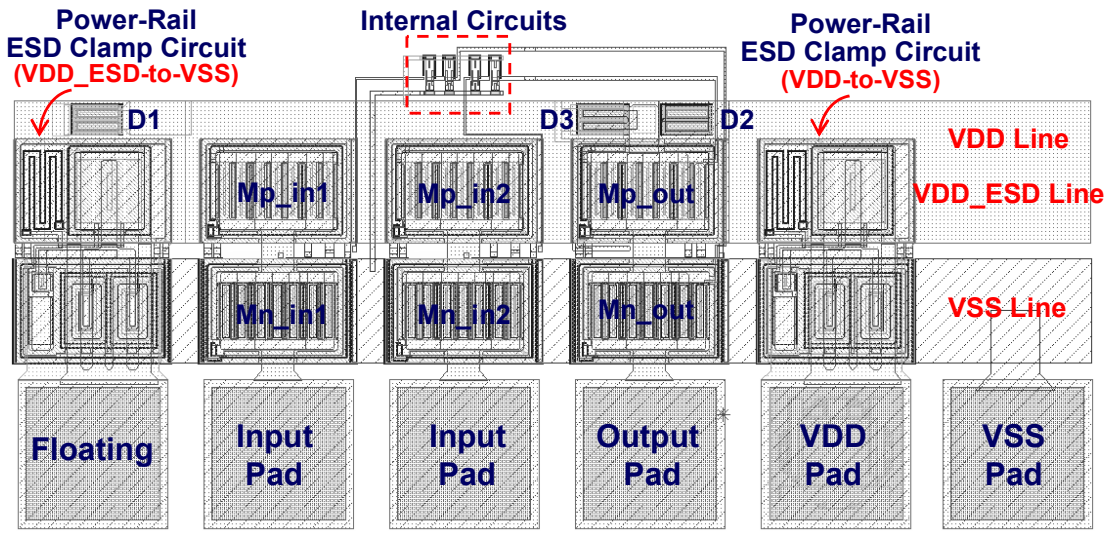


Fig. 3.5 The layout view of the new proposed ESD protection scheme I fabricated in a 0.35-μm silicided CMOS process.

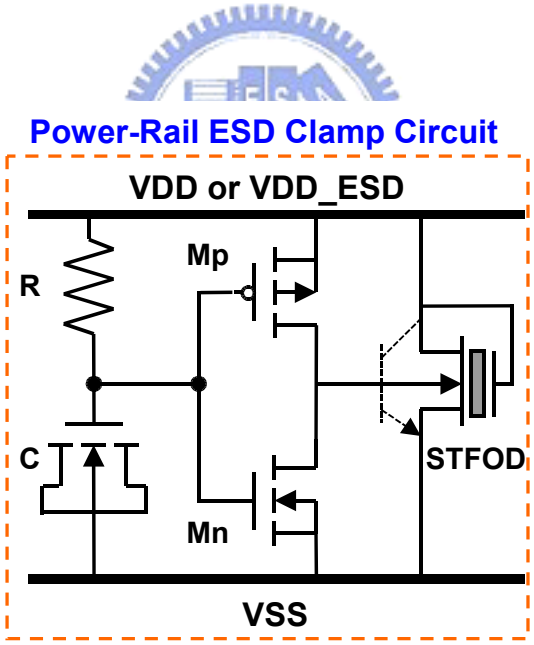
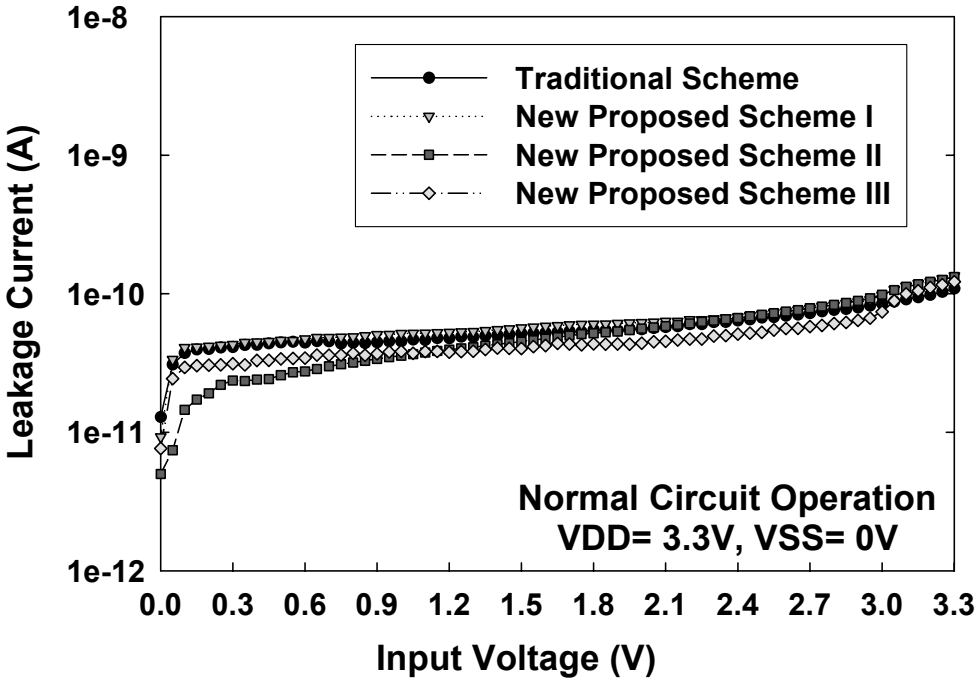
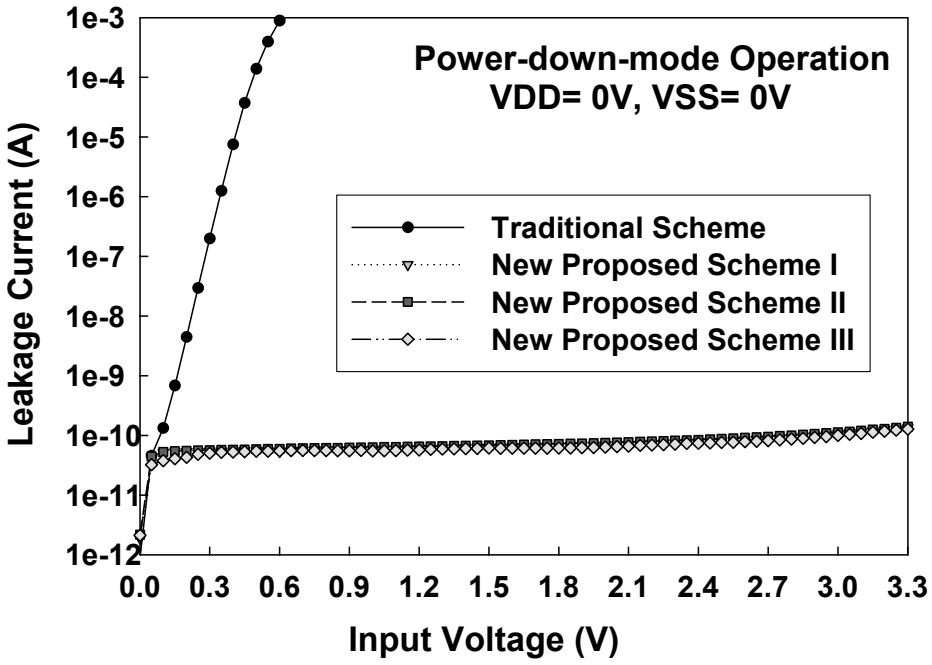


Fig. 3.6 The circuit diagram of power-rail ESD clamp circuit.

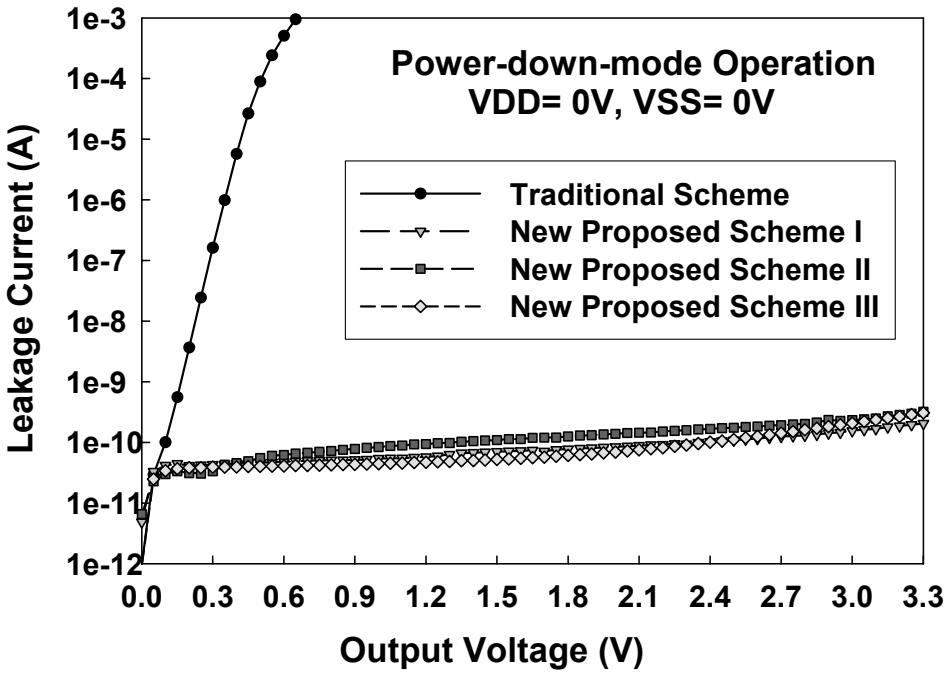


(a)



(b)

(continue to next page, **Fig. 3.7**)



(c)

Fig. 3.7 Comparison of the measured leakage currents at (a) the input pad under normal circuit operating condition, (b) the input pad under power-down-mode operating condition, and (c) the output pad under power-down-mode operating condition, of the traditional and new proposed ESD protection schemes.

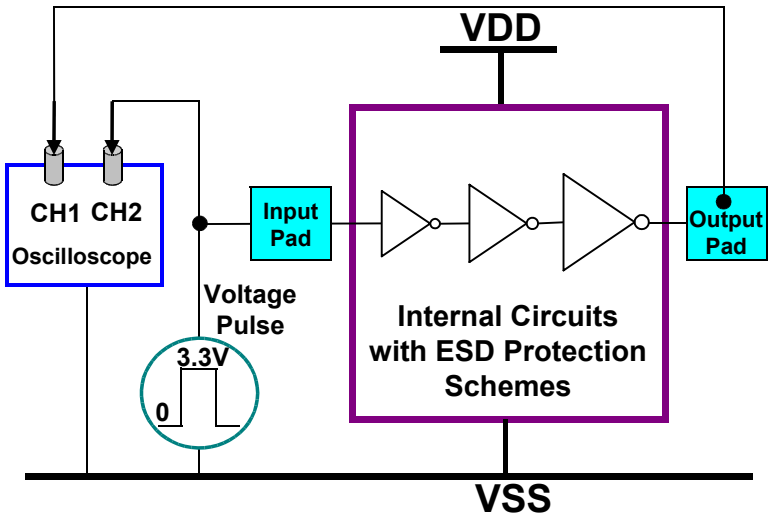
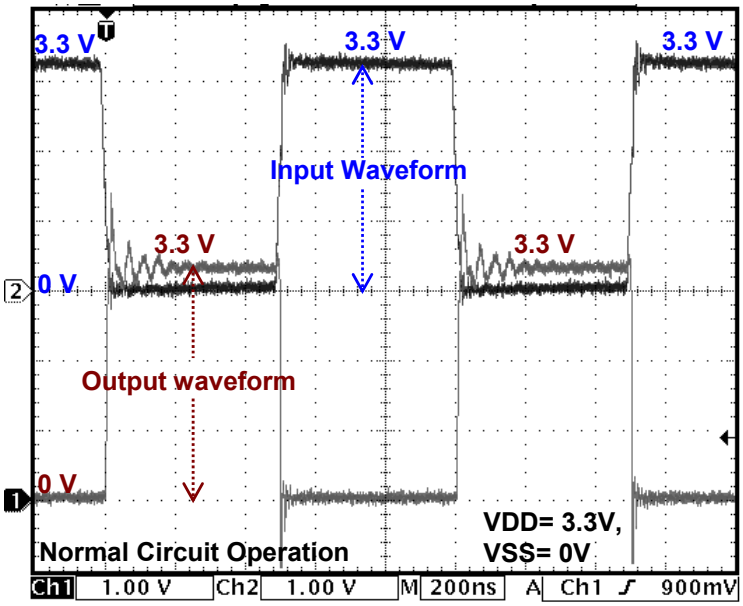
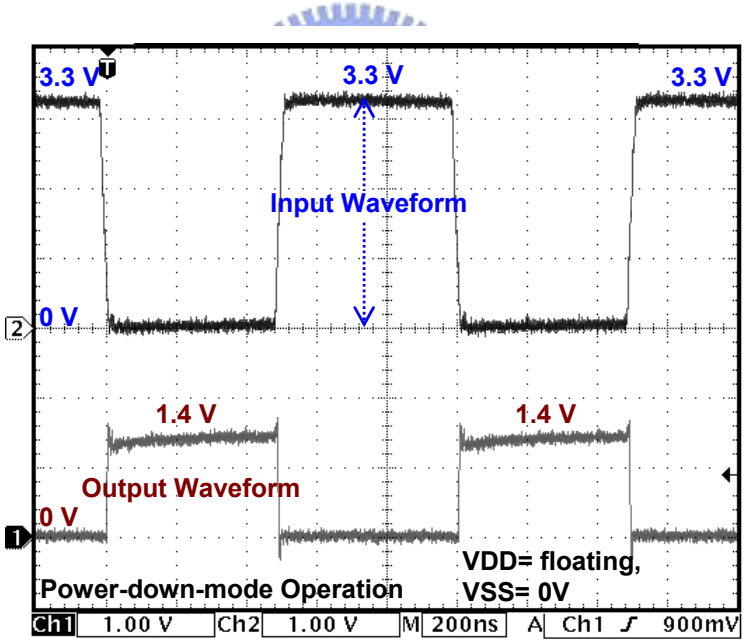


Fig. 3.8 The measurement setup to verify the function of I/O cells with the new proposed ESD protection schemes, or the traditional ESD protection scheme, under normal circuit operating condition and power-down-mode operating condition.

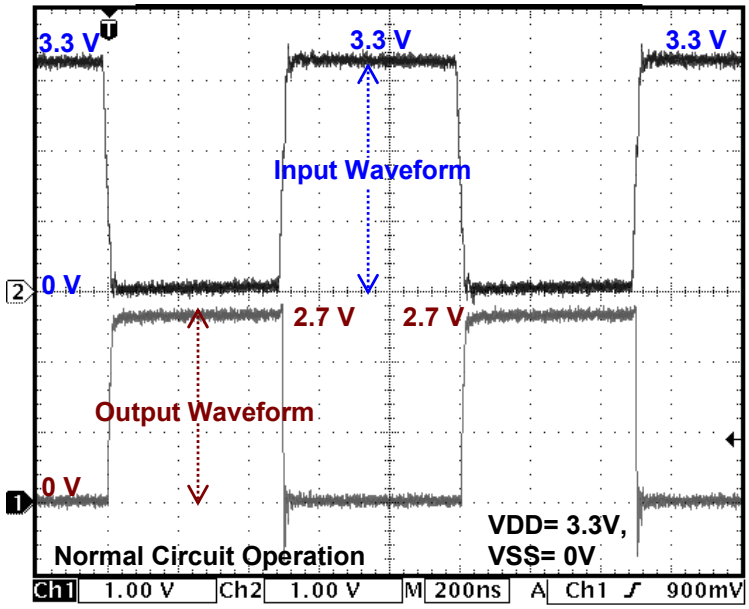


(a)

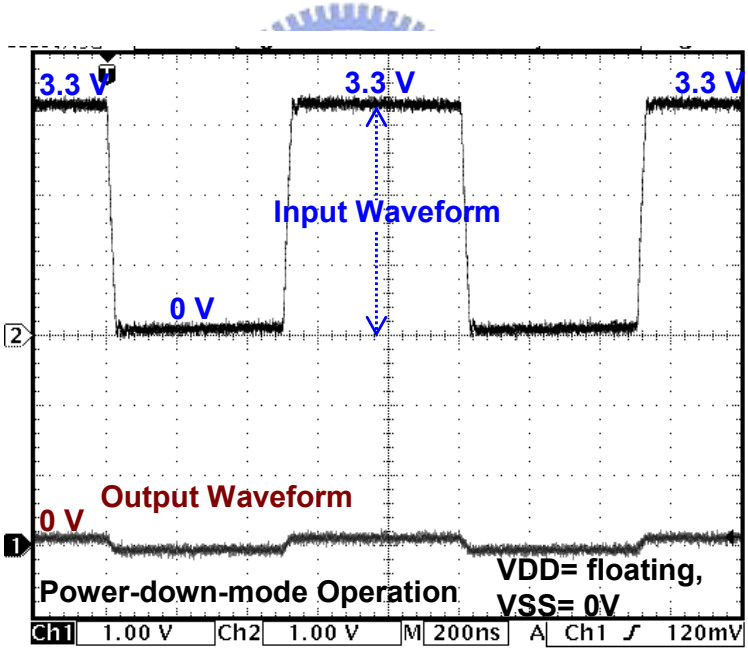


(b)

Fig. 3.9 The measured voltage waveforms on the input/output pad of IC with the traditional ESD protection scheme under (a) normal circuit operating condition with VDD= 3.3V and VSS= 0V, and (b) power-down-mode operating condition with VDD= floating and VSS= 0V. (*Y* axis= 1V/Div., *X* axis= 200ns/Div.)

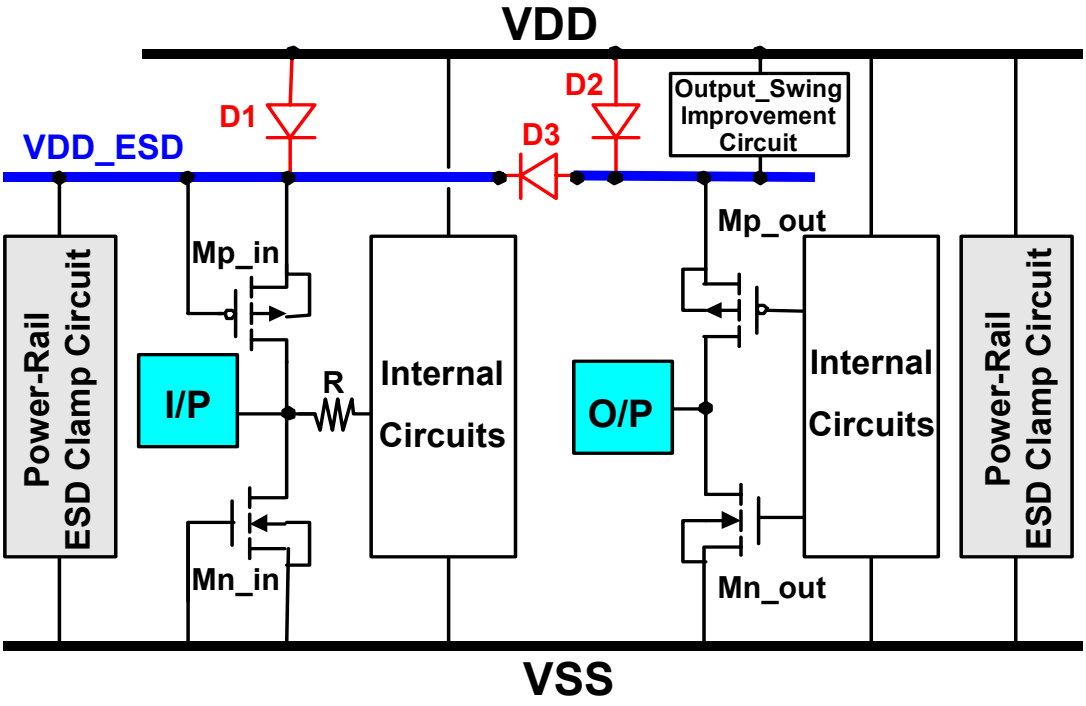


(a)

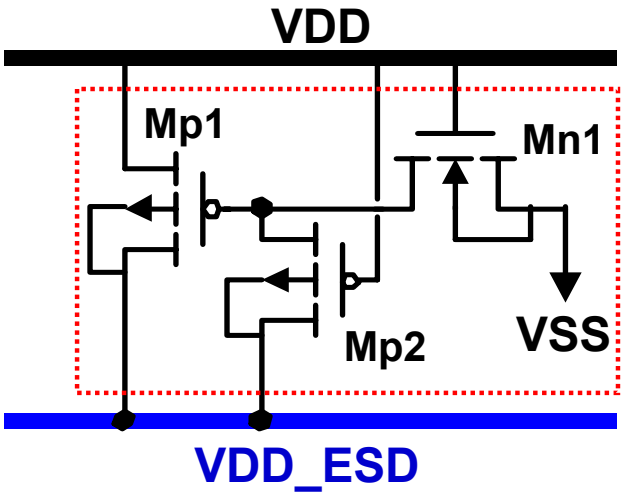


(b)

Fig. 3.10 The measured voltage waveforms on the input/output pad of IC with the proposed ESD protection scheme I under (a) normal circuit operating condition with VDD= 3.3V and VSS= 0V, and (b) power-down-mode operating condition with VDD= floating and VSS= 0V. (*Y* axis= 1V/Div., *X* axis= 200ns/Div.)



(a)



(b)

Fig. 3.11 (a) The output-swing improvement circuit connecting between the VDD power line and VDD_ESD bus line in the ESD protection scheme II. (b) The circuit diagram of output-swing improvement circuit.

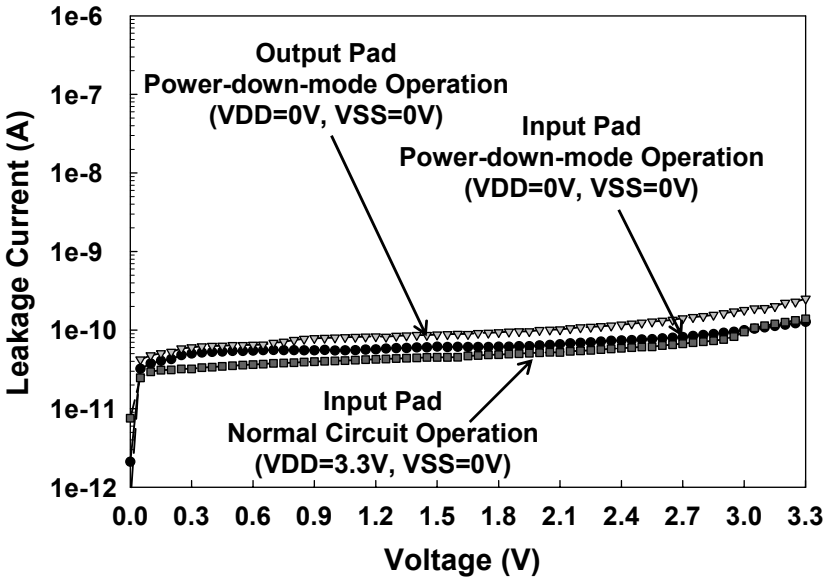
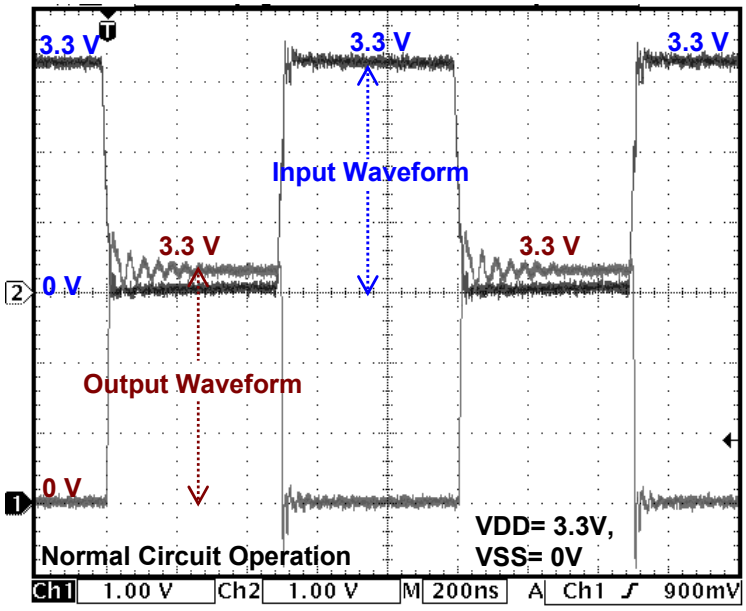
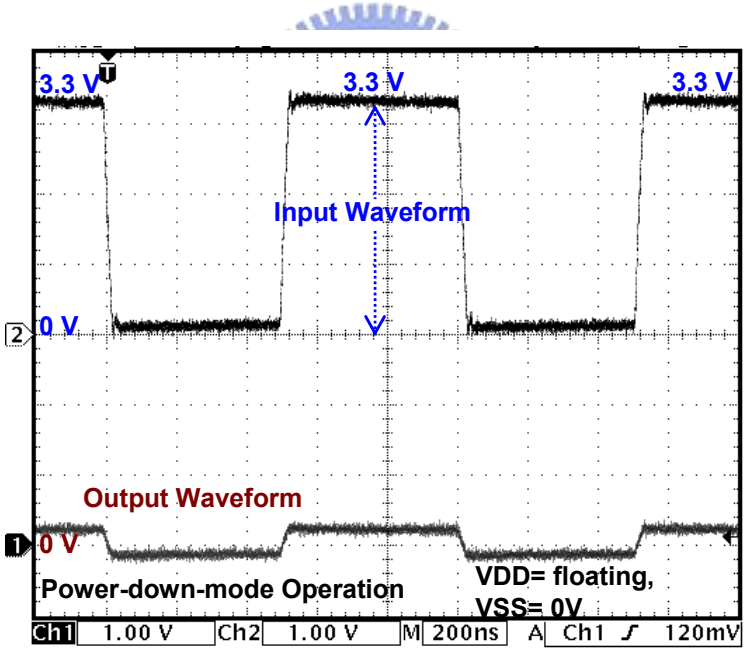


Fig. 3.12 The measured leakage currents at I/O pads of new proposed ESD protection scheme II with the output-swing improvement circuit under normal circuit operating condition and power-down-mode operating condition.



(a)



(b)

Fig. 3.13 The measured voltage waveforms on the input/output pad of the proposed ESD protection scheme II with output-swing improvement circuit under (a) normal circuit operating condition with VDD= 3.3V and VSS= 0V, and (b) power-down-mode operating condition with VDD= floating and VSS= 0V. (*Y* axis= 1V/Div., *X* axis= 200ns/Div.)

CHAPTER 4

ESD PROTECTION DESIGN IN HIGH-VOLTAGE CMOS PROCESS

When the high-voltage device is used as the power-rail ESD clamp device, the device is expected to be kept off in normal circuit operating condition. In the ESD stress condition, the ESD protection device should be triggered on to discharge ESD current. In this chapter, the double snapback characteristic in the high-voltage nMOSFETs has been investigated and analyzed by both measured and simulation results [44]. Furthermore, the holding voltage of the high-voltage devices in snapback breakdown condition has been found to be much smaller than the power supply voltage. Such characteristics will cause the high-voltage CMOS ICs susceptible to the latchup or latchup-like danger in the practical system applications, especially while these devices are used in the power-rail ESD clamp circuit. A new latchup-free design on the power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and successfully verified in a 0.25-μm 40-V CMOS process to achieve the desired ESD level [45], [46].

4.1 Double Snapback Characteristics in High-Voltage NMOSFETs

4.1.1 Double-Snapback Characteristics

The DDD (Double Diffused Drain) MOS structure fabricated in a 0.35-μm 18-V CMOS process and LDMOS (Lateral Diffused MOS) structure fabricated in a 0.25-μm 40-V CMOS process are studied in this work. The TLP system with a pulse width of 100 ns and a rise time of ~10 ns [75] is used to measure the snapback I-V curves of the fabricated 18-V and 40-V nMOSFET devices. The TLP-measured I-V characteristics of 18-V and 40-V gate-grounded nMOS (GGNMOS) devices are shown in Figs. 4.1(a) and 4.1(b), respectively. The corresponding cross-sectional view of the device structure is also shown in the inset of the

figure. From the measured results, the double-snapback characteristics are found both in 18-V nMOSFET and 40-V nMOSFET. For the 18-V nMOSFET shown in Fig. 4.1(a), after the first snapback voltage at 22.2 V, the device snaps back to 8.5 V. Then, the device quickly goes into the second snapback, and the voltage drops to only ~5 V. The slope of the snapback curves is almost the same at first and second snapback states. For the 40-V nMOSFET shown in Fig. 4.1(b), after the first snapback voltage at 27.2 V (52 V in dc), the device snaps back to 23 V, from where the voltage strongly increases again. Then, the device goes into the second snapback, and the voltage drops to only ~7 V. In 40-V nMOSFET, the turn-on resistance of the first snapback state is much larger than that of the second snapback state.

4.1.2 Simulations and Analysis

The first snapback mechanism involves both avalanche breakdown and turn-on of the parasitic bipolar transistor [78]. For 40-V nMOSFET, the avalanche generation is initiated by the n+ buried layer (NBL)/p-well junction. Fig. 4.2(a) shows the current distribution in the 40-V nMOSFET under first snapback state, where the current path flows vertically into the NBL region. Due to the longer current path through lightly doped well region, the turn-on resistance is large at the first snapback state, as that shown in Fig. 4.2(b). When the current further increases, the device enters into high-injection condition and the Kirk effect [79] occurs. The base push-out effect causes the maximum electric field to change from the NBL/p-well junction to the n+/n-well junction. Due to higher multiplication rate at this higher doped region, a strong snapback occurs to cause a low holding voltage. Fig. 4.2(b) shows the current distribution in the 40-V nMOSFET under the second snapback state. The current path changes from the vertical direction to the lateral direction, when the device switches from the first to the second snapback state. The turn-on resistance becomes much smaller when the current path flows in the lateral direction. For 18-V nMOSFET, the avalanche generation is initiated by the n-diffused-drain (NDD)/p-well junction. With shallower NDD diffusion in the device structure, the current path basically flows in the lateral direction at the first and second snapback states. Therefore, the turn-on resistance is almost the same at these two states. In addition, with shallower NDD diffusion, the first snapback state could be not obvious, because the maximum electric field changes from the NDD/p-well junction to the n+/NDD junction quickly.

The doping concentration and junction depth of lightly doped drain region (NDD for 18-V

nMOSFET and n-well for 40-V nMOSFET) are the major factors to influence double snapback characteristics. Because these factors directly affect the process of base push-out effect, which changes the maximum electric field from initial avalanche breakdown region to the n+/n- region. The increase of doping concentration and junction depth of lightly doped drain region will delay space-charge region edge moving toward n+/n- region, and therefore delay the device into the second snapback state.

4.2 High-Voltage ESD Protection Devices

4.2.1 TLP I-V Characteristics

Besides high-voltage nMOSFET device, SCR device, field-oxide (FOD) device, and high-voltage pMOSFET device fabricated in a 0.25-μm 40-V CMOS process are also studied in this work. The layout parameters of such ESD protection devices are drawn according to the foundry's ESD rules with the silicide-blocking mask. The cross-sectional views and TLP-measured I-V characteristics of high-voltage gate-grounded nMOS (GGNMOS) device, SCR device, FOD device, and gate-VDD pMOS (GDPMOS) device are shown in Fig. 4.3 - Fig. 4.6, respectively. For high-voltage GGNMOS device in Fig. 4.3 The second breakdown current (It2) of GGNMOS device with 200-μm channel width is 2.7A. For high-voltage SCR device in Fig. 4.4(a), the characteristic of very low holding voltage and high ESD robustness has been found. As shown in Fig. 4.4(b), the holding voltage of SCR device is only ~4V and the It2 current of SCR device with 200-μm width is over 6A. For high-voltage FOD device structure shown in Fig. 4.5(a), the device is isolated by the n+ buried layer (NBL) from the common p-type substrate. The spacing from collector diffusion to emitter diffusion of FOD device is 6μm in this study. As shown in Fig. 4.5(b), the TLP-trigger voltage is 19.7V (50V in DC), and the holding voltage is ~16V. The It2 current of FOD device with 200-μm width is 0.5A. The difference on trigger voltages of the device measured by DC (HP4155) and TLP is caused by the transient-coupling effect through the parasitic capacitance of the device. The TLP is designed with a rise time of 10ns to simulate the HBM ESD event. The dV/dt transient voltage at the zapping node could be coupled into the device through the parasitic capacitance in the drain/bulk junction to lower the trigger voltage. For high-voltage GDPMOS device in Fig. 4.6(a), no snapback characteristic is found. The holding voltage of the device is larger than the supply voltage of 40V. Due to the inefficient parasitic p-n-p bipolar action, the It2

current of GDPMOS device with 200-μm channel width is only 0.06A, as that shown in Fig. 4.6(b). Therefore, GDPMOS is not suitable for on-chip ESD protection device in high-voltage CMOS ICs due to too low ESD robustness.

4.2.2 Transient Latchup Test

Transient latchup (TLU) test is used to investigate the susceptibility of the ESD protection devices to the noise transient or glitch on the power lines during normal circuit operating condition. The measurement setup for TLU test is shown in Fig. 4.7. The positive or negative charging voltage (Vcharge) on the energy storage capacitor (C1) generating the transient is used to trigger the device into the latch state [80]. A supply voltage of 40V was used to bias the device as normal circuit operating condition. The transient trigger source was connected directly to the device-under-test (DUT). The small resistance (R1) is used to protect the DUT, when the DUT is triggered on into the latch state. In addition, the diode (D1) in Fig. 4.7 is used to avoid the damage to the power supply during TLU test [80]. The voltage waveform on the DUT (at node Y) during TLU test is monitored by a digital oscilloscope with a sampling rate of 5G Hz in this experiment. The measured voltage waveforms on high-voltage GGNMOS device, SCR device, and FOD device under TLU test are shown in Fig. 4.8 - Fig. 4.10, respectively.

From the measured results, the devices are initially kept off before the transient trigger, therefore the voltage waveforms are initially kept at 40V. After the transient trigger, the snapback characteristic in the device can be triggered on to generate a low-holding-voltage state. The clamped voltage level of the devices in snapback breakdown condition is consistent with the holding voltage measured by TLP stress. In Fig. 4.8, the clamped voltage level of high-voltage GGNMOS device is ~7V due to the transient triggering with the capacitor charging voltage of 55V. The GGNMOS device is triggered into the second snapback state directly by the transient pulse. If such high-voltage nMOSFET is used in the power-rail ESD clamp circuit, the latchup-like issue between the power rails will occur, when the high-voltage nMOSFET is triggered on by the noise transient on the power lines.

In Fig. 4.9, the clamped voltage level of high-voltage SCR device is only ~4V due to the transient triggering with the capacitor charging voltage of only 44V. Although SCR device has the advantage of high ESD robustness, the latchup issue in high-voltage CMOS ICs becomes worse. Figs. 4.10(a) and 4.10(b) show the measured voltage waveforms of

high-voltage FOD device under TLU test with positive and negative charging voltages, respectively. Both positive and negative charging voltages can trigger the FOD device into the latch state. The clamped voltage level of FOD device is ~16V due to the transient triggering with the capacitor charging voltage of 47V or -10V. For negative charging voltage, the parasitic N-well/p-substrate junction between the power rails may be turned on initially, but it is turned off quickly due to the transient ringing voltage waveform. Finally, the FOD device is triggered into the holding state. Latchup-like issue is the concern by using single FOD device as the power-rail ESD clamp in high-voltage CMOS ICs.

From the power dissipation view, the device with a lower holding voltage is helpful to sustain much higher ESD current. However, the device may be triggered on by the noise transient or glitch on the power lines during normal circuit operating condition, especially under the system-level EMC/ESD zapping test. If the holding voltages of high-voltage ESD protection devices are smaller than the power supply voltage of normal circuit operating condition, the high-voltage CMOS ICs will be susceptible to the latchup or latchup-like danger in the system applications, which often meet the noise or transient glitch issues.

4.3 Design of Latchup-Free Power-Rail ESD Clamp Circuits

The NMOS and SCR devices have higher It2 than that of FOD device, but their holding voltages (~7V in NMOS, ~4V in SCR) are far away from the 40-V operating voltage level. Such ESD protection devices with low holding voltage in power-rail ESD clamp circuits will cause serious latchup failure to high-voltage CMOS ICs. To overcome the latchup or latchup-like issue between the power rails in high-voltage CMOS ICs, a new stacked-field-oxide structure has been designed to increase the total holding voltage. The stacked-field-oxide structure with two cascaded FOD devices has been fabricated in a 0.25-μm 40-V CMOS process. The I-V characteristic and ESD robustness of stacked-field-oxide structure has been investigated by the TLP stress. The susceptibility of stacked-field-oxide structure to the noise transient during normal circuit operating condition has also been performed by the TLU test. Finally, a latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure is proposed and verified.

4.3.1 TLP I-V Characteristics

The measurement setup of single high-voltage FOD device and stacked-field-oxide structure under TLP stress is shown in Fig. 4.11(a). The TLP-measured I-V characteristics of these devices with different device widths are compared in Fig. 4.11(b). From the measured results, the holding voltage of stacked-field-oxide structure in snapback region is double of that of single FOD device. Therefore, the holding voltage of stacked-field-oxide structure can be linearly increased by increasing the numbers of cascaded FOD devices. The It2 currents of single FOD device and stacked-field-oxide structure as a function of device channel width are compared in Fig. 4.12. The It2 current of stacked-field-oxide structure is linearly increased while the device channel width increases. In addition, the It2 current of stacked-field-oxide structure is only slightly degraded as compared with that of single FOD device. The relation between the It2 and HBM ESD level, V_{ESD}, can be approximated as

$$V_{ESD} \cong (1500 + R_{ON}) \times It2, \quad (1)$$

where R_{ON} is the dynamic turn-on resistance of the device under test. From Fig. 4.12, the stacked-field-oxide structure with a device width of ~650μm for each FOD device can sustain the typical 2-kV (It2 of ~1.33A) HBM ESD stress. To meet the specified ESD level of driver ICs, it can be achieved by adjusting the device width of the stacked-field-oxide devices.

The trigger voltage of stacked-field-oxide structure is increased as compared with that of single FOD device. The substrate-triggered technique [56]-[58] can be applied to lower the trigger voltage of the device to ensure effective ESD protection. The TLP-measured I-V curves of the stacked-field-oxide structure with different substrate-triggered currents (Itrig) are shown in Fig. 4.13. From the measured results, the trigger voltage of the stacked-field-oxide structure is obviously decreased while the substrate-triggered current is applied. The trigger voltage can be reduced to only 17V when the substrate-triggered current is 10mA. Therefore, the trigger voltage of stacked-field-oxide structure can be effectively reduced lower than the breakdown voltage of internal circuits by substrate-triggered technique. Moreover, the It2 level of the stacked-field-oxide structure with substrate-triggered current can be improved [78].

4.3.2 Transient Latchup Test

The measured voltage waveforms of stacked-field-oxide structure under TLU test with the transient triggering of positive and negative charging voltages are shown in Figs. 4.14(a) and

4.14(b), respectively. From the observed voltage waveforms, the stacked-field-oxide structure is triggered on due to the transient triggering with the capacitor charging voltages of 80V or -50V. But, the clamped voltage waveform quickly comes back to the original supply voltage level of 40V, without keeping in the latch state after the triggering. The measured result is consistent with TLP-measured I-V curves, as those shown in Fig. 4.11(b). The total holding voltage of stacked-field-oxide structure with two cascaded FOD devices is near the supply voltage of 40V. After the stacked-field-oxide structure is triggered on during the TLU test, the clamped voltage level can quickly restore to the supply voltage. Therefore, no latchup or latchup-like issue is occurred. In addition, a higher charging voltage stored in the capacitor (C1) is needed to trigger on the stacked-field-oxide structure during the TLU test. Therefore, the latchup immunity of stacked-field-oxide structure to the noise transient on the power lines in high-voltage CMOS ICs has been significantly improved.

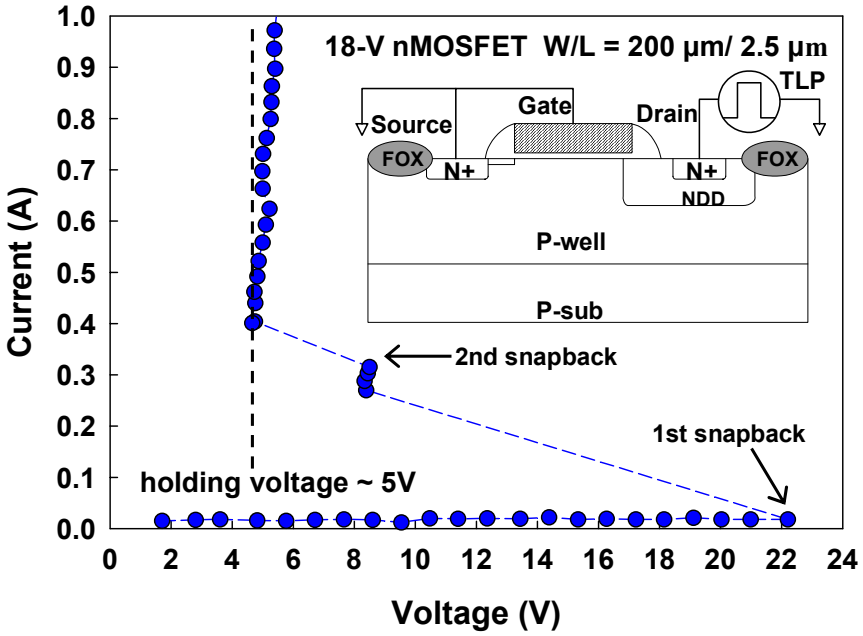
4.3.3 Latchup-Free Power-Rail ESD Clamp Circuits

The proposed power-rail ESD clamp circuits with two cascaded FOD devices and three cascaded FOD devices in high-voltage CMOS ICs are shown in Figs. 4.15(a) and 4.15(b), respectively. The substrate-triggered technique is achieved by the RC-based ESD detection circuit [76]. The trigger voltage of stacked FOD devices can be decreased to quickly discharge ESD current by the substrate-triggered technique [76]. The latchup immunity of power-rail ESD clamp circuit to the noise transient can be highly increased by the stacked-field-oxide structure. By adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process. Latchup-free power-rail ESD clamp circuit can be achieved for the IC applications with power supply of 40V.

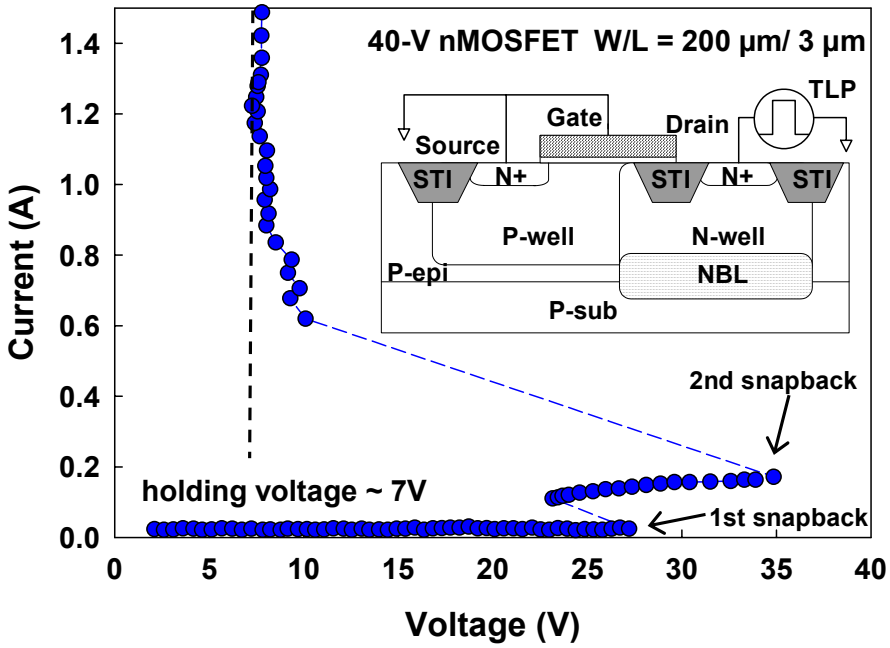
4.4 Summary

Latchup or latchup-like issue of ESD protection devices in high-voltage CMOS ICs has been clearly investigated by TLP stress and TLU test. The impact of low holding voltage of ESD protection devices to cause the LCD driver ICs susceptible to latchup or latchup-like

danger during normal circuit operating condition has been shown. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage without using extra process modification in the high-voltage CMOS technology. For the IC applications with power supply of 40V, a new latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure has been designed and successfully verified in a 0.25-μm 40-V CMOS process to meet the desired ESD level.

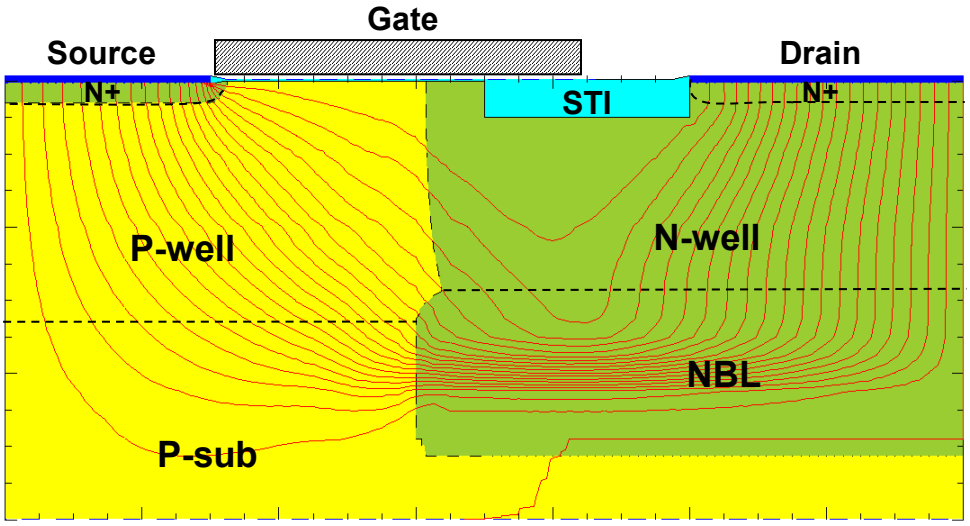


(a)

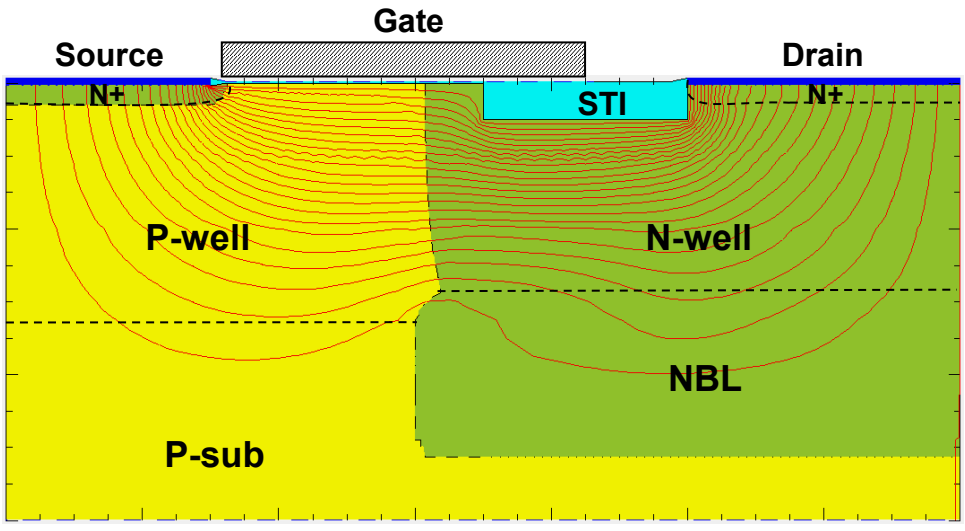


(b)

Fig. 4.1 The TLP-measured I-V characteristics of (a) DDD MOS structure fabricated in a 0.35-μm 18-V CMOS process and (b) LDMOS structure fabricated in a 0.25-μm 40-V CMOS process.

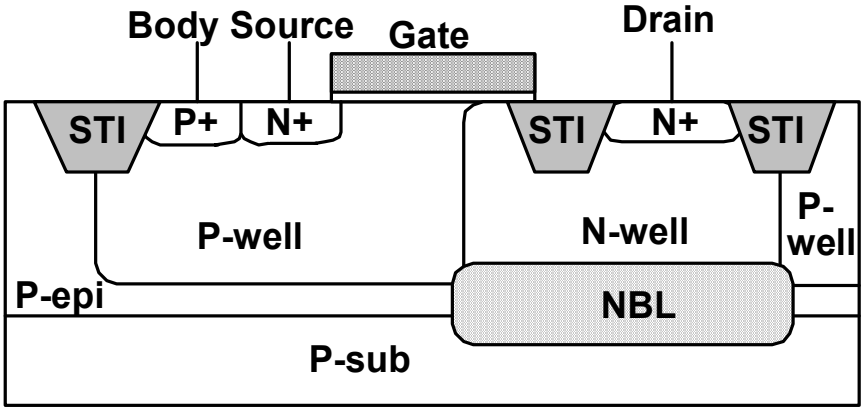


(a)

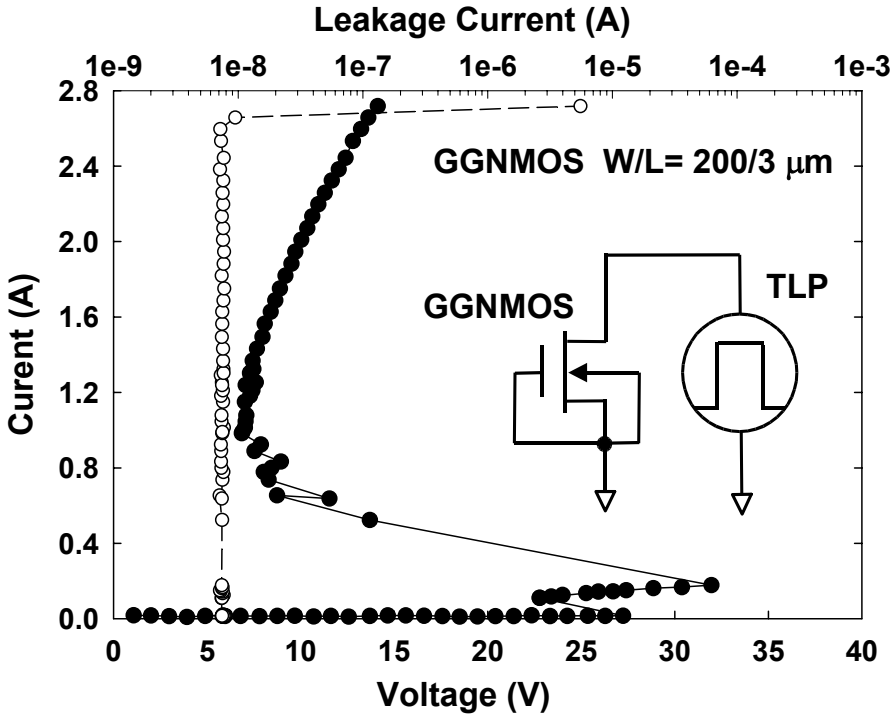


(b)

Fig. 4.2 Simulated current distributions in the 40-V nMOSFET under the (a) first snapback state, and (b) second snapback state.

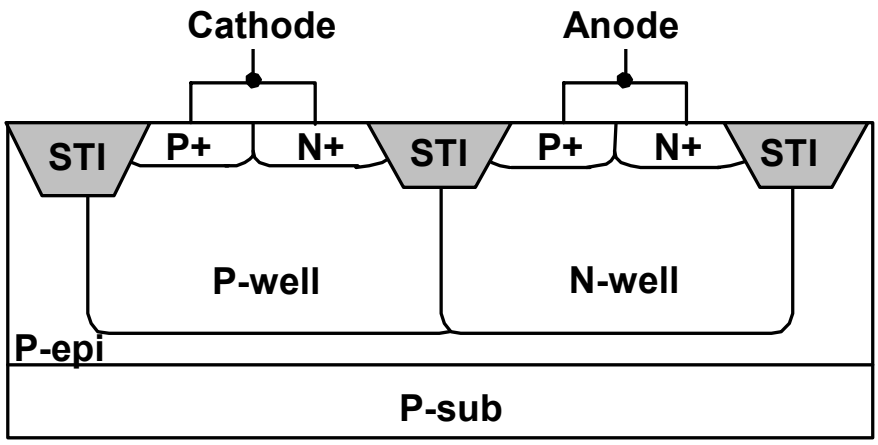


(a)

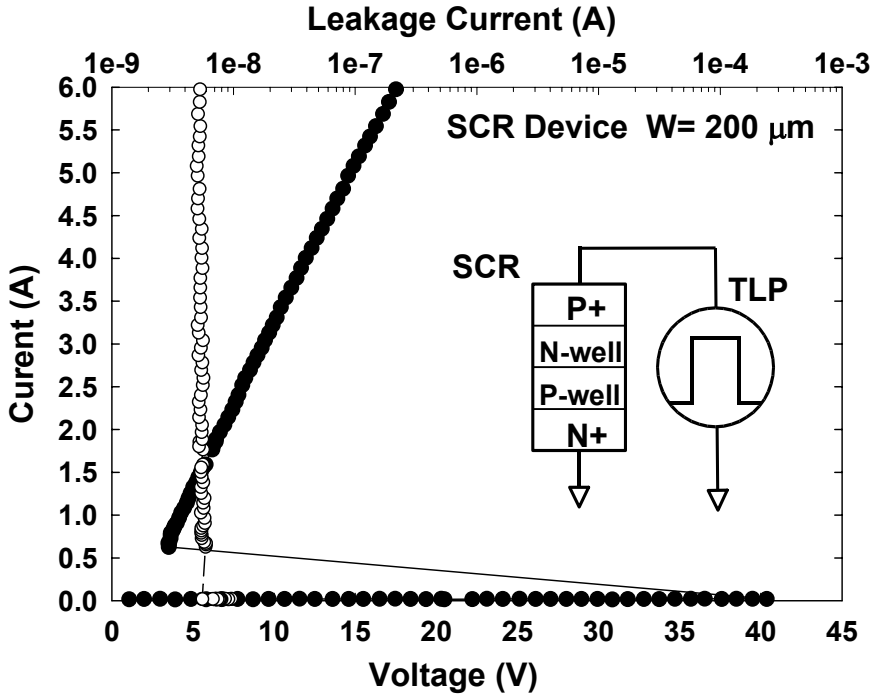


(b)

Fig. 4.3 The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage gate-grounded nMOS (GGNMOS) device fabricated in a 0.25-μm 40-V CMOS process.

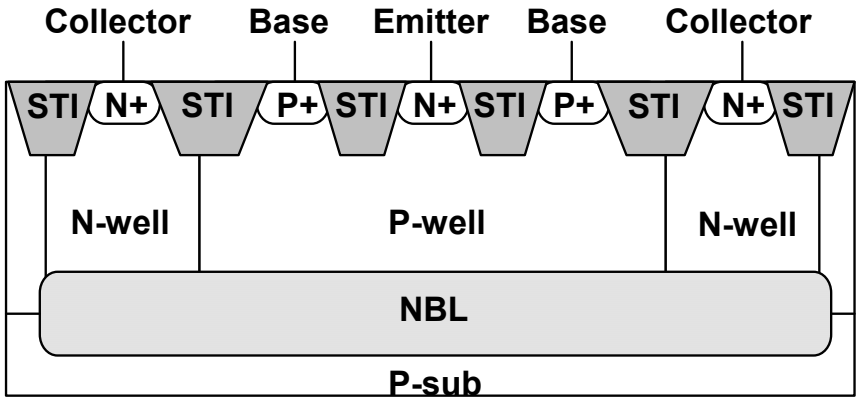


(a)

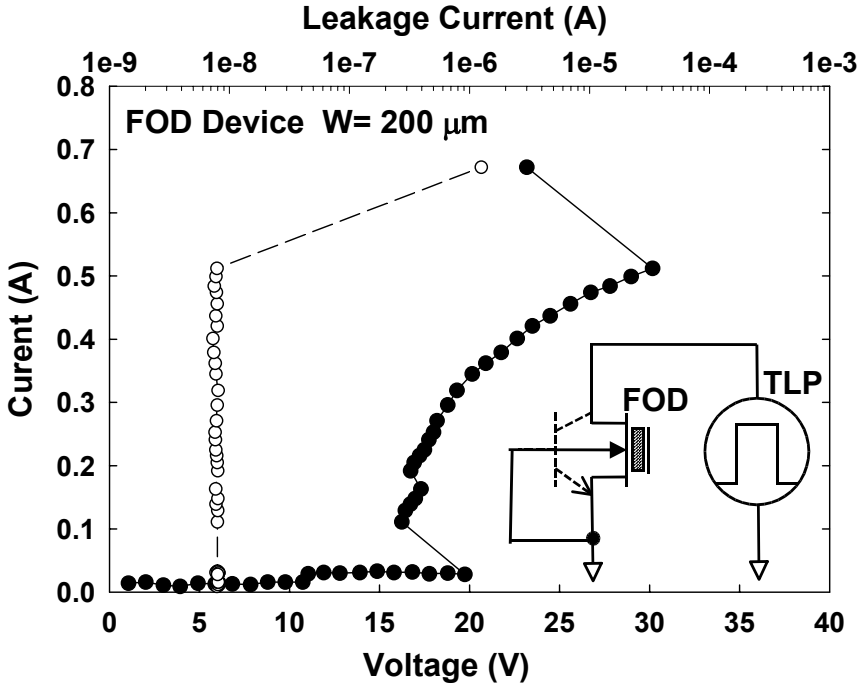


(b)

Fig. 4.4 The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage silicon controlled rectifier (SCR) device fabricated in a 0.25-μm 40-V CMOS process.

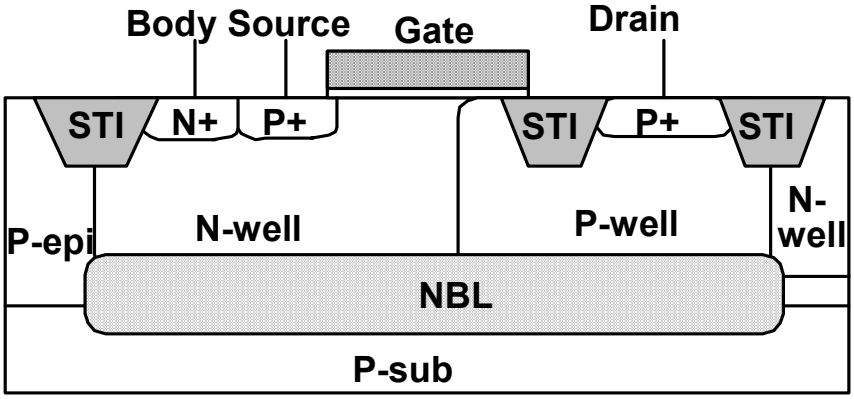


(a)

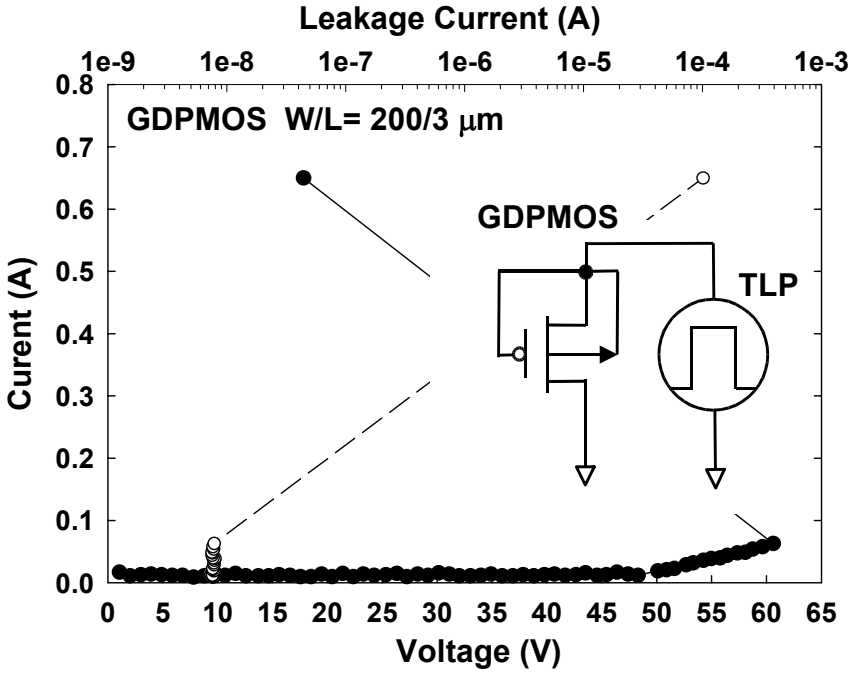


(b)

Fig. 4.5 The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage field-oxide (FOD) device fabricated in a 0.25-μm 40-V CMOS process.



(a)



(b)

Fig. 4.6 The (a) cross-sectional view, and (b) TLP-measured I-V characteristic, of high-voltage gate-VDD pMOS (GDPMOS) device fabricated in a 0.25-μm 40-V CMOS process.

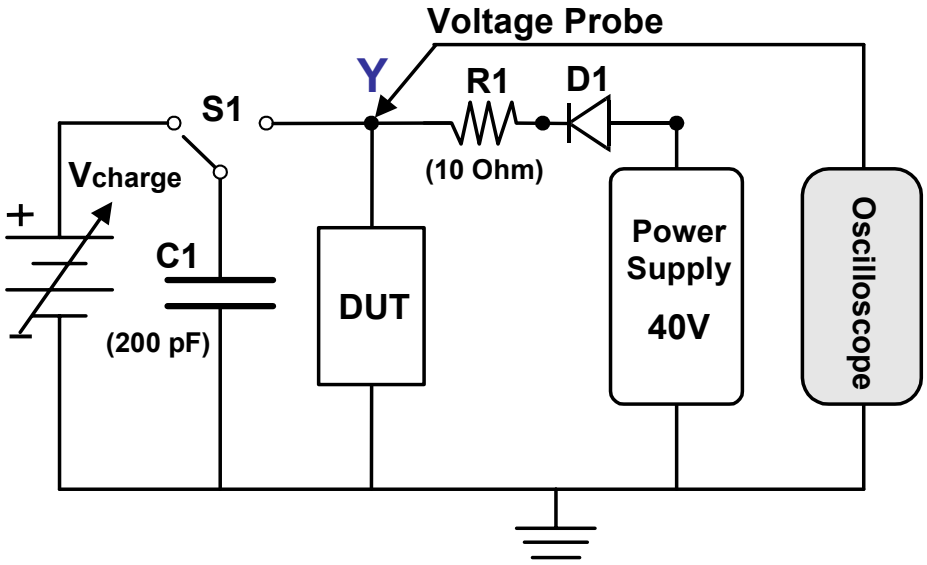


Fig. 4.7 The measurement setup for transient latchup (TLU) test.

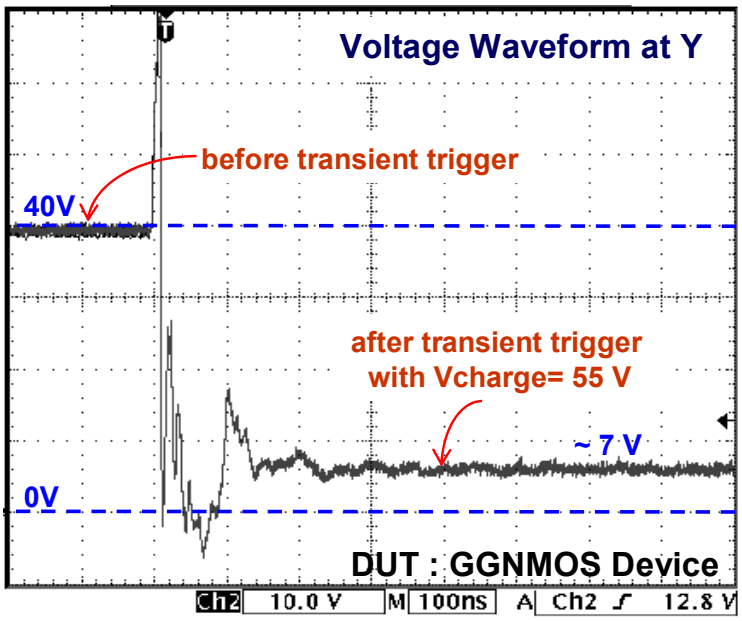


Fig. 4.8 The measured voltage waveform on the high-voltage GGNMOS device under TLU test. (*Y* axis= 10 V/Div., *X* axis= 100 ns/Div.)

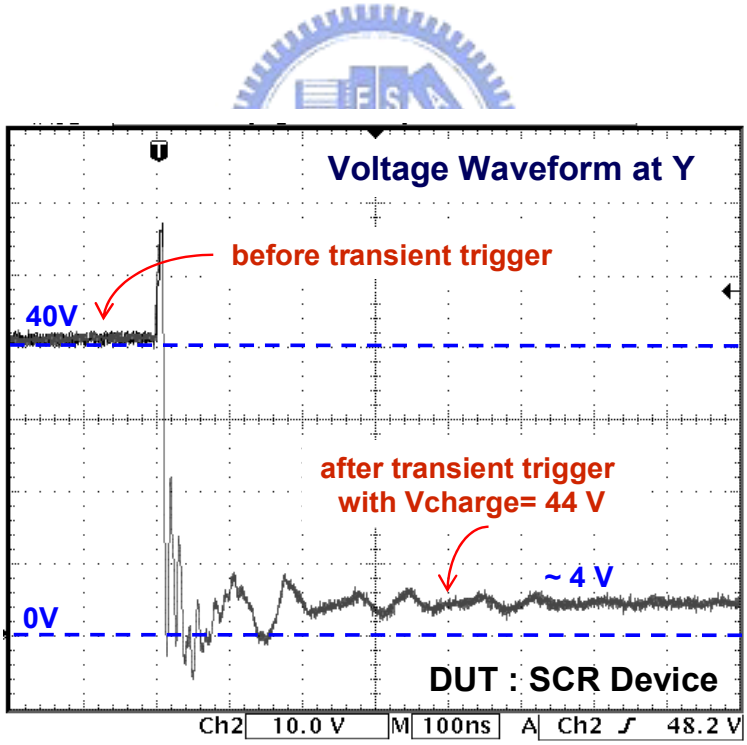
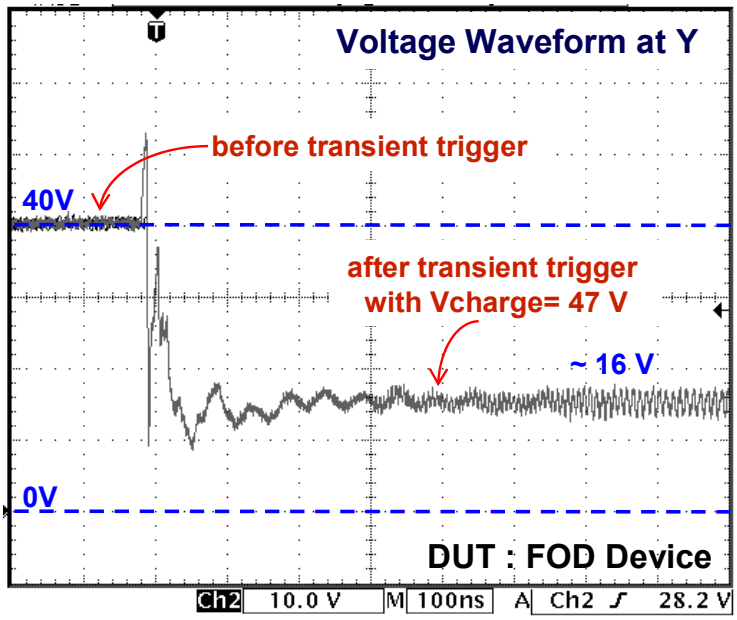
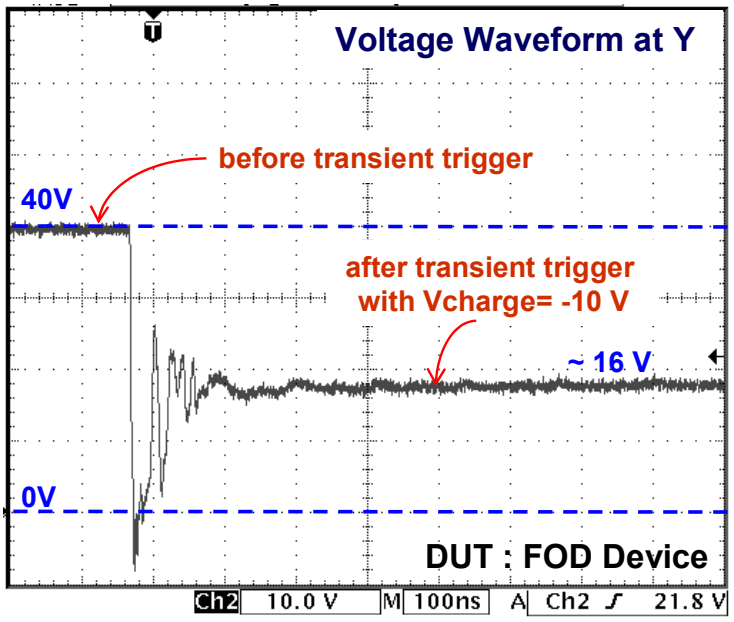


Fig. 4.9 The measured voltage waveform on the high-voltage SCR device under TLU test. (*Y* axis= 10 V/Div., *X* axis= 100 ns/Div.)

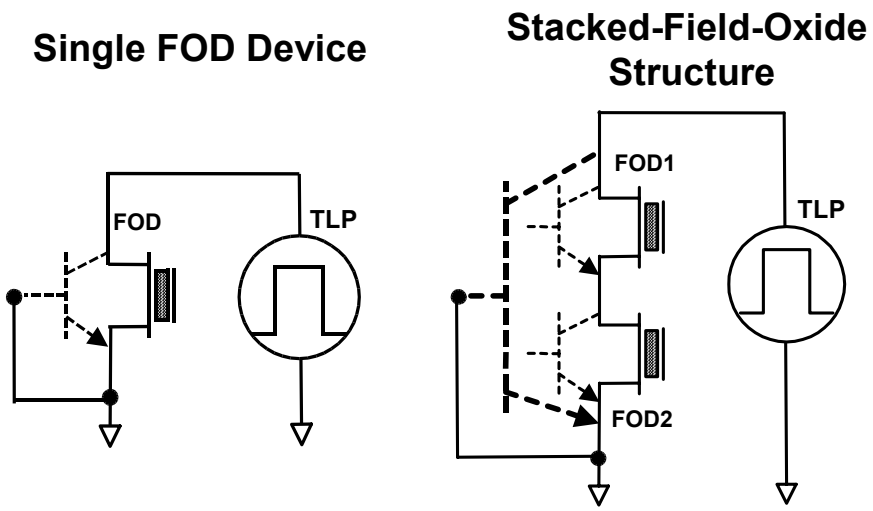


(a)

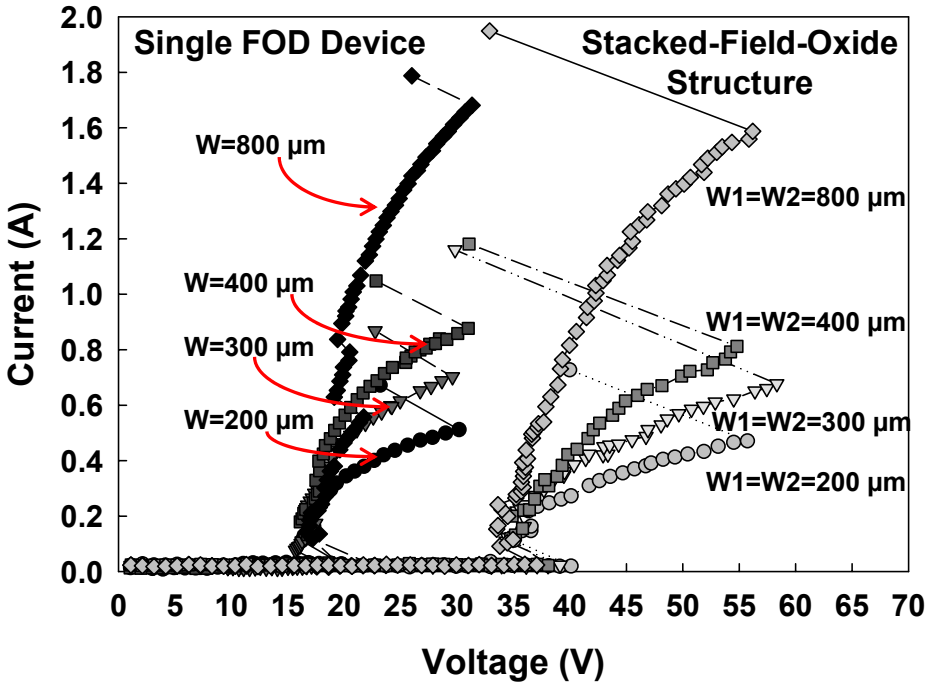


(b)

Fig. 4.10 The measured voltage waveforms on the high-voltage FOD device under TLU test with (a) positive charging voltage, and (b) negative charging voltage. (*Y* axis= 10 V/Div., *X* axis= 100 ns/Div.)



(a)



(b)

Fig. 4.11 (a) The measurement setup of single high-voltage FOD device and stacked-field-oxide structure under TLP stress. (b) The TLP-measured I-V characteristics of these devices with different device widths. W1 is the channel width of FOD1, and W2 is the channel width of FOD2.

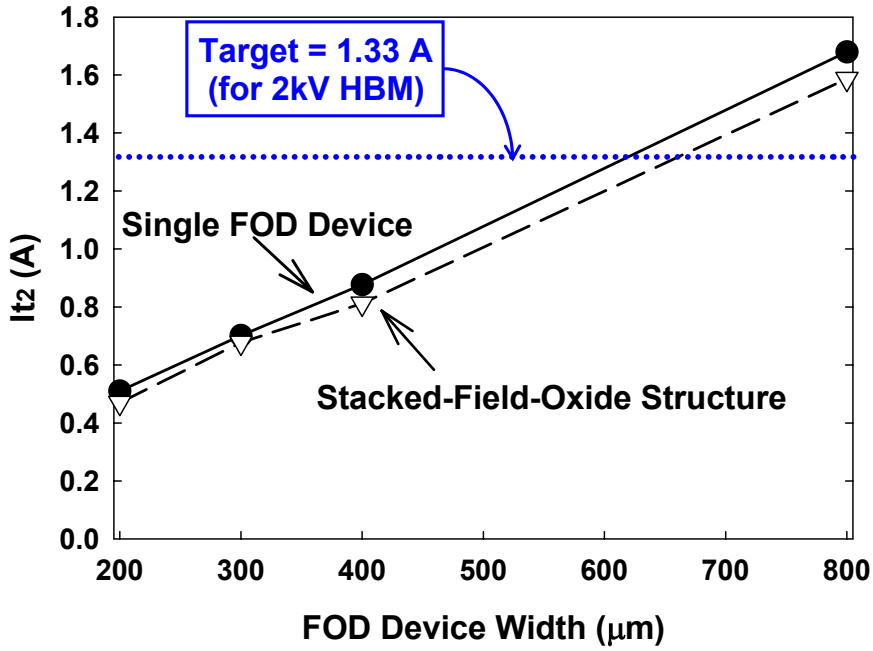


Fig. 4.12 It2 currents of single FOD device and stacked-field-oxide structure as a function of device channel width.

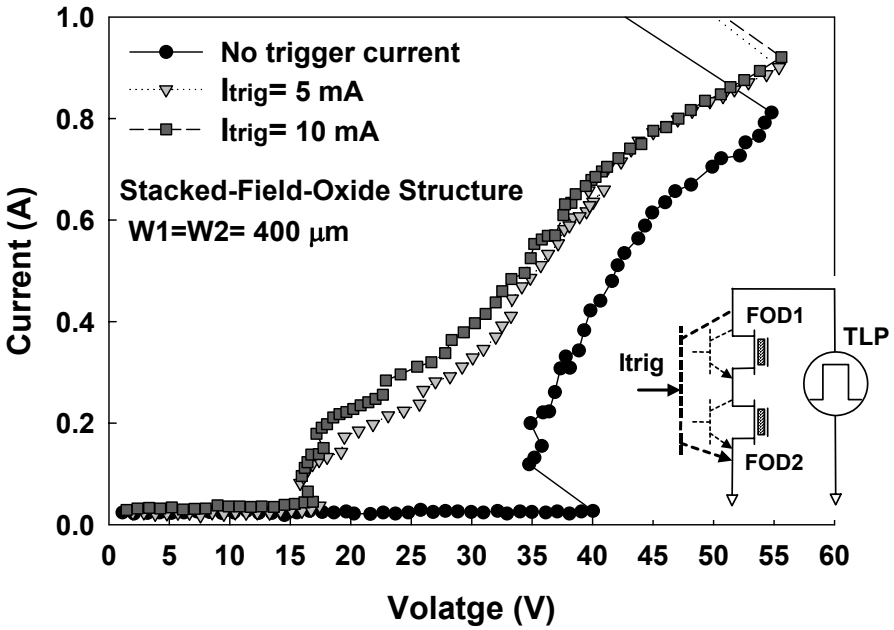
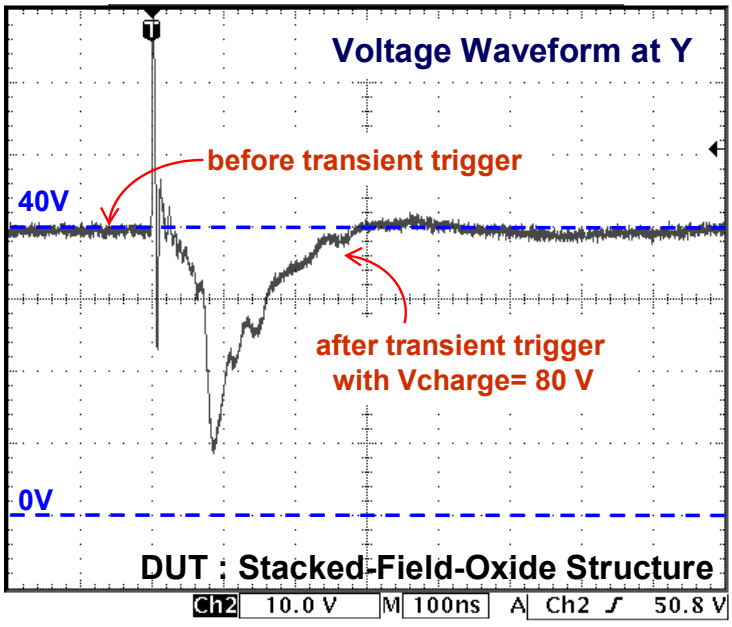
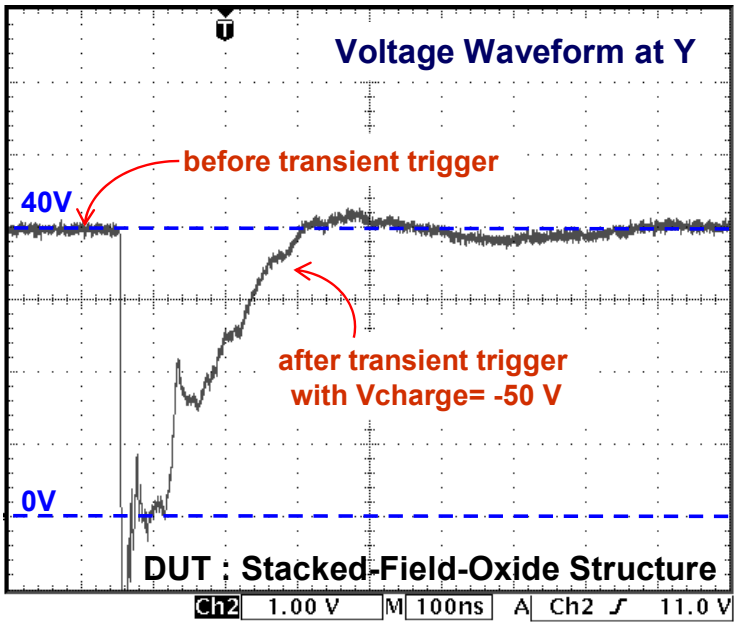


Fig. 4.13 The TLP-measured I-V curves of the stacked-field-oxide structure with different substrate-triggered currents.

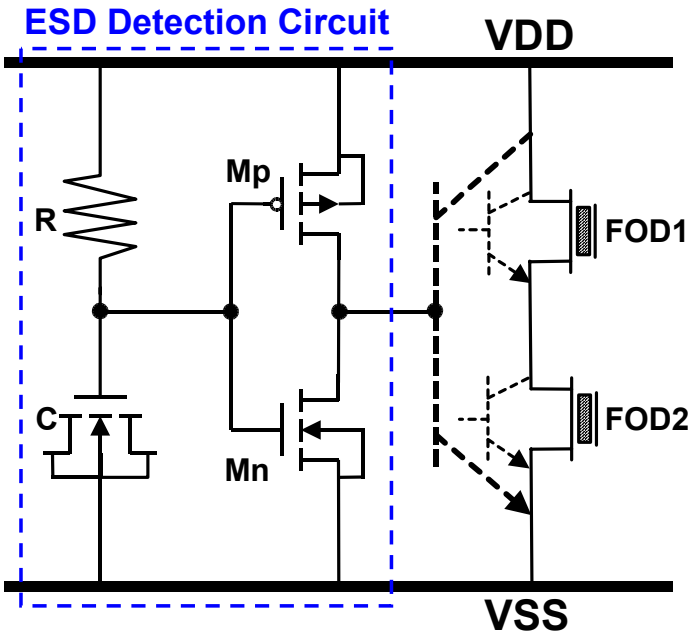


(a)

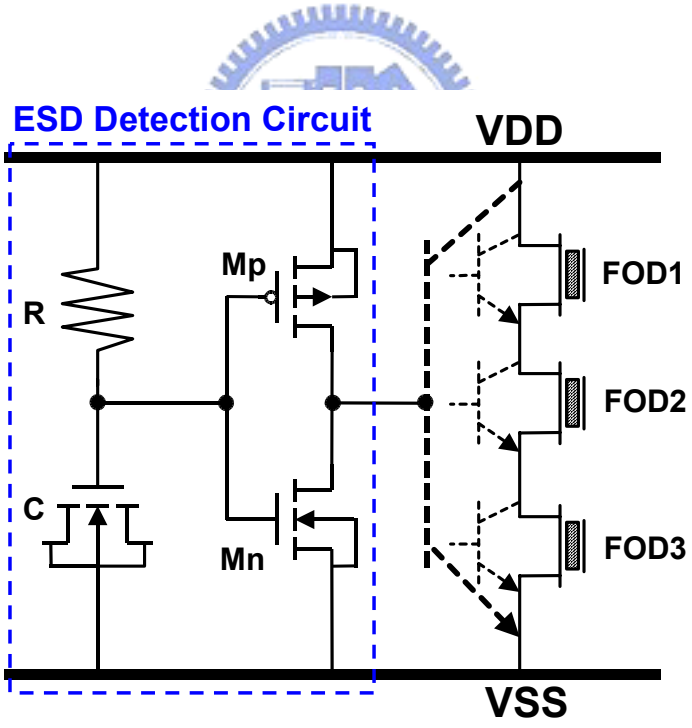


(b)

Fig. 4.14 The measured voltage waveforms on the stacked-field-oxide structure under TLU test with (a) positive charging voltage, and (b) negative charging voltage. (*Y* axis= 10 V/Div., *X* axis= 100 ns/Div.)



(a)



(b)

Fig. 4.15 The proposed power-rail ESD clamp circuits in high-voltage CMOS ICs with (a) two cascaded FOD devices, and (b) three cascaded FOD devices.

CHAPTER 5

I/O CELLS WITH EMBEDDED SCR AS POWER-RAIL ESD CLAMP DEVICE IN NANOSCALE CMOS TECHNOLOGY

In nanoscale CMOS technology, how to realize the area-efficient and turn-on-efficient power-rail ESD clamp circuits to protect the ultra-thin gate oxide will be an important challenge to SOC applications with a much larger chip size but a reduced cell pitch for I/O cell. In this chapter, a new ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in nanoscale CMOS technology is proposed. Two new embedded SCR structures without latchup danger are proposed to be placed between the input (or output) pMOS and nMOS devices of the I/O cells. Furthermore, the turn-on efficiency of embedded SCR can be significantly increased by substrate-triggered technique. By including the efficient power-rail ESD clamp device into each I/O cell, whole-chip ESD protection scheme can be successfully achieved within a small silicon area of I/O cell. Such new proposed I/O cells with embedded SCR structure as power-rail ESD clamp device have been successfully verified in a 130-nm CMOS process for SOC applications [54], [55].

5.1 Embedded SCR Structures in I/O Cells

If the holding voltage of the parasitic SCR is greater than the maximum voltage level of circuit operation, the double guard rings surrounding the input (or output) pMOS and nMOS devices in the I/O cells can be removed. To avoid the latchup occurrence in the internal circuits due to the noise triggering at the I/O pad, the additional guard rings should be added between the I/O cells and the core circuits [53]. Thus, the parasitic SCR structure between input (or output) pMOS and nMOS devices can be used as power-rail ESD clamp device in each I/O cell. The layout view and device structures of new proposed I/O cell with embedded SCR structure I are shown in Figs. 5.1(a) and 5.1(b), respectively. Keeping the single guard ring in the I/O cell, the anode and cathode of embedded SCR structure I are formed by

inserting the extra p+ diffusion in n-well and the extra n+ diffusion in p-well, respectively. To enhance the turn-on speed of embedded SCR structure, the p+ diffusion inserted half in n-well and half in p-well is connected out as substrate-triggered node. When a trigger current is applied into this trigger node, SCR will be triggered into its latching state quickly through the positive feedback regeneration mechanism [81]. The substrate-triggered technique can be realized by the RC-based ESD detection circuit [82]. With RC-based ESD detection circuit, the embedded SCR structure is kept off during the normal circuit operating condition, but it can be quickly triggered on during the ESD stress condition.

The ESD current discharging paths through the I/O cell with embedded SCR structure I under PS-mode, PD-mode, NS-mode, and ND-mode ESD stresses are shown in Figs. 5.2(a) ~ 5.2(d), respectively. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through two discharging paths (path A and path B), as the dashed lines shown in Fig. 5.2(a). The first discharging path (path A) is that the ESD current is discharged through the parasitic diode of pMOS (Mp) to VDD, and then through the embedded SCR structure from the VDD power line to the grounded VSS power line. The second discharging path (path B) is that the ESD current is directly discharged through the parasitic SCR structure from the I/O pad to the grounded VSS power line. Because the ESD current will be discharged through parasitic forward-diode path to VDD first, the ESD detection circuit can detect such ESD pulse to provide the substrate-triggered current to raise up the local substrate potential. The embedded SCR structure and the parasitic SCR structure from drain of pMOS to the grounded n+ in p-well can be quickly triggered on to discharge the ESD current by such substrate-triggered current. The major ESD current will be discharged through the path with lower clamping voltage and lower turn-on resistance. The ESD current at the I/O pad under PD-mode ESD stress can be discharged through the parasitic diode of pMOS (Mp) to the grounded VDD power line, as the dashed lines shown in Fig. 5.2(b). The negative ESD current at the I/O pad under NS-mode ESD stress can be discharged through the parasitic diode of nMOS (Mn) to the grounded VSS power line, as the dashed lines shown in Fig. 5.2(c). The negative ESD current at the I/O pad under ND-mode ESD stress can be discharged through two discharging paths (path C and path D), as the dashed lines shown in Fig. 5.2(d). The first discharging path (path C) is that the negative ESD current is discharged through the parasitic diode of nMOS (Mn) to VSS, and then through the embedded SCR structure from the VSS power line to the grounded VDD power line. The second discharging path (path D) is that the negative ESD current is directly discharged through the parasitic

SCR structure from the I/O pad to the grounded VDD power line. Because the negative ESD current will be discharged through parasitic forward-diode path to VSS first, the ESD detection circuit can detect such ESD pulse to provide the substrate-triggered current to raise up the local substrate potential. The embedded SCR structure and the parasitic SCR structure from the p+ connected to VDD in n-well to the drain of nMOS can be quickly triggered on to discharge the ESD current by such substrate-triggered current. With the two discharging paths, the ESD robustness of the I/O pad under PS-mode and ND-mode ESD stresses can be further improved. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed I/O cell with embedded SCR structure I.

The layout area of the I/O cell can be further reduced by the new embedded SCR structure II. The layout view and device structures of new proposed I/O cell with embedded SCR structure II are shown in Figs. 5.3(a) and 5.3(b), respectively. Without the double guard rings, the anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively. The poly gate in the layout view has a close-loop ring to increase the anode and cathode areas of embedded SCR structure II. The ESD current discharging paths of the I/O cell with embedded SCR structure II under four modes ESD stresses are the same with that of I/O cell with embedded SCR structure I. Especially, under the PS-mode ESD stress, the parasitic SCR (path B) from the drain of pMOS to the source of nMOS can be triggered on to discharge ESD current. Under the ND-mode ESD stress, the parasitic SCR (path D) from the source of pMOS to the drain of nMOS provides the second ESD discharging path. It is important to note that the second discharging path for I/O cell with embedded SCR structure II under PS-mode ESD stress (path B) or under ND-mode ESD stress (path D) becomes more efficient due to the smaller anode-to-cathode spacing of the parasitic SCR structure. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed I/O cell with embedded SCR structure II.

The new proposed whole-chip ESD protection scheme with embedded SCR structure as power-rail ESD clamp device in each I/O cell is shown in Fig. 5.4. Several I/O cells can share one ESD detection circuit to reduce the layout area for high-pin-count applications. With the embedded SCR structure in each I/O cell, the whole-chip ESD protection efficiency is not degraded by the different pin locations in the chip. This will be more valuable for applications in the SOC chip with hundreds of I/O pins.

5.2 Experimental Results

The testchips with the traditional I/O cells and the new proposed I/O cells have been fabricated in a 130-nm salicided CMOS process. The input ESD protection devices are realized by the gate-connected-to-source pMOS (GDPMOS) and gate-grounded nMOS (GGNMOS) with the device dimensions (W/L) of 240/0.18 and 180/0.18 (μm/μm), respectively. The output ESD protection devices are realized by the output buffer of pMOS and nMOS with the same device dimensions as those of the input cell. The layout parameters of input ESD protection devices and output buffers are drawn according to the foundry's ESD rules with or without silicide blocking for comparison. In the new proposed I/O cells, the embedded SCR structures I and II are fully silicided with the SCR device widths of 49.5 and 45.5μm, respectively. The spacing from anode to cathode of the embedded SCR structure is kept at 2.35μm. The total layout area of the whole I/O cell with embedded SCR structure I is only 60μm × 50μm, and that with embedded SCR structure II is only 50μm × 50μm. The ESD detection circuit including R, C, and inverter is realized with R= 60kΩ, C= 3pF, pMOS dimension W/L= 40/0.18 (μm/μm), and nMOS dimension W/L= 8/0.18 (μm/μm). One set of delay-based R and C in the ESD detection circuit can be shared for all I/O cells, which are powered with the same power domain. Such R and C can be implemented in the area of VDD or VSS cells, which provide the power for I/O cells.

5.2.1 DC I-V Characteristics

To avoid the latchup issue, the holding voltage of ESD protection circuit with SCR device must be designed greater than the maximum voltage level of VDD. The dc I-V characteristics of embedded SCR structures I and II in the I/O cells are measured (using Tek370 curve tracer) by applying a voltage sweep on the VDD pin under the bias condition of 0-V VSS but I/O pad is floating. The measured dc I-V characteristics of embedded SCR structures I and II under different temperatures are shown in Figs. 5.5(a) and 5.5(b), respectively. The dependence of holding voltage of embedded SCR structures under different temperatures is summarized in Fig. 5.6. From the measured results, the holding voltage of embedded SCR structures slightly reduces when the temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of temperature. With smaller equivalent well resistance, the holding voltage of embedded SCR structure I is larger than that of embedded SCR structure II. The holding voltages of embedded SCR structures I

and II at temperature of 125°C are 1.54V and 1.27V, respectively, which are both greater than VDD of 1.2V. The measured results have verified that the embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup issue. Especially, the embedded SCR I has a high switching current of greater than 200mA in Fig. 5.5(a), which is suitable for application in the noisy environment to avoid the accidentally triggering.

The measured dc I-V characteristics of embedded SCR structures I and II in the I/O cells under different substrate-triggered currents (Itrig) are shown in Figs. 5.7(a) and 5.7(b), respectively. As shown in Fig. 5.7, the trigger voltage of the embedded SCR structure I without the substrate-triggered current is ~8.5V (by p+ trigger node/n-well junction breakdown), and that of the embedded SCR structure II is ~8V. The switching current and trigger voltage of the embedded SCR structure are decreased while the substrate-triggered current is increased. ESD protection devices with low trigger voltage can be turned on more quickly to discharge ESD current to provide more effective protection for internal circuits. To provide effective ESD protection to the ultra-thin gate oxide in 130-nm CMOS process, the substrate-triggered current of 12mA for embedded SCR structure I and substrate-triggered current of 6mA for embedded SCR structure II are the design suggestion.

As the discussions in section 5.1, one parasitic SCR structure (path B) between I/O pad and VSS power line can be triggered on to discharge ESD current for I/O pad under PS-mode ESD stress, and another parasitic SCR structure (path D) between I/O pad and VDD power line can be triggered on to discharge ESD current for I/O pad under ND-mode ESD stress. The dc I-V characteristics of these parasitic SCR structures for I/O cell with embedded SCR structure II are measured to verify their effectiveness. The dc I-V characteristics of parasitic SCR structure (path B) between I/O pad and VSS power line are measured by applying a voltage sweep on the I/O pad under the bias condition of 0-V VSS but VDD is floating similar to PS-mode. The measured dc I-V characteristics of parasitic SCR structure (path B) between I/O pad and VSS power line under different substrate-triggered currents are shown in Fig. 5.8(a). In addition, the dc I-V characteristics of parasitic SCR structure (path D) between I/O pad and VDD power line are measured by applying a negative voltage sweep on the I/O pad under the bias condition of 0-V VDD but VSS is floating similar to ND-mode. The measured dc I-V characteristics of parasitic SCR structure (path D) between I/O pad and VDD power line under different substrate-triggered currents are shown in Fig. 5.8(b). From the measured results, the holding voltage of parasitic SCR structure (path B) between I/O pad and VSS power line at temperature of 25°C is 1.84V, and that of parasitic SCR structure (path

D) between I/O pad and VDD power line is 1.6V. The trigger voltage of parasitic SCR structure between I/O pad and VSS power line without the substrate-triggered current is ~3.5V (by n+/p-well of nMOS junction breakdown), and that of parasitic SCR structure between I/O pad and VDD power line is ~5.5V (by p+/n-well of pMOS junction breakdown). The trigger voltage of these parasitic SCR structures can be effectively decreased while the substrate-triggered current is increased. Although the trigger voltage of these parasitic SCR structures without the substrate-triggered current is lower than that of embedded SCR structure, both SCR structures can be triggered on quickly to discharge ESD current with the appropriate substrate-triggered current generated from the ESD detection circuit.

5.2.2 TLP I-V Characteristics

To investigate the device behavior during high ESD current stress, transmission line pulse (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is used to measure the second breakdown current (It2) of the device [75]. The TLP-measured I-V characteristics of the I/O cells with embedded SCR structures under positive VDD-to-VSS ESD stress with or without ESD detection circuit are shown in Fig. 5.9(a). The enlarged view around the switching point for I/O cells with ESD detection circuit is shown in Fig. 5.9(b). From the measured results, the trigger voltages of embedded SCR structures I and II without ESD detection circuit are 10.5V and 8.8V, respectively. However, the trigger voltages of embedded SCR structures I and II can be reduced to only 2.7V and 1.74V, respectively, by the ESD detection circuit without involving the avalanche junction breakdown mechanism. Therefore, the trigger voltage of embedded SCR structure can be significantly reduced by substrate-triggered technique to ensure effective ESD protection. The It2 per micron of embedded SCR structure is as high as ~100mA/μm, without using the silicide-blocking process modification.

The TLP-measured I-V curves of I/O cells with or without embedded SCR structure under PS-mode ESD stress are compared in Fig. 5.10. Without the embedded SCR structure, the ESD current at the input pad under PS-mode ESD stress is discharged through the silicide-blocking GGNMOS by snapback breakdown. The trigger voltage (snapback breakdown voltage) of GGNMOS is 4.3V, and the It2 of silicide-blocking GGNMOS with dimension W/L= 180/0.18 (μm/μm) is 1.6A. However, the trigger voltages of input cell with embedded SCR structures I and II under PS-mode ESD stress are only 3.44V and 2.5V,

respectively. In addition, the It2 of input cell with embedded SCR structure under PS-mode ESD stress can be increased to ~3A. From the measured results, the new proposed I/O cells with embedded SCR structure have lower trigger voltage, lower clamping voltage level, smaller turn-on resistance, and higher ESD robustness, as compared with the traditional I/O cells. Therefore, the ESD level of I/O cell can be efficiently improved by inserting the embedded SCR structure in I/O cell.

The TLP-measured I-V curves of the input pad under PS-mode ESD stress with or without silicide blocking on the input pMOS and nMOS devices are shown in Fig. 5.11. The It2 of the input pad under PS-mode ESD stress with silicide blocking on pMOS and nMOS devices is ~3A, and that without silicide blocking is ~2A. Whereas, the embedded SCR structures are fully silicided in these I/O cells. From the measured I-V curves, there is a distinct change of slope in the high current stress region, because the clamping voltage on the pad reaches the triggering voltage of the nMOS to cause a decrease on the turn-on resistance. With smaller turn-on resistance of fully silicided nMOS, the total turn-on resistance of the input pad under PS-mode ESD stress can be effectively reduced by input cell with fully silicided process. But with the fully silicided process, the It2 is dropped because the input nMOS device can sustain less ESD current when the parasitic npn bipolar transistor is triggered on. From the electrical measurements after the input pad under PS-mode ESD stress, the input pad is shorting to ground to indicate that the ESD damages are located at the input nMOS device. Therefore, with lower clamping voltage, the I/O cell with embedded SCR structure II is the design suggestion for fully silicided process.

The TLP-measured I-V curves of the I/O cells with embedded SCR structures I and II under NS-mode ESD stress are shown in Fig. 5.12. The It2 of input pad under NS-mode ESD stress with embedded SCR structure I is 4A, and that with embedded SCR structure II is 3A. The I/O cell with embedded SCR structure I under NS-mode ESD stress has a higher It2 current, because the p+ pickup in the layout with a close-loop ring causes a larger effective turn-on area (parasitic diode of nMOS) for ESD current discharging. For the I/O cell with embedded SCR structure II under NS-mode ESD stress, there is a change of slope at high current stress region. The parasitic npn bipolar transistor of nMOS device is suspected to be triggered on to discharge ESD current from source (collector) to drain (emitter) to cause the decrease on the turn-on resistance.

5.2.3 ESD Robustness and Failure Analysis

To verify the ESD robustness of the new proposed ESD protection scheme, the output buffer of pMOS (Mp_out) and nMOS (Mn_out) in the output cell are individually controlled by the input cells, as that shown in Fig. 5.13. The SCR structure is embedded in each I/O cell. The human-body-model (HBM) ESD robustness of the new proposed ESD protection scheme with embedded SCR structures I and II under different pin combinations is listed in Table 5.1. The failure criterion is defined as 30% corresponding I-V curve shifting at 1-μA current bias. With the embedded SCR structure I, the ESD level of the I/O pads is 4.5kV, which is dominated by the I/O pad under PS-mode ESD stress. However, the ESD levels of the I/O pads under other modes of ESD stresses are near to or even over 8kV. The ESD damages of the I/O cells with embedded SCR structure I under PS-mode ESD stress are located at input or output nMOS device. Fig. 5.14(a) shows the failure location at the input nMOS device for the I/O cells with embedded SCR structure I under PS-mode ESD stress. Although the major ESD current path is discharged through the embedded SCR structure or parasitic SCR structure for the I/O pad under PS-mode ESD stress, the parasitic npn bipolar transistor of input or output nMOS device can be triggered on at high current stress region. However, this ESD level of such I/O cells is higher enough for safe IC production and field applications. To further improve ESD level, the increase of SCR effective area is a design suggestion.

With the embedded SCR structure II, the ESD level of the I/O pads is 5.0kV, which is dominated by the I/O pad under NS-mode ESD stress. The I/O pad under NS-mode ESD stress with embedded SCR structure II has a lower ESD level than that with embedded SCR structure I, which has been confirmed by the TLP-measured I-V curves in Fig. 5.12. From the failure analysis, the ESD damages of the I/O cells with embedded SCR structure II under both PS-mode and NS-mode ESD stresses are located at input or output nMOS device. Fig. 5.14(b) shows the failure location at the center finger of input nMOS device for the I/O cells with embedded SCR structure II under NS-mode ESD stress. From the failure spot in Fig. 5.14(b), the ESD current is discharged from source (collector) to drain (emitter) to imply that the parasitic npn bipolar transistor of nMOS device is triggered on. Although the parasitic forward-diode path of nMOS device is turned on first, the parasitic npn bipolar transistor of nMOS device is still triggered on at high current stress region. With an ESD level of 5kV in a small layout area, such I/O cells are very suitable for high-pin-count SOC applications.

The comparison on the HBM ESD robustness between the traditional I/O cell and new

proposed I/O cells with embedded SCR structures is shown in Table 5.2. For the I/O cell with embedded SCR structure I (II), the HBM ESD level per layout area is 1.5 V/μm^2 (2 V/μm^2), but it is only 1 V/μm^2 for the traditional I/O cell. This has verified the excellent area efficiency of the new proposed I/O cell with embedded SCR structure.

5.2.4 Turn-On Verification During Pin-to-Pin ESD Stress

To verify the turn-on efficiency of the proposed I/O cells with embedded SCR structure in whole-chip ESD protection scheme, a 0-to-4V sharply rising voltage pulse with a rise time of 10ns is applied to one I/O pad while another I/O pad is relatively grounded (to simulate the pin-to-pin ESD stress condition). The measured voltage waveforms on the I/O pads of traditional I/O cells and new proposed I/O cells with embedded SCR structure II under pin-to-pin ESD stress condition are compared in Figs. 5.15(a) and 5.15(b), respectively. With the traditional I/O cells, the applied 0-to-4V voltage waveform is not degraded. It implies that the ESD protection devices in traditional I/O cells can't be triggered on by the applied voltage pulse. However, with the new proposed I/O cells, the applied 0-to-4V voltage pulse can quickly trigger on the ESD protection circuit to cause a degraded voltage waveform in Fig. 5.15(b) with a clamped voltage level of ~2.3V. This implies that the embedded SCR structure II or the parasitic SCR structure between I/O pad and VSS power line can be triggered on by the applied voltage pulse. The degraded voltage waveform has verified the effectiveness of the proposed I/O cells with embedded SCR structure to protect the ultra-thin gate oxide in nanoscale CMOS process.

5.3 Summary

An area-efficient ESD protection design for I/O cells in a 130-nm CMOS technology with embedded SCR structures has been proposed and verified. The embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup danger. The turn-on speed of SCR can be significantly enhanced by substrate-triggered technique. The ESD discharging paths of the new proposed I/O cells with embedded SCR structures under ESD stresses have been clearly investigated by TLP stress, failure analysis, and turn-on verification. High ESD robustness has been practically achieved in the testchip with new proposed I/O cells to sustain HBM ESD stress of up to 5kV in a 130-nm salicided CMOS process. By including the embedded

SCR structure as the power-rail ESD clamp device in each I/O cell, one set of high-ESD-robust and high-area-efficient I/O cells have been developed in a 130-nm CMOS technology for system-on-a-chip (SOC) applications.

TABLE 5.1

HBM ESD robustness of the new proposed ESD protection scheme with embedded SCR structure in each I/O cell.

ESD Protection Scheme \ HBM ESD Stress	PS-Mode VSS (+)	NS-Mode VSS (-)	PD-Mode VDD (+)	ND-Mode VDD(-)	VDD-to-VSS (+)	VDD-to-VSS (-)
I/O Cells with Embedded SCR I (Input Pad)	5.0kV	7.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR I (Output Pad)	4.5kV	7.75kV	>8kV	>8kV		
I/O Cells with Embedded SCR II (Input Pad)	5.5kV	5.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR II (Output Pad)	5.5kV	5.0kV	>8kV	>8kV		

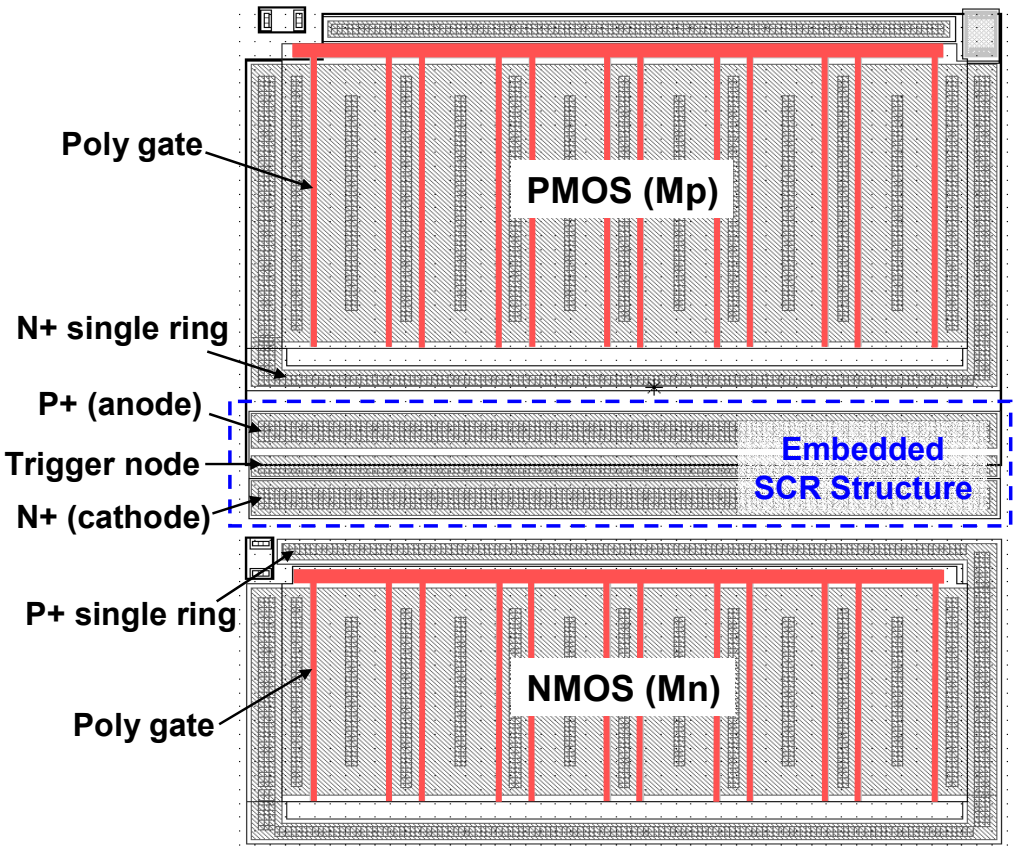
Silicide Blocking only on nMOS and pMOS
Input/Output pMOS W/L= 240/0.18 (μm) **SCR I width= 49.5 (μm)**
Input/Output nMOS W/L= 180/0.18 (μm) **SCR II width= 45.5 (μm)**

TABLE 5.2

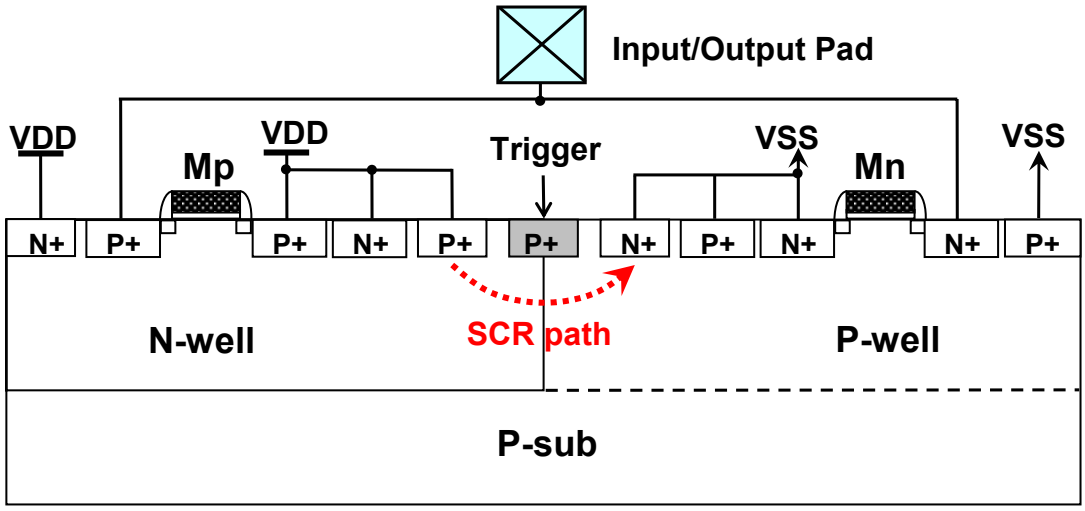
Comparison on the HBM ESD robustness between the traditional I/O cell and the new proposed I/O cells with embedded SCR structures.

I/O Cell	Traditional I/O Cell	I/O Cell with Embedded SCR Structure I	I/O Cell with Embedded SCR Structure II
Layout Area (μm^2)	50 X 60	50 X 60	50 X 50
HBM (kV)	3	4.5	5
VESD,HBM/Area ($V/\mu m^2$)	1	1.5	2

Silicide Blocking only on nMOS and pMOS
Input/Output pMOS W/L= 240/0.18 (μm) **SCR I width= 49.5 (μm)**
Input/Output nMOS W/L= 180/0.18 (μm) **SCR II width= 45.5 (μm)**

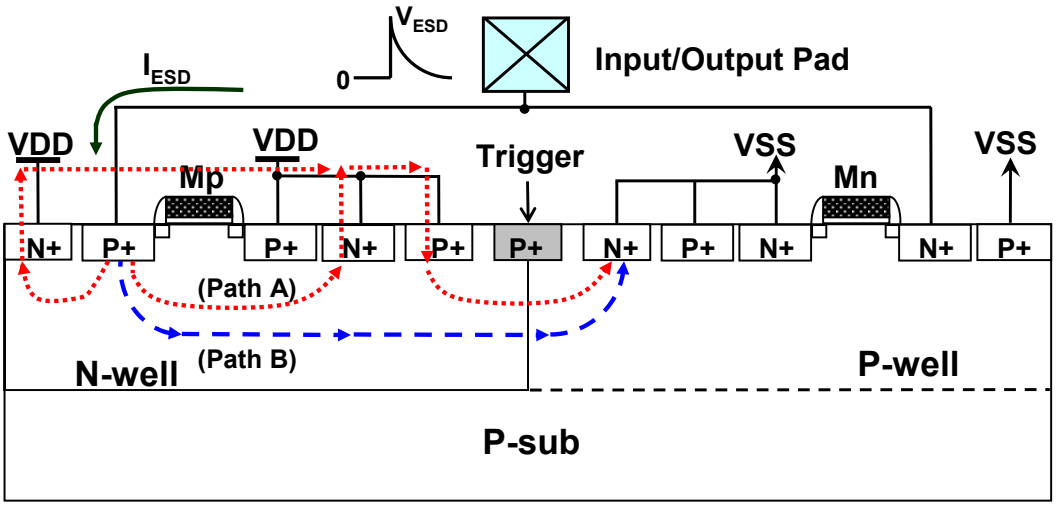


(a)



(b)

Fig. 5.1 (a) Layout view and (b) device structures of the new proposed I/O cell with embedded SCR structure I. The anode and cathode of embedded SCR structure I are formed by inserting extra p+ diffusion in n-well and n+ diffusion in p-well, respectively.



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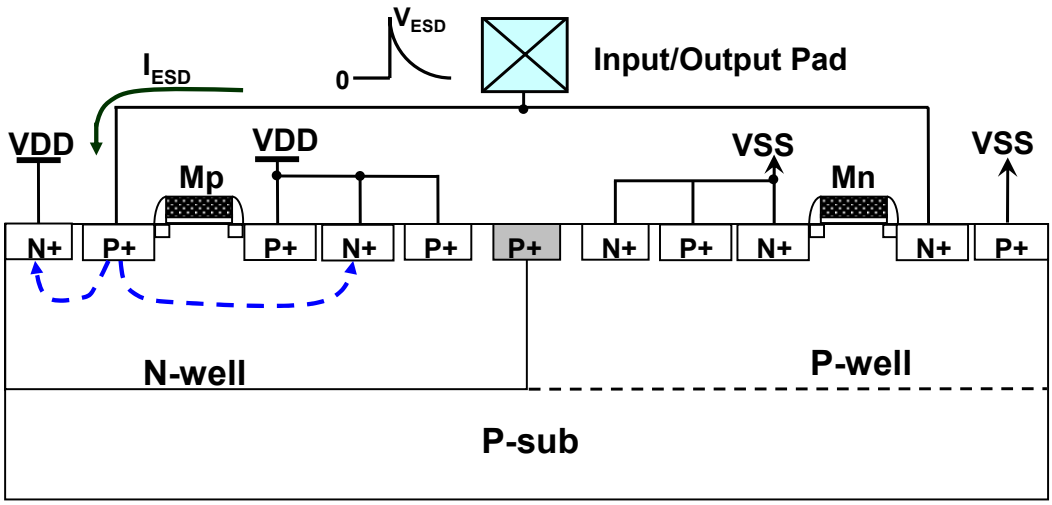
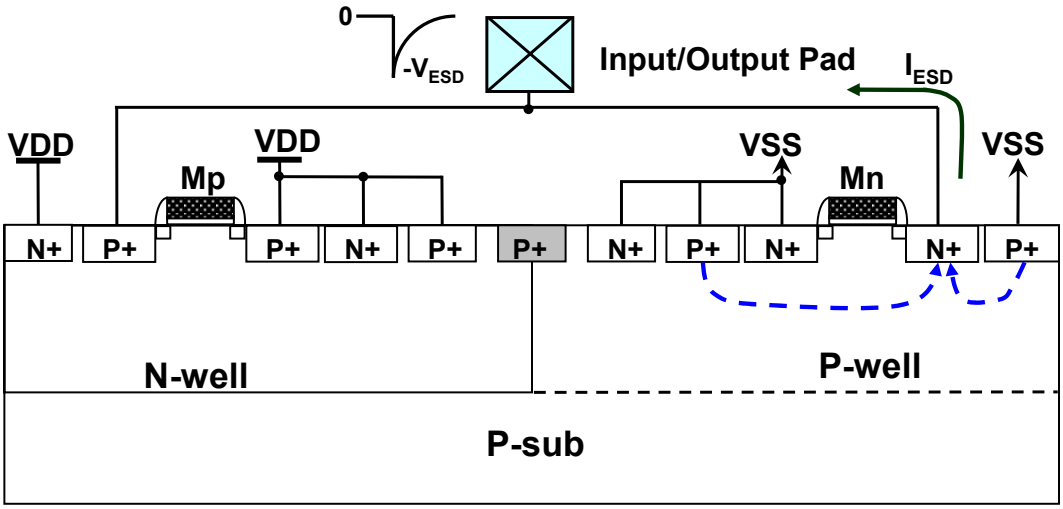


(b)

(continue to next page, **Fig. 5.2**)



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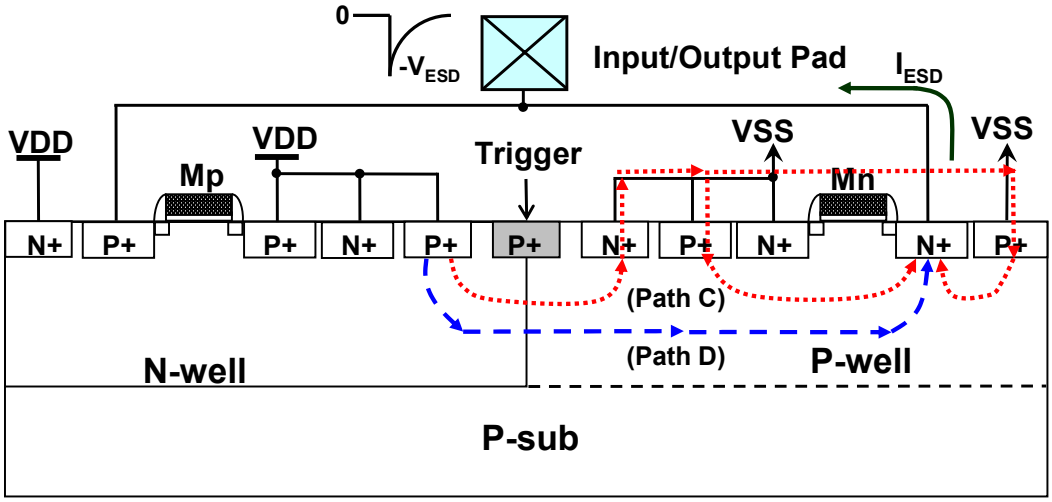
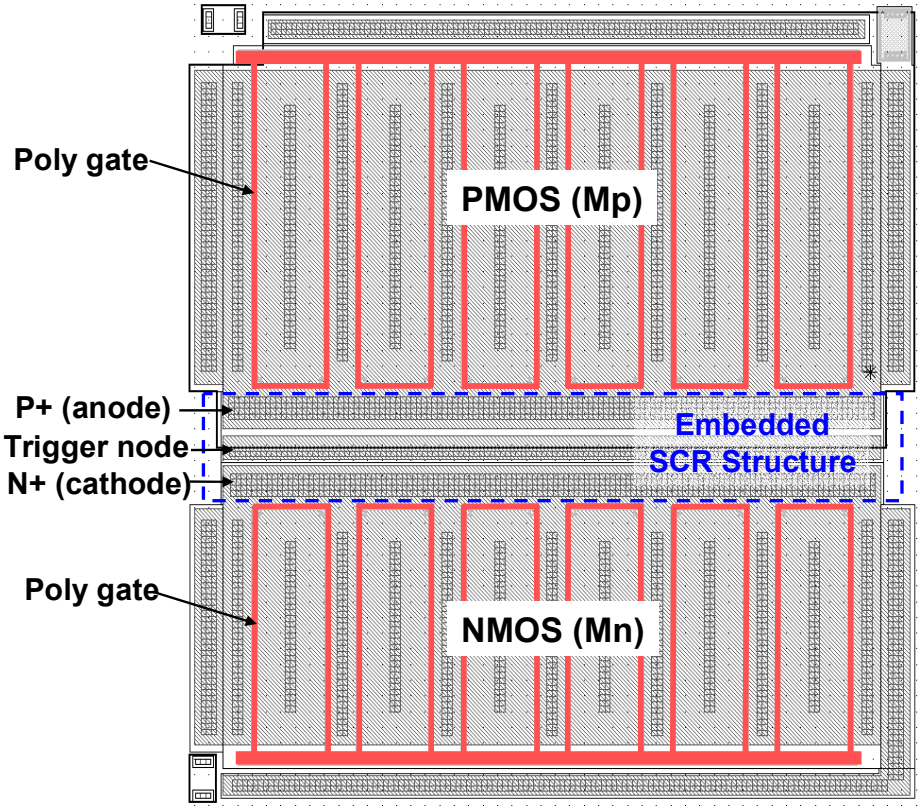
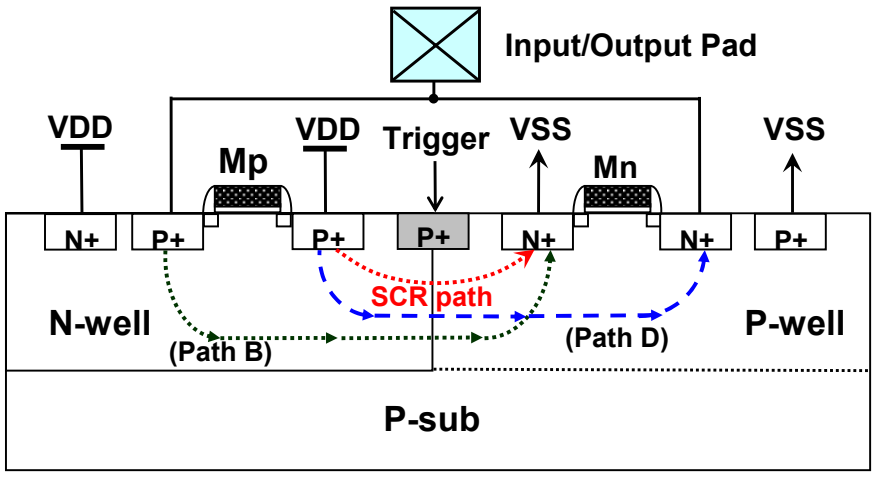


(d)

Fig. 5.2 The ESD current discharging paths of I/O cell with embedded SCR structure I under (a) positive-to-VSS ESD stress condition, (b) positive-to-VDD ESD stress condition, (c) negative-to-VSS ESD stress condition, and (d) negative-to-VDD ESD stress condition.



(a)



(b)

Fig. 5.3 (a) Layout view and (b) device structures of new proposed I/O cell with embedded SCR structure II. The anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively.

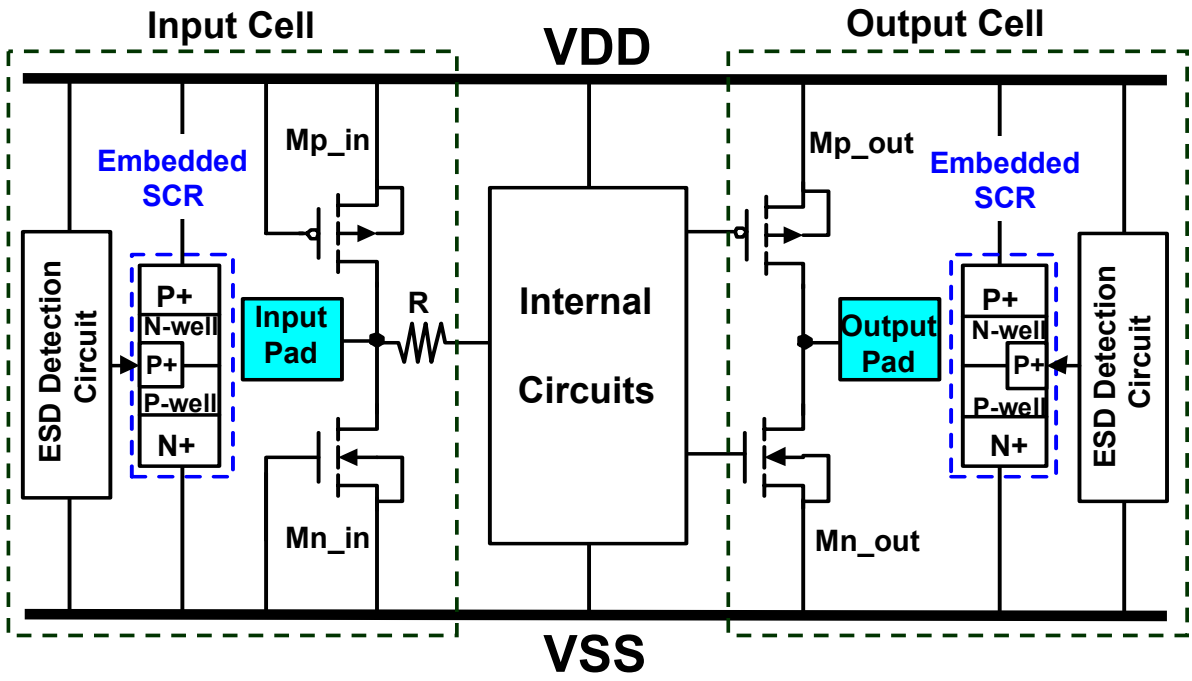
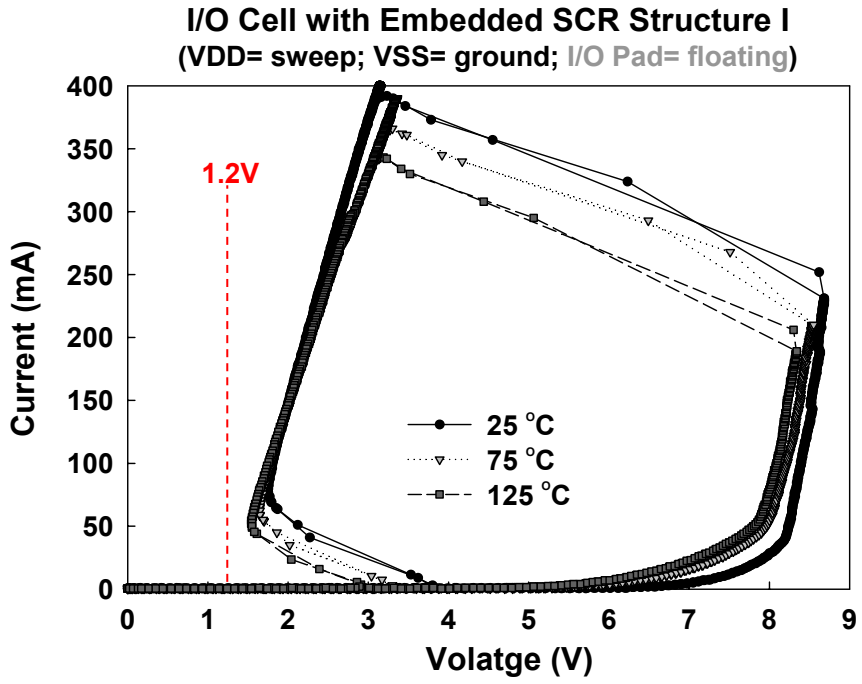
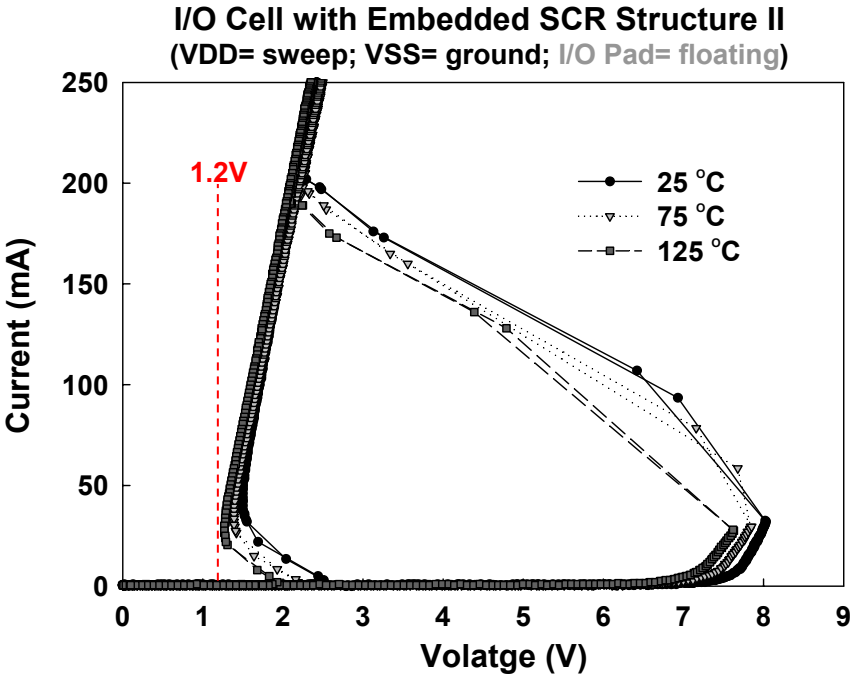


Fig. 5.4 The new proposed whole-chip ESD protection scheme with embedded SCR structure in each I/O cell. The substrate-triggered technique was realized by the RC-based ESD detection circuit.



(a)



(b)

Fig. 5.5 The measured dc I-V characteristics of the (a) embedded SCR structure I, and (b) embedded SCR structure II, in the I/O cells under different temperatures.

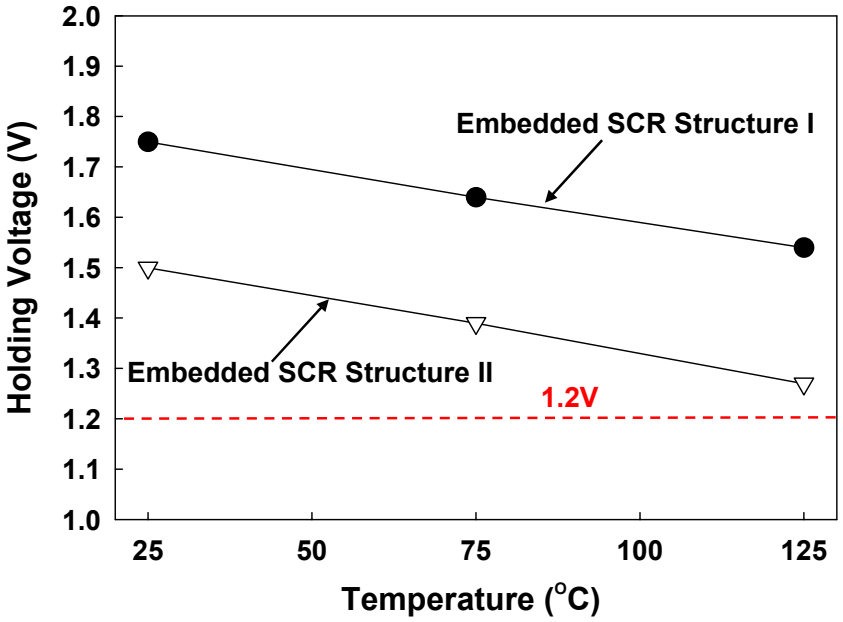
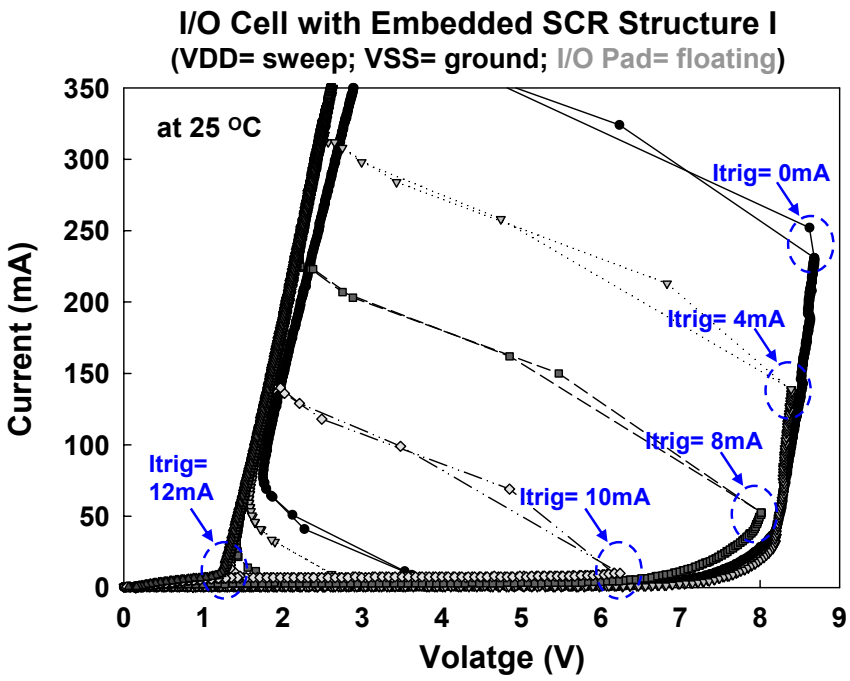


Fig. 5.6 The relation between the holding voltage of the embedded SCR structures and the operating temperature.



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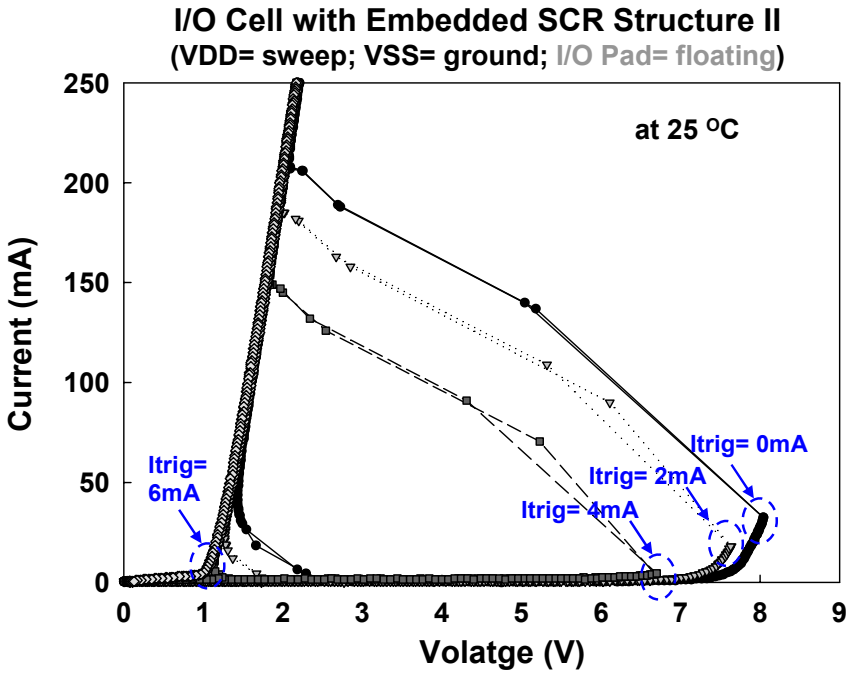
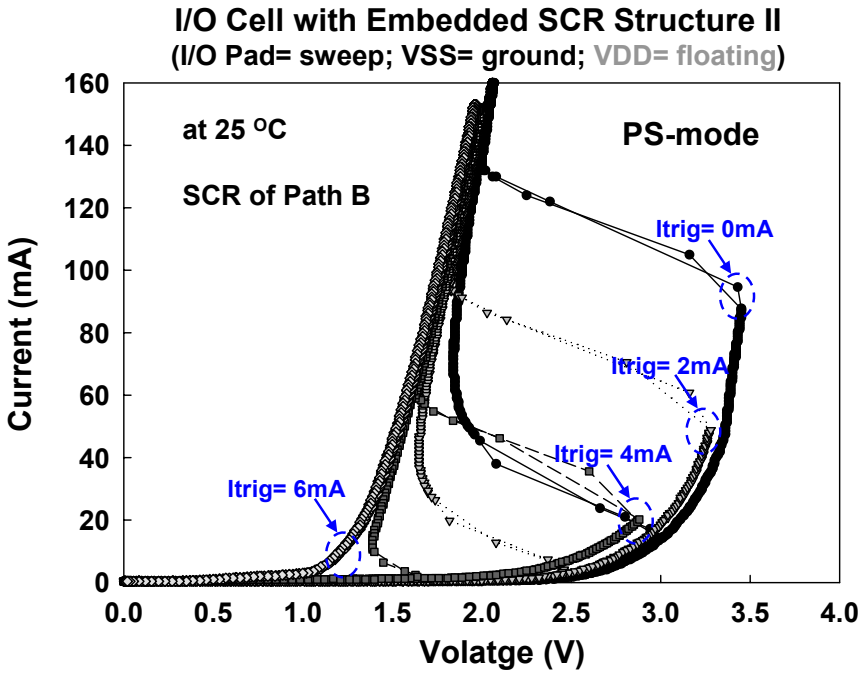
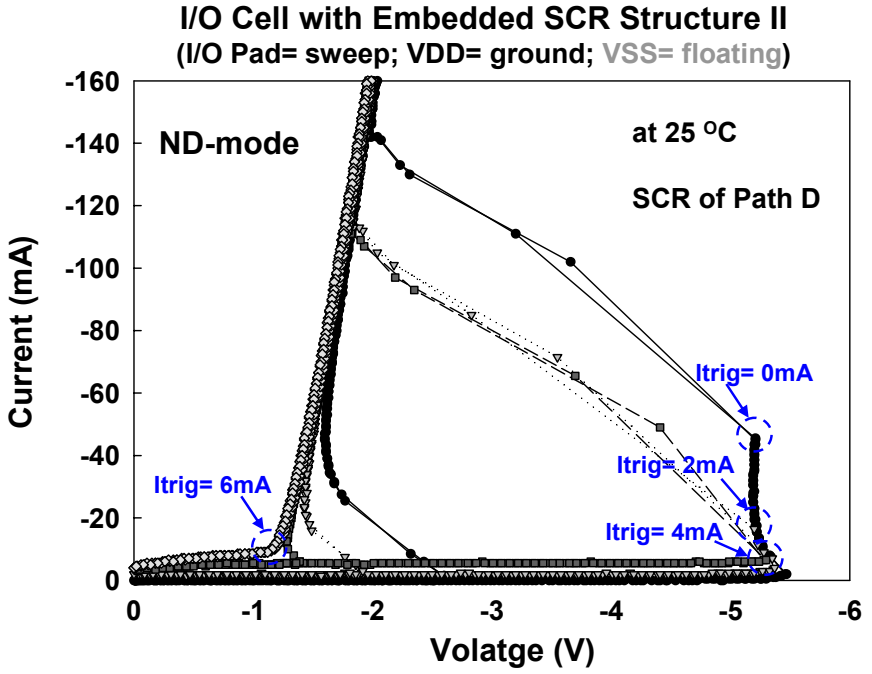


(b)

Fig. 5.7 The measured dc I-V characteristics of the (a) embedded SCR structure I, and (b) embedded SCR structure II, in the I/O cells under different substrate-triggered currents (Itrig).

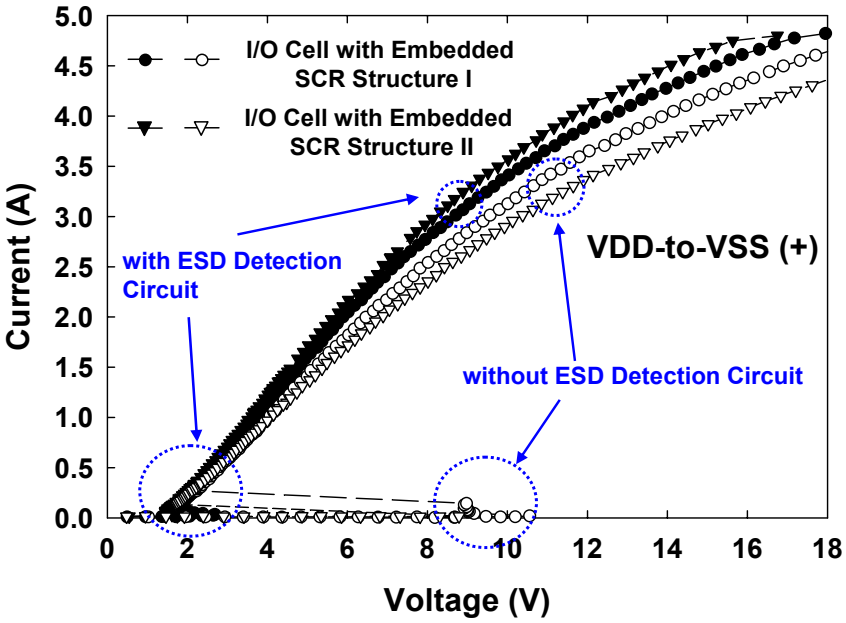


(a)



(b)

Fig. 5.8 The measured dc I-V characteristics of (a) the parasitic SCR structure (path B) between I/O pad and VSS power line, and (b) the parasitic SCR structure (path D) between I/O pad and VDD power line, in the I/O cell with embedded SCR structure II under different substrate-triggered currents (Itrig).



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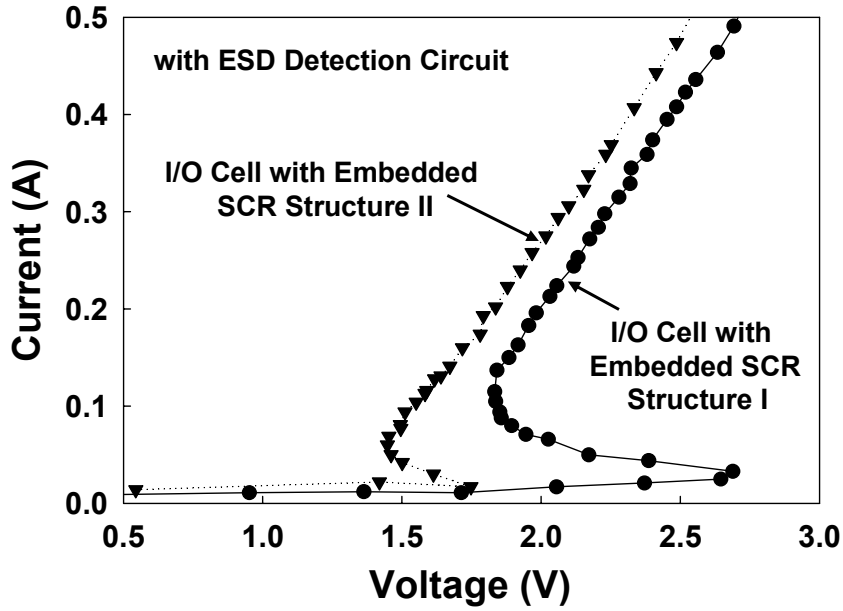


(b)

Fig. 5.9 (a) The TLP-measured I-V curves of the I/O cells with embedded SCR structures I and II under positive VDD-to-VSS ESD stress with or without ESD detection circuit. (b) The enlarged view around the switching point of the measured curves for I/O cells with ESD detection circuit.

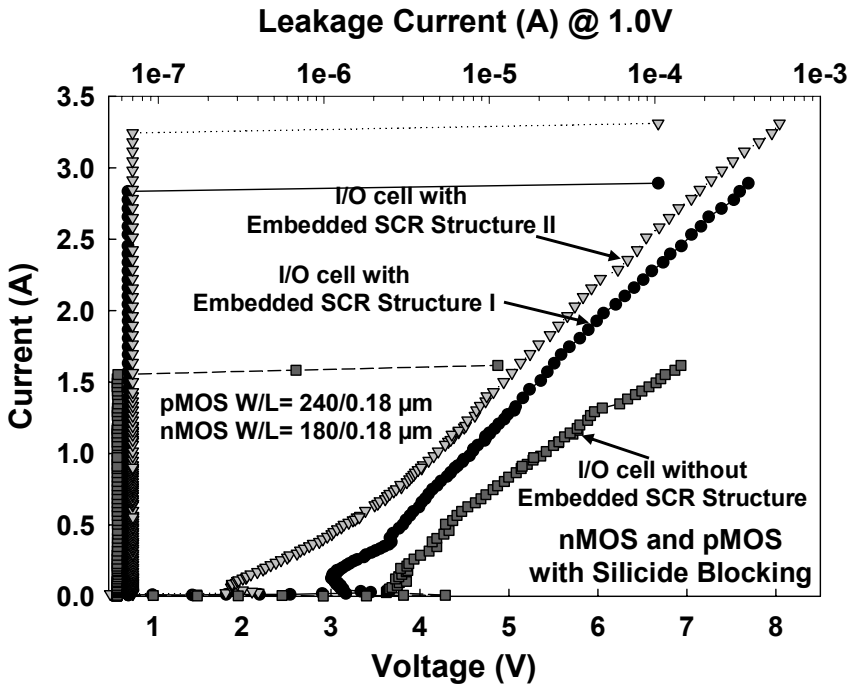


Fig. 5.10 The TLP-measured I-V curves of the input pad under positive-to-VSS ESD stress with or without embedded SCR structure, where the I/O nMOS and pMOS are silicide-blocking but the embedded SCR structures are fully silicided.

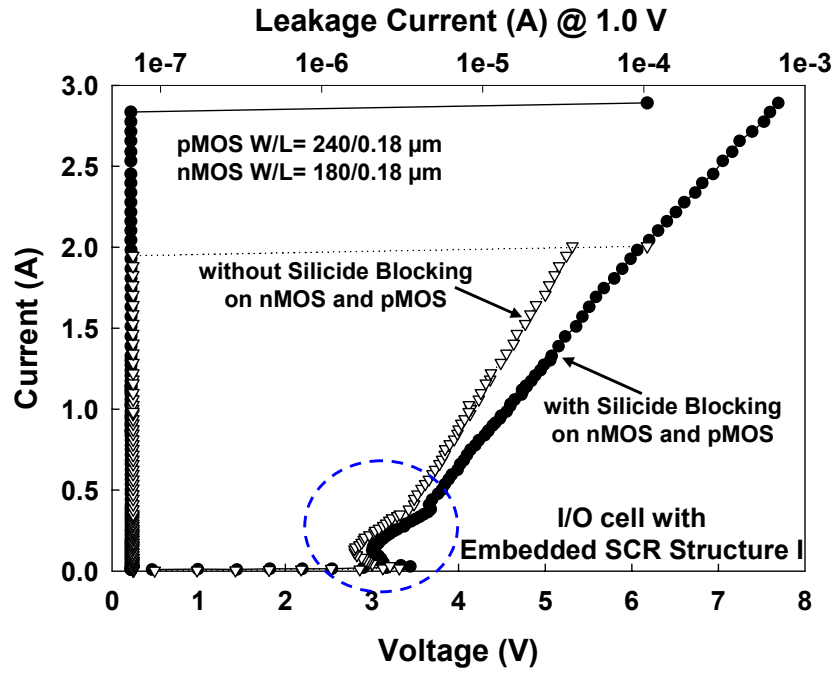


Fig. 5.11 The TLP-measured I-V curves of the input pad under positive-to-VSS ESD stress with or without silicide blocking on the input pMOS and nMOS devices, whereas the embedded SCR structures are fully silicided.

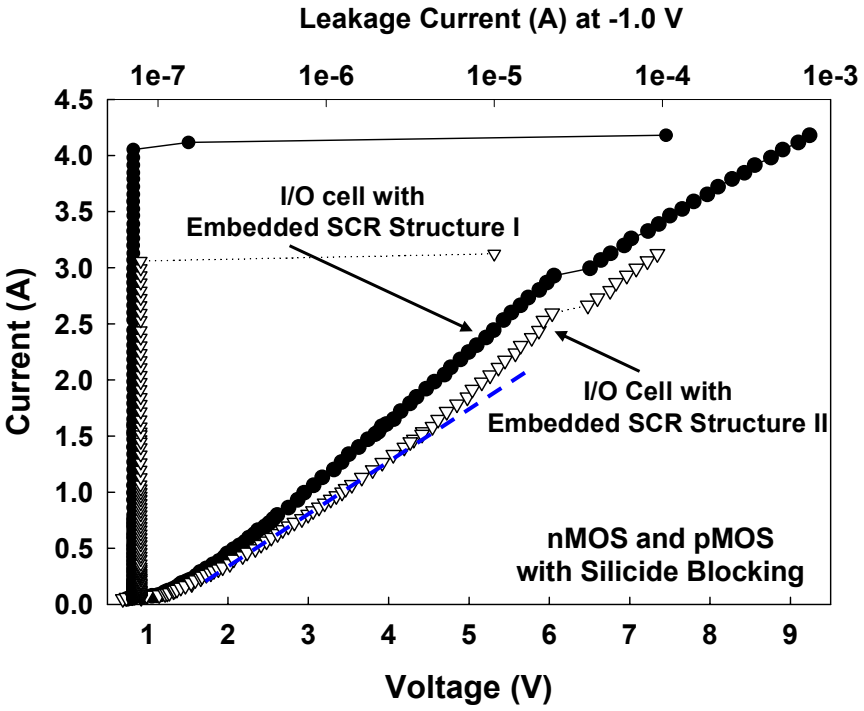


Fig. 5.12 The TLP-measured I-V curves of the I/O cells with embedded SCR structures I and II under negative-to-VSS ESD stress.

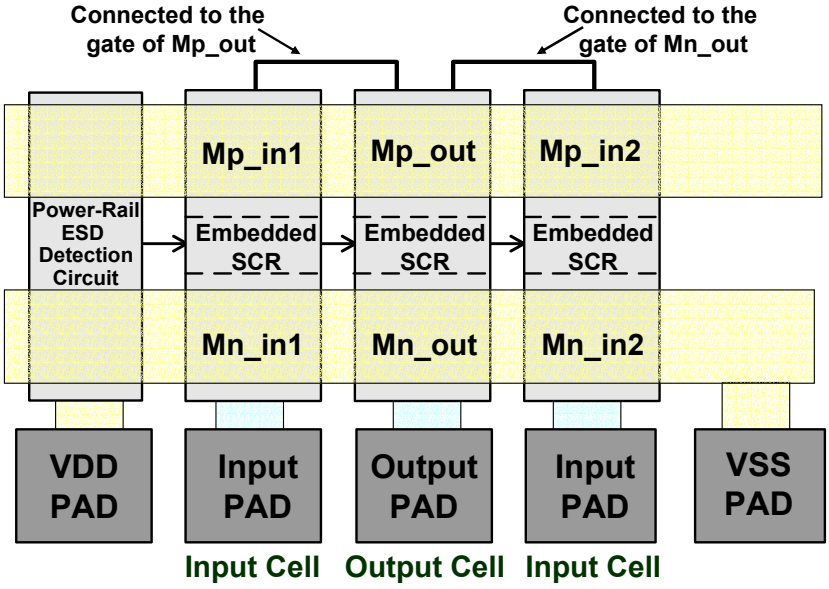
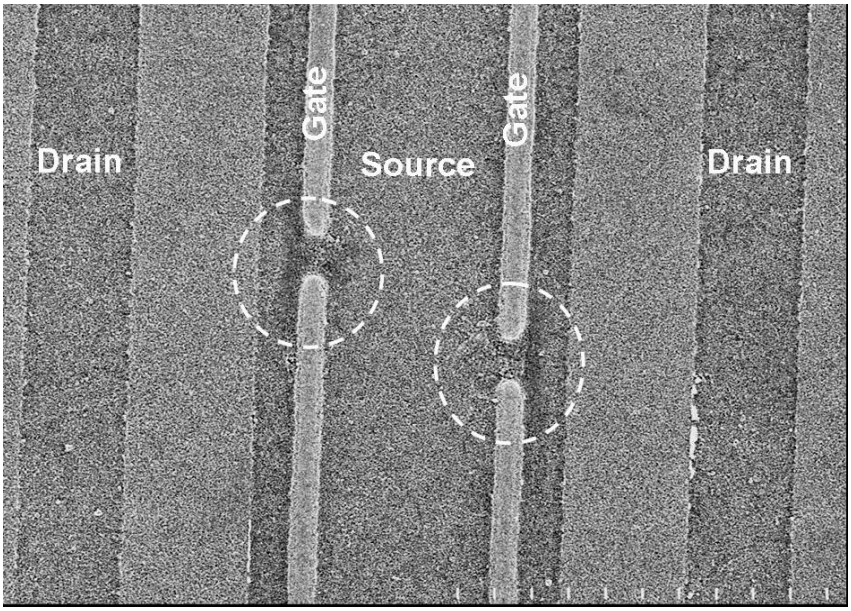
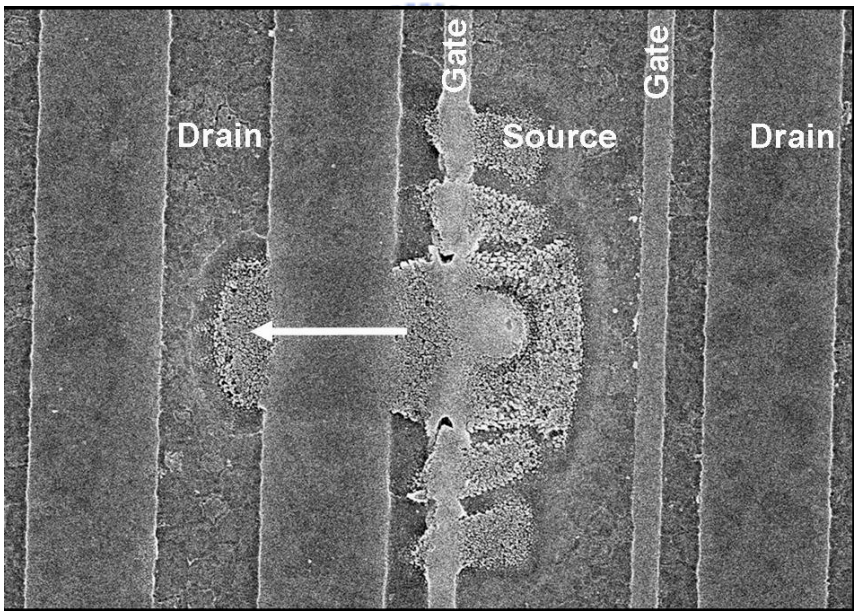


Fig. 5.13 The testchip to verify ESD robustness of the I/O cells with embedded SCR structures. The output buffer of pMOS (Mp_out) and nMOS (Mn_out) in output cell are individually controlled by the input cells.

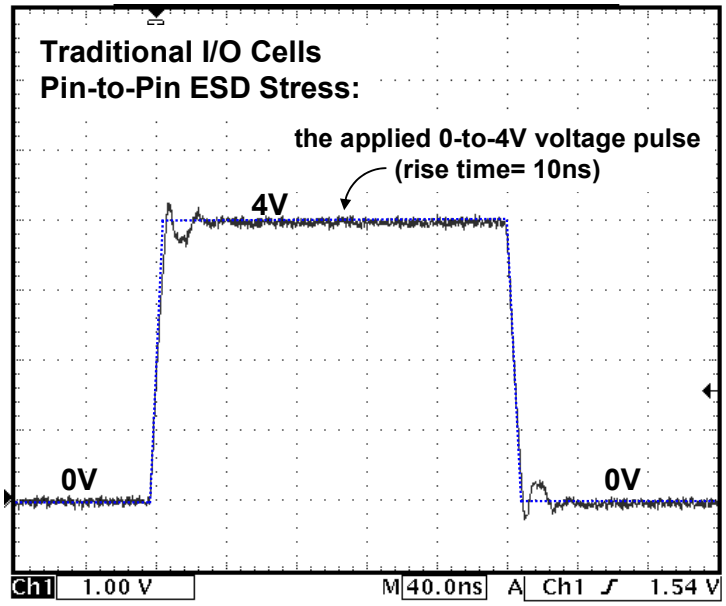


(a)

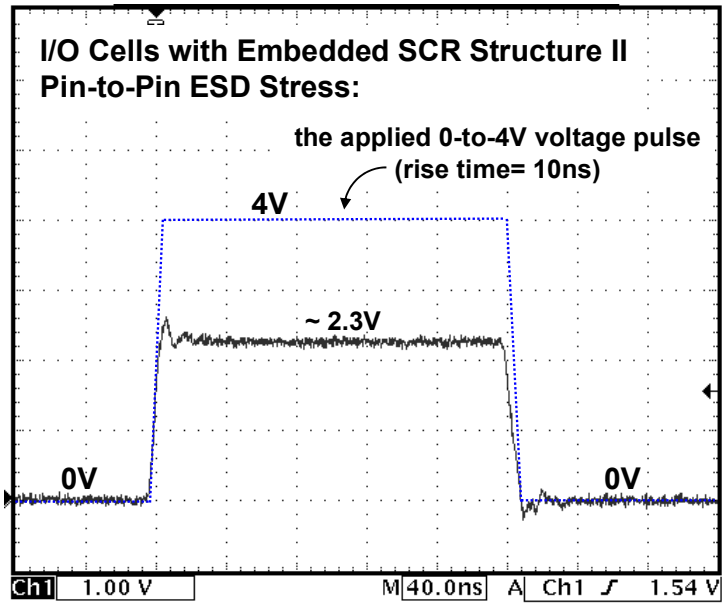


(b)

Fig. 5.14 (a) The failure location at the input nMOS device for the I/O cells with embedded SCR structure I under positive-to-VSS ESD stress. (b) The failure location at the input nMOS device for the I/O cells with embedded SCR structure II under negative-to-VSS ESD stress.



(a)



(b)

Fig. 5.15 Measured voltage waveforms on the I/O pads triggered by a 0-to-4V voltage pulse with a rise time of 10ns for the (a) traditional I/O cells, and (b) new proposed I/O cells with embedded SCR structure II, under pin-to-pin ESD stress condition. (*Y* axis: 1 V/div., *X* axis: 40 ns/div.)

CHAPTER 6

CONCLUSIONS AND FUTURE WORKS

6.1 Main Results of This Thesis

In this thesis, the novel ESD protection circuits have been developed for mixed-voltage I/O interfaces, power-down-mode application, high-voltage CMOS process, and nanoscale CMOS technology with high ESD robustness. Each of the ESD protection circuits has been successfully verified in the testchips.

In chapter 2, to improve ESD robustness of the stacked-nMOS device in the mixed-voltage I/O circuit, the stacked-nMOS device with new proposed substrate-triggered circuit, has been designed and successfully verified in a 0.25-μm salicided CMOS process. The I-V characteristics of stacked-nMOS device with substrate-triggered technique have been measured to verify its effectiveness. By using this substrate-triggered design, the trigger voltage of the stacked-nMOS device can be reduced from the original 8.5V to become 5.3V to ensure effective protection for the mixed-voltage I/O circuits. The HBM ESD level of the mixed-voltage I/O buffer with a stacked-nMOS of 240-μm channel width can be improved from the original 3.4 kV up to 5.6 kV by the substrate-triggered circuit. Without using the thick gate oxide, this new proposed ESD protection design is very useful in the sub-quarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins.

In chapter 3, three new ESD protection schemes without leakage current path for CMOS IC operating in power-down-mode condition have been successfully designed and verified in a 0.35-μm silicided CMOS process. Under the normal circuit operating condition, the I/O cells with the new proposed ESD protection schemes can be operated normally. Under the power-down-mode operating condition, the new proposed ESD protection schemes can provide the I/O pad without leakage path, and avoid triggering the internal circuits those should be “off”. High ESD robustness has been practically achieved in the testchip with these new proposed ESD protection schemes to sustain HBM ESD stress of up to 7.5kV in a 0.35-μm silicided CMOS process. Furthermore, the output signal of the new modified ESD

protection schemes can be successfully pulled up to VDD again by the output-swing improvement circuit under normal circuit operating condition.

In chapter 4, the double snapback characteristic in the high-voltage nMOSFETs has been clearly investigated and analyzed by both measured and simulation results. Furthermore, Latchup or latchup-like issue of ESD protection devices in high-voltage CMOS ICs has been clearly investigated by TLP stress and TLU test. The impact of low holding voltage of ESD protection devices to cause the high-voltage CMOS ICs susceptible to latchup or latchup-like danger during normal circuit operating condition has been shown. By adjusting different numbers or different types of stacked ESD devices in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage without using extra process modification in the high-voltage CMOS technology. For the IC applications with power supply of 40V, a new latchup-free power-rail ESD clamp circuit with stacked-field-oxide structure has been designed and successfully verified in a 0.25-μm 40-V CMOS process to meet the desired ESD level.

In chapter 5, an area-efficient ESD protection design for I/O cells in a 130-nm CMOS technology with embedded SCR structures has been proposed and verified. The embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup danger. The turn-on speed of SCR can be significantly enhanced by substrate-triggered technique. The ESD discharging paths of the new proposed I/O cells with embedded SCR structures under ESD stresses have been clearly investigated by TLP stress, failure analysis, and turn-on verification. High ESD robustness has been practically achieved in the testchip with new proposed I/O cells to sustain HBM ESD stress of up to 5kV in a 130-nm salicided CMOS process. By including the embedded SCR structure as the power-rail ESD clamp device in each I/O cell, one set of high-ESD-robust and high-area-efficient I/O cells have been developed in a 130-nm CMOS technology for SOC applications.

6.2 Future Works

In mixed-voltage I/O interfaces, the effective ESD protection design has been proposed and verified in this thesis. But, for some mixed-voltage circuit applications, the power supply voltage may exceed the ordinary VDD of the process to drive a high-voltage output signal. Therefore, it is required to design the high-voltage-tolerant power-rail ESD clamp circuit with

low-voltage devices but without suffering the gate-oxide reliability issue. In the high-voltage-tolerant power-rail ESD clamp circuit, the standby leakage current between the power rails is an important concern, especially when the IC is operating at high-temperature environment. In high-voltage CMOS technology, the total holding voltage of the stacked-device structure can be designed higher than the supply voltage to avoid the latchup or latchup-like issues in high-voltage CMOS ICs. But, the layout area of the stacked-device structure will increase as compared to that of the single device, especially for high ESD robustness requirement. The design of new device with the characteristics of both high holding voltage and high ESD robustness from the structure design or process modification will be a useful solution. In nanoscale CMOS technology, the ESD protection design for the charged-device model (CDM) ESD event will be another challenge to protect the ultra-thin gate oxide, especially for the SOC applications with a large chip area. Such ESD topics will be the continual future works for research.

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ESD Protection Designs for Mixed-Voltage I/O Interfaces in CMOS Integrated Circuits

PUBLICATION LIST

(A) Referred Journal Papers:

[1] Ming-Dou Ker and **Kun-Hsien Lin**, "Design on ESD protection scheme for IC with power-down-mode operation," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 8, pp. 1378-1382, Aug. 2004.

[2] Ming-Dou Ker and **Kun-Hsien Lin**, "Double snapback characteristics in high-voltage nMOFETs and the impact to on-chip ESD protection design," *IEEE Electron Device Letters*, vol. 25, no. 9, pp. 640-642, Sept. 2004.

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[7] Ming-Dou Ker and **Kun-Hsien Lin**, "ESD protection design for I/O cells with embedded SCR structure as power-rail ESD clamp device in nanoscale CMOS technology," submitted to *IEEE Journal of Solid-State Circuits*.

[8] Ming-Dou Ker and **Kun-Hsien Lin**, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: design concept and circuit implementations," submitted to *IEEE Trans. on Circuits and Systems I*.

(B) International Conference Papers:

[1] Ming-Dou Ker, **Kun-Hsien Lin**, and Che-Hao Chuang, "MOS-bounded diodes for on-chip ESD protection in a 0.15-μm shallow-trench-isolation salicided CMOS

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[2] Ming-Dou Ker and **Kun-Hsien Lin**, "ESD protection design for IC with power-down-mode operation," in *Proc. of IEEE International Symposium on Circuits and Systems*, 2004, pp. 717-720.

[3] **Kun-Hsien Lin** and Ming-Dou Ker, "Design on latchup-free power-rail ESD clamp circuit in high-voltage CMOS ICs," in *Proc. of EOS/ESD Symposium*, 2004, pp. 265-272.

[4] **Kun-Hsien Lin** and Ming-Dou Ker, "ESD protection design for I/O cells in sub-130-nm CMOS technology with embedded SCR structure," in *Proc. of IEEE International Symposium on Circuits and Systems*, 2005, *in press*.

(C) Local Conference Papers:

[1] **Kun-Hsien Lin** and Ming-Dou Ker, "Whole-chip ESD protection design for IC with power-down application," in *Proc. of Taiwan ESD Conference*, 2003, pp. 142-147.

[2] **Kun-Hsien Lin** and Ming-Dou Ker, "Latchup-free power-rail ESD clamp circuit in high-voltage CMOS ICs ," in *Proc. of Taiwan ESD Conference*, 2004, pp. 25-30.

(D) Patents:

[1] 柯明道、**林昆賢**, "靜電放電防護電路," 中華民國發明專利, Nov. 2004. (專利證書號 # 224391)。

[2] 柯明道、**林昆賢**, "可避免鎖住效應之高壓積體電路電源間靜電放電箝制電路," 中華民國發明專利，申請中。

[3] Ming-Dou Ker and **Kun-Hsien Lin**, "ESD protection circuit for IC with power-down-mode operation," USA patent pending.

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[5] Ming-Dou Ker and **Kun-Hsien Lin**, "A silicon controlled rectifier for the electrostatic discharge protection," ROC and USA patent pending.

[6] Ming-Dou Ker and **Kun-Hsien Lin**, "ESD protection design against charge-device model ESD events," ROC and USA patent pending.