國 立 交 通 大 學

電機與控制工程學系

博 士 論 文

低電源電壓之高增益 CMOS 電荷幫浦式直流/直流穩壓系統積體電路設計

ICs Design of Low-Voltage High-Gain CMOS Charge Pump DC/DC Regulators

研 究 生: 胡致暉

指導教授: 張隆國 博士

中 華 民 國 九 十 六 年 八 月

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研 究 生: 胡致暉　　Student: Chih-Huei Hu

指導教授: 張隆國 博士　　Advisor: Lon-Kou Chang

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國立交通大學電機與控制學系（研究所）博士班

摘　　要

本論文研製之新型 CMOS 電荷幫浦式電路（charge pump circuits）利用電壓增益提升電路（pumping gain increase circuit）實現高效率直流轉直流的升壓輸出。傳統電荷幫浦式電路中，利用 MOS 開關當作電荷傳輸元件，因受電晶體本身臨界電壓（threshold voltage）的影響，多級串接架構的後級會有嚴重的基板效應（body effect）產生，使得可產生的最高電壓受到限制。文中所介紹的電壓增益提升電路可藉由電路規劃避開基板效應對升壓效率的限制，並且能克服輸出級跨壓損失的問題。因此，此電路的升壓輸出能確實隨著串接級數增加而提高。進一步利用電壓增益提升電路規劃指數升壓架構（exponential-gain structure），不同於傳統串接方式，指數升壓架構能以較少的級數實現更高的升壓輸出。

論文中並針對電阻性負載之電壓增益提升電路提出完整的分析進而推導出等效的電路模型。為了提高此等效模型的實用性，刻意將模型簡單化與規則化，讓使用者可以快速的得到不同級數之等效模型，用以規劃電壓增益提升電路的元件參數，同時亦可預測電路的輸出特性。此外，藉由此等效模型的數學分析，提出穩態時電路升壓輸出的數學式，並由數學式找出針對電容與串接級數最佳化的方式，使能有效的降低晶片面積。此模型與最佳化策略雖然是由電壓增益提升電路推導而來，但同樣適用於其他無內

部跨壓損失的改良型電荷幫浦式電路。除此之外，推導出的等效模型可進一步應用於建構具頻率補償的電荷幫浦式穩壓轉換器。論文中將藉由一設計範例，說明如何安排迴授網路以及合適的控制器參數，以達到所需求的電路特性與規格。

論文中以 0.35 微米互補式金氧半導體混合製程實現電壓增益提升電路，利用一般電池的電壓（1.5V）當作低電壓的輸入電源，模擬並量測實體晶片以驗證電路與指數升壓架構的可行性。此外，等效模型與最佳化的結果同樣透過量測被證實是實用的，而且正確性相當高，在多數情況下，由模型得到的穩態輸出值和晶片量測結果相比，最大誤差約為 5%。

ICs Design of Low-Voltage High-Gain CMOS Charge Pump DC/DC Regulators

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Abstract

This dissertation presents a novel CMOS charge pump circuits (CPCs) utilizing the pumping gain increase (PGI) circuits and the exponential-gain structure with high voltage transfer efficiency to generate boosted output voltages. By employing the PGI circuits, the threshold voltage problem of the MOSFET used as a switch is solved and the limitation of the diode-configured output stage is removed. Thus the boosted output voltage increases more linearly versus the pumping stage number. For the further application of the PGI circuits, an exponential-gain structure is also presented. By using this structure, fewer voltage pump stages are needed to obtain the required output voltage. For 1.5 V supply voltage operation, the simulation and experimental results show that the proposed designs would have good pumping efficiency with a low input supply such as one battery cell.

In addition, thorough analysis and a complete equivalent model of the PGI circuit with a resistive load are proposed. Based on the simple analytical model, the characteristics of the PGI circuit can be approximately predicted and the simple equations, which are useful for a pencil and paper design with an acceptable safety margin, can also be found for planning the desired circuit performance in the steady state. Furthermore, an optimized method of the PGI circuit for a resistive load is developed in terms of the stage number and the ratio between pump capacitors as optimization criterions. For 1.5 V supply voltage operation, reliability and

accuracy are demonstrated by comparisons between SPICE simulations of the PGI circuit and the corresponding results from the equivalent model. The model also has been validated by means of measurement taken from a test chip, and typically the relative errors are lower than 5 %. Finally, although the derivation of the model was based on PGI circuits, the design strategy can also be equally valid for any other improved CPC designs which are able to eliminate voltage drops within the inner stages and the output stage.

Finally, a design procedure of a charge pump regulator based on the equivalent model is illustrated with a design example. The presented charge pump regulator adopts the automatic pumping frequency scheme including a voltage-controlled oscillator, a charge pump circuit, an error detector, and a compensator. By employing the equivalent model, this regulator with a frequency compensation scheme can be implemented and all of the characteristics can be designed through manual and/or computer analysis. The final regulator provides a negative feedback to the pump operation and would insure the output voltage against the variations of loading conditions. From the design example, the accuracy has been demonstrated by comparing the simulation results between the equivalent regulator model and the practical regulator. The primary advantage of this modeling approach is the ease by which the regulator system can be analyzed. This permits that a fast charge pump regulator design would work in practice.

Acknowledgements

I would first like to express my deep appreciation to professor Lon-Kou Chang for his support, guidance, and advice during my graduate years at National Chiao Tung University (NCTU). He has also provided me with fresh incentive and encouragement in my research. Quite frankly, I know I could not have come this far without the close cooperation and the constructive criticisms of able people in the field like him. Besides, I take this opportunity to express my appreciation to my Ph. D. committee members Jin-Chern Chiou, Jium-Ming Lin, Chia-Chi Chu, Wei-Neng Chang, and Mu-Huo Cheng for giving me suggestions and recommendations. In addition, I would like to express my sincere gratitude to professor Wei-Neng Chang during my undergraduate years for the basic training on research. Meanwhile, the dissertation was supported by the National Chip Implementation Center (CIC) for fabricating my circuits.

I am grateful to extend my gratitude to the group members of Lab. 815, in Department of Electrical and Control Engineering, for providing stimulation and enjoyable working environment in my pursuit of Ph.D. degree. Finally, I give the greatest thankfulness to my family for the endless support and inspiration. Especially to my girlfriend, who kept encouraging and supporting me, with her omnipresent tolerance and love. I am aware that my accomplishment is primarily due to the unstinting support I have received from them.

Contents

List of Tables

List of Figures

Chapter 1

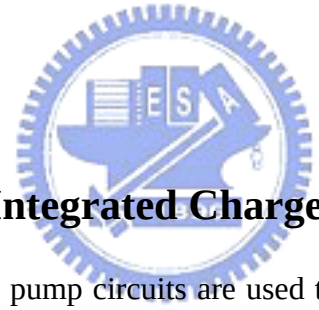
Introduction

1.1 Motivation

In recent years, progress has been made towards small, inexpensive, and mobile equipments. The new-generation portables require the use of a single Li-ion cell (i.e. 3.6V normally) or batteries (1.5 V – 3 V) for system power. The growing portable equipment market has created a strong demand for DC/DC converters which can fit the size of the equipment. In addition, in portable mixed-mode systems where the power consumption is critical, the converters that can operate in low supply voltage environments are very desirable and crucial.

In view of the device level, dimensions of transistors have been scaled down toward the nanometer region and supply voltages for CMOS integrated circuits have been continuously reduced due to the reliability and power consumption issues. Lower supply voltages result in lower power consumptions so that chip designs migrate to the lower voltage level. Unfortunately, reducing the supply voltage does not offer similar benefits for analog circuits. In order to save the chip area or have the high-speed performance, some circuits are fabricated in advanced low-voltage processes but supplied by higher voltage levels. Besides, some other peripheral components or ICs in an electronic system are still operated in higher voltage environments, such as 3.3 V or 5 V. Thus, a voltage generator circuit, which can operate with a low supply voltage, is demanded to generate a higher voltage than the supply voltage for mixed-voltage operations.

Charge pump circuit (CPC) is a kind of voltage generators and has been shown to be an effective technology to provide the solution for above demands to convert an input voltage upward to a higher one with either a positive or a reverse polarity on a chip. Since charge pump circuits use capacitors as energy storage devices instead of magnetic components, the converters are amenable to compact and lower cost designs without electromagnetic interference (EMI) problems. For low power designs, the capacitors needed by charge pump circuits could be small enough to be fabricated in integrated circuits. Thus, charge pump circuits are suitable for portable systems with only one battery as its power supply and for low-voltage chip design. With the continued shrinking of handheld devices such as cell phones, PDAs, pagers and laptops, the use of charge pump converters is becoming more attractive over inductive based structures.



1.2 Applications of Integrated Charge Pump Circuits

Generally, integrated charge pump circuits are used to provide output voltages higher than the power supply. They have been extensively applied in nonvolatile memories for many years, such as Electrically Erasable Programmable Read Only Memory (EEPROM) and flash memory that require a high voltage to program the floating-gate devices for rewriting data [1]-[14]. Recent development of low voltage circuit design, charge pump circuits can also be adopted to power ICs and analog switch circuits, such as switched-capacitor filters and A/D converters, for generating high voltages to control MOS gates at high or low level in order to perform “ON” or “OFF” operations [15]-[16].

1.2.1 EEPROM and Flash Memory

For electrical re-programmability in floating-gate devices, EEPROMs and flash memories

depend on a technology mechanism referred to “Fowler-Nordheim (F-N) tunneling” or “cold electron tunneling”. The effect of tunneling allows electrons to pass through the energy barrier at the silicon-silicon dioxide (Si-SiO_2) interface at a lower energy than the 3.2 eV required passing over this energy barrier. Based on the F-N tunneling mechanism, the floating gate tunneling oxide cell was developed by Intel and has been one of the most common EEPROM cell [8]-[9]. As shown in Fig. 1.1, a basic cell of an EEPROM contains a select transistor and a double polysilicon storage transistor with a floating polysilicon gate isolated in silicon dioxide capacitively coupled to a second polysilicon control gate which is stacked above it. A thin dielectric layer between the floating gate and the source enables the flow of electrons into and from the floating gate during program/erase operations, by means of F-N tunneling.

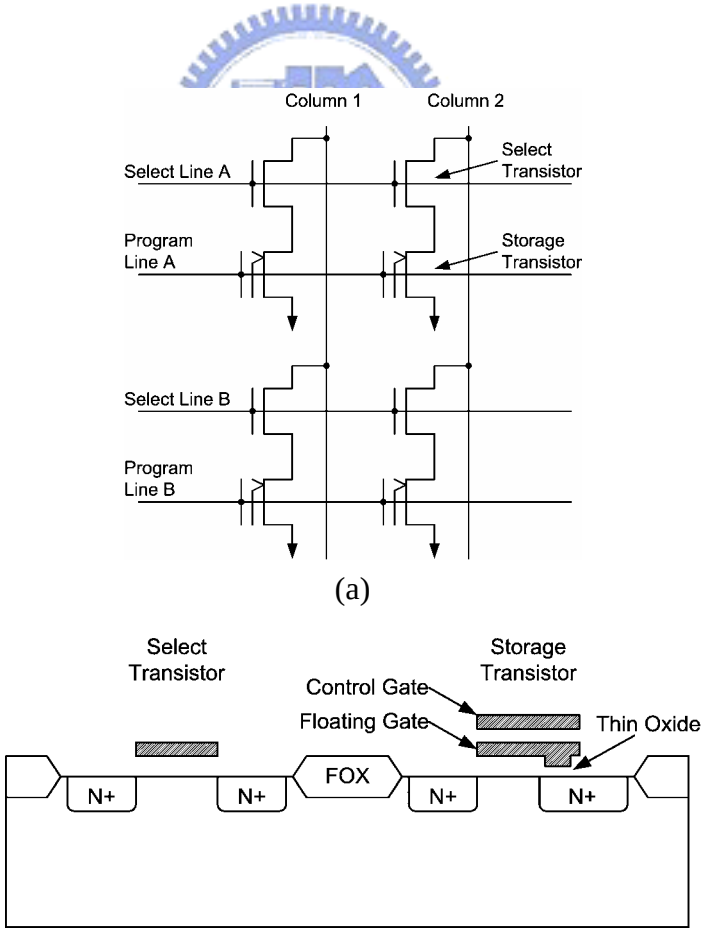
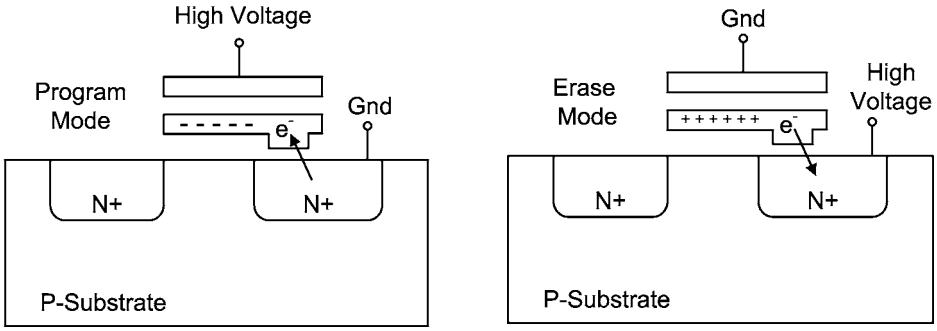


Fig. 1.1 (a) Circuit symbol and (b) cross section of a basic EEPROM cell [8].

In the program mode, a positive high voltage is applied to the control gate of the cell, while the drain is floating and both the source and the substrate are grounded. The floating gate is charged negatively with electrons tunneling from the source through the thin oxide. The stored negative charge on the floating gate shifts the threshold voltage of the transistor toward the positive value. In a subsequent program operation, the transistor will not conduct channel current so that the transistor will be "off". Fig. 1.2(a) shows the floating gate transistor during programming. The erase operation removes electrons from the floating gate by applying a positive high voltage at the source, while the drain is floating and both the control gate and the substrate are grounded. As shown in Fig. 1.2(b), electrons tunnel from the floating gate to the source leaving the floating gate relatively more positively charged. Thus, the threshold voltage is shifted in the negative direction. During subsequent erase operation, the channel current would flow so that the transistor will be "on". Fig. 1.3 shows the shift in the i_D–v_{GS} characteristic of a floating-gate transistor as a result of programming or erasing. To read the content of the memory cell, a suitable voltage v_{GS}, employed mainly by the supply voltage, somewhere between the low and high threshold voltages (V_{T0} and V_{T1}) can be applied.



(a) (b)

Fig. 1.2 (a) Program configuration and (b) erase configuration of a double polysilicon storage transistor in a basic EEPROM cell [10].

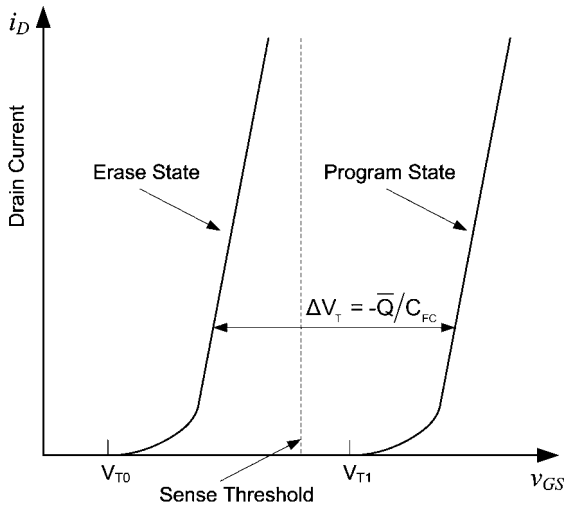


Fig. 1.3: Illustrating the shift in the $i_D - v_{GS}$ characteristic of a floating-gate transistor as a result of programming or erasing [11].

In the conventional scheme, F-N tunneling erase has been achieved by raising the source junction to a positive high voltage and grounding the control gate. The source junction is formed to be a double diffusion structure in order to obtain a high breakdown voltage. The deeply formed drain junction prevents channel length scaling, which is required for high-density memory cells. The negative-gate-biased source erase scheme can overcome this problem by applying a negative voltage to the control gate to obtain F-N tunneling. The source voltage necessary for F-N tunneling can be reduced to the supply voltage V_{DD}. Fig. 1.4 shows a conventional double diffusion structure compared with the negative-gate-biased source erase scheme, which has the benefit of scaling down the channel length.

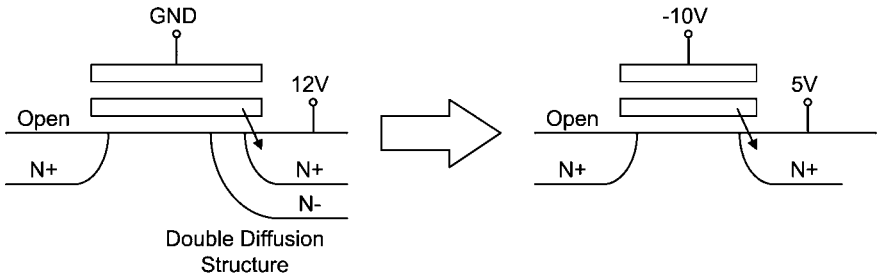


Fig. 1.4 Negative-gate-biased source erase scheme [1].

Due to the two-transistor type cell, byte-write and byte-erase abilities are accomplished by the EEPROM. However, a major disadvantage of the EEPROM is in a large size of the two-transistor memory cell and that has kept the cost high. Flash memory is a direct derivate of the one-transistor cell EPROM (Erasable Programmable Read Only Memory). It resulted from innovative cell designs and improved technology that allowed the one-transistor cell EPROM to be reprogrammed electrically in the system. Many of the flash memory cells that have developed use the split gate concept in which the separate select and storage transistor gates of the EEPROM are merged into a single device with the channel region shared by the two gates [10]-[12]. Thus, the flash memory has a smaller chip size and a higher density compared to EEPROM. However, unlike EEPROMs with byte-write and byte erase abilities, the flash memory only can be programmed or erased by section.

No matter which nonvolatile memory scheme is used, a high voltage with either a positive or a reverse polarity to obtain F-N tunneling is critical in a floating gate structure. As these voltages can be provided externally or generated within the device, memory chips can be divided into double-supply and single-supply devices. In the former case, one supply pin (V_{DD}) is used for the general-purpose supply, and the other pin (V_{PP}) is devoted to program/erase operations (obviously, V_{PP} is higher than V_{DD}). In the latter case, only the V_{DD} pin is present, and all other voltages are generated on-chip.

The charge pump circuit is a common on-chip voltage generation for producing any voltage between ground and the power supply on a memory chip [13]-[14]. Furthermore, it is also possible to generate high voltages that are below ground and above the power supply value for creating F-N tunneling. A block diagram of a common flash EEPROM is shown in Fig. 1.5. In this figure, charge pump circuits not only generate large positive and negative voltages (V_H) of up to 20 V for programming and erasing but also provide medium voltage (V_P) of around 5 V to control the operation mode. Since V_H and V_P are generally applied to the control gate and the source junction, respectively, the drivability of the V_H generator can be set lower

than the V_P one. In addition, a reference voltage is needed to control V_H and V_P to achieve the required stable value which must be guaranteed for accurate read/write/erase operation of the memory cell.

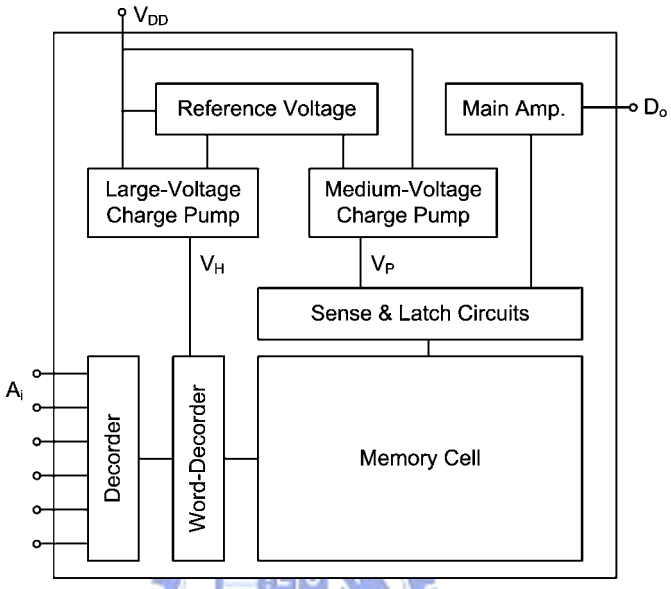


Fig. 1.5 Block diagram of a common flash EEPROM [14].

1.2.2 Switch Capacitor System

Switched-capacitor (SC) technique is an efficient way of implementing analog functions in CMOS technology due to its intrinsic resolution and accuracy. The elements required for the realization of SC circuits are capacitors, switches, and op amplifiers. However, the supply voltage reduction of modern ICs due to technology scaling has a drastic impact on switched-capacitor circuit performance. This is not only due to dynamic range reduction but also because, below a certain supply voltage, switches cannot be driven by adequate overdrive, and their switch-on condition cannot be easily guaranteed over acceptable signal ranges [17]. Thus, conventional CMOS transmission gates may no longer be adequate or even functional as analog switches if the signal swing of the switch control is kept between the nominal supply voltages.

Recently, switched-capacitor circuits at very low supply voltages could only be realized either in a special process with extra low threshold voltage (V_T) of transistors or by using an on-chip voltage multiplier, which generates higher switch control voltages to drive critical switches. The voltage multiplier needed for SC designs is often derived from the EEPROM technology by means of using charge pump circuits and the structure of high voltage generator. For example, as shown in Fig. 1.6, a common high voltage generator consists of five circuit blocks: the charge pump circuit (CPC), the low-pass filter (LPF), the high voltage sensor (HVS), the voltage-controlled oscillator (VCO), and the non-overlapped clock buffer (NOCB). A negative feedback loop is formed to stabilize the output voltage $V_{out,H}$ and the pump ability is adjusted by the frequency of non-overlapped clocks. The voltage sensor can detect $V_{out,H}$ and transfer it to a voltage V_c for controlling the voltage-controlled oscillator. If $V_{out,H}$ is less than the desired value, the voltage V_c generated by HVS is fed to VCO for increasing the frequency of non-overlapped clocks through NOCB. Thus, $V_{out,H}$ will be pumped to the desired value. Otherwise, the clock frequency is decreased for pushing down $V_{out,H}$ to the desired lower value [18]-[21].

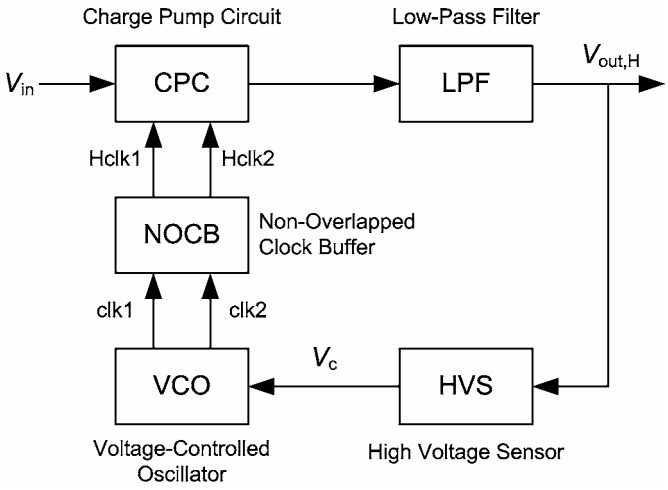


Fig. 1.6 Architecture of a common high voltage generator.

Fig. 1.7 illustrates the example of a low-voltage switched capacitor system. The signal paths are fully differential to maximize noise immunity against disturbances from supplies and substrate when digital circuits and switch circuits are on the same chip. The analog signal paths operate directly between the two main power supply lines V_{DD} and V_{SS}. To maximize SNR, a signal swing extending near the supply voltages is necessary. The analog switches are implemented with NMOS transistors so that an on-chip high-voltage generator is used to generate the high-voltage V_{HH} required to completely turn on the NMOS switches.

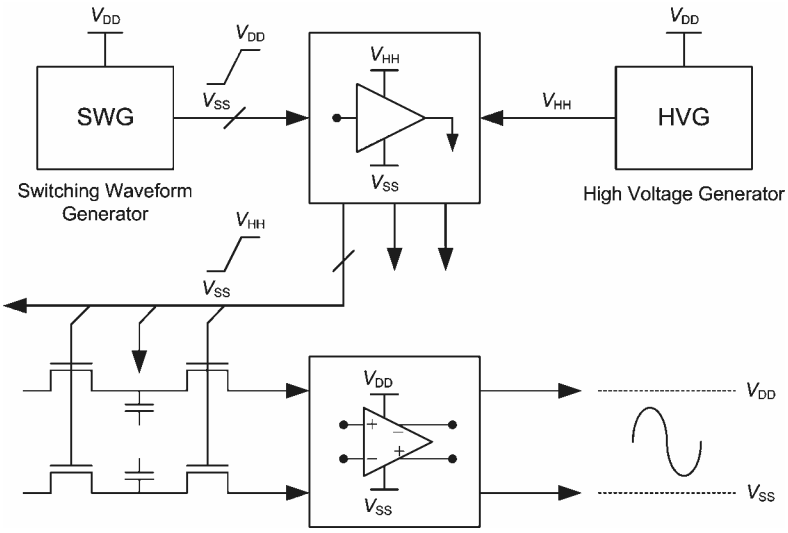


Fig. 1.7 An example for low-voltage switched-capacitor system [18].

1.3 Contributions of the Dissertation

A charge pump styled voltage generator utilizing the exponential-folds structure and the pumping gain increase (PGI) circuits with high voltage transfer efficiency is proposed. PGI circuits used in the linear DC/DC converter are proposed to solve the threshold voltage problem and the limitation of the diode-configured output stage so that the boosted output voltage increases more linearly versus the pumping stage number. With the exponential-folds structure, fewer voltage pump stages are needed to obtain the higher output voltage and

further improve the voltage pumping gain. Especially, this design still has good efficiency with a low input supply voltage such as one battery cell.

In addition, a complete equivalent model of high efficiency PGI circuits with a resistive load and the corresponding thorough analysis are proposed. Based on this analytical model, characteristics of PGI circuits can be approximately predicted and several handy equations, which are useful for a pencil-and-paper design, can also be found for planning the desired circuit to achieve good enough performance with an acceptable accuracy tolerance in the steady state. In addition, an optimized design method for PGI circuits with a resistive load is developed in terms of the total number of gain stages in the design and the ratio between pump capacitors.

Furthermore, since the proposed model provides a good substitute for a practical PGI circuit for mathematical analysis. By using this equivalent model, a feedback control scheme of the charge pump regulator can be easily planned for adjusting operation to obtain a desired output voltage under different conditions. A design procedure of a charge pump regulator is presented by an example to describe and demonstrate the feasibility.

Briefly, the thesis illustrates several solutions of charge pump designs, so that charge pump styled voltage generators for varied low-voltage applications with good enough performance can be obtained easily.

1.4 Organization

The thesis is organized into six chapters.

Chapter 1 is the introduction and indicates the most popular application about charge pump styled voltage generators. Chapter 2 introduces previous studies and explains their features and limitations. The survey focus on some typical circuit topologies in charge pumps. Chapter 3 presents the pumping gain increase circuits dealing with the augmented threshold voltage problem in the pump stages and depicts a new idea of exponential-folds structure to obtain a higher output voltage with fewer voltage pump stages. Chapter 4 illustrates an equivalent model of PGI circuits for a pencil-and-paper design. Characteristics of PGI circuits can be designed effectively through this model to achieve good enough performance with an acceptable accuracy tolerance in the steady state. Chapter 5 depicts a design procedure with consideration of the equivalent model to plan a charge pump regulator. A design example is used to describe and demonstrate the feasibility. Chapter 6 summarizes the main results of this dissertation. Then, some suggestions for future works are also addressed in this chapter.

Chapter 2

A Survey of Previous Charge Pump Circuits

2.1 Introduction

In modern mixed-mode circuit designs, low-voltage and small-size voltage generators have been extensively required. Charge pump circuits (CPCs) can provide an effective technology required to meet these demands to convert the voltage upward to a higher one with either a positive or a reverse polarity. Since CPCs use capacitors as energy storage devices instead of magnetic components, the voltage generators have no electromagnetic interference (EMI) problems and are amenable to compact and lower cost designs. For low power designs, the capacitors required by CPCs can be small enough to be fabricated in integrated circuits.

Most charge pumps are based on the circuit proposed by Dickson that uses diode-connected MOSFETs as charge transfer devices [22]-[25]. In this design, the maximum output voltage is limited by the threshold voltage V_t loss problem of the diode-connected MOSFETs due to the body effect. When more pump stages are employed for producing higher pumping voltages, the body effect will be getting more serious. Therefore, the voltage pumping gain will be further reduced and the pumping efficiency will be highly degraded.

In recent years, several modifications of the Dickson CPC have been proposed to alleviate the augmented threshold voltage problem. It is possible to use process topology to reduce the body effect problems [1], [26]-[29]. Without making alterations in process, several attempts

have been made to alleviate the V_t loss problem by circuit topologies. The four-phase pulse CPC is the favorable style in the electronics market [1], [30], [31]. However, this circuit uses a more complicated timing control scheme. Some designs use isolated body techniques [6], [32], but these techniques require extra cost due to utilization of triple-well technology that increases the layout and process complexity. Additional gate biasing circuits used to dynamically control the transfer devices are also popular in charge pump designs [33], [34]. Nevertheless, the pumping gain is still degraded by the V_t loss problem in some of these circuits [33]-[36]. In addition, another voltage drop problem also exists at the output stage and degrades the total pumping efficiency further. In this chapter, some typical topologies based on Dicksons CPC will be introduced and discussed.

2.2 Dickson Charge Pump Circuit

2.2.1 Dickson CPC

The *N*-stage positive Dickson CPC using pn-junction diodes as the charge transfer devices is shown in Fig. 2.1 [22]. The voltage at each node is pumped by the charge transferred along the diode chain as the coupling capacitors are successively charged and discharged during each half of the clock cycle. Since voltages in the diode chain are not reset after each pump cycle, the average potentials of all nodes increase progressively from the input to the output.

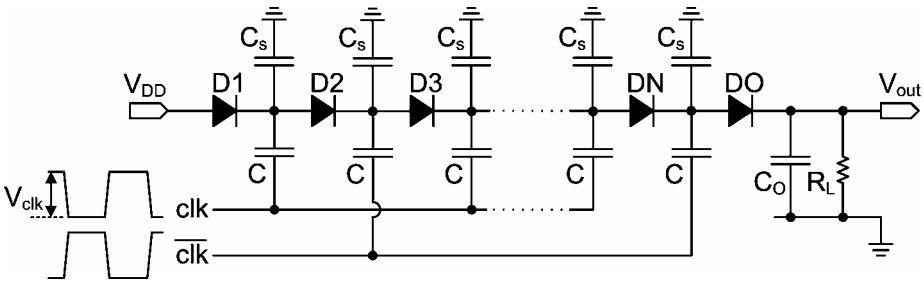


Fig. 2.1 An *N*-stage positive Dickson charge pumps implemented by pump capacitors in parallel with diode chain [22].

In this structure, C and C_s are pump capacitors and stray capacitors, respectively, and D_n is the pn-junction diode in the n-th stage. The supply voltage is V_{DD} and the circuit is driven by two anti-phase clock signals clk and $\overline{\text{clk}}$ with amplitude V_{clk} which is usually equal to V_{DD}. When clk is high and $\overline{\text{clk}}$ is low, the diodes of even stages are forward bias and transfer charges to the succeeding pump capacitors. Similarly, when clk is low and $\overline{\text{clk}}$ is high, the diodes of odd stages are forward bias and transfer charges to the succeeding pump capacitors. After several cycles of pump operations, the output voltage of this charge pump circuit shown in Fig. 2.1 can be pumped high by charges pushed from the power supply to the output node stage by stage.

Using the steady-state analysis from the simple model of the Dickson charge pump [22] – [24], the voltage fluctuation $\Delta V_{n,\text{diode}}$ in the n-th stage associated with the voltage division resulting from a clock coupling capacitance C and a stray capacitance C_s can be expressed as

$$\Delta V_{n,\text{diode}} = \left(\frac{C}{C + C_s} \right) V_{clk} - \frac{I_{out}}{f\left(C + C_s\right)} - V_{diode} \qquad (2.1)$$

where f is the clock frequency, I_{out} is the output current, and V_{diode} is the turn-on voltage of the pn-junction diode (the forward bias diode voltage or the diode cutoff voltage). In (2.1), the first term is the common expression of the voltage swing occurring at each pump node contributed by the clock source, clk or $\overline{\text{clk}}$, through the associated pump capacitor C. The second term is shown the voltage drop due to I_{out}. If C_s and I_{out} are small enough and C is large enough, C_s and I_{out} can be ignored from (2.1). Since V_{clk} is usually the same as the normal power supply voltage V_{DD}, the voltage fluctuation of each pump node can be simply expressed as

$$\Delta V_{n,\text{diode}} \approx V_{clk} - V_{diode} = V_{DD} - V_{diode} \qquad (2.2)$$

Thus, $\Delta V_{n,\text{diode}}$ can be regarded as the pumping gain of the n-th stage. In each stage, the necessary condition for the boost function of the charge pump circuit is that $\Delta V_{n,\text{diode}}$ must be

larger than zero. With the condition that V_{diode} and $\Delta V_{n,\text{diode}}$ are constants, the total pumping voltage in an N-stage Dickson charge pump circuit with a load can be obtained as

$$V_{\text{out}} - V_{\text{DD}} = N\left(\Delta V_{n,\text{diode}}\right) - V_{\text{diode,DO}} = N\left[\left(\frac{C}{C+C_{\text{s}}}\right)V_{\text{clk}} - \frac{I_{\text{out}}}{f\left(C+C_{\text{s}}\right)} - V_{\text{diode}}\right] - V_{\text{diode,DO}} \tag{2.3}$$

Hence, the output voltage of the N-stage diode charge pump circuit can be expressed as

$$V_{\text{out}} = V_{\text{DD}} - V_{\text{diode,DO}} + N\left[\left(\frac{C}{C+C_{\text{s}}}\right)V_{\text{clk}} - \frac{I_{\text{out}}}{f\left(C+C_{\text{s}}\right)} - V_{\text{diode}}\right]. \tag{2.4}$$

where V_{out} is the output voltage, V_{DD} is the input supply voltage, V_{clk} is the voltage amplitude of the pump clock signals, V_{diode} is the voltage drop of a forward bias diode, N is the total stage number, I_{out} is the output current loading, and f is the frequency of the driving clock signals.

Through the similar structure, Fig. 2.2 shows the N-stage negative Dickson charge pump circuit using pn-junction diodes as the charge transfer devices. As the above description, the output voltage of the N-stage charge pump circuit without output loading current can be expressed as

$$V_{\text{out}} = -N\left[\left(\frac{C}{C+C_{\text{s}}}\right)V_{\text{clk}} - V_{\text{diode}}\right] + V_{\text{diode}} \tag{2.5}$$

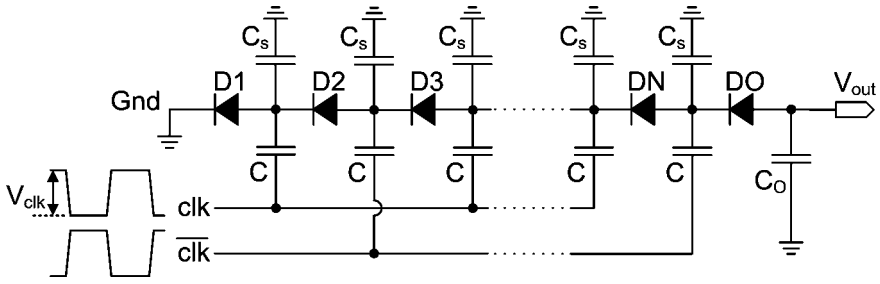


Fig. 2.2 An N-stage negative Dickson charge pumps implemented by pump capacitors in parallel with diode chain.

However, it is difficult to implement isolated diodes in the common silicon substrate. In the past, some nonvolatile memory products were developed in a p-well process in which the whole substrate could be brought to the high programming voltage such that the drain-to-p-well junction of the NMOS transistor can be used as diode. However, this is unacceptable if the high voltage is generated on chip [24]. In other words, the charge pump circuit with diodes shown in Fig. 2.1 and Fig. 2.2 can not be easily fabricated into the standard CMOS process. Therefore, in the MOSFET technology, diode-connected transistors are being substituted for the diode chain and are used to transfer the charge in one direction. Fig. 2.3 shows the *N*-stage Dickson charge pump circuit implemented by pump capacitors in parallel with diode-connected MOSFETs.

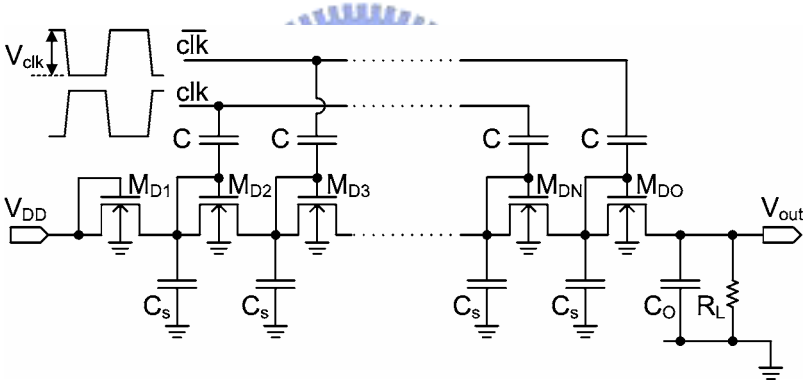


Fig. 2.3 An *N*-stage Dickson charge pumps implemented by pump capacitors in parallel with diode-connected MOSFETs.

When the diode-connected MOSFET is forward bias, the drain-source voltage drop (V_{ds}) across the NMOS-diode is identical to its threshold voltage V_{tn}. Neglecting the body effect, the voltage fluctuation ΔV_n of the *n*-th pump stage and the output voltage of the *N*-stage Dickson charge pump circuit have been derived as

$$\Delta V_n = \left(\frac{C}{C + C_s} \right) V_{clk} - \frac{I_{out}}{f\left(C + C_s\right)} - V_{tn,MDn} \tag{2.6}$$

and

$$V_{\text{out}} = V_{\text{DD}} - V_{\text{tn,MDO}} + N\left[\left(\frac{C}{C+C_{\text{s}}}\right)V_{\text{clk}} - \frac{I_{\text{out}}}{f\left(C+C_{\text{s}}\right)} - V_{\text{tn,MD}n}\right] \tag{2.7}$$

where $V_{\text{tn,MD}n}$ denotes the threshold voltage of the n-th diode-connected MOSFET MDn.

2.2.2 Equivalent Model of the Dickson CPC

From (2.7), an extremely simple equivalent circuit for the Dickson charge pump is shown in Fig. 2.4 and the output voltage can be derived as

$$V_{\text{out}} = V_{\text{eq}} - R_{\text{eq}} I_{\text{out}} \tag{2.8}$$

where

$$V_{\text{eq}} = V_{\text{DD}} - V_{\text{tn,MDO}} + N\left[\left(\frac{C}{C+C_{\text{s}}}\right)V_{\text{clk}} - V_{\text{tn,MD}n}\right] \tag{2.9}$$

$$R_{\text{eq}} = \frac{N}{f\left(C+C_{\text{s}}\right)} \tag{2.10}$$

In (2.8), V_{eq} and R_{eq} are the equivalent open-circuit output voltage and the equivalent output series resistance, respectively [23]-[25]. There will be a voltage ripple at the output due to the discharging of the output capacitance C_{O} by the resistive load R_{L}.

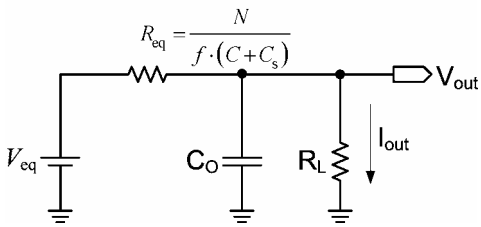


Fig. 2.4 Equivalent model of the Dickson charge pump.

In deriving this model for the voltage multiplier, it has been assumed that all of the pump capacitors are completely charged and discharged with the same drain-source voltage drop across each diode-connected MOSFET. Thus, the output voltage keeps increasing with increasing stage number and theoretically any pump voltage can be generated.

In practice this is not the case due to the undesirable characteristic of the diode-connected MOSFET, such as internal series resistance and the body effect. Since the model is based on the approximation of the uniform threshold voltage, the error introduced by this approximation will of course be generated. This results in unequal voltage drops across each pump stage and a nonlinear manner with load current [23]-[25].

2.2.3 Limitation of the Dickson CPC

In a standard CMOS process, all NMOS transistors have a common body at p-substrate so that the body potentials V_b will be equalized. Thus, the problem of body effect cannot be disregard in charge pump circuits based on diode-connected MOSFETs. In Fig. 2.3, since the substrate terminal is grounded, the common body potential V_b is equal to zero. Thus, different source-substrate voltages (V_{sb}) are applied to diode-connected MOSFETs and cause different threshold voltages on NMOS transistors. The dependence of the threshold voltage on the source-substrate voltage is expressed as

$$V_t = V_{T0} + \gamma \cdot \left[\sqrt{V_{bs} + 2\phi_f} - \sqrt{2\phi_f} \right] \tag{2.11}$$

where V_{T0} is the threshold voltage for V_{bs} = 0 V, ϕ_f is the band bending in the substrate needed to invert the silicon surface, and γ denotes the body effect coefficient.

In (2.11), it can be seen that as the node voltage of each stage increases by the charge pump, the increased reverse-biased source-substrate junction voltage will increase the threshold voltage of the NMOS transistor due to the body effect. Thus, from (2.6) to (2.10), the voltage fluctuation ΔV_n of each pump stage is not a constant because $V_{tn,MDn}$ is enlarged by the body effect, which increases as more pump stages are used. The increased threshold voltage V_{tn} results in the degradation of ΔV_n and that can be given as

$$\Delta V_1 > \Delta V_2 > \cdots\cdots\cdots > \Delta V_{N-1} > \Delta V_N \tag{2.12}$$

where

$$V_{tn,MD1} < V_{tn,MD2} < \cdots\cdots\cdots < V_{tn,MDN} < V_{tn,MDO} \quad (2.13)$$

The maximum voltage drop occurs in the output stage, referred to $V_{tn,MDO}$, because the most serious body effect occurs on MDO due to a large build up of V_{sb}. Thus, the pumping efficiency of the succeeding stage will be less than that of the forestages.

When more pumping stages are used, the V_t augmentation problem will be more serious and will result in the degradation of the output voltage [6], [32]-[36]. It can be obvious that if more cascaded pump stages are added in, $V_{tn,MDN}$ in the last pump stage and $V_{tn,MDO}$ in the output stage will increase. Once ΔV_N in the last stage reduces to zero, V_{out} will start to saturate. In other words, if the total pump stage number N is increased further, the pumping efficiency of the Dickson charge pump circuit is degraded and the maximum output voltage is limited. Thus, the output voltage cannot be maintained as a linear function of the number of stages and the pumping efficiency will be highly degraded as the number of stages increases further.

In the low-voltage system where V_{DD} and V_{clk} are small, since the threshold voltage cannot be scaled down as the scaling trend of the supply voltage, the V_t augmentation problem makes a great impact on the final pump voltage and the pumping gain will be further reduced [6], [31]-[33]. The loss of pumping gain also results in an increased power loss [35]. This low efficiency restricts the application of the Dickson charge pump structure to low supply voltage systems.

2.3 Improved Charge Pump Circuits based on Process Topology

Several modified charge pump circuits based on the Dickson structure were reported to enhance the pumping efficiency [1], [6], [23]-[36]. Based on process techniques, several attempts have been made to implement fully isolated p-n junction diodes in the Dickson charge pump circuit shown in Fig. 2.1 [1], [26]-[29]. Besides, in the case of using MOS-

diodes as transfer devices, some processes make use of ion implantations to adjust the threshold voltage of the transistor to the desired value and to improve the punch-through feature of transistors.

2.3.1 Normal Transfer Device

Traditionally, a p^+/n-well diode with the grounded p-substrate as shown in Fig. 2.5 is a kind of p-n junction diodes in the standard CMOS process; nevertheless, an undesired parasitic p-n junction exists between the n-well and the grounded p-type substrate. If the voltage on the cathode of the p^+/n-well diode is larger than the junction breakdown voltage between the n-well and the grounded p-substrate, the charge on the cathode will leak to ground through this parasitic p-n junction. Besides, it can also be found that the p^+/n-well diode exhibits a vertical parasitic bipolar transistor, which is in part responsible for leakage currents.

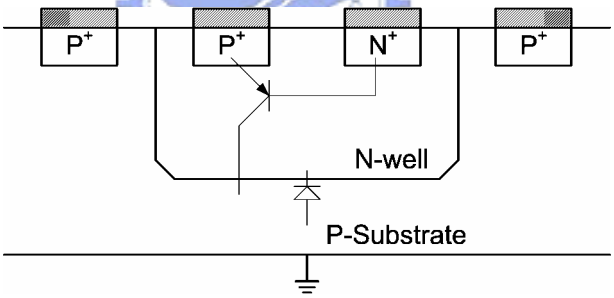
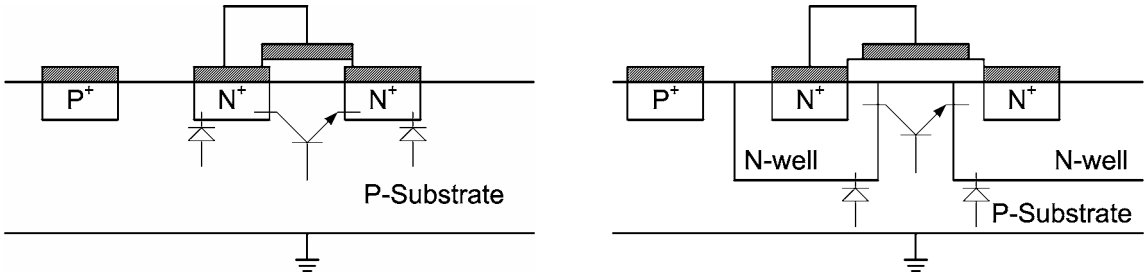


Fig. 2.5 Cross-section of an p^+/n-well diode created on an n-well using p^+ and n^+ diffusions with the grounded p-substrate.

A diode-connected NMOS transistor, whose gate and drain are connected, with the grounded p-substrate is another kind of p-n junction diodes in the standard CMOS process as shown in Fig. 2.6(a). Similarly, an undesired p-n junction parasitizes between the n^+ region (source/drain) and the grounded p-type substrate. If the voltage on the cathode or anode of the transistor is larger than the junction breakdown voltage between the n^+ region and the grounded p-type substrate, the charge will also leak to ground through this parasitic junction.

It is also found in this structure that the lateral parasitic bipolar transistor would result in leakage currents.



(a) (b)

Fig. 2.6 Cross-section of an diode-connected NMOS transistor with the grounded p-substrate. (a) Standard NMOS transistor. (b) High voltage NMOS transistor.

Another high breakdown voltage structure of an NMOS transistor is that the source and drain regions are surrounded by separate n-wells shown in Fig. 2.6(b). The n-well is lower doped than conventional n-diffusions thus allowing the possibility of a higher breakdown voltage. Using this power NMOS to substitute for a standard NMOS in diode-connected style, it can be seen that higher breakdown voltages of the power NMOS will reduce the limitation from undesired junctions. However, the layout is atypical in that the active layer was added beneath the gate in order to achieve thin oxide in the gate to n-well overlap region.

Consequently, while above normal transfer devices are used in the Dickson charge pump circuit, the maximum output voltage and the pumping efficiency will be limited by the breakdown voltage of the undesired junction. In addition, parasitic devices are in part responsible for leakage currents.

2.3.2 Utilizing Body Diode as the Transfer Device

The implementation of silicon-on-insulator (SOI) MOSFET body diodes in place of typical transfer devices reduces the voltage drop across each stage and increases the voltage efficiency of the charge pump [27]. In an SOI process, each MOSFET body is isolated from

neighboring transistors due to the buried oxide (BOX) layer. The cross section of an n-channel SOI transistor is shown in Fig. 2.7, and the two p-n junctions of this structure form a back-to-back diode configuration as indicated in the drawing.

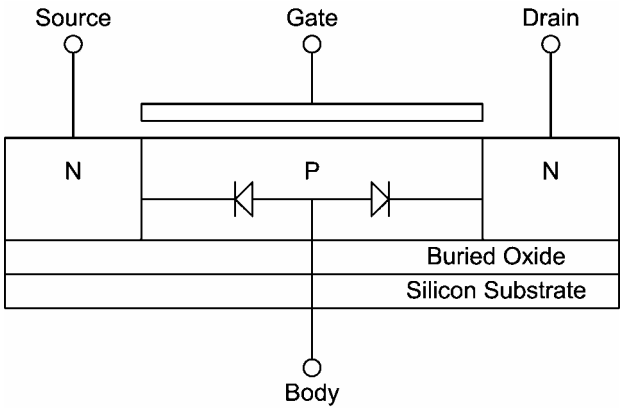


Fig. 2.7 Cross-section of an SOI n-channel device for body diode connection.

For body diode implementation, the floating-body of the n-channel is connected to the drain, thus shorting the junction from the p-type body to the n-type drain. Hence, only one diode exists between the gate-drain-body connection and the source. In this configuration, the gate-drain-body connection will serve as the anode and the source as the cathode. Fig. 2.8 shows the two-dimensional structure of an SOI NMOS body-diode under gate-drain-body connection. The vertical white line represents the p-n junction of the body diode, where the right side is the anode or p-type region of the NMOS structure and the left side is the cathode or n-type source region.

The build-in voltage across this silicon body diode is approximately 0.4 V. Comparing with the transfer device realized by transistors in the diode-connected style, using body diodes can prevent the augmented threshold voltage problem as the pump stage number increases. Furthermore, since the device is isolated to others by the insulation layer in the SOI CMOS process, charge pump circuits realized by the body diode can pump the output voltage higher without the limitation of parasitic p-n junctions, such as the breakdown voltage of undesired

junctions or leakage currents. However, the voltage pumping gain per stage is still reduced by the build-in voltage of the body diode, and the SOI CMOS process is more expensive than the common bulk CMOS process.

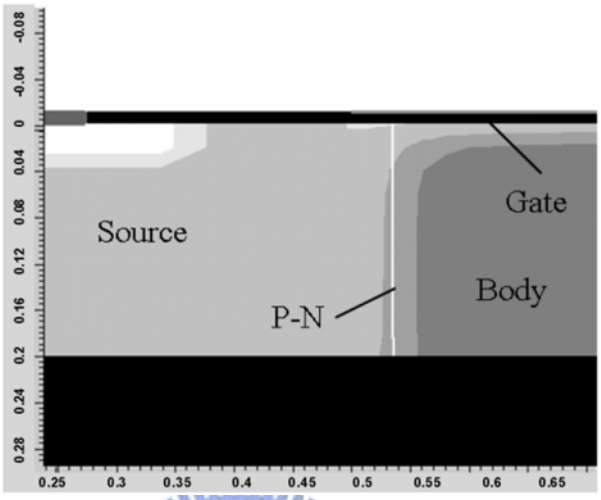


Fig. 2.8 2-D structure of an SOI NMOS body-diode [27].

2.3.3 Utilizing Polysilicon Diode as the Transfer Device

In the past, it is difficult to implement fully isolated p-n-junction diodes in the common silicon substrate. In the recent sub-quarter-micron standard CMOS process with shallow trench isolation (STI) [37], the polysilicon diode, which is fully isolated from the silicon substrate, can be implemented and applied in the charge pump circuit [28].

As shown in Fig. 2.9, the polysilicon diode can be realized on the polysilicon layer in the recent STI process which has separated doping impurities for PMOS and NMOS gates. The STI layer is located above the silicon substrate. The intrinsic polysilicon layer is deposited on the STI layer, and then the p-type and n-type impurities are doped into the intrinsic polysilicon layer to form the PMOS gate and the NMOS gate, respectively. An extra un-doped (intrinsic) polysilicon region (i) can be inserted between the p-type and n-type doped polysilicon regions. The length L_c of the un-doped region can be used to adjust the I–V

characteristic of the polysilicon diode.

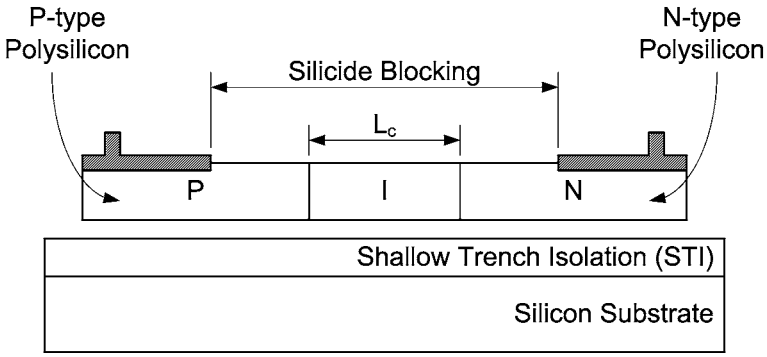


Fig. 2.9 Schematic cross section of the polysilicon diode.

Because the polysilicon diode is implemented on the STI layer, it is isolated from the silicon substrate. Charges on the anode and the cathode of the polysilicon diode would not leak to the silicon substrate. In addition, the parasitic capacitance of the polysilicon diode formed on the STI layer has been studied in [38], which is smaller than those of traditional p^+/n-well junction diodes and MOS diodes. Therefore, the polysilicon diode can be applied to the charge pump circuit without the limitation of parasitic junctions for achieving better pumping efficiency.

2.3.4 Utilizing Triple-Well Technique

Triple-well technology has become popular for charge pump circuit fabrication as it allows easier handling of the negative voltages necessary when the negative-gate erase technology is adopted. With this kind of technology shown in Fig. 2.10, p-well/n^+ junction diodes can be used with no risk of charge injection into the substrate, since the p-well region is isolated from the p-substrate by a reverse-biased n-well. In addition, when the triple-well process is used, the gate-drain connection for a MOS diode, which implements a charge transfer device, can also be applied with isolation. Therefore, based on the triple-well technology, p-well/n^+

junction diodes or MOS diodes applied to the charge pump circuit would reduce the leakage current from parasitic junctions.

However, if the triple-well p-well/n^+ junction diode is used, the pumping voltage per stage is still reduced by the build-in voltage. If the triple-well MOS diode is applied, the V_t augmentation problem still exists and the pumping efficiency of the succeeding stage is still less than that of the forestage.

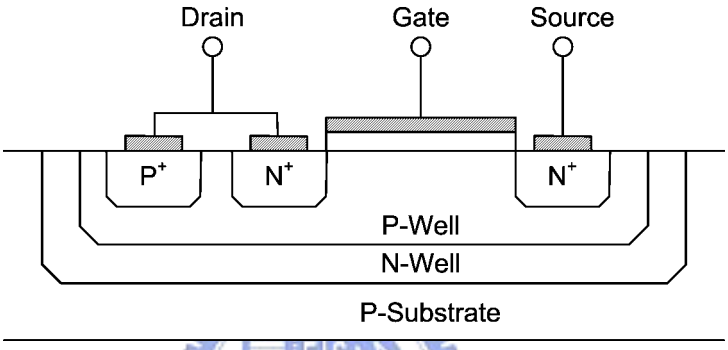


Fig. 2.10 Schematic cross section of the NMOS transfer device in triple-well process.

2.4 Improved Charge Pump Circuits based on Circuit Topology

Besides process topologies, several modifications based on circuit topologies were used to enhance the pumping efficiency [6], [29]-[34]. Normally, these circuit topologies employ additional control circuits or multiple timing control scheme of pump clocks to reduce the V_t loss problem without making alterations in process.

2.4.1 Floating-Well Technique

Fig. 2.11 shows the floating-well technique using PMOS diodes as charge transfer devices [6]. The floating-well technique can be utilized to eliminate the body effect issue on diode-connected PMOS transistors in the Dickson charge pump circuit.

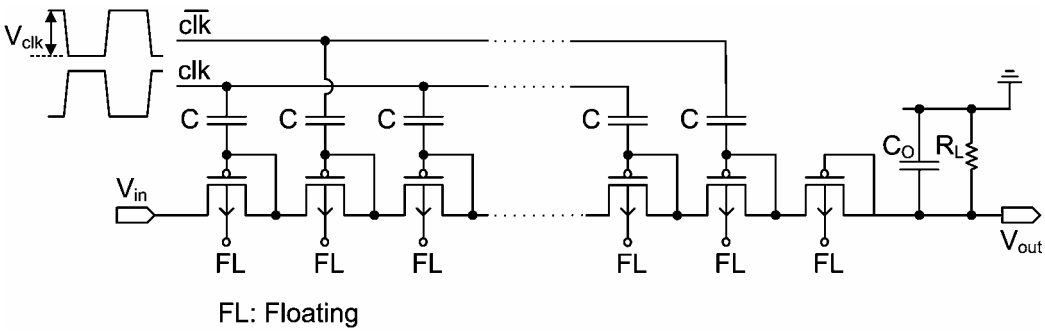


Fig. 2.11 Floating-well charge pump circuit using PMOS diodes as charge transfer devices.

For proper operations with floating-well condition, PMOS transistors are used with their body (n-well) floating as shown in Fig. 2.12(a), and Fig. 2.12(b) shows the internal signals. During the first phase (clk is high and $\overline{\text{clk}}$ is low), V_n is high and the transistor M_n is off. Meanwhile, V_{n+1} is at its low level and the transistor M_{n+1} is turned on for transferring charges from C_n to C_{n+1}. The n-well potential of M_{n+1} denoted to $V_{w,n+1}$ is initially set to

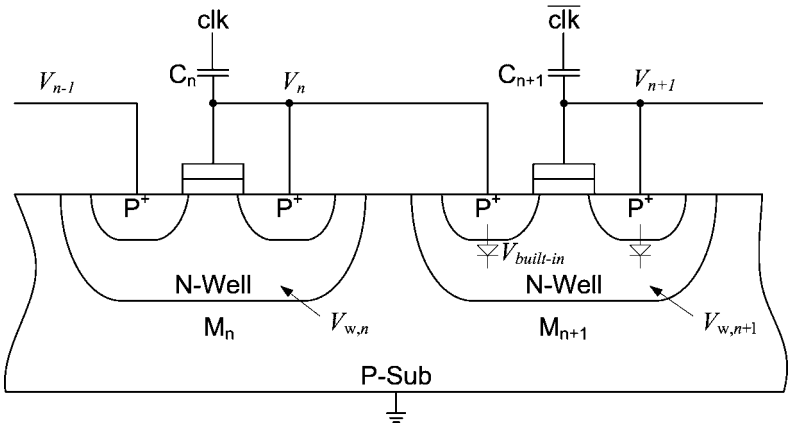
$$V_{W,n+1} = V_n - V_{built\text{-}in} \tag{2.14}$$

where $V_{built\text{-}in}$ is the built-in potential of p^+ to n-well diode and V_n can be considered as the source voltage of M_{n+1}. From (2.14), V_{sb} of M_{n+1} is given as

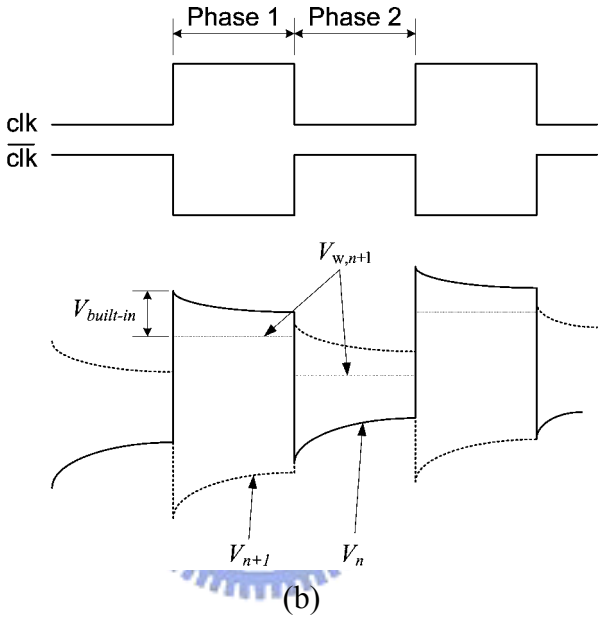
$$V_{sb} = V_n - V_{w,n+1} = V_{built\text{-}in} \tag{2.15}$$

Thus, the threshold voltage could be fixed due to a constant V_{sb} in the conducting PMOS diode.

In addition, at the beginning of charge transfer, V_{sb} of M_{n+1} is equal to $V_{built\text{-}in}$ (> 0 V), which means the effective threshold voltage (V_{tp}) of the PMOS transistor is even slightly lower than the body-effect free threshold voltage (V_{TP0}). Thus, the V_t augmentation problem can be reduced, and the output voltage would be higher than that of the conventional Dickson CPC. Furthermore, the same floating-well concept also can be utilized for NMOS transistors, but it requires the triple-well process to fabricate NMOS diodes in a separated pocket p-well.



(a)



(b)

Fig. 2.12 (a) Vertical structure and (b) internal signals of the floating-well charge pumps.

Utilizing floating-well technique in charge pump circuits exhibits the output characteristic similar to that of a charge pump circuit with an ideal diode chain. The pumping efficiency would be increased rather than the traditional CPC with MOS diode configuration limited by the V_t augmentation problem. In addition, the floating-well charge pump circuit can generate enough voltages even at a supply voltage less than 2.0 V. However, the voltage pumping gain per stage is still reduced by the threshold voltage.

2.4.2 Adaptive Body Technique

The adaptive body technique mitigates the limitation of the varying threshold voltage encountered in the basic Dickson design. The main idea is to control the body of the MOSFET as an active terminal to avoid the problem associated with the threshold voltage increase in charge transfer MOSFETs [32]. By adjusting the body voltage, V_{sb} and V_{th} of the transistor used as a switch in each pump stage are kept constant. With no threshold voltage increase, a higher output voltage can be obtained.

Fig. 2.13 shows the charge transfer block (CTB) with two auxiliary MOSFETs to dynamically bias the body terminal of the diode-connected MOSFET through the schematic and the cross-section view. For each charge transfer block, two auxiliary MOSFETs and one charge transfer MOSFET share the body separated from the body of other blocks.

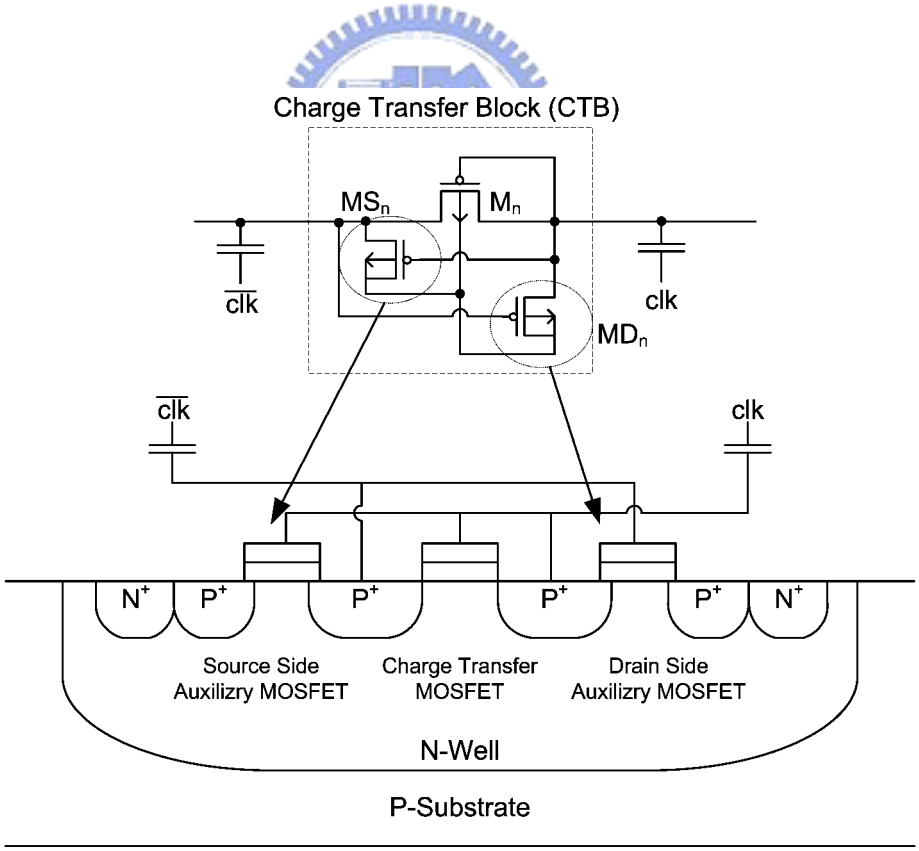


Fig. 2.13 Schematics and cross-section of a charge transfer block.

A multi-stage charge pump circuit using the adaptive body connected technique is shown in Fig. 2.14. The body voltage of the *n*-th charge-transfer MOSFET M_n is set by the source-side auxiliary transistor MS_n and the drain-side auxiliary transistor MD_n in the *n*-th charge transfer block. When clk is low and $\overline{clk}$ is high, M_n is ON and MS_n turns on. Then, the source and the body of M_n are connected through MS_n, so that the body potential is approximately equal to the potential of the source of M_n. In this way, since no reverse bias exists between the source and the body of the charge-transfer MOSFET, the threshold voltage of M_n stays with V_{TP0} (threshold voltage for V_{sb} = 0 V) during the charge transfer state preventing the V_t augmentation problem. In the same clock state, M_{n-1} is OFF and MD_{n-1} turns on so that the drain and the body of the (*n*-1)th charge transfer MOSFET are connected to prevent the body from floating. When clk is high and $\overline{clk}$ is low, the pump operates in opposite manners as that of the previous state.

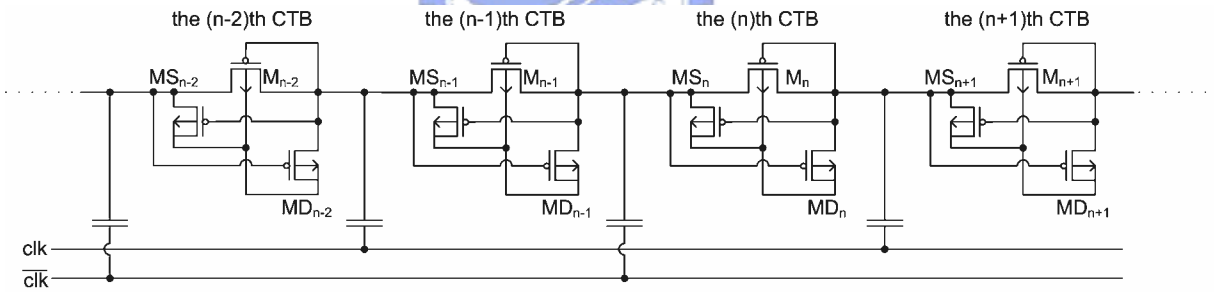


Fig. 2.14 A multi-stage charge pump circuit using the adaptive body connected technique.

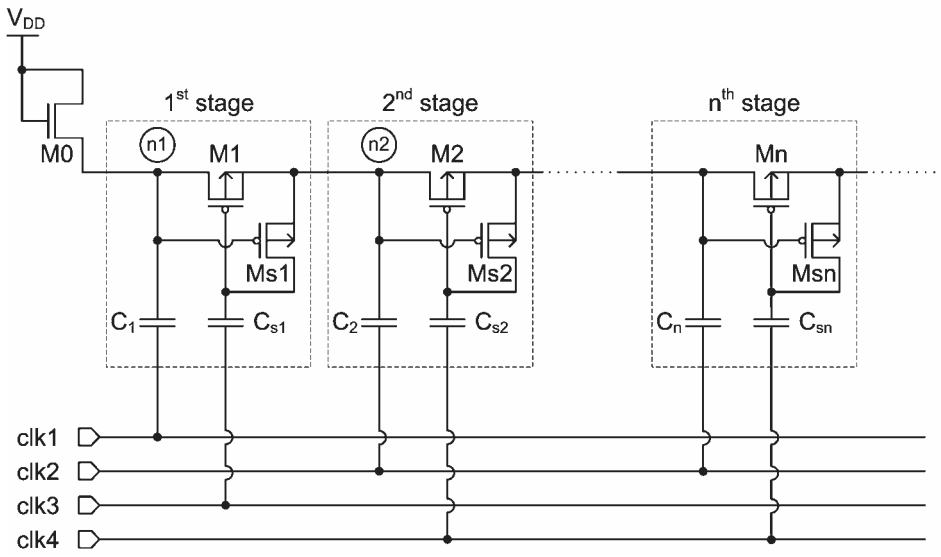
Based on this technique, the body voltage of the charge-transfer MOSFET keeps track of higher value of the source or the drain voltage at each clock state by auxiliary MOSFETs. Since the source-body voltage in each CTB stage no longer increases, the threshold voltage will remain relatively constant throughout the chain. Therefore, the problem of increasing threshold voltages can be minimized, and the charge pump equation becomes identical to that of an ideal-diode Dickson CPC as (2.4).

However, this adaptive body connected technique increases the parasitic capacitance at

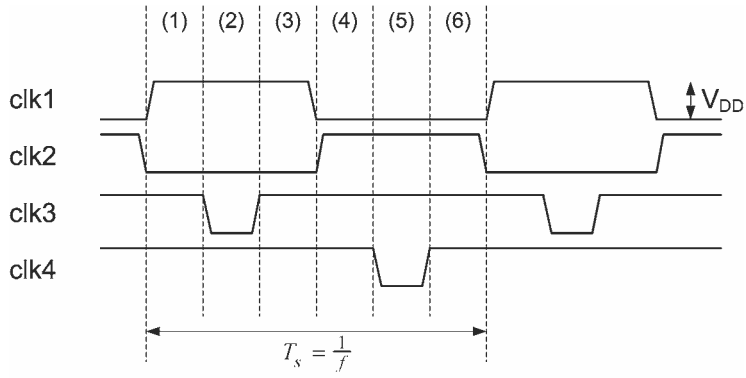
each pumping node due to a large bulk-to-well pn-junction capacitance, so pump capacitances have to be enlarged. The auxiliary MOSFETs used to dynamically control the body terminal of the diode-connected MOSFET may also generate the substrate current in the floating-well device.

2.4.3 Four-Phase Technique

The four-phase charge pump circuit is the favorable style in the electronics market. Using special four-phase clocks, the gain degradation due to threshold voltage can be alleviated [1], [30], [31], [39]. Fig. 2.15 shows the schematic and the clock timing diagram of an example of the four-phase charge pump circuit. C_1 and C_2 are pump capacitors, and M1 and M2 are charge transfer transistors with their gates driven by clocks through C_{s1} and C_{s2}. Ms1 and Ms2 are transistors used to precharge the gates of M1 and M2, respectively. Instead of NMOS transistors in the conventional charge pump circuit, PMOS transistors are adopted for all of charge transfer transistors and precharging transistors. In addition, a individual n-well of PMOS transistor is employed in each unit stage for isolation.



(a)



(b)

Fig. 2.15 The four-phase charge pump circuit. (a) Circuit structure. (b) Clock timing diagram.

The operation of this four-phase charge pump circuit in steady state is explained according to Fig. 2.16 as follows:

1. In Fig. 2.16-A and the phase (6) in Fig. 2.15(b), before clkl is activated, node n1 is precharged to $V_{DD} - V_{tn}$, where V_{tn} is the threshold voltage of NMOS diode M0. At this moment, clk2 is high and the voltage of node 2 can be pumped to $3V_{DD} - V_{tn} - \Delta V_L$ where ΔV_L is the voltage drop due to the output load. As a result of this bias condition, M1 is OFF since Ms1 turns on to connect the gate of M1 and the output node n2.
2. In Fig. 2.16-B and the phase (1) in Fig. 2.15(b), after clk2 falls and clk1 goes high, node n2 and the gate of M1 falls down to $2V_{DD} - V_{tn} - \Delta V_L$, and node n1 is pulled up to $2V_{DD} - V_{tn}$ through C_1. In this transition, Ms1 is shut off, which makes the gate of M1 as a high-impedance node.
3. In Fig. 2.16-C and the phase (2) in Fig. 2.15(b), the subsequent transition in clk3 decreases the gate voltage of M1. Assuming that the potential of clk3 and the gate of M1 are low enough to conduct M1 completely, the voltage of node n2 can be charged up to $2V_{DD} - V_{tn}$ without the voltage drop of the transfer device.
4. The operation of M1 during the phase (6)-(1)-(2) in Fig. 2.15(b) shows analogy to the operation of M2 during the phase (3)-(4)-(5) in Fig. 2.15(b).

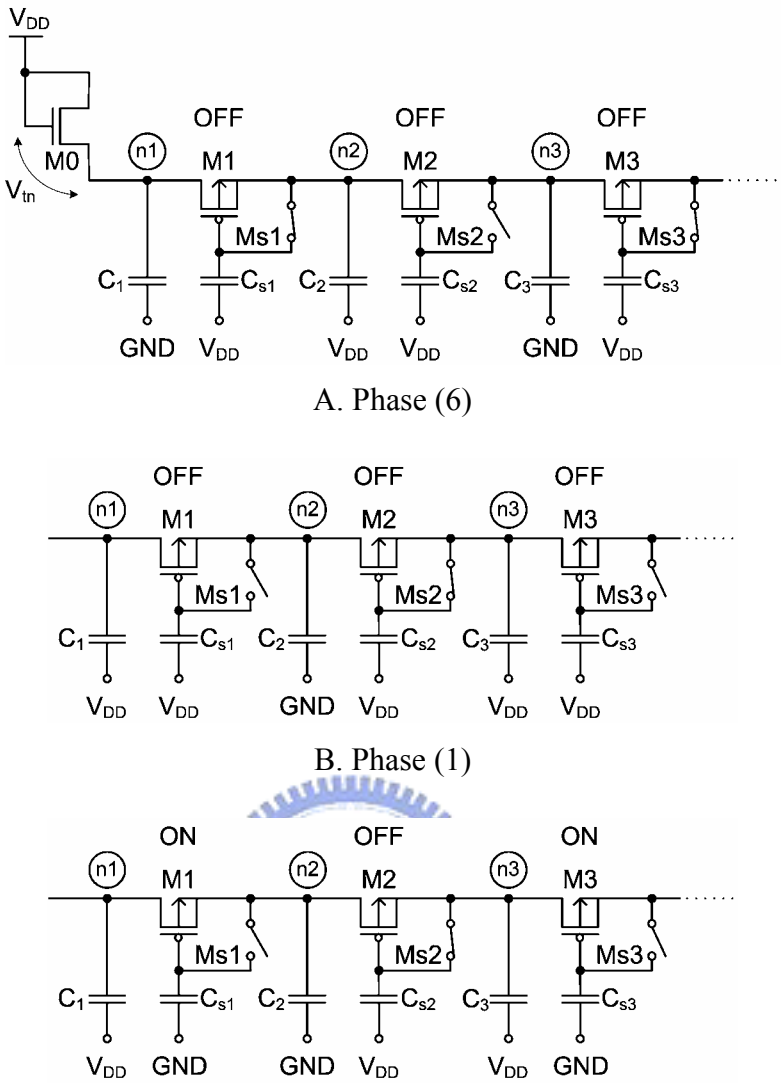


Fig. 2.16 Operation of the four-phase charge pump circuit.

To further eliminate the threshold voltage drop, the gate control voltage of the charge transfer transistor may be decreased below 0 V by bootstrapped clock generators. In addition, the bootstrapped circuit can efficiently enhance the output pull-down speed. Based on this four-phase clock cycle with low enough levels of clk3 and clk4, the voltage drop across each stage can be eliminated and the maximum pump voltage in each stage of this circuit is V_{DD}.

Although four-phase clock generators are often applied in charge pump circuits to improve pumping efficiency, more complicated timing control schemes must be used and the complex clock generator would consume more power.

2.4.4 Gate Bias Technique

Extra gate biasing circuits are used to dynamically control the main charge pump circuit, so that the pumping efficiency of the main charge pump circuit can be enhanced. The new charge pump (NCP2) design [33], shown in Fig. 2.17, utilizes the pass transistors MNx and MPx to dynamically control the charge transfer switch (CTS). The boosted gate control voltage of each CTS is assigned from the succeeding stage to backward control the charge transfer switch, so that the transfer device can be turned on completely as an ideal switch without suffering the limitation of threshold voltage.

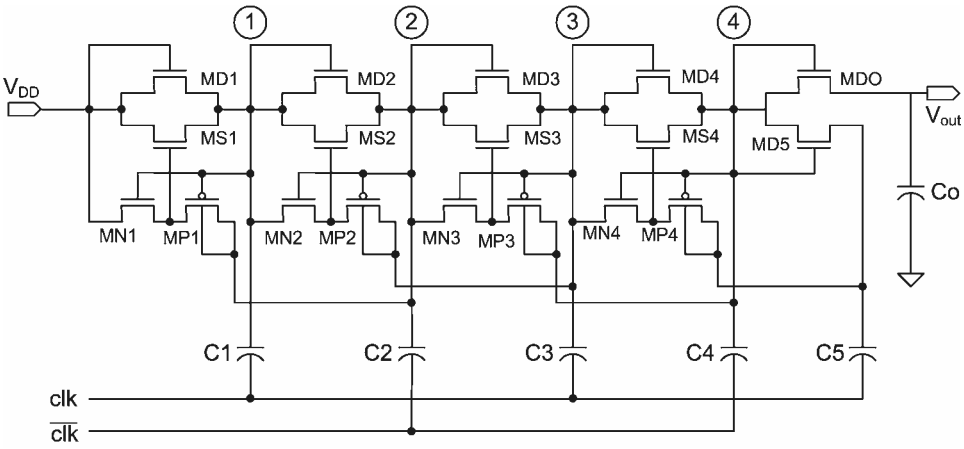


Fig. 2.17 NCP2 circuit.

In Fig. 2.17, when clk is low and $\overline{\text{clk}}$ is high, the pass transistor MN1 is OFF and MP1 is ON, so it can be considered that the gate of MS1 and the node 2 are connected. Since $\overline{\text{clk}}$ is high, the voltage of node 2 is pumped to high level ($3V_{DD}$). Therefore, by this high voltage of node 2 from succeeding stage, the charge transfer switch MS1 would be completely turned on to transfer charges from the power supply V_{DD} to C_1. When clk is high and $\overline{\text{clk}}$ is low, the voltage on node 1 can be pumped as high as $2V_{DD}$ to turn on MN1 and to turn off MP1. Thus, the gate voltage of MS1 would be at its low level as the supply voltage, and MS1 can be completely turned off to prevent charges back to the power supply.

The operation of the other CTS's is similar to that of MS1 mentioned above. Because the CTS's can be completely turned on or turned off by the dynamic control circuit, the voltage pumping gain has been further improved. However, V_{tn} still unavoidably grows along with the increasing body effect resulted from increasing pumping voltage presenting at each terminal of CTS. Until the switch control voltage can't be greater than the increased V_{tn}, the boosted output voltage will arrive at the saturation level. Especially, NCP2 uses diode-connected transistor MDO as the output stage to prevent the reverse leakage current from the output load. Since the largest V_{tn} occurs at MDO, there will be a large voltage drop in the output stage.

Another example of gate biasing technique is shown in Fig. 2.18. The bottom part under the dash line is the main pumping circuit, and the body control transistors (MB1 to MB5) of this main pump circuit are connected on the substrates of major charge transfer switches (MS1 to MS5). MBx are turned on or off simultaneously with MSx, so that the voltage V_{sb} is approximately zero in each charge transfer switch and the body effect can be eliminated.

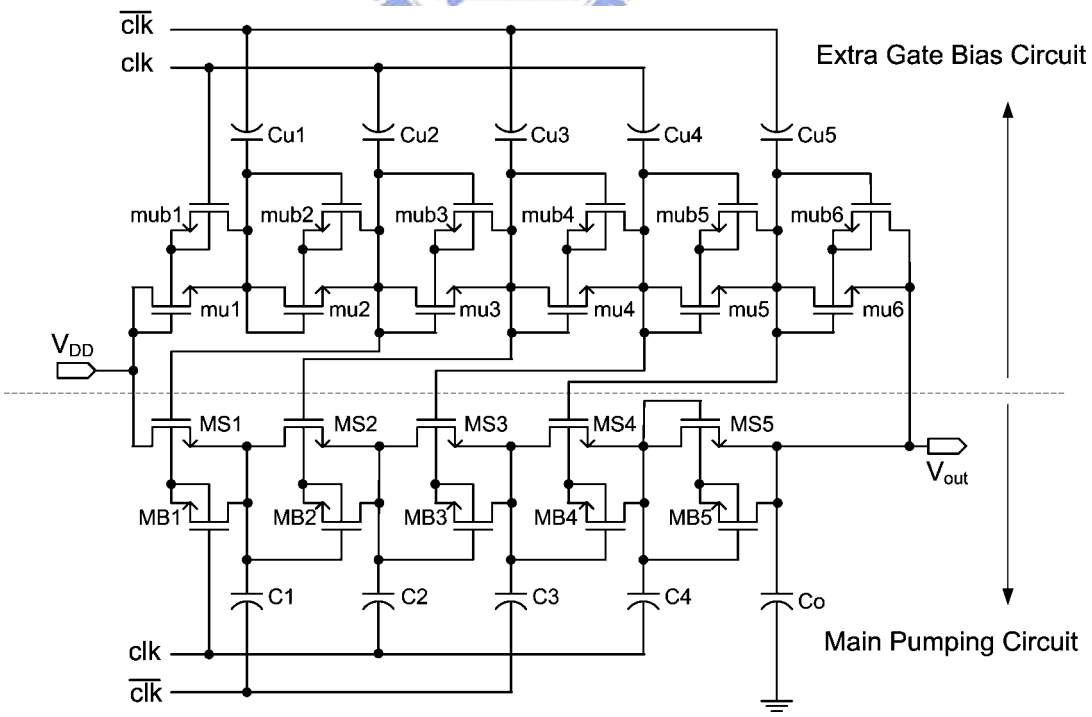
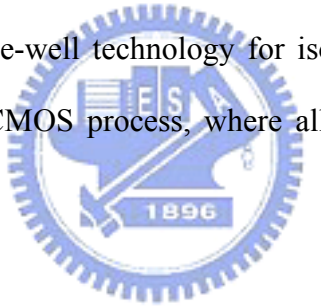


Fig. 2.18 Charge pump circuit with extra gate bias circuits.

The part above the dash line is the extra gate bias circuit pumped simultaneously with the main circuit. The extra gate bias circuit has more pumping stage number than the main charge pump circuit and provides boosted gate control voltage of the charge transfer switch (MS1 to MS5). Assuming that the boosted gate control voltage is pumped higher than the increased threshold voltage, the major charge transfer switch would turn on completely without the threshold voltage limitation. Especially, the voltage drop across the output stage can also be reduced by this technique. Therefore, the pumping efficiency can be improved.

Although the pumping efficiency of this circuit is better than that of NCP2 design, this structure may lead to a problem of reverse charge sharing when a large output current is applied. In addition, this technique consumes extra power and occupies larger silicon area than others because of complex extra biasing circuits. The manufacture of floating body of NMOS transistor requires triple-well technology for isolation, but triple-well technology is not included in the standard CMOS process, where all NMOS transistors have a common body.



2.5 Summary

The Dickson charge pump circuit and several modifications, widely used in memories and switched-capacitor systems, have been presented and discussed in this chapter. From the topologies of different processes, several isolated transfer devices can be obtained with no risk of charge injection into the substrate since the parasitic junction can be eliminated by isolations. Thus, pump circuits can achieve better pump efficiency easily. However, the build-in voltage of the diode still results in the voltage drop in each pump stage, and the V_t augmentation problem still exists while using diode connected transistors as transfer devices. Moreover, some of these topologies adopt atypical CMOS processes which increase the layout and process complexity and require extra cost on fabrication.

The primary advantage of using circuit topologies to solve the V_t augmentation problem is that the pump design can be fabricated in the standard CMOS process. Through some control scheme such as gate bias circuits, body control circuits, and multi-phase control methods, the voltage pumping gain has been further improved. However, these complex circuits would result in complicated layout, occupy larger silicon area, and consume extra power.

Chapter 3

High Efficiency MOS Charge Pumps Based on Exponential-Gain Structure with Pumping Gain Increase Circuits

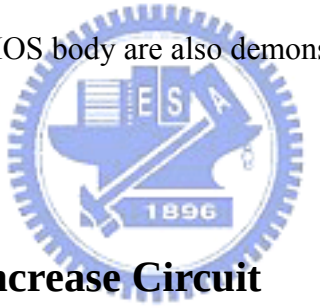
3.1 Introduction

In the previous chapter, the charge pump circuit realized with transistors in the diode-connected style was reported by Dickson. Due to the body effect, the pump efficiency of the Dickson charge pump circuit is degraded as the stage number increases. Several approaches for improving the pumping efficiency have focused on solving this threshold voltage augmentation problem.

Generally, charge pump circuits based on Dickson structure are linear growing pump circuits, so they need many pumping stages to generate a high output voltage. As long as the voltage drop across each stage does not be removed completely especially at the output stage, the voltage gain cannot be maintained to keep the output voltage being proportional to the pump stage number and the pumping efficiency would decrease as the pump stage number increases. Thus, more pumping stages have to be used to obtain the required high output voltage.

This study presents a series of new charge pump circuits that offer high pumping gain in the inner stage and a very low voltage drop at the output stage. In practice, the output voltage of

the proposed pump circuits is almost perfectly proportional to the pumping stage number. In Section 3.2, the configuration and operating principle of the proposed circuits denoted by pumping gain increase (PGI) circuits will be described, and the performance improvement is verified by both simulation and measurement results. In Section 3.3, the exponential-gain architecture for reducing the stage number and simplifying the complexity of the circuit is proposed. With i cascaded voltage multipliers, each supporting a gain of n, the pumping output voltage can be increased by a factor of n^i by using the exponential-gain pump structure. Therefore, this new idea can even operate with a lower supply voltage and also offers a better voltage gain and a higher output voltage. The output voltage can reach over 10 V easily while the regular supply voltage is 1.5 V, so the topology can operate with only one battery supply. Measurements taken from test chips that were fabricated using a standard 0.35-μm CMOS technology with a common NMOS body are also demonstrated in the article.



3.2 Pumping Gain Increase Circuit

Charge pump circuits always suffer from increased drain-source voltage drop (V_{ds}) across every charge transfer MOS switch where V_{ds} is affected by the augmented threshold voltage. The pumping efficiency becomes worse as the stage number of CPC increases. The pumping gain increase circuits detailed in this section are being proposed to increase the total pumping efficiency by solving the voltage drop problems in the inner charge transfer switches (CTS's) and the isolated switch of the output stage.

3.2.1 PGI-1 Circuit

The pumping gain increase circuit develops from the NCP2 circuit which utilizes dynamic CTS's to assign the gate control input of each transfer switch to the higher voltage level provided by the next pump stage. However, with the increasing pump voltage at the source terminal of each charge transfer switch, the threshold voltage V_t still unavoidably grows along with the increased source-body voltage (V_{sb}). In the last CTS, there is no succeeding stage to generate any higher voltage level. When the pump stage number increases to a value such that the gate control voltage (V_{gs}) of the last CTS cannot exceed the increased V_t, the limited gate control voltage would cause undesired operations in last few stages and the pumping output voltage will arrive at the saturation level. Although CTS's in inner stages have high transfer efficiency, but ones in last few stages would have low transfer efficiency. In addition, NCP2 uses an NMOS-diode in the output stage to prevent reverse charge injection from the output node, so that a large voltage will be dropped across the diode due to the augmented threshold voltage problem.

Instead of using the diode-configured MOS switch at the output stage in NCP2, a pumping gain increase circuit denoted by PGI-1 is proposed. Fig. 3.1 shows a charge pump circuit built by a three-stage NCP2 circuit with a PGI-1 circuit at the back. The objective is to increase the voltage level of the switch control signal in the last pump stage and to eliminate the voltage drop across the output stage. The main idea is similar to the circuit shown in Fig. 2.18 introducing the extra gate bias circuit to the main charge pumps. In PGI-1 circuit, only a small auxiliary CTS is added to provide a high voltage level, which is larger than the increased threshold voltage, to drive the last CTS and the output switch, so that all pump stages including of the output one would have perfect pumping performance.

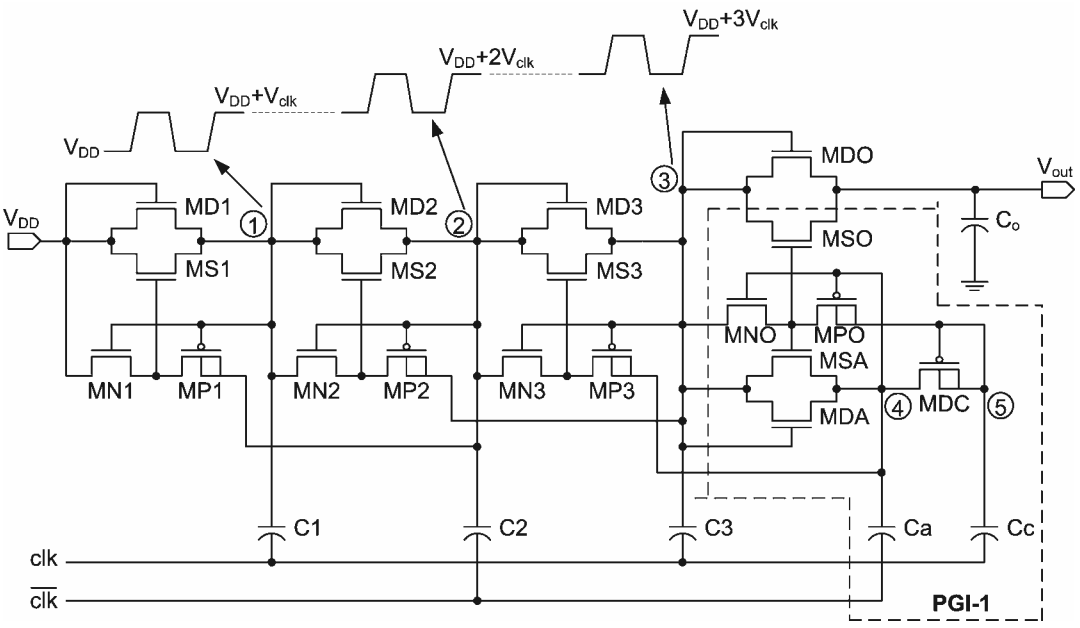


Fig. 3.1 A three-stage NCP2 using PGI-1 as its output stage.

The operation of the PGI-1 circuit is explained as follows. In Fig. 3.1, clk and $\overline{\text{clk}}$ are out-of-phase and have the same voltage amplitude V_{clk}. The MOS diode (MDx) is used to establish initial voltages. When clk is low and $\overline{\text{clk}}$ is high, the voltage V_2 and V_4 of nodes 2 and 4 are raised to higher potential levels. In the ideal case, the gate-source voltage of MP1 and MP3 can be obtained as

$$\left|V_{\text{gs,MP1}}\right| = \left|V_{\text{gs,MP3}}\right| = 2V_{\text{clk}} \tag{3.1}$$

If $$2V_{\text{clk}} > \left|V_{\text{tp0}}\right| \tag{3.2}$$

where V_{tp0} is the threshold voltage of PMOS transistor for $V_{\text{sb}} = 0$, then MP1 and MP3 would be turned on, causing the gate-source voltage of MS1 and MS3 as

$$V_{\text{gs,MS1}} = V_{\text{gs,MS3}} = 2V_{\text{clk}} \tag{3.3}$$

Assuming that

$$2V_{\text{clk}} > V_{\text{tn,MS3}} > V_{\text{tn,MS1}} \tag{3.4}$$

the switches MS1 and MS3 will be turned on completely by the raising voltage V_2 and V_4, respectively. In this period, MN1 and MN3 are always OFF since the gate-source voltages are

both zero. Thus, the pump capacitors C_1 and C_3 will be charged through MS1 and MS3, causing the voltage V_1 and V_3 of nodes 1 and 3 being pulled up to V_{DD} and (V_{DD}+2V_{clk}), respectively. Simultaneously, C_c is further charged through MDC.

On the other hand, since V_2 and V_4 are raised to higher potential levels, the gate-source voltage of MN2 and MNO can be obtained as

$$V_{gs,MN2} = V_{gs,MNO} = 2V_{clk} \tag{3.5}$$

Assuming that

$$2V_{clk} > V_{tn,MNO} > V_{tn,MN2} \tag{3.6}$$

then MN2 and MNO would be turned on, causing MS2, MSA, and MSO being turned off by the lower voltage V_1 and V_3 to prevent reverse charge injection.

Similarly, when clk is high and $\overline{clk}$ is low, the voltages V_1, V_3 and V_5 are raised to higher potential levels. The high voltage V_3 leads the preceding switch MS2 to be turned on to charge C_2. Simultaneously, MSO and MSA are turned on, since V_4 is low and V_5 is high. Thus, C_a and C_o are charged through MDA/MSA and MDO/MSO, respectively. If the control voltage level of MSO is high enough to overcome the augmented $V_{tn,MSO}$, MSO can be turned on and the pump efficiency of the output stage can be kept as high as that of the forestages.

The choice between an NMOS diode and a PMOS diode for MDC is an important design issue of PGI-1. Although PGI-1 can eliminate the V_{ds} drop in the output stage, the V_{tn} increase still exists and affects the internal charge transfer devices, especially when MDC is an NMOS diode. For the case of an NMOS diode based MDC, the pumping voltage in the circuit can be expressed as follows:

(1) When clk is high and $\overline{clk}$ is low,

$$V_{Ca} \simeq V_{C3} + V_{clk} \tag{3.7}$$

where $C_3 >> C_a$ and V_{Ca} and V_{C3} are the voltages across C_a and C_3, respectively.

(2) When clk is low and $\overline{clk}$ is high,

$$V_{Cc} \simeq \left(V_{Ca} + V_{\text{clk}}\right) - V_{\text{ds,MDC}} \tag{3.8}$$

where $C_a > C_c$ and V_{Cc} are the voltages across C_c.

From (3.7), a complete conduction of MSA is needed to obtain higher V_{Ca} which is established by (V_{C3}+V_{clk}). From (3.8), the corresponding gate control voltage of MS3 and MSA for conduction is provided by (V_{Ca}+V_{clk}) and (V_{Cc}+V_{clk}), respectively, where V_{Cc} is established by [(V_{Ca}+V_{clk}) – $V_{\text{ds,MDC}}$]. To turn on MSO and MSA and to give perfect pumping efficiency in the output stage, $V_{\text{gs,MSO}}$ and $V_{\text{gs,MSA}}$ must be high enough to conquer their threshold voltages. Thus, the lower-bound condition for turning on MSO and MSA must be satisfied:

$$V_{\text{gs,MSO}} \simeq \left(V_{Cc} + V_{\text{clk}}\right) - V_{\text{out}} > V_{\text{tn,MSO}} \tag{3.9-a}$$

$$V_{\text{gs,MSA}} \simeq \left(V_{Cc} + V_{\text{clk}}\right) - V_{Ca} > V_{\text{tn,MSA}} \tag{3.9-b}$$

If no load is applied to the output, V_{Ca} will be the same as V_{out} and the lower bounds of MSO and MSA will have the same value. Substituting (3.8) into (3.9), the lower-bound condition for turning on MSO can be obtained as

$$V_{\text{gs,MSO}} \simeq 2V_{\text{clk}} - V_{\text{ds,MDC}} > V_{\text{tn,MSO}} \tag{3.10}$$

In (3.10), the threshold voltage depends on the body effect and can be obtained by

$$V_{\text{th}} = V_{\text{th0}} + \gamma\left(\sqrt{\left|2\phi_f + V_{sb}\right|} - \sqrt{2\phi_f}\right) \tag{3.11}$$

where V_{th0} is the threshold voltage with $V_{\text{sb}} = 0$. The Fermi level ϕ_f and the parameter γ are constant values if the process characteristics are fixed. From (3.11), it can be seen that the increasing $V_{\text{sb,MSO}}$ results in increasing the value of $V_{\text{tn,MSO}}$. Similarly, if MDC is an NMOS diode, a large $V_{\text{ds,MDC}}$ will occur due to a large $V_{\text{sb,MDC}}$. From (3.10), since the only constant is V_{clk}, the formula of the lower-bound condition for turning on MSO can be changed as

$$2V_{\text{clk}} > V_{\text{tn,MSO}} + V_{\text{ds,MDC}} \tag{3.12}$$

When the sum of augmented $V_{tn,MSO}$ and $V_{ds,MDC}$ is larger than $2V_{clk}$, MSO and MSA will not turn on and V_{out} will start to saturate.

With the aid of (3.11) and (3.12), the approximate value of the output saturation voltage can be graphically determined from Fig. 3.2. Line-1 is the threshold voltage of MSO ($V_{tn,MSO}$) with respect to various V_{out}. In the proposed circuit, all the bodies of NMOS transistors are connected to ground. Since the source of MSO is connected to the output terminal in PGI-1, V_{out} is equivalent to $V_{sb,MSO}$. Thus, $V_{tn,MSO}$ can be obtained by substituting V_{out} to (3.11) and that produces Line-1. When MDC is an NMOS diode, $V_{gs,MSO}$ can be calculated from (3.10) once $V_{ds,MDC}$ is known. However, $V_{ds,MDC}$ should be determined by its subthreshold voltage, which is smaller than $V_{tn,MDC}$. To obtain $V_{ds,MDC}$, SPICE simulation results were used to sketch Line-2. Line-3, which indicates $V_{gs,MSO}$, was obtained by calculating (3.10) with V_{clk} value and Line-2. Thus, the intersection of Line-1 and Line-3 gives the critical value of $V_{gs,MSO} = V_{tn,MSO}$. The intersection at point 1 shows that the saturation point of V_{out} is about 4 V while V_{clk} = 1.5 V. Thus, if more than two pump stages are used in PGI-1 circuit with MDC of NMOS diode and $V_{DD} = V_{clk}$ = 1.5 V, V_{out} will start to saturate around 4 V.

An alternative design employed to solve the saturation problem uses a P-MOSFET, based on an N-well/P-substrate, for the MDC in the modified PGI-1. The body of the PMOS is connected to its output side so that the MDC operates as a forward-biased PN junction diode in the charging periods of C_c. This PMOS diode can be easily implemented with a standard CMOS process. Base on the PMOS-diode MDC, the simulation result shows that the $V_{ds,MDC}$ voltage drop is fixed to a small value about 0.5 V and the PMOS-diode MDC no longer has the augmented V_t problem. Thus, the saturation voltage of V_{out} can be increased further according to (3.10), which denotes that $V_{ds,MDC}$ is about 0.5 V. However, the MSO switch still affects the saturation effect. From the intersection at point 2 in Fig. 3.2, the saturated output voltage has been increased to about 8.8 V where both V_{DD} and V_{clk} are 1.5 V.

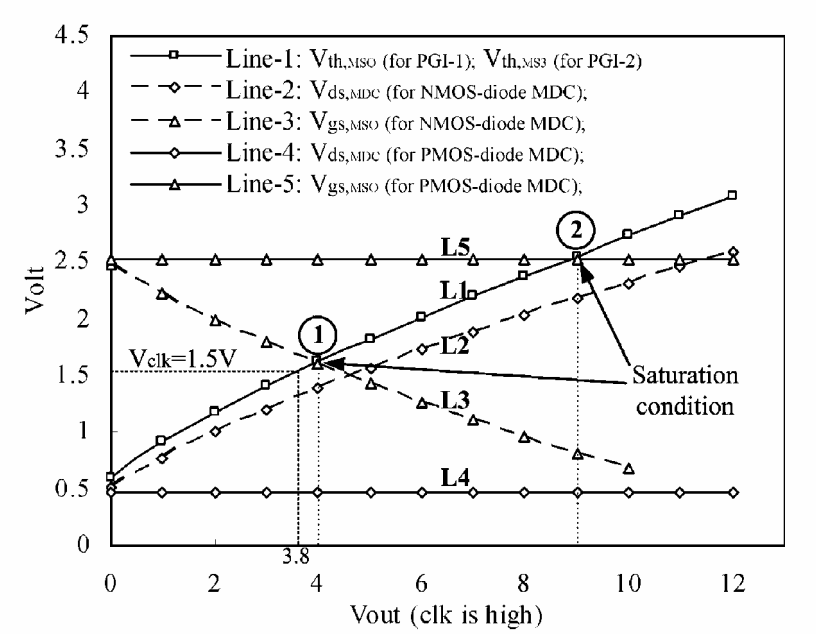


Fig. 3.2 The graphical solution for obtaining the output saturation voltage in PGI-1 circuit, shown in Fig. 3.1, under NMOS-diode MDC and PMOS-diode MDC where V_{DD} and V_{clk} are 1.5 V and all the voltages are taken when clk is high.

3.2.2 PGI-2 Circuit

In the second type of pumping gain increase circuit, PGI-2, the charging switch of the output stage is replaced by a single PMOS switch. Fig. 3.3 shows a three-stage PGI-2 circuit. MSO is a PMOS output switch. The control circuit of the MSO switch is omitted by connecting the gate of MSO to the CTS of the forestage. When clk is high, V_1 is raised to the higher potential ($V_{DD}+3V_{clk}$). This high voltage V_1 leads MN3 to be turned on and MP3 to be turned off. Thus, V_2 is equal to the lower voltage ($V_{DD}+V_{clk}$) and forces MS3 to turn off and MSO to turn on. Since MSO is turned on, no voltage-gain is lost in the output stage. Conversely, when clk is low, MP3 is turned on and MN3 is turned off. This forces MS3 to turn on and MSO to turn off and keeps C_o isolated from its forestage.

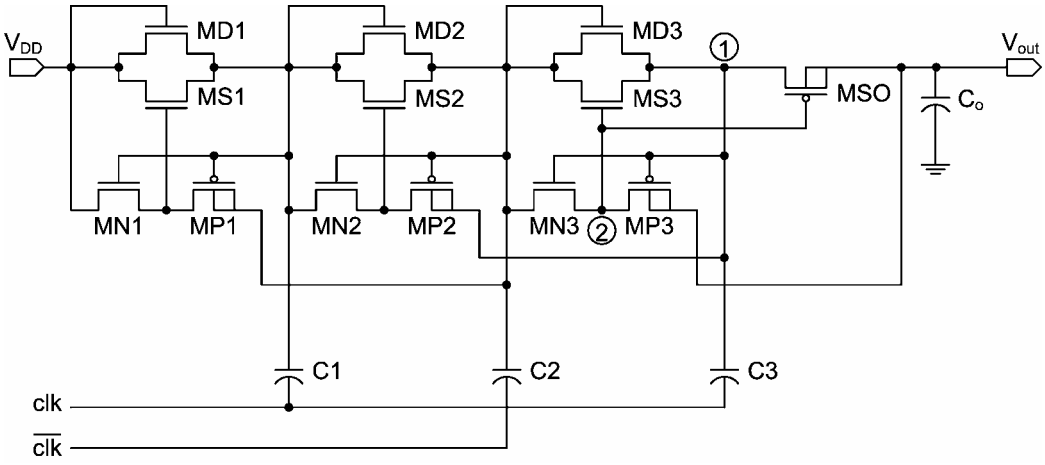


Fig. 3.3 A three-stage PGI-2 circuit.

The PGI-2 circuit solves the output voltage gain loss problem, but output saturation still exists due to the fact that MS3 is affected by the augmented threshold voltage problem. The saturation condition in PGI-2 can be derived as follows:

(1) When clk is high and $\overline{\text{clk}}$ is low, MSO will be turned on by $V_2 = V_{DD}+V_{clk}$ and V_{out} is established as

$$V_{out} \simeq \left(V_{C3} + V_{clk}\right) - V_{ds,MSO} \tag{3.13}$$

where V_{C3} is the voltages across C_3.

(2) When clk is low and $\overline{\text{clk}}$ is high, MS3 will be turned on by $V_2 = V_{out}$ as (3.13) and $V_{gs,MS3}$ is given by

$$V_{gs,MS3} \simeq V_{out} - V_{C3} \tag{3.14}$$

Substituting (3.13) in (3.14) and rewriting $V_{gs,MS3}$ gives the saturation condition as

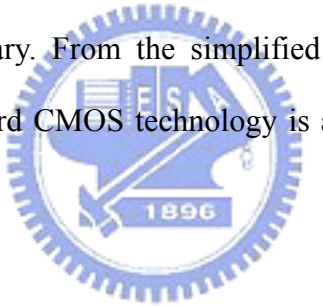
$$V_{gs,MS3} \simeq V_{clk} - V_{ds,MSO} > V_{tn,MS3} \tag{3.15}$$

In above equations, $V_{ds,MSO}$ across the output stage is very small since MSO is turned on during the duration of high clk. Even though $V_{ds,MSO}$ is approximately zero, (3.15) shows that the output saturation will start when the augmented threshold voltage $V_{tn,MS3}$ becomes greater than V_{clk}. This scenario happens in the PGI-2 circuit using multiple stages. Comparing (3.15)

with (3.10), the output saturation level yielded by PGI-2 is smaller than that yielded by PGI-1 due to the $2V_{clk}$ term in (3.10).

Similar to the graphic analysis in PGI-1, Line-1 of Fig. 3.2 also can be used to find the output saturation level of PGI-2. When clk is high and $\overline{clk}$ is low, the source of MS3 is connected to V_{out} through MSO, so that $V_{sb,MS3}$ is equivalent to V_{out}. Thus, Line-1 also expresses $V_{tn,MS3}$ in PGI-2 with respect to various V_{out}. Using the graphic solution previously discussed, the approximate value of the output saturation voltage is 3.8 V in PGI-2, since the augmented $V_{tn,MS3}$ becomes greater than V_{clk}. Thus, if more than two pump stages are used in PGI-2 circuit with $V_{DD} = V_{clk} = 1.5$ V, V_{out} will start to saturate around 3.8 V.

Although the saturation condition of PGI-2 circuit is not as good as that of the PGI-1 circuit, PGI-2 is very simple and the boost circuit for producing the additional control voltage higher than V_{out} is no longer necessary. From the simplified circuit structure and layout, PGI-2 fabricated using normal standard CMOS technology is amenable to compact and lower cost design.



3.2.3 PGI-3 Circuit

In PGI-2, only the output stage is replaced by a single PMOS. In the third type of pumping gain increase circuit, PGI-3, all NMOS CTS's have been replaced by PMOS CTS's. The circuit in PGI-3 is simper than the former two PGI circuits. PGI-3 circuit has a high saturation level and a high pumping gain. The key operation theory associated with this is described as follows.

Fig. 3.4 shows a three-stage PGI-3 circuit. When clk is low and $\overline{clk}$ is high, MN1 and MN3 are turned on causing MS1 and MS3 being turned on. This will result in V_{C1} and V_{C3} being charged to V_{DD} and ($V_{DD} + 2V_{clk}$), respectively. During this time, the gate terminal of the output switch MSO (node 5) is connected to V_{out} through MPO. Thus, MSO is cut off for this duration. Similarly, when clk is high and $\overline{clk}$ is low, MN2 and MNO are turned on causing

MS2 and MSO being turned on. Thus, the voltage V_{C2} and V_{out} would be charged to (V_{DD} + V_{clk}) and (V_{DD} + 3V_{clk}), respectively, through MS2 and MSO.

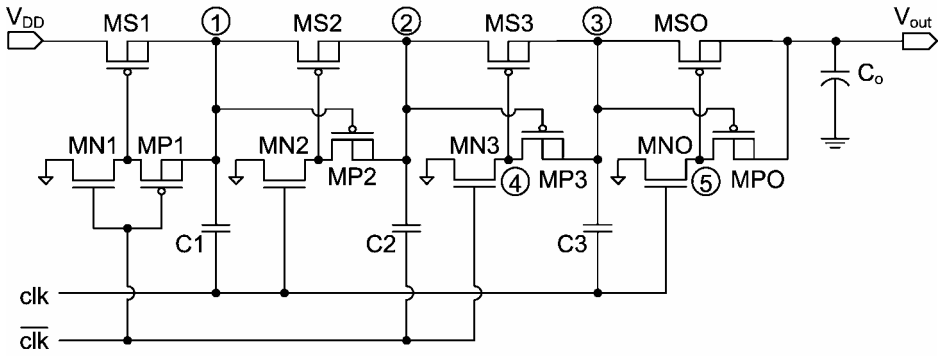


Fig. 3.4 A three-stage PGI-3 circuit.

It is important to mention that the connection of the body of PMOS CTS provides a body diode connection in parallel to a PMOS transistor in saturation mode. Fig. 3.5 shows the vertical structure and internal signals of MS3 as an example to illustrate that the increasing V_t problem has been reduced substantially by PMOS CTS's in PGI-3, where the arrow denotes the direction of the current flow. When clk is low and $\overline{\text{clk}}$ is high, C_3 is charged by two current paths through MS3. Since, the potential energy level of the p-doping source (node 2) is higher than that of the n-well body (node 3), a body diode denoted by path-1 is shown to transfer charges and results in a cut-in voltage ($V_{cut\text{-}in}$) across this junction diode. The other conduction path-2 is the p-channel generated as the gate-source voltage becomes sufficiently negative. PN junction diodes are useful to establish initial voltages while the gate voltages have not been set yet. When all transfer switches can be turned on by appropriate gate voltages, the voltage drop across each stage would be approximately zero.

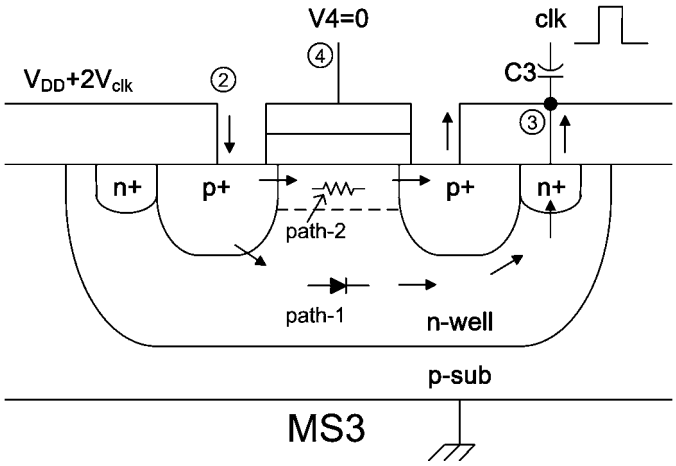


Fig. 3.5 Vertical structure and internal signal flows of PMOS MS3 in PGI-3 circuit as shown in Fig. 3.4.

There are two attractive benefits of this design: the use of body diodes reduces the charging time of pump capacitors and the load capacitor, and the V_{ds} steady-state values of all MSx and MSO are approximately zero, due to the conduction of the PMOS transistors. Since all of $|V_{gd}|$, $|V_{gs}|$, and $|V_{gb}|$ are greater than $|V_{tp}|$, there is no V_t augmentation problem in the PGI-3 circuit. In addition, the boost circuit for producing the additional control voltage higher than V_{out} is no longer necessary.

3.2.4 Simulation and Measurement Results

Before simulation, another important issue is that appropriate W/L ratios of CTS's and charging capacitances must be chosen in order to obtain high pumping gain and voltage transfer efficiency. From the energy conservation, in the steady state situation, the average power transferred out of a pumping stage should be approximate to the average power transferred to the pumping stage, i.e., $\overline{i_o v_o} \approx \overline{i_i v_i}$. Since $v_o > v_i$, it can be expressed that $i_o < i_i$. Therefore, the W/L ratios of each CTS and the charging capacitance of each stage are suggested be arranged as a fashion of proportional decrease from the first stage to the output stage, but that does not guarantee satisfaction to layout area and compact designs. An optimization design method for minimizing the die area of the *N*-stage pumping gain increase

circuit in terms of the total number of pump stages and the ratio of the pump capacitances will be proposed in the next chapter. In addition, it is not strict to determine the W/L ratio of the pass transistors MN's and MP's because they only provide very less power to drive CTS's.

The HSPICE simulation using the high block voltage model for TSMC 0.35 μm mixed signal CMOS technology was performed for verification. The threshold voltage (V_{tn0}) of the NMOS transistor is about 0.72 V and V_{tp0} of the PMOS transistor is about -1.0 V. The operation frequency of pump clock is about 2 MHz and V_{clk} = 1.5 V. The rise time and fall time of the pump clock are set to 1 ns. In the case of 1.5 V supply voltage, the transient simulation results for the output voltage of PGI-1 circuit under different pump stage with a light load are shown in Fig. 3.6. It can be seen that the output voltage is almost perfectly proportional to the pumping stage number. However, V_{out} will start to saturate if more than five pump stages are used in PGI-1 circuit. This is because that while V_{tn} of the NMOS charge transfer switch at the last stage increases over ($2\,V_{clk} - V_{ds,MDC}$), the PGI-1 circuit unable to conquer the body effect and a large voltage drop will be produced. To review the graphical solution form the intersection at point 2 in Fig. 3.2, the saturated output voltage of the PGI-1 circuit with a PMOS-diode MDC under the condition of $V_{DD} = V_{clk}$ = 1.5 V is predicted lower than 8.8 V. Thus, the results obtained from Fig. 3.6 agree approximately with those expected.

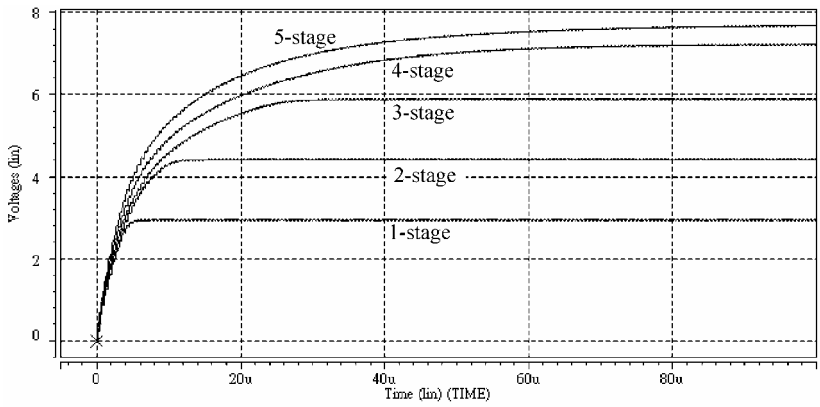
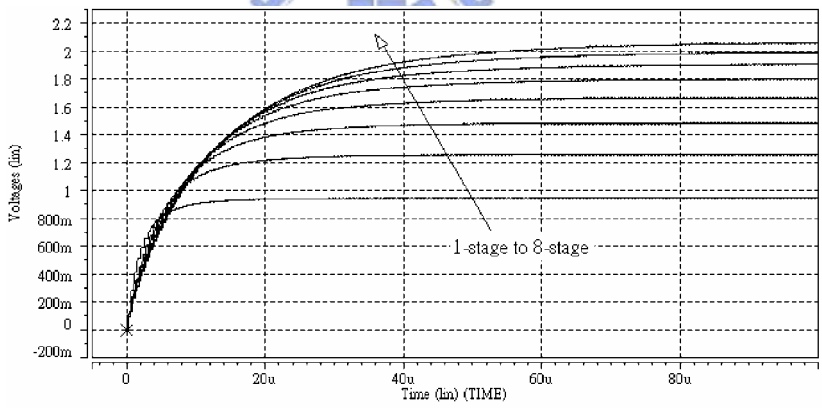
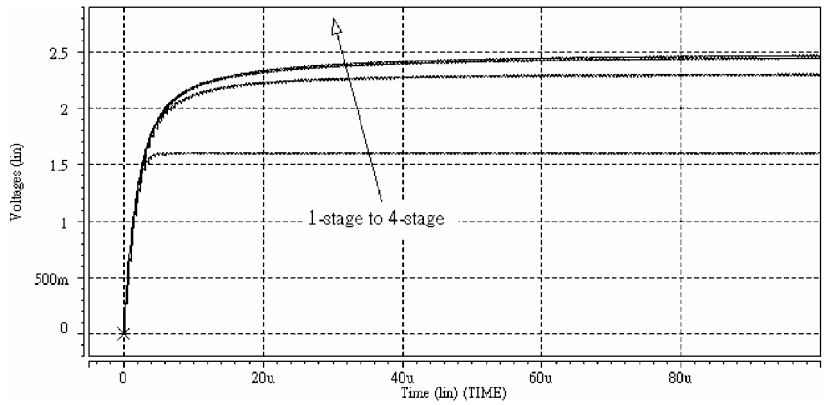


Fig. 3.6 The output waveforms of PGI-1 circuit under different pump stage with $V_{DD} = V_{clk}$ = 1.5V, f_{clk} = 2 MHz, and I_{out} = 10 μA.

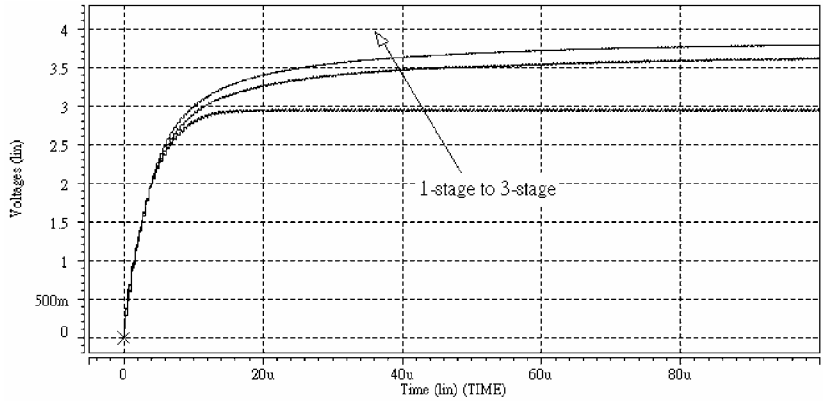
Similar simulation results for the output voltage of various charge pump designs in the light load condition are shown in Fig. 3.7, and all results are summarized in Fig. 3.8. In order to obtain reasonable comparisons from all circuits under test, the charging switches have been designed to have the same channel width and length. From Fig. 3.8, the order from high to low of output saturation voltages is PGI-3, PGI-1, PGI-2, NCP2, and Dickson. The PGI-3 circuit exhibits the best charge pumping performance among these five circuits, and the pumping gain of PGI-3 is very close to the ideal value without a saturation problem. The output voltage of PGI-3 can easily exceed 10 V with a 1.5 V supply when 6 pumping stages are used. In addition, although all four CPC's, except PGI-3, have obvious saturated limitation as the stage number increases more, the output saturation voltage of PGI-1 is about 7.8 V, which is much higher than the other three CPC's.



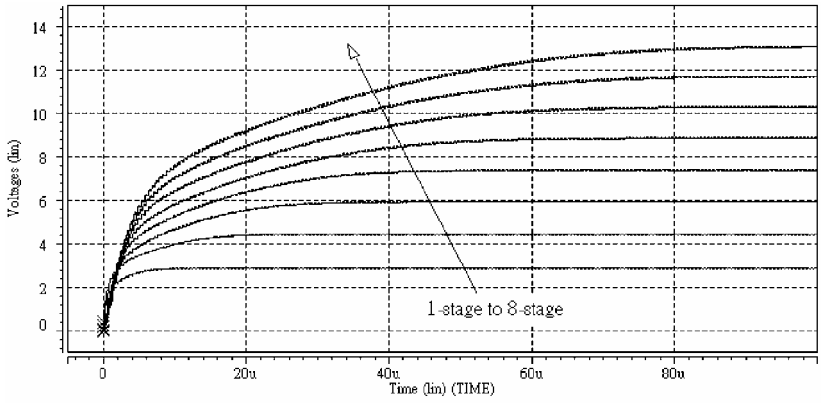
(a) Dickson



(b) NCP2



(c) PGI-2



(d) PGI-3

Fig. 3.7 The output waveforms of various charge pump circuit under different pump stage with $V_{DD} = V_{clk} = 1.5V$, $f_{clk} = 2$ MHz, and $I_{out} = 10$ μA.

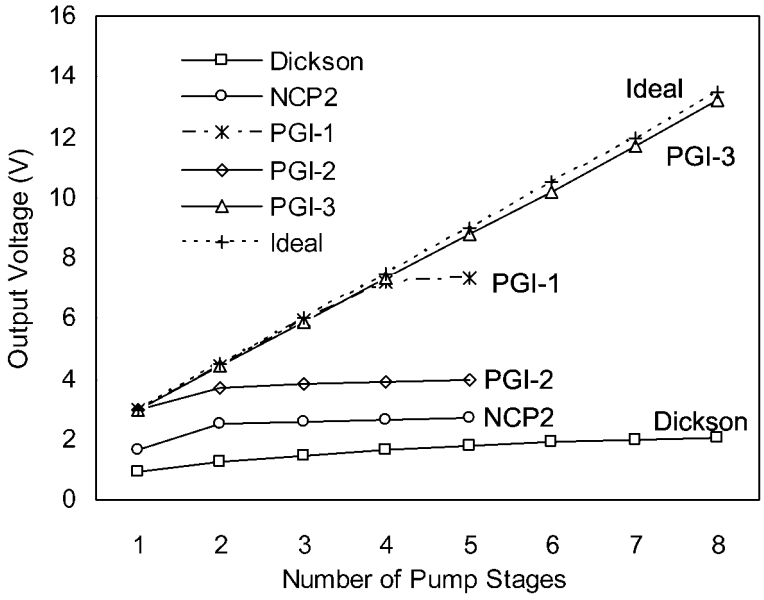


Fig. 3.8 Simulated output voltage versus pump stage number of various CPC's with $V_{DD} = V_{clk} = 1.5V$, $f_{clk} = 2$ MHz, and $I_{out} = 10$ μA.

The load current also has influence on the output voltage. Fig. 3.9 shows the simulation results that compare the output voltages of various charge pump circuits at different supply voltage and output current loading. All PGI circuits have three pumping stages. The load capacitor at the output is 100 pF. The frequency of the pumping clocks is 2 MHz. As shown in Fig. 3.9, the output voltage always decreases as load current increases, and that supports the generalization of (2.7). For the PGI-2 circuit, the pump efficiency is obviously lower than that of the other two circuits, since the limitation of output saturation occurs if more than two pump stages are used. For the three-stage PGI-1 and PGI-3 circuits, the saturation problem does not exist so that the pumping performance of these two cases would be better and approximate to ideal case. In addition, since PGI-3 use PMOS CTS's, the corresponding output voltage losses are greater than that in the PGI-1 circuit, which uses NMOS CTS's, especially in the case of a larger output current.

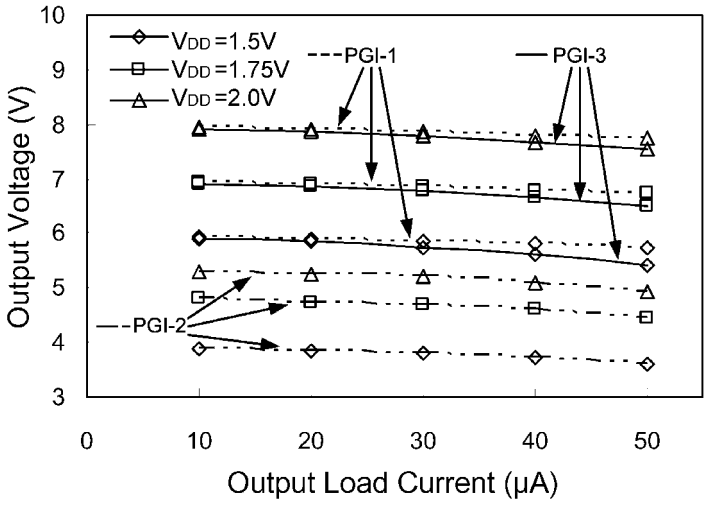


Fig. 3.9 Simulated output voltage versus output load current of various 3-stage PGI circuits under different V_{DD}.

From the same simulated condition in Fig. 3.9 without optimal design, the power efficiency η_p of the charge pump is calculated using the conventional definition of the output power divided by the input power as:

$$\eta_p = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_{\text{out}} V_{\text{out}}}{I_{\text{power}} V_{\text{DD}}} \tag{3.16}$$

and is plotted in Fig. 3.10 versus the output current (I_{out}) for 3-stage PGI-1 and PGI-3 circuits with $V_{\text{DD}} = V_{\text{clk}} = 1.5$ V. It can be obvious that PGI-3 can give the pump circuit a greater efficiency. The performance difference between these two circuits is ascribed to more power consumption from extra boost circuits and additional pump capacitors in PGI-1.

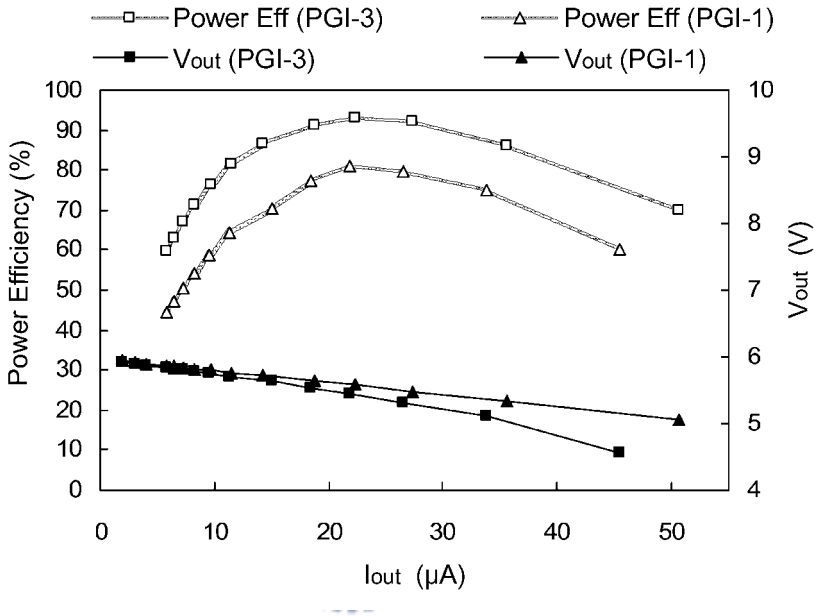


Fig. 3.10 The power efficiency of PGI-1 and PGI-3 circuits versus the output current where $V_{\text{DD}} = V_{\text{clk}} = 1.5$ V.

A three-stage PGI-1 and PGI-3 have been fabricated using a TSMC 0.35-μm mixed mode process. Fig. 3.11 shows a microphotograph of the practical design, and PGI circuits and pump capacitors are in the left region. Fig. 3.12 shows the measurement output voltages at different supply voltage and output current loading. This prototype is primarily designed for 1.5 V supple voltage operation. Although the rated operating voltage of this process is 5 V, it is found from the measured data that no breakdown happens to the devices when the output is below 8 V.

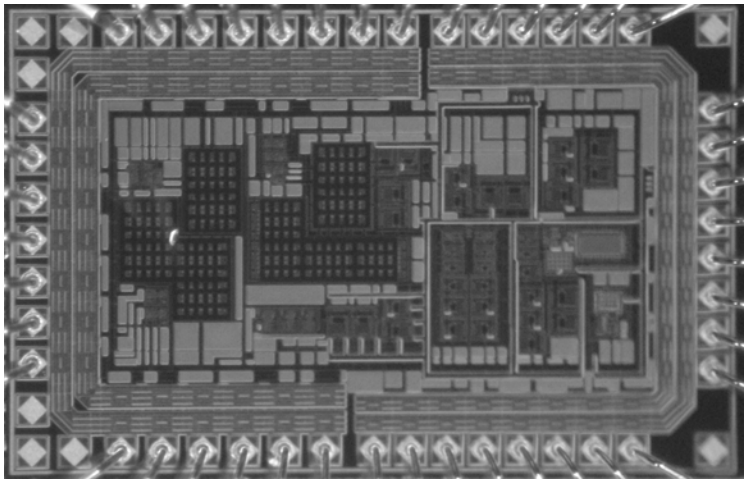


Fig. 3.11 Microphotograph of the PGI circuits.

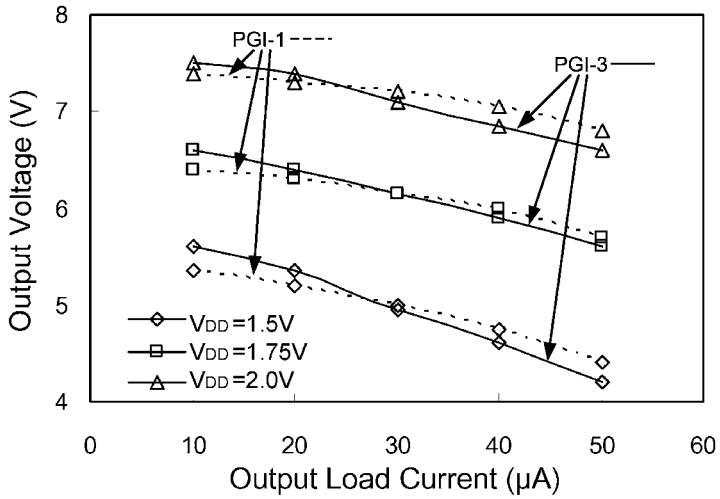


Fig. 3.12 Measured output voltage versus output load current of 3-stage PGI-1 and PGI-3 circuits under different V_{DD}.

Compared with the simulation result shown in Fig. 3.9, the measured output voltage is lower than that predicted by simulation due to additional parasitic capacitors, parasitic resistors, and extra switching losses in the clock generation circuit. For the case of low output current loading, the output voltage of PGI-3 is slightly better than that of PGI-1, as the W/L ratios of PMOS CTS's in PGI-3 are greater than that of NMOS CTS's in PGI-1 in the practical layout. In PGI-3, the output can climb above 7.5 V with a load current of 10 μA and a supply voltage of 2 V. This result is close to a 2V-to-8V ideal case with a 4× pumping gain.

The measurement results for 1.5 V and 1.75 V supply voltages in the condition of light load are also close to the ideal value.

3.3 Exponential-Gain Pump Structure

3.3.1 Architecture

Since most CPC's have a linear growing structure and voltage gain losses, many stages will be needed to obtain high output voltages. Moreover, due to V_t augmentation problem, they will not achieve higher output voltages. Thus, an exponential-gain pump structure is proposed to solve the voltage saturation by making the clock voltage grows exponentially along with the number of stages cascaded. Compared with the linear-gain structure shown in Fig. 3.13(a), the exponential-gain pump structure, shown in Fig. 3.13(b), adopts less stage number to support the same output voltage.

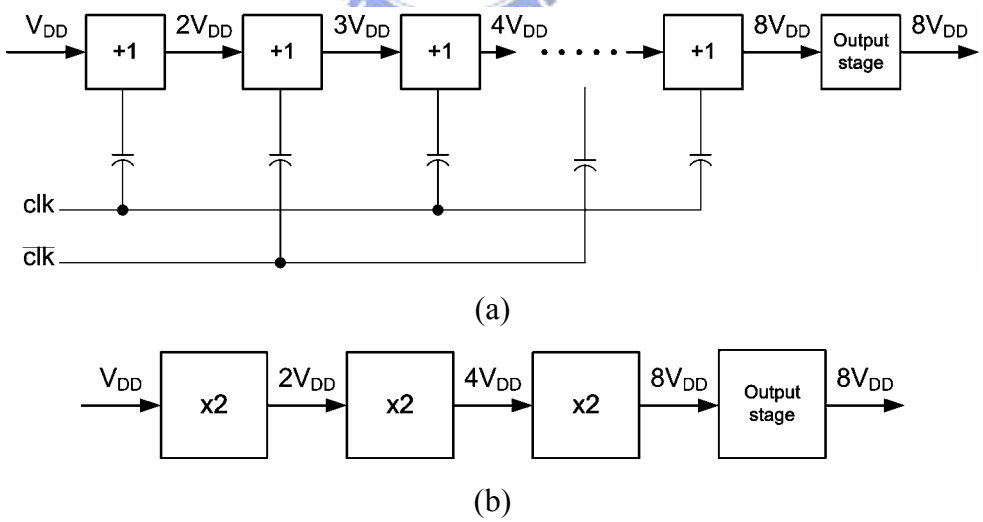


Fig. 3.13 A conceptual block diagram of eight-fold voltage gain by using (a) a linear growing structure in 7-stage case and (b) an exponential-gain pump structure in 3-stage case.

An *n*-times voltage multiplier is the fundamental cell of this structure. The output of this fundamental cell is connected as the power supply to the next one. With *i* cascaded cells, an

exponential-gain pump structure will be formed to provide the total voltage gain of n^i. In Fig. 3.13(b), the system can be considered as a 2^3 exponential-gain pump structure formed by three cascaded voltage doublers. It should be noted that with this structure the output voltage will be confined by the fabrication process. To obtain a high output voltage which exceeds the breakdown voltage of the low voltage chip, the cascaded cells need to be placed in a chip or in discrete chips fabricated by the process which can provide a breakdown voltage higher than the operating voltage.

In Fig. 3.14, an exponential-gain example of a 2×2 charge pump circuit denoted by 2×2 CPC is proposed. The first stage of a 2× PGI-1 circuit, named Cell-1, is used to provide the supply voltage (V_{o1}) of the next 2× PGI-1 circuit. If more cells are cascaded, then the voltage of whole charge pump circuit will grow exponentially. From (3.12), since the growth of clock voltage is always greater than the growth of V_t in this structure, the V_t problem can be suppressed very well.

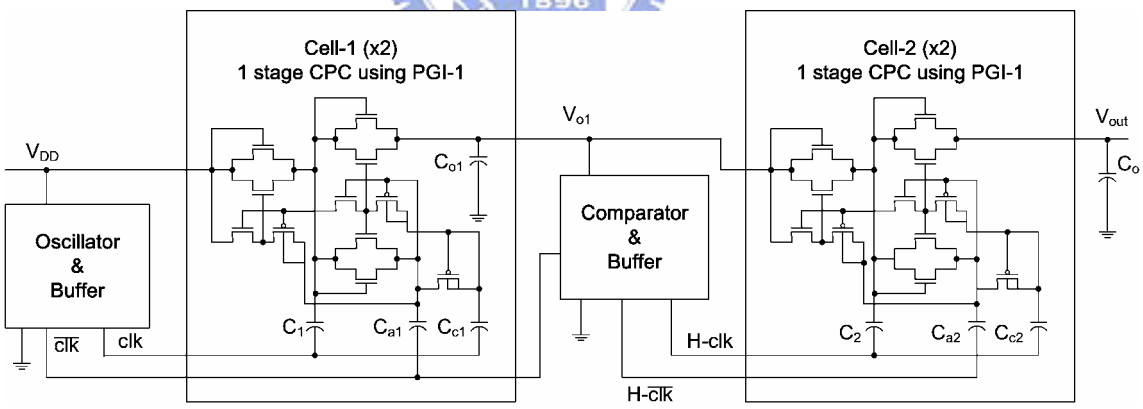


Fig. 3.14 The block diagram of a 2×2 exponential-gain pump structure.

Other 2× cells based on PGI-2 and PGI-3 circuits have also been used to realize a 2×2 CPC. The advantage of this new structure can be viewed in several ways: fewer stages, lower power dissipation from switching, and high flexibility. Since the complexity of the circuit and the pumping stage number in each cell has been reduced, the parasitic effect has also been

reduced and the output saturation problem will not occur, even though PGI-2 or NCP2 are used as the fundamental cell. The number of switches is decreased substantially and the power loss from switching is also reduced. In addition, a higher pumping gain can be obtained more flexibly by appropriately adjusting the number of CPC stages in each cell or the number of cascaded cells. Thus this structure is not only suited for high pumping gain, especially in high output voltage and low supply voltage applications, but also simplifies the whole circuit configuration.

3.3.2 Simulation and Measurement Results

Fig. 3.15 shows the transient simulation results of the three-stage PGI-1, PGI-2, PGI-3, and the proposed exponential-gain 2×2 CPC based on the PGI-1 as the fundamental cell. All of these circuits are designed for a 4× ideal pumping gain in the condition of light load and simulated with the same technology. The geometric size of each design is almost identical in all devices without optimal sizing. The simulation results show that the output voltage of the 2×2 CPC is a little smaller than those of the PGI-1 and PGI-3, and that can be ascribed to the extra power consumption from the internal comparator and buffer of the exponential-gain pump structure.

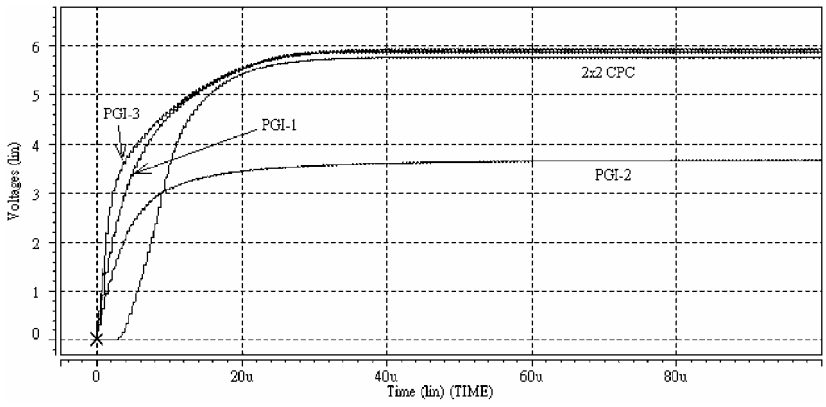


Fig. 3.15 Simulated transient output waveforms of 2×2 CPC and various 3-stage PGI circuits with $V_{in} = V_{clk} = 1.5$ V and $I_{out} = 10$ μA.

The simulated output voltages versus expected gain of PGI-1, PGI-3, and exponential-gain CPC are summarized in Fig.3.16 and Table 3.1. Ideally, an (*N*-1)-stage linear CPC, such as PGI-1 and PGI-3, can generate an output voltage closed to *N*-fold of the supply voltage. In the case of the exponential-gain structure, the output voltage is close to the ideal value without any saturation problem in the present testing range and easily exceeds 10 V when using a 3×3 CPC with a 1.5 V supply. Table 3.1 also shows that the exponential-gain structure has high flexibility to generate a desired output voltage.

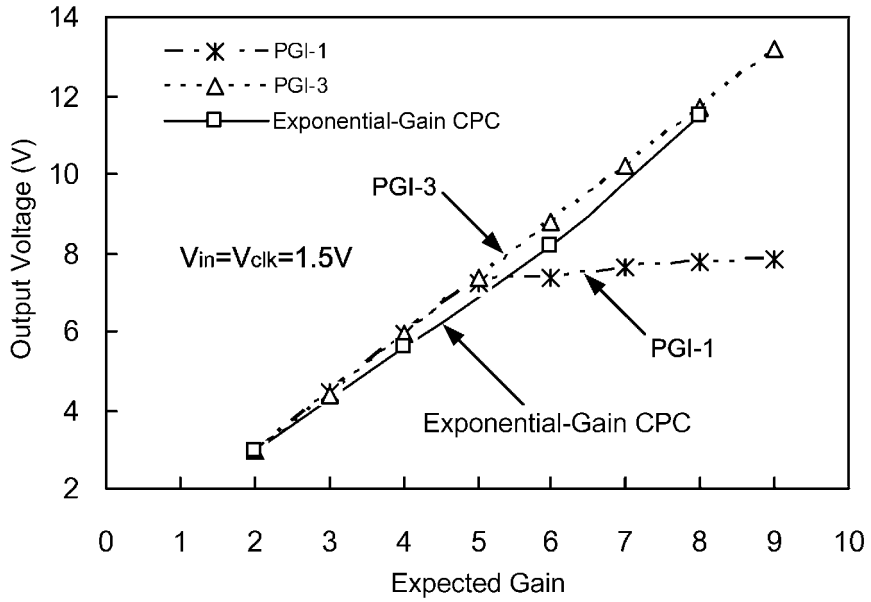


Fig. 3.16 Simulated output voltage versus expected gain of exponential-gain structure, PGI-1, and PGI-3 with $V_{in} = V_{clk} = 1.5$ V and $I_{out} = 10$ μA.

Table 3.1 Comparison of output voltages generated by PGI-1 and exponential-gain structure over several gain configurations.

Ideal Folds V_{in} = 1.5 V (Ideal Output)	**Stage Number of PGI-1** (Output Voltage)	**Exponential-Gain Structure** (Output Voltage)
four-times of V_{in} (6V)	3-stage (V_{out} = 5.93V)	2×2 structure (V_{out} = 5.8 V)
six-times of V_{in} (9V)	5-stage (V_{out} = 7.7 V)	2×3 structure (V_{out} = 8.4 V) 3×2 structure (V_{out} = 8.5V)
nine-times of V_{in} (13.5V)	8-stage (V_{out} = 8.0 V)	3×3 structure (V_{out} = 12.1 V)

A 2×2 CPC using PGI-1, PGI-2, and PGI-3 for the fundamental cell has been fabricated with a standard 0.35-μm CMOS technology. Fig. 3.17 summarizes the measured output voltage versus various supply voltages, 1.3 V to 2.2 V, and a 10 μA output load current. The measured data show that the output voltages of 2×2 CPC's formed by PGI-2 or PGI-3 are lower than those formed by PGI-1. The main reason for this effect is that PGI-2 and PGI-3 use PMOS switches deficient in the driving abilities of charge transfer devices. The measured results also show that the output voltage of the exponential-gain CPC using PGI-1 has a tendency to saturate when the supply voltage exceeds 2 V. This is due to the breakdown voltage limitation of the process having been reached in the PGI-1 circuit of Cell-2.

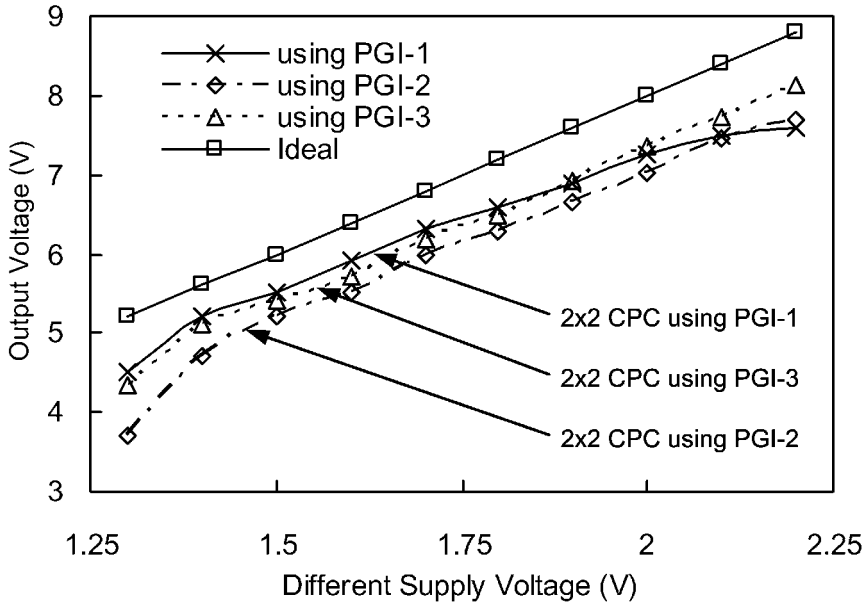


Fig. 3.17 Measured output voltages of 2×2 CPC using PGI-1, PGI-2 and PGI-3 under different supply voltages.

3.4 Summary

The conventional charge pump circuit always suffers from the problem of increased drain-source voltage drop V_{ds} across each charge transfer MOS switch, where V_{ds} is affected by the threshold voltage affected by the body effect. Thus, the output voltage cannot be maintained as a linear function of the number of stages and the pumping efficiency will be degraded as the stage number increases further. Novel MOS charge pumps utilizing an exponential-gain structure and pumping gain increase circuits with high voltage transfer efficiency to generate boosted output voltages have been described to overcome key problems in CPC designs.

First, three different PGI circuits are proposed to reduce the voltage drop across the output stage and inner charge transfer MOS switches. The PGI circuits allow the output voltage to increase linearly as the number of pumping stages increases. However, in PGI-1 and PGI-2, the threshold voltage increase problem still exists and limits the output voltage, as the stage number gets too large. In PGI-3, there is no saturation limit, since $|V_{gs}|$ of each CTS can always be larger than $|V_{tp}|$. Therefore, the output voltage is close to the ideal level and the charge transfer efficiency can be enhanced. The main results of the comparison with these three PGI circuits are provided in Table 3.2.

Table 3.2 Comparison with the three different PGI circuits.

	pumping ability	**saturated limitation**	**internal stage voltage drop**	**output stage voltage drop**	**process problem**
PGI-1	*high*	*yes*	*no*	*no*	*yes*
PGI-2	*moderate*	*yes*	*no*	*no*	*yes*
PGI-3	*high*	*no*	*no*	*no*	*moderate*

The second design is an exponential-gain pump structure that can pump the output voltage exponentially from a low power supply without an output saturation effect. This structure can be applied to produce any pumping gain with its n^i architecture. For example, a 2×2 (2^2) CPC

can be used to generate a boosted output of 6 V with a 1.5 V supply voltage. As shown in simulation and measurement results, the proposed designs are able to generate high voltages efficiently from a power supply below 2 V. A three-stage PGI-3 circuit or a 2×2 CPC can generate a boosted output close to the ideal value of 6 V from a 1.5 V supply.

Thus, it is conceivable that PGI circuits and the exponential-folds structure can be applied to generate high output voltages more effectively from a low voltage source such as using a battery cell.

Chapter 4

Analysis and Modeling of On-Chip Pumping Gain Increase Circuits with a Resistive Load

4.1 Introduction

In recent years, many efforts have been made in the analysis and optimization of the Dickson structure in order to support a convenient and rapid design scheme [23]-[25], [40], [41]. Similarly, in this chapter, a thorough analysis and a complete average model of the pumping gain increase (PGI) circuit, which is a type of improved charge pump circuits, with a resistive load have been presented. Based on this simple analytical model, the characteristics of PGI circuits can be approximately predicted and several handy equations can also be found for planning the desired circuit to achieve good enough performance with an acceptable accuracy tolerance in the steady state.

In section 4.2, a general equivalent model based on PGI circuits is described. Analyses based on the charge balance and average conceptions are presented. By using this simple analytical model, characterization of PGI circuits can be performed in a pencil-and-paper manner and the output behavior can be approximately determined. An optimization design method for minimizing the die area of an *N*-stage PGI circuit in terms of the total number of pump stages and the pump capacitor ratio is also presented. This design strategy can also be

applied to other improved CPC designs that have no voltage drop within the inner stages and the output stage. In section 4.3, simulation results are presented to verify this equivalent model for designing PGI circuits. Presented in Section 4.4, experimental results measured from a test chip that was fabricated with a TSMC 0.35-μm mixed-mode technology demonstrate the validity of the proposed model. Conclusions are given in Section 4.5.

4.2 Equivalent Model for the Voltage Multiplier

PGI circuits, which are shown in chapter 3, provide a method of using NMOS and PMOS charge transfer switches (CTS's) to eliminate the drain-source voltage drop V_{ds} across each pump stage and allow the output voltage to increase linearly as the cascade number of the pump stage increases. It is notable, that in PGI-3, there is no output saturation limitation no matter how many pump stages are used. Ignoring non-ideal characteristics such as switching losses and parasitic capacitances, an analytical equivalent model can be constructed based on the identity of an N-stage PGI circuit.

4.2.1 Behavioral Model of Intermediate Stages

From the characteristic of an N-stage PGI circuit, the equivalent circuit can be simplified as shown in Fig. 4.1, where clk and $\overline{\text{clk}}$ are two anti-phase clocks with the same amplitude V_{clk}, C_m is the pump capacitor of the m-th pump stage, V_m is a time variant voltage across C_m, $V_{o(m)}$ is the voltage at node m connecting to the positive branch of C_m, and S_m is the m-th equivalent ideal transfer switch between C_{m-1} and C_m. Each stage has two operating modes, the charging mode operating with DT_s duration and the discharging mode with $(1-D)T_s$ duration, where D is the duty ratio and T_s is the switching period. The corresponding waveforms of $V_{o(m-1)}$, $V_{o(m)}$, and $V_{o(m+1)}$ are shown in Fig. 4.2.

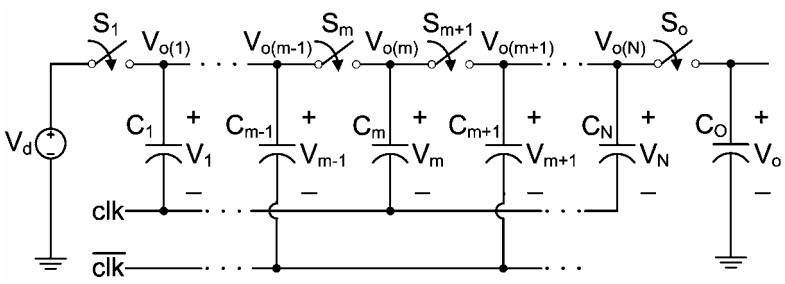


Fig. 4.1 Conceptual diagram of an *N*-stage PGI circuit.

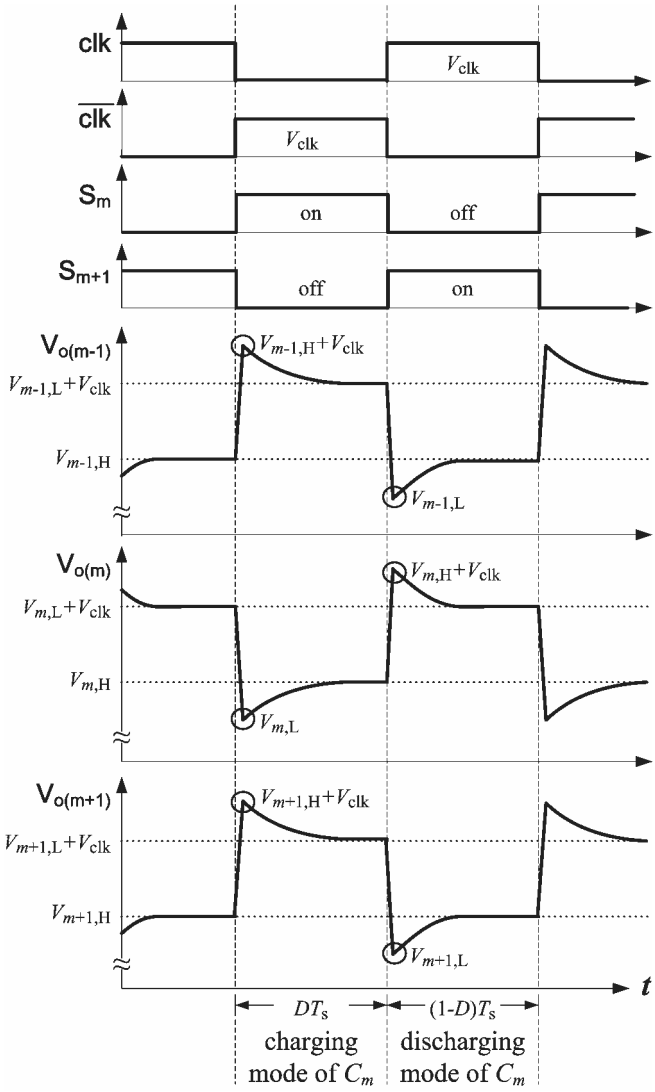


Fig. 4.2 The clock signal, states of switches, and the steady-state waveforms of $V_{o(m-1)}$, $V_{o(m)}$, and $V_{o(m+1)}$.

In order to find a general model, the charge balance and the average of V_m are used to calculate the transfer charge and the average current between pump capacitors. In Fig. 4.2, V_m

increases from the lowest level $V_{m,\mathrm{L}}$ to the highest level $V_{m,\mathrm{H}}$ in the charging mode of C_m and decreases back to $V_{m,\mathrm{L}}$ in the discharging mode. Let $V_{m,\mathrm{avg}}$ denote the arithmetic average of $V_{m,\mathrm{L}}$ and $V_{m,\mathrm{H}}$ and be given as

$$V_{m,\mathrm{avg}} = \frac{V_{m,\mathrm{H}} + V_{m,\mathrm{L}}}{2} \tag{4.1}$$

Similar notations are also applied to all voltages across pump capacitors.

From Fig. 4.2, in the time DT_s which is the charging mode of C_m, $V_{\mathrm{o}(m\text{-}1)}$ is lifted up by $\overline{\mathrm{clk}}$, and part of the charge $\Delta Q_{m,\mathrm{charge}}$ stored in $C_{m\text{-}1}$ will transfer to C_m. Thus, V_m will increase from $V_{m,\mathrm{L}}$ to $V_{m,\mathrm{H}}$, and $V_{m\text{-}1}$ will decrease from $V_{m\text{-}1,\mathrm{H}}$ to $V_{m\text{-}1,\mathrm{L}}$. By using charge conservation, $\Delta Q_{m,\mathrm{charge}}$ can be expressed as

$$\Delta Q_{m,\mathrm{charge}} = C_{m-1}\left(V_{m-1,\mathrm{H}} - V_{m-1,\mathrm{L}}\right) = C_m\left(V_{m,\mathrm{H}} - V_{m,\mathrm{L}}\right) \tag{4.2}$$

If DT_s is sufficiently large to complete the charge transfer in time, the node voltage $V_{\mathrm{o}(m\text{-}1)}$ and $V_{\mathrm{o}(m)}$ will be almost equal at the end of DT_s and that can be expressed as

$$V_{\mathrm{clk}} + V_{m-1,\mathrm{L}} = V_{m,\mathrm{H}} \tag{4.3}$$

or an alternative expression useful for finding $\Delta Q_{m,\mathrm{charge}}$ given as

$$V_{\mathrm{clk}} + V_{m-1,\mathrm{H}} - \Delta V_{m-1} = V_{m,\mathrm{L}} + \Delta V_{m,\mathrm{charge}} \tag{4.4}$$

where $\Delta V_{m-1} = V_{m-1,\mathrm{H}} - V_{m-1,\mathrm{L}}$ and $\Delta V_{m,\mathrm{charge}} = V_{m,\mathrm{H}} - V_{m,\mathrm{L}}$

From (4.1) – (4.4), the transferred charge $\Delta Q_{m,\mathrm{charge}}$ can be expressed by average voltages and obtained as

$$\Delta Q_{m,\mathrm{charge}} = \frac{C_{m\text{-}1}C_m}{C_{m\text{-}1}+C_m}\left(V_{\mathrm{clk}} + V_{m\text{-}1,\mathrm{H}} - V_{m,\mathrm{L}}\right) = \frac{2C_{m\text{-}1}C_m}{C_{m\text{-}1}+C_m}\left(V_{\mathrm{clk}} + V_{m\text{-}1,\mathrm{avg}} - V_{m,\mathrm{avg}}\right) \tag{4.5}$$

In (4.5), it can be seen that there is only $\Delta Q_{m,\mathrm{charge}}$ transferring from $C_{m\text{-}1}$ to C_m in a cycle time so that the average charging current $I_{m,\mathrm{avg}}$ of C_m corresponding to $\Delta Q_{m,\mathrm{charge}}$ can be found by

$$I_{m,\mathrm{avg}} = \frac{\Delta Q_{m,\mathrm{charge}}}{T_\mathrm{s}} = \frac{C_{m\text{-}1}C_m}{C_{m\text{-}1}+C_m}\cdot\frac{2}{T_\mathrm{s}}\left(V_{\mathrm{clk}} + V_{m\text{-}1,\mathrm{avg}} - V_{m,\mathrm{avg}}\right) \tag{4.6}$$

This average charging current $I_{m,\mathrm{avg}}$ of C_m also can be considered as the average discharging

current $I_{m\text{-}1,\text{avg}}$ of $C_{m\text{-}1}$. Equation (4.6) shows that $I_{m,\text{avg}}$ is a linear function of the difference between (V_{clk}+$V_{m\text{-}1,\text{avg}}$) and $V_{m,\text{avg}}$. Thus, the equivalent resistance between the nodes (m-1) and m can be obtained as

$$R_m \equiv \frac{T_s}{2C_{m\text{-}1}C_m/\left(C_{m\text{-}1}+C_m\right)} \tag{4.7}$$

where the value of $C_{m\text{-}1}C_m/\left(C_{m\text{-}1}+C_m\right)$ is regarded as $C_{m\text{-}1}$ and C_m in series.

Based on above description related to the charging mode of C_m, the behavior of m-th pump stage in the time DT_s can be derived from (4.6) – (4.7) and shown in Fig. 4.3(a).

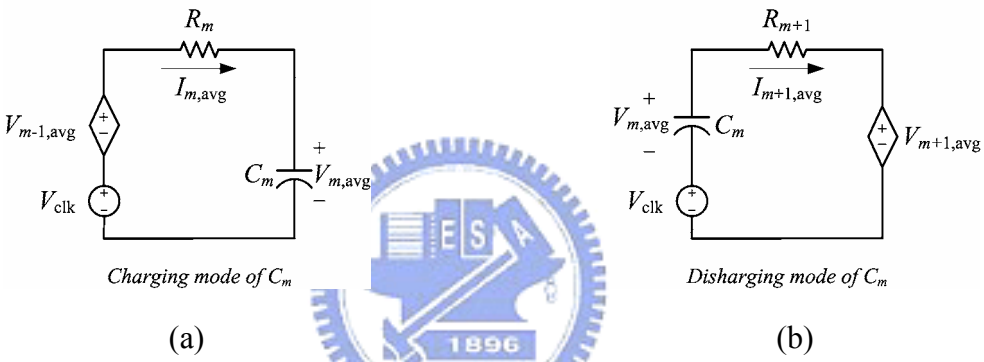


Fig. 4.3 Equivalent model for (a) charging mode of C_m and (b) discharging mode of C_m.

Similarly, in the time (1-D)T_s which is the discharging mode of C_m, the pumping operation between C_m and C_{m+1} behaves in a similar manner as the operation between $C_{m\text{-}1}$ and C_m, except that clk changes to high and $\overline{\text{clk}}$ changes to low. Thus, from the same procedure, part of the charge $\Delta Q_{m,\text{discharge}}$ stored in C_m will transfer to C_{m+1} and can be expressed as

$$\Delta Q_{m,\text{discharge}} = \frac{2C_mC_{m+1}}{C_m+C_{m+1}}\left(V_{\text{clk}}+V_{m,\text{avg}}-V_{m+1,\text{avg}}\right) \tag{4.8}$$

Therefore, in a (1-D)T_s duration, the average discharging current $I_{m+1,\text{avg}}$ of C_m (or the average charging current of C_{m+1}) and the equivalent resistance between nodes m and (m+1) can be obtained as

$$I_{m+1,\text{avg}} = \frac{\Delta Q_{m,\text{discharge}}}{T_s} = \frac{C_mC_{m+1}}{C_m+C_{m+1}}\cdot\frac{2}{T_s}\left(V_{\text{clk}}+V_{m,\text{avg}}-V_{m+1,\text{avg}}\right) \tag{4.9}$$

and

$$R_{m+1} \equiv \frac{T_s}{2C_m C_{m+1} / \left(C_m + C_{m+1}\right)} \tag{4.10}$$

From above description related to the discharging mode of C_m, the behavior of m-th pump stage in the time $(1\text{-}D)T_S$ can also be derived from (4.9) – (4.10) and shown in Fig. 4.3(b). Since Fig. 4.3 shows a simple and regular modular structure based on the equations (4.5) – (4.10), the equivalent model of each intermediate stage of PGI circuits can be deduced as the m-th pump stage model shown in Fig. 4.4. Because of its simple and regular scheme, this equivalent model can be taken as a module to cascade with other duplicate ones for planning a multi-stage PGI circuit.

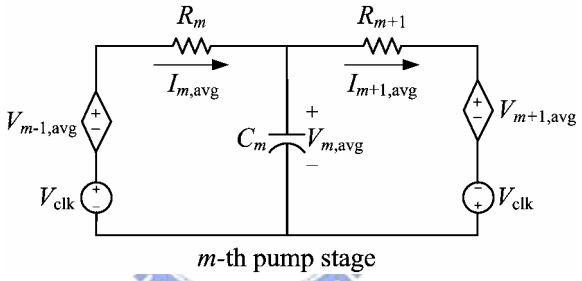


Fig. 4.4 Equivalent model for the m-th pump stage.

4.2.2 Behavioral Model of Input Stage

In the first stage, the equivalent model of the charging mode of C_1 is a little different from the general model mentioned above, since the preceding stage is connected to a voltage source V_{DD}. Thus, the average voltage of V_1 has to be modified as

$$V_{1,avg} = \frac{V_{DD} + V_{1,L}}{2} \tag{4.11}$$

In the charging mode of C_1, V_1 increases from the lowest level $V_{1,L}$ to V_{DD}. Replacing (4.11) into the formula of charge conservation, the transferred charge $\Delta Q_{1,charge}$ in a cycle time can be expressed by $V_{1,avg}$ and V_{DD} and given as

$$\Delta Q_{1,charge} = C_1\left(V_{DD} - V_{1,L}\right) = 2C_1\left(V_{DD} - V_{1,avg}\right) \tag{4.12}$$

Therefore, the corresponding average charging current $I_{1,\text{avg}}$ of C_1 and the resultant equivalent resistor R_1 are given as

$$I_{1,\text{avg}} = \frac{\Delta Q_{1,\text{charge}}}{T_s} = \frac{2C_1}{T_s}\left(V_{\text{DD}} - V_{1,\text{avg}}\right) \tag{4.13}$$

and

$$R_1 \equiv \frac{T_s}{2C_1} \tag{4.14}$$

The operation of C_1 in its discharging mode is the same as that of the inner pump capacitor C_m mentioned in section 4.2.1. Thus, the average discharging current $I_{2,\text{avg}}$ of C_1, which is also the average charging current of C_2, and the equivalent resistor R_2 can be obtained from (4.9) and (4.10) and given as

$$I_{2,\text{avg}} = \frac{\Delta Q_{1,\text{discharge}}}{T_s} = \frac{C_1 C_2}{C_1 + C_2} \cdot \frac{2}{T_s}\left(V_{\text{clk}} + V_{1,\text{avg}} - V_{2,\text{avg}}\right) \tag{4.15}$$

and

$$R_2 \equiv \frac{T_s}{2C_1C_2/\left(C_1 + C_2\right)} \tag{4.16}$$

Thus, employing (4.13) – (4.16), the equivalent model of the first pump stage in the PGI circuit can be depicted as shown in Fig. 4.5.

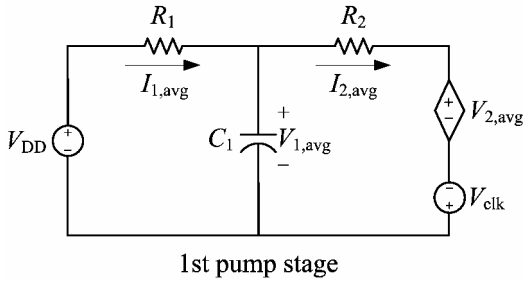


Fig. 4.5 Equivalent model for the first pump stage.

4.2.3 Behavioral Model of Last Stage and Output Stage

The load can be generally represented by a resistive load R_L connected in parallel to the output capacitor C_O. Thus, the behavior of the charge transmitted to R_L during each cycle period must be included in the model operation. According to the equivalent circuit shown in Fig. 4.1, the corresponding waveforms of the node voltage on the top of the last pump capacitor C_N, referred to $V_{o(N)}$, and the output voltage V_o are given in Fig. 4.6.

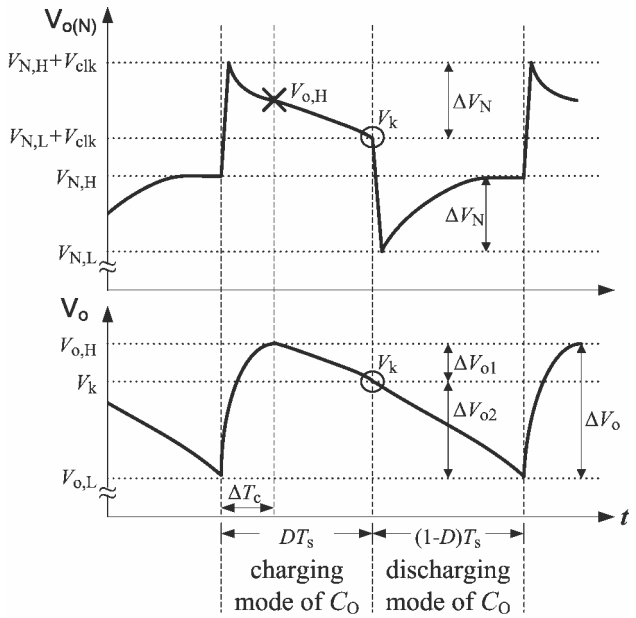


Fig. 4.6 The steady-state waveforms of $V_{o(N)}$ and V_o.

While in the charging period DT_s of C_O, the switch S_o is turned on and the charge is quickly delivered from C_N to C_O in a very short period ΔT_c. This causes V_o to increase from its low level $V_{o,L}$ to high level $V_{o,H}$. After ΔT_c, C_N and C_O discharge through R_L as a parallel capacitance $C_N||C_O$. At the end of the DT_s period, both V_o and $V_{o(N)}$ will decrease from their high level to a voltage V_k as follows:

$$V_k = V_{o,H} - \Delta V_{o1} = V_{N,H} + V_{clk} - \Delta V_N \tag{4.17}$$

where the variation of $V_{o(N)}$ in the DT_s period can be given as $\Delta V_N = V_{N,H} - V_{N,L}$, and ΔV_{o1} is

the voltage drop values in the periods of (DT_s – ΔT_c) as shown in Fig. 4.6. Assuming that $\Delta T_c \ll DT_s$ and using charge conservation, the consumed charge of R_L in the DT_s period can be considered as

$$\Delta Q_{R,D} = \frac{V_{o,avg}}{R_L} DT_s = \left(C_N + C_O\right)\Delta V_{o1} \tag{4.18}$$

When the discharging period $(1–D)T_s$ of C_O starts, the switch S_o is turned off and the consumed charge of R_L is only provided by C_O. At the end of the $(1–D)T_s$ period, V_o will decrease from V_k to its low level as follows:

$$V_{o,L} = V_k - \Delta V_{o2} \tag{4.19}$$

where ΔV_{o2} is the voltage drop values in the periods of $(1–D)T_s$ as shown in Fig. 4.6. Similarly, by using charge conservation, the consumed charge of R_L in the $(1–D)T_s$ period can be considered as

$$\Delta Q_{R,(1\text{-}D)} = \frac{V_{o,avg}}{R_L}\left(1-D\right)T_s = C_O \Delta V_{o2} \tag{4.20}$$

In a cycle time, from (4.18) and (4.20), ΔV_{o1} and ΔV_{o2} can be derived as

$$\Delta V_{o1} = \frac{C_O D}{C_N\left(1-D\right)+C_O}\Delta V_o \tag{4.21}$$

and

$$\Delta V_{o2} = \frac{\left(C_O + C_N\right)\left(1-D\right)}{C_N\left(1-D\right)+C_O}\Delta V_o \tag{4.22}$$

where $\Delta V_o = V_{o,H} - V_{o,L}$. From (4.21) and (4.22), ΔV_{o1} is smaller than ΔV_{o2} because ΔV_{o1} is produced from the discharge of $C_N||C_O$ and ΔV_{o2} is produced only from the discharge of C_O.

Considering charge conservation in the period of DT_s, the charge delivered from C_N to C_O in a very short period ΔT_c at the start of the DT_s period results in V_o to increase from $V_{o,L}$ to $V_{o,H}$ and $V_{o(N)}$ to decrease from ($V_{N,H}$ + V_{clk}) to $V_{o,H}$. Afterward, C_N and C_O discharge through R_L, and both V_o and $V_{o(N)}$ decrease from $V_{o,H}$ to V_k. By employing the average conception in this period, it can be supposed that V_o increases from $V_{o,L}$ to V_k and all the consumed charge

of R_L in the DT_s period is provided by C_N that causes $V_{o(N)}$ decreasing from ($V_{N,H}$ + V_{clk}) to V_k as shown in Fig. 4.7. In other words, in each cycle time, the transfer charge $\Delta Q_{N,discharge}$ discharging from C_N is equal to the summation of the obtained charge $\Delta Q_{O,charge}$ of C_O and the consumed charge $\Delta Q_{R,D}$ of R_L during DT_s. This relation can be expressed as

$$\Delta Q_{N,discharge} = \Delta Q_{O,charge} + \Delta Q_{R,D} \tag{4.23}$$

where

$$\Delta Q_{N,discharge} = C_N \Delta V_N \tag{4.24}$$

$$\Delta Q_{O,charge} = C_O \left(V_k - V_{o,L} \right) = C_O \Delta V_{o2} \tag{4.25}$$

$$\Delta Q_{R,D} = \frac{V_{o,avg}}{R_L} DT_s \tag{4.26}$$

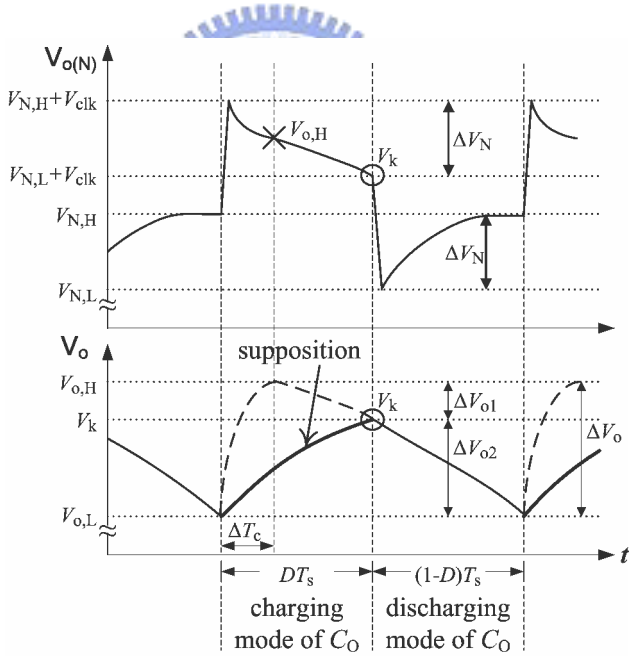


Fig. 4.7 The supposed steady-state waveforms of $V_{o(N)}$ and V_o.

Substituting (4.24) – (4.26) into (4.23), the following equation is obtained as

$$\Delta V_N = \frac{C_O}{C_N} \Delta V_{o2} + \frac{V_{o,avg}}{C_N R_L} DT_s \tag{4.27}$$

Employing (4.17), (4.19), (4.27), and the average definitions of $V_{o,avg}$ and $V_{N,avg}$ as (4.1), the

relationship between ΔV_{o1} and ΔV_{o2} can be obtained as

$$\left(1+\frac{C_O}{C_N}\right)\Delta V_{o2}=2\left(V_{clk}+V_{N,avg}-V_{o,avg}\right)+\Delta V_{o1}-\frac{V_{o,avg}}{C_N R_L}DT_s \tag{4.28}$$

Substituting (4.21) and (4.22) into (4.28), the voltage variation ΔV_o can be found as

$$\begin{aligned}\Delta V_o=&\frac{2C_N{}^2(1-D)+C_NC_O}{(1-D)(C_N+C_O)^2-C_NC_OD}\left(V_{clk}+V_{N,avg}-V_{o,avg}\right)\\&-\frac{C_N(1-D)+C_O}{(1-D)(C_N+C_O)^2-C_NC_OD}\cdot\frac{V_{o,avg}}{R_L}DT_s\end{aligned} \tag{4.29}$$

In addition, substituting (4.22) and (4.29) into (4.27), the voltage variation ΔV_N is found as

$$\begin{aligned}\Delta V_N=&\frac{2C_O(C_N+C_O)(1-D)}{(1-D)(C_N+C_O)^2-C_NC_OD}\left(V_{clk}+V_{N,avg}-V_{o,avg}\right)\\&+\frac{C_N(1-D)+C_O(1-2D)}{(1-D)(C_N+C_O)^2-C_NC_OD}\cdot\frac{V_{o,avg}}{R_L}DT_s\end{aligned} \tag{4.30}$$

Using the voltage variations ΔV_N to derive the charge transfer rate, the average discharging current $I_{Nd,avg}$ of C_N in a cycle time corresponding to $\Delta Q_{N,discharge}$ which is the charge delivered from C_N can be simply obtained as

$$\begin{aligned}I_{Nd,avg}=&\frac{\Delta Q_{N,discharge}}{T_s}=\frac{C_N\Delta V_N}{T_s}\\=&\frac{2}{T_s}\cdot\frac{C_NC_O(C_N+C_O)(1-D)}{(1-D)(C_N+C_O)^2-C_NC_OD}\left(V_{clk}+V_{N,avg}-V_{o,avg}\right)\\&+\frac{C_N{}^2(1-D)+C_NC_O(1-2D)}{(1-D)(C_N+C_O)^2-C_NC_OD}\cdot\frac{V_{o,avg}}{R_L}D\\=&I_{NO}+I_{NR,D}\end{aligned} \tag{4.31}$$

In (4.31), the first term is shown the average current (I_{NO}) delivered from C_N to C_O, and the second term is the average current ($I_{NR,D}$) from C_N to R_L during DT_s. Comparing (4.9) with (4.31), $I_{Nd,avg}$ is different from all the average discharging currents of inner pump stages and $I_{Nd,avg}$ no longer varies with only the difference between (V_{clk}+$V_{N,avg}$) and $V_{o,avg}$. From (4.31), the equivalent resistance can be obtained as

$$R_{NO} \equiv \frac{T_s}{2} \cdot \frac{(1-D)(C_N + C_O)^2 - C_N C_O D}{C_N C_O (C_N + C_O)(1-D)} = \frac{T_s}{2}\left[\frac{C_N + C_O}{C_N C_O} - \frac{D}{(C_N + C_O)(1-D)}\right] \tag{4.32}$$

$$R_{NR,D} \equiv \frac{1}{D} \cdot \frac{(1-D)(C_N + C_O)^2 - C_N C_O D}{C_N{}^2 (1-D) + C_N C_O (1-2D)} R_L \tag{4.33}$$

where R_{NO} is connected between the node N and the output terminal, and $R_{NR,D}$ is connected at the output terminal.

Similarly to (4.31), using the voltage variation ΔV_o from (4.29), the average charging current $I_{oc,avg}$ of C_O in a cycle time corresponding to $\Delta Q_{O,charge}$ which is the charge obtained by C_N can be derived as

$$\begin{aligned} I_{oc,avg} &= \frac{\Delta Q_{O,charge}}{T_s} = \frac{C_O \Delta V_o}{T_s} \\ &= \frac{2}{T_s} \cdot \frac{C_N C_O (C_N + C_O)(1-D)}{(1-D)(C_N + C_O)^2 - C_N C_O D}\left(V_{clk} + V_{N,avg} - V_{o,avg}\right) \\ &\quad - \frac{C_O (C_N + C_O)(1-D)}{(1-D)(C_N + C_O)^2 - C_N C_O D} \cdot \frac{V_{o,avg}}{R_L} D \\ &= I_{NO} - I_{OR,D} \end{aligned} \tag{4.34}$$

The first term is equal to I_{NO} delivered from C_N to C_O, and the second term is the average current ($I_{OR,D}$) from C_O to R_L in the DT_s period. In addition, from (4.31) and (4.34), it can be found that the consumed charge $\Delta Q_{R,D}$ of R_L during DT_s can be obtained as

$$\Delta Q_{R,D} = \left(I_{Nd,avg} - I_{oc,avg}\right)T_s = \left(I_{NR,D} + I_{OR,D}\right)T_s = \frac{V_{o,avg}}{R_L} DT_s \tag{4.35}$$

which agrees with the definition of (4.26). From (4.34), the equivalent resistance can be obtained as

$$R_{NO} \equiv \frac{T_s}{2}\left[\frac{C_N + C_O}{C_N C_O} - \frac{D}{(C_N + C_O)(1-D)}\right] \tag{4.36}$$

$$R_{OR,D} \equiv \frac{1}{D} \cdot \frac{(1-D)(C_N + C_O)^2 - C_N C_O D}{C_O (C_N + C_O)(1-D)} R_L = \left[\frac{C_N + C_O}{C_O D} - \frac{C_N}{(C_N + C_O)(1-D)}\right] R_L \tag{4.37}$$

where R_{NO} is connected between the nodes N and the output terminal, and $R_{OR,D}$ is connected at the output terminal.

In the $(1–D)T_s$ period, the consumed charge $\Delta Q_{R,(1\text{-}D)}$ of R_L is only provided by C_O as shown in (4.20). Thus, this average current $I_{OR,(1\text{-}D)}$ and the equivalent resistance $R_{OR,(1\text{-}D)}$ are given as

$$I_{OR,(1\text{-}D)} = \frac{\Delta Q_{R,(1\text{-}D)}}{T_s} = \frac{V_{o,avg}}{R_L}(1-D) \tag{4.38}$$

and

$$R_{OR,(1\text{-}D)} \equiv \frac{R_L}{(1-D)} \tag{4.39}$$

Based on equations (4.31) – (4.39), the equivalent model of the last (N-th) pump stage and the output stage can be derived and shown in Fig. 4.8.

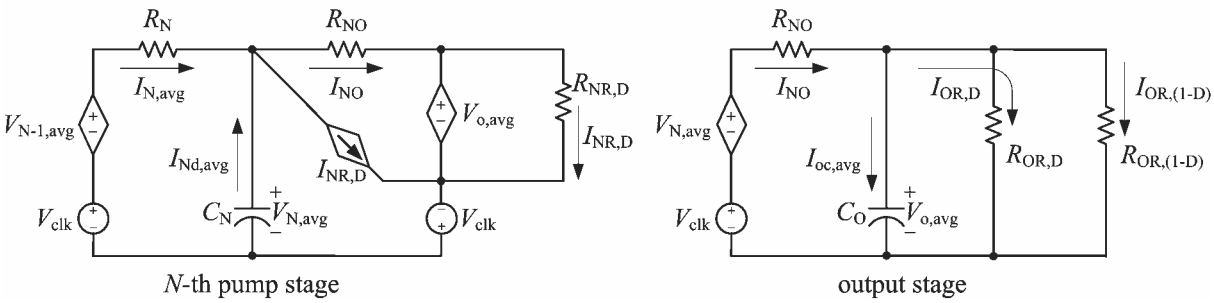


Fig. 4.8 Equivalent model for the last pump stage and the output stage.

4.2.4 Simplification of the Equivalent Model

From equations (4.31) – (4.39) and Fig. 4.8, although the last and the output models can be deduced, it is complicated and unfit to merge with general ones for creating the whole equivalent model. This equivalent circuit model can be simplified greatly if ΔV_{o1} is equal to ΔV_{o2} or $V_{o,avg} = V_k$.

Assuming that $\Delta T_c \ll DT_s$, ΔV_{o1} is the drop voltage caused by discharging from $C_N||C_O$ to R_L in the time DT_s, and ΔV_{o2} is the drop voltage caused by discharging only from C_O to R_L in

the time $(1–D)T_s$. Thus, ΔV_{o1} and ΔV_{o2} are proportional to the discharge time and inversely to the capacitances. The voltage variations can be given as

$$\Delta V_{o1} = \frac{DT_s V_{o,avg}}{R_L\left(C_N + C_O\right)} \tag{4.40}$$

and

$$\Delta V_{o2} = \frac{\left(1-D\right)T_s V_{o,avg}}{R_L C_O} \tag{4.41}$$

By equalizing the expressions of ΔV_{o1} and ΔV_{o2}, the condition of $V_{o,avg} = V_k$ can be met by choosing C_N and C_O such that

$$\frac{D}{1-D} = \frac{C_N + C_O}{C_O} \tag{4.42}$$

Employing (4.42), $V_{o,avg}$ is being substituted for V_k, and $\Delta V_{o1} = \Delta V_{o2} = \left(1/2\right)\Delta V_o$. Through the same derive procedure mentioned in section 4.2.3, the average discharging current $I_{Nd,avg}$ and the equivalent discharging resistance R_{Nd} of C_N can be rewritten as

$$I_{Nd,avg} = \frac{2C_N}{T_s}\left(V_{clk} + V_{N,avg} - V_{o,avg}\right) \tag{4.43}$$

and

$$R_{Nd} = \frac{T_s}{2C_N} \tag{4.44}$$

Similarly, the average charging current $I_{oc,avg}$ of C_O and its equivalent charging resistance can be derived as

$$I_{oc,avg} = \frac{2C_N}{T_s}\left(V_{clk} + V_{N,avg} - V_{o,avg}\right) - \frac{V_{o,avg}}{R_L}D = I_{Nd,avg} - I_{OR,D} \tag{4.45}$$

$$R_{Nd} = \frac{T_s}{2C_N} \tag{4.46}$$

$$R_{OR,D} \equiv \frac{R_L}{D} \tag{4.47}$$

In the $(1–D)T_s$ period, the average current $I_{OR,(1-D)}$ and the equivalent resistance $R_{OR,(1-D)}$ are identical with (4.38) and (4.39), respectively. In Fig. 4.8, it can be seen that the equivalent

output resistance is connected as $R_{OR,D}$ and $R_{OR,(1\text{-}D)}$ in parallel. From (4.39) and (4.47), the value of $R_{OR,D}||R_{OR,(1\text{-}D)}$ is exactly equal to R_L. Composing the relationships (4.38) – (4.47), the equivalent model of the last pump stage and the output stage can be simplified as shown in Fig. 4.9.

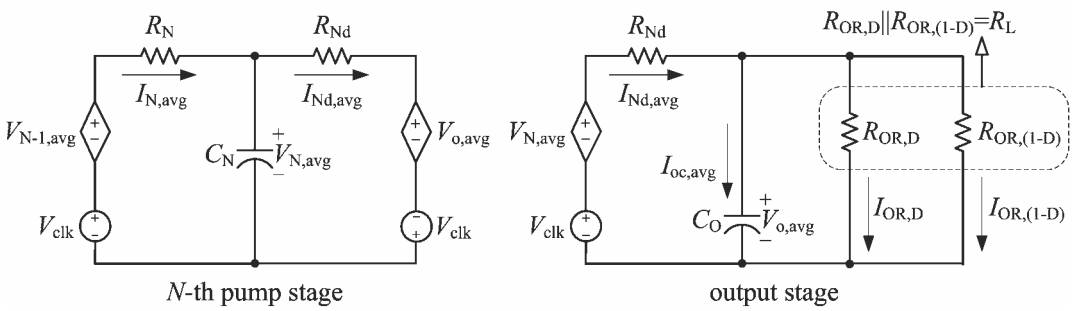


Fig. 4.9 Equivalent simplified model for the last pump stage and the output stage.

The above behavior analysis of regular inner stages, the input stage, the last stage, and the output stage gives the whole equivalent model of an N-stage PGI circuit shown in Fig. 4.10. In the complete circuit model, all labeled voltages are averages and each dependent voltage source is controlled by the voltage across the corresponding capacitor. Based on this regular and simplified model, the behavior of a multi-stage PGI circuit with a resistive load can be easily controlled and designed.

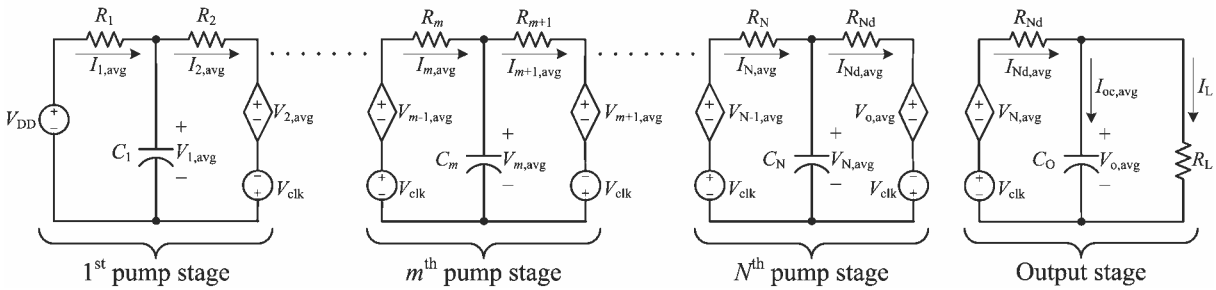


Fig. 4.10 Equivalent model for an N-stage PGI circuit.

4.3 Optimization

The practical output voltage of the PGI circuit with a resistive load varies around its average value once the charge pump circuit reaches its final value, so that $V_{o,avg}$ in the presented equivalent model can represent the steady-state output value with undulation. Moreover, for obtaining a desired output value in the steady state, circuit parameters such as capacitor values and the duty ratio of the pump clock can be calculated form the equivalent model.

As can be seen in Fig. 4.10, all pump capacitors can be considered open when the PGI circuit reaches the steady state, so that all transfer currents ($I_{m,avg}$) on equivalent resistors will be identical with the load current I_L. Equalizing the equations of all these transfer currents mention in section 4.2, the average voltage $V_{o,avg}$ of an N-stage PGI circuit in the steady state can be found and expressed simply by

$$V_{o,avg} = \frac{R_L\left(V_{DD} + NV_{clk}\right)}{R_1 + R_2 + ... + R_N + R_{Nd} + R_L} = \frac{R_L\left(V_{DD} + NV_{clk}\right)}{\left(\sum_{m=1}^{N} R_m\right) + R_{Nd} + R_L} \tag{4.48}$$

Considering charge conservation in a cycle time, an approximation can be obtained as

$$\frac{V_{o,avg}}{R_L} T_s = C_O \Delta V_o \tag{4.49}$$

Substituting the equations of all equivalent resistances into (4.48) and replacing R_L by a approximate value from (4.49), $V_{o,avg}$ in the steady state can be rewritten as

$$V_{o,avg} = \left(V_{DD} + NV_{clk}\right) - C_O \Delta V_o \left(\frac{1}{C_1} + \frac{1}{C_2} + ... + \frac{1}{C_N}\right) = \frac{V_{DD} + NV_{clk}}{\left[1 + \frac{T_s}{R_L}\left(\sum_{m=1}^{N} \frac{1}{C_m}\right)\right]} = \frac{V_{DD} + NV_{clk}}{\left[1 + \frac{T_s}{R_L C_{series}}\right]} \tag{4.50}$$

where C_{series} represents the total capacitance of all pump capacitors connected in series.

In (4.50), $V_{o,avg}$ is directly relative to the pump capacitances, supply voltages, and the total number of pump stages. Besides C_O, which is mainly used to smooth the output voltage, is

designed by the allowable ΔV_o from (4.49) and the clock duty ratio D is found by (4.42), other pump capacitances and switching frequency f_s can be determined from (4.50) for obtaining a desired output value with a resistive load R_L. In addition, the result expressed by (4.50) shows that $V_{o,avg}$ is determined by the ratio of T_s to the constant $R_L \times C_{series}$. Thus, if the time constant $R_L \times C_{series}$ is smaller than T_s, $V_{o,avg}$ can be effectively regulated by tuning the switching period T_s.

From (4.50), an alternative expression of $V_{o,avg}$ in terms of the load current I_L can be obtained as

$$V_{o,avg} = \left(V_{DD} + NV_{clk}\right) - \frac{T_s}{C_{series}} I_L \tag{4.51}$$

In (4.51), the highest ideal output voltage ($V_{DD} + NV_{clk}$) will occur with the condition of $I_L = 0$. As the load current increases, the output voltage will decrease at a rate of (T_s/C_{series}). Moreover, if pump capacitors are all the same value, it can be seen that the derived result (4.51) would match the Dickson's result (2.4) with $C_s = 0$ and $V_{diode} = 0$. This comparison proves that the proposed model deduced from PGI circuits is an ideal case of the Dickson structure. Consequently, even though the model and the derivation were based on PGI circuits, it is shown that the same design strategy can be applied to any improved charge pump design which is able to eliminate voltage drop within the inner stages and the output stage as an ideal case.

Considering chip size and therefore cost, decreasing the sum of pump capacitances C_{TP} will greatly decrease the die area. Assuming that pump capacitances are designed proportionally as

$$K = \frac{C_1}{C_2} = \frac{C_2}{C_3} = ... = \frac{C_{m-1}}{C_m} = ... = \frac{C_{N-1}}{C_N} \tag{4.52}$$

where K is a regulative constant, a generalization about each pump capacitance can be expressed as

$$C_m = K^{(N-m)} C_N \tag{4.53}$$

In addition, from (4.50), the summation of ($1/C_m$) can be found as

$$\sum_{m=1}^{N}\frac{1}{C_m}=\frac{\left(V_{\mathrm{DD}}+NV_{\mathrm{clk}}-V_{\mathrm{o,avg}}\right)R_{\mathrm{L}}}{V_{\mathrm{o,avg}}T_{\mathrm{s}}} \tag{4.54}$$

Substituting (4.53) into (4.54), the last pump capacitance C_{N} is obtained by

$$C_N=\left(\frac{\sum_{i=1}^{N}K^{(i-1)}}{K^{(N-1)}}\right)\frac{V_{\mathrm{o,avg}}T_{\mathrm{s}}}{\left(V_{\mathrm{DD}}+NV_{\mathrm{clk}}-V_{\mathrm{o,avg}}\right)R_{\mathrm{L}}} \tag{4.55}$$

Thus, from (4.53) and (4.55), C_{TP} of an N-stage PGI circuit can be given as

$$C_{\mathrm{TP}}=\sum_{m=1}^{N}C_m=\sum_{m=1}^{N}K^{(N-m)}C_N=\left(\sum_{i=1}^{N}K^{(i-1)}\right)C_N=\frac{\left(\sum_{i=1}^{N}K^{(i-1)}\right)^2V_{\mathrm{o,avg}}T_{\mathrm{s}}}{K^{(N-1)}\left[\left(V_{\mathrm{DD}}+NV_{\mathrm{clk}}\right)-V_{\mathrm{o,avg}}\right]R_{\mathrm{L}}} \tag{4.56}$$

From (4.56), the minimum C_{TP} can be found by making $dC_{\mathrm{TP}}/dK=0$, which is given as

$$\frac{dC_{\mathrm{TP}}}{dK}=\left[\frac{2\left(\sum_{i=1}^{N}K^{(i-1)}\right)\left(\sum_{i=1}^{N}\frac{K^{(i-1)}(i-1)}{K}\right)}{K^{(N-1)}}-\frac{\left(\sum_{i=1}^{N}K^{(i-1)}\right)^2(N-1)}{K^{(N-1)}\times K}\right]\frac{V_{\mathrm{o,avg}}T_{\mathrm{s}}}{\left(V_{\mathrm{DD}}+NV_{\mathrm{clk}}-V_{\mathrm{o,avg}}\right)R_{\mathrm{L}}}=0 \tag{4.57}$$

This derivation has a reasonable solution which is K = 1. Thus, an arrangement is made by equalizing all pump capacitances for the minimum die area, and this minimum value of each pump capacitance referred as $C_{m,\mathrm{min}}$ is given by

$$C_{m,\mathrm{min}}=\frac{NV_{\mathrm{o,avg}}T_{\mathrm{s}}}{\left(V_{\mathrm{DD}}+NV_{\mathrm{clk}}-V_{\mathrm{o,avg}}\right)R_{\mathrm{L}}} \tag{4.58}$$

From (4.58), the minimum C_{TP} ($C_{\mathrm{TP,min}}$) in an N-stage PGI circuit can be found by $N\times C_{m,\mathrm{min}}$. Fig. 4.11 shows the relation between C_{TP} and K for various selected $V_{\mathrm{o,avg}}$ in a 3-stage example. It can be seen that the minimum C_{TP} exactly occurs at K = 1. Thus, if C_m is chosen according to (4.58), the PGI circuit with a fixed stage number would occupy the smallest die area for a desired output voltage with a resistive load.

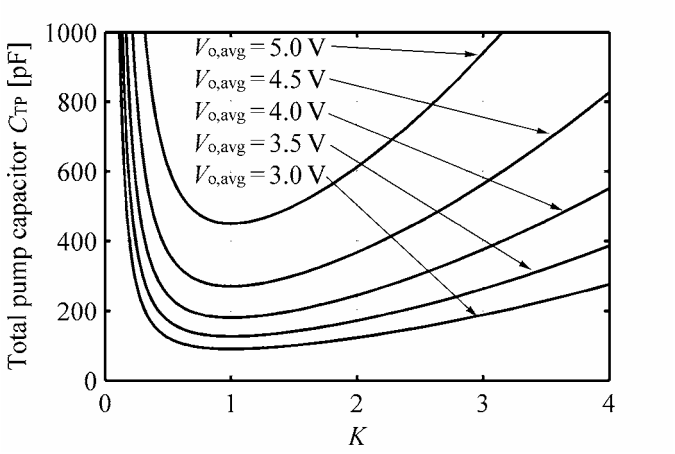


Fig. 4.11 Total pump capacitances C_{TP} calculated from the 3-stage model versus the value of K under various desired $V_{o,avg}$, where $V_{DD} = V_{clk} = 1.5$ V, $R_L = 100$ kΩ, and $f_s = 1$ MHz.

Furthermore, in the condition of $K = 1$, by solving $dC_{TP}/dN = 0$ for a fixed $V_{o,avg}$ given as

$$\frac{dC_{TP}}{dN} = \frac{2NV_{o,avg}T_s}{\left(V_{DD} + NV_{clk} - V_{o,avg}\right)R_L} - \frac{N^2 V_{o,avg}T_s V_{clk}}{\left(V_{DD} + NV_{clk} - V_{o,avg}\right)^2 R_L} = 0, \text{ where } K = 1 \qquad (4.59)$$

The optimum number of stages N associated with the minimum C_{TP} can be found. The solution is given as

$$N = \frac{2\left(V_{o,avg} - V_{DD}\right)}{V_{clk}} \qquad (4.60)$$

The optimum value of N must be an integer near the result of (4.60). Fig. 4.12 provides the information needed to find the suitable stage number N for generating a specified $V_{o,avg}$ with minimum C_{TP}. It can be seen that C_{TP} will enlarge as the desired $V_{o,avg}$ is close to the value of $(V_{DD} + NV_{clk})$. The parameters for an example of $V_{o,avg} = 4$ V are given in Table 4.1.

Table 4.1 Comparison between the value of C_{TP} under different stage number where $V_{o,avg} = 4$V, $V_{DD} = V_{clk} = 1.5$ V, $R_L = 100$ kΩ, $f_s = 1$ MHz, $\Delta V_o = 0.2$ V, and $C_O = 200$pF.

Stage number	$C_{m,min}$ (pF)	C_{TP} (pF)
$N = 2$	160	320
$N = 3$	60	180
$N = 4$	45.7	182.8
$N = 5$	40	200

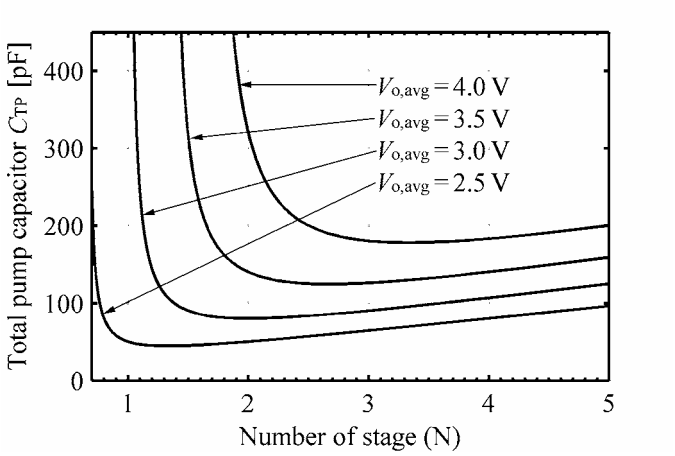


Fig. 4.12 Total pump capacitances C_{TP} versus the stage number N over various desired $V_{o,avg}$, where $K = 1$, $V_{DD} = V_{clk} = 1.5$ V, $R_L = 100$ kΩ, and $f_s = 1$ MHz.

As an example, by using the result from Fig. 4.11 and Fig. 4.12, a PGI circuit with an output voltage of 4 V across a resistive load of 100 kΩ can be designed for a minimum C_{TP} with $N = 3$ and $C_1 = C_2 = C_3 = 60$ pF.

4.4 Model Validation

4.4.1 Simulation Results

In order to validate the accuracy of the derived model, SPICE simulations are performed by output responses for both the equivalent 3-stage circuit shown in Fig. 4.1 and the corresponding 3-stage model, where $V_{DD} = V_{clk} = 1.5$ V, $R_L = 100$ kΩ, $f_s = 1$ MHz, and D was determined by employing the relation between C_3 and C_O from (4.42).

Fig. 4.13 shows the output simulation waveforms of the equivalent 3-stage circuit and the model, respectively, where the simulation conditions are $C_m = 60$ pF (m = 1, 2, 3), $C_O = 200$ pF, $I_L = 40$ μA, and $D = 0.57$. Under these design conditions, the output ripple ΔV_o of the equivalent 3-stage circuit is limited to 0.2 V, and the mean of this undulate output voltage is 4 V, which is equal to $V_{o,avg}$ of the model in the steady state. A satisfactory agreement between

these two simulations can be observed during the procedure of boosting. In addition, from additional simulation data with different C_m values and various pump stage numbers, the output value of the model always follows the undulate output waveform of the equivalent circuit as shown in Fig. 4.14 and Fig. 4.15. Consequently, these simulation results show that the presented model can predict the output behavior of a multi-stage PGI circuit with a resistive load.

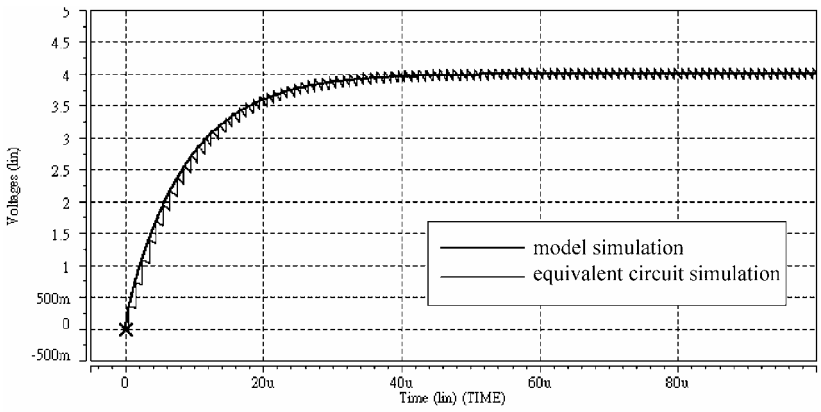


Fig. 4.13 Comparison between simulated output waveforms of the equivalent 3-stage circuit and of the corresponding model.

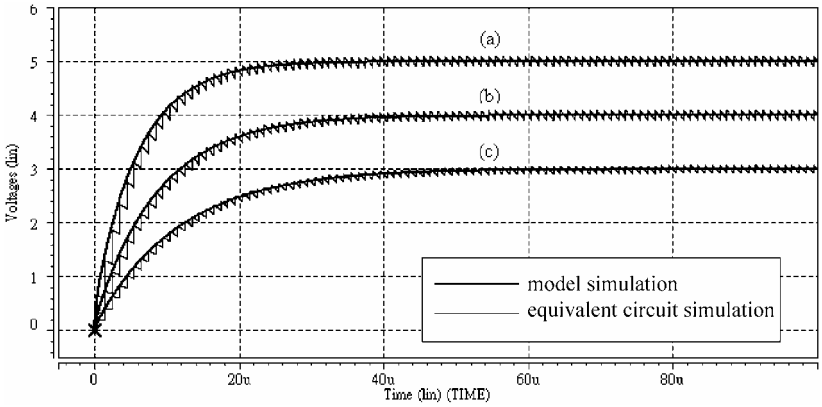


Fig. 4.14 Comparison between simulated output waveforms of the equivalent 3-stage circuit and of the corresponding model under different C_m values. (a) $V_{o,avg}$ = 5 V and C_m = 150 pF. (b) $V_{o,avg}$ = 4 V and C_m = 60 pF. (c) $V_{o,avg}$ = 3 V and C_m = 30 pF.

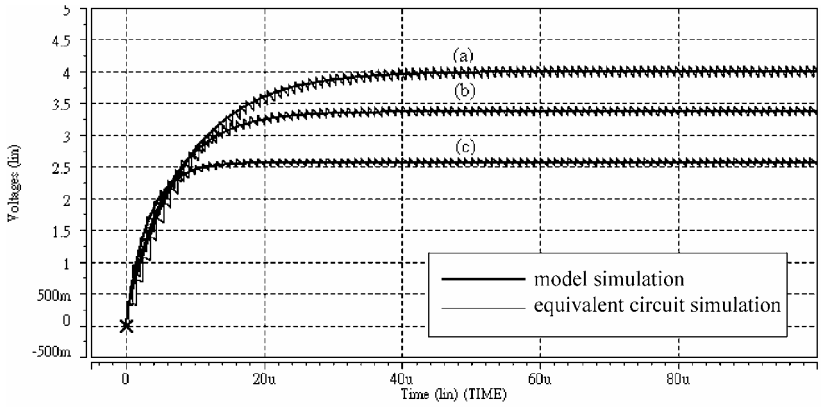
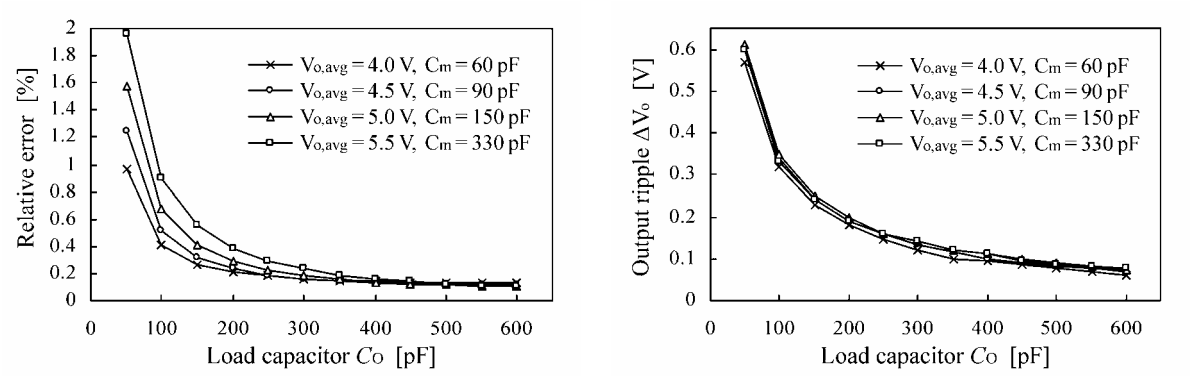


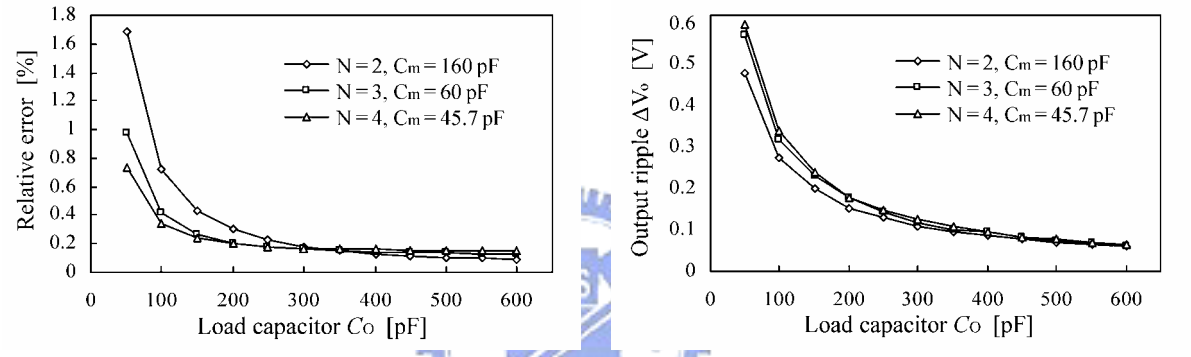
Fig. 4.15 Comparison between the simulated output waveforms of the equivalent circuit and of the corresponding model with various numbers of pump stages, where all pump capacitances are fixed at 60 pF. (a) 3-stage for $V_{o,avg}$ = 4 V. (b) 2-stage for $V_{o,avg}$ = 3.375 V. (c) 1-stage for $V_{o,avg}$ = 2.57 V.

However, in common uses, the duty ratio of CPCs is usually set to D = 0.5. With this configuration, (4.42) is ineffective in finding a suitable value of C_O/C_N for equating V_k to $V_{o,avg}$ shown in Fig. 4.7. If $C_O >> C_N$, ΔV_{o1} will be close to ΔV_{o2} and the difference between $V_{o,avg}$ and V_k can be reduced. Otherwise, a slightly greater error will exist. Consequently, when the duty ratio D = 0.5, the accuracy of the equivalent model depends on the ratio of C_N and C_O. Fig. 4.16(a) shows the difference error between $V_{o,avg}$ in the model and the mean of the undulate output voltage in the equivalent 3-stage circuit obtained from SPICE simulation results when a square clocks (D = 0.5) are employed. In addition, the corresponding value of the output ripple ΔV_o is shown in Fig. 4.16(b). Since the C_N/C_O ratio will decrease as the value of C_O increases, from Fig. 4.16, the larger the value of C_O is, the smaller the relative error and the output ripple ΔV_o will be. If C_O is larger than 200 pF, it appears that the error and ΔV_o are less than 0.4 % and 0.2 V, respectively. Similarly, by using various numbers of pump stages as shown in Table 4.1, the relative errors and ΔV_o of the equivalent circuit with $V_{o,avg}$ = 4 V and D = 0.5 are shown in Fig. 4.17.



(a) (b)

Fig. 4.16 (a) Relative errors between the model and the 3-stage circuit for different desired $V_{o,avg}$ with V_{DD} = V_{clk} = 1.5 V, R_L = 100 kΩ, f_s = 1 MHz, and D = 0.5. (b) Corresponding output ripple ΔV_o.



(a) (b)

Fig. 4.17 (a) Relative errors between the model and the equivalent circuit with different stage number N for $V_{o,avg}$ = 4 V and D = 0.5. (b) Corresponding output ripple ΔV_o.

A practical embodiment of a 3-stage PGI-3 circuit, which is built by the circuit shown in Fig. 3.4, was simulated in transistor level by using parameters of a TSMC 0.35-μm mixed mode process and using general clocks (D = 0.5). With the same simulation conditions used in Fig. 4.13 except that the duty ratio D = 0.5, the transient simulation waveforms are shown in Fig. 4.18. From the simulation results, the final mean value of the practical circuit is about 3.95 V, and the error between this mean value and the $V_{o,avg}$ (= 4 V) of the model is about 1.25%. In addition, other simulation results with different C_m values and various numbers of pump stages are shown in Fig. 4.19 and Fig. 4.20. The output value of the model can be demonstrated to follow the undulate output waveform of the practical PGI circuit.

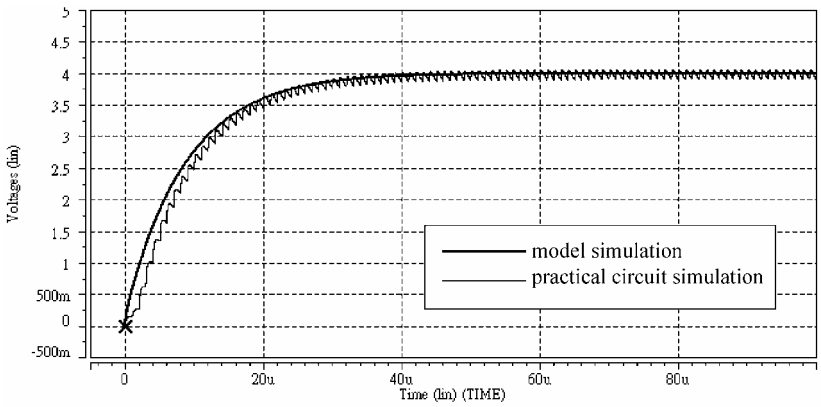


Fig. 4.18 Comparison between simulated output waveforms of the practical 3-stage PGI-3 circuit and of the corresponding model.

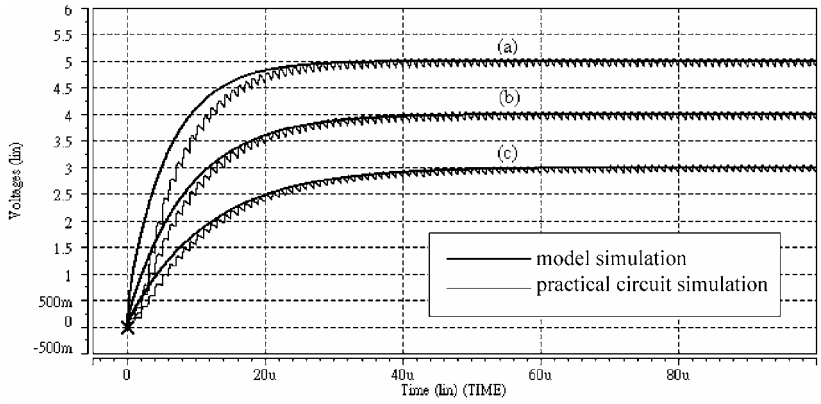


Fig. 4.19 Comparison between simulated output waveforms of the practical 3-stage PGI-3 circuit and of the corresponding model under different C_m values. (a) $V_{o,avg}$ = 5 V and C_m = 150 pF. (b) $V_{o,avg}$ = 4 V and C_m = 60 pF. (c) $V_{o,avg}$ = 3 V and C_m = 30 pF.

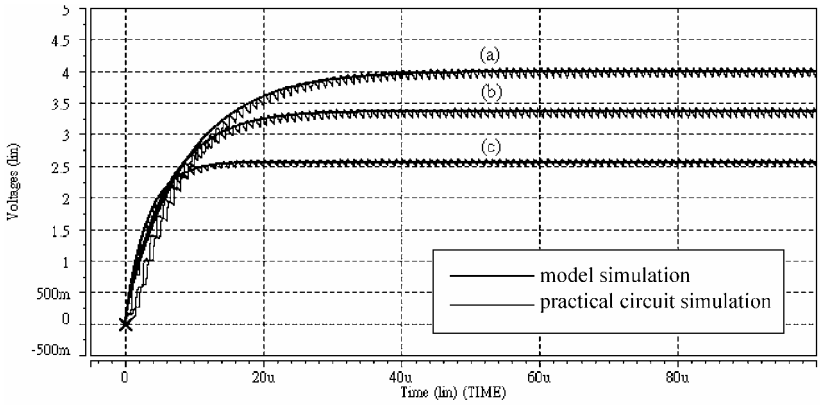


Fig. 4.20 Comparison between simulated output waveforms of the practical 3-stage PGI-3 circuit and of the corresponding model with various numbers of pump stages, where all pump capacitances are fixed at 60 pF. (a) 3-stage for $V_{o,avg}$ = 4 V. (b) 2-stage for $V_{o,avg}$ = 3.375 V. (c) 1-stage for $V_{o,avg}$ = 2.57 V.

Besides the influence of the duty ratio D, these small errors are most likely due to the fact that switching losses and parasitic capacitances of the practical PGI circuits are taken into account in SPICE simulations but not included in the equivalent model. In addition, the full practical circuit simulation waveform lags slightly behind that of the model. This waveform lag is due to the fact that gate control voltages of the transfer switches generated by CTS's in the PGI circuit would not be pumped to the levels for turning on the switches completely in the initial few cycles. In summary, the output behavior and the final $V_{o,avg}$ of the model closely match the simulation results of the practical PGI circuit. Thus, the presented simple and regular equivalent model is useful for designing PGI circuits.

4.4.2 Measurement Results

In order to validate results of the analysis and design considerations, several PGI circuits with different total number of stages were fabricated in a TSMC 0.35-μm mixed mode process. To increase the flexibility of the measurements, pump capacitors are connected externally. A 2-stage PGI-3 circuit with different values of C_m was tested under $V_{DD} = V_{clk} = 1.5$ V, $R_L =$ 100 kΩ, $f_s = 1$ MHz, $C_O = 330$ pF, and $C_1 = C_2 = C_m$. Three kinds of the output voltage data are plotted in Fig. 4.21 for the comparison. The first one is obtained from the simulation results of the presented model. The second one is obtained from the measured output voltage for $D = 0.5$. The last one is also obtained from the measured output voltage but the value of D is calculated from (4.42). The performance data and the corresponding error are summarized in Table 4.2.

Table 4.2 Simulated results of the model and measured results of the 2-stage PGI design.

Pump Capacitor C_m (pF)	Equivalent Model $V_{o,avg}$ (V)	Practical 2-Stage PGI-3 Design				
		D = 0.5		D is given by (4.42)		
		V_{out} (V)	Err	duty, D	V_{out} (V)	Err
47	3.16	3.03	4.1%	0.53	3.05	3.5%
100	3.75	3.65	2.7%	0.57	3.67	2.1%
147	3.96	3.88	2.0%	0.59	3.9	1.5%
220	4.13	4.03	2.4%	0.63	4.06	1.7%
267	4.19	4.08	2.6%	0.64	4.1	2.1%
330	4.24	4.11	3.1%	0.67	4.15	2.1%
430	4.30	4.16	3.3%	0.70	4.2	2.3%

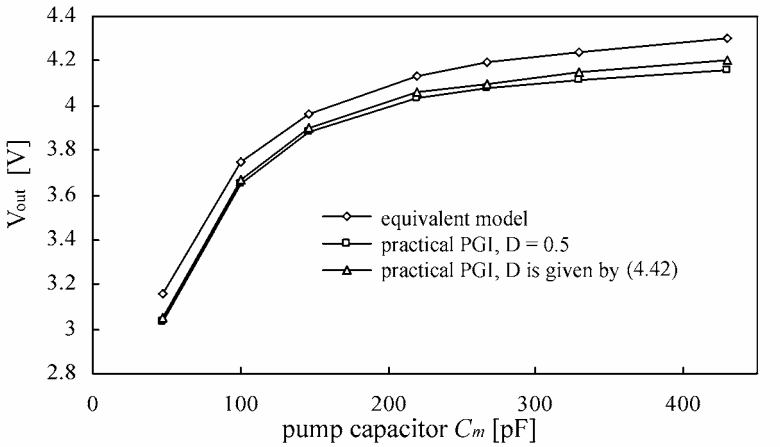


Fig. 4.21 Measured output voltages of a 2-stage PGI-3 circuit under different values of C_m.

For this typical example, measured output voltages are close to $V_{o,avg}$ of the model, e.g., for C_m = 100 pF, the mean values of the measured output voltage V_{out} are 3.65 V and 3.67 V when D = 0.5 and 0.57 calculated from (4.42), respectively, and $V_{o,avg}$ is 3.75 V when using the model simulation. It can be seen from Table 4.2 that the error voltages in this case are lower than 0.1 V, and all relative errors of the measurement are less than 5 %. The measured output voltage is smaller than the model simulation output voltage $V_{o,avg}$, due to additional parasitic capacitors, parasitic resistors, and extra switching losses. Leakage currents of any nature will also cause deviations from the model. In the case of C_m above 150 pF, where C_m/C_O is above 0.45, Fig. 4.21 shows that the V_{out} measured as D is obtained from (4.42) is more accurate than that measured as D = 0.5. However, even though the ratio of C_m/C_O is increased, relative errors in the case of D = 0.5 only increase slightly. This agrees with the theoretical result

depicted in Fig. 4.16. Consequently, as these data suggest, even the output voltage of the PGI circuit can be approximately predicted by the formula (4.48) from the deduced model, and accuracy can be increased by choosing an appropriate ratio of C_m/C_O.

Further experiments of the 2-stage PGI-3 circuit at $D = 0.5$ were also taken by changing the ratio of C_1 to C_2. The measured data are shown in Fig. 4.22. The curves of V_{out}-to-K and C_{TP}--to-K give information that $K = 1$ is the optimum selection to generate a desired DC output voltage. For instance, when $V_{out} = 3.6$ V is considered, Fig. 4.22 shows that $K = 1$ gives the minimum C_{TP}. This observation is in accordance with the prediction of (4.58).

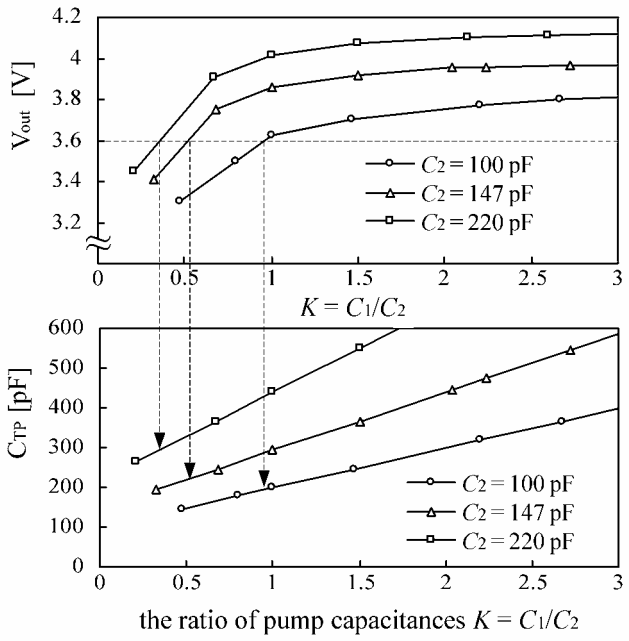


Fig. 4.22 Measured output voltages of a 2-stage PGI-3 circuit with a different ratio of C_1 and C_2.

4.5 Summary

A complete equivalent model of high efficient charge pumping gain increase circuits with a resistive load and the corresponding thorough analysis are proposed in this chapter. The equations of this average model also have been deduced for design within an acceptable

accuracy tolerance. By using the presented model and equations, the output behavior and the characteristics of PGI circuits can be approximately predicted. Furthermore, the pump capacitances and the switching period can be determined in satisfying the requirement of a desired final output voltage with a ripple ΔV_o. Based on the analysis presented, with a given resistive load and a desired output voltage across it, an optimal number of pump stages and equalized pump capacitors have been proved for the objective of minimum total pump capacitance, which represents minimum chip size.

In addition, the influence of the duty ratio D on the output voltage and the accuracy of the model under general clocks (D = 0.5) have been discussed. The simulation results of the presented model and the SPICE simulations of PGI circuits exhibit satisfactory agreement on transient behavior and the final value of the output voltage. Analysis of the measurement results for an integrated 2-stage PGI-3 circuit with resistive load also has validated the model. A comparison of data shows that the relative errors are lower than 5 %.

Since the structure of each pump stage model is simple and regular, it is easy to construct the complete model of a multi-stage PGI circuit. The importance of having a model like this is not only because it increases understanding of the output behavior of PGI circuits, but it also helps in the design procedure, giving an initial estimate of the silicon area required for pump capacitors to be used. Furthermore, although the derivation of the model was based on a PGI circuit, it is shown that the same design strategy can also be applied to any other improved charge pump designs that have no voltage drop within the inner stages and the output stage.

Chapter 5

Charge Pump Regulator Design Based on the Proposed Equivalent Model

5.1 Introduction

Conventional charge pump circuits are usually designed to operate at a fixed pump frequency with a rated output voltage without regulation. However, for most charge pump applications, the output load current is often inconstant. The output voltage generated by charge pump circuits has to be quite accurate, independent of the current drawn by the load, process, and environmental variations. Therefore, it is necessary to design a charge pump regulator to guarantee the output voltage level at the different loading.

The proposed average model provides a good substitute for a practical pumping gain increase circuit for mathematical analysis. By using the equivalent model, characterization of pumping gain increase circuits can be performed in a pencil-and-paper manner. Therefore, this model is helpful to plan the control scheme in arithmetic for an embodiment of the regulator based on the pumping gain increase circuit. With an appropriate control scheme, a desired output voltage can be obtained under changing conditions.

In this chapter, a design method of a charge pump regulator based on the proposed equivalent model is presented for battery power applications. A design example of a 2-stage

pumping gain increase circuit with a desired output voltage of 3 V across a resistive load is presented with a battery power of 1.5 V. In section 5.2, basic control concepts of conventional charge pump regulators are described. Section 5.3 gives characterization of the converter consisting of an equivalent model and a voltage controlled oscillator (VCO). A feedback control scheme employing a simple compensator is also described. In section 5.4, time-domain simulations of the model case and of the practical regulator in transistor level are presented for verification. Consequently, according to the design procedure, a charge pump style DC/DC regulator with a simple control scheme can be obtained.

5.2 Conception of Charge Pump Regulator

Fig. 5.1 illustrates a conventional boosted charge pump regulator, which is widely used as program/erase voltage generators for single voltage flash memories [42]-[43]. It supplies an inconsistent current consumed in the decoder of flash memory, and the output voltage is regulated to a substantial constant level with a finite insensitive voltage window. In Fig. 5.1, the conventional charge pump regulator contains three separate blocks: a charge pump circuit, an oscillator, and a low voltage detector. When the output voltage is below the rated value, the comparator turns on the oscillator. Otherwise the comparator disables the oscillator. The comparable signal is obtained by scaling down the output voltage from a resistive voltage divider and comparing it to a band-gap reference voltage (V_{bg}). Hysteresis added to the comparator circuit prevents for undesirable operation when the supply carries noise. By using this control scheme, a relative constant output voltage with a variable load current can be achieved.

In the conventional regulator, the clock blocking scheme is adopted to isolate the output voltage level from the value of a load resistor, which determines the load current. The charge

pump continues to charge the load capacitor during the pumping period and stops during the blocking period. Although its average output voltage has a constant value regardless of load resistance, a large output ripple is generated during the pumping and the blocking periods, especially in the case of a large load current. The operation of clock blocking is shown in Fig. 5.2.

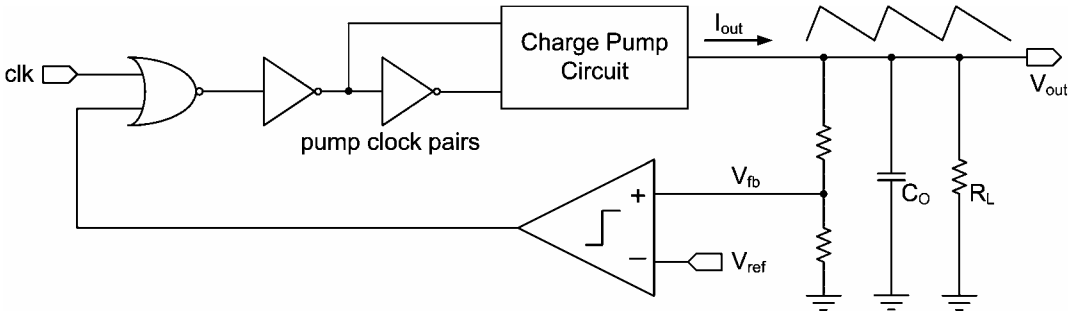


Fig. 5.1 Conceptual schematic of a conventional charge pump regulator.

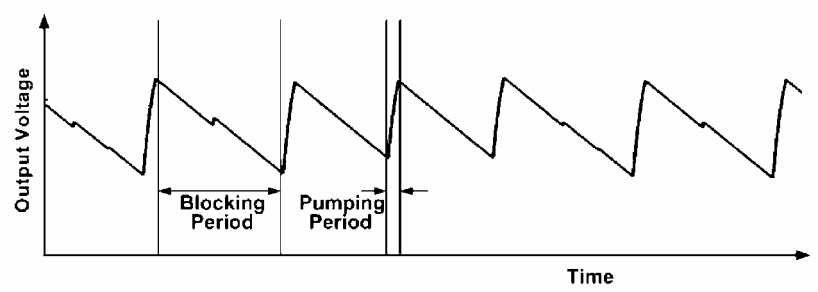


Fig. 5.2 Operation of a regulated charge pump.

Another structure referred to automatic pumping frequency control scheme is exploited to the charge pump regulator for reducing the output ripple [43]-[44]. The block diagram is shown in Fig. 5.3. From this structure, the pump frequency is linearly determined by a voltage-controlled oscillator (VCO). When the output voltage is detected, an error amplifier compares the feedback output voltage (V_{fb}) with the reference voltage (V_{ref}) and linearly converts the error signal to be the control signal of the voltage-controlled oscillator. Thus, the oscillation frequency gets higher as the output voltage level becomes lower. Contrarily, the

frequency gets lower as the output voltage level becomes higher. In this control scheme, the pumping period would be changed automatically for supplying a constant output voltage regardless of load current variations.

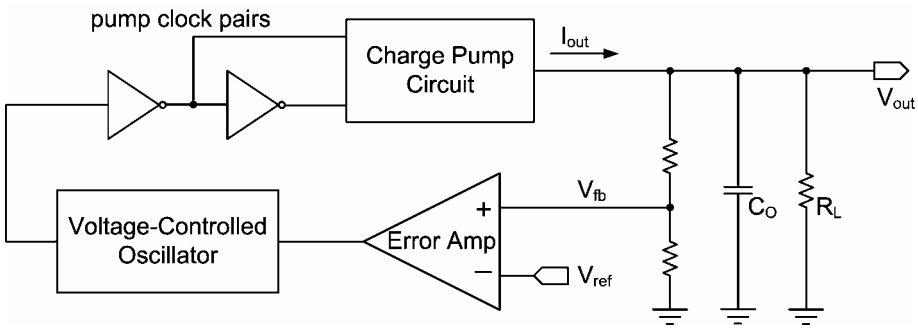


Fig. 5.3 Conceptual schematic of a charge pump regulator using an automatic pumping frequency control scheme.

The automatic pumping frequency control scheme forms a self regulating feedback control that regulated the pump output voltage at the set point. In this control scheme, the most important considerations for the regulator design are the following:

1. The feedback and pump should ramp up sufficiently fast as a system requirement.
2. The fluctuation of pump frequency cannot cause a rate of changing at the output (up or down) faster than the feedback comparator delay.

To achieve these goals, the close-loop function of the regulator must have sufficient phase margin to ensure stability. The proposed averaged model, which can follow the behavior of pumping gain increase circuits, is useful to develop open-loop transfer functions $G(s)$ between the control parameter and the output. Thus, the feedback control and the compensation can be simply added in the system to alter the phase behavior and to improve the margins.

5.3 Design Procedure of Charge Pump Regulator

In this chapter, a design example of the charge pump regulator based on the proposed equivalent model is described. The kernel of the charge pump regulator consists of a voltage-controlled oscillator and a two-stage pumping gain increase circuit as shown in Fig. 5.4. The supply voltage V_{DD} is 1.5 V and V_c and f_s are the input control voltage and the output pump frequency of the voltage-controlled oscillator, respectively. In the example, the regulator utilizes the automatic pumping frequency control scheme to generate an desired output voltage of 3 V at the range of load current from 30 μA to 120 μA [10], [33], [45]. After compensation, the phase margin would exceed 60° which guarantees stable operation.

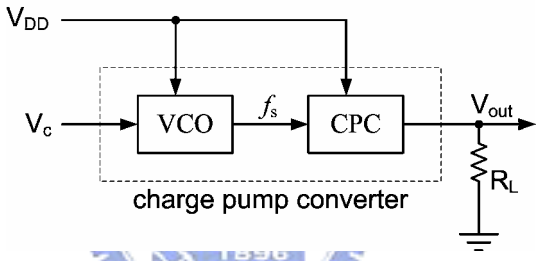


Fig. 5.4 Conceptual block diagram of a charge pump converter.

5.3.1 Analysis of Two-Stage Equivalent Model

Based on the analysis mentioned in chapter 4, the equivalent model of a two-stage pumping gain increase circuit is given in Fig. 5.5. The standard load resistance R_L is selected to 50 kΩ for a load current of 60 μA. Considering chip size and therefore cost, the value of each pump capacitor is limited to 100 pF where the die size of the capacitor is 0.225 mm^2 in a TSMC 0.35 μm mixed mode process. From (4.57), the best choice of the ratio of C_1 and C_2 is $K = 1$, so that $C_1 = C_2 = 100$ pF. In this case, from (4.58), a theoretical center pump frequency f_c can be set to 800 kHz. In addition, the output capacitance C_O is selected to 375 pF for the output ripple of 0.2 V from (4.49). Table 5.1 summarizes the design parameters of this two-stage pumping gain increase circuit.

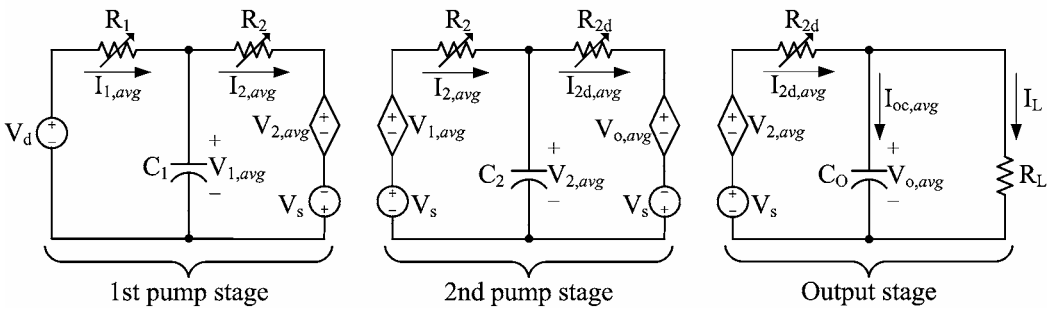


Fig. 5.5 Two-stage equivalent model.

Table 5.1 Parameters used in the design example.

Parameter	Value
Pump Stage Number (N)	2
Supply Voltage (V_d)	1.5 V
Pump Clock Voltage (V_s)	1.5 V
Center Pump Frequency (f_c)	800 kHz
Resistive Load (R_L)	50 kΩ
Output Voltage (V_{out})	3.0 V
Load Current (I_L)	60 μA
Output Ripple (ΔV_o)	0.2 V
Output Capacitance (C_O)	375 pF
Pump Capacitor (C_1)	100 pF
Pump Capacitor (C_2)	100 pF

By using these design parameters, the equivalent resistance of each pump stage is obtained as

$$R_1 \equiv \frac{T_s}{2C_1} = \frac{1}{2f_sC_1} \tag{5.1}$$

$$R_2 \equiv \frac{T_s}{2C_1C_2/(C_1+C_2)} = \frac{C_1+C_2}{2f_sC_1C_2} \tag{5.2}$$

$$R_{2d} \equiv \frac{T_s}{2C_2} = \frac{1}{2f_sC_2} \tag{5.3}$$

When the pumping gain increase circuit achieves the steady state, capacitors can be considered open and the output voltage is obtained by scaling down the source voltage ($V_d + 2V_s$) by the voltage divider of the equivalent resistance as shown in Fig. 5.6.

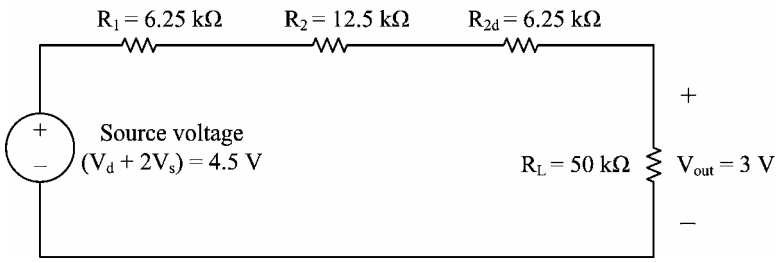


Fig. 5.6 Steady state equivalent circuit.

From (5.1) to (5.3), it can be seen that the resistance is inversely proportional to the pump frequency f_s. By decreasing pump frequency, all of the equivalent resistance would be enlarged so that the output voltage decreases. To the contrary, the output voltage increases. Fig. 5.7 shows the dependence of the output voltage on the pump frequency under different resistive loads. To keep the desired output voltage of 3 V, the pump frequency has to be increased to 1.6 MHz in the condition of R_L = 25 kΩ and decreased to 400 kHz in the condition of R_L = 100 kΩ. Therefore, variations of the pump clock frequency from the voltage-controlled oscillator must be larger than the range of 400 kHz to 1.6 MHz, which guarantees an output voltage of 3 V at variable resistive load of 25 kΩ to 100 kΩ.

In Fig. 5.7, the output voltage has nonlinear oscillator frequency dependence especially at a resistive load of 100 kΩ. Obviously, increment or decrement of the output voltage resulted from the frequency fluctuation around a low central frequency would be larger than that around a high central frequency. The dependence of the output voltage variation on the specific central frequency under different resistive loads is summarized in Fig. 5.8 and Table 5.2. This output voltage variation also can be considered as a circuit gain at a specific central frequency. In the standard case of R_L = 50 kΩ and f_c = 800 kHz, it can be seen that the mean variance of the output voltage (ΔV_f) is about ± 0.13 V when the frequency fluctuation (Δf) is ± 100 kHz. Although a lower central frequency has a better regulating ability, it results in a larger output ripple and longer response time. In the example case, f_c is set to 800 kHz, which

is a trade-off setting according to loading conditions and the characteristics of the pumping gain increase circuit. In addition, the setting of the central frequency is a decisive factor for designing the linear operating range of the voltage-controlled oscillator.

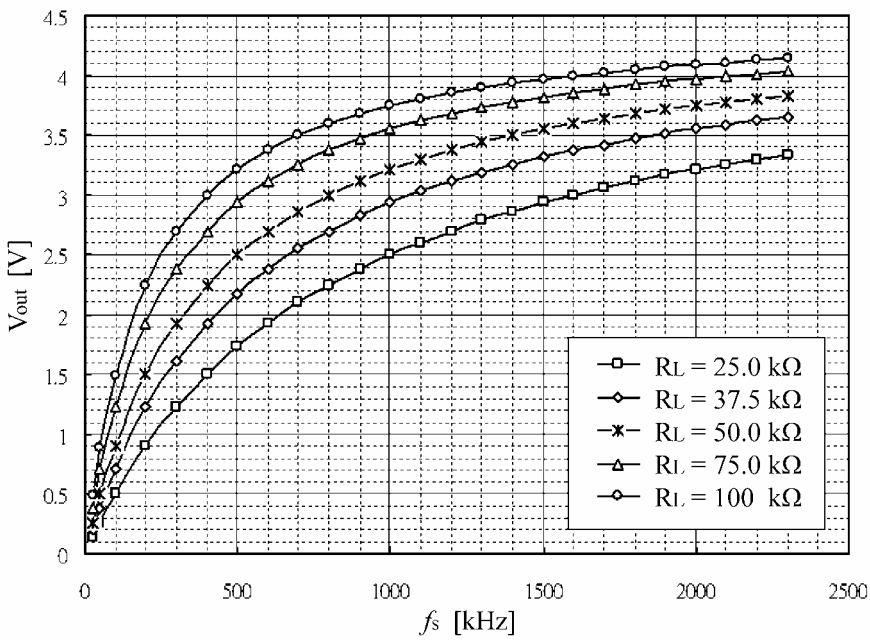


Fig. 5.7 Dependence of the output voltage (V_{out}) on the pump clock frequency (f_s) under different resistive loads.

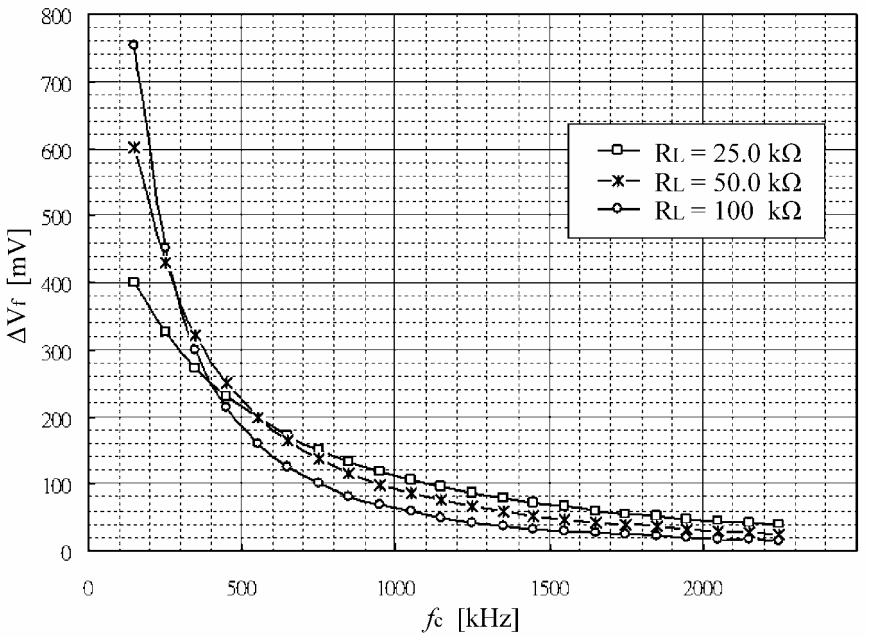


Fig. 5.8 Dependence of the regulating ability on the central frequency (f_c) under different resistive loads, where the mean variance of the output voltage (ΔV_f) is resulted from the frequency fluctuation (Δf = 100 kHz) around a specific central frequency.

Table 5.2 Performance summary of the equivalent model.

V_{out} = 3 V					
Resistive Load (R_L)	25 kΩ	37.5 kΩ	50 kΩ	75 kΩ	100 kΩ
Load Current (I_L)	120 μA	80 μA	60 μA	40 μA	30 μA
Central Frequency (f_c)	1.6 MHz	1.067 MHz	800 kHz	533.3 kHz	400 kHz
Mean Output Variance (ΔV_f) (Frequency Fluctuation: 100 kHz)	63 mV	102 mV	126 mV	210 mV	257 mV

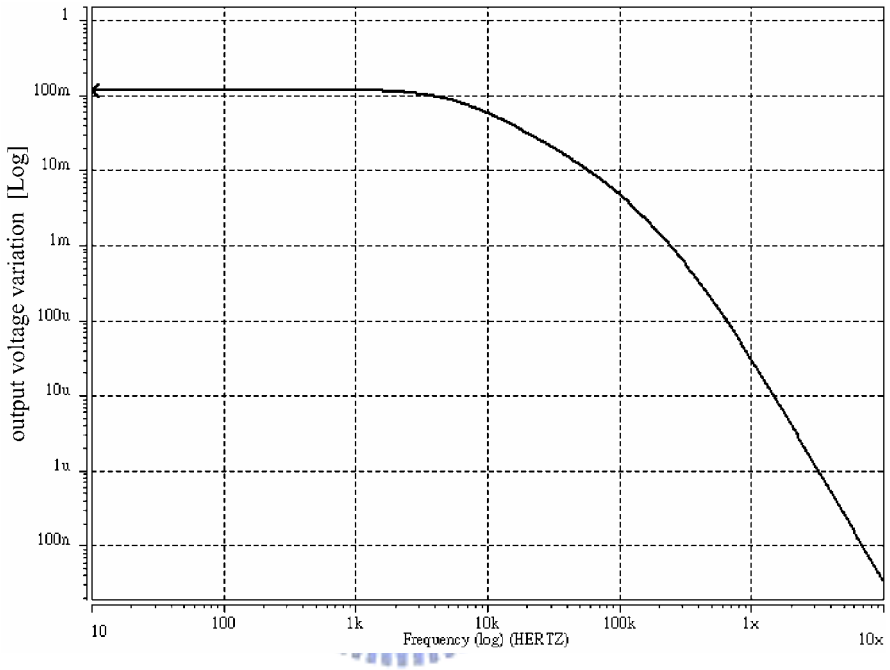


Fig. 5.9 Magnitude response of the equivalent model, where R_L = 50 kΩ, C_O = 375 pF, f_c = 800 kHz, and the magnitude fluctuation of the input small signal Δf = 100 kHz.

From the AC small-signal simulation, the magnitude response of the equivalent model is obtained as shown in Fig. 5.9, where R_L = 50 kΩ, C_O = 375 pF, f_c = 800 kHz, and the magnitude fluctuation of the input small signal Δf = 100 kHz. It can be thought that f_c is analogous to the input DC operating point of the normal small-signal analysis, and Δf is analogous to the magnitude of the AC source. Thus, the AC small-signal frequency indicates the variation speed of the equivalent resistor which results in the output voltage undulation. In this case, the simulation result reveals the magnitude response which is about 125 mV in the low-frequency fluctuation, and the dominant pole frequency of the pumping gain increase

circuit referred to $\omega_{p(cpc)}$ is about 6 kHz. It is apparent that this dominant pole is primarily influenced by the output node with R_L and C_O. Furthermore, the other circuits' poles should be designed to have at least a decade higher frequency than $\omega_{p(cpc)}$ in order to avoid interacting on each other in the regulator system.

5.3.2 Analysis of Voltage-Controlled Oscillator

The voltage-controlled oscillator is used to provide clock signal at the certain frequency for the charge pump. From the discussion on the section 5.3.1, the design considerations of the voltage-controlled oscillator are the following: the operating frequency requires exceeding the range of 400 kHz to 1.6 MHz, and the center frequency requires setting to 800 kHz.

The kernel of the voltage-controlled oscillator used in this work is a source coupled multivibrator, which represents the CMOS version of a well-known bipolar emitter-coupled multivibrator [46], [50]. This circuit topology has been widely used in applications involving waveform generation, such as voltage-controlled oscillators for phase-locked loops (PLLs), because of the low count of active components. The conceptual representation of the basic operation is shown in Fig. 5.10(a) and (b) [47]-[49]. Assume the currents I_1 and I_2 are equal to I_D, and the circuit is already at one of its two stable states, for which transistor M1 is ON. As a consequence, the voltage at node X is fixed as

$$V_X = V_{DD} - R_1\left(I_1 + I_2\right) = V_{DD} - R_1\left(2I_D\right) \tag{5.4}$$

Complementary, transistor M2 is OFF, and current I_2 directly discharging the timing capacitor C_{time} decreases Y node voltage. Therefore, M2 will maintain its OFF state until voltage V_{gs2} is large enough for conduction. As a result, the gate of transistor M1, which was initially at V_{DD} due to the lack of current flowing through R_2, changes to a lower voltage given as

$$V_{g,M1} = V_{DD} - R_2\left(I_1 + I_2\right) = V_{DD} - R_2\left(2I_D\right) \tag{5.5}$$

which toggles its state. As a consequence M1 turns off and the process repeats again. Note

that the effect of asymmetrical current I_1 and I_2 results in different slopes of capacitor voltage charge, therefore providing a duty cycle different from 50%.

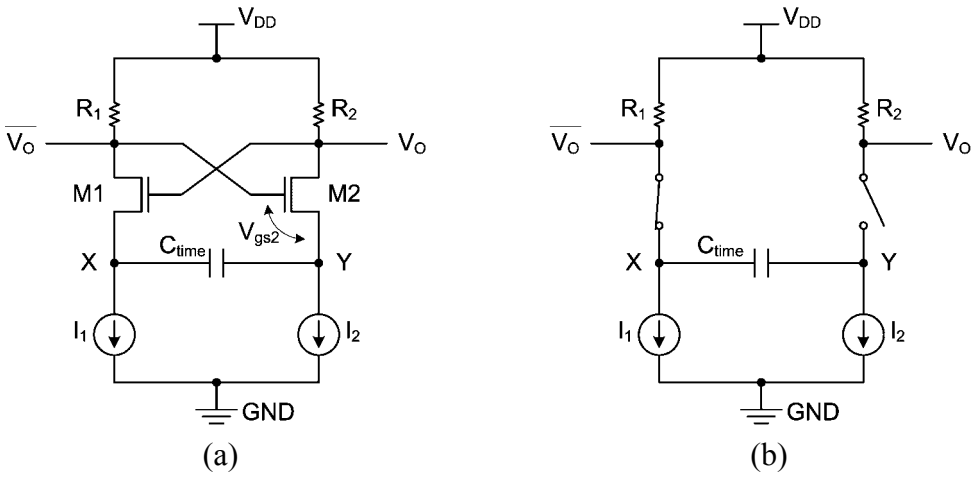


Fig. 5.10 Conceptual representation of the basic source coupled multivibrator operation.

Fig. 5.11(a) shows a schematic of a source coupled multivibrator, and the simplified schematic shown in Fig. 5.11(b) is helpful in illustrating the oscillator operation and determining the oscillator frequency. Cross-coupled transistors M1 and M2 operate as switches and provide the oscillation feedback. The discharge transistors M5 and M6 behave as two current sources sinking a current I_D. The charging currents for each branch of the oscillator are supplied by M3 and M4, which pull the output to V_{DD}. If M1 is on and M2 is off, the drain of M2 is pulled to V_{DD} by M4 and this is the high voltage level of V_O. Since the gate of M1 is at V_{DD}, the source and drain of M1 are approximately ($V_{DD} - V_{tn,M1}$) and this is the low voltage level of $\overline{V_O}$. In addition, $\overline{V_O}$ referred to the gate voltage of M2 is held at the voltage ($V_{DD} - V_{tn,M1}$) through M1 until M2 turns on and M1 turns off. Initially, at the moment when M1 turns on and M2 turns off, point Y tracing the drain voltage of M2 is V_{DD}. Afterward the current I_D through C_{time} causes point Y to discharge down toward ground. When point Y gets down to ($V_{DD} - V_{tn,M1} - V_{tn,M2}$), M2 turns on and M1 turns off. As a consequence V_O gets down to its low voltage level ($V_{DD} - V_{tn,M2}$) and $\overline{V_O}$ pulls to its high voltage level V_{DD}.

The wave forms at the points X, Y, V_O, and $\overline{V_O}$ are shown in Fig. 5.12 for continuous time operation. Assuming that $V_{tn,M1} = V_{tn,M2} = V_{tn}$, V_O and $\overline{V_O}$ are out of phase with the same voltage swing range from (V_{DD} − V_{tn}) to V_{DD}. Since the oscillator output signals are not yet digital, the oscillator requires a buffer, possibly an inverter or self-biased differential amplifier to restore CMOS logic levels.

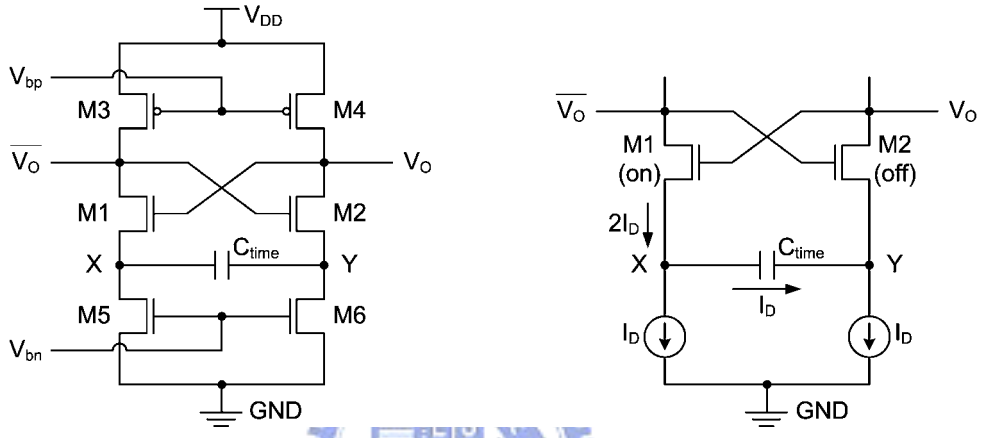


Fig. 5.11 (a) Schematic of a source coupled multivibrator. (b) Simplified schematic of source coupled multivibrator, where M1 is on and M2 is off.

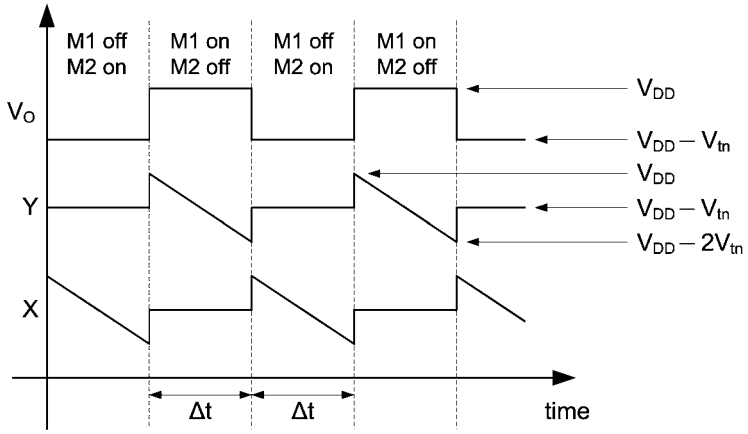


Fig. 5.12 Voltage waveforms of the source coupled multivibrator.

Furthermore, the voltage at point Y changed an amount of ($V_{tn,M1}$ + $V_{tn,M2}$) before switching took place. The time takes point Y to change ($V_{tn,M1}$ + $V_{tn,M2}$) is given by

$$\Delta t = \frac{\left(V_{\text{tn,M1}} + V_{\text{tn,M2}}\right) C_{\text{time}}}{I_{\text{D}}} \tag{5.6}$$

Since the circuit is symmetrical, two of these discharging times are needed for each cycle of the oscillator. When $V_{\text{tn,M1}} = V_{\text{tn,M2}} = V_{\text{tn}}$, the frequency of oscillation is given as

$$f_s = \frac{1}{2\Delta t} = \frac{I_{\text{D}}}{4 C_{\text{time}} V_{\text{tn}}} \tag{5.7}$$

Briefly, the oscillation frequency of the source coupled multivibrator is proportional to the value of the charging current and inversely proportional to the value of the floating timing capacitor C_{time}. In other words, the oscillation frequency is determined by the charging and discharging slopes of C_{time}. Referring to Fig. 5.11, the total current supplied to the oscillator is $2I_{\text{D}}$, but only one-half of the total current contributes to the charging current of C_{time}. The rest current does not affect the operating speed and thus it becomes a waste in terms of the power consumption. However, its current operation scheme provides a broad frequency control range.

The direct implementation of the previous voltage-controlled oscillator at transistor level is depicted in Fig. 5.13. The whole circuit is realized by three functional blocks: the main source coupled multivibrator determining the oscillation frequency, the input bias circuit supporting a control bias voltage to change the charging current of C_{time}, and the output buffer providing the logic operation with a large driving ability. Fig. 5.14 shows the simulation results of the output frequency with different input control voltage V_{c}, where C_{time} = 3 pF and V_{DD} = 1.5 V. The operating frequency range is observed from 60 kHz to 4.2 MHz, which is larger than the required range specified in section 5.3.1 (400 kHz to 1.6 MHz). The center frequency is obtained at 800 kHz while V_{c} is 1.0 V. A limited adjustable range of V_{c} is observed from 0.6 V to 1.5 V because a small supply voltage V_{DD} is used.

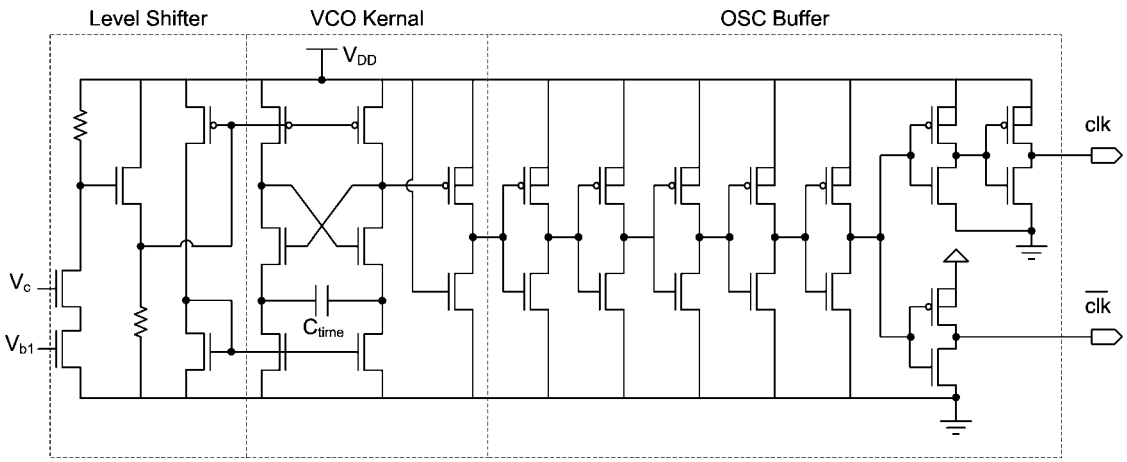


Fig. 5.13 Overall schematic of the voltage-controlled oscillator circuit.

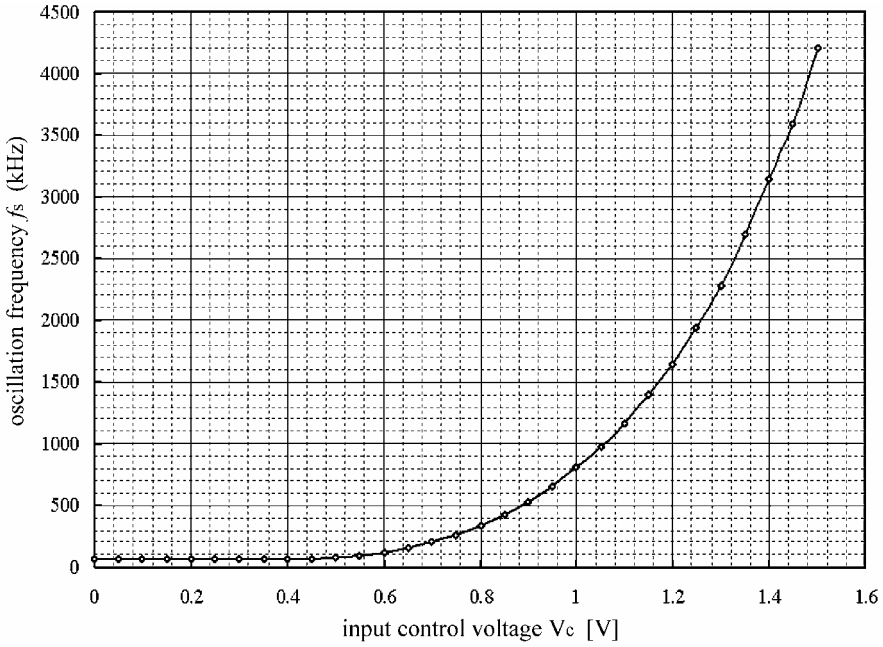


Fig. 5.14 Oscillation frequency (f_s) versus input control voltage (V_c).

5.3.3 Analysis of a Modeling Charge Pump Converter

As shown in Fig. 5.5, the input pump clock signals of the equivalent model are separated into the clock magnitude (V_s) and the clock frequency (f_s) which determines the equivalent resistance of each pump stage. Therefore, for combining the voltage-controlled oscillator with the equivalent model as a charge pump converter shown in Fig. 5.4, the characteristic between the oscillation frequency (f_s) and the input control voltage (V_c) must be formularized.

Using a piecewise linear function in SPICE simulation, the characteristic of the voltage-controlled oscillator illustrated in Fig. 5.14 can be converted to a function as

$$f_s = f_c + \Delta f = f\left(V_c + v_c\right) \tag{5.8}$$

where f_s is the output pump clock frequency, f_c is the center frequency under an input DC operating voltage V_c = 1V, and Δf is the fluctuation frequency in response to a small signal variation v_c. By connecting this SPICE function with the equivalent model, the relationship between the input V_c and the output V_{out} of the charge pump converter with different output resistive load can be obtained as shown in Fig. 5.15. Without the control feedback loop, the output voltage is decided by a fixed input control voltage V_c and an assigned resistive load R_L.

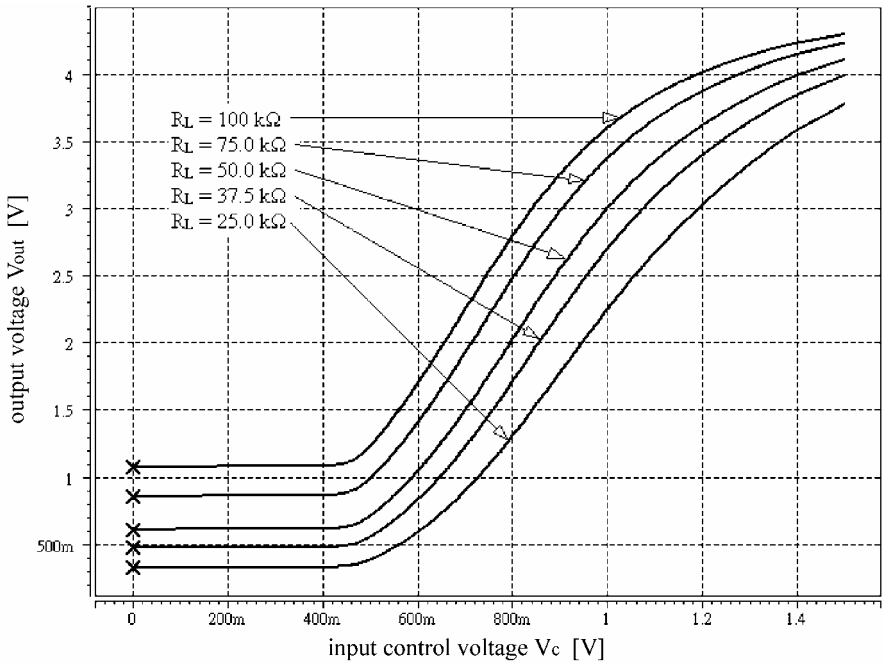


Fig. 5.15 Output voltage V_{out} versus input control voltage V_c, where $V_{DD} = V_s$ = 1.5 V, and C_O = 375 pF.

Fig. 5.16 shows the dependence of the mean variance of the output voltage (ΔV_f) on the input operating voltage (V_c) and the resistive load R_L under the condition of v_c = 50 mV. In the case of R_L = 50 kΩ, ΔV_f is about 215 mV while V_c = 1 V and v_c = 50 mV. From Fig. 5.14, it can be seen that when R_L = 50 kΩ, V_c = 1 V, and v_c = 50 mV, the frequency fluctuation (Δf) is

about 200 kHz. Thus, the result accords with the conclusions in Fig. 5.8 and Table 5.2, which represent ΔV_f is about 0.126 V as Δf = 100 kHz. Furthermore, from Fig. 5.16, it can be predicted that the assignment of the input operating voltage (V_c) affects the small-signal gain of the charge pump converter. The highest gain would occur at V_c = 0.7 – 0.9 V under different resistive loads, but a higher gain might result in a worse phase margin in the whole close-loop system.

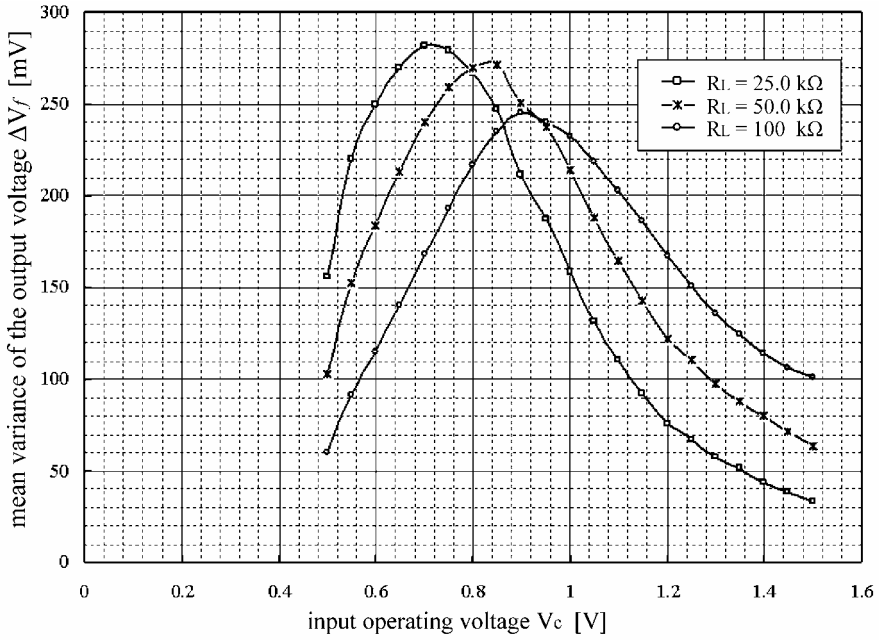


Fig. 5.16 Dependence of the mean variance of the output voltage (ΔV_f) on the input operating voltage (V_c), where v_c = 50 mV.

By using the standard design parameters summarized in Table 5.1, the frequency response of the modeling charge pump converter is shown in Fig. 5.17, where V_c = 1 V and R_L = 50 kΩ. The simulation results reveal the low-frequency gain is about 11.5 dB (3.8×), and the dominant pole frequency of this modeling converter referred to $\omega_{p(mc)}$ is about 6 kHz. The performance characteristics of this modeling converter under different resistive loads are summarized in Table 5.3.

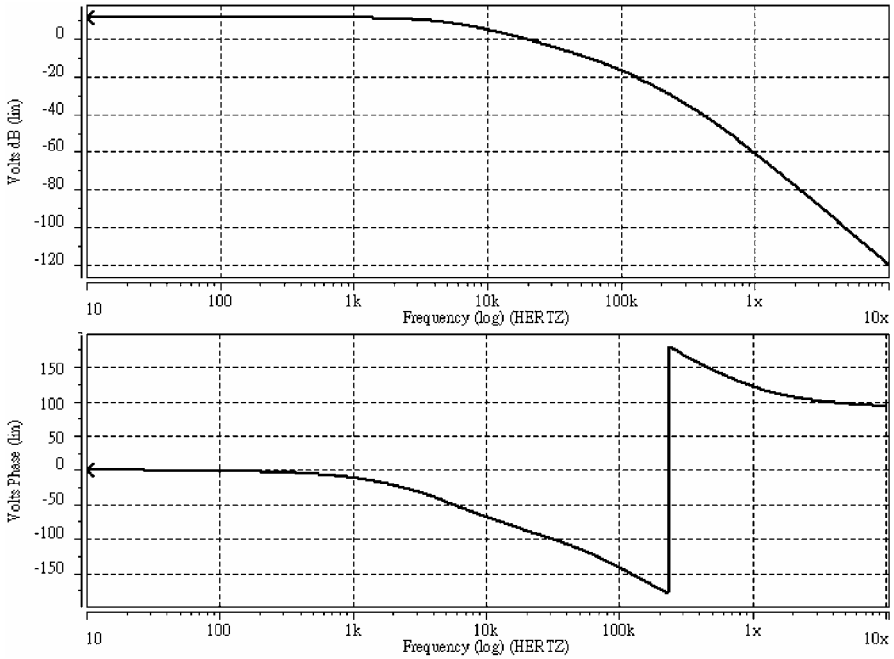


Fig. 5.17 Bode plot of the modeling converter, where V_c = 1 V and R_L = 50 kΩ.

Table 5.3 Performance summary of the charge pump converter.

R_L	25 kΩ	37.5 kΩ	50 kΩ	75 kΩ	100 kΩ
Low Frequency Gain	12.8 dB (4.36×)	12.26 dB (4.1×)	11.5 dB (3.75×)	9.84 dB (3.1×)	8.36 dB (2.62×)
Bandwidth	10.4 kHz	7.1 kHz	5.38 kHz	3.62 kHz	2.73 kHz
Unit Gain Frequency	41.53 kHz	27.47 kHz	19.2 kHz	10.62 kHz	6.6 kHz
Dominant Pole Frequency $\omega_{p(mc)}$	10.54 kHz	7.15 kHz	5.41 kHz	3.63 kHz	2.74 kHz

5.3.4 Charge Pump Regulator for Open-Loop Test

To establish a simple charge pump regulator, an automatic pumping frequency control scheme shown in Fig. 5.3 is adopted. In this feedback loop, the difference between a divided output voltage and a reference voltage is detected and amplified by an error amplifier for adjusting the pump clock frequency of the voltage-controlled oscillator, and then the output voltage would be regulated. When the divided output voltage is below the reference value, the pump clock frequency gets higher for increasing the output voltage. On the contrary, the pump clock frequency gets lower for decreasing the output voltage.

In the presented design example, the performance of a basic two-stage MOS operational amplifier is adequate to be adopted as the error amplifier [50]-[52]. Table 5.4 shows the characteristics of the designed two-stage MOS amplifier. By using a negative feedback on the designed two-stage operational amplifier to obtain an accurate close-loop gain of 29.5 dB (30×) and to extend the bandwidth to 1 MHz, the dominant pole frequency of the error amplifier would be high enough to avoid interacting on the converter's dominant pole, which is about 2.7 kHz – 10.5 kHz shown in Table 5.3, and the bandwidth would be sufficiently large for the pumping gain increase circuit operation. Fig. 5.18 shows the frequency response of the designed error amplifier.

Table 5.4 Characteristics of the designed two-stage MOS operational amplifier.

Supply Voltage	1.5 V
Open-Loop Gain	46 dB
Phase Margin	77°
Bandwidth	100 kHz
Unit-Gain Frequency	30 MHz
Slew Rate (R_L = 1 kΩ, C_L = 20 pF)	1.2 V/μs
Output Swing	1 mV – 1.5 V
CMRR	60 dB
PSRR	60 dB

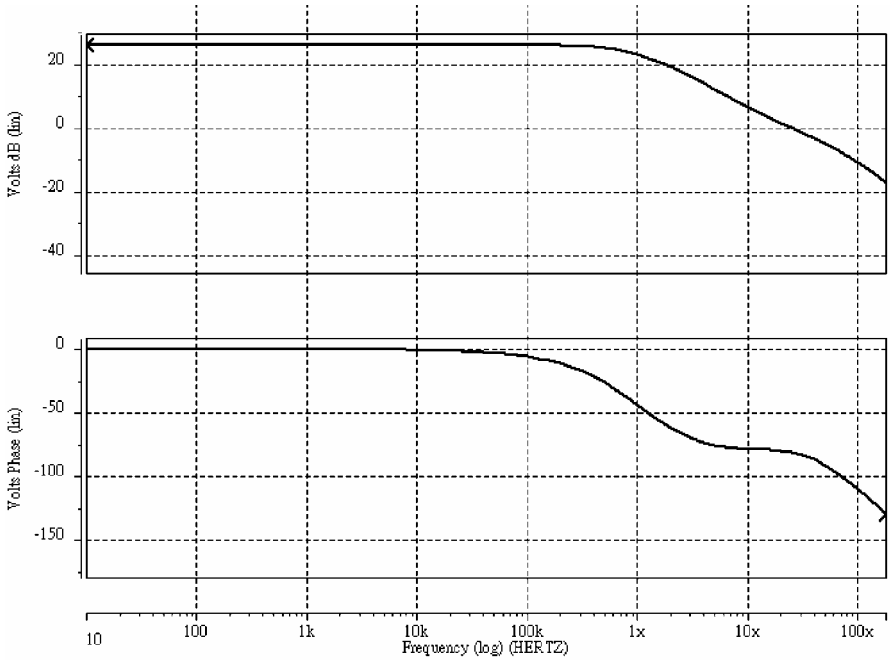


Fig. 5.18 Bode plot of the designed error amplifier with a low supply voltage V_{DD} = 1.5 V.

Before trying to design a close-loop control of the charge pump regulator as shown in Fig. 5.3, it would be helpful to analyze the open-loop behavior. Fig. 5.19 shows the open-loop test of the regulator example, where the feedback degeneration resulted from a resistive voltage divider (R_1 and R_2). From this figure, tests of the input-output behavior by imposing a small-signal (v_{ac}) in the source voltage (V_b) with different resistive load will be performed. Results of these tests are illustrated in Table 5.5.

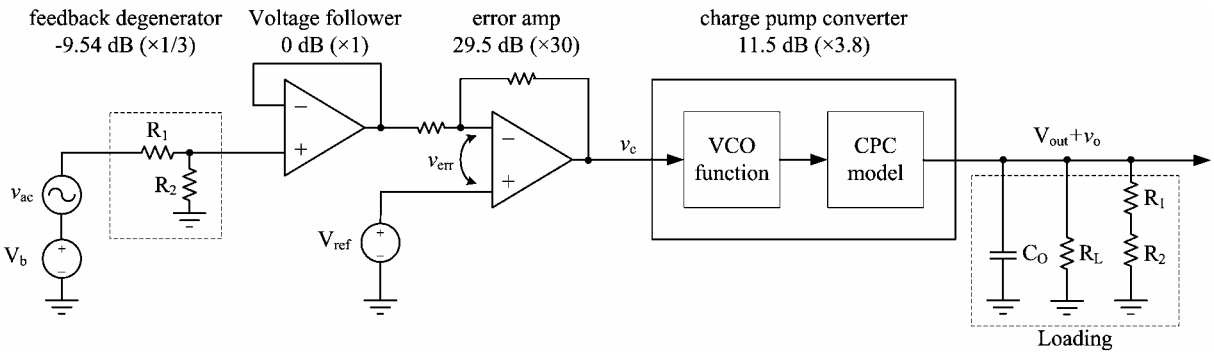


Fig. 5.19 Charge pump regulator for open-loop test.

Table. 5.5 Results of the open-loop tests, where $C_1 = C_2 = 100$ pF, $C_O = 375$ pF.

resistive load R_L	reference voltage V_{ref}	bandwidth BW	unit-gain frequency UGF	open-loop gain $A_o = v_o / v_{ac}$	dominant pole $\omega_{p(open)}$
25 kΩ	1.1 V	10.57 kHz	186.3 kHz	31.6134 dB	10.71 kHz
	1.0 V	10.57 kHz	194.1 kHz	32.3006 dB	
	0.9 V	10.57 kHz	201.7 kHz	32.9879 dB	
	0.8 V	10.57 kHz	192.5 kHz	32.2794 dB	
	0.7 V	10.57 kHz	165.8 kHz	30.0865 dB	
	0.6 V	10.54 kHz	109.1 kHz	24.8199 dB	
37.5 kΩ	1.1 V	7.27 kHz	142.5 kHz	30.7000 dB	7.32 kHz
	1.0 V	7.27 kHz	152.0 kHz	31.7012 dB	
	0.9 V	7.27 kHz	169.9 kHz	33.4893 dB	
	0.8 V	7.27 kHz	169.7 kHz	33.5484 dB	
	0.7 V	7.27 kHz	151.9 kHz	32.0272 dB	
	0.6 V	7.26 kHz	104.2 kHz	27.4494 dB	
50 kΩ	1.1 V	5.554 kHz	112.4 kHz	29.6425 dB	5.58 kHz
	1.0 V	5.554 kHz	122.4 kHz	30.8505 dB	
	0.9 V	5.554 kHz	145.3 kHz	33.4116 dB	
	0.8 V	5.554 kHz	150.8 kHz	34.0469 dB	
	0.7 V	5.553 kHz	139.5 kHz	33.0717 dB	
	0.6 V	5.548 kHz	99.32 kHz	29.0857 dB	
75 kΩ	1.1 V	3.799 kHz	74.27 kHz	27.6680 dB	3.81 kHz
	1.0 V	3.799 kHz	83.44 kHz	29.0717 dB	
	0.9 V	3.799 kHz	109.6 kHz	32.6364 dB	
	0.8 V	3.799 kHz	121.2 kHz	34.0906 dB	
	0.7 V	3.799 kHz	118.8 kHz	33.9835 dB	
	0.6 V	3.797 kHz	90.27 kHz	31.0084 dB	
100 kΩ	1.1 V	2.908 kHz	51.69 kHz	25.9767 dB	2.916 kHz
	1.0 V	2.908 kHz	59.38 kHz	27.4589 dB	
	0.9 V	2.908 kHz	85.20 kHz	31.6702 dB	
	0.8 V	2.908 kHz	99.47 kHz	33.6901 dB	
	0.7 V	2.908 kHz	101.9 kHz	34.1432 dB	
	0.6 V	2.907 kHz	82.39 kHz	32.0586 dB	

The data presented in Table 5.5 support a trend about the mean variance of the output voltage, which also implies the loop gain, in Fig. 5.16. Since the worst phase margin generally comes with the highest loop gain, it can be predicted that the worst case of phase margin would occur at R_L = 100 kΩ and V_{ref} = 0.6 V – 0.7 V, which has a maximum open-loop gain. To confirm the stability of all the other cases, the phase margin of this worst condition must exceed 45° through a compensator design in the complete close-loop system. Consequently, instability should never occur.

Besides, from Table 5.5, the dominant pole frequency $\omega_{p(open)}$, which is primarily influenced by the output node with R_L and C_O, increases as the resistive load decreases and is located in the range from 2.9 kHz to 10.7 kHz. Since the other pole frequency is much higher then 10 kHz, the system characteristics are dominated by the output load.

5.3.5 Frequency Compensation of Charge Pump Regulator

Figs. 5.20 and 5.21 show the close-loop charge pump regulator without compensation and its conceptual signal-flow diagram, respectively. Basis for the data of the open-loop tests shown in Table 5.5, characterization of the close-loop system can be performed in a pencil-and-paper manner. In the standard design example of R_L = 50 kΩ and V_{ref} = 1 V, it can be thought that the regulator has a open-loop gain A_o given as

$$A_o = A_1 \times A_2 = 114 \tag{5.9}$$

where A_1 is the converter gain of 3.8 and A_2 is the amplifier gain of 30. The output is fed to the load as well as a feedback network, which produces a divided output voltage. This divided voltage is related to the output voltage by the feedback factor β of 1/3. From the feedback theory, the gain of this feedback regulator can be obtained as

$$A_f = \frac{A_o}{1 + A_o\beta} = \frac{114}{1 + 114 \times \frac{1}{3}} = 2.92 = 9.3 \text{ dB} \tag{5.10}$$

In (5.10), the close-loop gain is almost entirely determined by the feedback network which is

constructed by a resistive voltage divider.

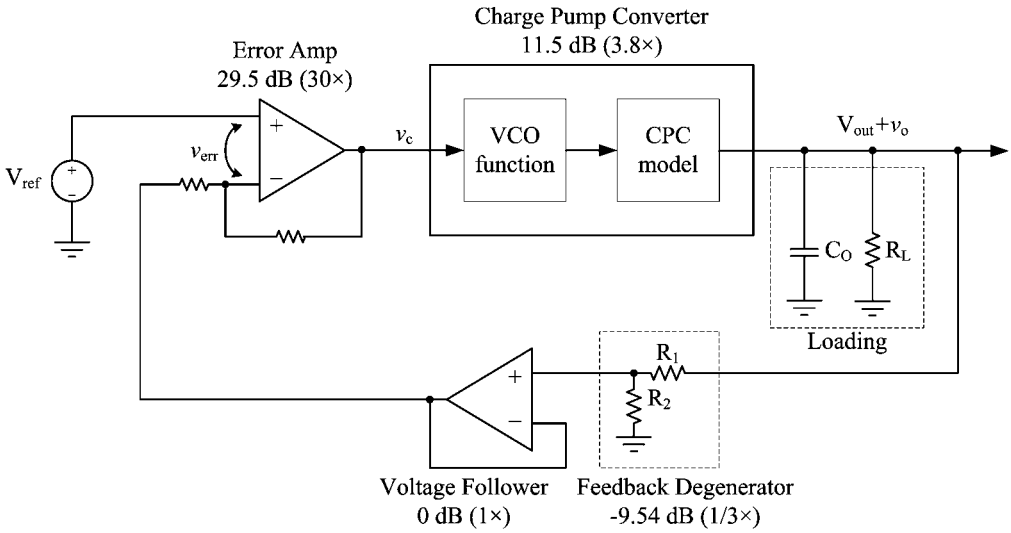


Fig. 5.20 Close-loop charge pump regulator without compensation.

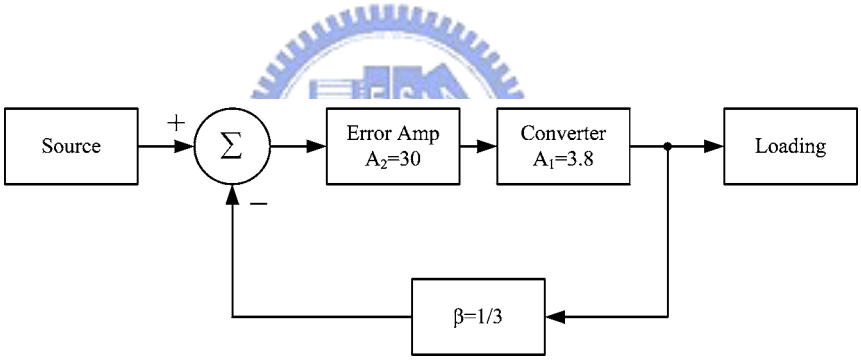


Fig. 5.21 Conceptual signal-flow diagram of the close-loop charge pump regulator without compensation.

Consider the dominant pole frequency of the open-loop system mentioned above, the 3-dB frequency (ω_{pf}) in the close-loop system is increased by a factor equal to the amount of feedback ($1+A_o\beta$) and can be given as

$$\omega_{pf} = \omega_{p(open)} \times (1 + A_o\beta) = 39 \times \omega_{p(open)} \tag{5.11}$$

Thus, the bandwidth of this feedback system under different resistive load is increased and can be predicted to the range from 113 kHz to 417 kHz. Since the lowest pump clock frequency from the voltage-controlled oscillator is about 60 kHz, the extended bandwidth of

this feedback system is too high to regulate the output voltage accurately. In addition, ω_{pf} at high frequency would substantially decline the phase margin.

Furthermore, since ω_{pf} is determined by $\omega_{p(open)}$ and the loop gain $A_o\beta$, the first and the second pole of the close-loop system are brought closer together when $\omega_{p(open)}$ and the open loop gain A_o are increased. A value of $\omega_{p(open)}$ is reached at which the poles become coincident. If $\omega_{p(open)}$ is further increased, the poles become complex conjugate and move along a vertical line in a root-locus diagram. As shown in Fig. 5.22, the uncompensated close-loop response can show a peak as a general case of second-order response. The characteristic equation of a second-order network can be written in the standard form:

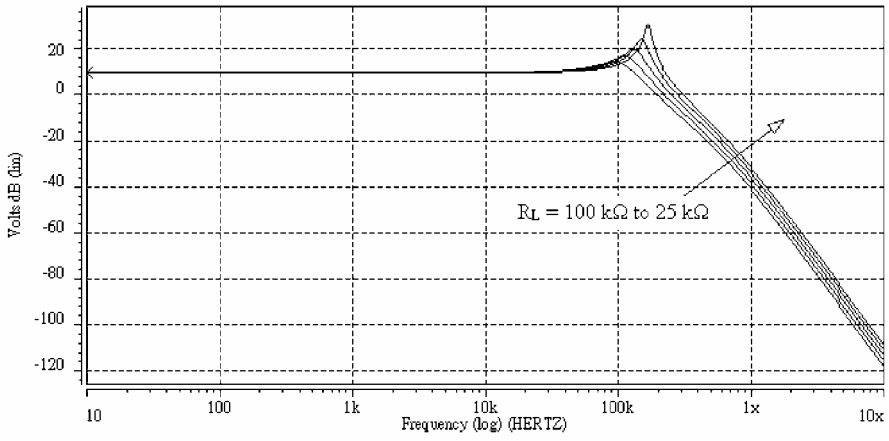
$$s^2 + s\frac{\omega_0}{Q} + \omega_0{}^2 = 0 \tag{5.12}$$

and the Q factor for the poles of the feedback loop is given as

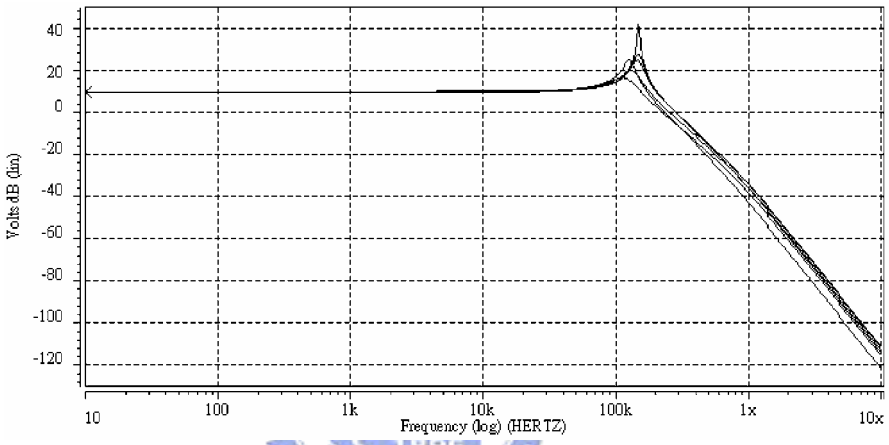
$$Q = \frac{\sqrt{(1 + A_o\beta)\omega_{p1}\omega_{p2}}}{\omega_{p1} + \omega_{p2}} \tag{5.13}$$

From the open-loop data on Table 5.5, the open-loop gain A_o and dominant pole $\omega_{p(open)}$ are increased by decreasing the resistive load R_L as V_{ref} = 1 V. Replacing the data into (5.13), it can be obtained that as R_L is decreased at V_{ref} = 1 V, the Q factor and the response gain peak will become higher as shown in Fig. 5.22(a).

From above discussion, the uncompensated regulator may result in unstable operation and unexpected response gain peaks of the system. To overcome these problems, a compensator is added to the close loop for limiting the bandwidth to about 6 kHz, which is tenfold lower than the lowest pump clock frequency, and increasing the phase margin. From (5.11), a new pole is introduced by the compensator at about 154 Hz to achieve the close-loop bandwidth of 6 kHz. Since this new pole is not distant from $\omega_{p(open)}$, which is at 2.9 kHz to 10.7 kHz according to the resistive load, the phase margin will be further reduced. Thus, a new zero is demanded to cancel this open-loop dominant pole.



(a)



(b)

Fig. 5.22 Magnitude response of the uncompensated regulator: (a) with V_{ref} = 1 V under different resistive load, and (b) with R_L = 50 kΩ under different reference voltage.

As shown in Fig. 5.23, an RC low-pass filter, which is one of the simplest phase-lag controllers, is used to introduce a new pole and a new zero for compensating the charge pump regulator. The transfer function of this RC low-pass filter is given by

$$G_c(s) = \frac{R_{c2}C_c \cdot s + 1}{(R_{c1} + R_{c2})C_c \cdot s + 1} = \frac{R_{c2} + \frac{1}{sC_c}}{R_{c1} + R_{c2} + \frac{1}{sC_c}} \tag{5.14}$$

From (5.14), the zero frequency f_{HZ} and the pole frequency f_{DP} can be obtained as

$$f_{HZ} = \frac{1}{2\pi R_{c2}C_c} \tag{5.15}$$

$$f_{DP} = \frac{1}{2\pi\left(R_{c1} + R_{c2}\right)C_c} \tag{5.16}$$

In the open-loop analysis, the lowest phase margin is anticipated on the conditions of R_L = 100 kΩ and V_{ref} = 0.6 V – 0.7 V. By adjusting the RC values of the compensator, the phase margin of this worst condition is improved to exceed 60° with f_{HZ} = 10 kHz and f_{DP} = 150 Hz. Fig. 5.24 shows the compensated frequency response for R_L = 100 kΩ with different reference voltages. All simulation results are illustrated in Table 5.6. It can be seen that the phase margin of all cases is higher than 60° , which is the worst phase margin in the compensated system. Thus, stability is guaranteed. According to the reference voltage, the close-loop bandwidth is about 4 kHz – 9 kHz, which is moderate in regulation.

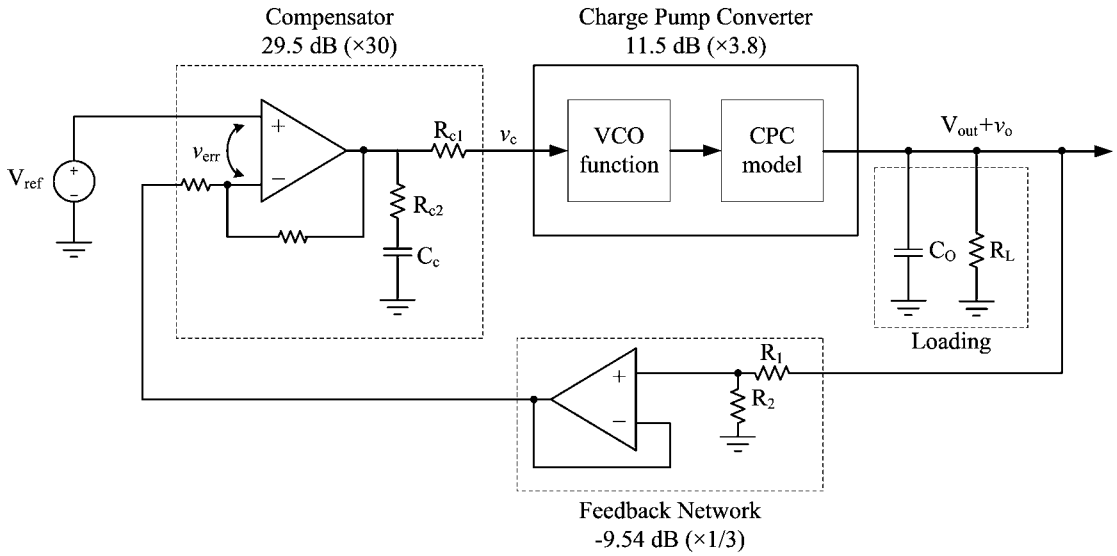


Fig. 5.23 Close-loop charge pump regulator with compensation.

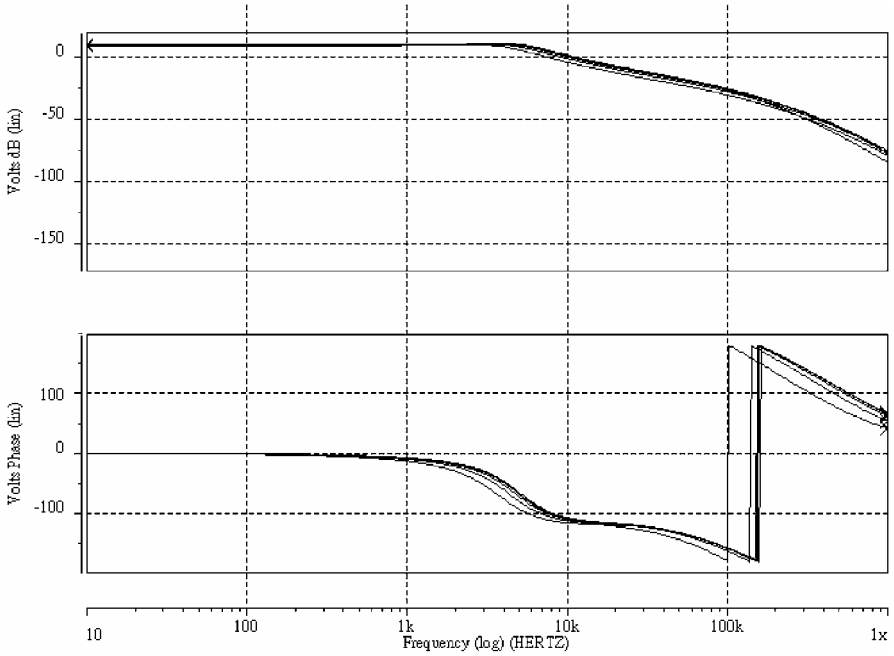


Fig. 5.24 Bode plot of the compensated charge pump regulator for R_L = 100 kΩ with different reference voltages.

Table. 5.6 Results of the compensated close-loop tests.

resistive load R_L	reference voltage V_{ref}	bandwidth BW	unit-gain frequency UGF	close-loop gain A_f	phase margin PM
25 kΩ	1.1 V	4.603 kHz	12.03 kHz	9.4767 dB	97.3431°
	1.0 V	5.590 kHz	14.52 kHz	9.5424 dB	95.3750°
	0.9 V	6.742 kHz	17.43 kHz	9.6090 dB	93.1298°
	0.8 V	7.923 kHz	20.44 kHz	9.6847 dB	90.5837°
	0.7 V	8.545 kHz	22.08 kHz	9.7519 dB	88.2607°
	0.6 V	9.111 kHz	23.44 kHz	9.8508 dB	82.0463°
37.5 kΩ	1.1 V	5.258 kHz	10.97 kHz	9.5040 dB	86.5681°
	1.0 V	6.727 kHz	13.69 kHz	9.5836 dB	84.9926°
	0.9 V	7.453 kHz	15.10 kHz	9.6289 dB	84.2440°
	0.8 V	8.759 kHz	17.73 kHz	9.7072 dB	82.7443°
	0.7 V	8.989 kHz	18.25 kHz	9.7653 dB	81.5444°
	0.6 V	9.553 kHz	19.37 kHz	9.8653 dB	76.6006°
50 kΩ	1.1 V	5.287 kHz	9.711 kHz	9.5062 dB	79.4094°
	1.0 V	6.643 kHz	11.96 kHz	9.5877 dB	78.5024°
	0.9 V	8.001 kHz	14.38 kHz	9.6577 dB	77.9077°
	0.8 V	8.384 kHz	15.12 kHz	9.7101 dB	77.4834°
	0.7 V	8.935 kHz	16.20 kHz	9.7774 dB	76.3979°
	0.6 V	9.048 kHz	16.40 kHz	9.8684 dB	72.5602°
75 kΩ	1.1 V	5.262 kHz	8.496 kHz	9.5292 dB	69.5187°
	1.0 V	6.565 kHz	10.53 kHz	9.6138 dB	69.5043°
	0.9 V	7.011 kHz	11.27 kHz	9.6523 dB	69.5820°
	0.8 V	7.633 kHz	12.34 kHz	9.7170 dB	69.5921°
	0.7 V	7.930 kHz	12.89 kHz	9.7796 dB	68.9982°
	0.6 V	7.890 kHz	12.83 kHz	9.8671 dB	65.9300°
100 kΩ	1.1 V	4.896 kHz	7.466 kHz	9.5313 dB	63.0735°
	1.0 V	5.932 kHz	9.022 kHz	9.6110 dB	63.3800°
	0.9 V	6.541 kHz	9.984 kHz	9.6610 dB	63.7818°
	0.8 V	6.877 kHz	10.54 kHz	9.7168 dB	63.8780°
	0.7 V	7.118 kHz	10.96 kHz	9.7791 dB	63.4803°
	0.6 V	7.000 kHz	10.79 kHz	9.8636 dB	60.7666°

5.4 Time-Domain Simulation Results of Charge Pump Regulator

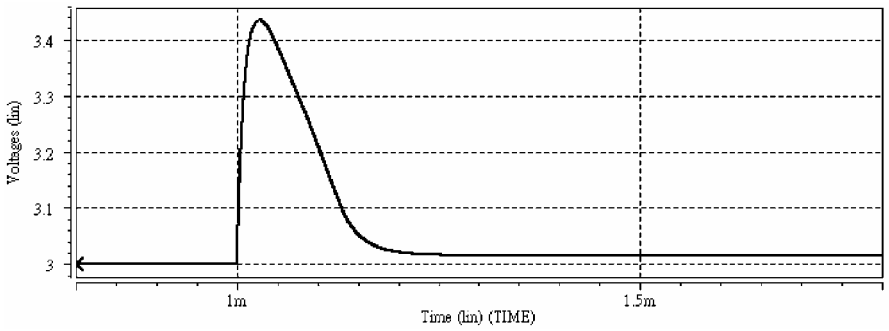
5.4.1 Transient Responses of the Modeling Charge Pump Regulator

In section 5.3, a design example of charge pump regulator based on the proposed equivalent model is presented. The time-domain characteristics of this regulator are represented by the transient and the steady-state responses of the system when certain test signals are applied. Short disturbances or impulse inputs might alter the output temporarily, but the regulator will return to the desired operating point.

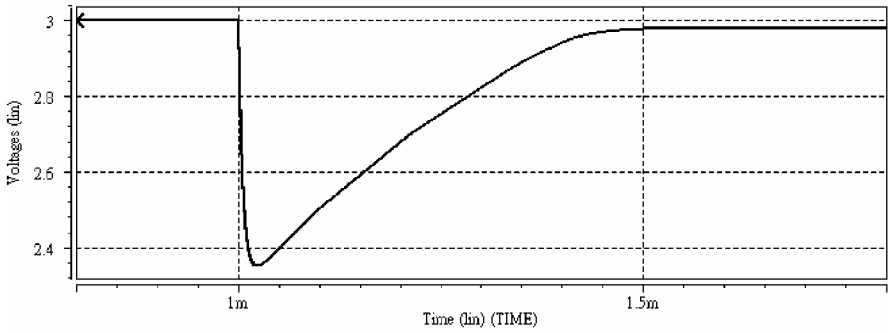
The transient performance of the compensated regulator is characterized by changing the resistive load R_L and the reference voltage V_{ref} as different step inputs. Since V_{ref} is related to the output voltage by the feedback factor β of 1/3, the regulating output voltage should be triple as large as the voltage of V_{ref}. Thus, in the standard case of R_L = 50 kΩ and V_{ref} = 1V, the simulated output voltage is 3.0002 V, which is very close to the ideal value of 3 V. Its percentage of error is about 0.007%, which displays the accuracy of the regulator in the standard case.

Fig. 5.25(a) shows the output waveform when R_L is changed from 50 kΩ to 100 kΩ at a certain moment with V_{ref} = 1V. The final output voltage is 3.0157 V for the error of 0.52%, and the response time is about 0.165 ms. Fig. 5.25(b) shows the output waveform when R_L is changed from 50 kΩ to 25 kΩ with V_{ref} = 1V. The final output voltage is 2.981 V for the error of 0.63%, and the response time is about 0.408 ms. Results of several different tests are illustrated in Table 5.7. It can be obtained that the response time would be extended by increasing the amount of resistive load variation (ΔR_L). In other words, a large response time is caused by a large fluctuation in the pump frequency for achieving the steady-state. It also can be seen that the response time resulted from the condition of decreasing R_L is larger than that of increasing R_L with the same amount of resistive variation. For example, from Table 5.7,

when the resistive load is reduced from 50 kΩ to 25 kΩ at V_{ref} = 1 V, the response time is about 0.408 ms. It is larger than the response time of 0.177 ms, which is reacted by increasing R_L from 25 kΩ to 50 kΩ. In addition, the reference voltage also brings about the change of the transient performance. A higher V_{ref} will cause a rise of the response time.



(a)



(b)

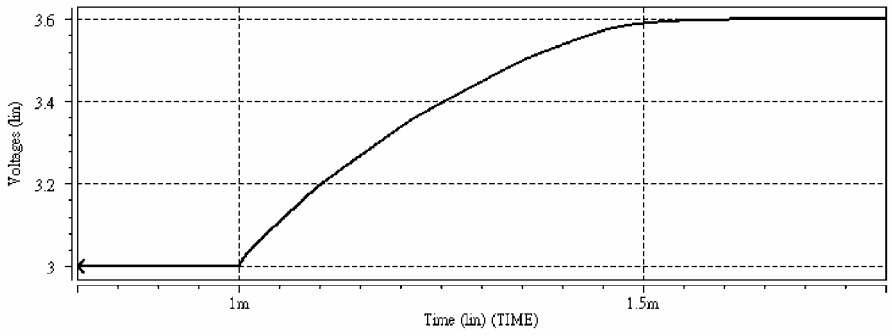
Fig. 5.25 Transient output response of the compensated regulator with a resistive load variation at V_{ref} = 1V. (a) R_L is changed from 50 kΩ to 100 kΩ. (b) R_L is changed from 50 kΩ to 25 kΩ.

Table. 5.7 Results of the resistive load variation tests.

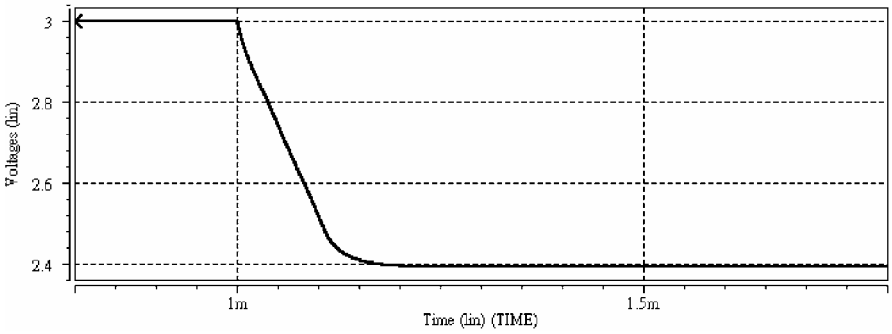
Initial R_L	Final R_L	Response Time at V_{ref} = 0.8 V	Response Time at V_{ref} = 1.0 V	Response Time at V_{ref} = 1.2 V
25 kΩ	50 kΩ	0.161 ms	0.177 ms	0.205 ms
	100 kΩ	0.309 ms	0.305 ms	0.315 ms
50 kΩ	25 kΩ	0.255 ms	0.408 ms	0.663 ms
	100 kΩ	0.164 ms	0.166 ms	0.196 ms
100 kΩ	25 kΩ	0.419 ms	0.589 ms	0.722 ms
	50 kΩ	0.182 ms	0.241 ms	0.409 ms

Furthermore, it is informative to observe the system behavior by changing the reference voltage V_{ref} as a step input. Fig. 5.26 (a) and (b) show the output waveforms corresponding to V_{ref} changed from 1 V to 1.2 V and changed from 1 V to 0.8 V, respectively, at a certain moment with the standard case of R_L = 50 kΩ. The steady state of the regulating output voltage would be very close to $3V_{ref}$ by the feedback factor β of 1/3. From these figures, it can be seen that the output approaches the final value without any oscillations and overshoot. These responses can be considered as overdamped cases of a second-order system, where the damping ratio $\zeta \geq 0.707$.

All various levels shift in the reference voltage with different R_L are tested, and the results are summarized in Table 5.8 and Table 5.9. Table 5.8 illustrates the response information with respect to V_{ref} changed from a fixed voltage of 1 V under different R_L, and Table 5.9 shows the results with respect to V_{ref} changed from different voltage level with the standard R_L of 50 kΩ. It can be seen that a large response time is caused by a large increment or decrement of the reference voltage (ΔV_{ref}). Besides, the response time resulted from the condition of increasing V_{ref} is larger than that of decreasing V_{ref} with the same shifted amount of the reference voltage. For example, when V_{ref} is reduced from 1 V to 0.8 V at R_L = 50 kΩ, the response time is about 0.134 ms. It is smaller than the response time of 0.209 ms, which is reacted by increasing V_{ref} from 0.8 V to 1 V. In addition, a smaller R_L will cause a rise in the response time.



(a)



(b)

Fig. 5.26 Transient output response of the compensated regulator with a reference voltage variation at R_L = 50 kΩ. (a) V_{ref} is changed from 1 V to 1.2 V. (b) V_{ref} is changed from 1 V to 0.8 V.

Table. 5.8 Results of the reference voltage variation tests with respect to V_{ref} centered at 1V with different resistances of R_L.

Initial Condition	ΔV_{ref} (V)	Ideal V_{out} (V)	Final V_{out} (V)	Error (%)	T_{delay} (ms)	T_{rise} or T_{fall} (ms)	Response Time (ms)
R_L = 25kΩ V_{ref} = 1V V_{out} = 2.98V	- 0.2	2.4	2.3756	1.018	0.060	0.114	0.143
	- 0.1	2.7	2.6793	0.766	0.025	0.081	0.110
	+ 0.1	3.3	3.2811	0.572	0.149	0.302	0.354
	+ 0.2	3.6	3.5767	0.649	0.336	0.621	0.745
R_L = 50kΩ V_{ref} = 1V V_{out} = 3.00V	- 0.2	2.4	2.3916	0.351	0.060	0.108	0.134
	- 0.1	2.7	2.6967	0.122	0.027	0.067	0.091
	+ 0.1	3.3	3.3013	0.040	0.074	0.149	0.185
	+ 0.2	3.6	3.5991	0.026	0.172	0.378	0.446
R_L = 100kΩ V_{ref} = 1V V_{out} = 3.02V	- 0.2	2.4	2.4055	0.227	0.070	0.117	0.140
	- 0.1	2.7	2.7111	0.413	0.034	0.063	0.082
	+ 0.1	3.3	3.3184	0.557	0.052	0.097	0.084
	+ 0.2	3.6	3.6189	0.524	0.113	0.221	0.266

Table 5.9 Results of the reference voltage variation tests with respect to V_{ref} changed from different center voltage levels with the standard R_L of 50 kΩ.

Initial Condition	ΔV_{ref} (V)	Ideal V_{out} (V)	Final V_{out} (V)	Error (%)	T_{delay} (ms)	T_{rise} or T_{fall} (ms)	Response Time (ms)
V_{ref} = 0.8V V_{out} = 2.39V	+ 0.1	2.7	2.6968	0.118	0.040	0.083	0.110
	+ 0.2	3.0	3.0005	0.017	0.093	0.177	0.209
	+ 0.3	3.3	3.3015	0.045	0.150	0.312	0.368
	+ 0.4	3.6	3.591	0.250	0.306	0.463	0.619
V_{ref} = 1V V_{out} = 3.00V	- 0.2	2.4	2.3916	0.351	0.060	0.108	0.134
	- 0.1	2.7	2.6967	0.122	0.027	0.067	0.091
	+ 0.1	3.3	3.3013	0.040	0.074	0.149	0.185
	+ 0.2	3.6	3.5991	0.026	0.172	0.378	0.446
V_{ref} = 1.2V V_{out} = 3.60V	- 0.4	2.4	2.3915	0.356	0.160	0.241	0.285
	- 0.3	2.7	2.6966	0.126	0.122	0.190	0.227
	- 0.2	3.0	3.0004	0.015	0.081	0.140	0.176
	- 0.1	3.3	3.3014	0.042	0.037	0.099	0.132

Further analysis of the data in Table 5.7 to 5.9 indicates that the response time might be increased if the operating pump frequency is required to increase for reaching the final steady state. Thus, a large increment of V_{ref} or a large decrement of R_L as a step input requires large time for the response to reach and stay within a range about the final value. From the simulation, the largest response time about 0.864 ms occurs in the condition of V_{ref} changed from 0.8 V to 1.2 V at R_L = 25 kΩ. Based on the design procedure mentioned above, transient-response specifications can be summarized in Table 5.10.

Table 5.10 Transient-response specifications.

Supply Voltage	1.5V
Standard Resistive Load	50kΩ
Standard Reference Voltage	1V
Standard Output Voltage	3.0V
Standard Output Current	60μA
Allowable Variation Range of Resistive Load	25kΩ to 100kΩ
Allowable Shift Level of Reference Voltage	0.8V to 1.2V
Allowable Range of Output Voltage	2.4V to 3.6V
Allowable Range of Output Current	24μA to 144μA
Maximum Response Time	< 0.9ms
Maximum Percentage of Error	< 2%
Start-Up Time	< 2ms

5.4.2 Transient Responses of the Practical Charge Pump Regulator

A simple implementation of the practical compensated charge pump regulator in transistor level is shown in Fig. 5.27. The circuit is simulated in a TSMC mix-mode 0.35 μm CMOS process technology. All design parameters of the practical circuit are in complete accord with those of the modeling design example mentioned above. Table 5.11 shows the simulated average output voltage ($V_{o,avg}$) and the corresponding percentage error of the practical regulator in the steady state with different resistors and different reference voltages. The results of the average output voltage are almost identical as those in the modeling design example, and all percentage errors are less than 2 % when V_{ref} is of 0.8 V to 1.1 V. The output ripple is lower than 0.2 V with this frequency regulation method.

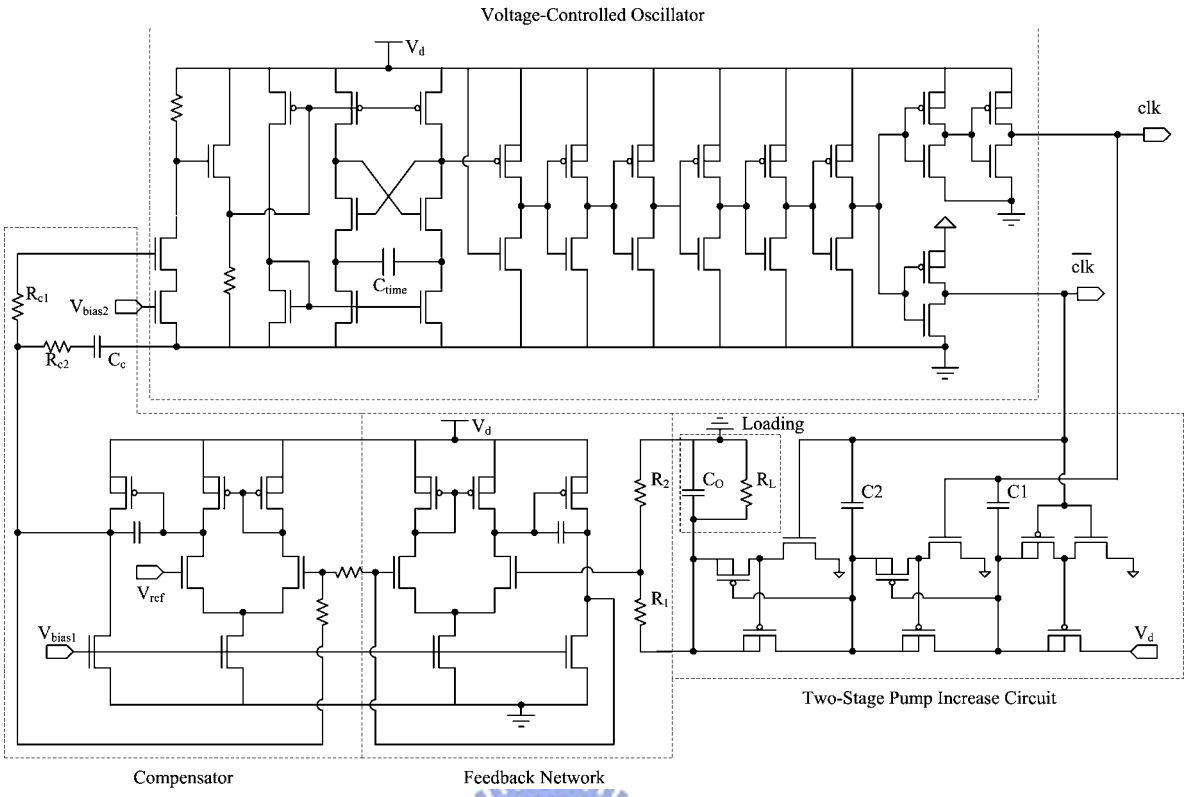
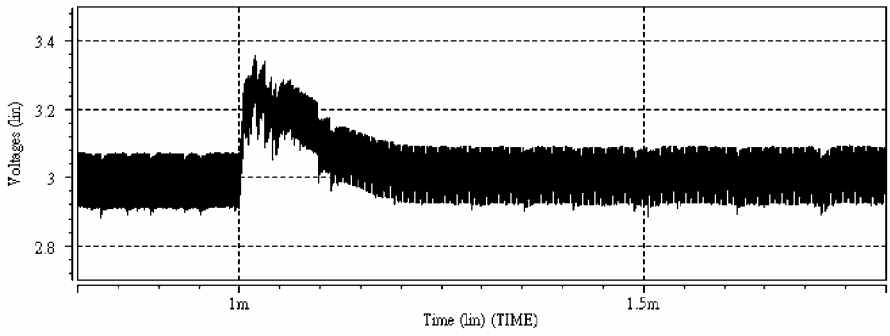


Fig. 5.27 Schematic diagram of a simple compensated charge pump regulator.

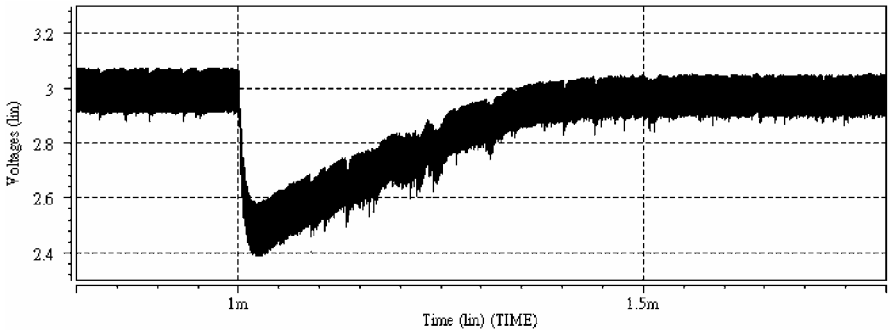
Table 5.11 Simulation results of average output voltage and the corresponding percentage error in the steady state with different resistors and different reference voltages.

Reference Voltage		R_L = 25 kΩ	R_L = 50 kΩ	R_L = 100 kΩ
V_{ref} = 0.8 V	$V_{o,avg}$	2.387 V	2.423 V	2.442 V
	error	0.542 %	0.958 %	1.750 %
V_{ref} = 0.9 V	$V_{o,avg}$	2.676 V	2.711 V	2.736 V
	error	0.889 %	0.407 %	1.333 %
V_{ref} = 1.0 V	$V_{o,avg}$	2.953 V	2.989 V	3.031 V
	error	1.567 %	0.367 %	1.033 %
V_{ref} = 1.1 V	$V_{o,avg}$	3.248 V	3.283 V	3.322 V
	error	1.576 %	0.515 %	0.667 %
V_{ref} = 1.2 V	$V_{o,avg}$	3.489 V	3.527 V	3.563 V
	error	3.08 %	2.028 %	1.028 %

Fig. 5.28(a) and (b) show the output waveforms when R_L is changed instantly from 50 kΩ to 100 kΩ and when R_L is changed instantly from 50 kΩ to 25 kΩ, respectively, with V_{ref} = 1V. The pump clock frequency automatically decreases when the resistive load becomes lighter. Compared with Fig. 5.25, the results obtained agree approximately with those expected. In addition, the effects of changing the reference voltage as a step input are also tested. Fig. 5.29 (a) and (b) show the output waveforms corresponding to V_{ref} changed from 1 V to 1.2 V and changed from 1 V to 0.8 V, respectively, with the standard case of R_L = 50 kΩ. The simulation results agree with those obtained in Fig. 5.26. In fact, other simulation tests of the practical regulator design under different conditions are also made, and the results confirm those of the modeling regulator design described in section 5.4.1. Therefore, the characteristics of this practical regulator design would correspond to the transient-response specifications given in Table 5.10.

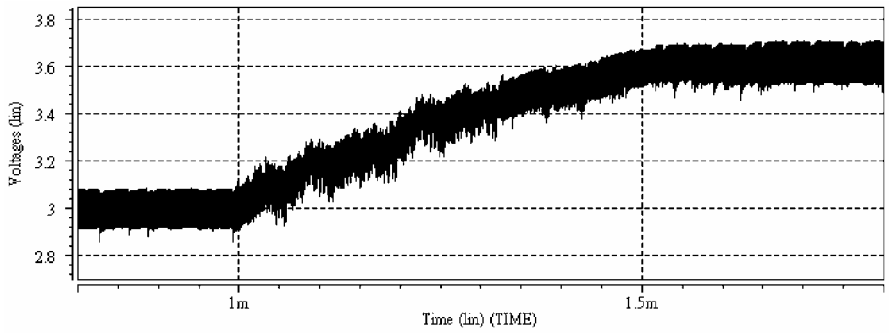


(a)

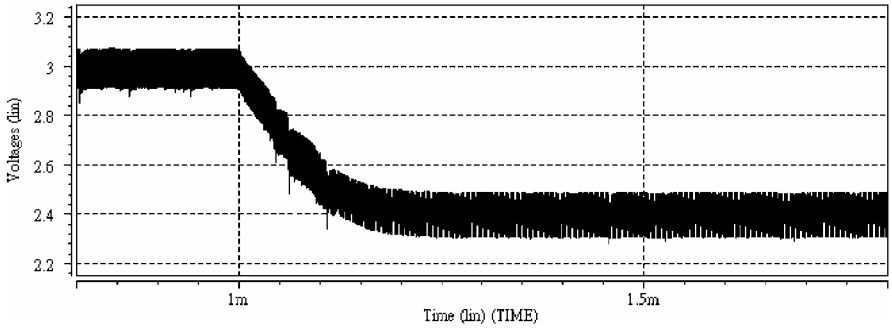


(b)

Fig. 5.28 Transient output response of the practical regulator with a resistive load variation at V_{ref} = 1V. (a) R_L is changed from 50 kΩ to 100 kΩ. (b) R_L is changed from 50 kΩ to 25 kΩ.



(a)



(b)

Fig. 5.29 Transient output response of the practical regulator with a reference voltage variation at R_L = 50 kΩ. (a) V_{ref} is changed from 1 V to 1.2 V. (b) V_{ref} is changed from 1 V to 0.8 V.

5.5 Summary

Based on the presented design procedure, a charge pump regulator with a frequency compensation scheme can be implemented and the characteristics can be designed though manual and/or computer analysis of the equivalent model. This analytical model helps to plan a charge pump regulator and its design tradeoffs. The regulator provides a negative feedback to the pump, insuring that the pump output will be constant, regardless of process, environment and loading conditions. Short disturbances such as resistive load variation or impulse inputs such as reference voltage shift might alter the output voltage temporarily, but the regulator will return to the desired operating point.

From the design example, the proposed design procedure is verified by comparing the simulation results of the practical regulator and analytical data from the modeling design. The

two sets of results are found to be practically identical. Thus, the accuracy of the modeling design has been demonstrated. Performance data are summarized in Table 5.12. It should be noted that the allowable discrepancy in the two sets reflects a slight error in the idealization of the model.

In addition, this charge pump regulator scheme can be built with discrete components, or be integrated on an IC chip. In the first case, a high output voltage and large output power and can be obtained by using power MOSFETs and large discrete capacitors. In the second case, smaller power and output voltage can be delivered by small capacitors operating at higher frequency.

Table 5.12 Performance summary of the regulator example.

	Min.	***Typ.***	***Max.***
Supply Voltage		1.5V	
Resistive Load	25kΩ	50kΩ	100kΩ
Reference Voltage	0.8V	1.0V	1.2V
Output Voltage	2.4V	3.0V	3.6V
Output Current	24μA	60μA	144μA
Output Ripple	0.15V	0.2V	0.25V
Response Time			< 0.9ms
Error Percentage			< 2%
Start-Up Time			< 2ms

Chapter 6

Conclusions and Suggestions

6.1 Conlusions

Nowadays, the perspective is changing. As the power supply scales down, other critical circuits whose performances are strongly dependent on core power supply levels and variations will require a dedicated and stabilized supply voltage, higher or lower than V_{DD}. High voltage generator is therefore one of the key challenges of designers. In this thesis, the discussions are focused on charge pump designs for low voltage applications.

Conventional CPCs have deficiencies such as a large cascade stage number for a high pump output voltage, and the saturated limitation of the output voltage. Thus, the output voltage cannot be maintained as a linear function of the number of stages and the pumping efficiency will be degraded as the number of stages increase further. Several modifications have been presented and discussed in chapter 2.

In chapter 3, in order to overcome above problems, the pumping gain increase circuits are proposed to solve the voltage drop across the MOSFET charge transfer switches in the inner stages and the output stage caused by the threshold voltage increase problem. Thus, the output voltage increases more linearly versus the pumping stage number. From the simulation results, the PGI-3 circuit exhibits the best charge pumping performance among these three different PGI circuits, and the pumping gain of PGI-3 is very close to the ideal value without the saturation problem. The output voltage of PGI-3 can easily exceed 10 V with a 1.5 V supply

when six pumping stages are used.

In addition, an exponential-gain structure with high voltage transfer efficiency is also presented in chapter 3 as a further application of the PGI circuit. It can pump output voltage exponentially in fewer voltage pump stages from a low power supply without output voltage saturated limitation. The simulation results have shown that the exponential-folds pump structure can be applied to produce any structure with n^i architecture, such as that one can use a 3×3 circuit to generate a boosted output above 12V from a 1.5V supply under a 0.35 μm process. A 2×2 CPC is demonstrated using this technique from a 1.5 V supply voltage. It is conceivable that this charge pump styled voltage generator can be well suited to many types of portable equipment that require a high voltage from a low voltage source such as one battery cell.

In chapter 4, analysis and modeling technique of on-chip charge pumps with a resistive load based on pump gain increase circuits have been proposed. The equations of the model, which are useful for a pencil and paper design, also have been deduced for planning the circuit to achieve good enough performance with an acceptable accuracy tolerance in the steady state. Thus, the characteristics of PGI circuits can be approximately predicted and the circuit parameters can be determined in satisfying the requirement. In addition, an optimized design method for PGI circuits with a resistive load is developed in terms of the total number of gain stages in the design and the ratio between pump capacitors.

For 1.5 V supply voltage operation, reliability and accuracy are demonstrated by comparisons between SPICE simulations of the PGI circuit and the result of the equivalent model. The model also has been validated by means of measurements taken from a test chip and all the relative errors of measurements are less than 5 %. Finally, although the derivation of the model was based on PGI circuits, it is shown that the same design strategy can also be applied to any improved charge pump design which is able to eliminate the voltage drop within the inner stages and the output stage as an ideal case.

In chapter 5, the proposed equivalent model can be applied to design a charge pump regulator which is independent of the current drawn by load variations. By using this equivalent model, characterization of regulator can be performed in mathematical analysis with a pencil-and-paper manner. The presented regulator adopts the automatic pumping frequency scheme including a voltage-controlled oscillator, a charge pump circuit, an error detector, and a compensator. This control scheme provides negative feedback to the pump operation, insuring that the pump clock frequency would be changed automatically for generating a desired output voltage regardless of load current variations.

A design example of the charge pump regulator at the range of regulated output voltage from 2.4 V to 3.6 V across different resistive loads is used to illustrate the design procedure based on the equivalent model. In the case of regulator design, simulation can be carried out interactively during each design step to immediately check the consequence of a design decision, and the following procedure could be applied to plan the overall design:

1. Design the circuit parameters of the pumping gain increase circuit to comply with the required specifications through analyzing the model.
2. Design the voltage-controlled oscillator to agree with the required center frequency and the operating range, which can be determined by the information of output voltage variations according with the pump frequency fluctuations under different loading conditions.
3. Combine the voltage-controlled oscillator with the equivalent model to form the un-regulated charge pump converter. Its low-frequency gain and the dominant pole can be obtained by the AC small-signal simulation. This information is useful for characterization of the open-loop and close-loop system though manual and/or computer analysis.
4. Design the feedback loop of the converter to meet the static and dynamic requirements. To ensure stability of the regulator, it is necessary to introduce the compensator design. Check the compatibility of the chosen compensator to the regulator by frequency

response simulations.

5. If closed loop instability is expected, damp the feedback or redesign the compensator to meet the basic stability criteria.
6. Check the transient response to meet specifications. If the regulator does not meet specifications, repeat step (5) or trim the loop gain to improve performance.

From the design example, the accuracy of the modeling design has been demonstrated by comparing the simulation results between the modeling and the practical regulator. Consequently, based on the presented design procedure, a charge pump regulator can be implemented and the characteristics can be planned by analyzing the proposed equivalent model. The primary advantage of the modeling approach presented here is the ease by which the regulator system can be analyzed. This permits the development of charge pump regulator designs.

6.2 Suggestions for Future Works

The following issues raised in the course of this study appear to merit further investigation.

The traditional electrostatic discharge (ESD) protection circuits are not suitable for these applications. The more robust ESD protection circuits are required in low-voltage processes and must be developed.

Several clock signals with high voltage amplitude are generated in charge pump circuits for controlling the transfer switches, so that the cross coupling effect due to layout drawing occurs in the course of the clock signal transmission. The shielding work is required and must be discussed.

The gate-drain and the gate-source voltage of all devices in the proposed circuits might be large, so the proposed circuit will suffer the gate-oxide reliable problem. Especially the

operation frequency becomes higher in the advanced ICs, not only the DC overstress on the gate oxide but also the AC overstress must be considered in the high-voltage circuits realized with low-voltage devices in the future IC design.

The presented regulator can be considered as a stable overdamped case since it does not yield any oscillations and overshoot in transient responses. However, an overdamped system is always sluggish in responding to any inputs. From the control theory, it is desirable to improve the damping ratio of the system between 0.4 and 0.8 for sufficiently fast and damped transient responses.

In actual applications, since leakage currents discharge charge pump output and internal nodes, a standby scheme is necessary to charge pump operations for minimizing overall chip power consumption. In addition, when the transfer switch operates from standby to the active mode, the pumping output voltage cannot be provided with the required accuracy very rapidly due to the long setup transient of the pump circuit especially with a heavy load. To avoid the ensuing unacceptable penalty in the transient time when entering the pump mode from the standby condition, an effective high voltage standby management is necessary.

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