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Performance Improvement of Polycrystalline Silicon Nanowire Thin-Film Transistors by a High-*k* Capping Layer

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In this work, a novel polycrystalline silicon (poly-Si) nanowire thin-film transistor (NW-TFT) with side-gated configuration and a high-*k* material capping was fabricated and characterized. It was found that the gate fringing field effect via the high-*k* passivation layer can effectively improve the device performance in terms of higher ON current, larger ON/OFF current ratio, and steeper subthreshold slope (SS). The drain-induced barrier lowering (DIBL) effect is also effectively suppressed owing to better gate control.

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1. Introduction

Recently, we have proposed and demonstrated a novel single-gated (SG) polycrystalline silicon (poly-Si) nanowire thin-film transistor (NWTFT).[1)] Compared with conventional thin-film-transistors with a planar structure, the SG-NWTFT exhibits better electrical characteristics in terms of lower leakage current, higher carrier mobility, and better subthreshold slope (SS). This is mainly ascribed to the thinner channel body as well as the better crystalline quality due to much reduced amount of defects per unit length contained in the channel. However, the scheme is limited by the side-gated feature, since most of the NW surface is not governed by the bias, resulting in higher subthreshold leakage. To address this issue, we have developed a double-gated (DG) configuration.[2)] Although improved device performance has been demonstrated, the fabrication and operation conditions are more complicated with the DG scheme.

In this work, we propose and investigate a new approach to improve device performance by simply capping a high-*k* layer over side-gated NW devices. As shown in Fig. 1, the fringing field originating from the side-gate terminates on the surface of NW outside the nominal channel region and induces excess carriers for conduction. However, the field is rather weak because of the large equivalent oxide thickness (EOT) of the passivation oxide layer as compared with the gate oxide layer. To increase the fringing field, the use of a high-*k* passivation to reduce EOT is proposed in this work. With the new scheme, the effective conduction width is increased; therefore, the ON current and gate controllability can be improved. Owing to the better gate controllability, undesirable short channel effects can also be effectively suppressed.

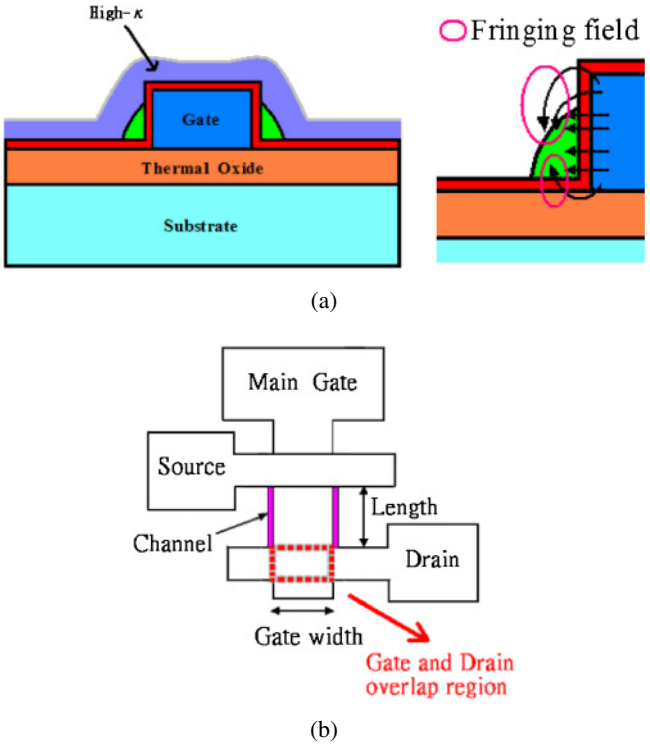


Fig. 1. (Color online) (a) Schematic cross-sectional view of the SG NW-TFT with high-*k* capping layer and the sketch of gate fringing-field on NW channel; and (b) Top view of SG NW-TFT.

2. Device Fabrication

The structure and top views of SG-NWTFT are shown in Figs. 1(a) and 1(b), respectively. A 6-in. n-type Si wafer was used as the starting substrate. First, a 150 nm SiO_2 layer was grown on Si wafer by thermal oxidation. Then, an n^+ poly-Si layer of 100 nm was grown on SiO_2 layer and defined by a g-line stepper and subsequent reactive plasma etching to serve as the main gate. A tetraethylorthosilicate (TEOS) oxide layer with a thickness of 15 nm deposited by low-pressure chemical vapor deposition (LPCVD) was employed as the gate oxide. An amorphous silicon (a-Si) layer was then deposited by LPCVD at 550 °C, and transformed into poly-Si [i.e., solid phase crystallization (SPC) process] by thermal annealing at 600 °C in N_2 ambient for 24 h. P_{31}^+ ion implantation at a dose of $1 \times 10^{15}\,cm^{-2}$ and 15 keV was performed. It should be noted that the implantation energy was intentionally adjusted to locate the implanted dopants near the top surface of the poly-Si layer. The source/drain (S/D) patterns were defined by a g-line stepper and subsequent reactive plasma etching. During the etching step, two Si nanowire channels were formed abutting the sidewall of the main gate in a self-aligned manner. Note that the doped places other than S/D regions were removed during the reactive plasma etching owing to the shallow penetration range of the low-energy implant. The S/D

dopants were subsequently activated by the thermal annealing treatment at 600 °C for 30 min. In the next step, two different treatments were applied to study the effect of surface passivation layer. In the first case [NW-TFT(A)], a 250-nm-thick oxide layer was used as the capping material. For the second case [NW-TFT(B)], an Al_2O_3 (10 nm)/HfO_2 (20 nm) stacked layer was deposited by metal–organic CVD (MOCVD) to cover the devices, followed by additional passivation using a 200 nm oxide layer. Finally, a standard metallization process was used for the formation of metal pads. Moreover, the poly-Si channels of SG-NWTFTs with and without the high-*k* passsivation layer were treated with ammonia (NH_3) plasma for 3 h to improve the characteristics.[3] A parallel-plate plasma reactor with an RF power of 200 W, a NH_3 flow rate of 700 sccm and a treatment temperature of 300 °C was used in this study. The current–voltage (*I*–*V*) characteristics of the NW-TFTs were characterized using an HP 4156 semiconductor parameter analyzer.

In this study, we found that capping with a single HfO_2 layer resulted in a large fluctuation in device characteristics due to unknown reason(s). Work is in progress to understand the cause of this behavior. However, this problem has been overcome by the insertion of a thin Al_2O_3 layer prior to deposition of the HfO_2 layer.

3. Results and Discussion

As shown in Figs. 2 and 3, the transfer and output characteristics of NW-TFT(B) shows higher on-current, less subthreshold leakage, and steeper SS than those of NW-TFT(A). As mentioned above, a high-*k* passivation tends to increase the effective conduction width by increasing field strength. Therefore, a stronger gate controllability over the channels is obtained through the high-*k* capping layer. The effect is somehow similar to that of the device with multiple-gated configuration. In addition, the nanowire channel conducting area is very small that the area of the depletion region induced by the high-*k* capping layer is sufficiently large to give a much smaller leakage path between source and drain, and hence induces less subthreshold leakage and a steeper SS.

The drain leakage current of NW-TFT in the OFF region is higher than expected, which is ascribed to the gate-induced drain leakage (GIDL) effect in the gate and drain overlapping region identified in our pervious work.[1] The drain leakage current of NW-TFT with a high-*k* passivation layer in the OFF region also shows the GIDL effect since the leakage current is also proportional to the gate width, as shown in Fig. 4. Moreover, the drain leakage current of NW-TFT(B) is higher than that of NW-TFT(A) at a fixed gate current. However, it can be observed that if the minimum I_d of NW-TFT(A) is shifted toward the right to meet the minimum I_d of NW-TFT(B) in Fig. 2, both drain leakage currents in the off-region coincide. It indicates that the drain leakage current of NW-TFT(A) and NW-TFT(B) can be ascribed to the same mechanism. The leakage difference in the off region is due to the threshold voltage difference, which is due to the high-*k* passivation layer. This can be alleviated by reducing the electric field by optimizing the doping profile or improving the poly-Si channel quality or adding a hard mask between the gate and the drain overlap region.[4]

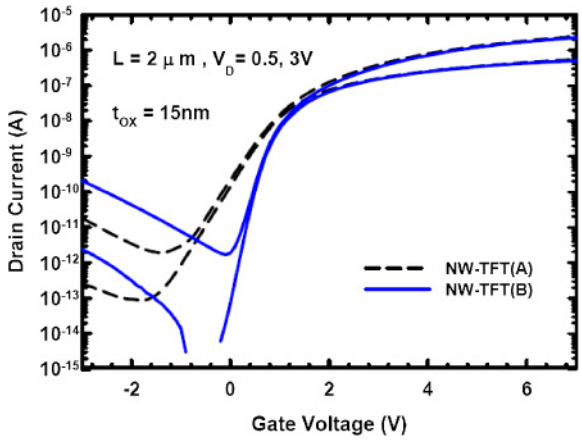


Fig. 2. (Color online) Transfer characteristics of devices without and with high-*k* capping layer.

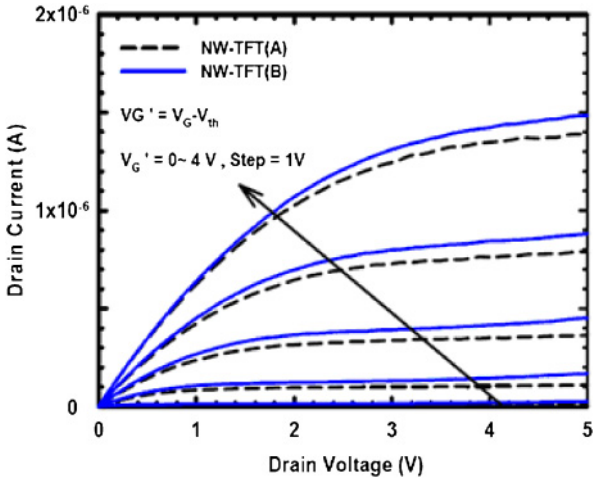


Fig. 3. (Color online) Output characteristics of devices without and with high-*k* capping layer.

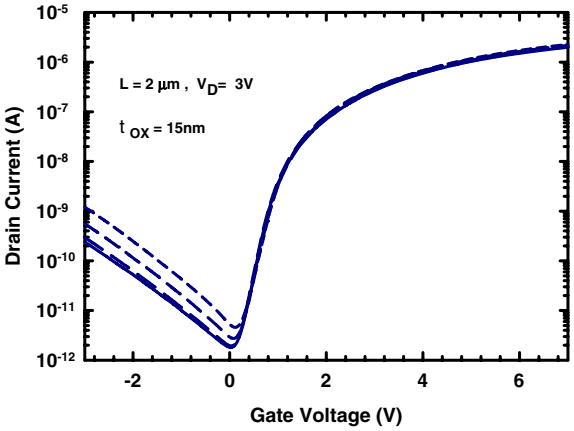
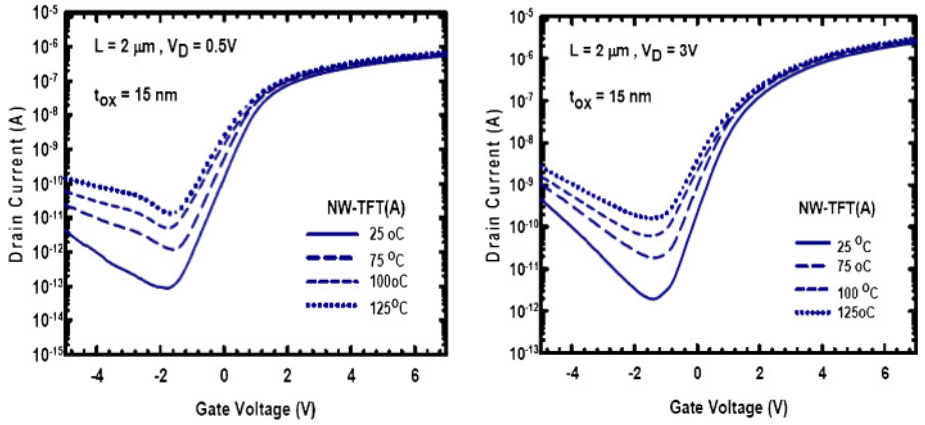
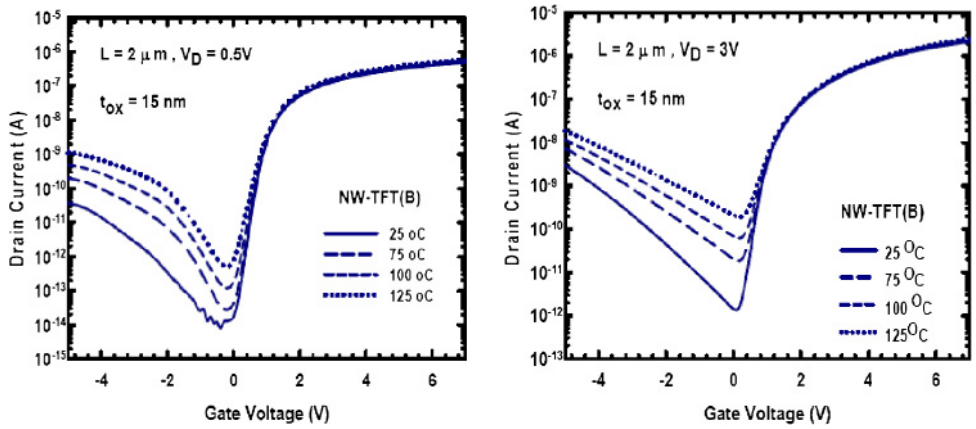


Fig. 4. (Color online) Drain leakage current of NW-TFT with high-*k* passivation layer in off region also shows the GIDL effect.

The transfer characteristics of NW-TFT(A) and NW-TFT(B) measured at different temperatures are shown in Figs. 5(a) and 5(b), respectively. Drain current increases with temperature for both devices, albeit the temperature dependence is weaker for NW-TFT(B) in the subthreshold region. This also supports the fringing field effect.



(a)



(b)

Fig. 5. (Color online) Drain current as a function of gate voltage measured at various temperatures. (a) NW-TFT(A) and (b) NW-TFT(B).

4. Conclusions

In this study, we have shown that with high-k passivation, thin-film-transistors can be improved owing to the gate fringing field effect. Compared with NW-TFTs with SiO_2 passivation, the device with high-k passivation shows higher ON current, larger ON/OFF current ratio, and steeper subthreshold slope (SS). In addition, it features good gate controllability comparable to that of the gate-surrounding device, and can efficiently suppress undesirable short-channel effects.

Acknowledgment

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