A Novel Hot-Electron Programming Method in a Buried Diffusion Bit-Line SONOS Memory by Utilizing Nonequilibrium Charge Transport

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***Abstract*—We propose a new hot-electron programming method with a low drain-to-source voltage in a buried-diffusion (BD) bit-line SONOS memory array. In this method, channel electrons are preaccelerated in a cell preceding a program cell. For a small bit-line width, some energetic electrons will traverse an n^+ BD region and enter a program cell with residual energy due to nonequilibrium transport. Our measurement result shows that this residual energy can significantly enhance hot-electron programming efficiency even at a V_{ds} of 2.5 V. The concept of this method is verified by means of a Monte Carlo analysis. Our study shows that this method is more effective as a bit-line width reduces.**

***Index Terms*—Low V_{ds}, new hot-electron programming, SONOS.**

I. Introduction

NOR-TYPE SONOS flash memories by utilizing channel hot-electron program and band-to-band tunneling hot-hole erase have been demonstrated with good performance and reliability, small die size, and low fabrication cost [1]–[5]. A virtual ground array with n^+ buried-diffusion (BD) bit lines is implemented to achieve a higher packing density [6]. For hot-electron programming in a NOR-type flash memory, a large drain-to-source voltage V_{ds} (~4 V) is usually required for channel electrons to surmount the SiO_2/Si barrier. As gate length is scaled down, surface punchthrough caused by a large V_{ds} becomes a major constraint in NOR-type flash scaling. To overcome this scaling limit, we propose a new concept of hot-electron programming in a BD bit-line array with a low V_{ds}. In our method, channel electrons gain energy in two stages (Fig. 1). Electrons are preaccelerated in a preceding cell, i.e., cell (N-1) in Fig. 1. Some energetic electrons may traverse the n^+ BD region and reach a program cell, i.e., cell (N), with residual energy. This residual energy is significant when the BD region is narrow and is attributed to nonequilibrium transport across the BD region where the electric field is almost zero. With the electron energy boosting, channel electrons in a program cell exhibit higher programming efficiency.

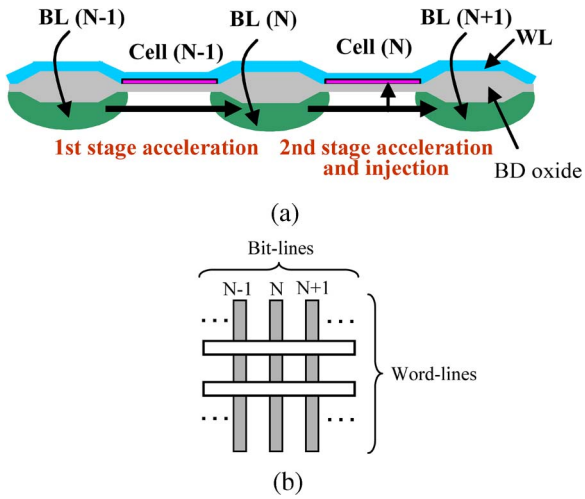

Fig. 1. (a) Illustration of a new hot-electron programming method and two-stage electron acceleration in a BD bit-line SONOS array. (b) Top view of the array.

In this letter, we compare the programming characteristics of our method and two conventional hot-electron methods. The electron preacceleration effect is characterized. Furthermore, the concept of our method is verified through a Monte Carlo simulation. The impact of a bit-line width is also evaluated.

II. Measurement Results

Fig. 1(a) and (b) shows the cross section and top view of a BD bit-line SONOS array, respectively. The BD width and the gate length are 0.1 μm in this letter. The program bias voltages are given in Table I. The biases of two conventional hot-electron program methods (methods B and C) are also shown in Table I for a comparative study. Method B has CHISEL injection [7], while method C does not have CHISEL. The programming characteristics of these methods are shown in Fig. 2. The V_{ds} in a program cell is fixed at 2.5 V in all the methods. A reverse read with a bit-line voltage of 1.6 V is employed [1]. Obviously, our proposed method has a faster programming speed compared to the conventional methods with or without CHISEL. Our method exhibits a larger program V_t window than method B by ~0.9 V. It should be pointed out that the program current [i.e., the channel current of cell (N)] in our

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TABLE I
PROGRAM BIAS VOLTAGES IN THIS METHOD (A) AND IN TWO CONVENTIONAL HOT-ELECTRON METHODS (B AND C). METHOD B HAS CHISEL INJECTION, WHILE METHOD C DOSE NOT HAVE CHISEL. $V_{\rm BL}$ IS THE BIT-LINE VOLTAGE, AND $V_{\rm WL}$ IS THE WORD-LINE VOLTAGE

voltages / methods	$V_{BL(N-1)}$	$V_{BL(N)}$	$V_{BL(N+1)}$	V_{WL}
A (this method)	0.0V	2.0V	4.5V	9.5V
B (w/ CHISEL)	floating	2.0V	4.5V	9.5V
C (w/o CHISEL)	floating	0.0V	2.5V	9.5V

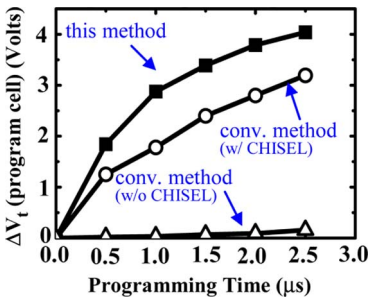

Fig. 2. Threshold voltage shift versus programming time of the three hot-electron program methods in Table I. The $V_{\rm ds}$ of a program cell is fixed at 2.5 V.

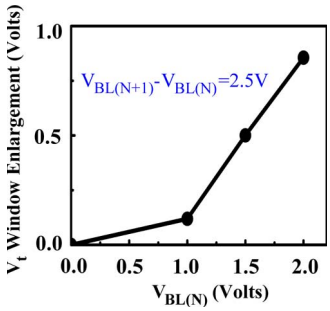

Fig. 3. Dependence of V_t window enlargement on the preacceleration voltage $V_{\rm BL(N)}$ in this method. The V_t window enlargement is defined as V_t (this method) $-$ V_t (method B). The $V_{\rm ds}$ of a program cell, i.e., $V_{\rm BL(N+1)} - V_{\rm BL(N)}$, is fixed at 2.5 V. The programming time is 2.5 μs.

method and in method B is about the same. The reason is that the voltages applied to the program cell in our method and in method B are exactly the same, except that the source of the channel current is different. The programming electrons in our method are from a preceding cell, which experience preacceleration, while they are from a bit line in method B. In addition, we measure the threshold voltage of cell (N-1) in programming. No threshold voltage shift (program disturb) is observed in a program period of 2.5 μs. To further examine the electron preacceleration effect on V_t window, we vary the preacceleration voltage $V_{\rm BL(N)}$ in programming while the $V_{\rm ds}$ of a program cell, i.e., $V_{\rm BL(N+1)} - V_{\rm BL(N)}$, is fixed at 2.5 V. The programming time is 2.5 μs, and a V_t window enlargement is defined as ΔV_t (this method) $-$ ΔV_t (method B). As shown in Fig. 3, a program V_t window shows positive dependence on the preacceleration voltage $V_{\rm BL(N)}$. This trend suggests that as $V_{\rm BL(N)}$ increases, program cell electrons have higher energy and, thus, higher injection efficiency.

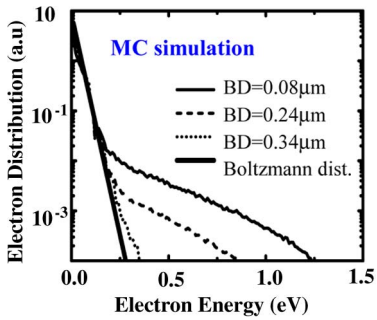

Fig. 4. Monte-Carlo-simulated electron energy distribution at the source of cell (N) for different BD widths. The bias voltages are given in Table I. The thick solid line represents a Boltzmann distribution.

III. MONTE CARLO ANALYSIS

To simulate nonequilibrium transport in the n^+ BD region and an electron residual energy distribution, a coupled Monte Carlo and 2-D numerical device simulation is performed [8], [9]. In the simulation, the electric field distributions in cells (N-1) and (N) are obtained from a 2-D device simulator. The Monte Carlo simulation includes a full band structure, and the carrier scattering parameters were calibrated in our earlier paper [9]. Electrons are launched at the source of cell (N-1) with a Boltzmann distribution and are collected at the source of cell (N) after transmitting the n^+ BD region. The MC-calculated electron energy distribution at the source of cell (N) is shown in Fig. 4 for different BD widths. It should be noted that the electron energy distribution apparently deviates from a Boltzmann distribution and exhibits a high-energy tail. Moreover, the high-energy tail becomes more pronounced as a BD width is reduced. The reason is that electrons acquiring energy in cell (N-1) cannot release their energy completely when passing through a narrow BD region. As a consequence, a smaller BD width has stronger nonequilibrium transport and, thus, a larger program V_t window.

IV. CONCLUSION

We propose a new hot-electron programming concept in a BD bit-line SONOS array. In our method, electron acceleration is achieved in two adjacent cells rather than in a single cell. In this way, the $V_{\rm ds}$ in each cell can be reduced to avoid surface punchthrough. Our characterization shows that this program method is more efficient than conventional hot-electron program methods. This method is more effective as a BD width reduces and is suitable for further scaling in a SONOS memory.

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