A 45nm Dual-Port SRAM with Write and Read Capability Enhancement at Low Voltage

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ABSTRACT

This paper presents circuit techniques to improve write and read capability for dual-port SRAM design fabricated in a 45nm low-power process. The write capability is enhanced by negative write biasing without any reduction in the cell current for the other port. The result shows 12% better improvement with just 1.9% area overhead. This technique has been verified successfully on 65nm and 45nm SRAM chip and improved 120mV lower at 95% yield of minimum operation voltage than a conventional one. The read capability is enhanced by cell current boosting and word line voltage lowering schemes. The SNM is also enhanced significantly. The target is to work below 0.8V with the worst process corner variation.

I. INTRODUCTION

As CMOS technology continues scaling down to 65nm and 45nm nodes, it is particularly difficult for SRAM design due to the fact that SRAM cell typically has more aggressive design rules and features than logic to meet stringent density requirement. Furthermore, with such a small cell size and high array density, device parameter fluctuation and characteristic variation become to impact to SRAM performance severely. Conventionally proposed raising up cell array's VDD (CVDD) to CVDD_up at read cycle and lowering down to CVDD_down at write cycle is a common and acceptable technique for single-port SRAM. However it can not apply to dual-port SRAM design. Since dual-port SRAM operation needs to read and write at the same column for 2-port operating requirement, adjusting column based CVDD_up/down can just satisfy only one port need and is not suitable for the other port. Thus the three combinational techniques, negative-write and read boosting, and word-line lowering, have been developed for the first time, which can meet read/write requirements simultaneously at the same column of dual-port SRAM operation.

II. NEGATIVE WRITE BIAS

Due to mismatch causing Vth of pass-gate NMOS of 8T dual-port SRAM cell rising, writing 0 into a bit-cell becomes difficult at low VDD condition for low Vgs. By applying a negative voltage to bit-line at this time [3], Vgs of pass-gate NMOS will enlarge again and pull down the storage node of bit-cell from logic 1 to logic 0 successfully while avoiding conventionally well known side-effects for "H"/-"L" read errors caused by CVDD_down and CVSS_up, respectively.

A negative voltage booster is combined with the local write buffer. Whenever a write enable signal of either A or B port activates the specified bank, its write buffer will pull down the corresponding bit-line to 0 in the first half period of a write pulse then start the booster to generate a negative pulse into bit-line in the second half period as Figure 1.

Figure 2 shows the required negative bit-line voltage for write vs. VDD for the normal and the worst cells. It is found that for the worst NMOS Vth shift, the bit-line voltage at a 1-port must become negative for VDD smaller than 0.8V to successfully flip the cell node. So applying negative bias into bit-line for write is the only way enabling to meet the dual-port read/write requirements.

Negative bit-line bias also keeps an advantage of lower VDD operation voltage than CVDD_down technique. For data retention reason, CVDD_down must keep a safe voltage margin above data retention voltage, otherwise, it will cause unselected cells disturbed. Allowing meshed power line of CVDD is also one of advantage. A characteristic comparison table between negative bit-line skill and CVDDLO technique is shown in table 1.

When a word line turns on, those on-cells will suffer stability issue. Especially at low VDD, on-

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cells' static noise margin degrade much. Adequately lowering word line voltage can gain back noise margin as shown in Figure 3. The circuitry for lowering word line voltage can be achieved by a voltage dividing technique.

In dual-port SRAM, a cell with both ports on will degrade SNM significantly. Meanwhile, if adequately lowering word line voltage to 0.9 times can almost recover SNM to original one as shown in the butterfly curves of Figure 4.

III. READ ENHANCING

With device mismatch, process variation, and word line lowering, the cell current may be not enough to sense out at a lower VDD condition. This paper proposes a negative voltage booster as Figure 5 to boost the selected column's VSS to negative and therefore re-enhance the read current [4]. In an initial condition, all columns' VSS connect to 0V. When either A or B port enables a column to read, it will start a negative booster to pull down the column's VSS to negative and turn off the VSS control at the other port. If CVDD lowers, Vgs and current become small. The cell current can be recovered by lowering down VSS with a similar range to re-gain Vgs and then boost cell current. The negative bias for VSS is generated in the same manner as that for bit-line.

In a write cycle, bit-line pull down to negative and those unselected cells at the same column must take care of leakage causing cell data disturb. Also while reading one port and writing the same column at the other port, the column's VSS pulling down to negative will cause another leakage source to make cells unstable. To avoid misleading the differentiation from the conventional ones, the following points are added: negative write bias and read enhancing techniques were independently proposed for a 0.25um process and before [3]-[4]. However, they did not consider any variation issue for dual-port at all. The proposed idea is integrating write and read concerns together and combining with statistical analysis for dual-port, that is an inventive step in design.

IV. SILICON EXPERIMENT

Regarding to negative write bias, Figure 6 shows an experiment result on 65nm. It shows that a single-port 2Mb SRAM chip with negative write function can work below 0.8V even though bit-cell's NMOS Vth 100mV weaker. In addition, Figure 7 shows comparisons between conventional ones and this work. It shows that the negative write biasing significantly improved 120mV Vddmin at low voltage on a 45nm dual-port SRAM chip as shown in Figure 7.

V. SUMMARY

This paper has presented the design techniques to enhance write and read capability on 1Mb dual-port SRAM chip using 45nm low-power process. The chip has been demonstrated that Negative write bias can improve write capability. Read current boosting can enhance read current and improve read capability. Lowering word line voltage can improve cell's SNM. These ideas were implemented on a 45nm 1Mb dual-port SRAM chip. The chip size is $7.84mm^2$ as shown in Figure 8.

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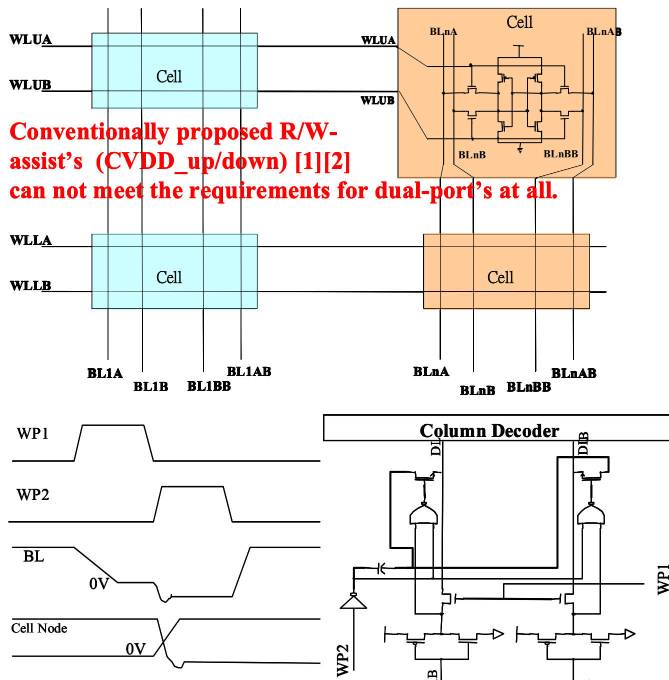

Figure 1: Negative write bias scheme.

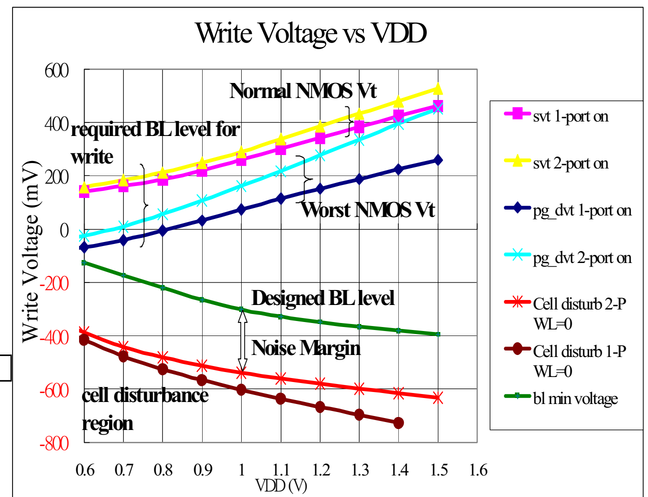

Figure 2: bit-line write voltage vs. VDD. Svt means standard Vt. Dvt indicates NMOS Vt deviation.

Table 1

A Characteristic Comparison Table between Negative Bit-Line Skill and CVDDLO Technique.

	Area penalty	Noise tolerance (mesh power)	VDD min for retention	SOC friendly
Negative BL	small for each I/O mux block	Good for VDD keep meshed	lower	Good for Metal4 as power mesh routing
CVDDLO	large for each column mux pitch	NG for no VDD mesh	higher	Power routing from metal5

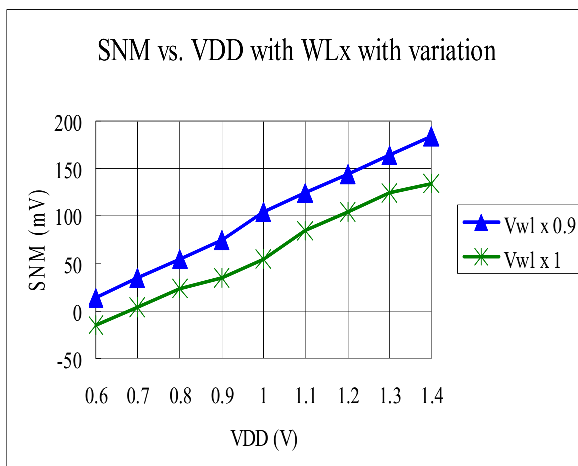

Figure 3: SNM @6σ tail bit vs. word-line voltage

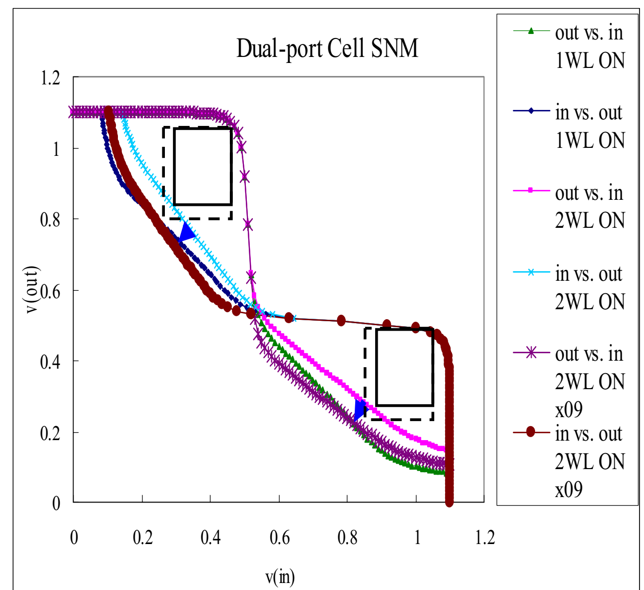

Figure 4: SNM vs. VDD between Vwl and 0.9 * Vwl with cell Vt deviation; Butterfly curves of SNM number among 1-port on (100%), 2-port on (80%), and 0.9x word line voltage (100%).

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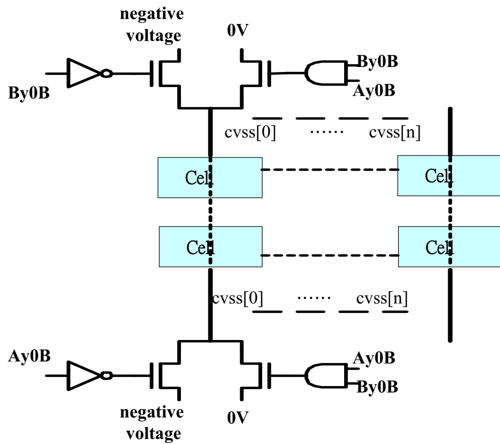

Figure 5: Read boost scheme.

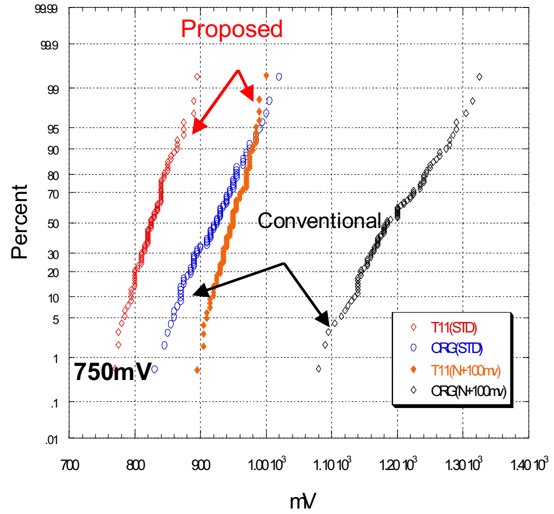

Figure 6: 65nm silicon result on cumulative percentage vs. vdd min. T11 indicates 2Mb single-port SRAM with negative write bias. ORG indicates normal 0V write voltage. Each dot indicates cumulative percentage of 2Mb SRAM chip pass yield at that vdd voltage.

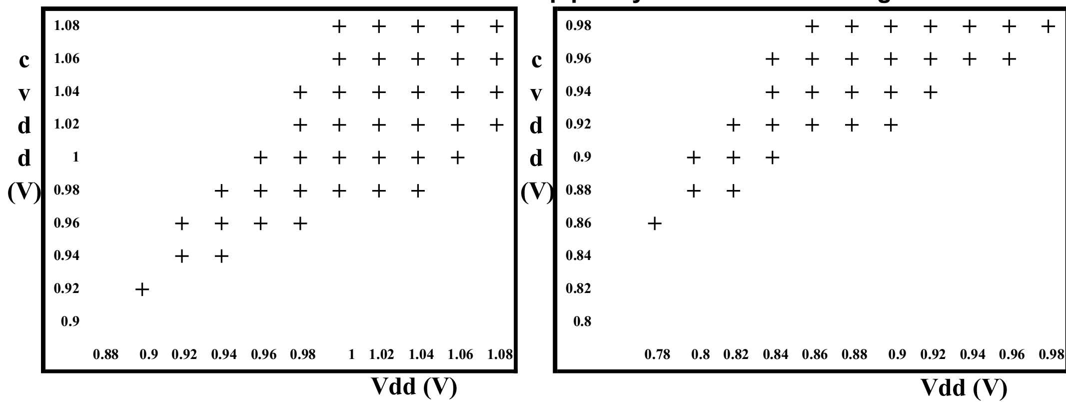

Figure 7: 45nm silicon result on testing dual-port functional comparison with (left picture) and without (right picture) negative bit-line technique. Vddmin improved 120mV with negative write bias.

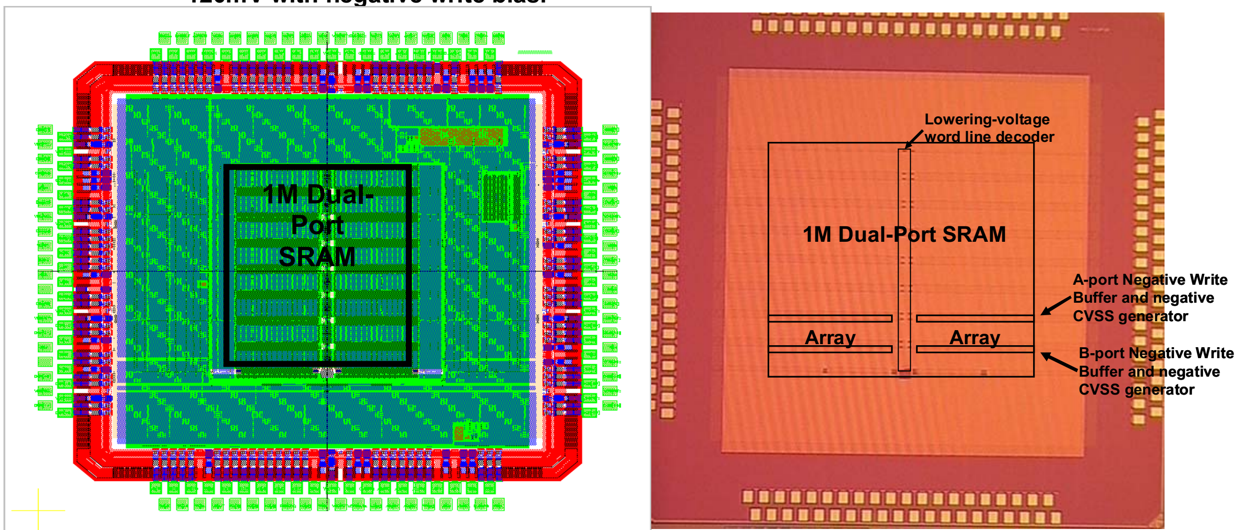

Figure 8: Layout plot and micrograph of 1Mb dual-port SRAM chip.

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