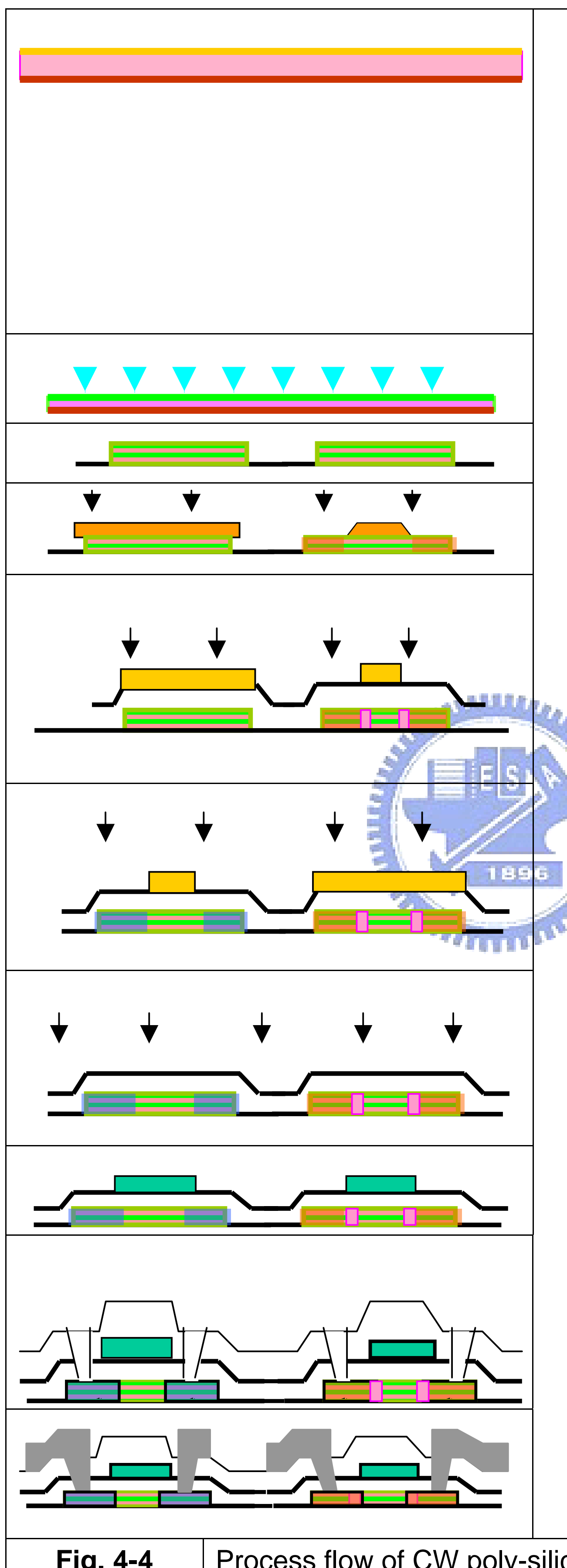

1. A buffer layer of 50nm/150nm thickness of SiNx/SiOx were deposited by plasma enhanced chemical vapor deposition (PECVD) at 500°C on glass substrate
2. Amorphous silicon film of a 50nm thickness was deposited on buffer layer as the active layer by PECVD at 500°C
3. Dehydrogenation at 500°C for one hour
4. Prior cleaning by HF 30sec + O3 100sec
5. Amorphous silicon crystallized by continuing wave laser with wavelength of 532 nm at room temperature
6. The polycrystalline layer was tailored into active islands
7. n+ ion doping of PH_2^+ ion implantation with the concentration of 6×10^{14} cm^{-2} for 13kev at room temperature
8. 1000Å thick TEOS gate oxide deposited using PECVD system
9. PR coating and patterned
10. LDD ion doping of PH_2^+ ion implantation with the concentration of 2×10^{13} cm^{-2} for 75kev at room temperature
11. PR coating and patterned
12. p+ ion doping of BF_2^+ ion implantation with the concentration of 1×10^{15} cm^{-2} for 30kev at room temperature
13. Rapid thermal annealing performed to activate the implanted dopants and recrystallize the source and drain region at temperature 650°C.
14. 2000Å thick Mo gate electrode was deposited using PVD
15. A 3000Å/500Å thick PECVD SiOx/SiNx deposited as passivation layers
16. Hydrogenation
17. Via hole open
18. Ti/Al/Ti deposited by PECVD system
19. Patterned to form the source and drain contact pads.

Fig. 4-4 Process flow of CW poly-silicon TFTs