國 立 交 通 大 學

電機學院　　電子與光電學程

碩 士 論 文

超寬頻無線網路應用之
低功率高速類比數位轉換器設計

A Low-Power High-Speed A/D Converter Design for UWB Wireless Applications

研 究 生：陳世基　　Shih-Chi Chen

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

中 華 民 國 九 十 六 年 六 月

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A Thesis

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摘　要

本篇論文提出利用互補金氧半製程實現一應用於極寬頻無線通訊系統的六位元、每秒 20 億次、寬頻低功率的快閃式類比數位轉換器。提出一結合串級電阻平均技術、內差技術、取樣保持電路和數位錯誤校正技術的低功率高速架構。對於平均技術、內差技術、取樣保持電路和數位校正技術的原理有詳細的分析和討論。使用平均技術，可以減少前級放大器的功率消耗。使用內差技術，可以使前級放大器的數量和輸入電容減半。使用取樣保持電路，可以改善動態效能。使用數位校正技術可以減少 2^N-1 個管線式閂鎖的功率。結合這些技術，在輸入頻率高達 976 百萬赫茲，每秒 20 億次取樣的情況下，六位元快閃式類比數位轉換器可實現 5.05 的有效位元。在微分非線性度和積分非線性度的結果分別低於 0.1LSB和 0.14LSB。信號對雜訊失真比和無雜波干擾之動態範圍在信號為 7.81 百萬赫茲時分別為 37.51 分貝和 48.94 分貝。信號對雜訊失真比和無雜波干擾之動態範圍在信號為接近Nyquiest頻率時分別為 32.2 分貝和 33.68 分貝。整個類比數位轉換器的消耗功率在 1.2 伏特的電壓下消耗 117 毫瓦，FOM只有 1.8p焦耳。

此快閃式類比數位轉換器是使用聯電 0.13 微米單層複晶矽 8 層金屬互補金氧半製程來實現，採用矽品 QFN32 來包裝並且黏著在印刷電路板上以利於測量。信號對雜訊失

真比在 20 億赫茲的取樣頻率以及輸入信號為 2.00 百萬赫茲時的量測結果為 27.97 分貝。計算出的有效位元為 4.3 位元。所量測到的微分非線性度和積分非線性度為 +1.56/-1.00 LSB 和 +1.91/-1.85 LSB。

A Low-Power High-Speed A/D Converter Design for UWB Wireless Applications

Student：Shih-Chi Chen Advisor：Dr. Kuei-Ann Wen

Degree Program of Electrical and Computer Engineering

National Chiao Tung University

ABSTRACT

A 6-bit 2-GSample/s flash A/D converter with wide bandwidth and low power for ultra-wideband (UWB) application is demonstrated in CMOS technology. A low-power high-speed architecture by combining the cascade resistive averaging, interpolation, wideband sample-and-hold and digital error correction technique is proposed. The principle of averaging, interpolation, wideband sample-and- hold technique and digital error correction is analyzed and discussed in detail. Use the averaging, can reduce power in preamplifiers. Use the interpolation can halve the number of preamplifiers and halve input capacitance. Use the sample-and-hold can improve dynamic performance. Use the digital error correction to can eliminate the power of 2^N-1 pipeline latches. With the combining techniques, a 6-bits flash A/D converter achieves effective 5.05 bits for input frequencies up to 976MHz at 2-GSample/s. The results show peak differential-nonlinearity (DNL) and integral-nonlinearity (INL) is less than 0.1LSB and 0.14LSB. The signal-to-noise and distortion ratio (SNDR) at

7.81MHz is 37.51dB and the spurious-free dynamic range (SFDR) at 7.81MHz is 48.94dB. Near Nyquiest input frequencies, SNDR and SFDR maintain above 32.2 and 33.68dB respectively. This flash A/D converter consumes 117mW from 1.2V power supply at 2-GSample/s, and a figure of merit (FOM) is only 1.8pJ.

The flash A/D converter is implemented in UMC 0.13μm 1P8M CMOS technology and has been packaged in SPIL QFN32 which is mounted on PCB board in favor of measurement. The measurement of the SNDR is 27.97dB under 2GHz sampling rate and 2.00MHz input frequency. The effective number of bits (ENOB) is calculated equal to 4.3 bits. The measured DNL and INL are +1.56/-1.00 LSB and +1.91/-1.85 LSB.

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感謝實驗室的四位學長-陳哲生學長、趙皓名學長、鄒文安學長、林立協學長，在研究的過程，適時地提供協助與意見，裨益研究不少。再者，感謝實驗室的同儕–顯聰、聰明、建龍、家岱、漢健、閎仁、書旗、振威、昱瑞、建毓，在學業及生活上彼此切磋砥勵，互助合作。亦感謝實驗室的學弟們-磊中、佳欣、俊彥、國爵、謙若、士賢、柏麟、為實驗室營造了歡欣的氣氛，緩和舒解掉不少緊張與壓力。更感謝助理們的幫助，排除萬難，令研究進展順遂。

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本論文獻給所有關懷、摯愛我的人，今有此成就得功歸於你們，畢業後，定當秉持著恭敬謙遜之情，發揮自我專業，貢獻國家，服務並回饋社會人群。

誌于　　2007

陳世基

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CHAPTER 1

INTRODUCTION

Wireless technologies introduce the advantages of an increasingly mobile lifestyle in cell phones and personal computers (PCs) and have resulted in greater demand for the same advantages in other consumer devices. Consumers enjoy the increased convenience of wireless connectivity. They will soon demand it for their video recording and storage devices, for real-time audio and video (AV) streaming, interactive gaming, and AV conferencing services as the need for digital media becomes more influence in the home. Many technologies used in the digital home, such as digital video and audio streaming, require high-bandwidth connections to communicate. Considering the number of devices used throughout the digital home, the bandwidth demand for wireless connectivity among these devices becomes very large indeed. The wireless networking technologies developed for wirelessly connecting PCs, such as Wi-Fi and Bluetooth technology, are not optimized for multiple high-bandwidth usage models of the digital home. Today's wireless personal area network (WPAN) technologies cannot meet the needs of tomorrow's connectivity of such a host of emerging consumer electronic devices that require high bandwidth. A new technology is needed to meet the needs of high-speed WPANs. The Ultra-wideband (UWB) wireless technology offers a good solution for the bandwidth, cost, power consumption, and physical size requirements of next-generation consumer electronic devices.

UWB radio communications have attracted growing attention due to its promising

capability to provide high data rate with low cost and low power consumption. In February 2002, the Federal Communications Commission (FCC) allocated a spectrum from 3.1 GHz to10.6 GHz for unlicensed use of UWB devices [1]. This landmark ruling has greatly increased interest in commercial applications of UWB radio, and opened up new opportunities to develop UWB technologies. As a result, UWB is emerging as a viable solution for a short-range indoor wireless network. The IEEE 802.15 Task Group 3a has been developing a physical layer standard based on UWB technologies to support high data rate for WPAN. At this point, two technical proposals, referred to as multi-band orthogonal frequency division multiplexing (MB-OFDM) and direct-sequence ultra-wideband (DS-UWB), are being considered as the final high-speed WPAN standard. The Multi-Band OFDM frequency band plan is shown in Figure 1.1. The potential for exploiting such low power UWB links for high data rate WPAN connectivity at short range particularly for in-home networking applications has led to considerable academic research interest in this technology.

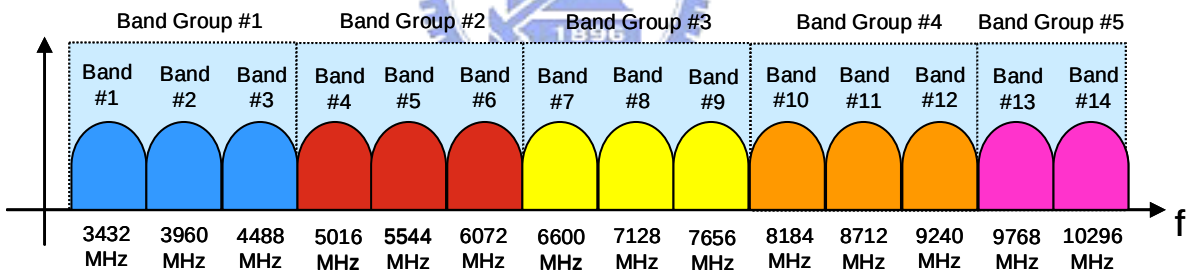


Figure 1. 1 The Multi-Band OFDM frequency band plan

1.1 Motivation

Due to the low transmit RF power, most of the concern in UWB receiver is about power consumption. This is especially important in portable devices where energy use in receive and stand-by modes is usually the dominant factor in battery life. In the MB-OFDM proposal, the frequency band is divided into 14 bands of a 528 MHz bandwidth and the data rate can be up to 480 Mb/s. So, the sampling rate of the A/D converter is 528MHz at least and 6-bits A/D converter with 5.05-bits ENOB for 480 Mb/s is sufficient. Direct-conversion architecture is adopted in the UWB receiver as shown in Figure 1.2. In receive path, the architectures under review burn most of their analog power in the A/D converter. The A/D converter consumes maximum power in UWB receiver. For A/D converter design, it is a great challenge how to give consideration to the performance and power consumption.

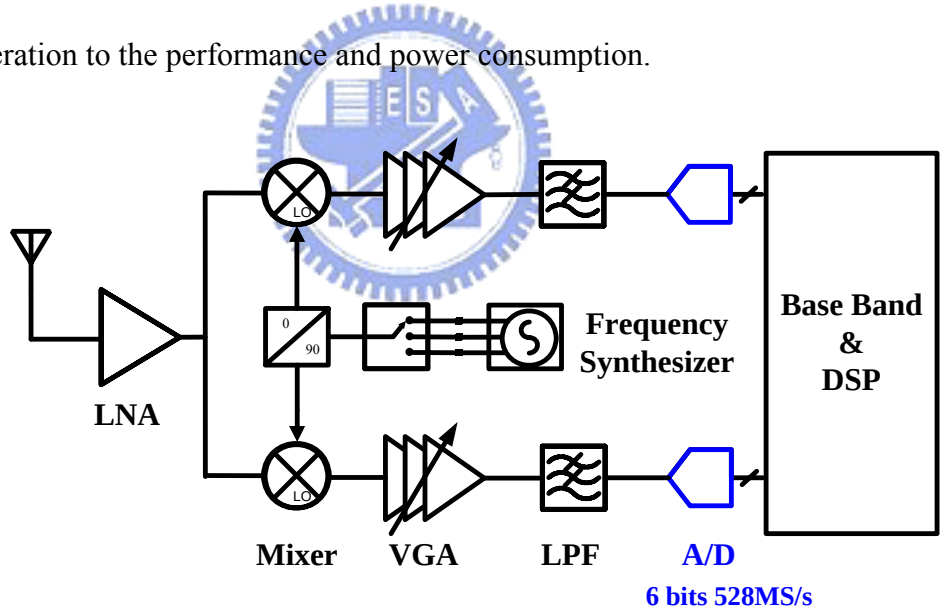


Figure 1. 2 The direct conversion architecture for UWB receiver

In general, CMOS flash A/D converter has the issues of input capacitance, input feedthrough, power dissipation, random offsets, bubble error and metastability error due to 2^n -1 preamplifiers, 2^n -1 comparators, threshold voltages variation in comparator and the speed of the comparator. To reduce the input capacitance and input feedthrough, the size of

preamplifier must be decreased, which increases the offset of the comparator. To reduce the offset of the comparator, the size of the comparator and preamplifier must be increased, which results in more power dissipation and low speed. In order to minimize the bubble error and metastability error, it needs to increase the speed of the comparators or use the pipeline latches at the output of the comparators, which increases the power dissipation and chip area. To minimize the issues while lower power consumption, we proposed a low-power high-speed A/D converter architecture combining the wideband sample-and-hold [2], interpolation [3], cascade resistive averaging [3] and digital error correction techniques [4] for low-power UWB applications. With the combining techniques, the simulation results show 5.05 ENOB can be achieved for input frequency of 976MHz while the A/D converter operates at 2G samples/s and consumes 117mW.

1.2 Thesis Organization

The organization of this thesis is overviewed as follows.

Chapter 2 reviews the architectures and applications of A/D converter. Chapter 3 presents wideband sample-and-hold, interpolation, cascade resistive averaging and digital error correction techniques to reach the low-power high-speed performance and then describes the design of each building block and analyzes the simulation results. Chapter 4 presents the test procedure and the experimental results obtained for the prototype and finally Chapter 5 concludes with a summary of contributions and recommendations for future work.

CHAPTER 2

Review of A/D Converter architectures and applications

In this Chapter, we first review a number of A/D converter architectures suited to different speed operation and study their speed-resolution-power trade-offs. Of interest to us are flash, pipelined, sigma-delta architectures.

Next, we describe general potential applications of A/D converters with different architectures, speed, resolution, and power dissipation. These include fiber-optic communication, digital oscilloscope, medical imaging, CCD imaging electronics, touchscreen digitizers and digital audio.

2.1 A/D Converter Architectures

A variety of A/D converters exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements, and temperature ranges, as well as specifications, covering a broad range of performance needs. And indeed, there exists a variety of applications in data acquisition, communications, instrumentation, digital audio, and interfacing for signal processing, all having different requirements. Considering architectures, for some applications just about any architecture could work well; for others, there is a best choice. In some cases the choice is simple because there is a clear-cut advantage to using one architecture over another, but in some cases the choice is more subtle. For example, flash A/D converters are most popular for applications requiring a throughput

rate of more than 1 GSPS with low resolution. Sigma delta converters are usually the best choice when very high resolution (20 bits or more) is needed. The differences in their architectures make one or the other a better choice, depending on the application. Among the variety of A/D converter architectures, the most popular presently used are flash A/D converter, pipelined A/D converter, and sigma-delta A/D converter [5][6]. In the following sections, these popular A/D converter architectures are briefly described.

2.1.1 Flash A/D Converter

The flash A/D converter architecture, also known as a fully parallel architecture, is fundamentally the fastest architecture. This architecture is conceptually the easiest to understand. An n-bit flash A/D converter consists of an array of 2^n-1 comparators and a set of 2^n -1 reference values, shown in Figure 2.1. Each of the comparators samples the input signal and compares the signal to one of the reference values. Each comparator then generates an output indicating whether the input signal is larger or smaller than the reference assigned to that comparator. The differences between the input and reference values are amplified to digital levels and generate thermometer code. The encoder converts the thermometer code produced by the comparators to a binary code. As seen from the figure, the comparators all operate in parallel. Thus, the conversion speed is limited only by the speed of the comparator. For this reason, the flash A/D converter is capable of high speed and it is used for high-speed applications such as wireless receiver, digital oscilloscopes, high-density disk drives, and so on.

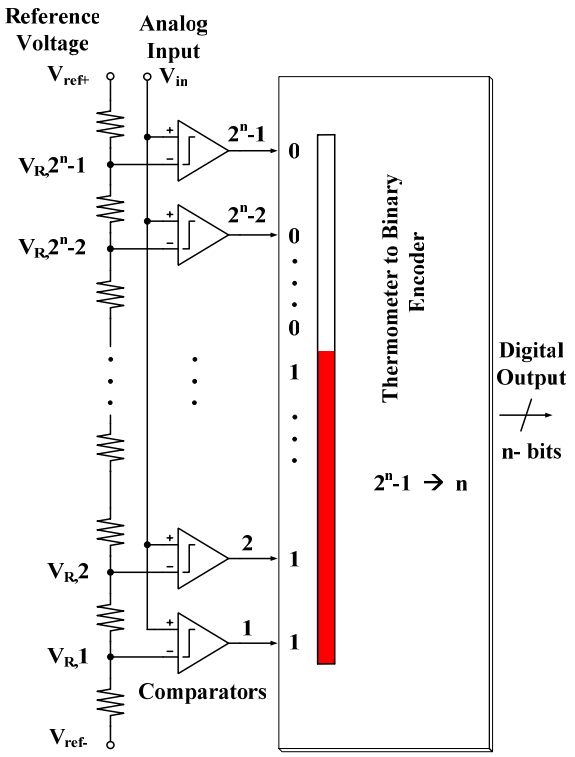


Figure 2. 1 Flash A/D Converter Architecture

The primary drawbacks to the flash A/D converter are the large hardware requirement and sensitivity to comparator offsets. As mentioned earlier, 2^n-1 comparators are required. For example, a 6-bits flash A/D converter needs 63 comparators, but 10-bits flash A/D converter needs 1023 comparators. For this reason, a high resolution flash A/D converter requires a large circuit area and dissipates high power. Furthermore, the large number of comparators present a large capacitance to the output of the sampling circuit. The required comparator offset voltage for a flash A/D converter with n bit resolution is less than $1/2^n$. At high resolutions, this required comparator offset becomes very small. Because comparators with small offsets are difficult to design and expensive to build and because so many comparators are required, A/D converters with resolutions higher than 8 bits rarely use the flash architecture.

2.1.2 Pipelined A/D Converter

The pipelined architecture effectively overcomes the limitations of the flash architecture. A pipelined converter divides the conversion task into several consecutive stages. Pipelining enables potentially faster conversion while avoiding the exponential growth of power and hardware. Figure 2.2 illustrates the block diagram of a pipelined A/D converter. The analog input is applied to the first stage in the chain, and N1 bits are detected. The analog residue is also generated and applied to the next stage. The same procedure repeats up to the end of the chain. This concept is similar to the idea of an assembly line because the interstage sampling allows all of the stages to operate concurrently. A common approach to pipelining is based on a precision multiply-by-two stage that merges most of the interstage operations into a compact circuit. Usually used with 0.5 bits of overlap, this technique provides a modular implementation.

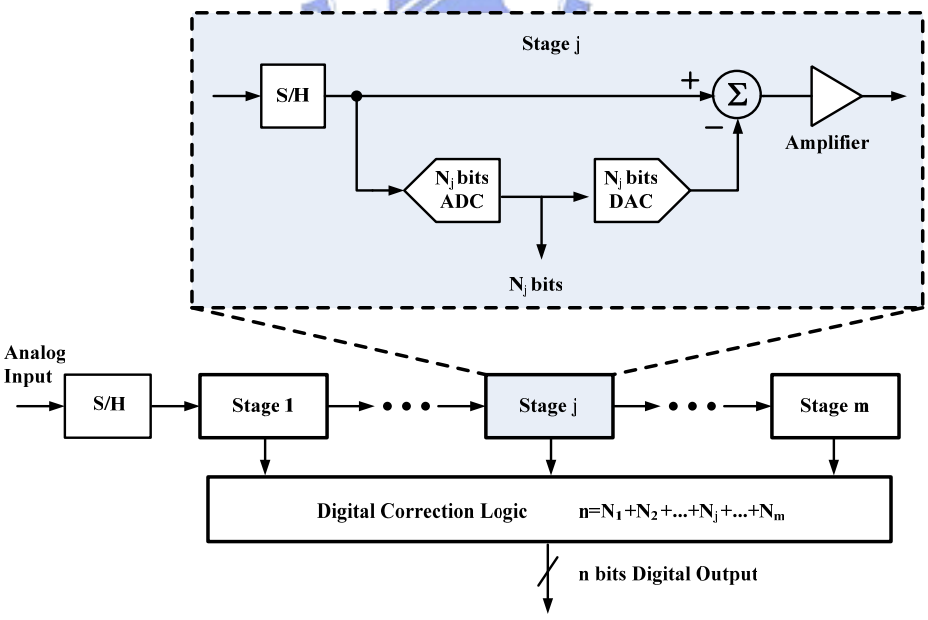


Figure 2. 2 Pipelined A/D Converter Architecture

The pipelined architecture offers a number of advantages. First, the throughput rate is determined by the speed of only one stage in the pipeline. Second, interstage residue

amplification relaxes the precision required of subsequent stages. Third, the power and hardware of pipelined converters grow almost linearly with the number of bits. Also, overlap and digital correction can be used to allow large offsets in the comparators.

The primary drawback of the conventional pipelined topology is the need for high precision in the interstage SHAs, D/A converters, and subtractors, especially at the front end. The precision typically mandates the use of op amps, imposing severe trade-offs among speed, voltage swing, gain, and power dissipation. As device dimensions, supply voltages, and the intrinsic gain ($g_m r_o$) of MOSFETs continue to scale down, the design of op amps becomes increasingly more difficult.

2.1.3 Sigma-Delta A/D Converter

The sigma-delta architecture takes a fundamentally different approach than those outlined above. In its most basic form, a sigma delta converter consists of an integrator, a comparator, and a single bit D/A converter, as shown in Figure 2.3. The output of the D/A converter is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the D/A converter, and the output of the D/A converter's is subtracted from the A/D converter input signal, etc. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the A/D converter is a stream of "ones" and "zeros," and the value of the signal is proportional to the density of digital "ones" coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output.

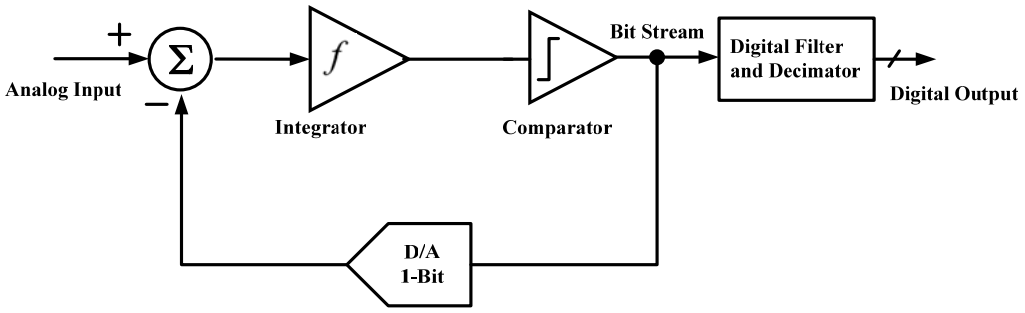


Figure 2. 3 Sigma-Delta A/D Converter Architecture

One of the most advantageous features of the sigma-delta architecture is the capability of noise shaping, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low- bandwidth high-resolution A/D converters for precision measurement. Also, since the input is sampled at a high "oversampled" rate, unlike the other architectures, the requirement for external anti-alias filtering is greatly relaxed. A limitation of this architecture is its latency, which is substantially greater than that of the other types. Because of oversampling and latency, sigma-delta converters are not often used in multiplexed signal applications. To avoid interference between multiplexed signals, a delay at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in sophisticated sigma-delta A/D converter designs by using multiple integrator stages and/or multi-bit D/A converters.

2.1.4 Summary of A/D converter Architectures

The most popular A/D converter architectures have been reviewed in the previous sections. The flash A/D converter architecture is the fastest, the Sigma-Delta A/D converter is very useful for high-resolution applications, and the pipelined A/D converter can be applied

for various applications. Each A/D converter architecture has tradeoffs among speed, resolution, and power dissipation. In summary, Table 2.1 provides the characteristics of popular A/D converter architectures [7]. In the third column, “sps” stands for samples per second. The “m” shown in the fourth column is the number of stages in the pipeline architecture.

Architecture	Resolution (bits)	Speed (sps)	Latency (cycle)	Comments
Flash	< 10	250M ~ 2G	1	-high input bandwidth -highest power dissipation -large die size
Pipeline	8 ~ 16	1M ~ 200M	m	-high throughput rate -low-power dissipation -on-chip self calibration
Sigma-Delta	> 14	> 200K	large	-high resolution -limited sampling rates -digital on-chip filtering

Table 2. 1 Summary of A/D converter architectures

2.2 A/D Converter applications

There are several applications require the different speed and resolution of A/D converters. Among these are communication, instrumentation, digital audio, digital video, and medical diagnostic equipment [8][9]. With the aid of digital signal processing (DSP), the A/D converter outputs can be processed to bring almost limitless versatility to an application. The basic building blocks of a typical system with a A/D converter include filter for analog input, A/D converter, DSP and memory system, processor and interface system, D/A converter and filter for analog output.

2.2.1 Fiber-optic Communication

High-speed fiber-optic communication requires the analog signal to be converted to digital a A/D converter. Following this the A/D converter outputs must be converted from parallel to serial output format for the driver to modulate a laser diode, as shown in Figure2.4. This allows a single fiber-optic cable to transmit several high-speed signals if necessary. On the other end of the cable, the photodiode detects the digital light pulses, which are then converted to logic level in a parallel format. The D/A converter output is finally filtered by an analog filter. Depending on the application, an option may be to first perform digital filtering before outputting to the D/A converter.

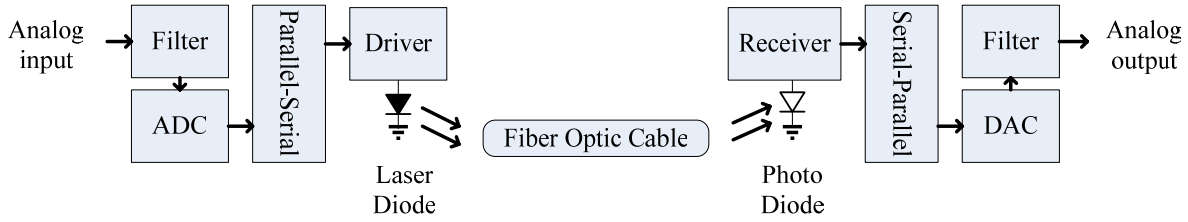


Figure 2. 4 Fiber-optic Communication

2.2.2 Digital Oscilloscope

A block diagram of a digital storage oscilloscope is shown in Figure2.5. Two input channels are first conditioned by a programmable amplifier. The trigger circuit controls when the sampling starts, which is controlled by sample-and-holds. Buffer amplifiers are required to isolate the low-impedance A/D converter input stage from loading the sample-and-holds. Once digitalized by the A/D converter, the input signals are stored in memory where a DSP can perform several operations (i.e., filtering, averaging, peak-to-peak time versus voltage, root-mean-square, etc.). Two D/A converters then provide both the vertical (signal measurement) and horizontal (time measurement) analog output signals. Finally the analog outputs are filtered before they go to the display driver.

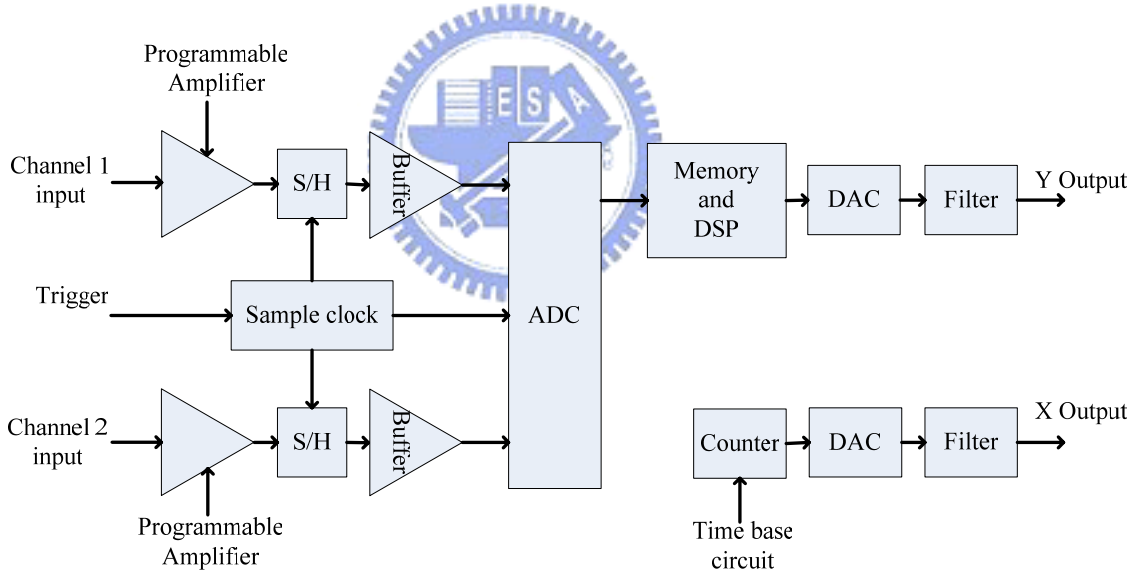


Figure 2. 5 Digital Oscilloscope

2.2.3 Medical Imaging

The One form of medical imaging is digital x ray (radiography), illustrated in Figure 2.6. With this technique, the images no longer need to be produced or stored on film. Instead, the images are stored within memory for display on a video monitor. In this system the x ray passes through a person onto photomultiplier fluoroscope sensor which converts the x rays to light. The various light intensities are then converted to an analog signal which is filtered before being digitized by the A/D converter. The DSP then enhances the image before driving the output D/A converter for the video image. The advantages to this process are that the time exposure to the x ray for a quality image is significantly shortened and stored images can be manipulated to enhance specific areas.

Figure 2. 6 Digital Radiography System

2.2.4 CCD Imaging Electronics

The charge-coupled-device (CCD) and contact-image-sensor (CIS) are widely used in consumer imaging systems such as scanners and digital cameras. A generic block diagram of an imaging system is shown in Figure 2.7. The imaging sensor (CCD, CMOS, or CIS) is exposed to the image or picture much like film is exposed in a camera. After exposure, the output of the sensor undergoes some analog signal processing and then is digitized by an A/D converter. The bulk of the actual image processing is performed using fast digital signal

processors. At this point, the image can be manipulated in the digital domain to perform such functions as contrast or color enhancement/correction, etc.

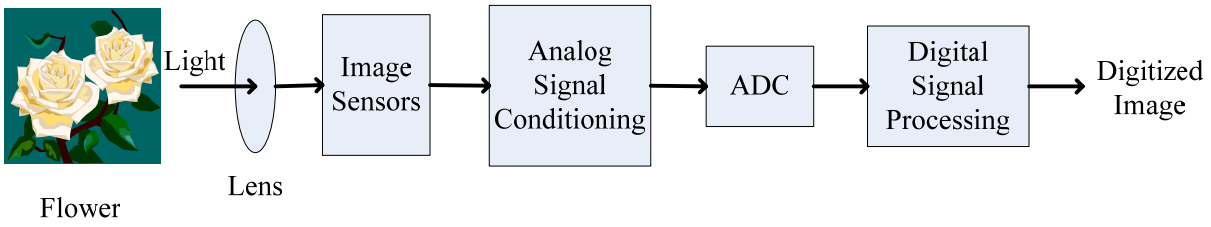


Figure 2. 7 Generic Imaging System for Scanners or Digital Cameras

2.2.5 Touchscreen Digitizers

The touchscreens have become widespread in hand held PDAs (Personal Digital Assistants) and other computer products. The majority of PDA makers use a four-wire resistive element as the touchscreen due to its low cost and simplicity. For the touchscreen to interface with the host processor, analog waveforms from the screen must first be converted to digital data . The user enters data on the screen with a stylus. An A/D converter converts this analog information to digital data that the host microprocessor uses to determine the stylus's position on the screen. During coordinate measurement, one of the resistive planes is powered through on-chip switches on the controller A/D converter. For X coordinate measurement, the X plane is powered. The Y plane senses where the pen is located on the powered plane. When the pen depresses on the screen, the planes short at this location (shown as the dotted line in the diagram). The voltage detected on the sense plane is proportional to the location of the touch on the powered plane. The four -wire resistive touchscreen interface for X coordinate measurement as shown in Figure 2.8. The Y coordinate can be measured by applying power to the Y plane, using the X plane to sense the position. Thus, X and Y coordinates can be

digitized from the screen. The digital code is then operated on by the host CPU, and character recognition and position information can be achieved.

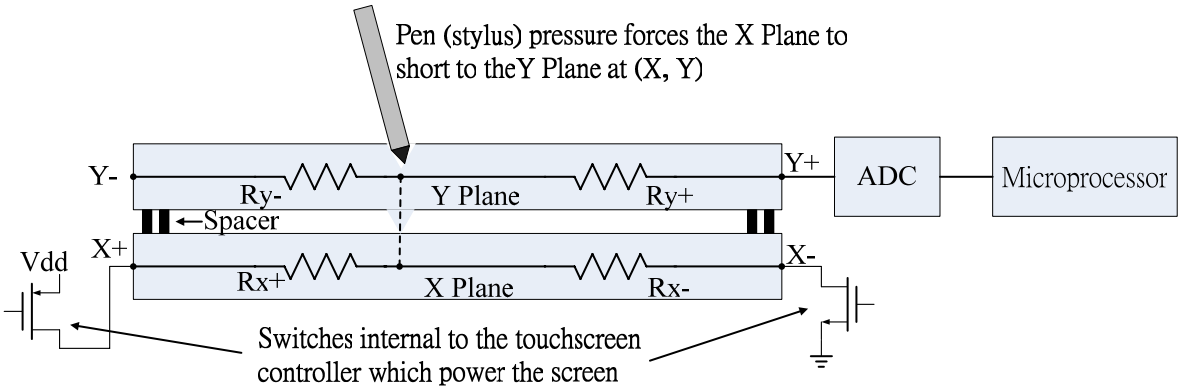


Figure 2. 8 Four-Wire Resistive Touchscreen Interface

2.2.6 Digital Audio

Modern wireless systems, such as cellular telephone, use low pass filter, high resolution A/D converters, digital signal processor (DSP) and high resolution D/A converters. The modern cell phone handset block is shown in Figure 2.9.When we speak to other person with cell phone, the low pass filter remove noise from voice, A/D converter transform voice into digital signal and then the digital signal is dealt with DSP. Modern cellular transmission systems make use of DSP-based speech compression algorithms in order to reduce the overall data rate to acceptable levels, rather than limiting the resolution of the converters. Digital audio systems place high resolution demands on A/D converters and D/A converters because of the wide dynamic range requirements. The digital audio signal may then be stored or transmitted. Digital audio storage can be on a flash memory, or any other digital data storage device. Audio data compression techniques — such as MP3— are commonly employed to reduce the size. Digital audio can be streamed to other devices. The last step for digital audio

is to be converted back to an analog signal with a D/A converter.

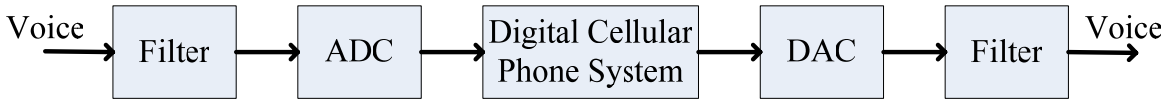


Figure 2. 9 Modern Cell Phone Handset block

CHAPTER 3

Low-Power High-Speed Techniques and Circuit Design

In this chapter, the low-power high-speed architecture is proposed to reduce the input capacitance, offset errors, power dissipation, bubble errors and metastability errors by using sample-and-hold, interpolation, averaging and digital error correction techniques. With the architecture, the dynamic performance is improved, the input capacitance is reduced, 83% power saving in preamplifiers is achieved and the power of $(2^n-1)m$ pipeline latches is removed.

The circuit design and related issues will be discussed in detail. The required resolution is 6 bits and the sampling rate is 2GHz. As the result, circuit design plays an important role to achieve the specifications. The block diagram of the proposed A/D converter is shown in Figure 3.1. The proposed A/D converter consists of analog part and digital part. The analog part consists of sample-and-hold, resistor ladder, interpolation preamplifiers, comparators and resistive averaging. The digital part consists of auxiliary circuit, AND gates, ROM, TSPC, Gray-to-binary decoder, clock generator and output buffer. The design issues of each component are discussed step by step. Finally, the static and dynamic performances simulation results are presented in the last section.

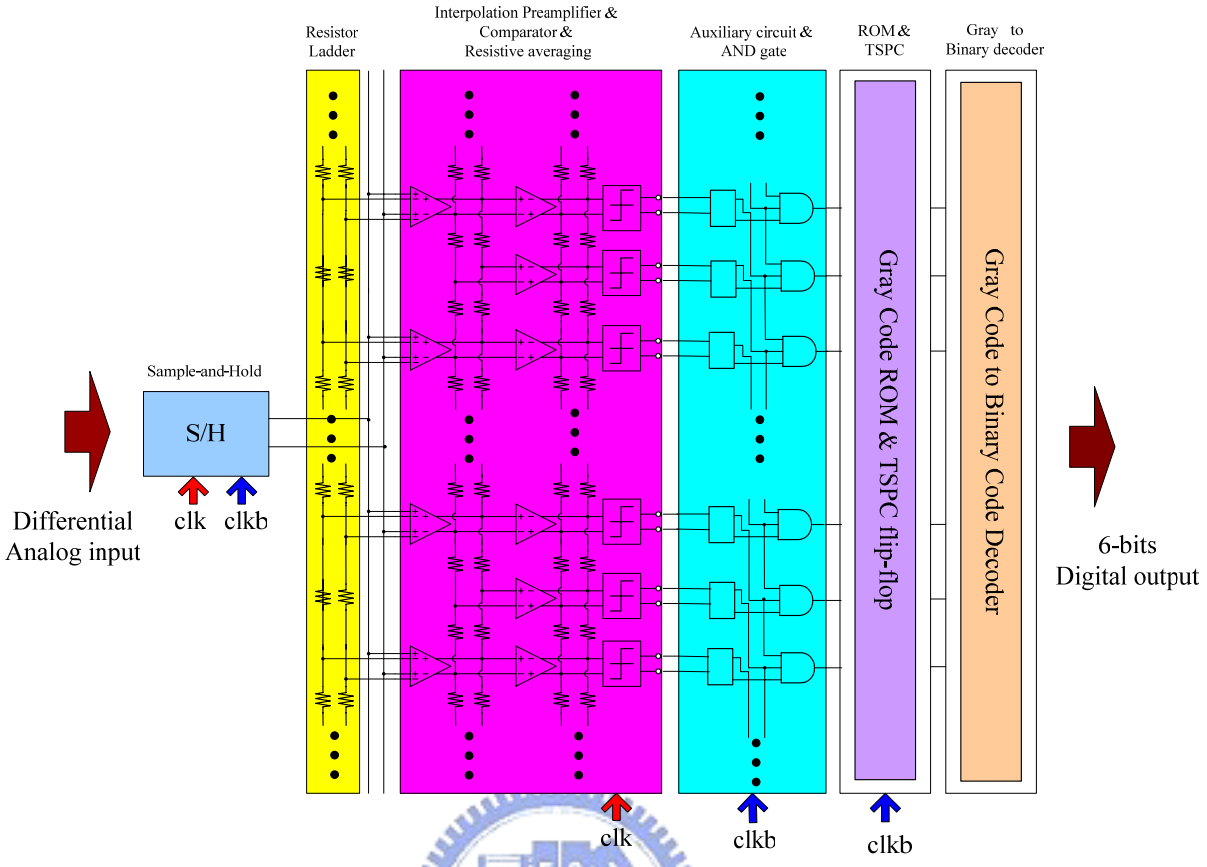


Figure 3. 1 Block diagram of the proposed low power A/D converter

3.1 Sample-and-Hold Technique

The purpose of the sample-and-hold (S/H) circuit is to track and hold the input signal long enough for the A/D converter to complete a conversion without appreciable error. The S/H circuit is a crucial part, especially for high speed sampling rates. To improve the dynamic performance of the A/D converter, a S/H circuit can be put in front of the converter. By holding the analog sample static during digitization, the S/H largely removes errors due to skews in clock delivery to a large number of comparators, limited input bandwidth prior to latch regeneration, signal-dependent dynamic nonlinearity, and aperture jitter. The distributed time skew problem of quantization is alleviated as a result of the usage of the front-end S/H

circuit. For gigahertz sampling rate operation, S/H becomes essential to achieve the desired converter resolution with wide input bandwidth.

Closed loop configuration provides good linearity and dynamic range but cannot achieve very high speeds. In order to operate at high speed, the S/H has to be a simple open-loop configuration. The basic S/H configuration shown in Figure 3.2 consists mainly of a sampling switch and a holding capacitor [3]. This single ended configuration makes it possible to design for very high speed, but it has signal-dependent charge injection and clock feedthrough.

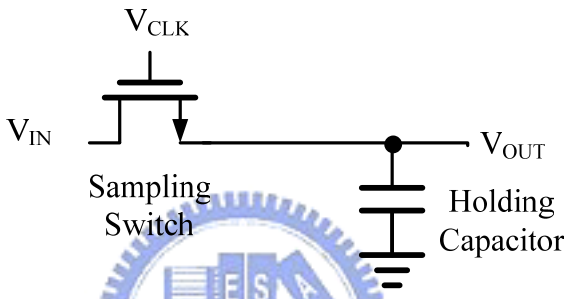


Figure 3. 2 Basic S/H Configuration

The pseudo-differential type S/H configuration shown in Figure 3.3 is the best choice to solve signal-dependent charge injection and clock feedthrough. This type S/H consists of sampling switches, dummy switches, holding capacitors, and unity gain buffers. The dummy switches are driven by reverse of the clock signal and they are used to reduce the effect of signal-dependent charge injection and clock feedthrough released from the sampling switches [2]. The holding capacitors are made large enough to overcome the gate capacitance variation of the MOSFET. The buffer is made by PMOS whose bulk is connected to its source to suppress the body effect.

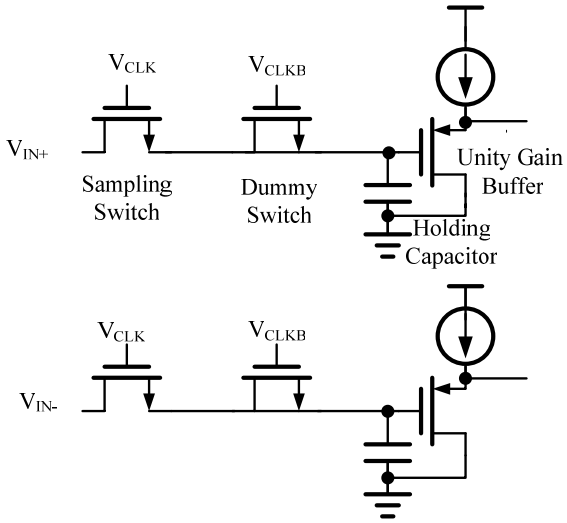


Figure 3. 3 Pseudo-Differential Type S/H Configuration

In Figure 3.3, the constant current source follower is the simplest realization of a unity gain buffer. But, it still has limitation and drawback. When the input to the buffer is fast and has large amplitude, the skew rate at the output of the circuit is limited. Thus, its speed can not be linearly improved by increasing the bias current. Although we can suppress the body effect by connecting its bulk to source, its gain still can not reach real unity. Due to the finite output resistance, its gain can only approximate 0.9. The buffer with this gain will degrades the amplitude of output signal when input frequency is very high. So, adding a PMOS loading to increase output resistance can make the gain approximates unity.

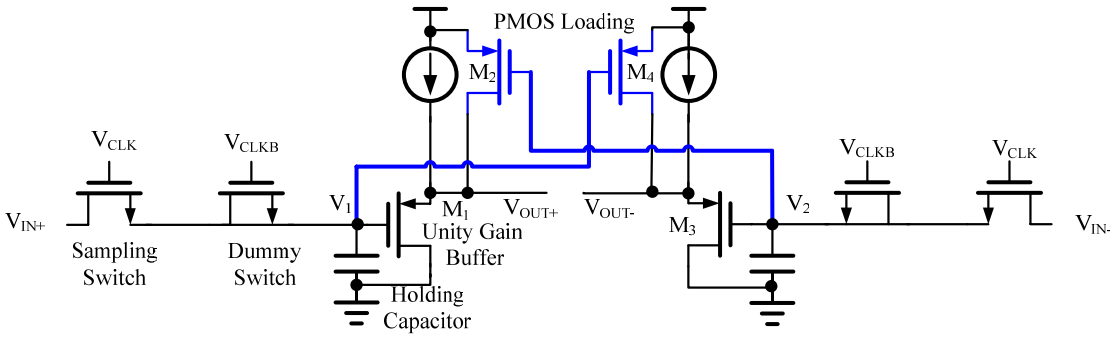


Figure 3. 4 The first cross-coupling type S/H Configuration with a PMOS Loading

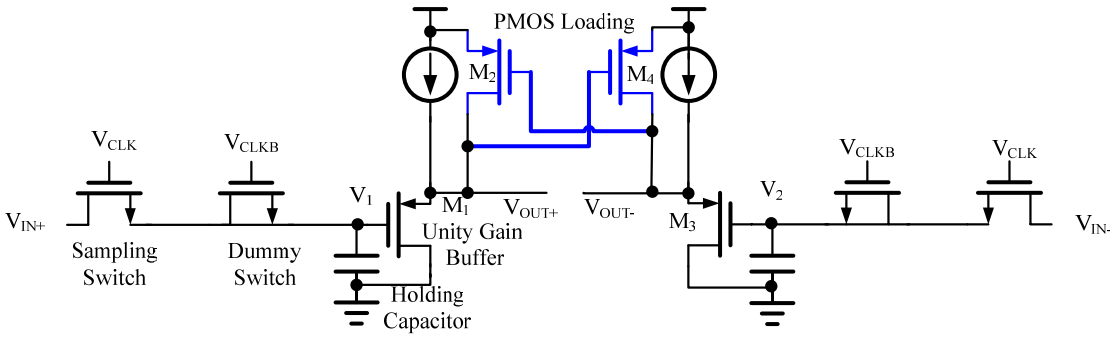


Figure 3. 5 The second cross-coupling type S/H Configuration with a PMOS Loading

There are two cross-coupling types of the S/H configuration and their gain can achieve unity. The first cross-coupling type is shown in Figure 3.4 and second cross-coupling type is shown in Figure 3.5. The gain of the first cross-coupling type S/H configuration is given by (detailed analysis is shown in Appendix):

$$\frac{V_{OUT+}}{V_1} = \frac{r_{o1}r_{o2}}{r_{o1} + (1 + g_{m1}r_{o1})r_{o2}}(g_{m1} + g_{m2}) \le 1 \tag{3.1}$$

and its 3db frequency is given by (detailed analysis is shown in Appendix):

$$f_{3db} = f_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi C_{gs1}(r_{o1} // r_{o2})} \tag{3.2}$$

The gain of the second cross-coupling type S/H configuration is given by (detailed analysis is shown in Appendix):

$$\frac{V'_{OUT+}}{V'_1} = \frac{r'_{o1}r'_{o2}}{r'_{o1} + (1 + g'_{m1}r'_{o1})r'_{o2}}(g'_{m1} + \frac{g'_{m2}g'_{m1}r'_{o1}}{1 + g'_{m1}r'_{o1}}) \ge 1 \tag{3.3}$$

and its 3db frequency is given by (detailed analysis is shown in Appendix):

$$f'_{3db} = f'_1 = \frac{1}{2\pi\tau'_1} = \frac{1}{2\pi C'_{gs1}(r'_{o1} // r'_{o2})} \tag{3.4}$$

Give a sinusoidal input waveform with amplitude A and radian frequency ω and assume

unity gain buffer is one pole transfer function as follows:

$$A(\omega) = \frac{A}{\sqrt{1 + (\frac{\omega}{\omega_{3db}})^2}} \tag{3.5}$$

If the tolerable output amplitude error is lower than 2% (6 bits accuracy), we have

$$1 - \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_{3db}})^2}} < 0.02 \quad \text{, and then} \quad f_{3db} \geq \frac{1G}{0.203} = 4.926G \tag{3.6}$$

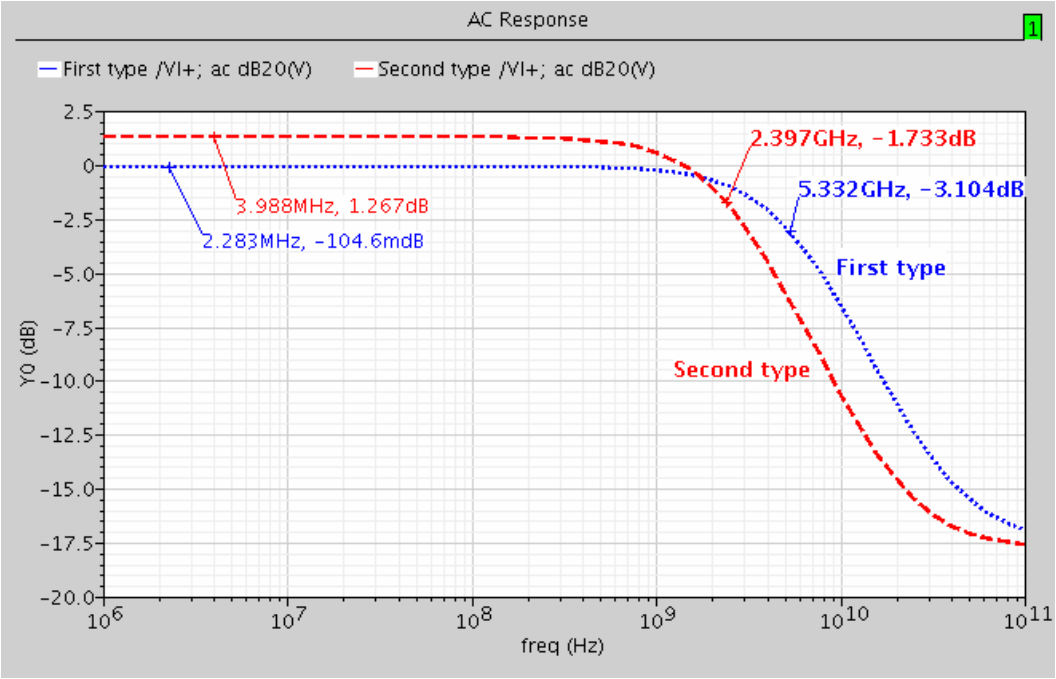


Figure 3. 6 The simulation of the first and second type S/H

The simulation of the first and second cross-coupling type S/H configuration is shown in Figure 3.6. From this figure, the gain of the first cross-coupling type S/H configuration approximates unity and its 3db frequency is 5.33GHz. The gain of the second cross-coupling type S/H configuration is larger than unity and its 3db frequency is 2.39GHz. From equation (3.6), the buffer 3db frequency must be high than 4.926GHz. Thus, the first cross-coupling type S/H configuration fits the design requirement and the 3db frequency is 5.33GHz. The proposed design can achieve the wide bandwidth to get high dynamic performance.

3.2 Interpolation Technique

It is needless to say that the number of elements and the power dissipation increase exponentially to the resolution of flash A/D converter. The flash A/D converter architecture is considered to realize the highest conversion frequency, however, it suffers from not only large chip size and large power dissipation, but also lower dynamic performance due to large input capacitance [10]. Hence, some circuit techniques that can reduce the element count are required. Interpolation technique is the good solution to solve these problems. The interpolation architecture of preamplifier is shown in Figure 3.7. △V1(=Vy1-Vx1), △V2(=Vy2-Vx2), △V(=Vy2-Vx1) are the outputs of the preamplifiers, Vin is the input voltage and Vr1, Vr2, Vr are the reference voltages.

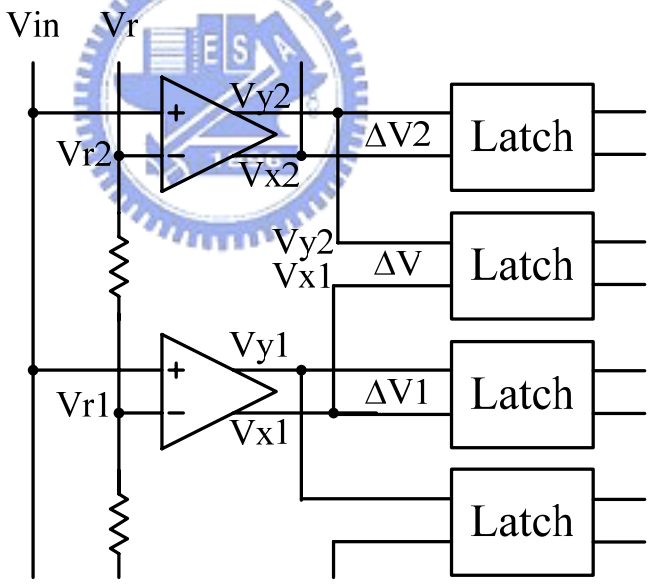


Figure 3. 7 Interpolation Preamplifier Architecture

Interpolation allows the generation of intermediate voltages, so that the input voltage does not need to be compared to 63 distinct reference voltages at the front-end of a flash A/D converter. Each input to reference voltage comparison at the front-end would require its own preamplifier, consuming an unacceptable amount of power and area. Virtual zero crossing

points shown in Figure 3.8, which are not the result of the input crossing a physical reference voltage, are created through interpolation at amplification stage. In other words, in this scheme a zero crossing is obtained by interpolating between two reference levels. Performance indices of the preamplifier such as input common-mode range, input capacitance, power dissipation, overdrive recovery speed, voltage gain, and capacitive feedthrough to the reference resistor ladder often place tight requirements on the preamplifier. Thus, using interpolation to reduce the number of preamplifiers relaxes its design requirements and can improve the differential nonlinearity [11].

However, there are some design conditions which need to be considered. Interpolation is only between close-enough preamplifier outputs to avoid non-linear zero crossing. The size of the input transistors of the preamplifier needs to be increased. Larger size can reduce the offset from the preamplifier itself. The gain of the preamplifier needs to be tuned well. Small gain of the preamplifier can not overcome the offset from comparator, but large gain of the preamplifier can cause no gain error at zero crossing shown in Figure 3.9. If no gain error at zero crossing happens, the preamplifier can not reduce the offset from the comparator. The only adequate gain of the preamplifier can generate the good zero crossing shown in Figure 3.8.

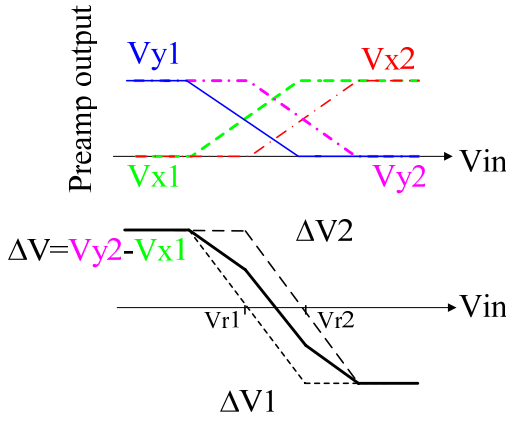


Figure 3. 8 Good Zero Crossing

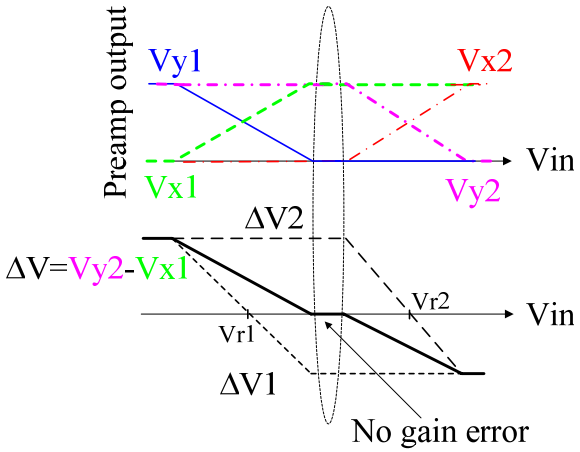


Figure 3. 9 No Gain Error at Zero Crossing

3.3 Averaging Technique

High speed flash A/D Converter with medium resolution usually employs differential pairs as pre-amplifying stages before the comparators. Their offset voltages are the ultimate limitation to the linearity that may be achieved by the A/D converter. Increasing the area of the components in the differential pairs reduces offset voltages , but increases parasitic capacitances, leading to a large power dissipation, large die size and large input capacitance or to the reduction of the maximum operating frequency [12].

To partially overcome this problem an averaging scheme will be introduced. This averaging scheme uses the outputs of more active input pairs to increase the effective gate area and in this way reduce the offset voltages. The figure 3.10 shows five differential preamplifiers with load resistor R0 as part of the input preamplifier chain used in flash A/D converter. Averaging is obtained by coupling the outputs of the differential preamplifiers via averaging resistor R1. This averaging resistor chain continues to couple more input stages. As long as the input preamplifiers are active and operate in the linear signal range, then the

output signal of these active preamplifiers contribute via the averaging resistors to the signal of a differential preamplifier operating around the zero crossing level. Here preamplifier (n=0) is supposed to be the zero crossing preamplifier. The output signals from the left neighbors of the zero crossing preamplifier influence the zero crossing. The same effect is obtained from the right neighbors. As long as the neighboring preamplifiers are in the linear region it looks like that the zero crossing amplifier consists of a much bigger device with a size equal to the sum of the areas of the active linear amplifiers [3].

By adding resistors R1, not only the offset error (noise) is reduced but also the gain of the preamplifier (signal) is loss. In order to reduce the effective gain of error but one of the signal is maintained, the resistive ratio of R1/R0 have to be choice properly to perform optimum.

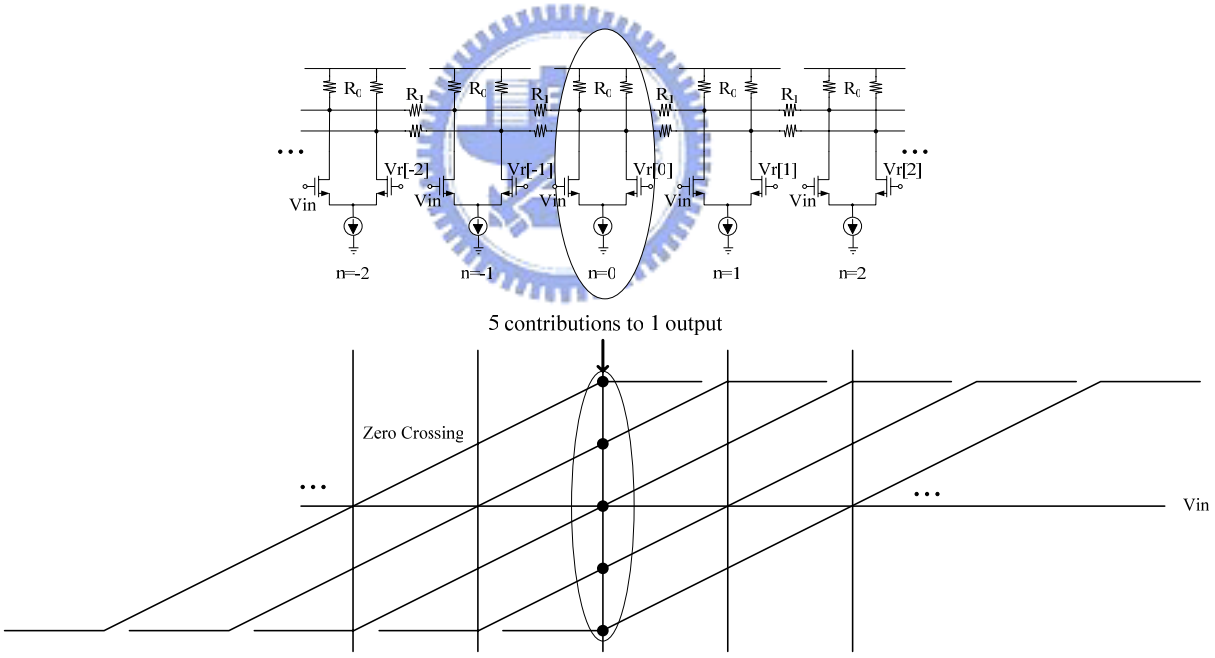


Figure 3. 10 Resistive Averaging Scheme and Zero Crossing

3.3.1 Spatial Filtering of the Averaging Resistive Network

The averaging requires the summation of quantities spread into two or more samples in either time or space. In the MOSFET example, the parallel connection spreads the noisy charges. Similarly in the preamp array of a flash A/D converter the output current spreads through the lateral connections in the averaging resistor network. Summation is automatic when physical quantities such as currents and charges merge at a node in accordance with Kirchhoff's laws.

The impulse response of the spreading network, which forms a spatial filter, characterizes the extent of spreading. Usually the wider the impulse response will get the higher the SNR. However, there are limits to this in uses such as offset averaging, where a wider impulse response also filters out signal. To correctly optimize the SNR, the properties of both signal and noise must be taken into account to find the best impulse response

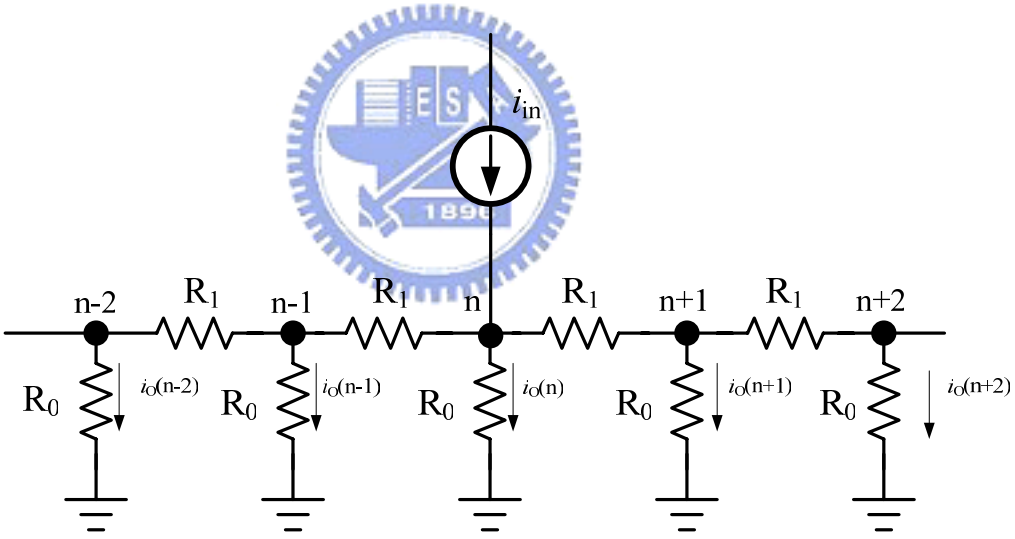


Figure 3. 11 The impulse Response of a resistor network as spatial filter

The impulse response, h(n), of the spatial filter is found by injecting a unit stimulus current at one node, and noting the resulting distribution of current in each R0 at other nodes as shown in Figure 3.11. For a stimulus current i_{in} injected to an arbitrary node n, Kirchhoff's current law (KCL) requires that

$$i_{in} - i_o(n) + (i_o(n-1) - i_o(n))R_0 / R_1 + (i_o(n+1) - i_o(n))R_0 / R_1 = 0 \qquad (3.7)$$

where the third and fourth terms are the currents flowing into node n from node (n-1) and (n+1), respectively. Using the transform simplifies analysis. Applying the z transform to (3.7)

$$H(z) = I_o(z) / I_{in}(z) = (1 + 2(R_0 / R_1) - (R_0 / R_1)(z + z^{-1}))^{-1} \tag{3.8}$$

The inverse transform H(z) of yields the spatial impulse response [13]

$$h(n) = h(0)b^{|n|}, \text{ where } b = e^{-|a\cosh(1+R_1/2R_0)|} < 1 \tag{3.9}$$

h (0) is a normalized coefficient. Uniform current division in the R0- R1 network leads to an impulse response that decays exponentially in n. The width of the impulse response can be controlled by the ratio of R1/R0 as shown in Figure 3.12. The impulse response acts as a low pass filter in spatial domain and the width of impulse response will influence the averaging effect. The smaller ratio of R1/R0 generates wider width of the impulse response to get effective averaging and then the larger ratio of R1/R0 generates narrower width of the impulse response to get poor averaging.

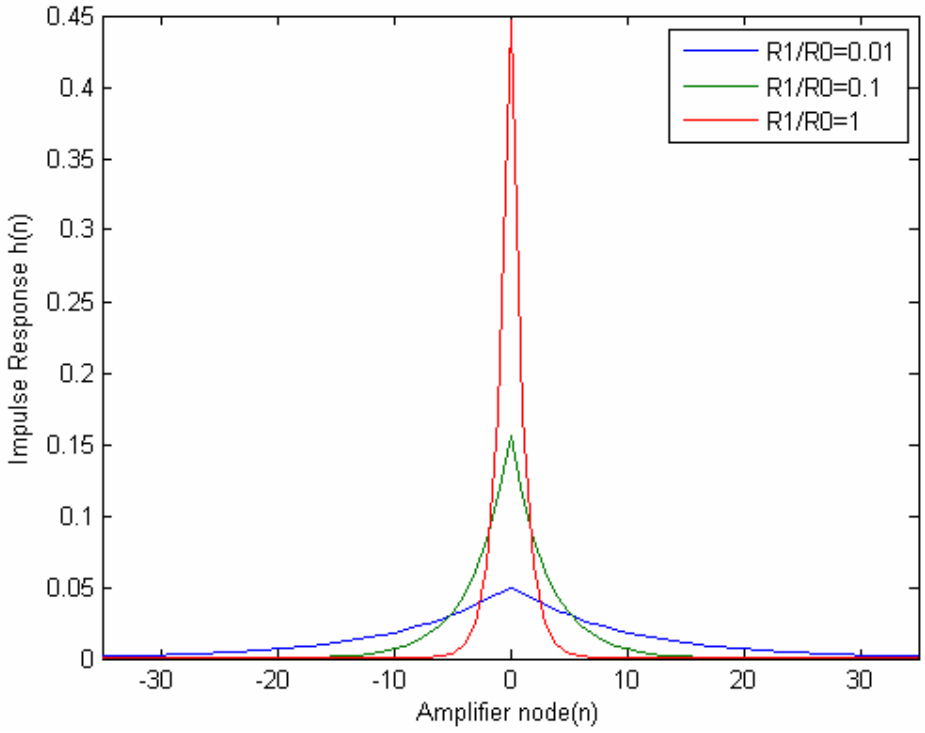


Figure 3. 12 Impulse response as a function of resistive ratio R1/R0 at node(0)

3.3.2 Error Correction Factor (ECF)

The parameter used to the averaging performance is error correction factor (ECF) [13]. The error correction factor is defined as ratio standard deviation of the original offsets and standard deviation of the input-referred offsets after averaging. Thus

$$ECF \equiv \frac{\sigma_{os}}{\sigma'_{os}} = \frac{g'_m(0)/g_m(0)}{\sigma(i'_{os})/\sigma(i_{os})} \tag{3.10}$$

Where σ_{os} (σ'_{os}), $\sigma(i_{os})$ ($\sigma(i'_{os})$) and $g_m(0)$ ($g'_m(0)$) represent standard deviation the input referred offset voltage, offset current and transconductance of the preamplifier before (after) averaging at the zero crossing node. Now let us derive the ECF for a spatial filter with the impulse response given by equation (3.9). Since the output of any filter is found by convolving its input with the impulse response, we have

$$g'_m(0) = \sum_{-\infty}^{\infty} g_m(n)h(0-n) = g_m \sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} h(n) \tag{3.11}$$

Where W_{ZX} is the width of linear active region of the preamplifier which can be expressed as $W_{ZX} = 2\sqrt{2}V_{eff}/LSB$ .The output noise current is given by

$$i'_{os}(0) = \sum_{-(W_n-1)/2}^{(W_n-1)/2} i_{os}(n)h(0-n) \tag{3.12}$$

which leads to the standard deviation

$$\sigma(i'_{os}) \equiv \sqrt{\overline{i'^2_{os}}} = \sigma(i_{os})\sqrt{\sum_{-(W_n-1)/2}^{(W_n-1)/2} h^2(n)} \tag{3.13}$$

Where W_n is the width of noise window of the preamplifier. Combining Equation (3.10), (3.11), (3.12) and (3.13), the ECF can be shown that

$$ECF = \frac{(1+b\cdot(1-2b^{(W_{ZX}-1)/2}))/(1-b)}{\sqrt{(1+b^2(1-2b^{(W_n-1)}))/(1-b^2)}} \quad \text{where} \quad b = e^{-|a\cosh(1+R_1/2R_0)|} \tag{3.14}$$

Figure 3.13 shows the error correction factor (ECF) respects to resistive ratio R1/R0. How accurate must be the ratio of R1/R0 to deliver near optimum benefits? The ratio is chosen larger than at the maximum point to prevent the gain loss. The resistive network causes the gain loss of the preamplifier as shown in Figure 3.14. The value of ECF will be higher if the value of R1/R0 is lower, but it also causes the gain loss of the preamplifier when the value of R1/R0 is lower. For example, if the ratio falls by 50% to 0.08, the ECF increases from 3.2 to 3.7 but gain loss increases from 3% to 11%. If rises by 50% to 0.24, the ECF also falls to 2.8 but gain loss approaches zero. Thus, a network with only roughly the right resistor ratio should yield close to optimum averaging. Consider W_{ZX} =35 and choose a ratio R1/R0=0.16 in our design. From the figure 3.13 and figure 3.14, the ECF is about 3.2 and the gain loss is only within 3% when the resistive ratio 0.16 is chosen.

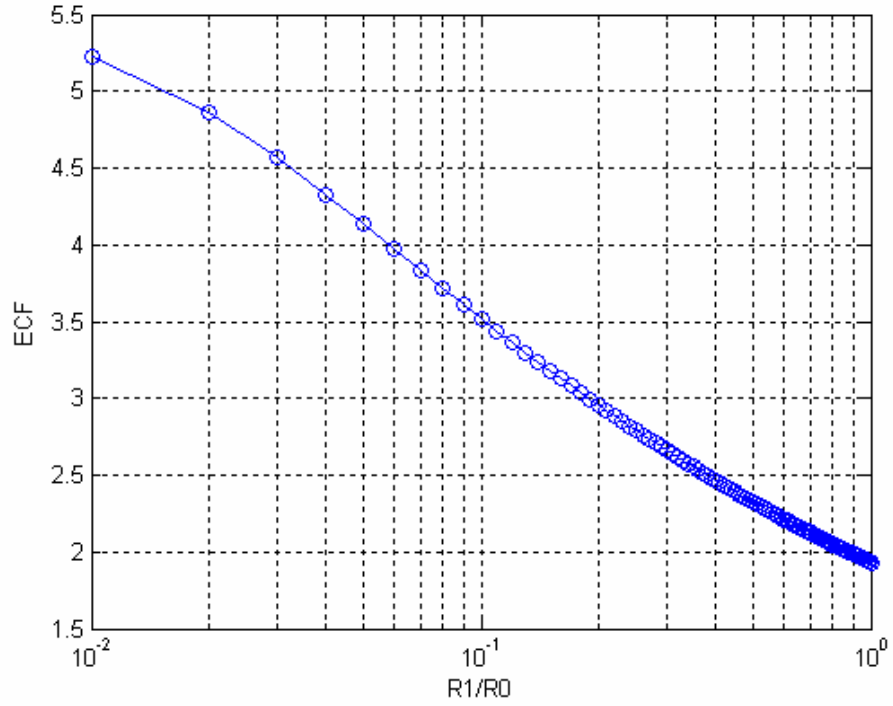


Figure 3. 13 The error correction factor verse resistive averaging ratio

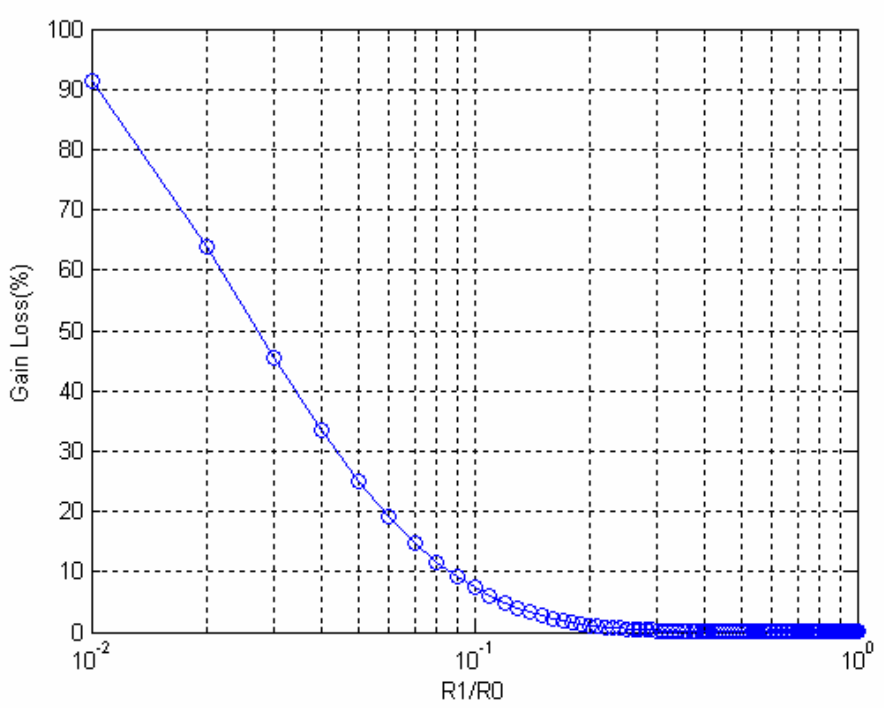


Figure 3. 14 Gain loss verse resistive averaging ratio

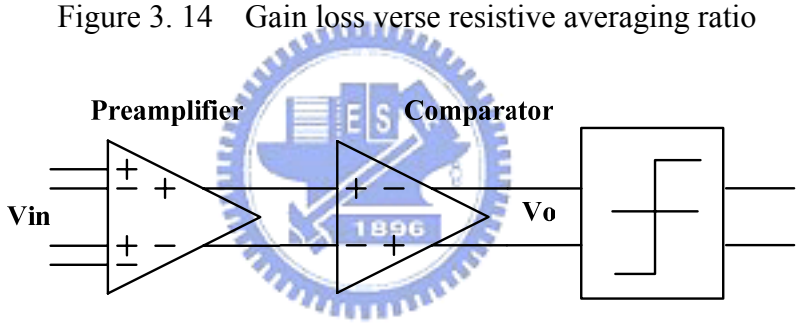


Figure 3. 15 Monte-Carlo simulation setup scheme

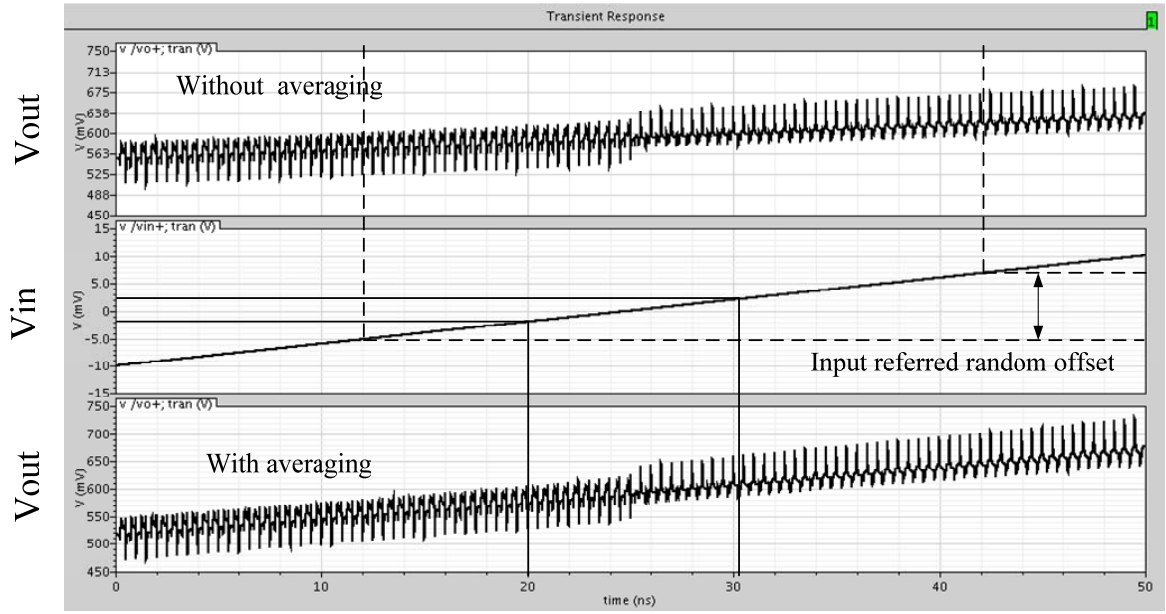


Figure 3. 16 The preamplifier Monte-Carlo analysis with and without averaging resistor

Monte-Carlo analysis is performed to verify the benefits of resistive averaging. Figure 3.15 shows the Monte-Carlo simulation setup scheme. The parameters for the device mismatch including threshold voltage mismatch and resistor mismatch are provided by foundry []. In the idea case with no transistor mismatch, the comparator output changes polarity when a slow ramp input cross the corresponding threshold. Figure 3.16 shows that the time the comparator changes polarity is randomly dispersed with respect to when the input cross zero. The preamplifier offset set voltage is 12mV when the preamplifier without averaging resistor. Using averaging resistor, the preamplifier offset reduce to 4.1mV. The simulation result is shown in Figure3.16; it is a composite plot of 60 Monte-Carlo transient analyses.

3.3.3 Nonlinearity Error and Compensation at the Edges

Finiteness of the array of preamplifiers poses unique problems at the edges of an

averaging flash A/D converter. Usually the preamplifier array comes to an end at the upper and lower limits of the analog full scale. This will disrupt averaging at the last few preamplifiers, because at the extreme nodes there is no longer an equal number of stimuli into the resistor network from both left and right. As shown in Figure 3.17 the vertical line that crosses the zero-crossing point at the right-hand extreme of full scale intercepts zero-crossings only in the upper half plane if there are no dummy zero-crossings. In presence of the lateral resistors, those intercept points contribute positive currents to the zero-crossing node and effectively pull the zero-crossing toward the center of the array. Unless the positive intercept points are balanced with negative ones from dummies or by distorting reference taps, all the zero-crossings within the range of half width of impulse response at each edge are pulled resulting a systematic INL curvature.

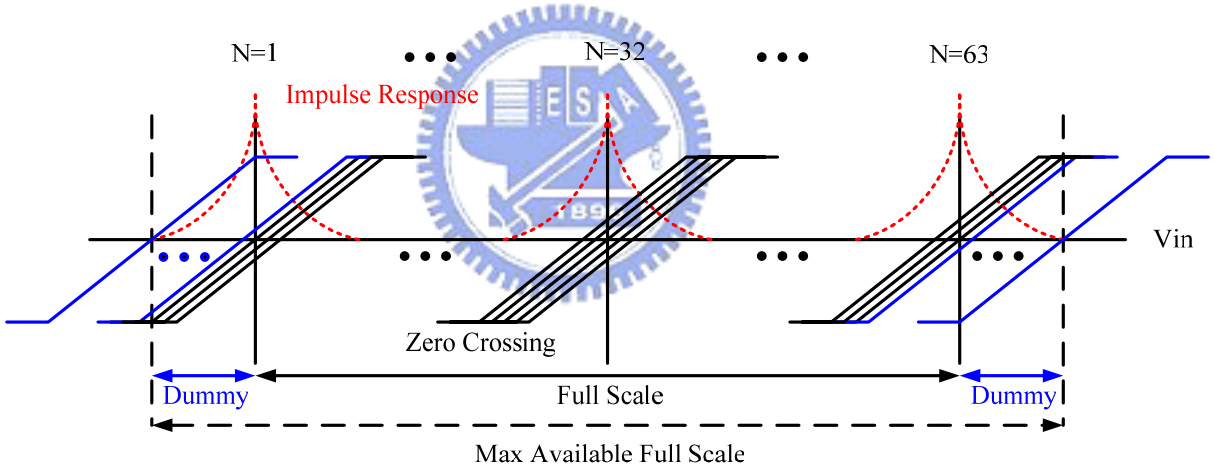


Figure 3. 17 Dummy preamplifiers to reduce edge effects

Linearity across the full scale requires that no distortion should build up at the edges. A straightforward solution is to add preamplifiers on either edge of the array to extend the averaging network by at least width of the impulse response, the extent of the interaction range [13]. Therefore, half number of dummy preamplifiers is attached at each end. The current flowing in averaging resistor shows a large bending at both ends, as shown in Figure 3.18

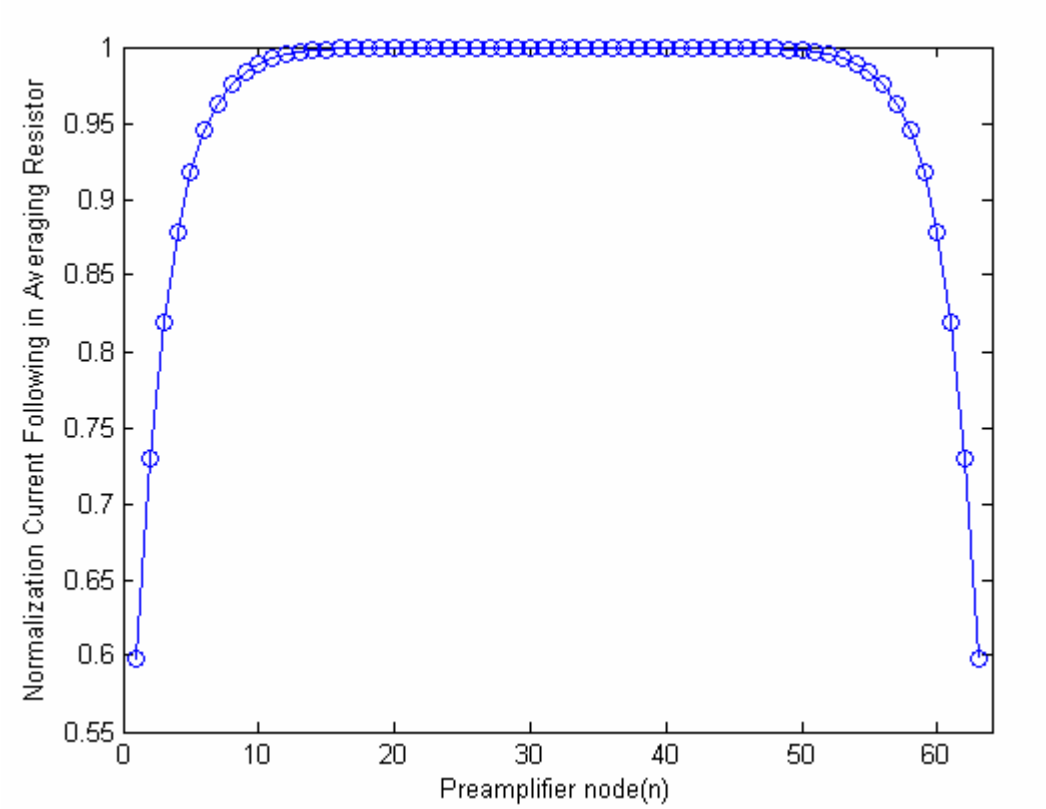


Figure 3. 18 The current flowing in resistive network shows the boundary condition

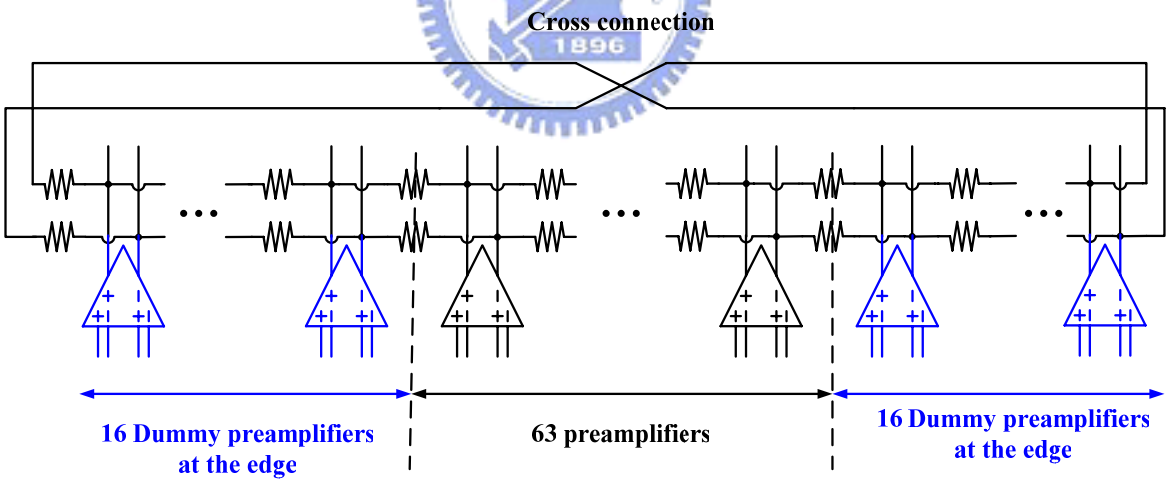


Figure 3. 19 Dummy preamplifiers with cross connection averaging

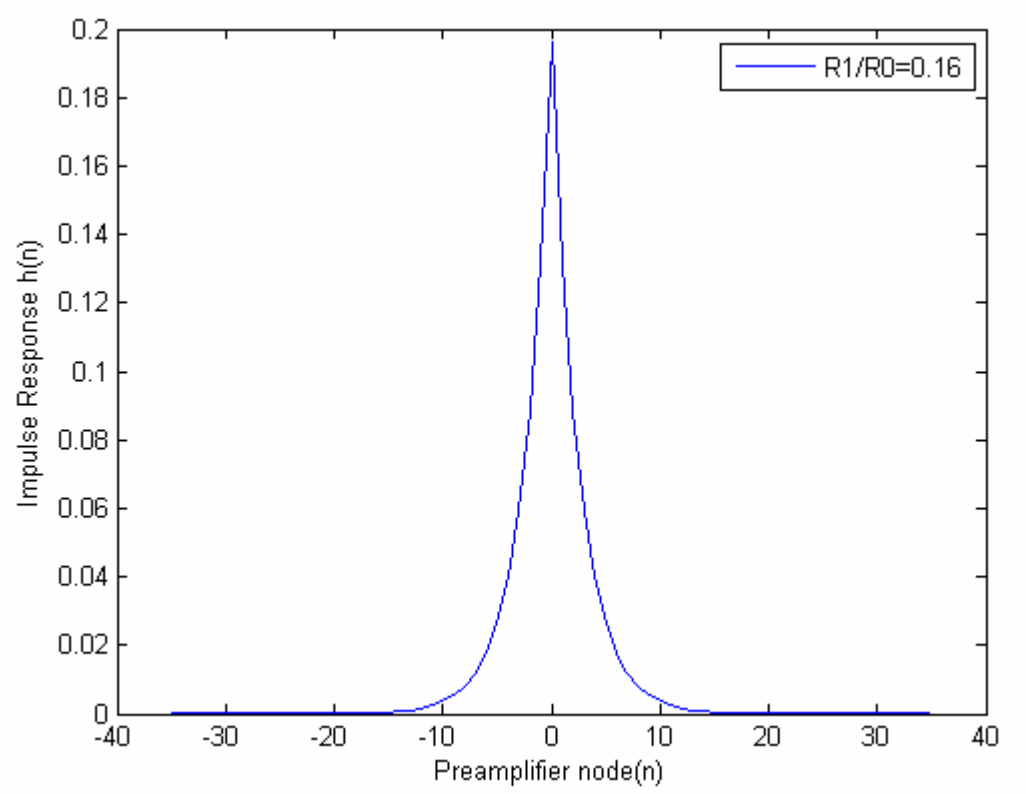


Figure 3. 20 Impulse response as a function of resistive ratio R1/R0=0.16 at node(0)

This bending is of a form as the low-to-high current in the lowest edge and the high-to-low current decreasing in the highest edge, causing the INL pattern at edge to go opposite direction. In order to keep the symmetry condition at the edge of preamplifiers, the dummy preamplifiers are added and the cross connection averaging resistor is adopted which is shown is Figure 3.19. The numbers of dummy preamplifiers are probably equal to the range of impulse response which is shown in Figure 3.20. In this design the range of impulse response of the averaging networking is about 16 dummy preamplifiers are enough to compensate the integral nonlinearity errors at the boundary condition. Figure 3.21 shows the simulation at the boundary condition with and without the dummy preamplifiers.

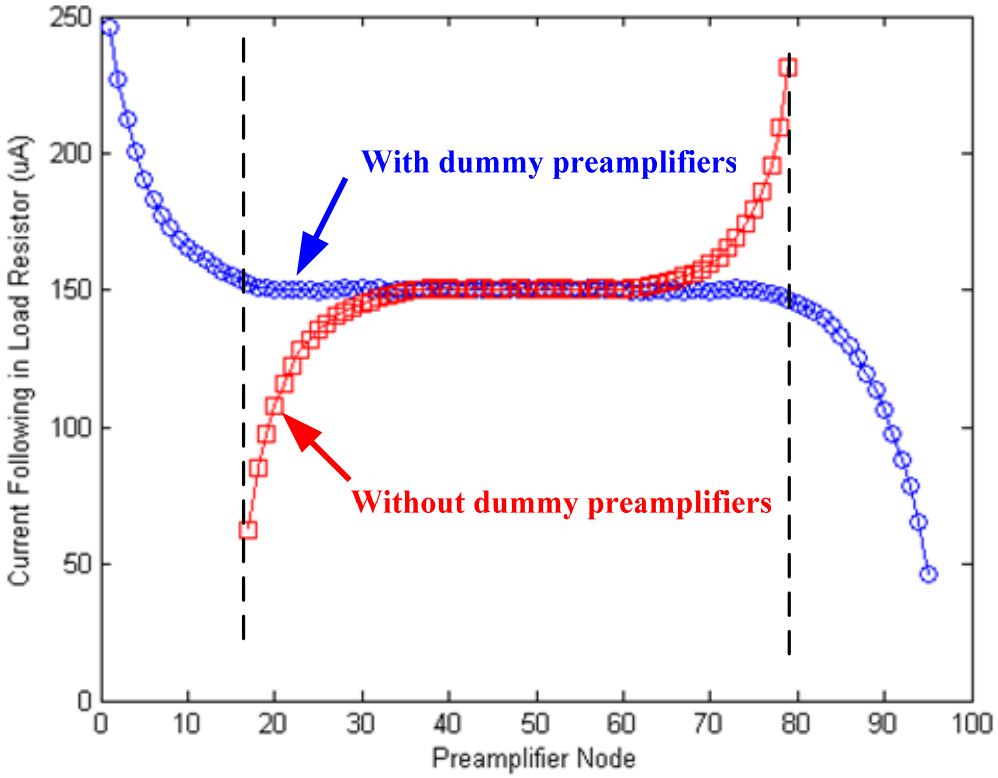


Figure 3. 21 Averaging current following in the load resistance

From this figure, the nonlinearity error is serous obviously at the edge of preamplifiers and the linearity range is extended with proper dummy preamplifiers at the boundary of preamplifiers array.

3.3.4 Power Saving in Preamplifiers Array

Averaging resistors are used in both preamplifiers and comparators in order to reduce the input referred offset. For unaveraged preamplifier, the standard deviation of input referred offset $\sigma(\Delta V_{os})$ is inverse proportional to the square root of the size (WL) of the input differential pair [14] as derived in Equation 3.11. With averaging resistors, the offset can be reduced by κ times. Therefore, for the same offset specification, the size of each preamplifier can be reduced κ^2 times compared with unaveraged one.

$$\sigma(\Delta V_{os}) \approx \sigma(\Delta V_{th}) \propto \frac{1}{\sqrt{WL}} \tag{3.15}$$

With the same preamplifier speed, overdrive condition and input-referred RMS offsets, the current consumption of the preamplifier is proportional to the size of the input differential pair is derived in Equation 3.12. Hence, the size reduction in preamplifiers also leads to power reduction and the power reduction factor is κ^2. In our averaging resistor design, the optimum κ is about 3 that is 9 times power reduction in a single preamplifier [15].

$$Speed \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{2I/V_{eff}}{2\pi(2/3)WLC_{ox}} \propto \frac{I}{WL} \tag{3.16}$$

Usually some dummy preamplifiers are required at the boundary to eliminate the linearity error due to the edge effect. Including the dummies, the total power dissipation in preamplifiers is scaled down as

$$\begin{aligned} \frac{P_{total,avg}}{P_{total,unavg}} &= \frac{N_{avg}}{N_{unavg}} \times \frac{P_{avg}}{P_{unavg}} = \frac{N_{avg}}{N_{unavg}} \times \frac{I_{avg}}{I_{unavg}} \\ &= \frac{N_{avg}}{N_{unavg}} \times \frac{(WL)_{avg}}{(WL)_{unavg}} = \left(1 + \frac{N_{dummy}}{2^n - 1}\right) \times \frac{1}{k^2} \end{aligned} \tag{3.17}$$

where $P_{total,avg}$ ($P_{total,unavg}$) represents the total power dissipation of the preamplifier array with (without) averaging resistors; N_{avg} (N_{unavg}) represents the number of the preamplifiers with (without) averaging resistors; P_{avg} (P_{unavg}) represents the power dissipation of a single preamplifier with (without) averaging resistors. N_{dummy} is the number of dummy preamplifiers and n is the resolution of the A/D converter. In our case, the total power of preamplifier array scaled down factor is 0.168 that is about 83% power reduction, exhibiting low power performance.

3.4 Digital Error Correction Technique

Comparators in a flash converter generate what is commonly known as a thermometer code. If a particular comparator's reference point is below the level of the input signal, the comparator's output is high**;** if the reference point is above the input, its output is low. It is easy to see why this code is called thermometer code. With an increasing input signal the number of ones is increasing. When everything is working ideally, the collection of comparator outputs should resemble a thermometer: all zeros above the input level and all ones below the input level. The zero-to-one transition point rises and falls within the input level. The thermometer code is translated to a final binary output word using the zero-to-one transition point to address a ROM. A high speed flash A/D converter with this type of the digital encoding structure typically suffers from two problems: bubble errors (or sparkles) in the thermometer code and metastability errors. The purpose of the digital encoding is to convert the comparator outputs into a 6-bits code word and to suppress the errors caused by the comparator metastability and bubble errors in the thermometer code. Thus, the digital encoding with the digital error correction is very important to achieve good resolution at high input frequencies.

3.4.1 Bubble Error Correction

Under extremely high input slew rate conditions, timing differences between the clock lines and signal lines can cause the effective sampling moments between comparators to be different. This can cause a bubble in the thermometer code where a one may be found among zeros. This is normally called a bubble in the thermometer code, because this error resembles bubbles in the mercury of a thermometer.

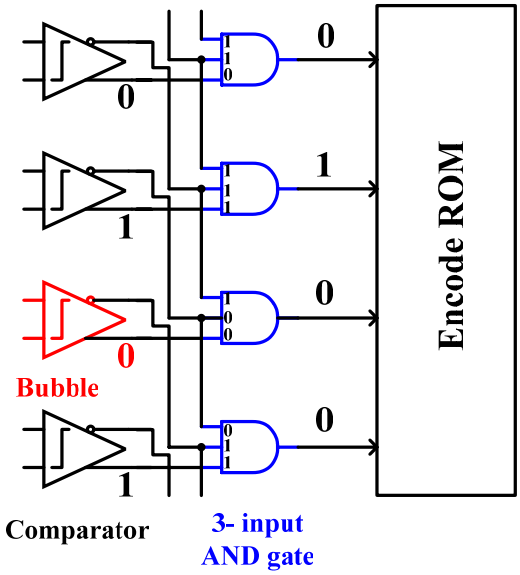


Figure 3. 22 Three input AND gate to solve a bubble error

Bubble errors result from three major sources [2]. First, the large overall input-referred random offset can switch the order of the two adjacent thresholds and create bubble errors. Second, the slew-dependent sampling and clock dispersion between comparators cause bubble errors. Finally, the propagation-delay variations through the preamplifier stage as a result of limited bandwidth and fast input frequency worsen the bit-error rate to generate bubble errors.

To overcome this problem a bubble correction method can be used. A common method of suppressing bubbles is to use what amounts to a three-input AND gate to address the ROM.

For example, two zeros have to be found above a one to cause the ROM line to go high. Then a sample correction of a bubble error in the thermometer code can be corrected as shown in Figure 3.22.

3.4.2 Metastability Error Correction

When the applied input signal is near the reference voltage for a comparator, the comparator output may be undefined at the end of evaluation time and then metatstability in a

flash converter can occur. Since input signal is typically continues amplitude, there is always a finite probability that voltage difference cannot be amplified sufficiently in the time allotted for comparison. If the output is not sufficiently amplified, indeterminate digital signals are propagated to the encoder logic, leading to errors.

The approach of reducing the metastability consists in introducing pipeline latches immediately after the comparator outputs and before the logic decoder, increasing the regeneration gain of the comparator. The n-bits flash A/D converter architecture with m levels of pipeline latches requires $(2^n-1)m$ latches as shown in Figure 3.23. Clock loading can be increased substantially as a clock signal must be distributed to each of these latches and all of the latches in the pipeline toggle at the sampling frequency, dissipating large power. To reduce error rates with less power and area, the number of latches must be reduced and the clock loading decreased [16].

In order to increase the comparator resolution time without inserting stages of 2^n-1 pipeline latches at the output of the comparators, the metastability error propagation from a metastable comparator must be handled by the encode circuitry. Figure 3.24 shows the metastability error propagation for a flash A/D converter with binary encoded, n-channel pull-down binary-encoded ROM. In this example, zeros in the ROM are implemented with an n-channel pull-down and ones with a no connection. Due to the two undefined word lines in the ROM, the undefined comparator outputs can propagate to the pull-down transistors and the bit lines in the ROM. As a example, for the two words “100000” and “01111” all of the propagated output bits will be undefined, leading glitches in the output waveform with as many as n bits in error.

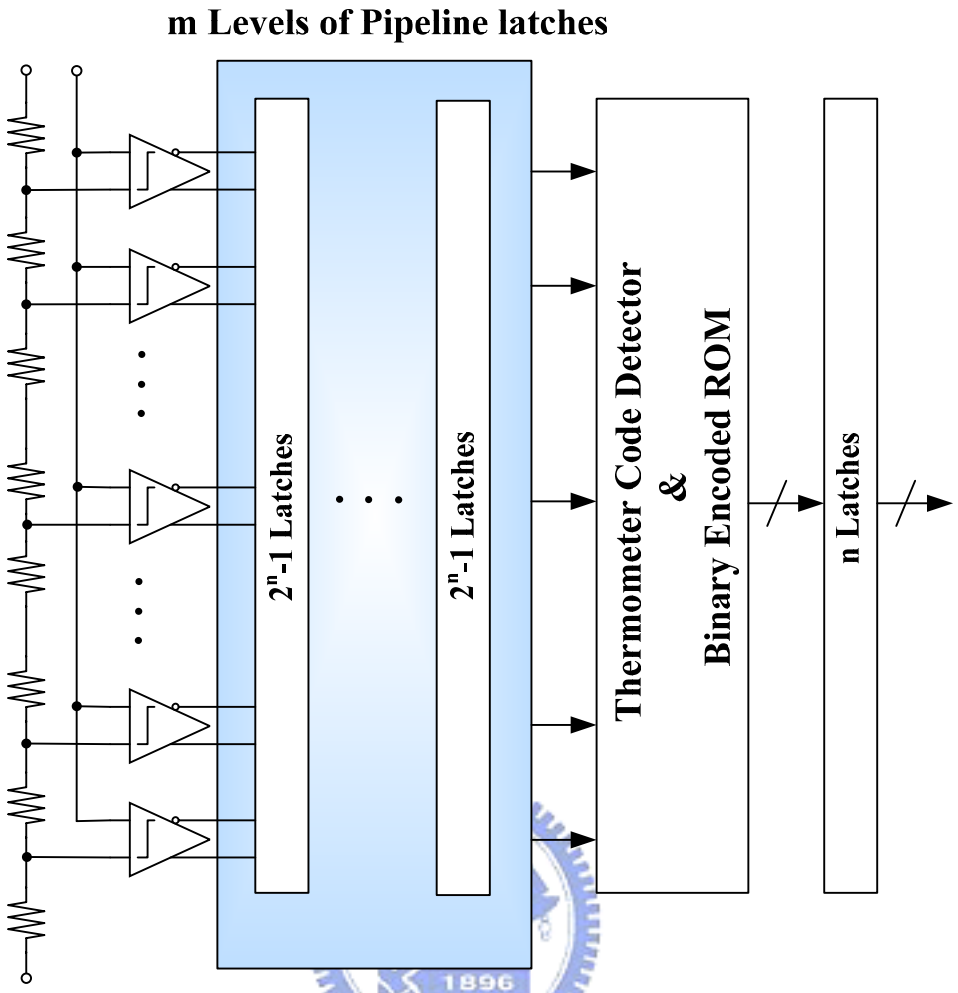


Figure 3. 23 Flash A/D converter with comparator pipelining to reduce metastability

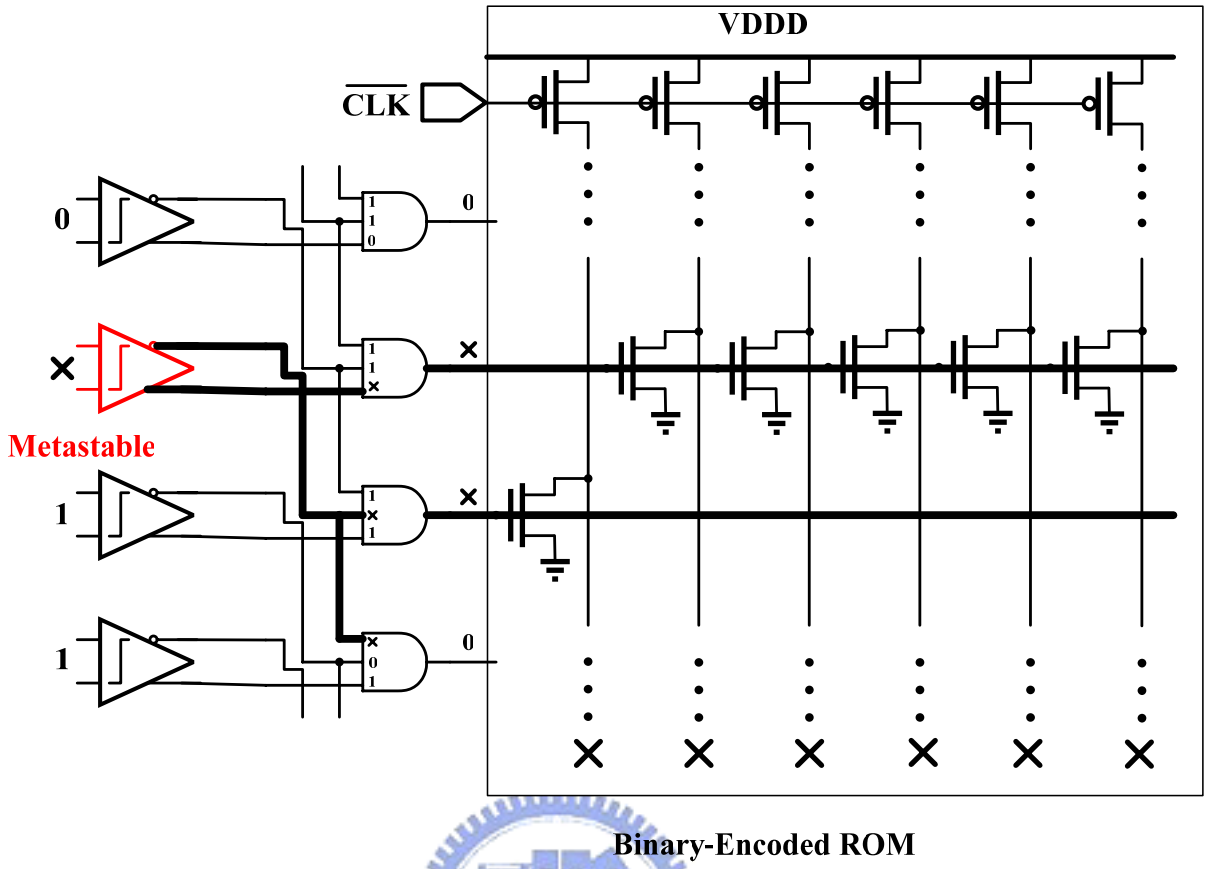


Figure 3. 24 Error propagation in binary-encoded ROM and output bits

In order to overcome metastability problem, a error correction method can be adopted. This method of reducing the metastability errors is to use the auxiliary circuits and the Gray encoded ROM based architectures as shown in Figure 3.25.

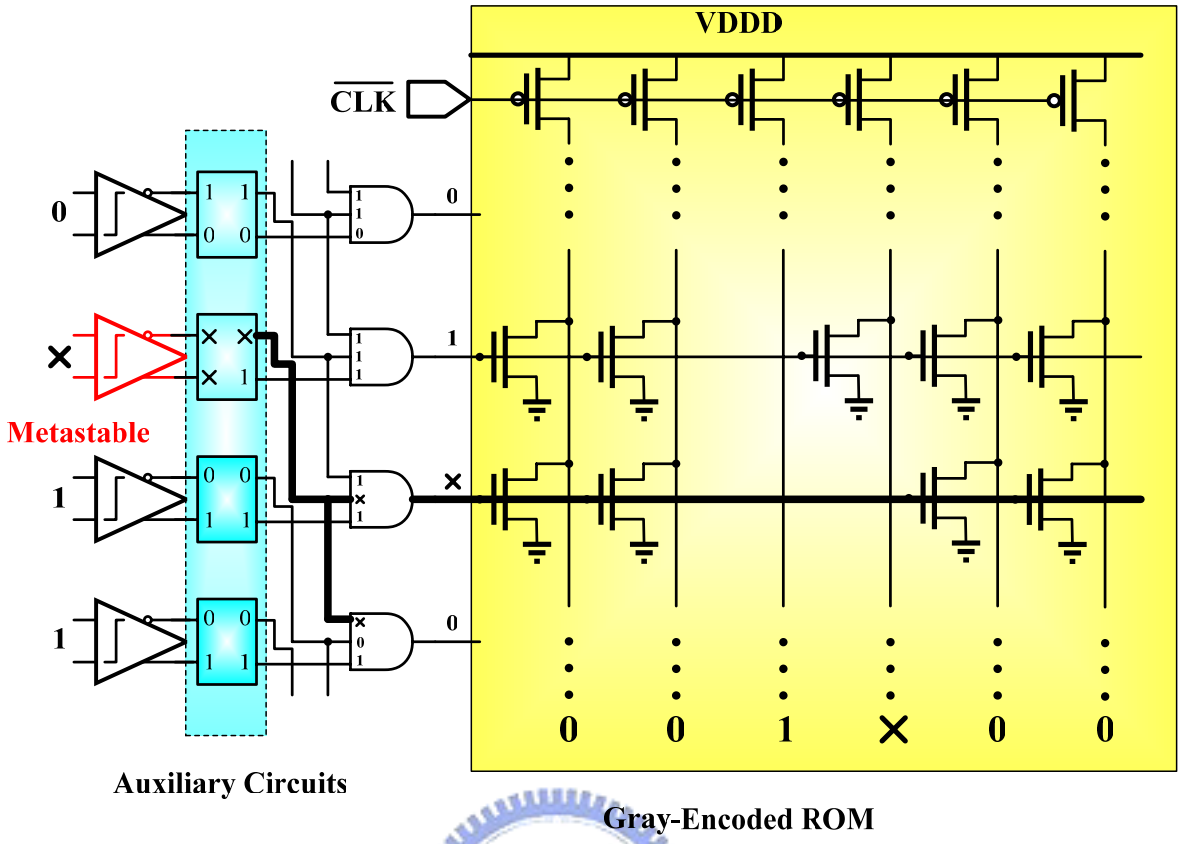


Figure 3. 25 Single bit error in ROM output with the auxiliary circuits and Gray-encode ROM

With stable outputs for metastable comparators, the outputs propagate to the ROM as follows. If both comparator outputs are high when the encoded ROM is clocked, two adjacent word lines will be turned on the ROM. This will cause large errors in a binary-encoded ROM because the output bits will be the logic AND of the two words. However, if a Gray-encoded ROM with the auxiliary circuits that guarantees at least one valid output is used, adjacent ROM words differ by only one bit and the resultant output word will be the word with more zeros.

Since metastability errors only occur with the analog input at a boundary between two output words, either output code can be a considered correct. The worst case for the encoded ROM is a signal comparator output settling as the ROM is clocked. The undefined comparator output is passed to the ROM as a word line high and as adjacent line undefined as

shown in Figure 3.25. Due to the Gray code, the logically AND output words leave only one output bit undefined. Thus, the Gray-encoded ROM is effective solution to reduce the metastability errors caused by an undecided comparator.

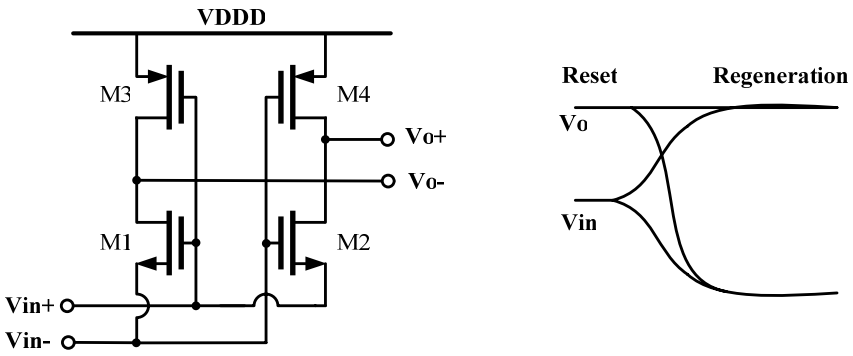


Figure 3. 26 Implementation of the auxiliary circuit

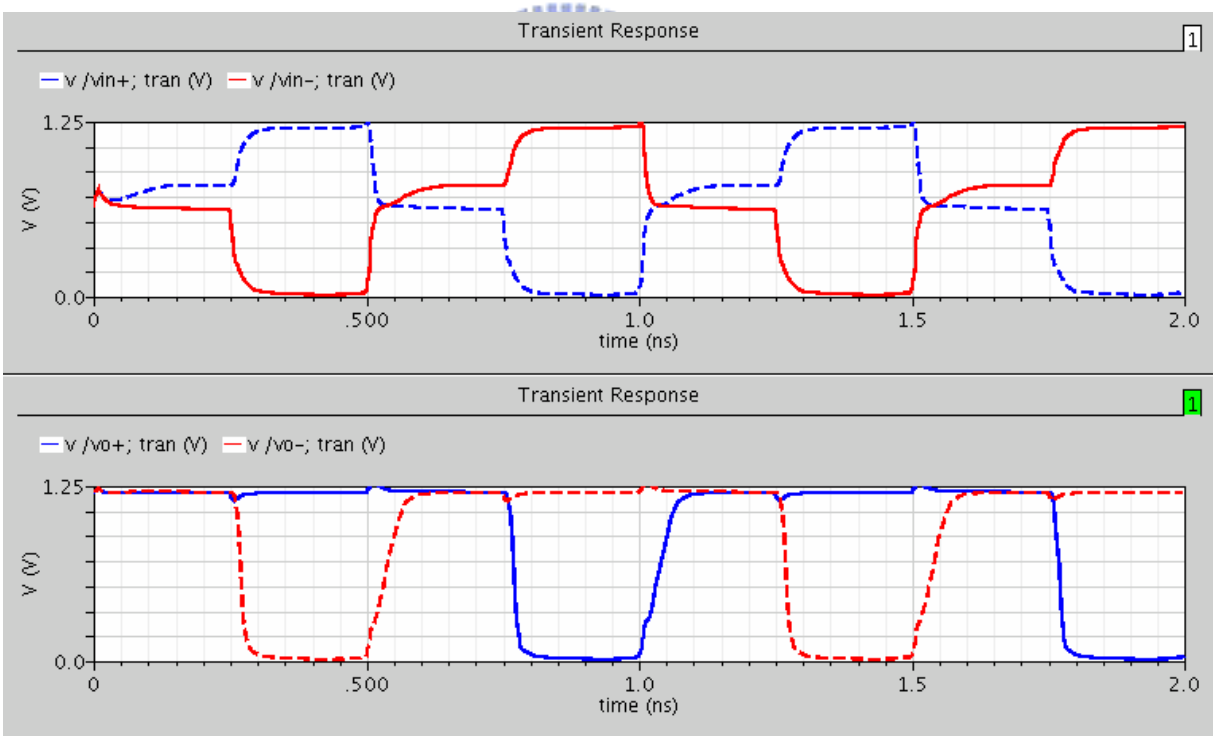


Figure 3. 27 Simulation result of the auxiliary circuit at 2GHz operation

Figure 3.26 shows the auxiliary circuit guarantees at least one valid output and used to valid high outputs for metastable inputs. This circuit is used in arbiter circuits with asynchronous inputs to avoid undefined output states. When the inputs from the comparator are intermediate

and equal, the device M3 and M4 are on and hold the outputs, Vo+ and Vo-, high. After the input voltages separate by more than one threshold voltage, one of the outputs is pull low by the input. The simulation result of the auxiliary circuit at 2GHz operation is shown in Figure 3.27.

The power consumption and area are decreased because the auxiliary circuits and the Gray-encoded ROM based architectures are used and the $(2^n-1)m$ pipeline latches after the comparator outputs are removed.

With the sample-and-hold, interpolation, averaging and digital error correction technique, the proposed A/D Converter achieves the goal of high speed conversion and low power consumption.

3.5 Resistor Ladder Design

The preamplifier amplifies the difference between the input voltage and its reference voltage. The reference voltages are generated by a resistor ladder. The ladder network divides the converter reference voltages in equal reference voltages for each preamplifier. One important source of errors in flash A/D converter is caused by the capacitive feedthrough of the high frequency input signal to the resistor reference ladder. The resistance value of the ladder must be small to reduce feedthrough and then a small resistance will cause high power consumption. A model is given to calculate the maximum allowed reference ladder resistance for a given shift in the reference voltages [17]. The calculation model is shown in Figure 3.28.

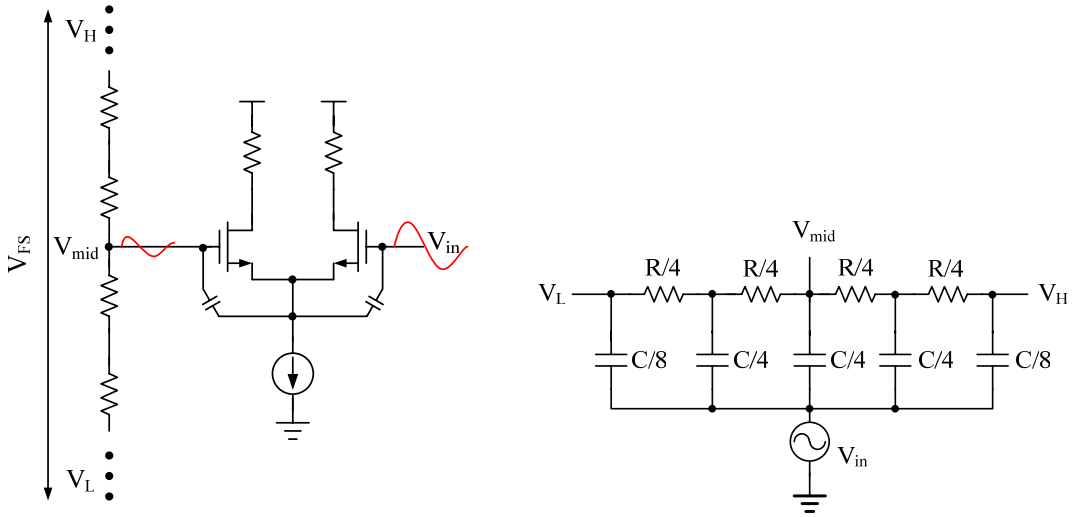


Figure 3. 28 Calculation model to derive the maximum ladder impedance

Consequently, the voltage at each tap of the ladder network can change substantially from its nominal DC value, degrading the converter performance especially at high input frequencies. The feedthrough from the input to the midpoint of the ladder is given by

$$\frac{V_{mid}}{V_{in}} = \frac{\alpha(\alpha+32)}{\alpha^2+32\alpha+128}, \quad \text{with } \alpha = \pi f_{in} RC \tag{3.18}$$

If it is assumed that α << 1, equation 3.18 can be simplified and the maximum reference ladder resistance for given feedthrough can be calculated by

$$R_{MAX} = \frac{\frac{4}{\pi}\frac{V_{mid}}{V_{in}}}{f_{in}C} \tag{3.19}$$

Where C is the total capacitance from the input to the resistive ladder and f_{in} is the input frequency. With this formula, the maximum ladder resistance can be calculated for which the feedthrough does not degrade the performance. This maximum ladder resistance gives rise to certain minimum power consumption in the reference ladder. This is taken into account in the global optimization. The total resistance of the ladder is approximately 752.

3.6 Preamplifier Design

The preamplifier stage should be wideband and provide sufficient gain to overcome the input-referred offset and kick-back noise from the comparators. The preamplifier is an optimized combination of two differential amplifier pairs with resistances as load, as shown in Figure 3.29. To achieve good performance over the whole input-range the bandwidth of the preamplifier must be wide. This is due to the problem of variable signal delay caused by the parallel structure of the different comparators (also called dispersion). This is an inherent problem of the high speed A/D converters.

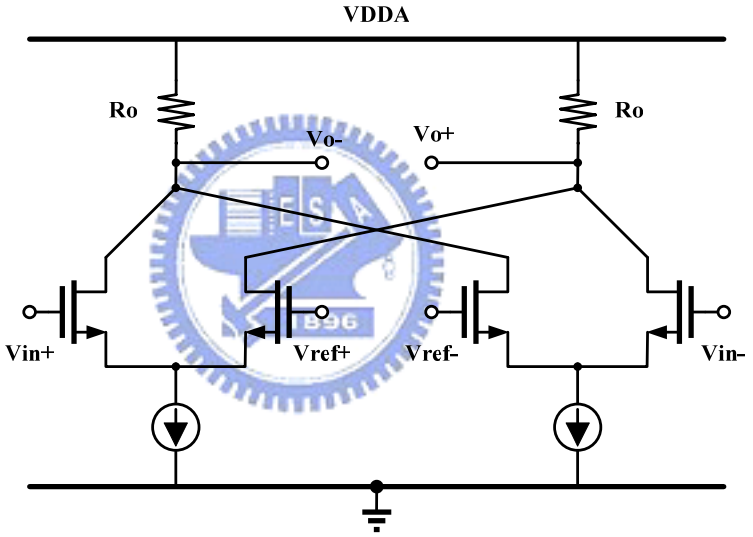


Figure 3. 29 The wideband preamplifier schematic

Suppose the high frequency sinusoidal signal is applied to an amplitude-limiting preamplifier of the A/D converter. This amplitude limitation results in variation of delay times of zero crossing of the differential stages. Each preamplifier sees a different section of the sinusoid and so there is a large variation in slope seen by each preamplifier. This slope is dependent on the level at which the input signal is equal to a reference voltage level. The variable slope introduces a variable delay of the zero crossings of the output signal. Each preamplifier can be modeled by a first order RC network [3]. The model used to calculate the

signal-dependent delay is shown in Figure 3.30. The response of such a network differs for different input slopes. This difference leads to a third order distortion, which can limit the dynamic performance of the high speed converter if the bandwidth of the preamplifier is not high enough.

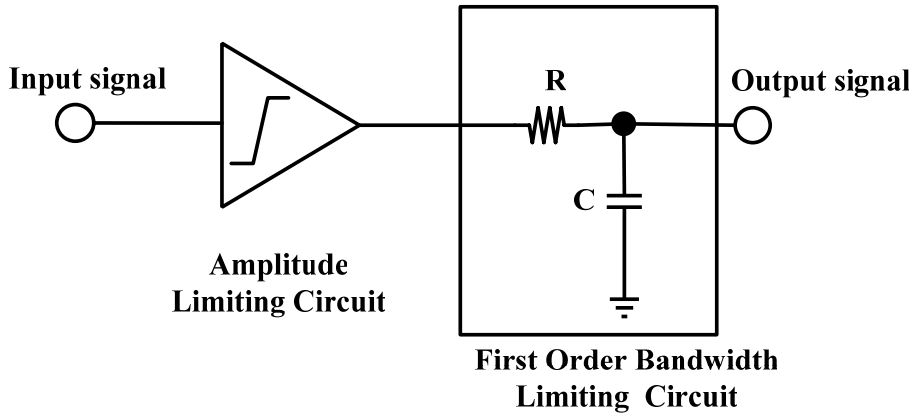


Figure 3. 30 The nonlinear model of a limiting preamplifier stage

To overcome this signal-dependent delay resulting in distortion a limitation on the bandwidth versus the input signal frequency of the preamplifier can now be calculated and the result of this calculation is described by the following output equations [18].

$$V_{out} = \sqrt{\tan^2 \eta + 1}\sin(\omega t + \eta) + \frac{2gf_{in}}{3\pi f_{bw}}\cos 3\omega t \qquad (3.20)$$

with

$$g \approx \exp(-0.5((V_{lr} f_{bw})/(V_{fs} f_{in})) - 1) \quad \text{and} \quad \tan\eta = \frac{3}{8\pi}\omega\delta t_d$$

Where V_{lr}, f_{bw}, V_{fs}, f_{in} and δt_d represent the input linear range, bandwidth, full scale range, input frequency and delay variation. In Figure 3.31 the results of the calculations are ploted. In this design, the third-order distortion must be less than 40 dB and the overdrive voltage is 0.2V. The Preamplifier Bandwidth / Input Frequency ratio must be higher than 3. The simulation result of the wide bandwidth preamplifier is shown in Figure 3.32.

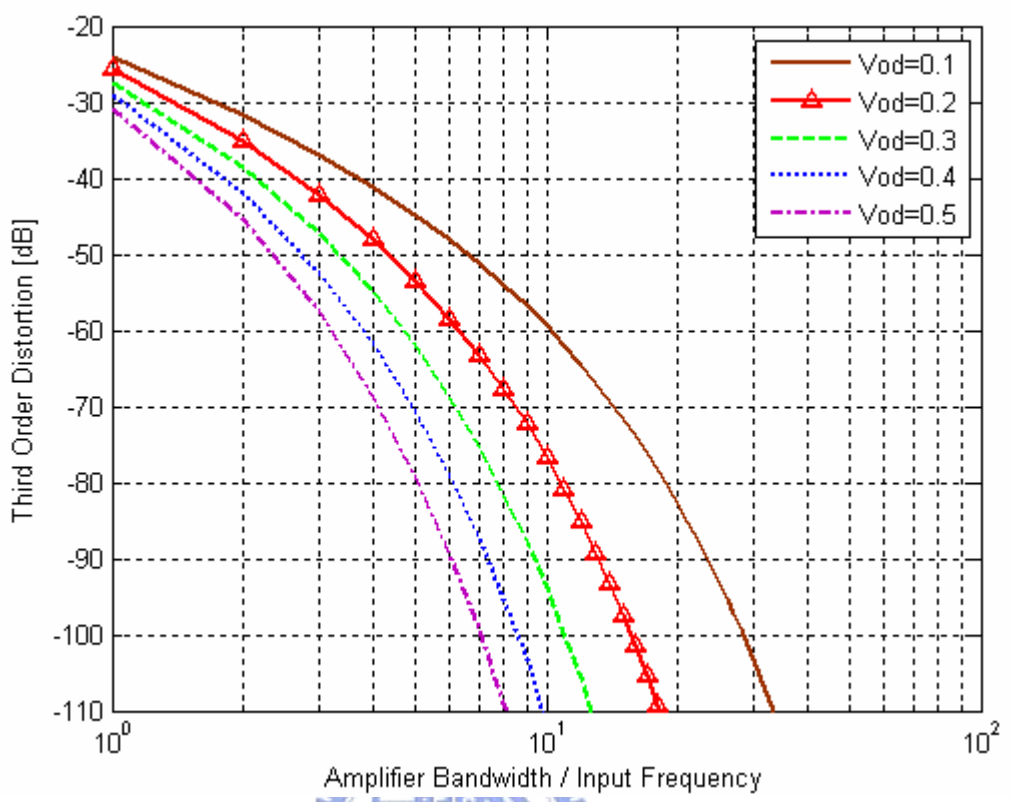


Figure 3. 31 Third-order distortion versus bandwidth/input frequency

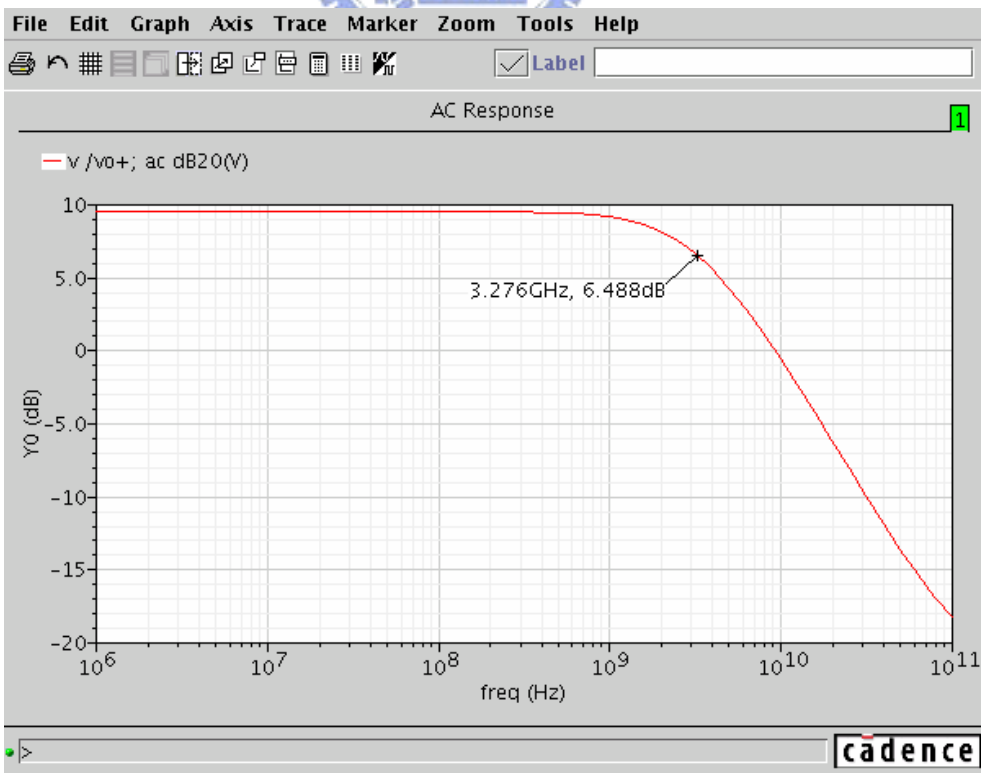


Figure 3. 32 The simulation of the wide bandwidth preamplifier

From the figure 3.32, the value of gain is 9.4dB and the value of bandwidth is 3.2GHz. The 9.4 dB gain of the designed preamplifier can reduce the comparator input referred offset and the 3.2GHz bandwidth design can keep the third-order distortion less than 40dBc when the input signal is near the 1GHz.

3.7 Comparator Design

After the preamplifier, the comparator regenerates the amplified input difference into valid digital logical levels. The comparator used in high speed converter is a very fast regenerative structure. In order to cope with both the static offset due to mismatch and the dynamic offset caused by the clocking- and latch-action of the comparator itself, the architecture must be low kick-back comparator. To obtain a low kick back effect in comparators and at the same time having a large CMOS logic output swing the circuit shown in Figure 3.33 can be used [3][19]. In this comparator system the input differential stage M1 and M2 is loaded with a current mirror consisting of M3, M4 and M5, M6. The output of this current mirror is applied to comparator stage consisting of M8 and M9 with the reset transistor M7.

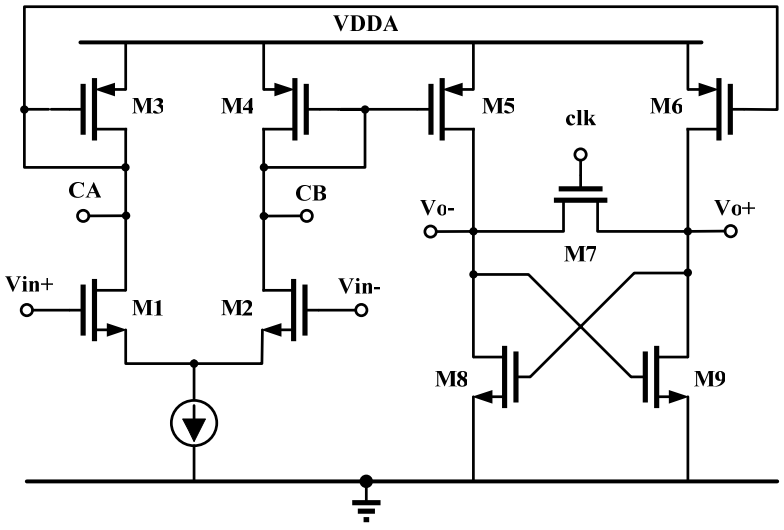


Figure 3. 33 Low kick back comparator schematic

During reset mode, transistor M7 shorts the drain of M8 and M9. The output voltage is equal to the gate-source voltage of these devices. The input stage sees as a load the diode connected transistors M3 and M4. At the moment transistor M7 is switched off, then the cross-coupled differential stage M8 and M9 start making a comparison with a large regenerative gain. As a result a output signal appears at the drain of M8 and M9. In case a high level is obtained then for example current mirror M5 connects to the output to VDDA. The diode input load remains roughly at same level with small input signals. No kick-back effect is found with this connection.

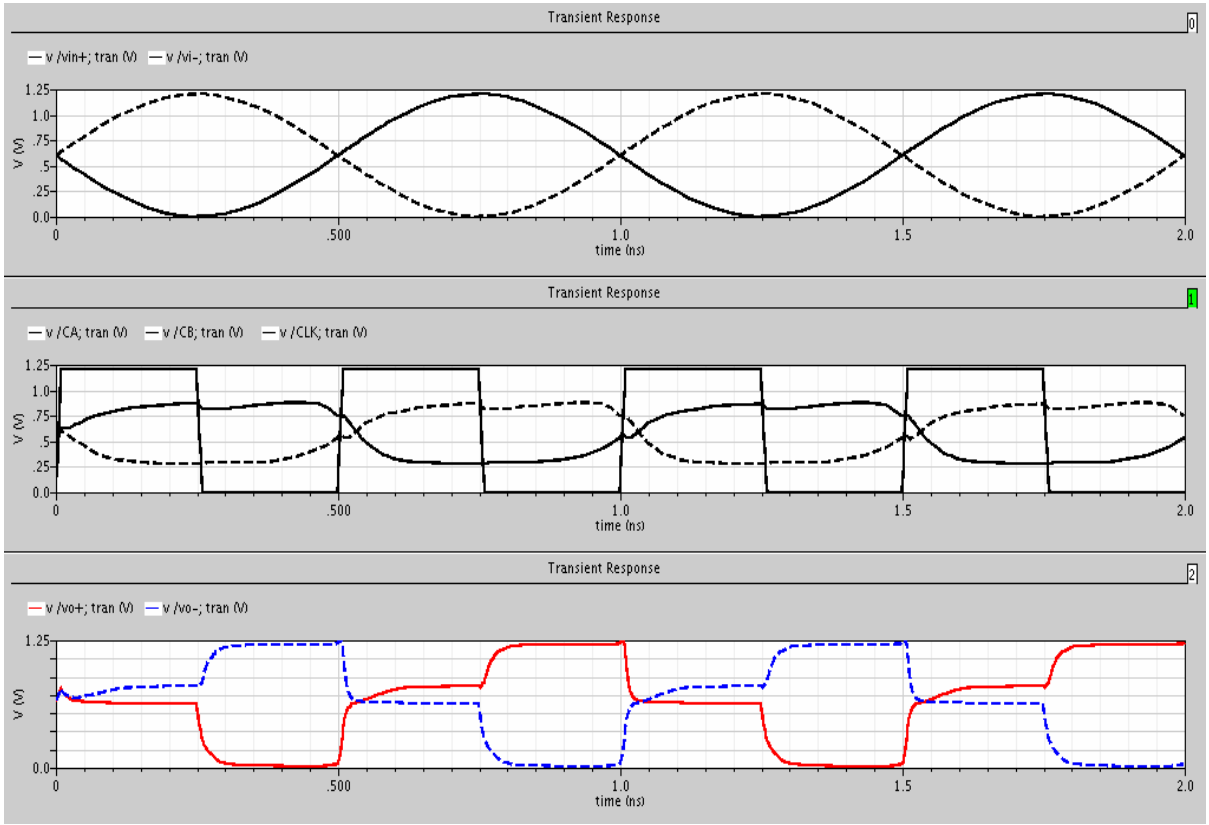


Figure 3. 34 Comparator overdrive test

The comparator speed is dominated at the output pole of the cross-coupled pair which is given by

$$P_{REG} = \frac{g_{m,NMOS}}{C_{Load}} \tag{3.21}$$

The comparator overdrive test is shown in Figure 3.34. The comparator can perform very well at 2GHz operation.

3.8 Digital Logic Design

The digital logic circuit is consisting of the auxiliary circuit, three-input AND gate, Gray-encoded ROM, true single phase clock flip-flop [20] and Gray-to-Binary decode. The outputs of the comparators constitute what is known as thermometer code. With using the digital logic circuit, the thermometer code can be converter into a binary code and in the meanwhile the bubble errors and metastability errors can be reduced by the auxiliary circuit, three-input AND logic and Gray-encoded ROM, which is introduced before section.

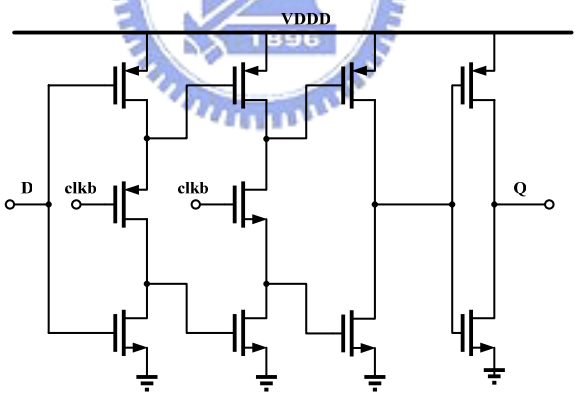


Figure 3. 35 The schematic of true single phase clock flip-flop

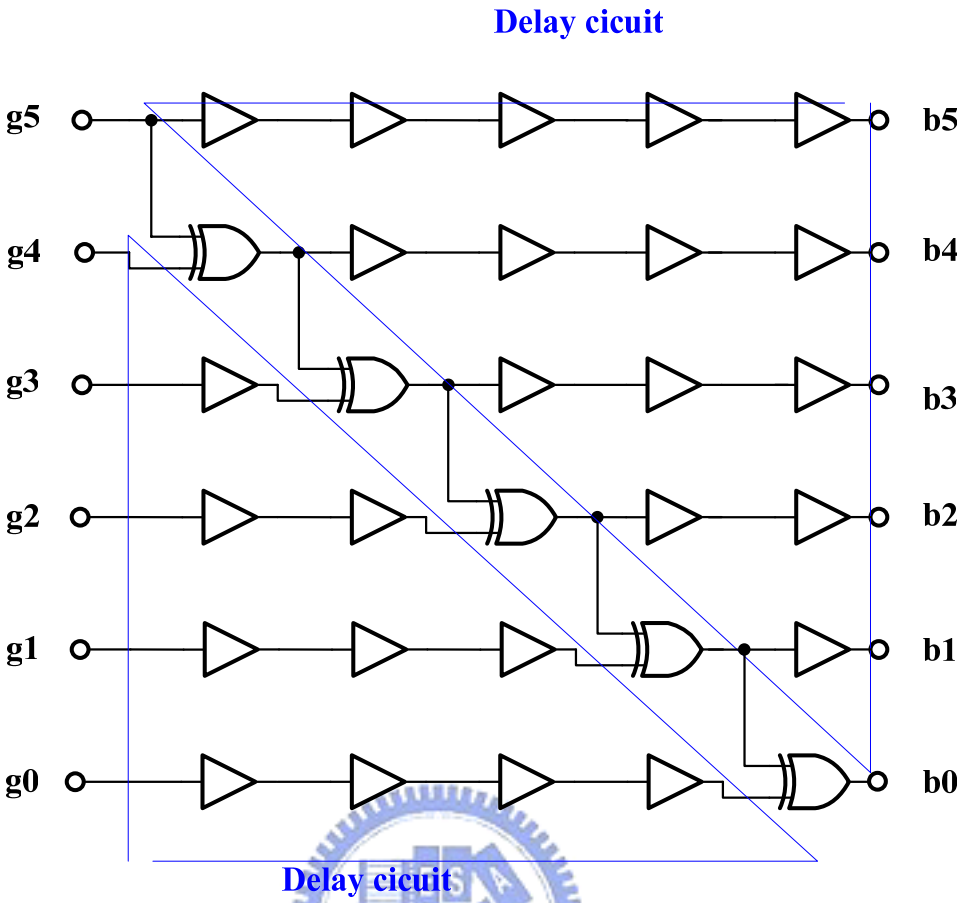


Figure 3. 36 Gray-to-Binary decoder with delay circuits

To operate at 2 GHz sampling rate and beyond, the flip-flops are implemented with true single phase clocked (TSPC) circuits which are connected after the Gray-encoded ROM. The outputs of Gray-encoded ROM are held for a whole clock period with a high-speed TSPC flip-flop. The schematic of the TSPC flip-flop is shown in Figure 3.35. The Gray code is converter into a binary code by the Gray-to-Binary decode. The Boolean functions of Gray-to-Binary decoder is shown blow

$$
\begin{aligned}
b_5 &= g_5 \\
b_4 &= g_4 \oplus g_5 \\
b_3 &= g_3 \oplus g_4 \oplus g_5 \\
b_2 &= g_2 \oplus g_3 \oplus g_4 \oplus g_5 \\
b_1 &= g_1 \oplus g_2 \oplus g_3 \oplus g_4 \oplus g_5 \\
b_0 &= g_0 \oplus g_1 \oplus g_2 \oplus g_3 \oplus g_4 \oplus g_5
\end{aligned}
\tag{3.22}
$$

The Gray-to-Binary decoder is consisting of the XOR gates with delay cells as shown in Figure 3.36. The delay cells are added to match the delay mismatch between the signal paths.

3.9 Clock Generator Design

In high speed A/D converter, clock jitter randomly modulates the periodic sampling instants of the S/H. Non-uniform sampling raises the noise floor of the digitized system, degrading signal-to-noise ratio (SNR). Clock jitter is increasingly a concern relative to the short period of high-speed A/D converters [21]. Given a sinusoidal input waveform with amplitude A and radian frequency ω, SNR due to clock jitter only is

$$SNR = 10 \cdot \log\left(\frac{A^2/2}{A^2\omega^2\delta T^2/2}\right) = -20 \cdot \log(\omega \cdot \delta T) \qquad (3.23)$$

where δT is the rms clock jitter. According to Equation 3.18, to obtain SNR of 38 dB (the ideal SNR for 6-b quantization of a sine wave) at input frequency of 1GHz, the rms clock jitter should be less than 2 ps.

Figure 3.37 illustrates how the buffering is implemented for the clock with the transmission gate and CMOS latches. The clock generator must be designed to have a minimum numbers of buffer stages and sharp transition in order not to introduce large jitters. The simulation result of the clock generator is shown in Figure 3.38. If the clock generator does have the transmission gate and CMOS latches, the cross points of the CLK and CLKB vibrate up and down to cause large jitters. If the clock generator adopts the transmission gate and CMOS latches, the cross points of the CLK and CLKB vibrate smooth to get small large jitters.

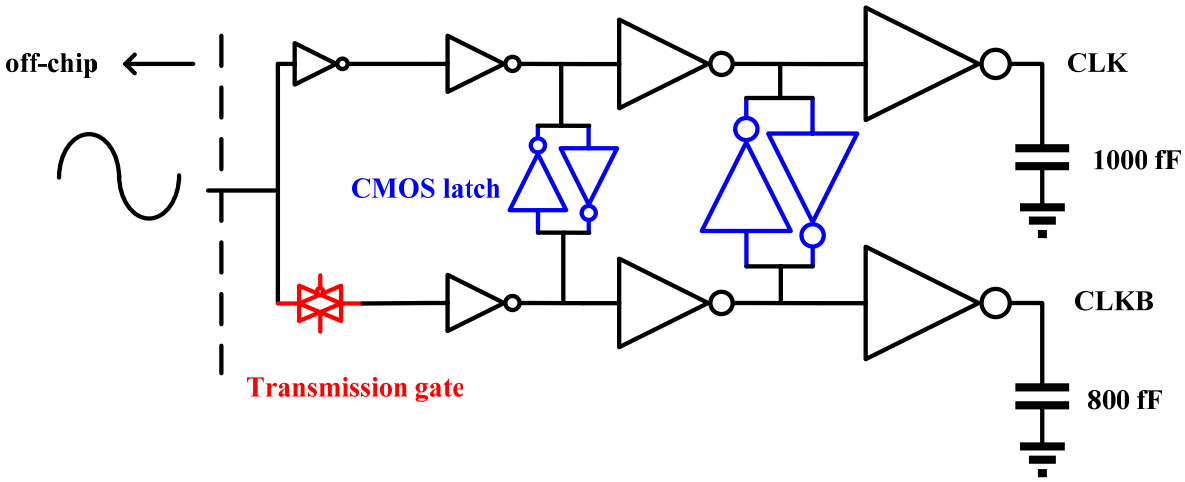


Figure 3. 37 Clock generator with transmission gate and CMOS latches

The CLK path connects to sample-and-hold and comparators with the loading of 1000fF. The CLKB path connects to digital logic including sample-and-hold, AND gates, ROM and TSPC flip-flops with the loading of 800fF.

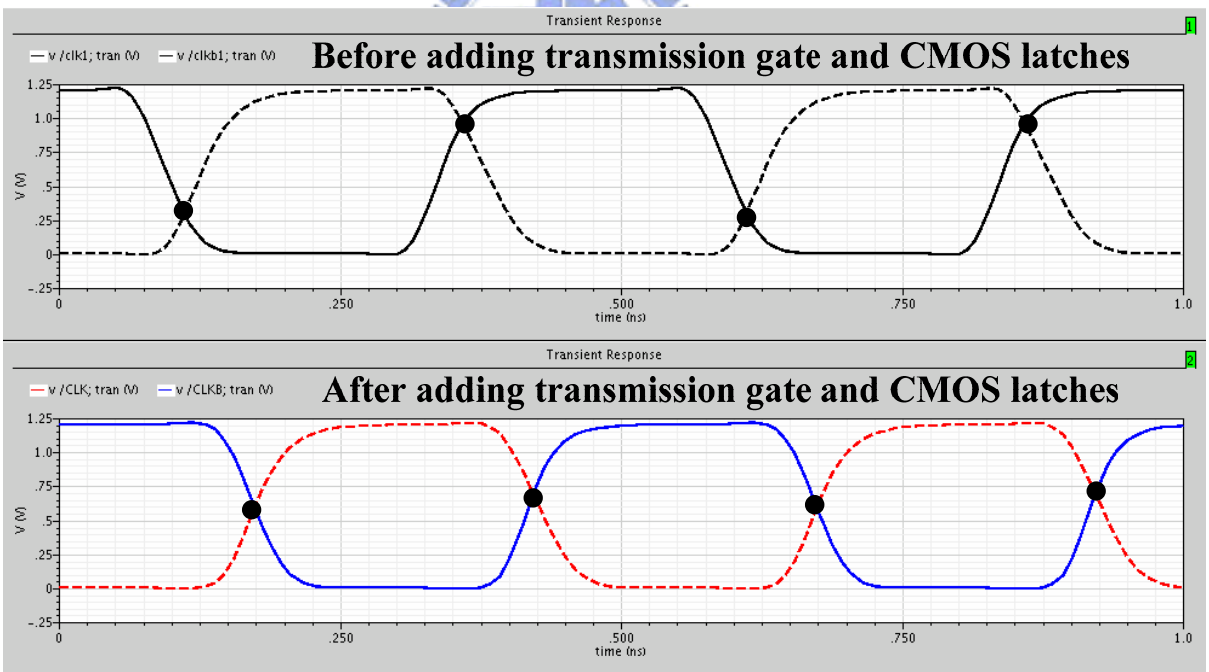


Figure 3. 38 The simulation of the clock generator

3.10 Simulation Results

The overall A/D converter circuit simulation for two versions of the A/D converter will be shown in this section. The static performance simulation in time domain analysis of whole A/D converter and the dynamic performance simulation in frequency domain analysis of whole A/D converter are presented. The static performance includes the differential -nonlinearity (DNL) and integral-nonlinearity (INL). The dynamic performance includes the signal-to-noise-and-distortion ratio (SNDR), spurious-free dynamic range (SFDR) and effective number of bits (ENOB). The first version A/D converter circuit design has some problems due to improper conditions at the edges of the preamplifiers. After improving circuits, we get the second version A/D converter.

3.10.1 Static Performance Simulation

The static performance of first version A/D converter with interpolation and averaging techniques is shown in Figure 3.39. The DNL is less than 1.47LSB and INL is less than 1.83 LSB. The static performance of second version A/D converter with interpolation and averaging techniques is shown in Figure 3.40. The DNL is less than 0.1LSB and INL is less than 0.14 LSB.

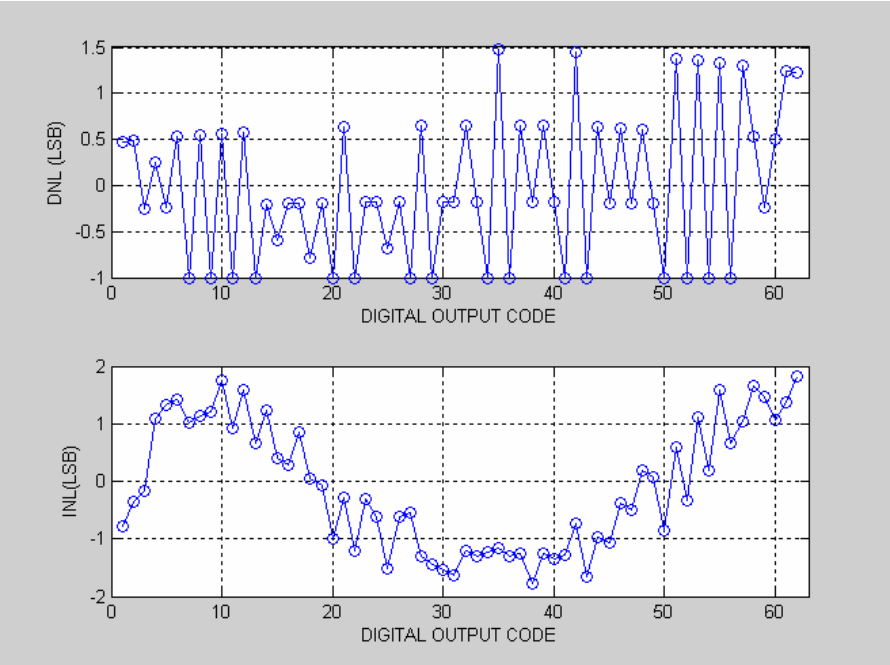


Figure 3. 39 DNL and INL simulation of first version A/D converter

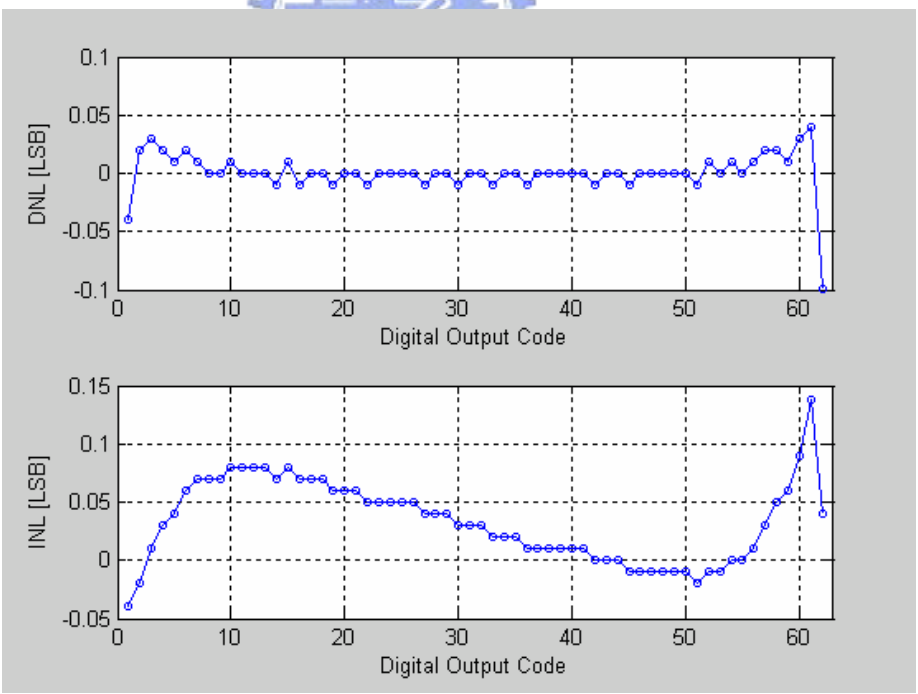


Figure 3. 40 DNL and INL simulation of second version A/D converter

3.10.2 Dynamic Performance Simulation

Figure 3.41 shows the dynamic performance of first version A/D converter at 2GHz sampling rate and 2MHz input frequency. The simulated SNDR, SFDR and ENOB are 29.54dB and 30.64dB and 4.61bits.

Figure 3.42 shows the dynamic performance of first version A/D converter at 2GHz sampling rate and the SNDR is decreased due to improper conditions at the edges of the preamplifiers.

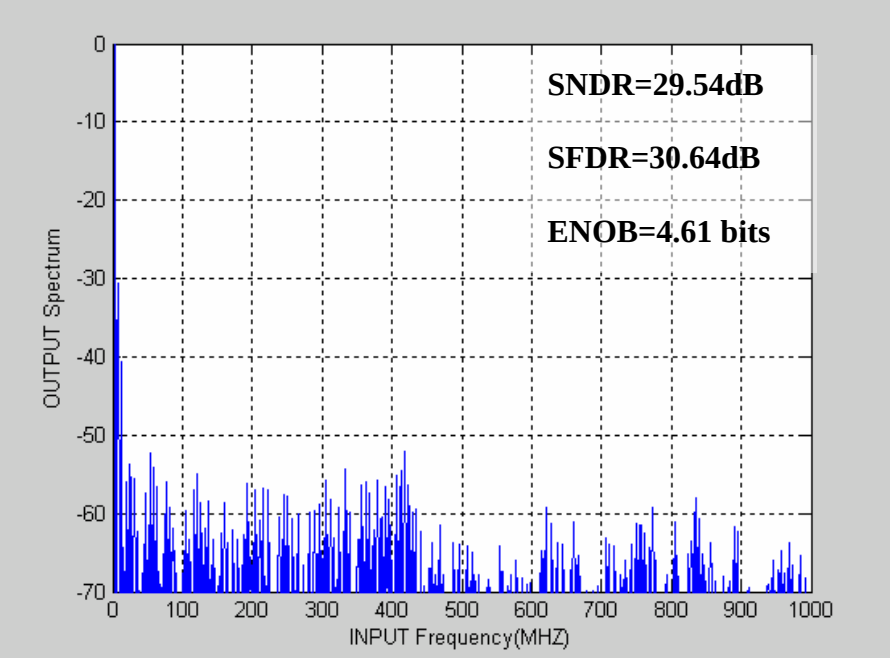


Figure 3. 41 Dynamic performance at a input frequency of 2MHz for first version A/D converter, sampled at 2GHz

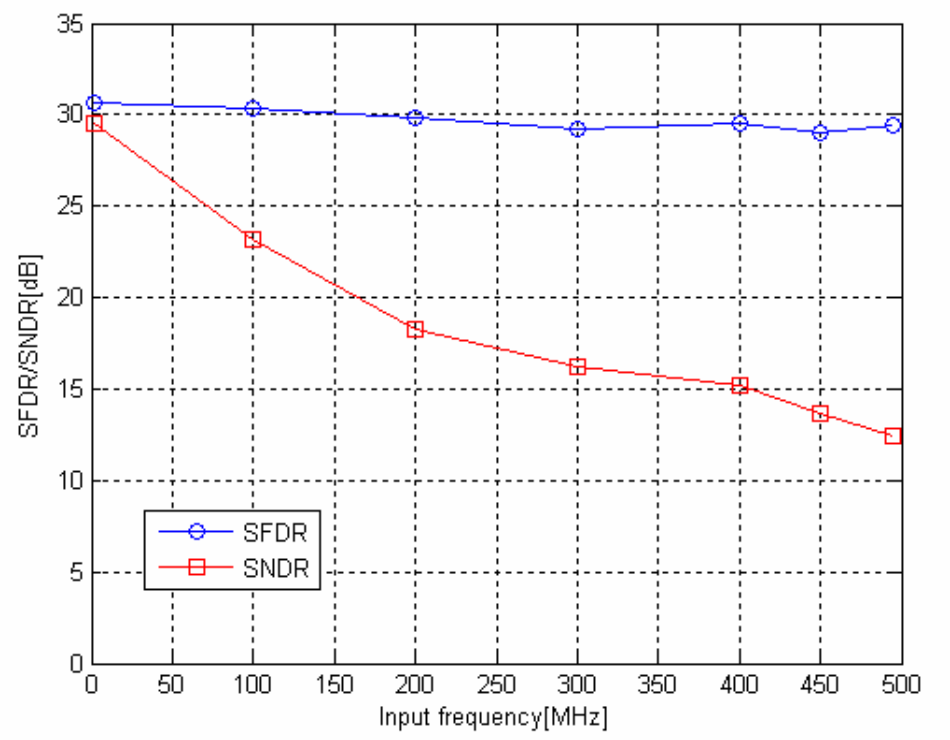


Figure 3. 42 SNDR and SFDR versus input frequency for first version A/D converter, sampled at 2GHz

Figure 3.43 shows the dynamic performance of second version A/D converter at 2GHz sampling rate and 7.81MHz input frequency. The simulated SNDR, SFDR and ENOB are 37.51dB and 48.94dB and 5.93bits.

Figure 3.44 shows the dynamic performance of second version A/D converter at 2GHz sampling rate and 492.18MHz input frequency. The simulated SNDR, SFDR and ENOB are 35.22dB and 38.65dB and 5.55bits.

Figure 3.45 shows the dynamic performance of second version A/D converter at 2GHz sampling rate and 976MHz input frequency. The simulated SNDR, SFDR and ENOB are 32.20dB and 33.68dB and 5.05bits.

Figure 3.46 shows the dynamic performance of second version A/D converter at 2GHz sampling rate and input frequency from low frequency to Nyquist frequency.

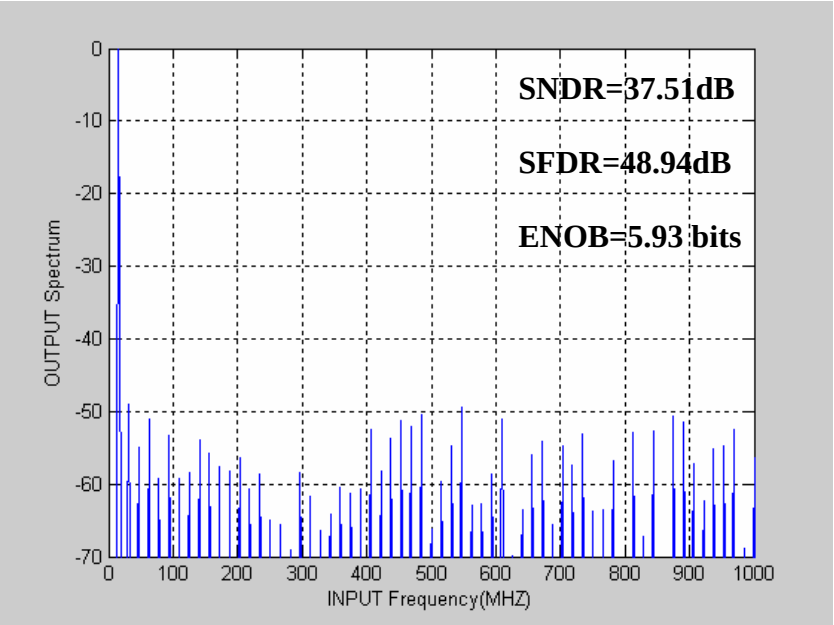


Figure 3. 43 Dynamic performance at a input frequency of 7.81MHz for second version A/D converter, sampled at 2GHz

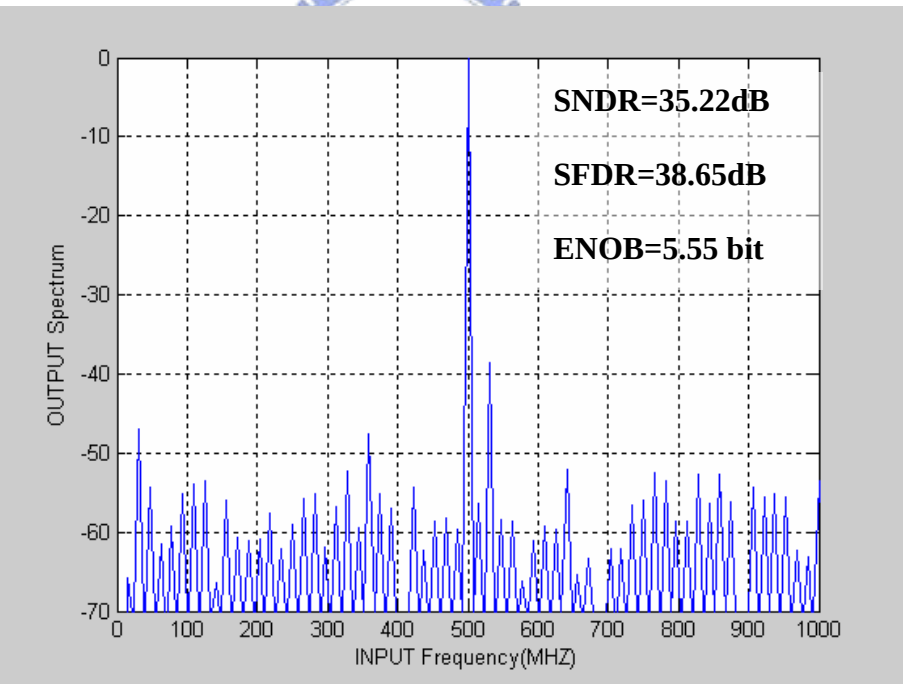


Figure 3. 44 Dynamic performance at a input frequency of 492.18MHz for second version A/D converter, sampled at 2GHz

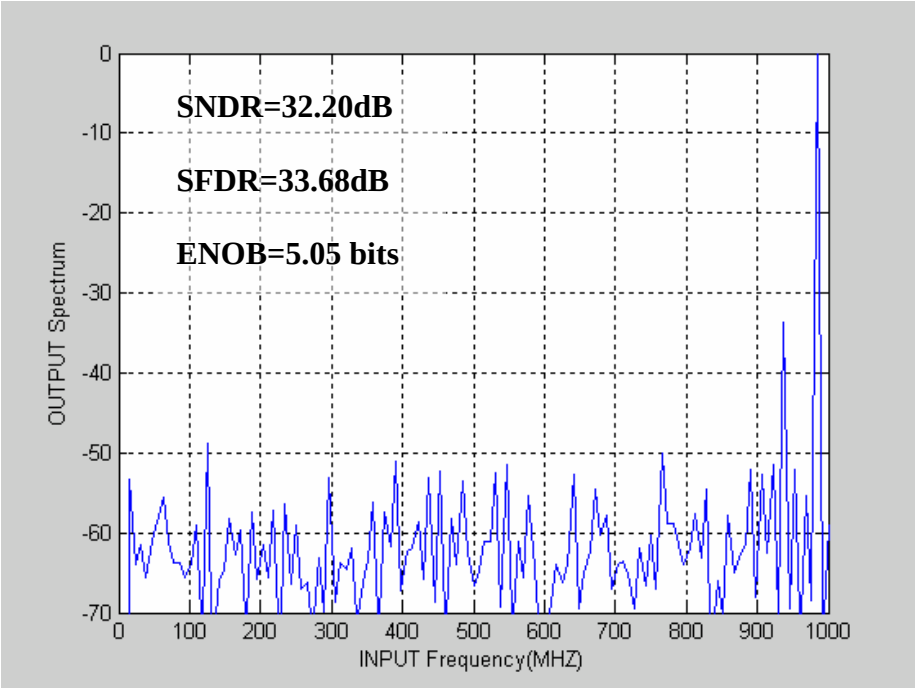


Figure 3. 45 Dynamic performance at a input frequency of 976.52MHz for second version A/D converter, sampled at 2GHz

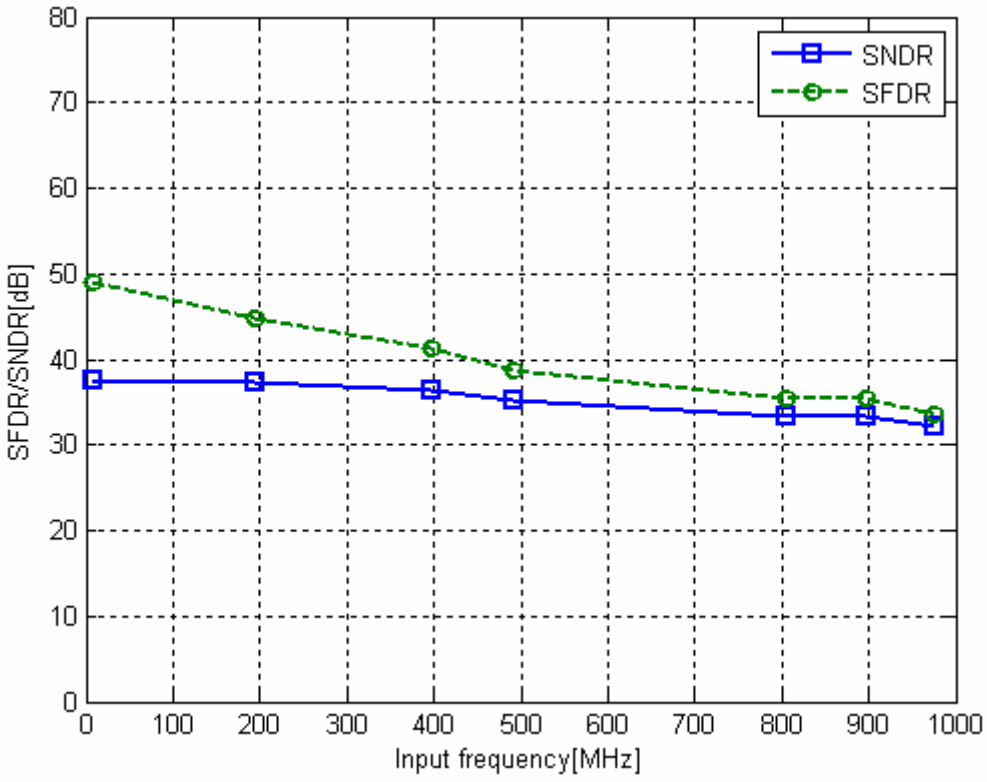


Figure 3. 46 SNDR and SFDR versus input frequency for second version A/D converter, sampled at 2GHz

	Power consumption (mW) (interpolation)	Power consumption (mW) (full preamplifiers)
Clock generator	7.5	7.5
Sample-and-hold	17.1	17.1
Resistor ladder	0.2	0.2
Preamplifier	**16.6**	**32.8**
Comparator	73.8	73.8
Auxiliary circuit and AND gate	0.9	1
Gray-encoded ROM and TSPC	0.3	0.3
Gray-to-binary decode	0.7	0.8
Total	117.1	133.5

Table 3. 1 Power saving after using interpolation technique

Technology	CMOS 0.13 μm
Supply voltage	1.2 V
Resolution	6 bits
Sampling rate	2 GHz
Full scale input	0.5 Vpp
DNL/INL	0.1LSB/0.14LSB
SNDR@fin=7.81MHz/976.56MHz	37.51dB/32.20dB
SFDR@fin=7.81MHz/976.56MHz	48.94dB/33.68dB
ENOB@fin=7.81MHz /976.56MHz	5.93 bits/5.05 bits
Power dissipation	117mW

Table 3. 2 The summary of second version A/D converter performance

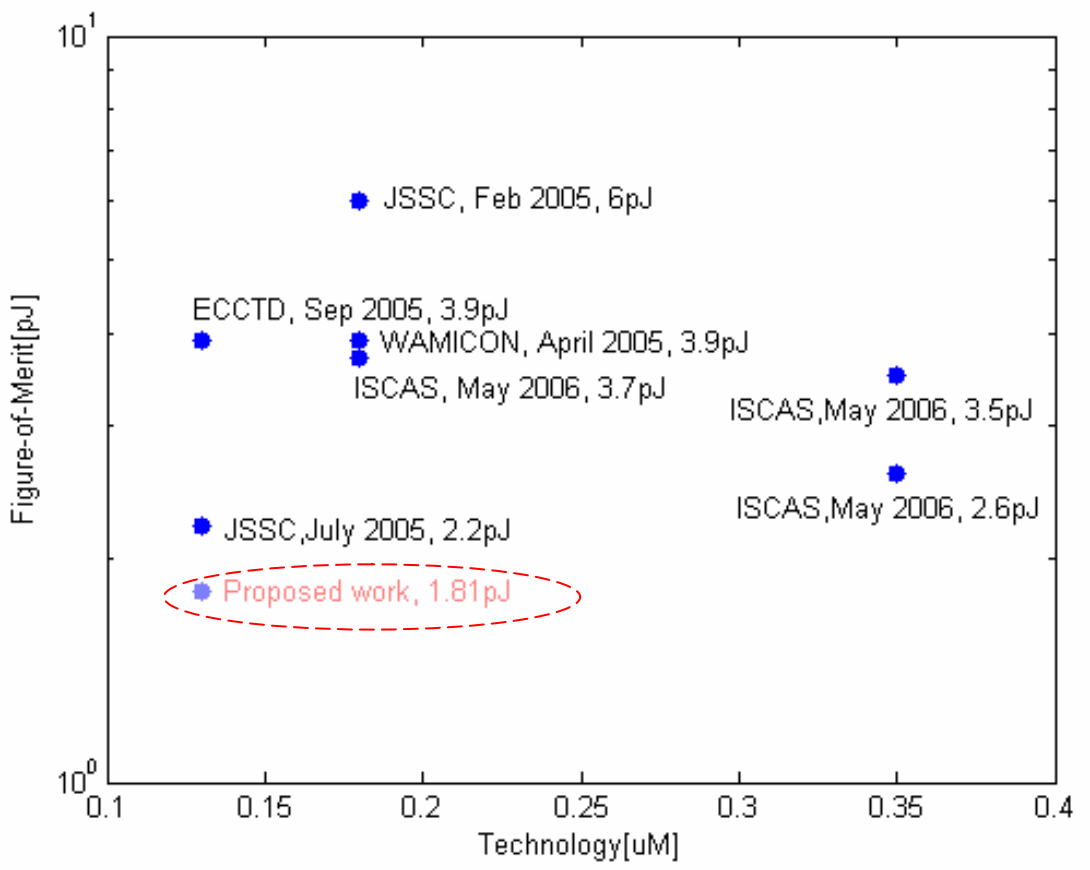


Figure 3. 47 The FOM comparison with publication paper

Table 3.1 shows the power saving after using interpolation technique. The preamplifier array can reduce 16.2mW when using interpolation technique. Table 3.2 shows the summary of second version A/D converter performance. The total power dissipation is 117mW and ENOB is 5.05 when input frequency approaches Nyquist frequency. The value of figure-of-merit (FOM) can be calculated and FOM without output buffer is 1.81pJ. The FOM comparison with other publication paper [15][22][23][24][25][26][27] are shown in Figure 3.47 The FOM is much lower than other published paper in our design by using sample-and-hold, interpolation, averaging and digital error correction technique.

CHAPTER 4

EXPERIMENT RESULTS

We have two versions of the A/D converter circuit design and just send the first version A/D converter for tape-out. After each circuit has been designed and simulated, this chapter starts with some back-end considerations for first version A/D converter, including layout technique, parasitic effects of package and bond wire, the electrostatic-discharging (ESD) protection, design of printed circuit board (PCB) and also measurement setup. While device scaling has enhanced the speed of transistors, unwanted interaction between different sections of integrated circuits as well as non-idealities in the layout and packaging increasingly limit both the speed and the precision of such systems. Today's circuit design is very heavily influenced by back-end considerations. Since this analog-to-digital converter design operates at high frequency as several mega-hertz to giga-hertz, these back-end considerations have great influences on the performance of proposed design.

4.1 Layout Design Consideration

For A/D converter circuit design, even with the same schematic design, different layouts will make entirely difference performance of the circuit. Therefore, the design of the layout is an important topic, especially for high frequency design. The most important things of the layout are parasitic and mismatches. For example, long metal lines will cause the parasitic capacitance and resistance to decrease the bandwidth and gain loss of the circuit. Improper layout could result in large difference of performance between simulated and measurement

result, or even result in failed circuits.

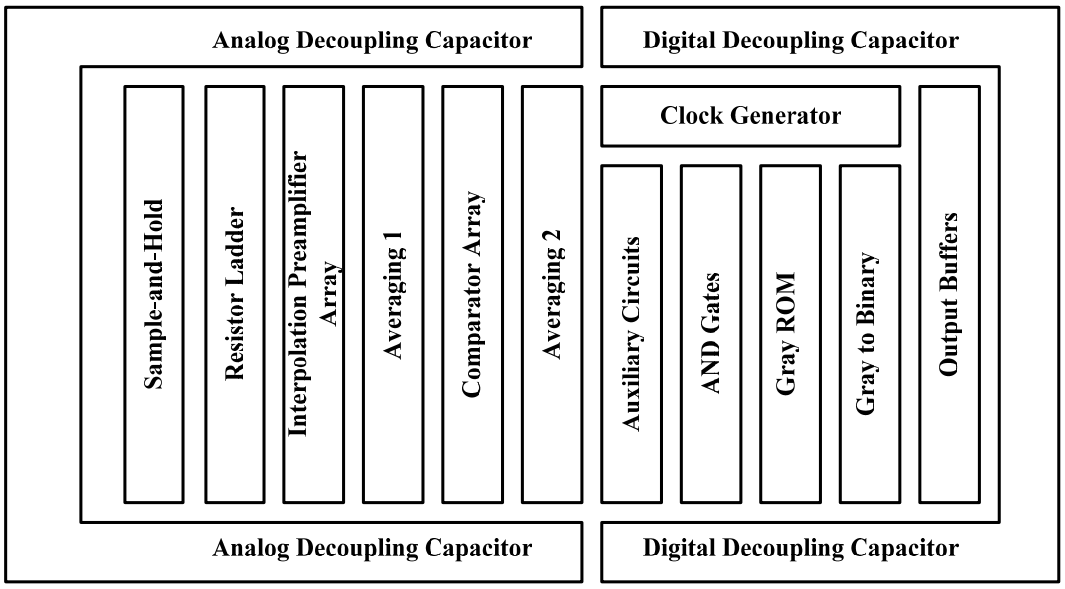


Figure 4. 1 Layout floorplan of A/D converter

The chip floorplan is shown in Figure 4.1. Layout plays an important role for the A/D converter design, since there are usually analog and digital parts in a A/D converter, and the signal coupling from digital part to sensitive analog part should be avoided. The analog power supply and digital supply are separated and the double guard ring is added in analog circuits and digital circuits to prevent the analog circuits from the digital noise. The power supply for the analog part and digital parts are only 1.2V. The analog power supply is fed to sample-and-hold, the preamplifier array and the comparator array and the digital power supply is fed to auxiliary circuits, AND gates, Gray-encoded ROM, TSPC flip flops, Gray-to-Binary decoder, clock generator and output buffers. In order to avoid large supply noise and ground bounce, large decoupling capacitances are added in DC power line for whole chip area. All the line widths are drawn according to following criteria, minimizing parasitic capacitance and series resistance. The DC current paths should be wide enough to prevent electro-migration. The line length of signal path should be kept as short as possible. The layout photograph of the flash A/D converter is shown in Figure 4.2, and the core circuit

area is 410μm x 530μm.

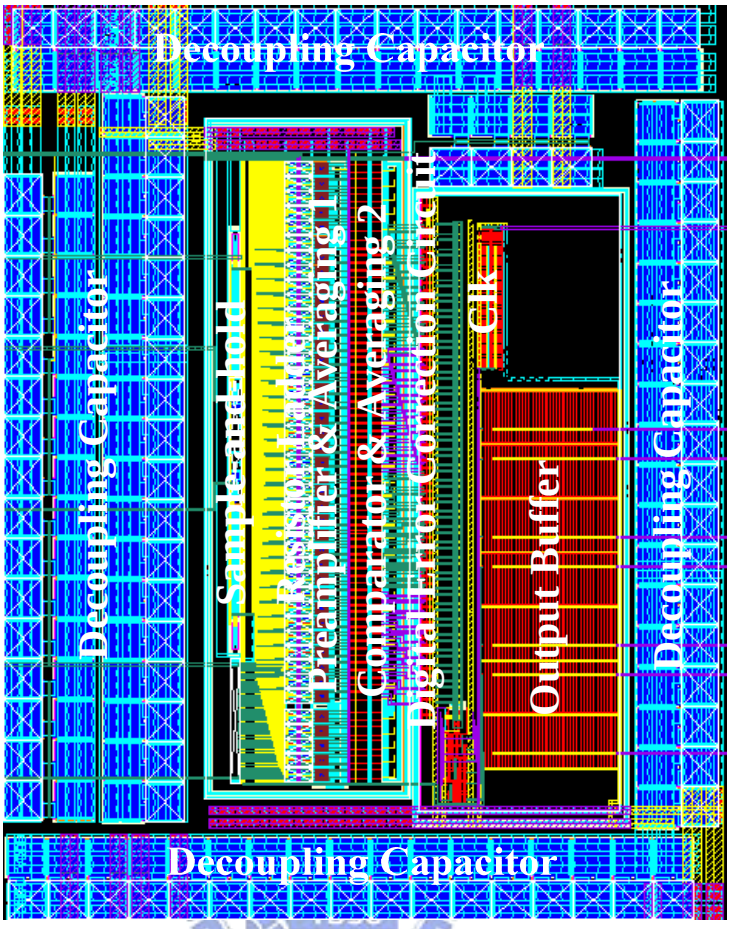


Figure 4. 2 Core layout photograph of the A/D converter

4.2 ESD Protection and Package

In the package, the electrostatic discharge (ESD) protection is added to each I/O pin. For thin oxide process, ESD protection is also a critical issue. Due to the process scales down, the channel is shorter and the tolerance of the gate voltage is smaller. Thus, MOSFET will be easily punctured. Figure 4.3 illustrates the ESD protection circuit used in proposed design. The diode-chain protection will guide large number of charges to VDD or GND, and the large gate-grounded NMOS will break down once a large potential across VDD and GND resulting in the charge in VDD flowing through NMOS to GND. The ESD circuit is provided by UMC

with 3.6kV human body mode (HBM) tolerance and induces around 40fF parasitic capacitor at each pad.

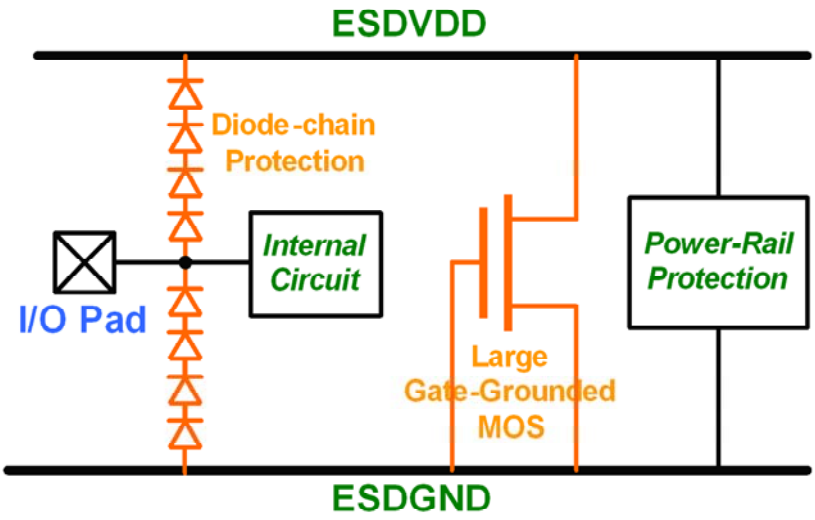


Figure 4. 3 ESD protection circuit

The QFN32 package provided by SPIL is employed in proposed design. This package is limited to 32 I/O pins. The overall area of package is 5 x 5 mm^2. The package model including bond wire effect of each I/O pin is depicted in Figure 4.4. The parasitic capacitor induced at each I/O pad is around 40fF while the series inductance induced by bone wire is about 1nH. Furthermore, the parallel capacitor will lead to signal coupling between adjacent pin which are the most concern of proposed design.

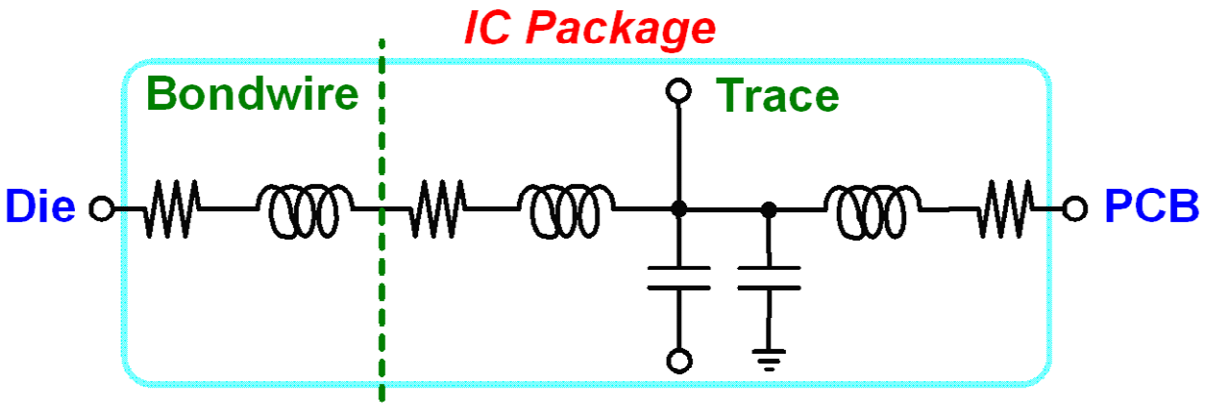


Figure 4. 4 Package model

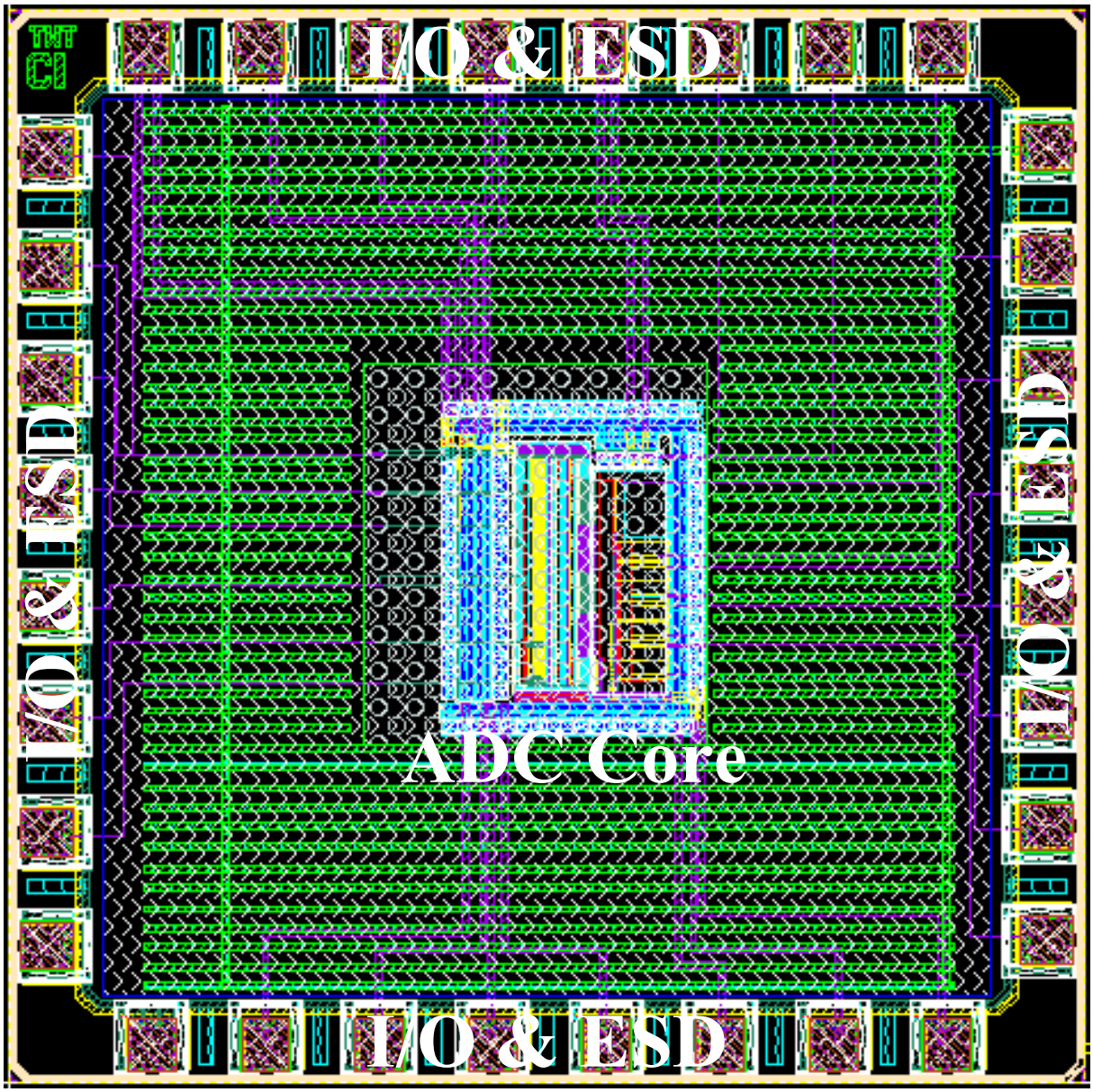


Figure 4. 5 Layout photograph of the A/D converter

The final layout photograph of the A/D converter is shown in Figure 4.5 including the A/D converter core circuit and ESD circuits. The chip is separated by analog part and digital part to avoid noise coupling. The layout area include IO pad is 1686um x 1686um.

4.3 Printed Circuit Board (PCB) Design

The printed-circuit board (PCB) is designed by using Protel 99 SE. The pin assignment is shown in Figure 4.6 and the function of the pin is shown in Table 4.1. In order to prevent noise coupling from digital circuits to analog circuits, the analog part and the digital part are separated. The analog power supply and digital power supply are also separated.

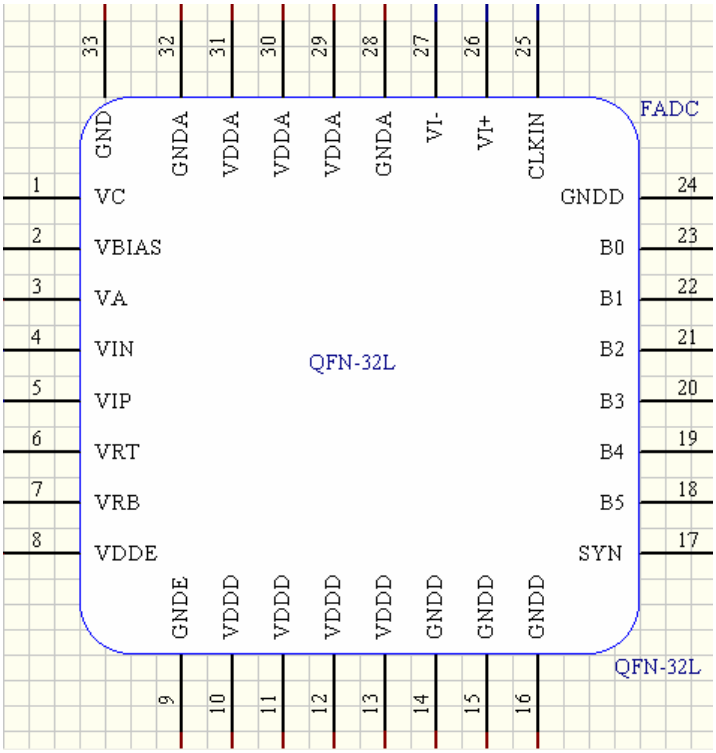


Figure 4. 6 The schematic of the pin assignment

As for the implementation of printed-circuit board (PCB), we adopt “RO4003” as our dielectric owning to this material has less loss at high frequency operation. We employ four-layer board to firm up the copper signal line, and further stabilize the high frequency signal paths. The large bypass capacitors are also added in the PCB in order to provide a stable DC voltage and avoid the unexpected performance degradation. The schematic of the PCB design is shown in Figure 4.7. The input differential signal is created by a transformer and signal generator. The PCB layout view is shown in Figure 4.8.

Pin Number	Pin Name	Function
1	VC	Comparator current bias
2	VBIAS	Preamplifier current bias
3	VA	Sample-and-hold current bias
4	VIN	Negative differential input signal
5	VIP	Positive differential input signal
6	VRT	Resistor ladder top voltage
7	VRB	Resistor ladder bottom voltage
8	VDDE	Supply of ESD Protection
9	GNDE	Ground of ESD Protection
10	VDDD	Digital power supply
11	VDDD	Digital power supply
12	VDDD	Digital power supply
13	VDDD	Digital power supply
14	GNDD	Digital ground
15	GNDD	Digital ground
16	GNDD	Digital ground
17	SYN	Synchronization for measurement
18	B5	Digital Output (MSB)
19	B4	Digital Output
20	B3	Digital Output
21	B2	Digital Output
22	B1	Digital Output
23	B0	Digital Output (LSB)
24	GNDD	Digital ground
25	CLKIN	Input clock signal
26	VI+	Test point1
27	VI-	Test point2
28	GNDA	Analog ground
29	VDDA	Analog power supply
30	VDDA	Analog power supply
31	VDDA	Analog power supply
32	GNDA	Analog ground

Table 4. 1 The function of the pin assignment.

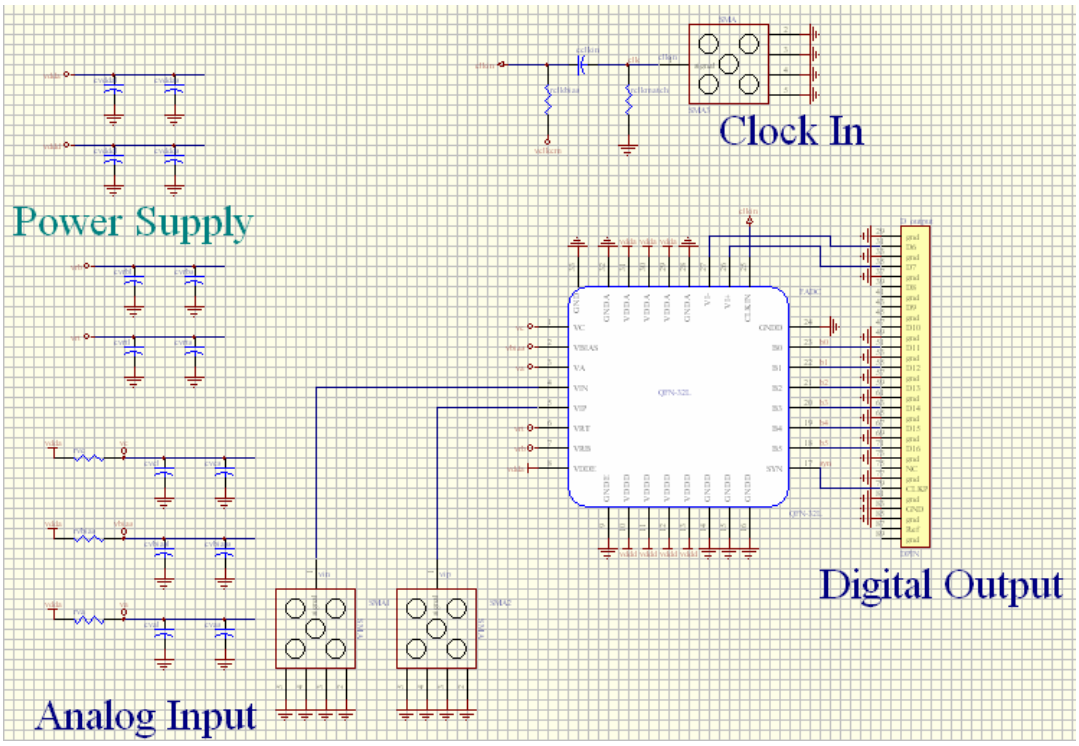


Figure 4. 7 The schematic of the PCB design.

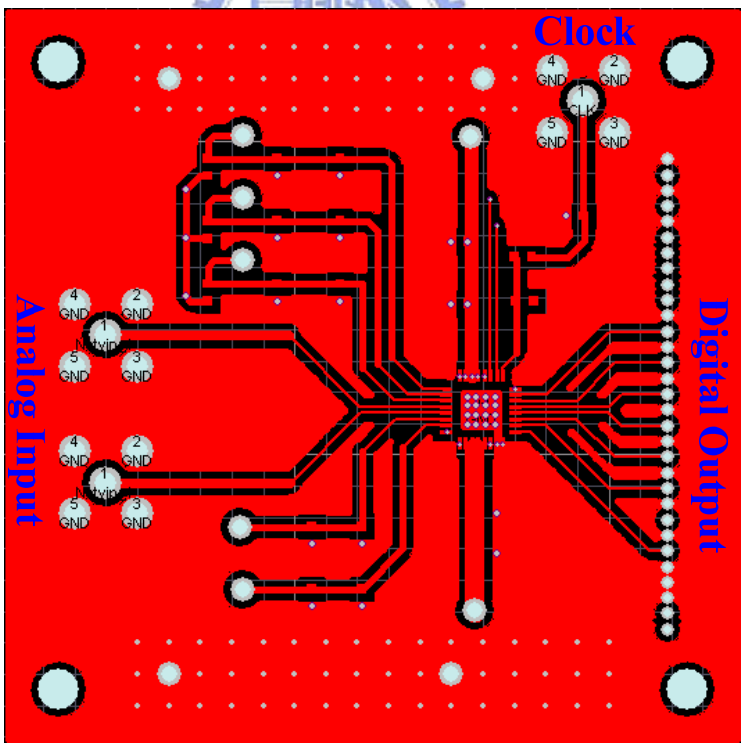


Figure 4. 8 The layout of the PCB

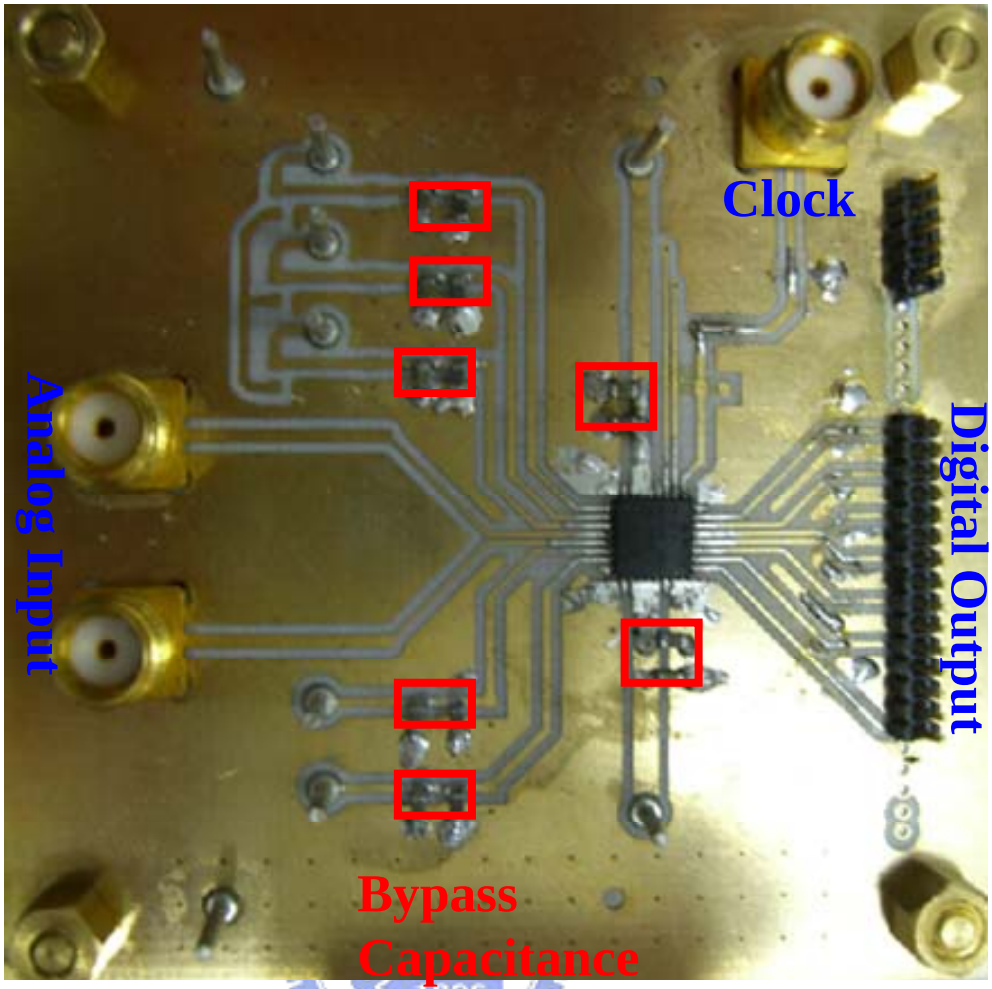


Figure 4. 9 The PCB of the flash A/D converter

The clock signal is created by a signal generator and a bias-tee. The input signal and clock signal path have to concern the input matching to prevent the signal degradation and the output of the A/D converter has to assign a synchronization pin for measurement. The PCB of the A/D converter is shown in Figure 4.9. The material of the PCB is RO4003 which is suitable for high frequency operation. In order to filter the supply noise, large bypass capacitances are located near the chip.

4.4 Measurement Setup

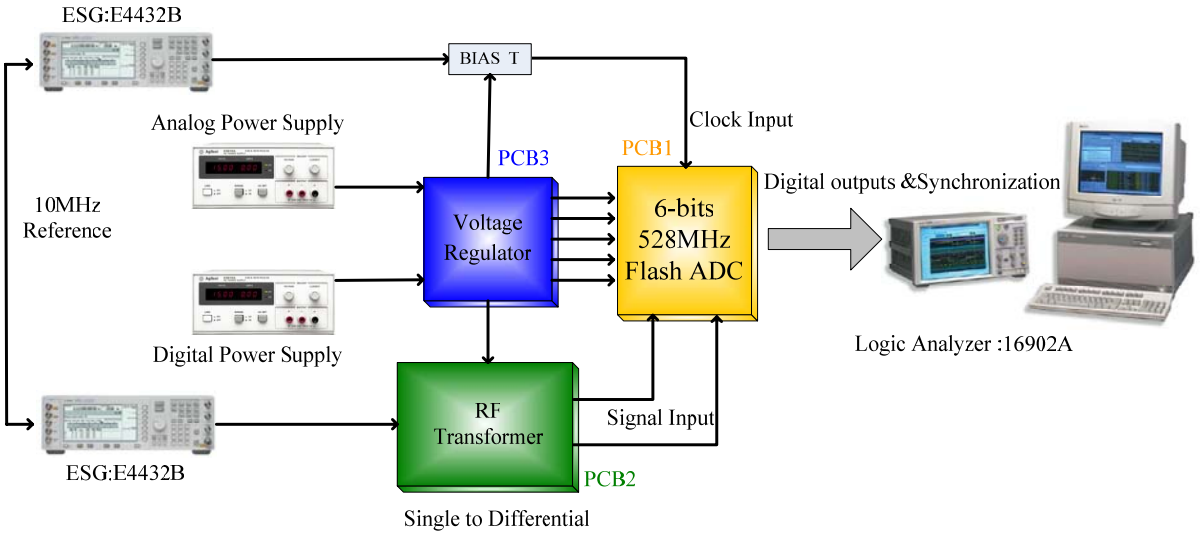


Figure 4. 10 Measurement plan

The measurement setup is also an important issue in the A/D converter design. The measurement plan is shown in Figure 4.10. We need several instruments such as ESG, Logic Analyzer, Oscilloscope and Power Supply. The input and output of these instruments are usually single-ended, so single-to-differential conversion is needed. The single-to-differential input signal is generated by the transformer which the model is Mini-Circuits ADT4-6WT. The analog input signal source and the clock source are generated by the ESG which is produced by Agilent E4432B and The input signal clock is produced by the Bias-T which the type is ZNBT 60-1W. The transformer and Bias-T are shown in Figure 4.11. The module of the logic analyzer is 16902A which the timing can achieve 2GHz.The testing environment is shown is Figure 4.12 and the device under test is shown in Figure 4.13.

Figure 4. 11 Transformer and Bias-T

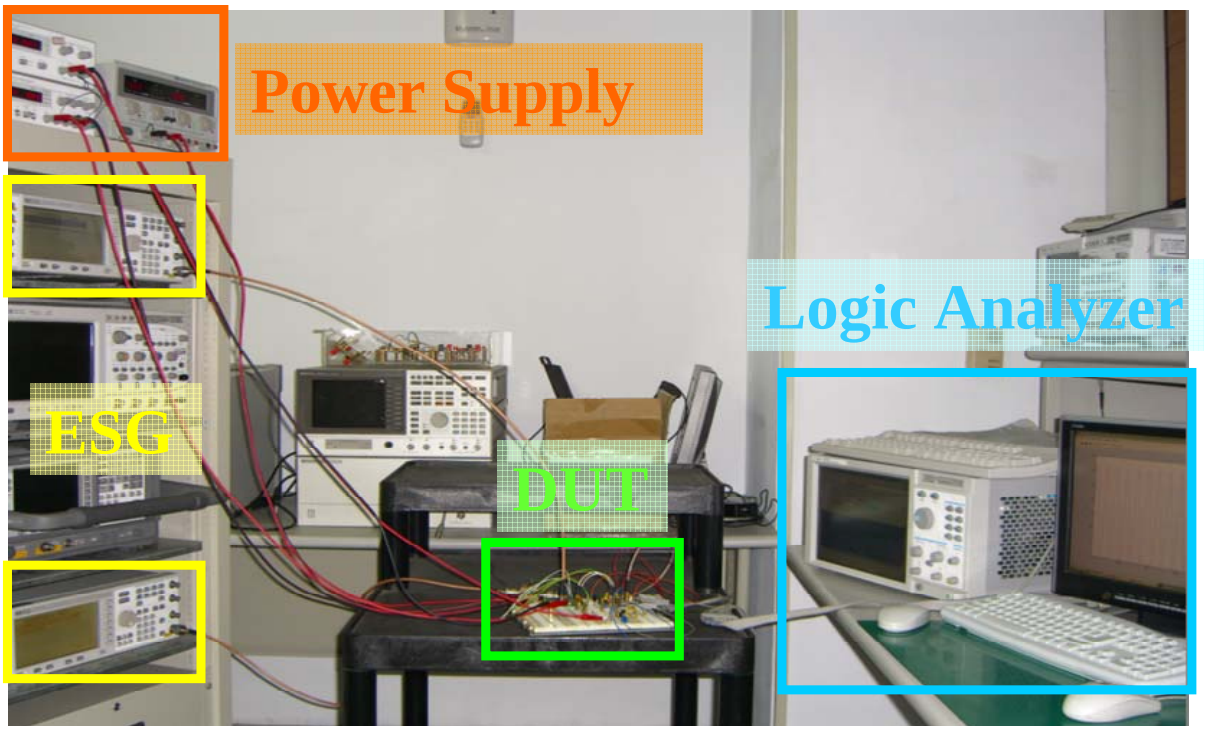


Figure 4. 12 Testing environment

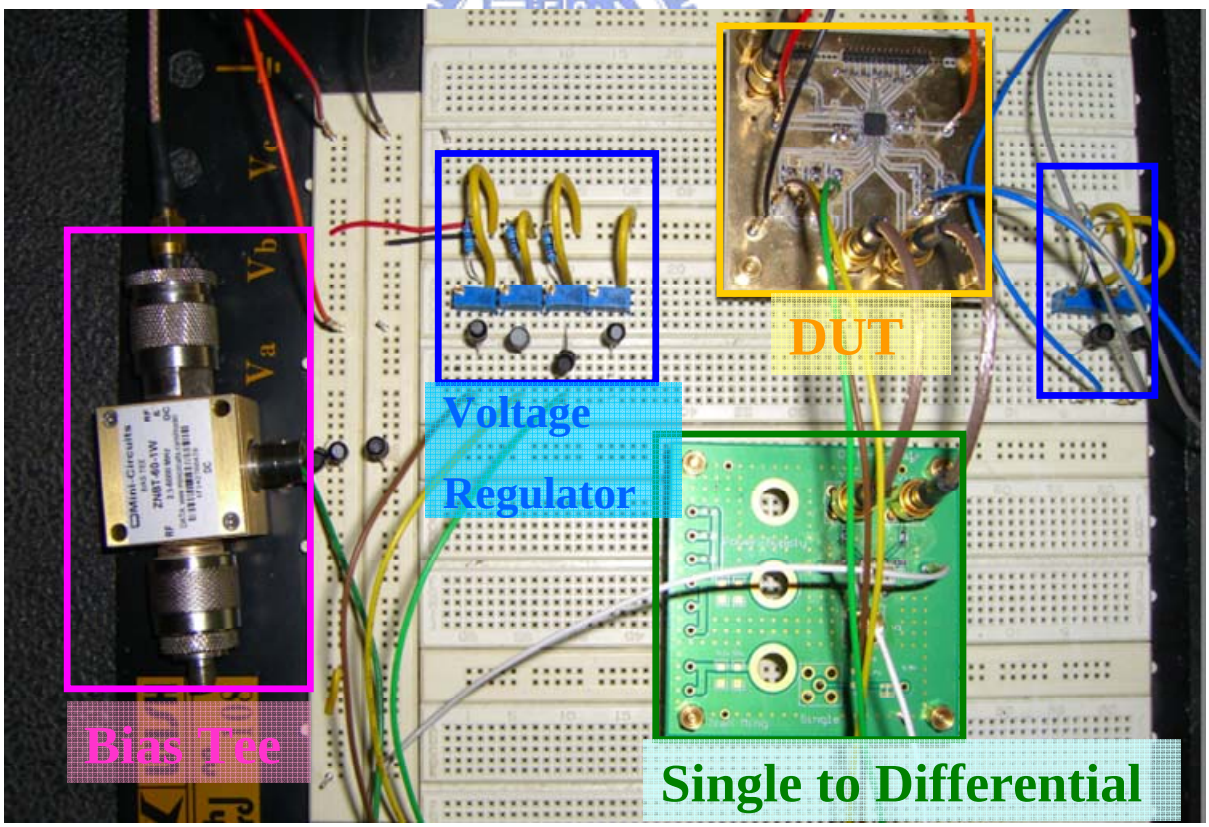


Figure 4. 13 Device under test

4.5 Measurement Results

The low-power high-speed flash A/D converter architecture with sample-and-hold, interpolation, resistive averaging and digital error correction technique and design concepts are described in Chapter3. In this section, we just show measurement results of first version A/D converter because second version A/D converter is not sent for tape-out and the first version circuits is fabricated by UMC 0.13μm single-poly-eight-metal (1P8M) CMOS technique. The analog power supply and digital power supply are 1.2V and the power dissipation is 88.93mW at 2GHz sampling rate. The data files are computed by the FFT testing [28] to measure the signal-to-noise-and-distortion ratio (SNDR), and spurious-free dynamic range (SFDR). The differential -nonlinearity (DNL) and integral-nonlinearity (INL) measurement is adopted by the histogram testing method [29].

4.5.1 Dynamic Testing

The dynamic testing plot from instrument is shown in Figure 4.14. The input frequency is 1.007MHz and the sampling frequency is 300MHz.

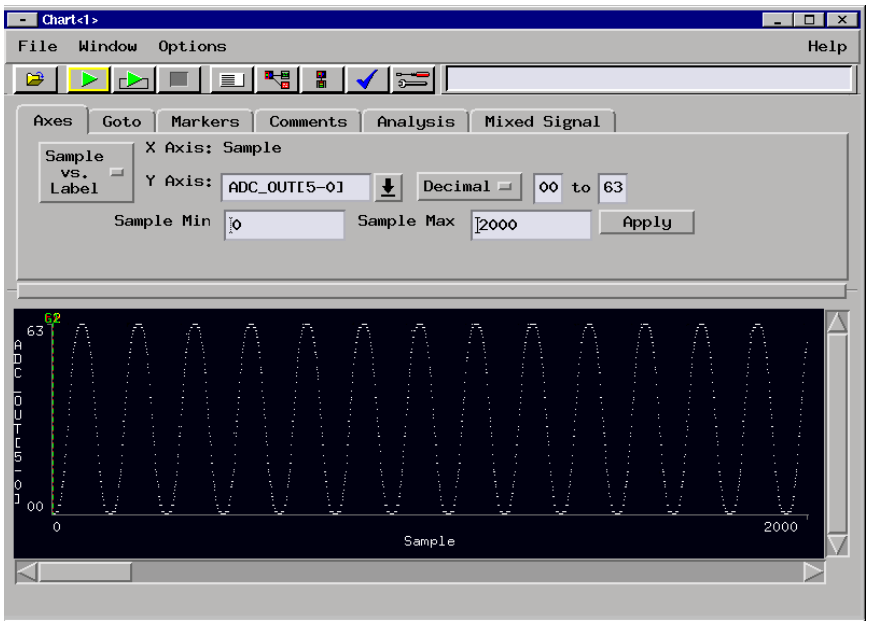


Figure 4. 14 Dynamic testing plot from Logic Analyzer

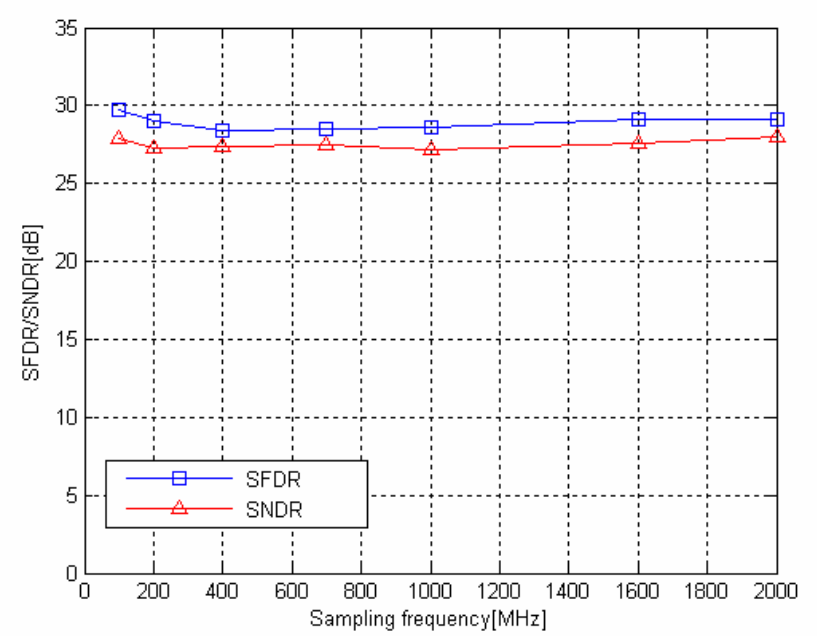


Figure 4. 15 Dynamic performance versus sampling frequency

The dynamic performance of the A/D converter is shown in Figure 4.15, the SNDR and SFDR is plotted against the sampling frequency. The input frequency is 2MHz and the SNDR is 27.97dB and SFDR is 29.04dB when the clock frequency at 2GHz. The effective number of bits is calculated equal to 4.3 bits.

4.5.1.1 Sampling Frequency at 300MHz

The dynamic performance of the A/D converter at 300MHz sampling frequency is described in this section. Figure 4.16 shows the FFT plot at 1.007M. Figure 4.17 shows the SNDR versus input frequency at 300MHz sampling rate and the SNDR is decreased due to improper conditions at the edges of the preamplifiers. Figure 4.18 shows the SFDR versus input frequency at 300MHz sampling rate. Figure 4.19 shows SNDR versus sampling rate at 1MHz input frequency. Figure 4.20 shows SFDR versus sampling rate at 1MHz input frequency.

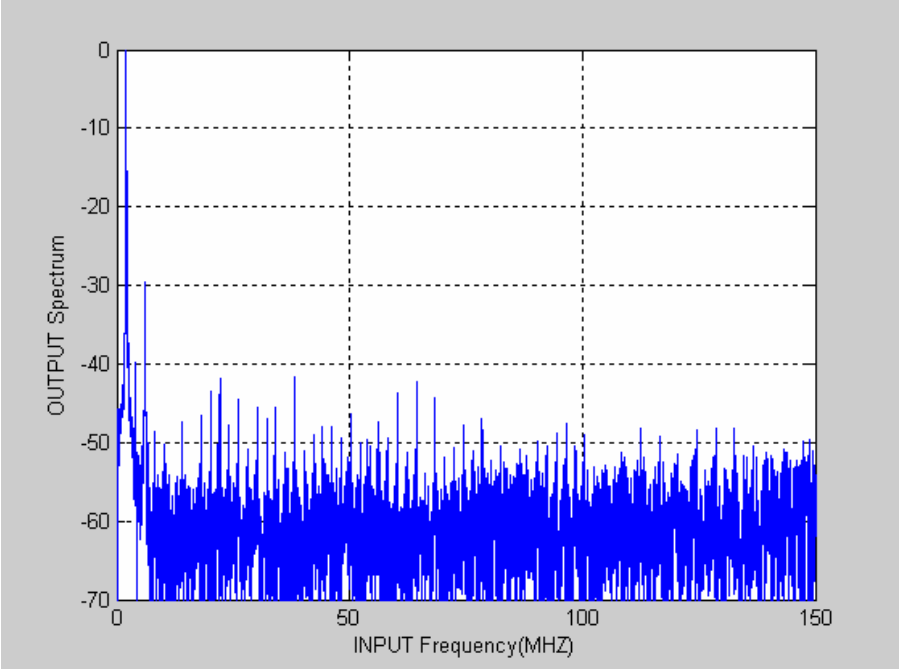


Figure 4. 16 FFT plot at 1.007MHz input frequency.

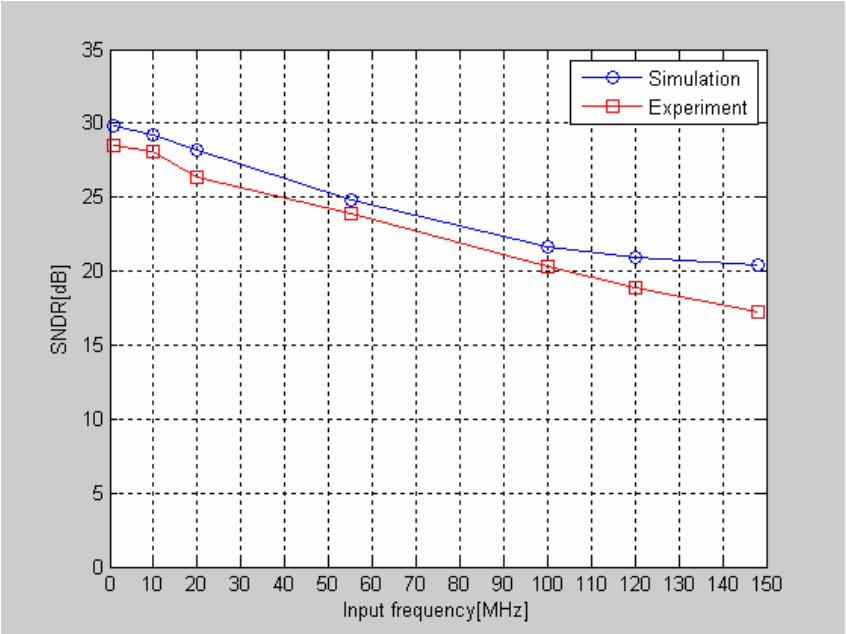


Figure 4. 17 SNDR versus input frequency at 300MHz sampling rate

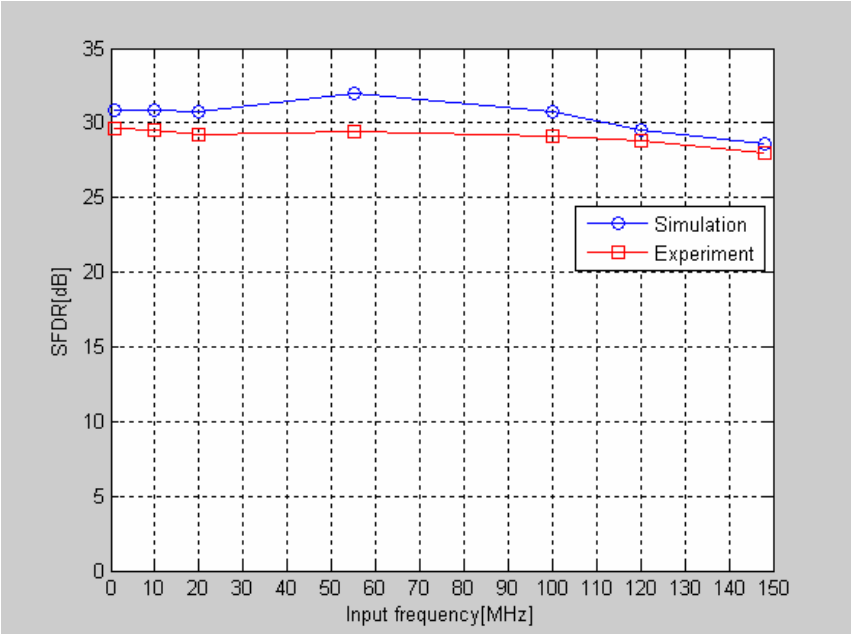


Figure 4. 18 SFDR versus input frequency at 300MHz sampling rate

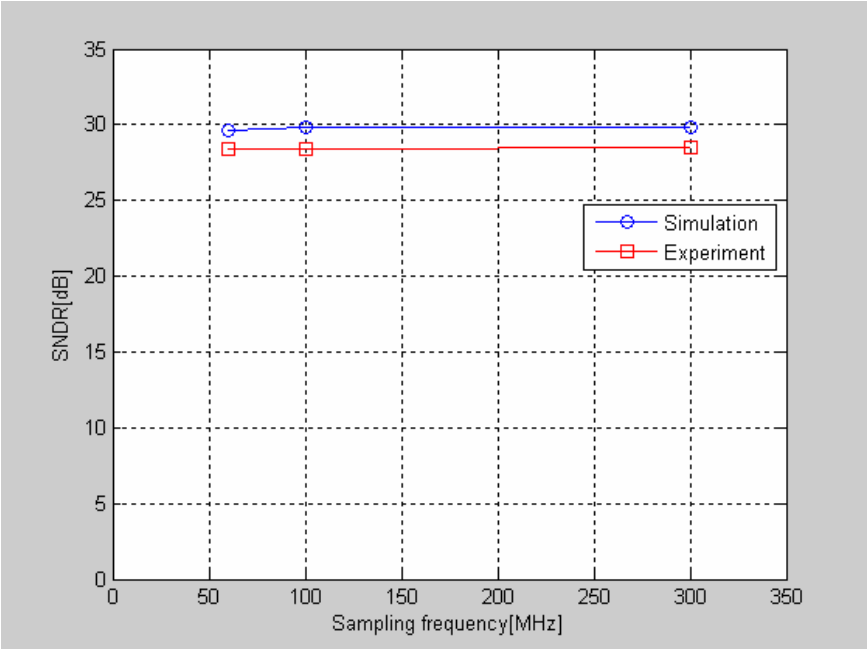


Figure 4. 19 SNDR versus sampling rate at 1MHz input frequency

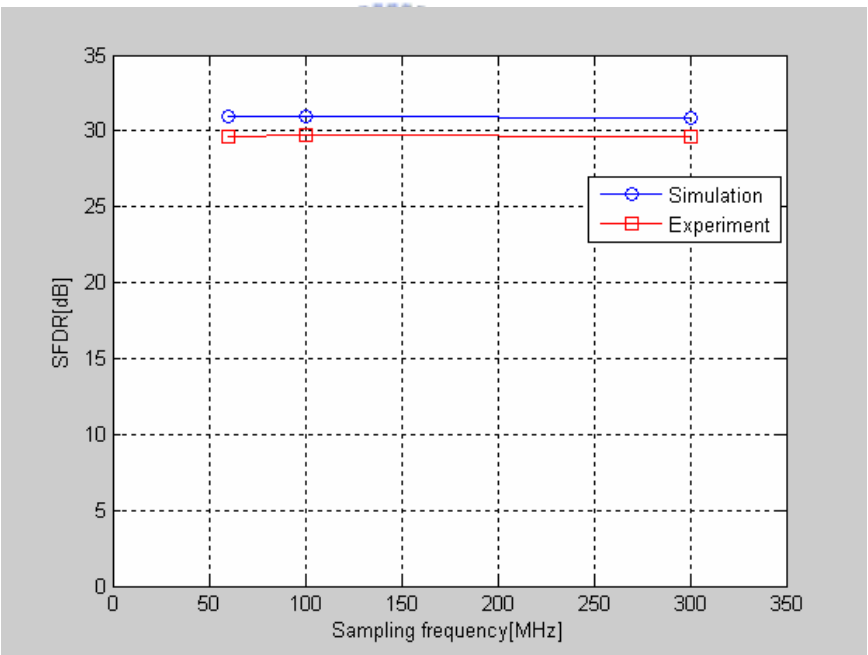


Figure 4. 20 SFDR versus sampling rate at 1MHz input frequency

4.5.1.2 Sampling Frequency at 2GHz

In this section, the operation frequency at 2GHz is presented. Figure 4.21 shows the SNDR versus input frequency at 2GHz sampling rate and the SNDR is decreased due to improper conditions at the edges of the preamplifiers. Figure 4.22 shows the SFDR versus input frequency at 2GHz sampling rate. Figure 4.23 shows SNDR versus sampling rate at 2MHz input frequency. Figure 4.24 shows SFDR versus sampling rate at 2MHz input frequency.

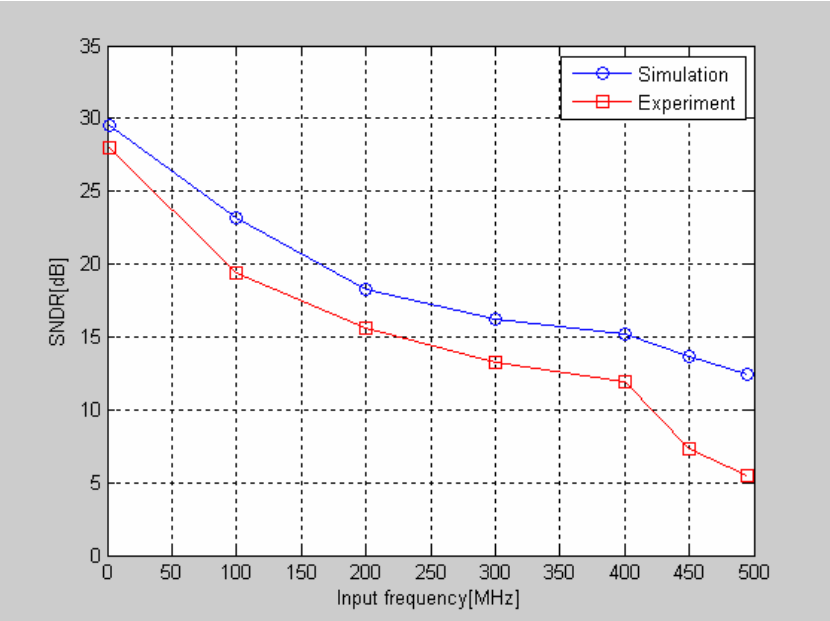


Figure 4. 21 SNDR versus input frequency at 2GHz sampling rate

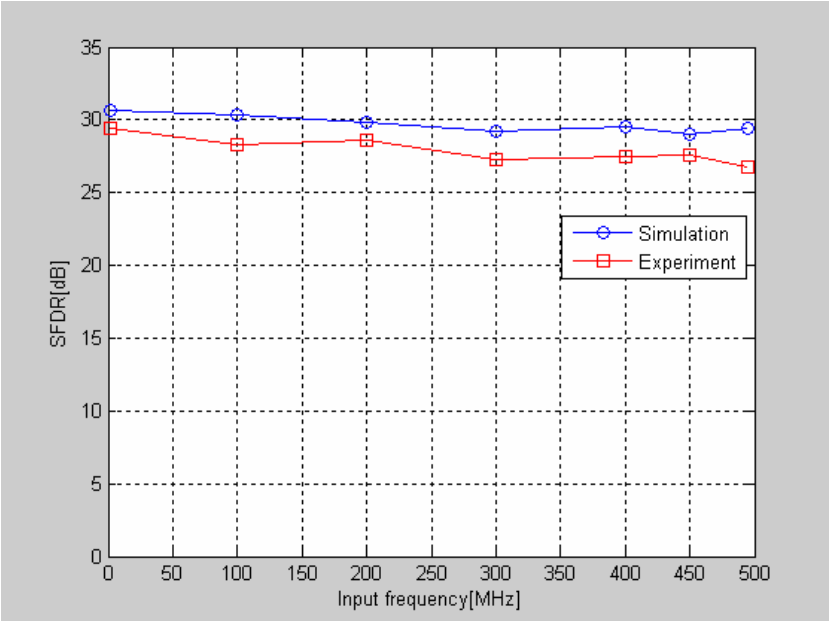


Figure 4. 22 SFDR versus input frequency at 2GHz sampling rate

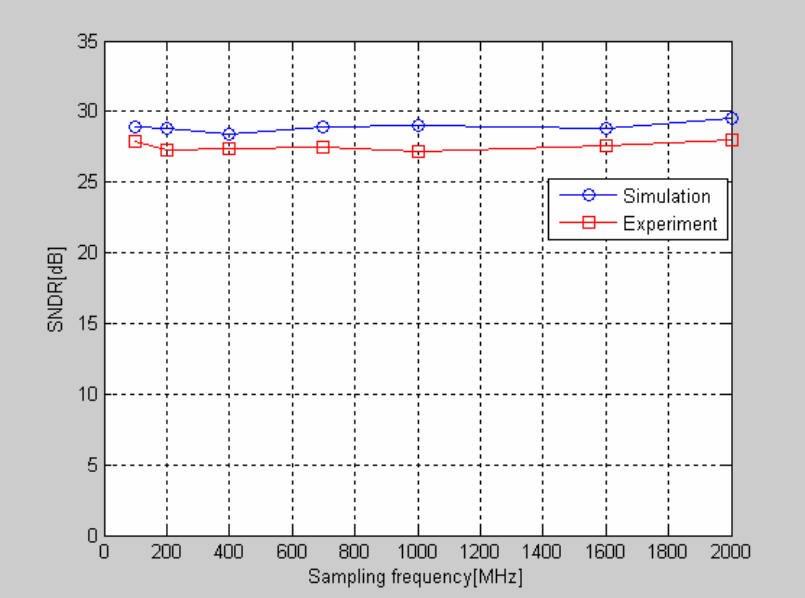


Figure 4. 23 SNDR versus sampling rate at 2MHz input frequency

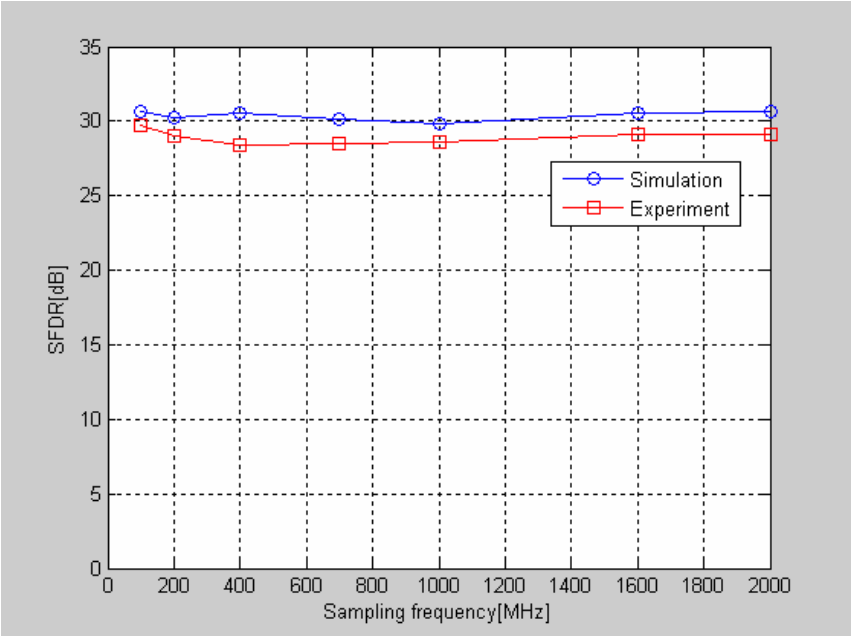


Figure 4. 24 SFDR versus sampling rate at 2MHz input frequency

4.5.2 Static Testing

The 16384 samples of data are collected to compute the DNL and INL which is shown in Figure 4.25 and 4.26. The sampling frequency is 2GHz and input frequency 2MHz sine wave is digitalized by the A/D converter under test. The measurement DNL is between +1.56 and -1.00 LSB and the measurement INL is between +1.91 and -1.85 LSB. The offset error is bad controlled in the A/D converter design to degrade the performance.

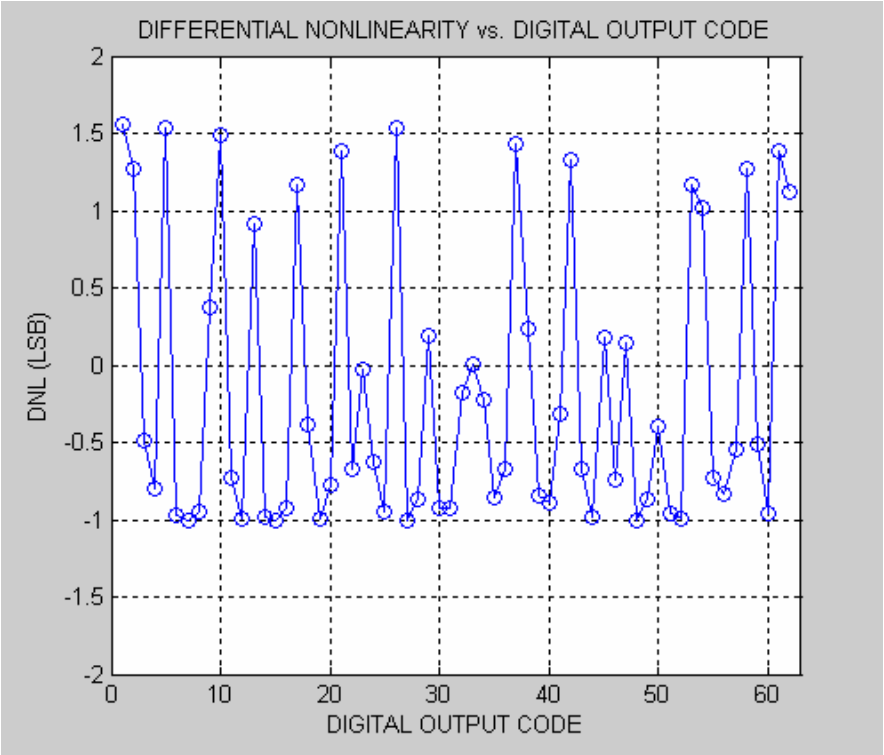


Figure 4. 25 Measured DNL error

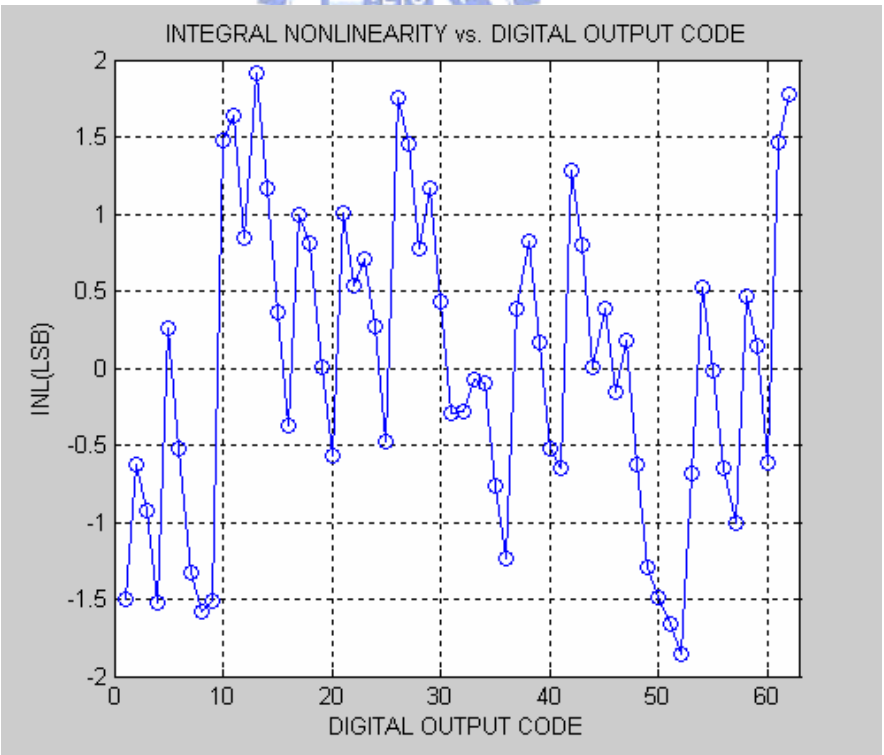


Figure 4. 26 Measured INL error

4.6 Summary

This chapter described in detail the experimental for the chip showed the measurement results of the implementation of the flash A/D converter in 0.13μm CMOS process. The total power dissipation is 88.93mW at 2GHz sampling rate. The measurement of the flash A/D converter is summarized in Table 4.2.

Parameters	Measurement Results
Resolution	6 bits
Conversion Rate	2GHz
DNL @ 2GHz sampling rate	+1.56 LSB / -1.00 LSB
INL @ 2GHz sampling rate	+1.91 LSB / -1.85 LSB
Input Range	0.5V Vpp differential
SNDR@2MHz input signal	27.97 dB
SFDR@2MHz input signal	29.04 dB
ENOB@2MHz input signal	4.3 bits
FOM	30.4 pJ
Analog/ Digital Power dissipation	64.27mW/ 24.66mW
Supply Voltage	1.2V
Technology	UMC 0.13μm CMOS

Table 4. 2 Measurement performance summary

CHAPTER 5

CONCLUSIONS

5.1 Summary

A 6-bit low-power high-speed flash A/D converter is proposed for UWB wireless applications. Use sample-and-hold to improve dynamic performance of A/D converter. when the input frequency is near the Nyquist frequency. Use interpolation technique to reduce the number of preamplifier and input capacitance. The A/D converter with interpolation technique consumes less power than full flash and improves differential non-linearity (DNL) of A/D converter. Add averaging resistance to reduce the offset of preamplifier and comparator and reduce the DNL to improve linearity. About 83% power saving by averaging resistance in preamplifiers is achieved. Use digital error correction technique to reduce bubble error and metastability error. The power of $(2^n-1)m$ pipeline latches is eliminated by the digital correction circuit. By combining these techniques, the first version A/D converter consumes about 88.4mW from 1.2V power supply at 2GSample/s and the signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) maintain above 29.54dB and 30.64dB for input frequency of 2MHz. The peak differential -nonlinearity (DNL) and peak integral-nonlinearity (INL) is less than 1.47LSB and 1.83LSB. By combining above techniques, the second version A/D converter consumes about 117mW from 1.2V power supply at 2GSample/s and the SNDR and SFDR maintain above 32.2 and 33.68dB for input frequency of 976MHz. The FOM of the A/D converter is 1.81pJ. The peak

DNL and peak INL is less than 0.1LSB and 0.14LSB.

The chip of first version A/D converter is fabricated in 0.13-μm CMOS technology. The supply voltage of analog and digital circuits is 1.2V and feeds them separately. The total power dissipation is 88.93mW at 2GHz sampling rate. The measurement of the SNDR is 27.97dB and SFDR is 29.04dB under 2GHz sampling rate and 2MHz input frequency. The measured DNL and INL are +1.56/-1.00 LSB and +1.91/-1.85LSB. The effective number of bits (ENOB) is calculated equal to 4.3 bits.

5.2 Future Work

In this thesis, we have two versions of the A/D converter circuit design. We just send the first version A/D converter for tape-out and there are some design considerations which are not paid an attention. We give some recommendations and improvement in this section. First, circuit simulation time is too long to waste a lot of time. In order to eliminate the long simulation time by HSPICE or SPECTRE, the behavior model can be constructed by MATLAB/SIMULINK to understand the influence on the A/D converter due to device mismatches and also realize the dynamic performance of the A/D converter. Second, the high speed testing is difficult for digital output. In order to have a better measurement performance, the digital output signal can be decimated at A/D converter output for measurement or design low-voltage differential signaling (LVDS) drivers at digital outputs for high speed digital applications. Finally, the second version of the A/D converter circuit design will be for next time tape-out and will get better performance in the future work.

Bibliography

[1] "FCC Notice of Proposed Rule Making, Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems," Federal Communications Commission, Washington, DC, ET-Docket 98-153.

[2] M. Choi and A. A. Abidi "A 6-b 1.3Gsamples A/D Converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1847-1858, Dec. 2001.

[3] Rudy van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd edition, Kluwer Academic Publishers, 2003.

[4] C. W. Mangelsdorf, "A 400-MHz input flash concerter with error correction," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 184-191, Feb. 1990.

[5] B. Black. Analog-to-Digital Converter Architectures and Choices for System Design. Analog Dialogue, 33-8, 1999. http://www.analog.com/library/analogDialogue/archive/33-08/adc/index.html

[6] B. Razavi, *Principles of Data Conversion System Design*. New York: IEEE Press, 1995.

[7] J. Yoo, "A TIQ Baesd CMOS Flash A/D Converter for System-on-Chiip Applications," PhD. dissertation, Univ. Pennsylvania State, Korea, 2003.

[8] Daugherty, Kevin M, *Analog-to-digital conversion : a practical approach*, New York ,McGraw-Hill ,1994.

[9] Walt Kester, *The Data Conversion Handbook*, Analog Devices, 2005.

[10] H. Kimura et al., "A 10-b 300-MHz interpolated parallel A/D converter,". IEEE J. Solid-State Circuits, vol. 28, pp. 438–446, Apr. 1993.

[11] R. Taft, C. Menkus, M. R. Tursi, O. Hidri, and V. Pons, “A 1.8-V 1.6-GS/s 8-b Self-Calibrating Folding ADC With 7.26 ENOB at Nyquist Frequency,” IEEE J. Solid-State Circuits, vol. 39, pp. 2107–2115, Dec. 2004.

[12] P.M. Figueiredo, J.C. Vital, “Averaging technique in flash analog-to-digital converters,” IEEE Transactions on Circuits and Systems , vol. 51, pp. 233–253, Feb. 2004.

[13] H. Pan and A. A. Abidi “Spatial Filtering in Flash A/D Converters,” *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 424-436, Aug. 2003.

[14] H. Tuinhout, M. Pelgrom, and M. Vertregt, “Transistor matching in analog CMOS applications,” in Proc. *IEEE IEDM Tech*. Dig., 1998, pp. 915–918.

[15] Jian-Ming Wu, Wen-Shen Wuen and Kuei-Ann Wen, "A Low Power CMOS A/D Converter for Ultra-wideband Wireless Applications", *accepted by IEEE Wireless and Microwave Technology Conference*, Clearwater, FL, USA, April 2005.

[16] C. L. Portmann and T. H. Y. Meng, “Power-efficient metastability error reduction in CMOS flash A/D converters,” *IEEE J. Solid-State Circuits*, no. 8, Aug. 1996.

[17] A. Venes and R. J. V. de Plassche, “An 80-MHz 80-mW 8-b CMOS folding A/D converter with distributed T/H preprocessing,” *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 1996, pp. 241–243.

[18] K. Uyttenhove, J. Vandenbussche, E. Lauwers, G. G. E.Gielen and M. Steyaert, “Design Tecnniques and Implementation of an 8-bit 200-MS/s Interpolatiin/Averaging CMOS A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 483-494, Mar. 2003.

[19] K. Bult, and A. Buchwald, “An embedded 240-mW 10-b 50 MS/s CMOS ADC in 1-mm^2,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 1887-1895, Dec. 1997.

[20] J.Yuan, and C. Svensson, “New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings,” *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 62-69, Jan. 1997.

[21] B. E. Boser and B. A. Wooley, “The design of sigma–delta modulation analog-to-digital converters,” *IEEE J. Solid-State Circuits*, vol. SC-23, pp. 1298–1308, Dec. 1988.

[22] X. Jiang and M.C.F. Chang, “A 1-GHz Signal Bandwidth 6-bit CMOS ADC With Power-Efficient Averaging” *IEEE J. Solid-State Circuits*, vol. 40, no. 2 pp. 532-535, Feb. 2005.

[23] Christoph Sandner, Martin Clara, Andreas Santner, Thomas Hartig, and Franz Kuttner, “A 6-bit 1.2-GS/s Low-Power Flash-ADC in 0.13-μm Digital CMOS,” IEEE J. Solid-State Circuits, vol. 40, pp. 1499–1505, Jul. 2005.

[24] Erik Säll and Mark Vesterbacka, “6 bit 1 GHz CMOS Silicon-on-Insulator Flash Analog-to-Digital Converter for Read Channel Applications,” ECCTD, Sep. 2005.

[25] Jun-Xia Ma, Sai-Weng Sin, Seng-Pan U , R.P.Martins, “A Power-Efficient 1.056 GS/s Resolution-Switchable 5-bit/6-bit Flash ADC for UWB Applications,” IEEE ISCAS, pp.4305– 4308, 2006.

[26] Vincenzo Ferragina, Nicola Ghittori, Franco Maloberti, “Low-Power 6-bit Flash ADC for High-Speed Data Converters Architectures, ” IEEE ISCAS, pp.3930– 3933, 2006.

[27] Shunsuke Akiyama and Takao Waho, “A 6-Bit Low-Power Compact Flash ADC Using Current-Mode Threshold Logic Gates, ” IEEE ISCAS, pp.3938– 3941, 2006.

[28] Maxim Integrated Products. Dynamic Testing of High-Speed ADCs, Part 2, 2001. http://www.maxim-ic.com/appnotes.cfm/appnote_number/729.

[29] Maxim Integrated Products. Histogram Testing Determines DNL and INL Errors, 2003. http://www.maxim-ic.com/appnotes.cfm/appnote_number/2085.

Appendix

The first cross-coupling type S/H configuration

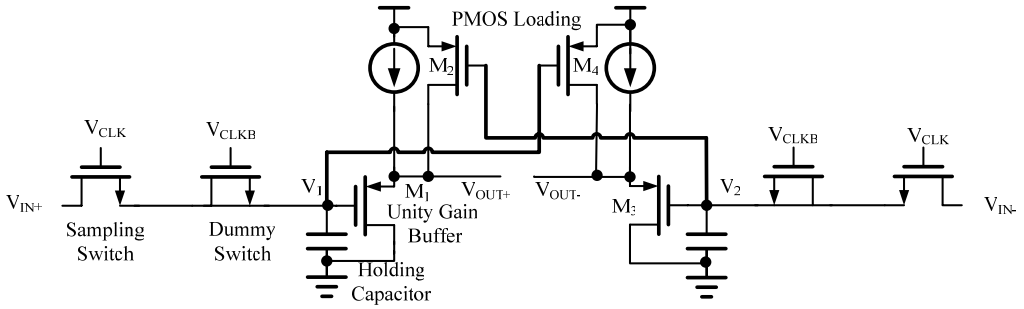


Figure A. 1 The first cross-coupling type S/H Configuration

Gain analysis:

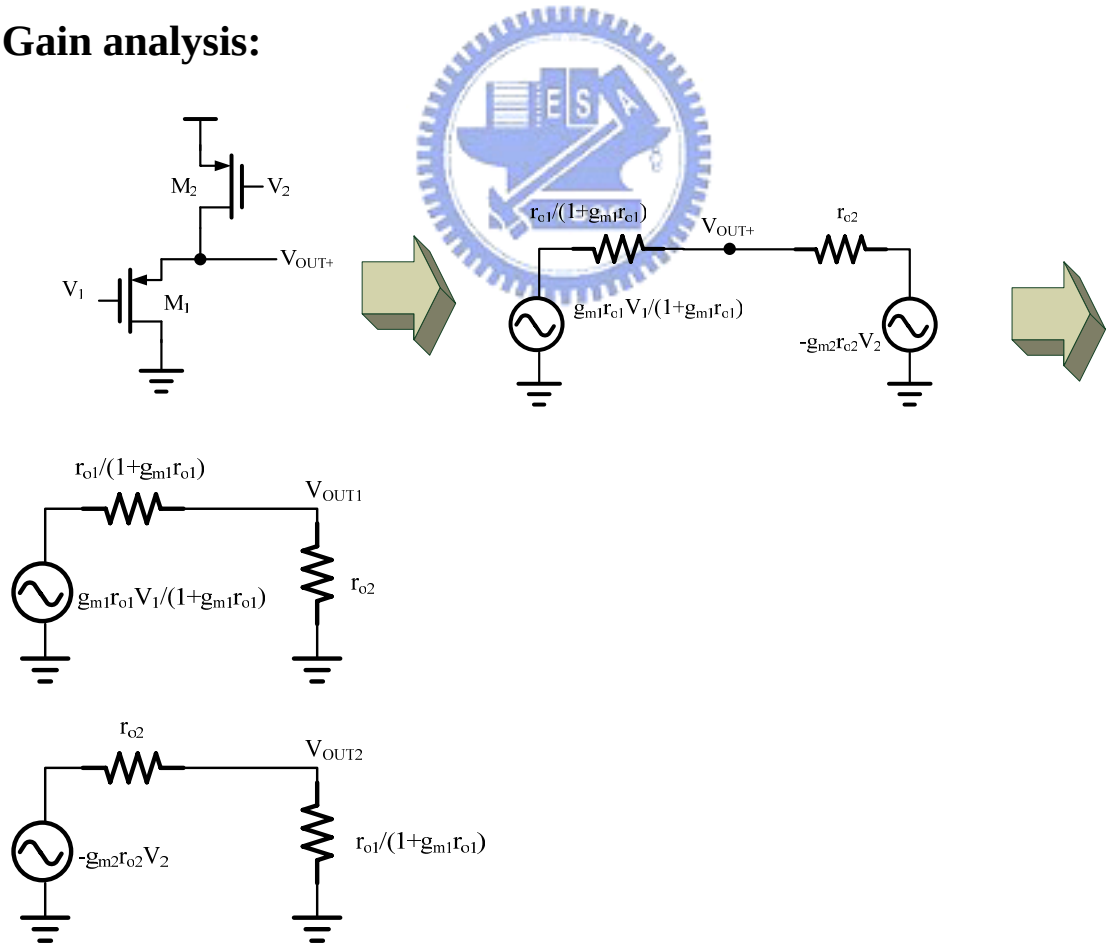


Figure A. 2 The small signal of the first cross-coupling type S/H for gain calculation

$$\frac{V_{OUT1}}{g_{m1}r_{o1}V_1/(1+g_{m1}r_{o1})} = \frac{r_{o2}}{r_{o1}/(1+g_{m1}r_{o1})+r_{o2}}$$

$$V_{OUT1} = \frac{g_{m1}r_{o1}r_{o2}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}V_1 \tag{A.1}$$

$$\frac{V_{OUT2}}{-g_{m2}r_{o2}V_2} = \frac{r_{o1}/(1+g_{m1}r_{o1})}{r_{o2}+r_{o1}/(1+g_{m1}r_{o1})}$$

$$V_{OUT2} = \frac{-g_{m2}r_{o2}r_{o1}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}V_2 \tag{A.2}$$

From figure, use superposition method and then the single output voltage is given by

$$V_{OUT+} = V_{OUT1} + V_{OUT2} = \frac{g_{m1}r_{o1}r_{o2}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}V_1 + \frac{-g_{m2}r_{o2}r_{o1}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}V_2$$

$$V_{OUT+} = \frac{r_{o1}r_{o2}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}(g_{m1}V_1 - g_{m2}V_2) \tag{A.3}$$

Substitute $V_1 = -V_2$ into equation (A.3). Solving this gives gain shown by

$$\frac{V_{OUT+}}{V_1} = \frac{r_{o1}r_{o2}}{r_{o1}+(1+g_{m1}r_{o1})r_{o2}}(g_{m1}+g_{m2}) \tag{A.4}$$

3dB frequency analysis:

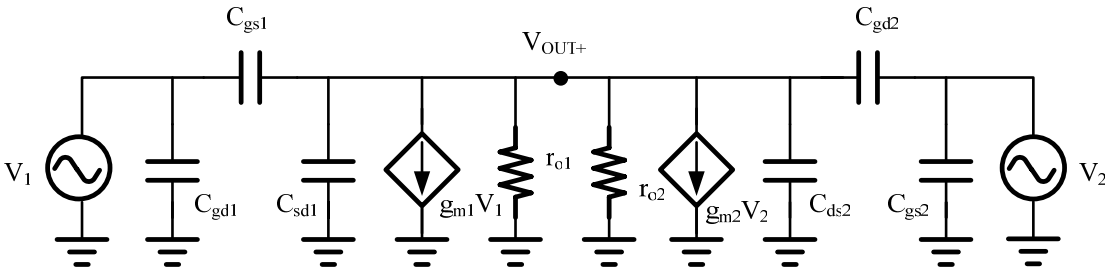


Figure A. 3 The small signal of the first cross-coupling type S/H for 3db frequency calculation

$$\tau_1 = C_{gs1}(r_{o1} // r_{o2}),\ \ \omega_1 = 2\pi f_1 = \frac{1}{\tau_1},\ \ f_1 = \frac{1}{2\pi\tau_1} \tag{A.5}$$

$$\tau_2 = (C_{sd1} + C_{ds2})(r_{o1} // r_{o2}),\ \ \omega_2 = 2\pi f_2 = \frac{1}{\tau_2},\ \ f_2 = \frac{1}{2\pi\tau_2} \tag{A.6}$$

$$\tau_3 = C_{gd2}(r_{o1} // r_{o2}),\ \ \omega_3 = 2\pi f_3 = \frac{1}{\tau_3},\ \ f_3 = \frac{1}{2\pi\tau_3} \tag{A.7}$$

$\omega_1 << \omega_2, \omega_3$ So, ω_1 is a dominant pole and 3db frequency is given by

$$f_{3db} = f_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi C_{gs1}(r_{o1} // r_{o2})} \tag{A.8}$$

The second cross-coupling type S/H configuration

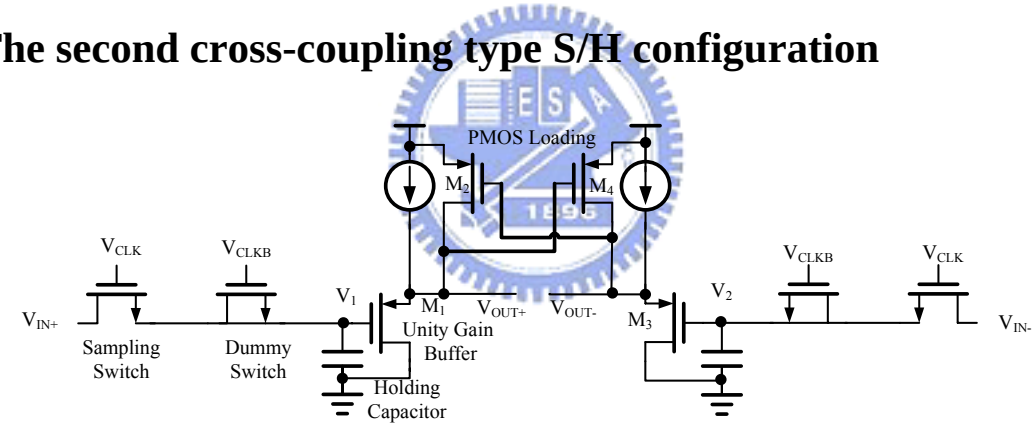
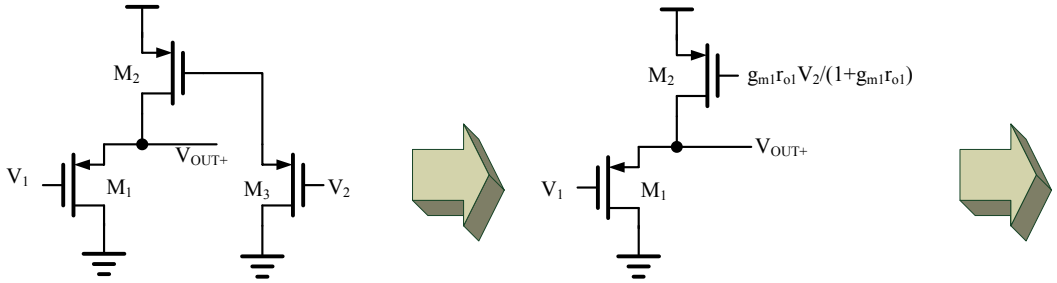


Figure A. 4 The second cross-coupling type S/H Configuration

Gain analysis:



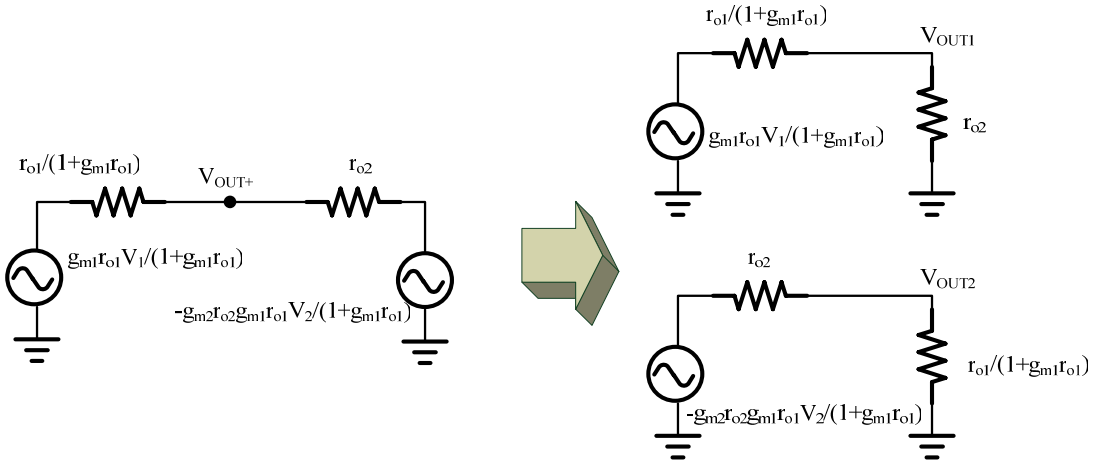


Figure A. 5 The small signal of the second cross-coupling type S/H for gain calculation

$$\frac{V_{OUT1}^{'}}{g_{m1}^{'}r_{o1}^{'}V_1^{'}/(1+g_{m1}r_{o1}^{'})}=\frac{r_{o2}^{'}}{r_{o1}^{'}/(1+g_{m1}^{'}r_{o1}^{'})+r_{o2}^{'}}$$

$$V_{OUT1}^{'}=\frac{g_{m1}^{'}r_{o1}^{'}r_{o2}^{'}}{r_{o1}^{'}+(1+g_{m1}^{'}r_{o1}^{'})r_{o2}^{'}}V_1^{'} \tag{A.9}$$

$$\frac{V_{OUT2}^{'}}{-g_{m2}^{'}r_{o2}^{'}g_{m1}^{'}r_{o1}^{'}V_2^{'}/(1+g_{m1}^{'}r_{o1}^{'})}=\frac{r_{o1}^{'}/(1+g_{m1}^{'}r_{o1}^{'})}{r_{o2}^{'}+r_{o1}^{'}/(1+g_{m1}^{'}r_{o1}^{'})}$$

$$V_{OUT2}^{'}=\frac{-g_{m2}^{'}r_{o2}^{'}r_{o1}^{'}}{r_{o1}^{'}+(1+g_{m1}^{'}r_{o1}^{'})r_{o2}^{'}}\bullet\frac{g_{m1}^{'}r_{o1}^{'}}{1+g_{m1}^{'}r_{o1}^{'}}V_2 \tag{A.10}$$

From figure, use superposition method and then the single output voltage is given by

$$V_{OUT+}^{'}=V_{OUT1}^{'}+V_{OUT2}^{'}=\frac{g_{m1}^{'}r_{o1}^{'}r_{o2}^{'}}{r_{o1}^{'}+(1+g_{m1}^{'}r_{o1}^{'})r_{o2}^{'}}V_1^{'}$$

$$+\frac{-g_{m2}^{'}r_{o2}^{'}r_{o1}^{'}}{r_{o1}^{'}+(1+g_{m1}^{'}r_{o1}^{'})r_{o2}^{'}}\bullet\frac{g_{m1}^{'}r_{o1}^{'}}{1+g_{m1}^{'}r_{o1}^{'}}V_2^{'}$$

$$V_{OUT+}^{'} = \frac{r_{o1}^{'} r_{o2}^{'}}{r_{o1}^{'} + (1 + g_{m1}^{'} r_{o1}^{'}) r_{o2}^{'}} (g_{m1}^{'} V_1^{'} - \frac{g_{m2}^{'} g_{m1}^{'} r_{o1}^{'}}{1 + g_{m1}^{'} r_{o1}^{'}} V_2^{'}) \quad \text{(A.11)}$$

Substitute $V_1^{'} = -V_2^{'}$ into equation (A.11). Solving this gives gain shown by

$$\frac{V_{OUT+}^{'}}{V_1^{'}} = \frac{r_{o1}^{'} r_{o2}^{'}}{r_{o1}^{'} + (1 + g_{m1}^{'} r_{o1}^{'}) r_{o2}^{'}} (g_{m1}^{'} + \frac{g_{m2}^{'} g_{m1}^{'} r_{o1}^{'}}{1 + g_{m1}^{'} r_{o1}^{'}}) \quad \text{(A.12)}$$

3dB frequency analysis:

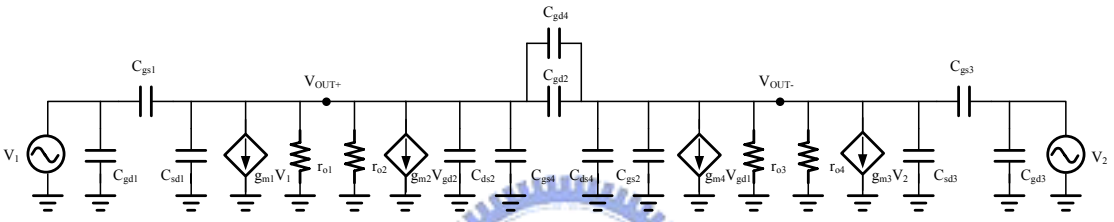


Figure A. 6 The small signal of the second cross-coupling type S/H for 3db frequency calculation

$$\tau_1^{'} = C_{gs1}^{'} \ (r_{o1}^{'} // r_{o2}^{'}), \ \omega_1^{'} = 2\pi f_1^{'} = \frac{1}{\tau_1^{'}}, \ f_1^{'} = \frac{1}{2\pi\tau_1^{'}} \quad \text{(A.13)}$$

$$\tau_2^{'} = (C_{sd1}^{'} + C_{ds2}^{'} + C_{gs4}^{'})(r_{o1}^{'} // r_{o2}^{'}), \ \omega_2^{'} = 2\pi f_2^{'} = \frac{1}{\tau_2^{'}}, \ f_2^{'} = \frac{1}{2\pi\tau_2^{'}} \quad \text{(A.14)}$$

$$\tau_3^{'} = (C_{gd2}^{'} + C_{gd4}^{'})(r_{o1}^{'} // r_{o2}^{'} + r_{o3}^{'} // r_{o4}^{'}), \ \omega_3^{'} = 2\pi f_3^{'} = \frac{1}{\tau_3^{'}}, \ f_3^{'} = \frac{1}{2\pi\tau_3^{'}}$$

(A.15)

$$\tau_4^{'} = (C_{sd3}^{'} + C_{ds4}^{'} + C_{gs2}^{'})(r_{o3}^{'} // r_{o4}^{'}), \ \omega_4^{'} = 2\pi f_4^{'} = \frac{1}{\tau_4^{'}}, \ f_4^{'} = \frac{1}{2\pi\tau_4^{'}}$$

(A.16)

$$\tau_5^{'} = C_{gs3}^{'}(r_{o3}^{'} // r_{o4}^{'}),\ \ \omega_5^{'} = 2\pi f_5^{'} = \frac{1}{\tau_5^{'}},\ \ f_5^{'} = \frac{1}{2\pi\tau_5^{'}} \tag{A.17}$$

$\omega_1^{'} = \omega_5^{'},\ \ \omega_2^{'} = \omega_4^{'},\ \ \omega_1^{'} << \omega_2^{'}, \omega_3^{'}$ So, $\omega_1^{'}$ or $\omega_5^{'}$ is a dominant pole

and 3db frequency is given by

$$f_{3db}^{'} = f_1^{'} = \frac{1}{2\pi\tau_1^{'}} = \frac{1}{2\pi C_{gs1}^{'}(r_{o1}^{'} // r_{o2}^{'})} \tag{A.18}$$

簡　　歷

姓　名：　陳世基

性　別：　男

籍　貫：　台灣省新竹縣

生　日：　西元 1973 年 2 月 7 日

地　址：　新竹縣竹北市新光街 31 巷 6 號

學　歷：　國立交通大學 電機學院 電子與光電學程 碩士班 2003/09 ~ 2007/06

私立高雄工學院 電子工程學系 1992/09 ~ 1996/06

經　歷：　鈺創科技股份有限公司 測試工程師 2000/06 ~ 2006/09

科榮股份有限公司 設備工程師 1998/06 ~ 2000/04

論文題目：　A Low-Power High-Speed A/D Converter Design for UWB Wireless Applications

超寬頻無線網路應用之低功率高速類比數位轉換器設計