國　立　交　通　大　學

電機資訊學院　電子與光電學程

碩 士 論 文

具有自我校正功能之 2.5Gsps 四階脈衝振幅調變接收器
A 2.5Gsps Self-calibrating 4-PAM Receiver

指導教授：李崇仁 蘇朝琴 教授

研 究 生：紀順閔

中 華 民 國 九 十 五 年 九 月

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研 究 生：紀順閔　　Student : Shunmin Chi

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國 立 交 通 大 學

電機學院與資訊學院　電子與光電學程

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所提論文:（中文）具有自我校正功能之 2.5Gsps 四階脈衝振幅調變接收器

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合於碩士資格水準、業經本委員會評審認可。

口試委員：

指導教授：

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中 華 民 國 95 年 9 月 5 日

具有自我校正功能之 2.5Gsps
四階脈衝振幅調變接收器

研究生 : 紀順閔　　指導教授 :李崇仁 教授

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摘　要

在這篇論文中包含了兩個主題，高速類比數位轉換器以及其校正電路。首先，我們將焦點放在高速類比數位轉換器的電路設計方法，係提出利用三態反相器的電壓轉換特性曲線的原理，藉由金屬氧化半導體不同的面積比例，產生不同臨界電壓的反相器來當作比較器。屆時利用任務週期的校正方式，來選擇幾個適當的比較器工作。接在比較器後端的是以三態反相器為基礎的多工器，對訊號具有逐級放大的增益效果。除此之外，在三態反相器的輸出端接上一個二極體式的電感性增益電路，可以提升訊號在高頻的表現。整體高速類比數位轉換器都是由三態反相器所組成，可以大量減少面積和達到高速的效能。另外，可以關閉沒有用到的三態反相器，以減少功率消耗。

接著，我們說明校正電路的機制。以類比訊號或多階層訊號而言，輸入訊號經過不同臨界電壓的比較器，便會產生不同任務週期的方波輸出。以一個四階脈衝振幅調變訊號而言，我們選擇最接近 75%、50%、25%任務週期的比較器可以解析出最佳數位訊號。我們採用次取樣的方式來計算各比較器的任務週期，取最接近理想任務週期之比較器，當成校正後的比較器。取樣頻率越低，功率消耗越少。隨機取樣的次數為 128 次，即為 7 位元的計數器。根據統計分析的推估結果，其校正效果等同於在 300 毫伏特的輸入訊號下，可以達到 99.35%以上的可信度選到最佳的通道。

本論文所提出的四階脈衝振幅調變接收器，其高速類比數位轉換器具有架構簡單、高速、低功率消耗以及小面積等優點；而其校正電路更使類比數位轉換器達到高準確度和降低製程變異的影響，還有低功率消耗的優點。

關鍵字：類比數位轉換器，比較器，脈衝振幅調變接收器，校正，次取樣。

A 2.5Gsps Self-calibrating 4-PAM Receiver

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Advisors: Dr. Chunglen Lee
Dr. Chauchin Su

Degree Program of Electrical Engineering and Computer Science
National Chiao Tung University

Abstract

This thesis proposes a high-speed *analog-to-digital converter* (ADC) and its calibration circuit. First, we focus on the design of high-speed ADC. We propose comparators by means of adjusting the aspect ratio of tri-state inverters to generate different threshold voltages. In this way, we can select some proper comparator working by duty cycle estimation. Connecting at the end of comparators are tri-state inverter based multiplexers. They have gain boosting effects. Besides, the diode connected inductive peaking circuit which is attached to the output of a multiplexer can enhance the performance at high frequency. The whole ADC is composed by tri-state inverters. It reduces the hardware overhead and achieves high-speed performance. Additionally, the inactive tri-state inverters can be properly switched off to reduce the power consumption.

Second, we illustrate the scheme of calibration. As far as an analog signal or multi-level signal is concerned, it outputs square waves with various duty cycle when input signal is passing through the comparator array with different threshold voltages. For a *4 level pulse amplitude modulation* (4-PAM) signal, we choose the comparators which are the closet to 75%, 50%, and 25% duty cycles for the best conversion. We make the duty cycle estimation by undersampling to select the optimal comparators as calibrated channels. The lower sampling frequency it is, the

less power dissipation it has. We make it undersampling 128 times which is equals to a 7-bit counter. According to the statistical analysis, we can have over 99.35% confidence level out of an input of 300mV swing to have the optimal channels after the calibration.

4-PAM receiver is proposed in this thesis. The ADC has advantages of simple structure, high-speed, low power consumption, and small area. The calibration circuit makes it highly accurate, and less impacted by process variation.

Index Terms: PAM receiver, *threshold inverter quantization* (TIQ), flash ADC, comparator, calibration, undersampling.

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再者，感謝鴻文的傾囊相授，給了許多寶貴的建議；感謝丸子解決了我們在實驗室裡遇到大大小小的事情；還有感謝陪我一路走來的學長、同學及學弟們，你們的相互扶持讓我感覺到人間有溫情，我也會記得大家一起奮戰，一起打球的歡樂時光。衷心的祝福各位健康快樂，順心如意。

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Chapter 1

Introduction

1.1 Motivation

Advance in process technology coupled with aggressive circuit design, has led to an explosive growth in speed and circuits integration complexity. For these improvements, to enhance overall system performance, the communication speed between systems and integrated circuits must increase accordingly. As the demand of mass transmission increases, it has become an inevitable trend to transmit at higher data rate in finite channels. Naturally, the importance of high speed link technology is on the rise.

Besides binary signal transmission, we develop multilevel signal transmission in high-speed link structures. For instance, the 4-PAM system carries double data capacity than binary transmission. Speed limitations due to process are completely examined by PAM scheme. For a given data rate, the 4-PAM scheme reduces half symbol rate compared to a conventional 2-PAM system. The symbol rate reduction decreases not only the required clock frequency, but also the *inter symbol interference* (ISI) jitter which impacts data eye-opening.

Because of noise sources, such as crosstalk between channels, or electro magnetic interference, they impact signal integrity. In addition, reflections due to impedance mismatch, signal degradation in channels, skin effects, ISI, and process variation make it difficult to receive data correctly in high-speed communication.

The signal integrity becomes a dominant factor for reliability and performance in communication system.

We hope to create a flash ADC by simple tri-state inverters with advantages of low power and small area. Random sampling in the comparator output, we can estimate the duty cycle of each comparator. Further more, we can precisely select the best comparators for the specific input signal by calibration. The self-calibrating ADC minimizes the impact of process variation and temperature, and achieves high-speed performance.

1.2 Thesis Organization

This thesis comprises five chapters summarized as below:

Chapter 1 reviews the present state of high-speed links, advantages of PAM transmission, and noise source impacting to signal integrity. Then we have the motivation to make a self-calibrating PAM receiver.

Chapter 2 illustrates three types of flash ADC architectures, inclusive of conventional flash converters, *threshold inverter quantization* (TIQ) flash converters, and modified TIQ flash converters. The modified TIQ architecture for high-speed operation is proposed. It describes some key methods to enhance high-speed and power-efficient performance.

In chapter 3, in order to improve the flash ADC accuracy, we develop a calibration scheme to select the best comparators and channels. This chapter describes the methodology of calibration, design considerations, and its confidence level through statistical analysis. It shows how we strike a balance among accuracy, hardware, and calibration time.

Chapter 4 shows simulated results, layout, and specification comparison. We check the ADC output waveform of corner cases before fed into *clocked data recovery* (CDR). Besides, we further analyze the calibration result to see if it coincides with our expectation. Last, we compare this work to other state-of-the-art in performance.

Chapter 5 describes the measurement items, configurations, test considerations, signal generation, and test flows. We proposed two sources for 4-PAM signal generation.

Finally, chapter 6 summarizes the advantages and the creativities of this work.

Even we can apply these key ideas to enhance the functionality.

Chapter 2

High Speed CMOS ADC Architectures

ADCs come in several basic architectures, although many variations exist for each type. Each type has advantages and disadvantages with a particular combination of speed, accuracy, and power consumption. They all fit into a particular application. For example, a digital oscilloscope needs high digitizing speeds but can sacrifice resolution, so it uses flash converters. Some communication devices use pipeline ADCs, which provide better solution than flash converters, but at the expense of speed. General data-acquisition equipments usually adopt successive approximation registers. And audio coders use sigma-delta converters for high resolution. In this chapter, we will focus on flash converters and its derivatives, inclusive of conventional flash ADCs, TIQ ADCs, and my proposal, modified TIQ ADCs.

2.1 Conventional Flash ADC [1]-[2]

The conventional flash architecture is the simplest and fastest analog-to-digital converter. In a typical flash ADC, the analog input signal is simultaneously compared to reference voltages by a string of comparator circuits, as shown in Figure 2.1. As the input voltage increases, the comparators set their outputs to logic 1, starting with the lowest comparator. Think of the flash converters as being like a mercury thermometer.

As temperature increases, the mercury rises. Likewise, as the input voltage rises, comparators referenced to higher voltages set their outputs from 0 to 1. The thermometer code is encoded into binary code. The reference voltages are provided by connecting to a resistor string to generate the monotonic increase of reference voltages of full scale.

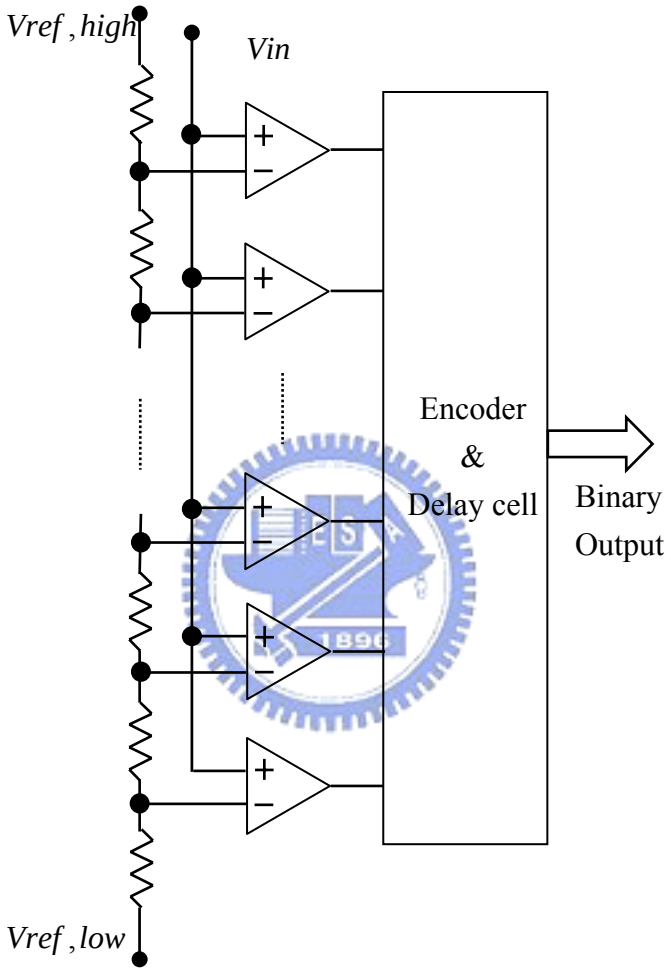


Figure 2.1 Conventional flash ADC architecture.

For an N-bit flash ADC, $2^N - 1$ comparators and 2^N resistors are required. Flash ADCs are fast, but they have drawbacks. When resolution increases, the amounts of comparators and resistors grow exponentially, and they consume considerable power. As a result, most flash ADC studies have been focused on less than 8-bit resolution.

As for error sources in flash ADCs, reference circuit linearity and charge

feed-through errors are the most popular. A primary factor determining the basic DC linearity of any flash ADC is the match that is obtained in the elements of the resistor divider. Matching of the resistor ladder elements is dependent on geometry in fabrication process. Analog MOS switches used for the reference and feedback switches, inevitably develop undesirable parasitic capacitances between the gate and source/drain terminals, as shown in Figure 2.2. When the MOS switches are turned off, transient currents flowing through the parasitic capacitances can alter the charge which is finally stored on the input coupling capacitor of the comparator. Charge feed-through may cause offset error and gain error in the conversion. [3]

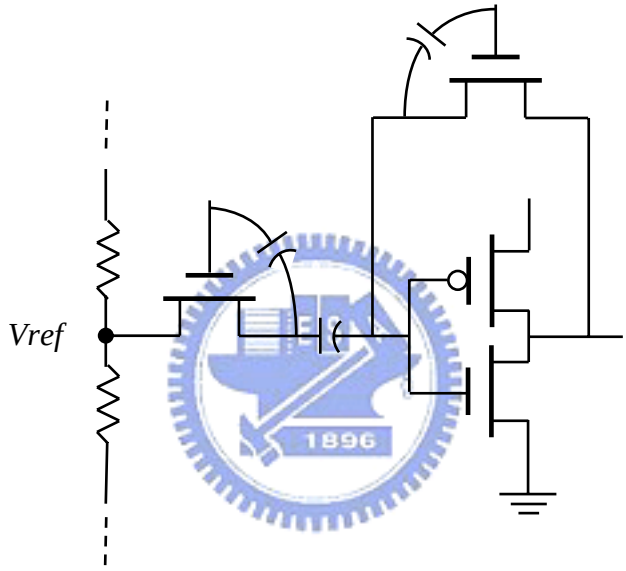


Figure 2.2 Parasitic capacitors in CMOS switches.

2.2 Threshold Inverter Quantization

Flash ADC [4]-[8]

The conventional flash ADC is considered to realize the fastest conversion rate but it suffers from not only larger chip size and larger power dissipation, but also lower dynamic performance due to large input capacitance. Consequently, another simpler flash converter named TIQ flash ADC is proposed. Figure 2.3 shows the block diagram of 4-bit TIQ containing 15 comparators, gain boosters and an encoder.

The idea is to use the digital inverters with various threshold voltages as analog voltage comparators. The gain boosters make sharper transition of comparator output and provide full swing. The encoder converts the thermometer code to the binary code in two steps.

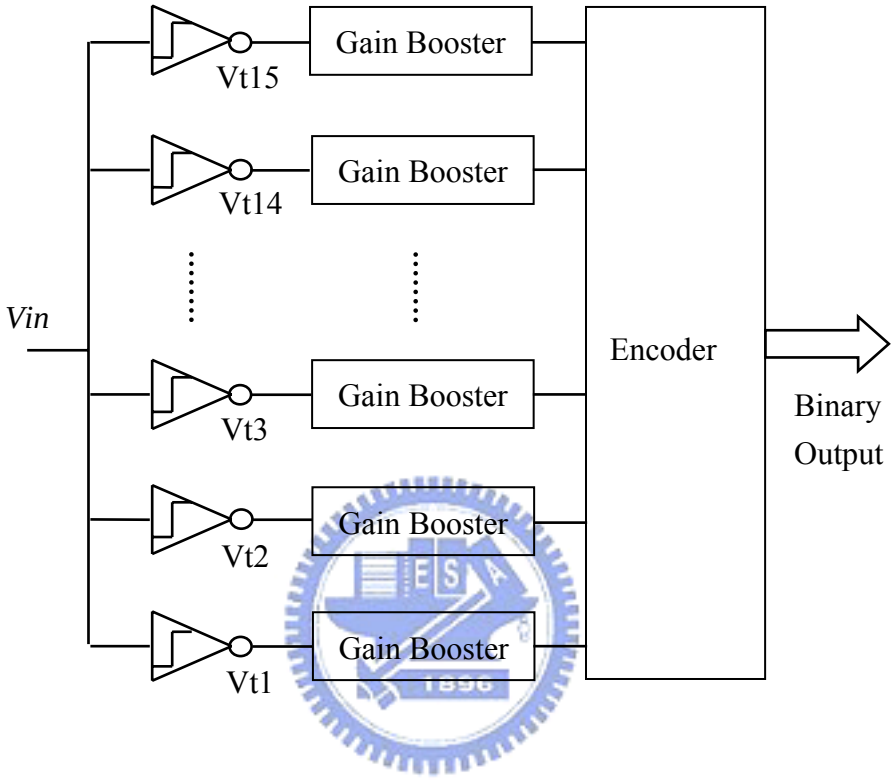


Figure 2.3 Block diagram of 4-bit TIQ.

By adjusting the aspect ratio of inverters, we can get various threshold voltages. When we want a higher threshold voltage, we can enlarge the width PMOS or shrink the width of NMOS. We get lower threshold voltage in the opposite way. The various threshold comparators are arranged in parallel and monotonically, as shown in Figure 2.4. In conventional flash converters, the comparators are identical, while the comparators are different in the TIQ based flash ADC. The TIQ technique has many advantages:

(1) Simpler voltage comparator circuits.

(2) Faster voltage comparison speed.

(3) Elimination of resistor ladder circuits.

(4) Do not need switches, clock signal, and coupling capacitors.

(5) Compatible with CMOS process, and ideal for SOC implementation.

But it has two criteria to be carefully considered as following:

(1) ADC input range varies due to process parameter changing form one fabrication to another.

(2) An inverter is single ended, not differential, causing the ADC to become more susceptible to noise.

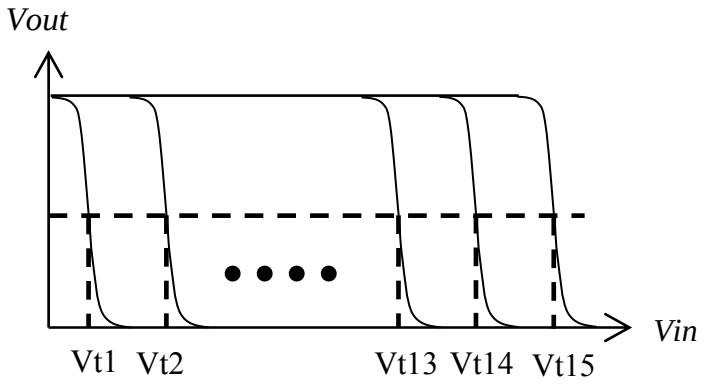


Figure 2.4 Voltage transfer curve of 15 comparators

The most critical issue for the *threshold inverter* (TI) comparator is the process variation. It impacts the offset, gain, and linearity of the conversion range. One solution is to add a programmable pre-amplifier to the analog input of the ADC in order to dynamically adjust the offset, gain, and linearity.

Other issues for the TIQ flash ADCs are temperature variation, power supply variation, and single ended input noise. The former two problems can be solved by DSP solution; the later noise issue also can be solved by adding a single differential input amplifier to recondition the ADC input signal.

As compare to conventional flash converters, they have some characteristics in common, such as high-speed conversion and sensitive to process variation. But TIQ flash ADCs have advantages of lower power consumption and smaller chip penalty.

2.3 Modified TIQ Flash Converter Architecture

As we mentioned in the previous section, the TIQ flash ADC has some merits in power consumption and small area. Further more, we want to enhance its high-speed characteristic and signal integrity. We replace the threshold inverters with tri-state inverters for power saving, and add inductive peaking circuits for high-speed performance. We take tri-state inverter based *multiplexer* (MUX) instead of cascading inverters for gain boosting. The modified TIQ flash ADC schematic is shown as Figure 2.5, and the design concepts is described as below.

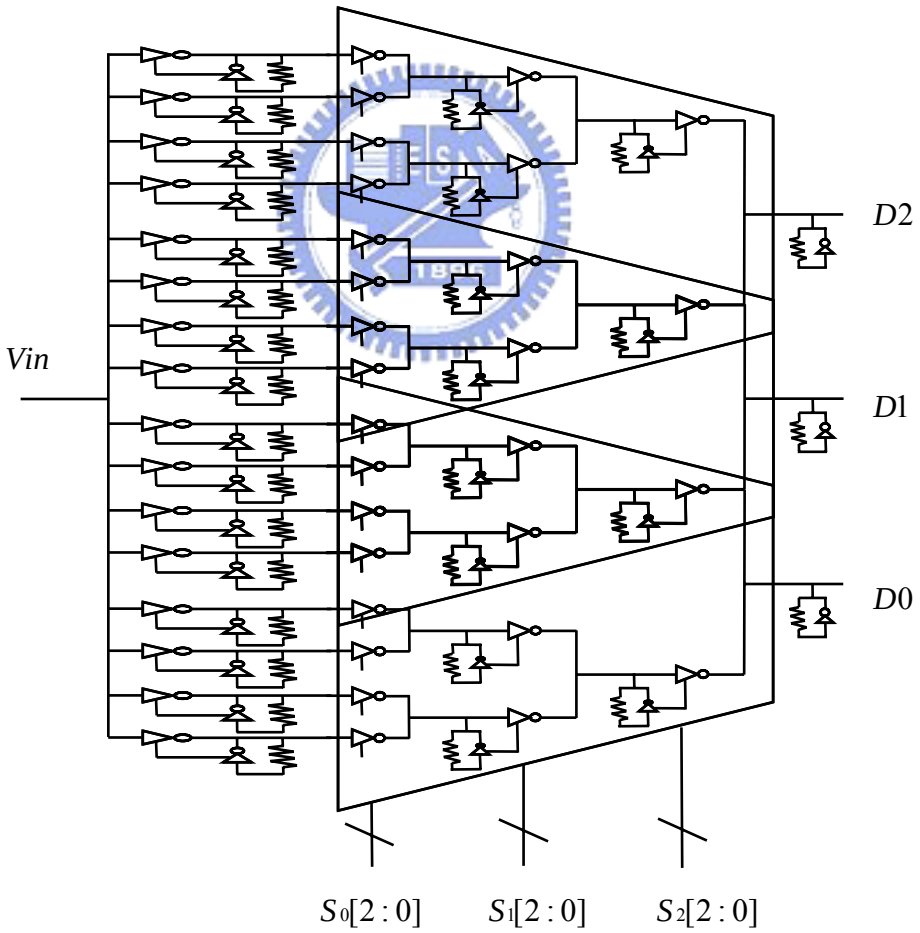


Figure 2.5 Schematic of the modified TIQ flash ADC.

2.3.1 Comparator Design

In 4-PAM transmission, we require three accurate comparators which equal to 2-bit ADC to convert 4-level signal. In order to achieve accurate performance for variable signals in 4-PAM transmission, we make sixteen floating comparators of monotonic threshold voltages in an ADC. We are going to select three accurate comparators among the floating comparators through calibration for the conversion. We replace inverters with tri-state inverters because they can be properly switched on or off. [9]

We take tri-state inverters as threshold comparators for the advantages of simple structure, high speed, low power, small area, and controllability. The unnecessary threshold comparators can be switched off to save power. We have a little overhead, but greatly improve power consumption. We put the enabling switches of tri-state inverters on the power side and ground side as shown in Figure 2.6. They can be pre-charged and perform better high frequency response. In this work, we set the conversion range from 600mV to 1200mV in the modified TIQ ADC. In addition, we attach the inductive peaking circuits at the output of comparators. It sacrifices gain but gets bandwidth to enhance high-speed performance. This will be discussed later.

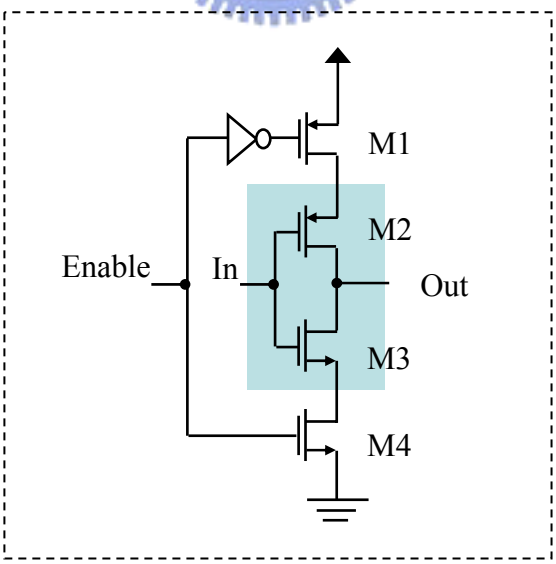


Figure 2.6 Schematic of the tri-state inverter.

2.3.2 Multiplexers [10]-[12]

The comparator outputs connect the inputs of tri-state inverter based MUX and we have three multiplexers coinciding with the three selected comparators. Consider that 16 comparators corresponding to 24 inputs of multiplexers, there are partial overlaps for the sake of small signal coverage and accuracy. [13] The 8-to-1 MUX is composed of tri-state inverters, inductive peaking circuits, and control logics. The tri-state inverters work as gain booster, while inductive peaking components enhance high-speed characteristics. The MUX allows only one path which represents the matching comparator, and the control logics switch off the inactive tri-state inverters to save power as shown in Figure 2.7.

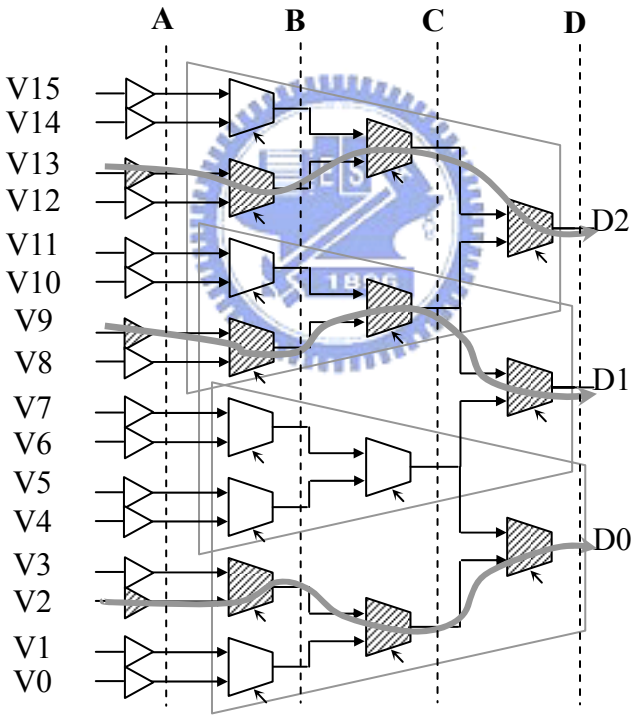


Figure 2.7 TIQ based ADC

Because tri-state inverter is the most used component in the circuits, needless to say, we must optimize it. We enlarge the width enabling MOS so that it drains larger current. Thus we get a multiplier of 4, and about 65ps transition time as shown in Figure 2.8. For signal balance consideration, we seek for the optimum of MOS sizing.

The crossing point in Figure 2.9 is the optimum for PMOS and NMOS. Only when pull-up current and pull-down current strike a balance, the tri-state inverter behaves well.

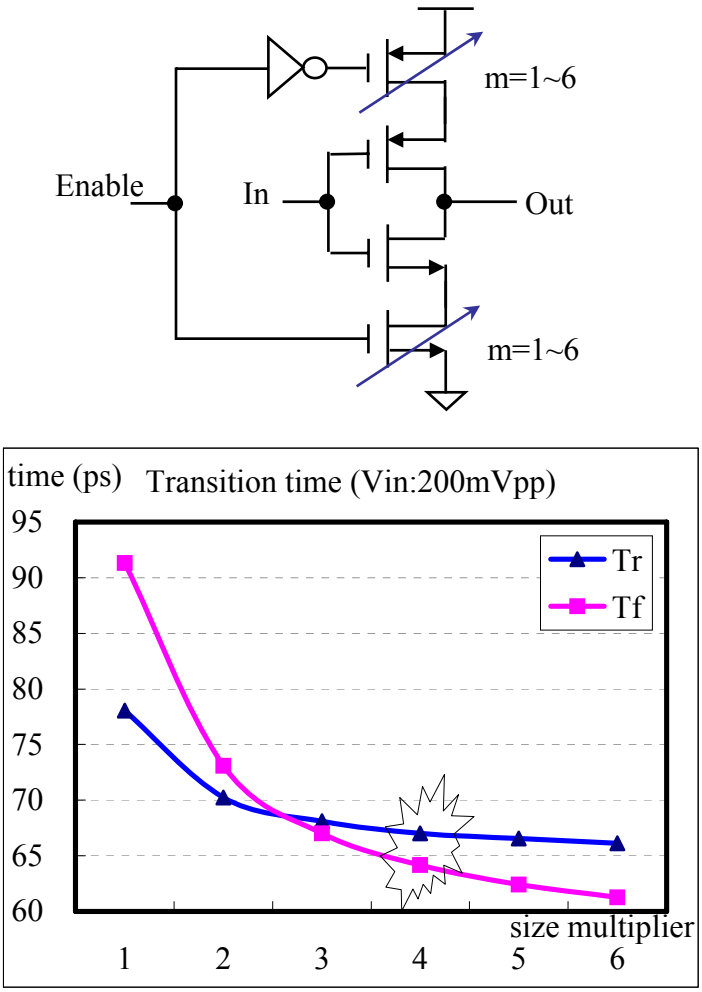


Figure 2.8 Enabling MOS sizing

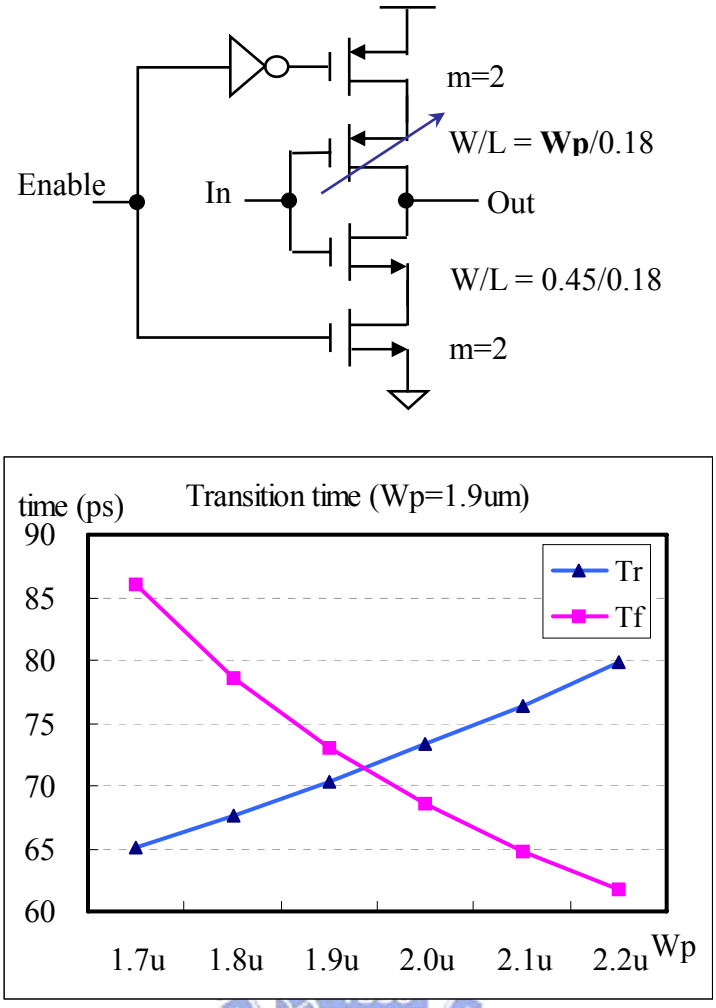


Figure 2.9 Inverter sizing

The MUX also has gain boosting effects due to cascading tri-state inverters shown in Figure2.10. Because of inductive peaking, we intentionally use a gain factor of 2. When receiving a decayed signal of 100mV swing, it is amplified stage by stage to 1600mV at the output of the MUX.

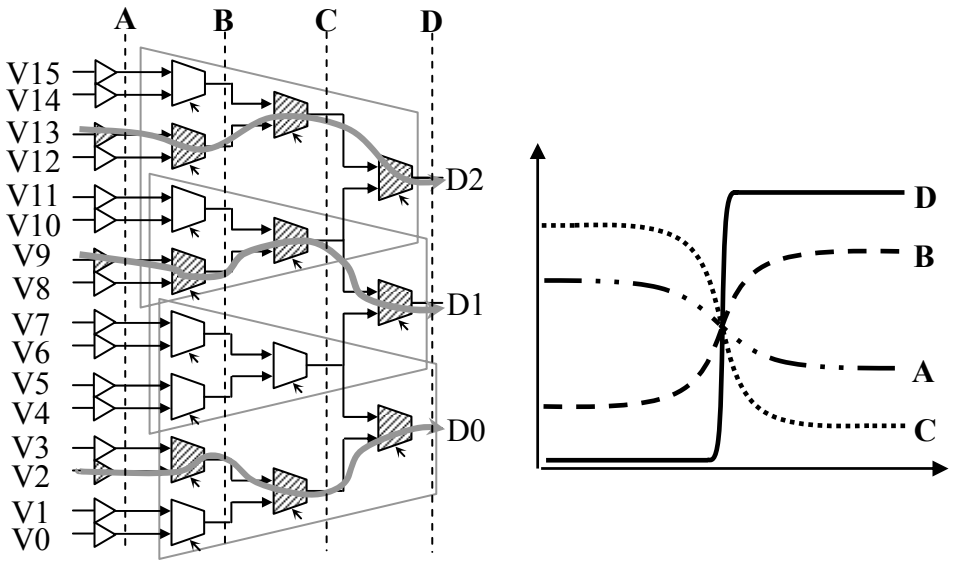


Figure 2.10 Gain boosting of TIQ based ADC

2.3.3 Inductive Peaking Circuits [14]-[15]

As we mentioned in the previous two sections, adding inductive peaking cells at the outputs of tri-state inverters can improve high-speed performance. The inductive peaking cells are identical in the MUX, while they are different in the threshold comparator bank accordingly. Each cell consists of a tri-state inverter and a resistor. The tri-state inverter is configured as diode connected by a resistor which is replaced with a transmission gate. In Figure 2.11, it shows the schematic of threshold comparator with and without inductive peaking component.

The short path between input and output of the tri-state inverter clamps at 0.9V of DC level. The connection of inductive peaking circuit lowers the output resistance of the tri-state inverter, and so does the gain. As a result, knee frequency increases as output resistance decreases. At low frequency, the output resistance is about $1/gm$, while it roughly equals to the resistance of transmission gate at high frequency. It is intended to design the resistance of transmission gate larger than $1/gm$, so it obtains larger gain and extends bandwidth at high frequency. The broadband technique is inductive peaking. The Figure 2.12 is a “Gain-Bandwidth Plot” about inductive peaking. Because the circuits consume more power, we take tri-state inverters instead of inverters. Thus the inactive inductive cells can be properly turned off.

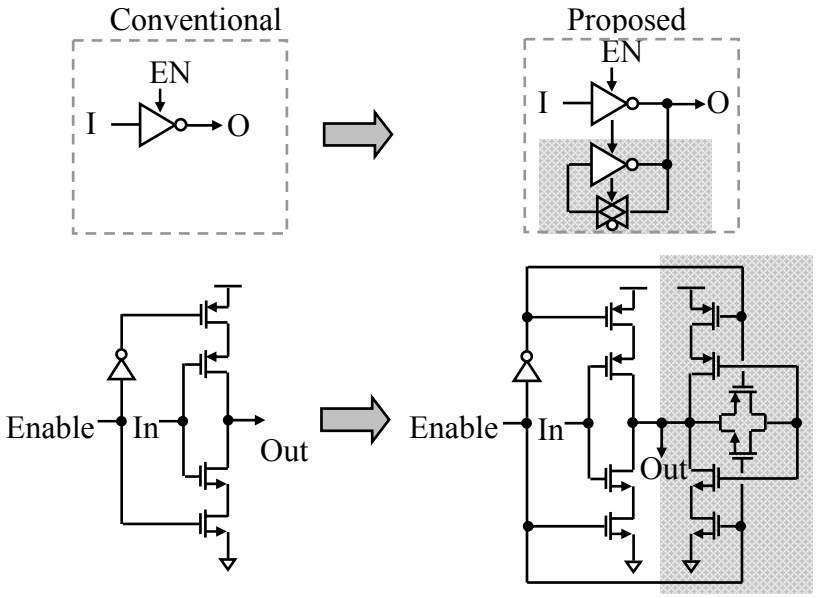


Figure 2.11 Schematic of inductive peaking circuits

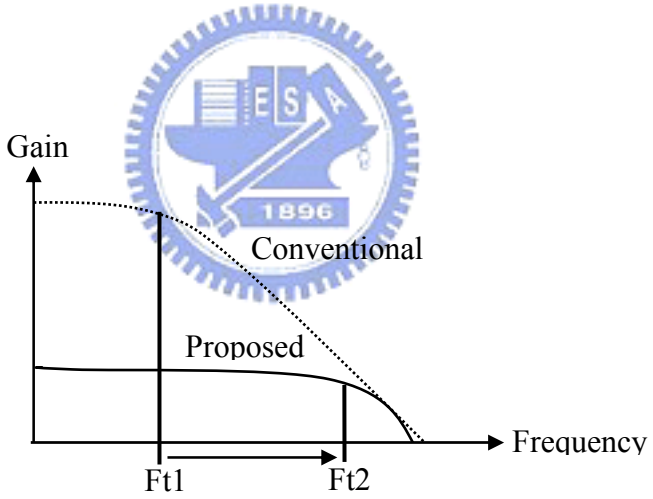


Figure 2.12 Gain-Bandwidth plot of inductive peaking

Chapter 3

Design of ADC Calibration

We realize calibration scheme by threshold voltage modulation. In other words, feeding a periodic signal to a comparator bank of various threshold voltages, it produces digital outputs of various duty cycles. The duty cycle is proportional to the portion of the threshold of input signal as shown in Figure 3.1. We randomly strobe the digital outputs to estimate the duty cycle of a channel by undersampling. After a great deal of counting, we can precisely obtain the duty cycle of the channel. Additionally, undersampling has a significant benefit: Power dissipation is proportional to clock rate, so we can save power by reducing the sampling frequency.

For a comparator array with the same input frequency, a larger swing has closer duty cycle outputs due to its sharper slope. The denser the duty cycles are, the more accuracy we will have in the calibration. So far as 4-PAM signal is concerned, the center between two levels is the best threshold voltage for conversion. In other words, the three ideal duty cycles of comparators should be 75%, 50%, and 25%.

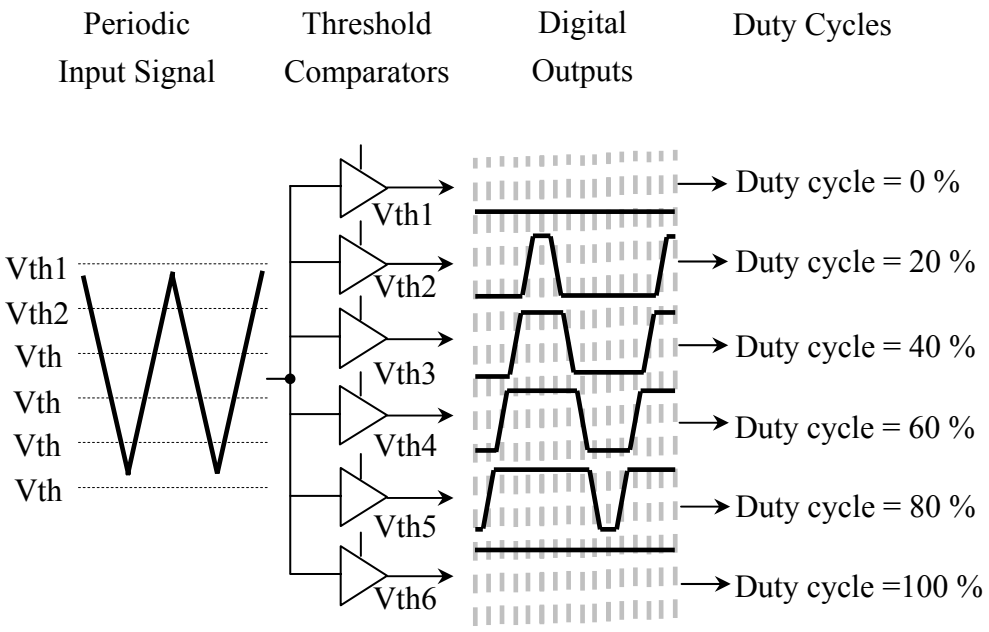


Figure 3.1 Threshold comparators and duty cycles

3.1 Schematics of Calibration

The calibration circuits consist of a duty cycle estimator, an absolute offset comparator, a minimum register, channel select registers, a channel select counter, a level select counter, and a controller. [16] The block diagram is shown in Figure 3.2.

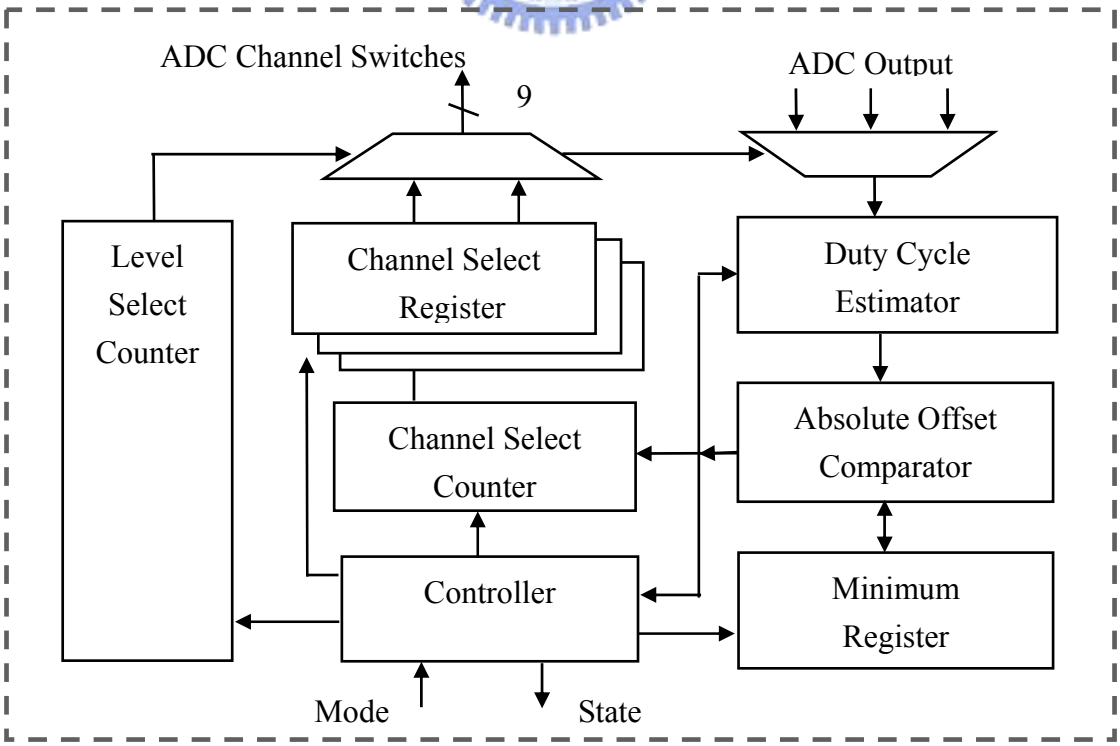


Figure 3.2 Block diagram of calibration

3.1.1 Duty Cycle Estimator

In Figure 3.3, this module is composed of a stimulus timer and a counter. The timer is triggered by undersampling clock, and the counter is sampling data from MUX outputs synchronously. We can easily calculate the percentage of "one" which is so called "duty cycle" in the counting.

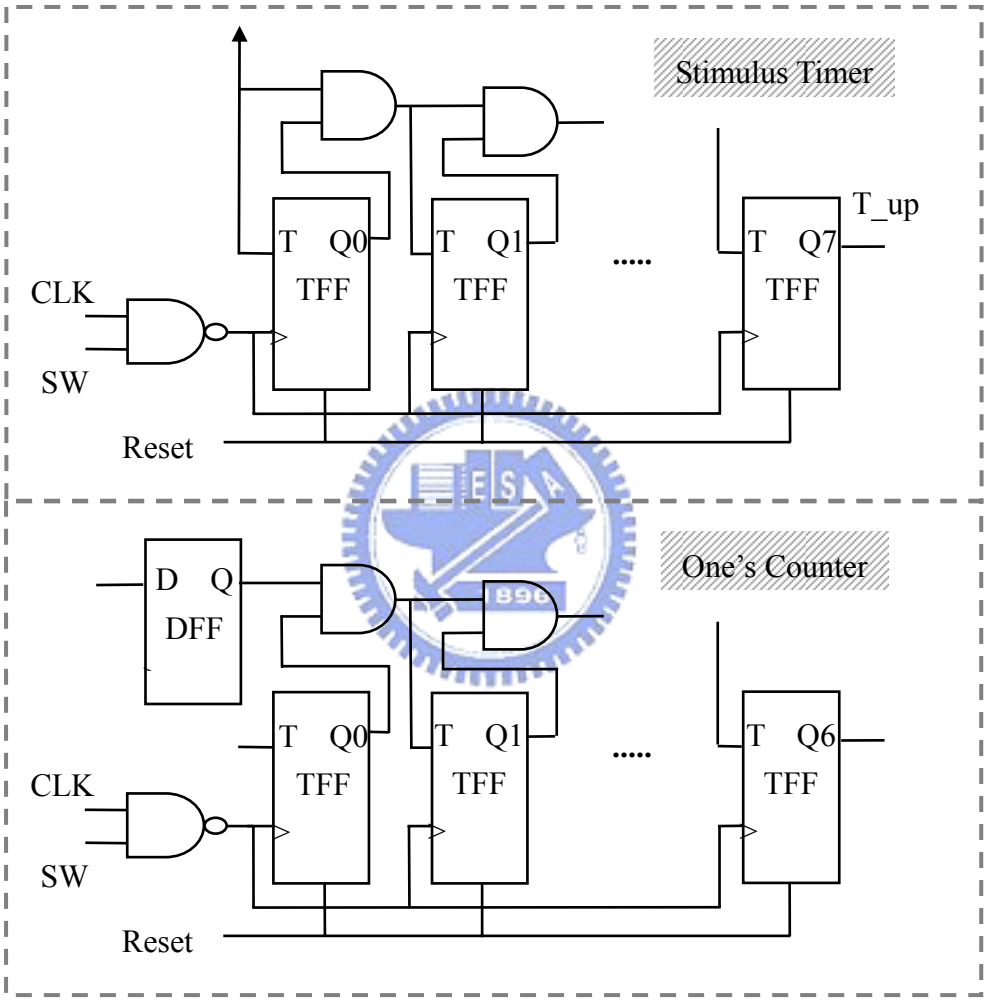


Figure 3.3 Schematic of duty cycle estimator

3.1.2 Absolute Offset Comparator

The absolute offset comparator judges which channel is the closet to the target duty cycle of a MUX. An easy way to find out the best channel is to compare their "distance" to the target. The "distance" here is the absolute difference between

sampled number and target number. So it is a digital comparator which compares the sampled value to the temporary minimum. When the absolute offset value is less than temporary minimum, the temporary minimum will be updated by the absolute offset value in the minimum register.

In Figure 3.4, "D" represents absolute offset value while "Q" stands for minimum value in the comparator cell. When counting number is less than the target, "INV" activates to make one's complement for subtraction to get a positive value. The implementation of one's complement is easier than that of two's complement in digital system, but it has "one" error in one's complement. When the sampling value is very large, this error can be ignored.

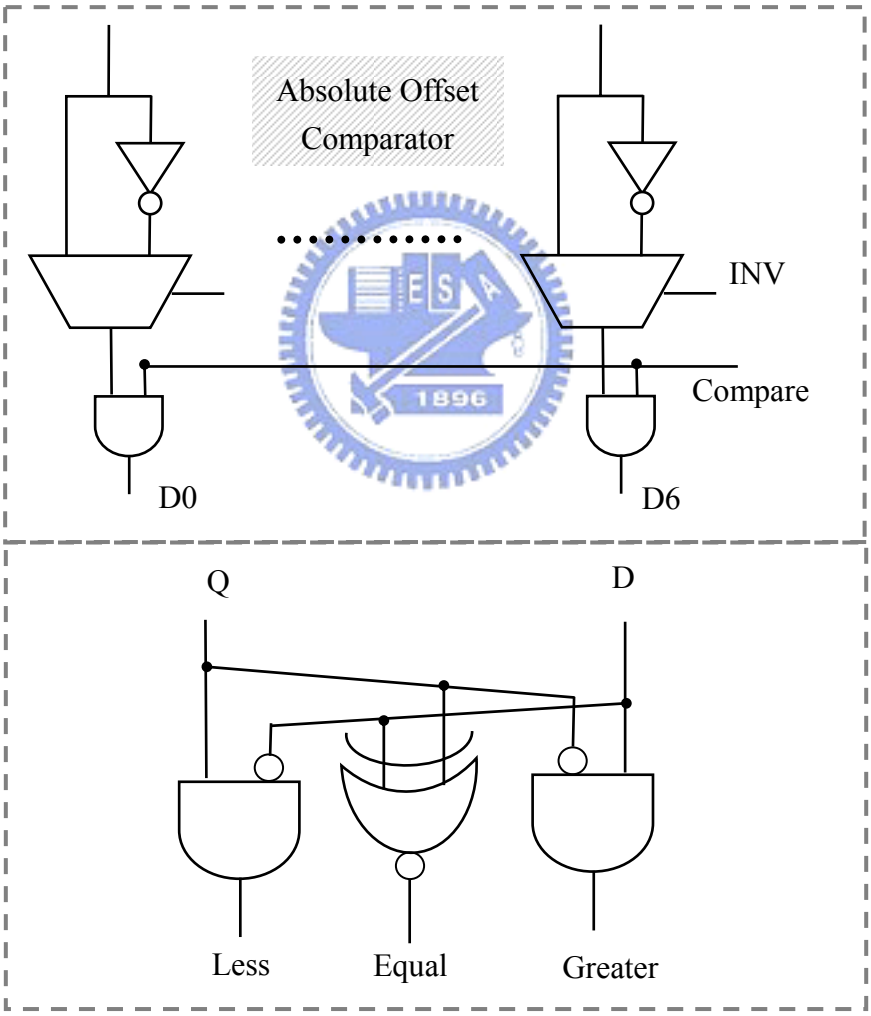


Figure 3.4 Schematic of absolute offset value

3.1.3 Minimum Register

The minimum register is a "parallel in, parallel out" register as shown in Figure3.5. It reloads absolute offset value when "Less" signal triggers the *data flip flops* (DFF). To trigger it by "Less" signal can save more power than by clock signal, and avoid error of critical path delay from the comparator.

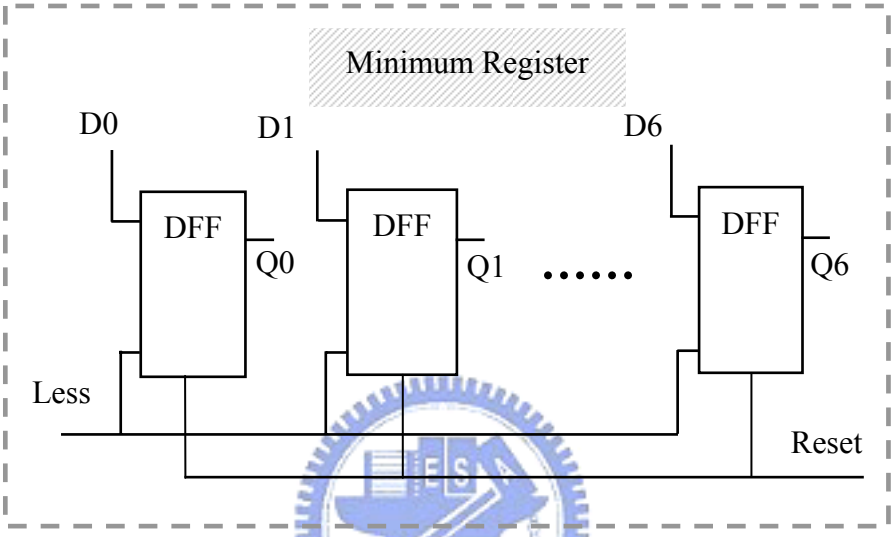


Figure 3.5 Schematic of minimum register

3.1.4 Channel Select Counter / Registers

Duty cycle estimator evaluates the channels one by one through channel select counter. The channel select registers update the channel numbers when minimum register update occurs. Thus optimal channel numbers are stored in the registers after calibration. The schematics of channel select counter and register are configured as one's counter and minimum register respectively in previous sections, but they have only 3 bits.

3.1.5 Level Select Counter

Level select counter is the same schematic as channel select counter. It makes an increment when the estimation of a MUX is finished. There are three threshold comparators to be determined through level select counter.

3.1.6 Controller

The calibration controller is built in combinational logics. It commands other function blocks to act and being triggered by them for state transition. The state machine tells the status of calibration and it is helpful to debug.

3.1.7 Self-calibrating PAM Receiver Architecture

The self-calibrating 4-PAM receiver includes two blocks: 2-bit ADC and calibration circuits. We build some control pins between the interfaces for testing considerations as shown in Figure 3.6. Such as manual switches for manually select channels, it helps us to test device characteristics and debug.

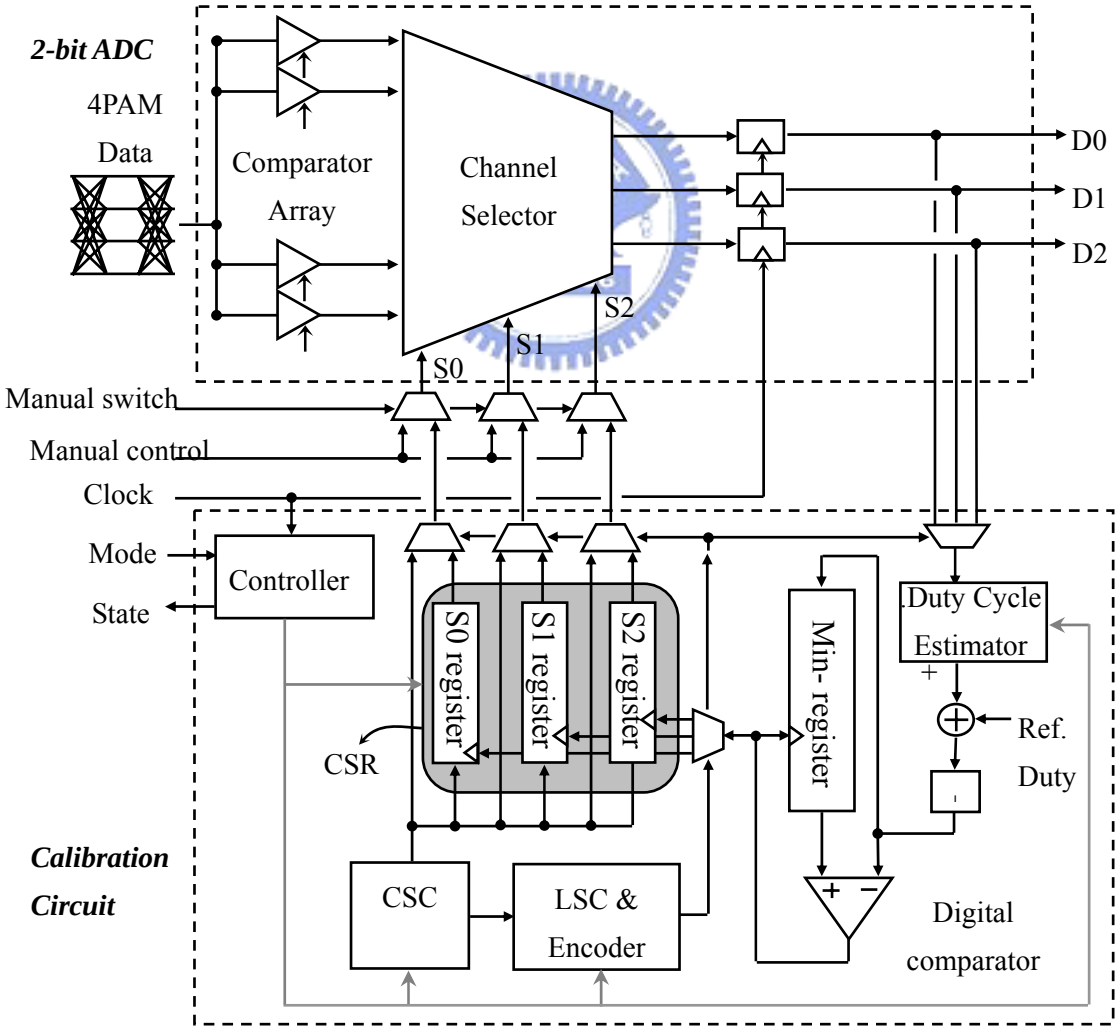


Figure 3.6 Architecture of Self-calibrating PAM Receiver

3.2 Flow Chart and State Diagram

The calibration flow as shown in Figure 3.7 can be viewed as three loops: small loop for stimulus timer, middle loop for channel select counter, and large loop for level select counter.

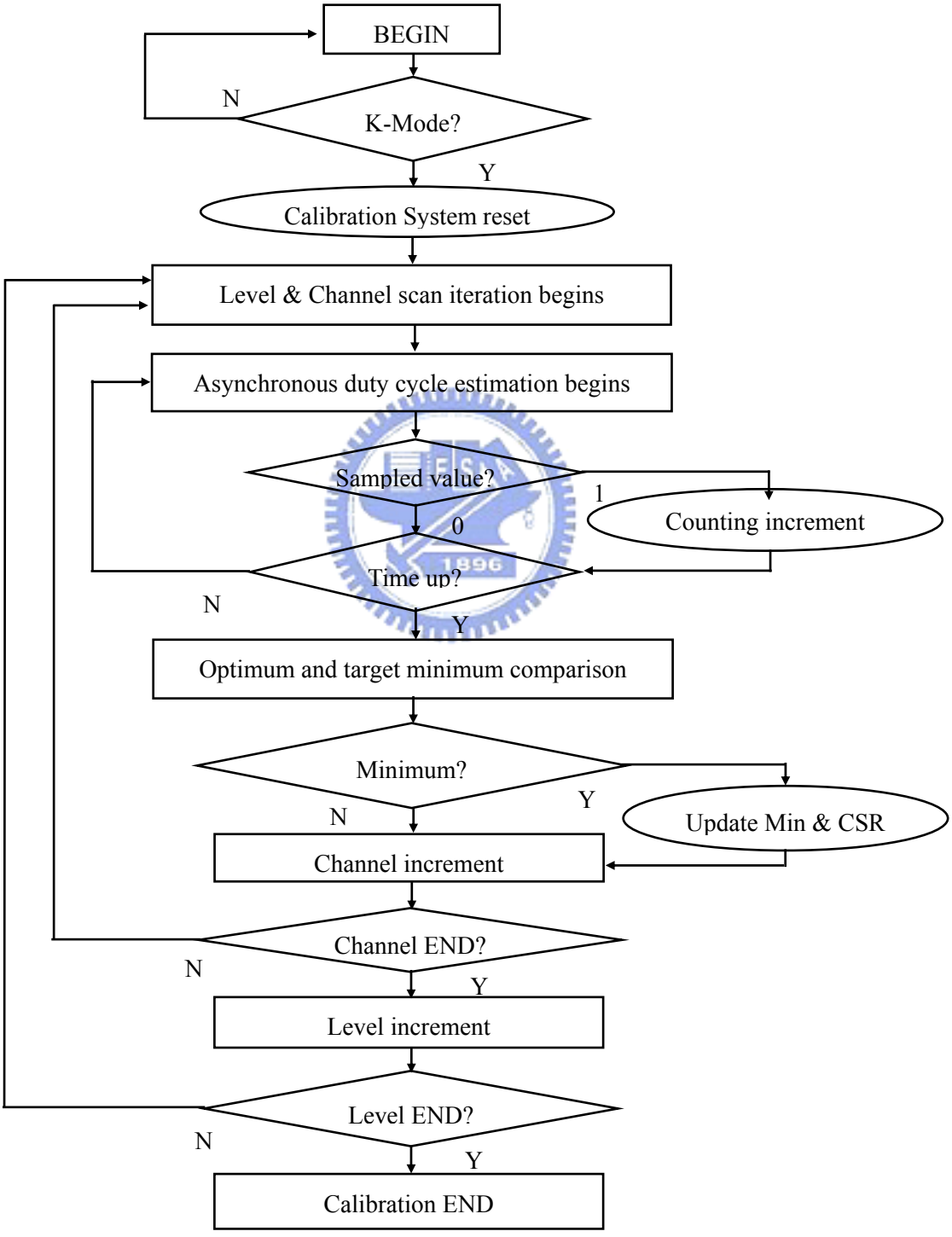
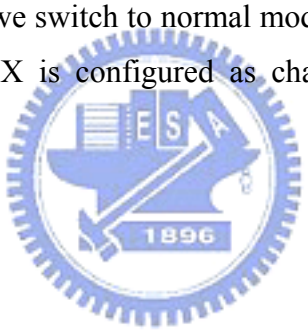


Figure 3.7 Flow chart of the calibration

3.2.1 Flow Chart

In Figure 3.7, calibration starts as long as it is switched to calibration mode, resetting counters and registers. Stimulus timer starts to count and one's counter samples from ADC output during this period. When time is up, the sampled value is processed through absolute offset comparator and compared with minimum. The minimum register and channel select register are updated when new value is less than previous one. The single channel evaluation route is shown in Figure 3.8. After comparison, channel select counter makes an increment and goes on to next channel counting if it is not the last channel of the MUX. If it is, the first channel select register stores the optimal channel number of the MUX for 75% duty cycle, and the system loops back for the next threshold level. The channel route is shown in Figure 3.9. Repeat the same procedure till three threshold levels are done. The system will return to normal operation, if we switch to normal mode in any cases. And the default channel number of each MUX is configured as channel number 3, center of the channel number.



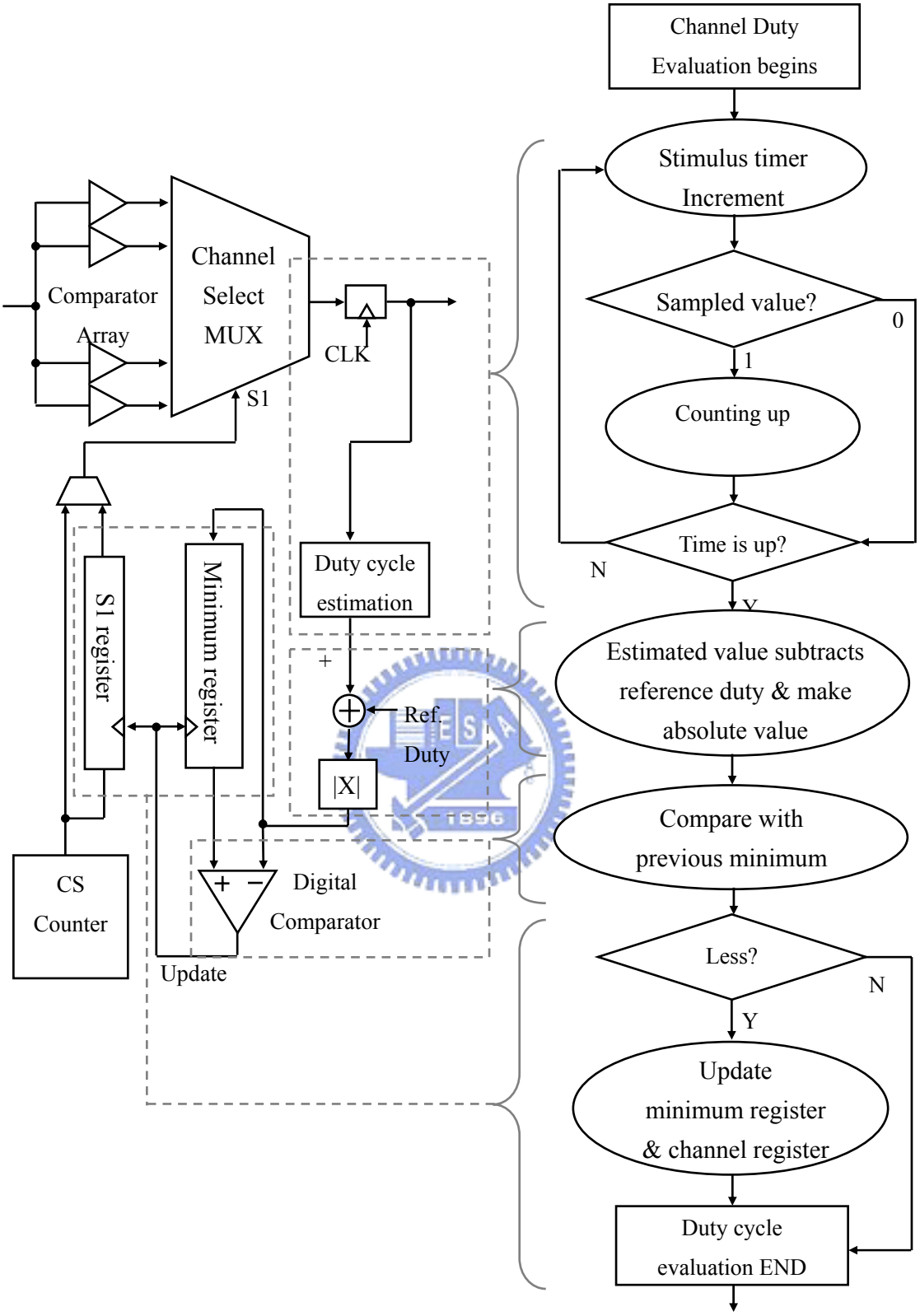


Figure 3.8 Single channel duty cycle evaluation route

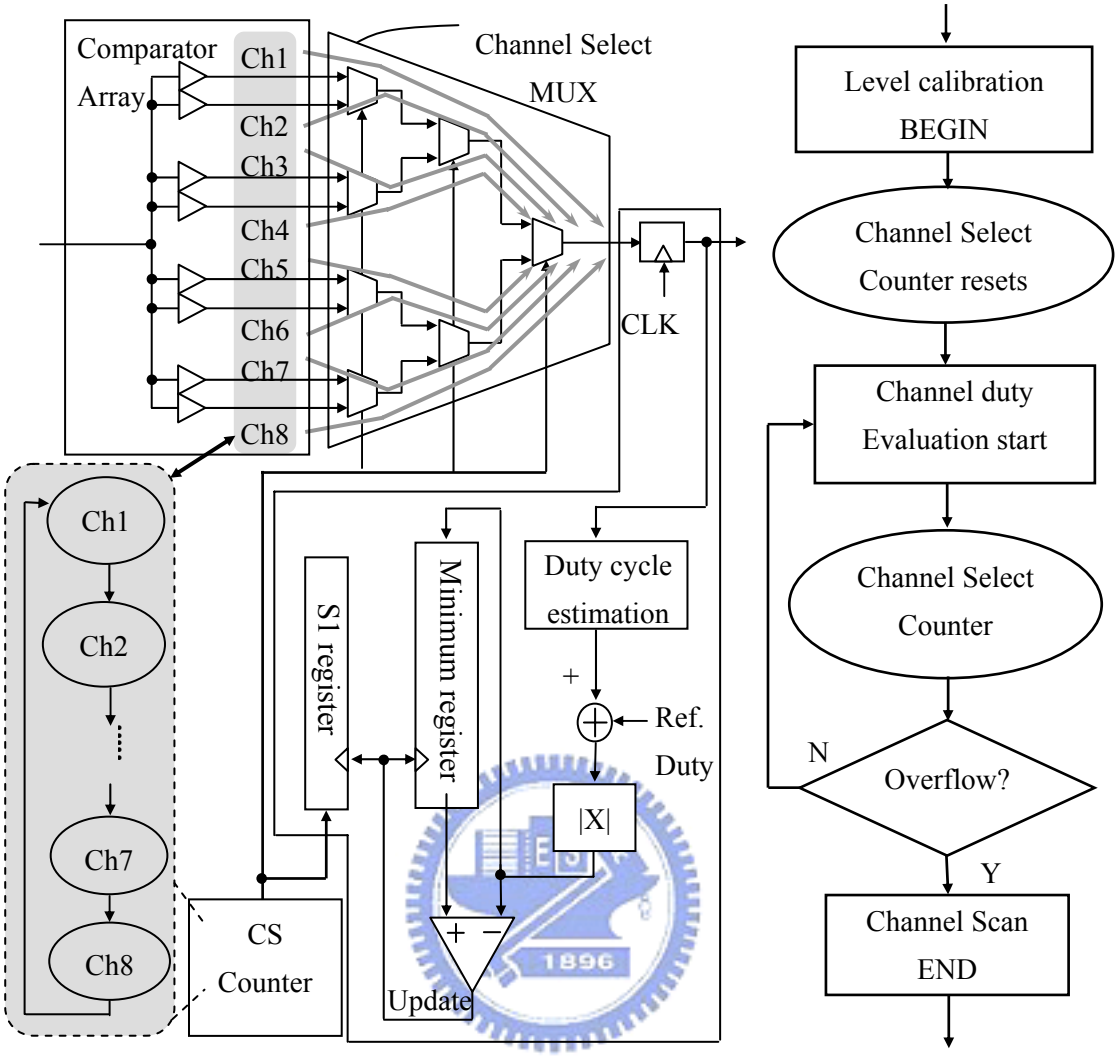


Figure 3.9 Channel scan route of a level

3.2.2 Truth Table and State Diagram

The calibration flow is controlled by the controller. We fill out the transition table as shown in Table 3.1, and get excitation equations. By these equations, we complete the control logics.

State	PS	S0	S0	S1	S2	S3	S3	S4	S5	S5	S6	S6	S7	S7
	NS	S0	S1	S2	S3	S3	S4	S5	S2	S6	S2	S7	S7	S0
	PS	000	000	001	010	011	011	100	101	101	110	110	111	111
	NS	000	001	010	011	011	100	101	010	110	010	111	111	000
Input	Mode	0	1	1	1	1	1	1	1	1	1	1	1	0
	T_up	X	X	X	X	0	1	1	X	X	X	X	X	X
	CH_END	X	X	X	X	X	X	X	0	1	X	X	X	X
	Lev_END	X	X	X	X	X	X	X	X	X	0	1	X	X
Output	Reset	0	0	1	0	0	0	0	0	0	0	0	0	0
	Reset_CH	0	0	1	0	0	0	0	0	0	1	1	0	0
	Reset_T	0	0	0	1	0	0	0	0	0	0	0	0	0
	CK_SW	0	0	0	1	1	1	0	0	0	0	0	0	0
	CMPR	0	0	0	0	0	0	1	0	0	0	0	0	0
	CH_in	0	0	0	0	0	0	0	1	1	0	0	0	0
	Lev_in	0	0	0	0	0	0	0	0	0	1	1	0	0

Table 3.1 Truth table of the calibration

The state diagram is shown in Figure 3.10 and the notations represent controller inputs and outputs. There are total eight states in the calibration, and the state machine needs three DFFs to show up.

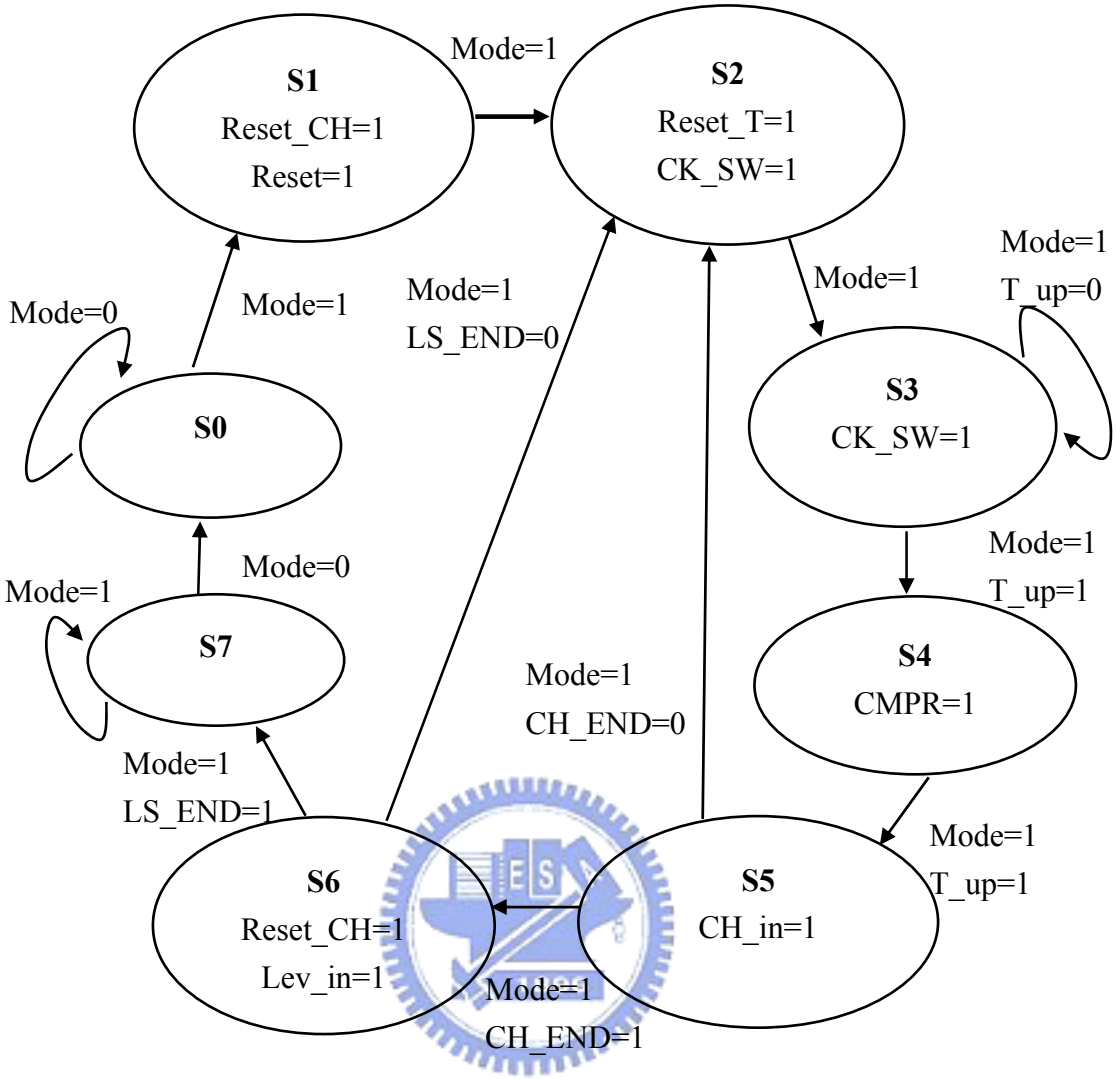


Figure 3.10 State diagram of the calibration

3.3 Statistical Analysis [17]-[19]

3.3.1 Random Variables

Bernoulli random variable can be modeled as a single coin toss. That is, $I_A(\xi)$ equals one if the event A occurs, and zero otherwise. I_A is called the Bernoulli random variable since it describes the outcome of a Bernoulli trial if we identify $I_A = 1$ with a "success", and $I_A = 0$ with a "failure". It is the value of the indicator function I_A for some event A; X=1 if A occurs, and X=0 otherwise. The Bernoulli random variable is shown in Equation 3.1.

$$S_x = \{0,1\}$$
$$P_0 = q = 1 - p \qquad P_1 = p \qquad 0 \le p \le 1$$
$$E[X] = p \qquad VAR[X] = p(1-p)$$

Equation3.1 Bernoulli random variable

Suppose that a random experiment is repeated *n* independent times. Let X be the number of times a certain event A occurs in these *n* trials. X is a random variable with range $S_X = \{0,1,\ldots,n\}$. For example, X could be the number of heads in *n* tosses of a coin and is called "binominal random variable". It can be the number of success in *n* Bernoulli trials. The binominal random variable is shown in Equation 3.2. Discrete random sampling can be modeled as binominal random variable as well, thus we can apply to duty cycle estimation.

$$S_x = \{0,1,\ldots,n\}$$
$$P_k = \binom{n}{k} p^k (1-p)^{n-k} \qquad k = 0,1,\ldots.n$$
$$E[X] = np \qquad VAR[X] = np(1-p)$$

Equation 3.2 Binominal random variable

3.3.2 Confidence Interval and Confidence Level

Based on central limit theorem, binominal distribution can be made for Gaussian approximation by normalizing with zero mean and unit variance. We estimate the required number of samples using the Gaussian approximation for the binominal distribution. Let $f_A(n)$ be the relative frequency of A in *n* Bernoulli trials. The probability of interest is

$$P[|f_A(n)-p|<\varepsilon] \cong P\left[|Z_n|<\frac{\varepsilon\sqrt{n}}{\sqrt{p(1-p)}}\right]=1-2Q\left(\frac{\varepsilon\sqrt{n}}{\sqrt{p(1-p)}}\right)$$

Equation 3.3 Confidence level of event A

The above probability cannot be calculated because *p* is unknown. However, it can be easily shown that $p(1-p)\le 1/4$ for *p* in the unit interval. For such *p*, it follows that $\sqrt{p(1-p)}\le 1/2$, and since tail function *Q*(*x*) decreases with increasing argument.

$$P[|f_A(n)-p|<\varepsilon]\ge 1-2Q\left(2\varepsilon\sqrt{n}\right)$$

$$Q(x)=\frac{1}{\sqrt{2\pi}}\int_x^\infty e^{\frac{-t^2}{2}}dt \cong \left[\frac{\frac{e^{-x^2/2}}{\sqrt{2\pi}}}{\left(1-\frac{1}{\pi}\right)x+\frac{1}{\pi}\sqrt{x^2+2\pi}}\right]$$

$$\begin{cases} P[A]: \text{probability of event A} \\ \varepsilon : \text{desired accuracy interval} \\ Q(x): \text{probability of the tail of the pdf} \end{cases}$$

Equation 3.4 Gaussian approximation for binominal probability and tail function

Analyzing from Equation 3.4, we know that tail function *Q*(*x*) is a decreasing function containing two parameters. Definitely, either loose desired accuracy or more samples, we are more confident with the result due to higher probability. In other

words, we get more occurrences if we claim for loose boundaries or tolerances. Or we can make more experiments to concrete our conclusion for the accuracy. Figure3.11 shows the probability of event A with a confidence interval ε in a normal distribution.

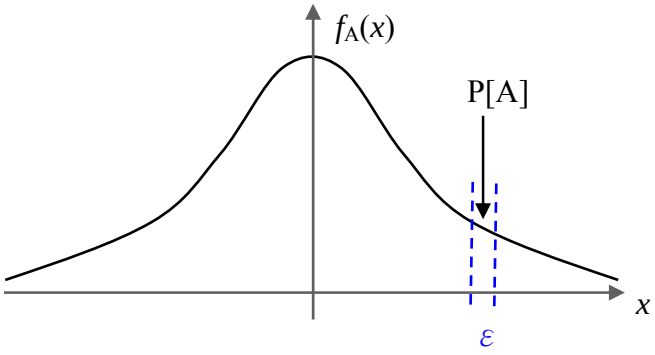


Figure 3.11 Confidence interval of probability

Instead of seeking a single value that we designate to be the "estimate" of the parameter of interest, we can attempt to specify an interval of values that is highly likely to contain the true value of the parameter. Find an interval [L(x), U(x)] such that

$$P\,[L\,(x) \le k \le U\,(x)] = 1 - \alpha$$

This is, the interval contains the true value of the parameter with probability $1 - \alpha$. Such an interval is a $(1 - \alpha)\times 100\%$ confidence interval, and $(1 - \alpha)$ is so called "confidence level" shown in Figure 3.11. The narrower confidence interval, the more accurately we can specify the estimation for parameter.

3.3.3 Samples and Accuracy

The number of samples and input signal amplitude are dependent with the accuracy of selecting comparators. For example, the larger the signal amplitude, the denser duty cycles at comparator outputs due to sharper waveform for a periodic frequency. As a consequence, we must have more samples to keep the same distinguishing ability. In accordance with statistics as we mentioned in previous sections, every sampling can be treated as Bernoulli trial, and successive Bernoulli trials are binominal random variables. Each comparator has its duty cycle as binominal variables in the estimation.

We are interested in how many samples and the confidence level we need for the conversion. More samples imply higher accuracy, but more hardware and

calibration time. Obviously they are trade-off. For a given signal, we evaluate the number of samples to maintain a certain confidence level so that we can select the optimal comparators. We configure the threshold gap of 40mV in the comparator array. It means that we have a resolution of 40mV. From table 3.2, for an input of 300mV swing, we can have over 99.35% confidence level in a 7-bit counter. Meanwhile, it equals that 95.45% confidence level for a 400mV swing. When the number of samples is larger, calibration time becomes longer and accuracy rises significantly.

Variance σ^2= 1/4					
accuracy ε	**x**	**Q(x)**	**N-bit timer**	**# of samples**	**confidence level**
40/100	4.53	1.181E-05	5	32	100.00%
	6.4	4.422E-10	6	64	100.00%
	9.05	**5.855E-19**	**7**	**128**	**100.00%**
	12.8	9.798E-37	8	256	100.00%
	18.1	2.648E-72	9	512	100.00%
	25.6	1.88E-143	10	1024	100.00%
	36.2	9.33E-286	11	2048	100.00%
40/200	2.26	0.0227664	5	32	95.45%
	3.2	0.0018694	6	64	99.63%
	4.53	**1.181E-05**	**7**	**128**	**100.00%**
	6.4	4.422E-10	8	256	100.00%
	9.05	5.855E-19	9	512	100.00%
	12.8	9.798E-37	10	1024	100.00%
	18.1	2.648E-72	11	2048	100.00%
40/300	1.51	0.0881241	5	32	82.38%
	2.13	0.0299467	6	64	94.01%
	3.02	**0.0032689**	**7**	**128**	**99.35%**
	4.27	3.652E-05	8	256	99.99%
	6.03	4.273E-09	9	512	100.00%
	8.53	5.515E-17	10	1024	100.00%
	12.1	8.756E-33	11	2048	100.00%
40/400	1.13	0.1388265	5	32	72.23%
	1.6	0.0771742	6	64	84.57%
	2.26	**0.0227664**	**7**	**128**	**95.45%**
	3.2	0.0018694	8	256	99.63%
	4.53	1.181E-05	9	512	100.00%
	6.4	4.422E-10	10	1024	100.00%
	9.05	5.855E-19	11	2048	100.00%
40/600	0.75	0.1884185	5	32	62.32%
	1.07	0.1478554	6	64	70.43%
	1.51	**0.0881241**	**7**	**128**	**82.38%**
	2.13	0.0299467	8	256	94.01%
	3.02	0.0032689	9	512	99.35%
	4.27	3.652E-05	10	1024	99.99%
	6.03	4.273E-09	11	2048	100.00%

(Accuracy ε here is the ratio of threshold gap over input signal amplitude)

Table 3.2 Estimation of samples and confidence level

Chapter 4

Simulation Results

We are going to discuss simulation results, specification comparison, and layout in this chapter. Simulation results include comparator corners, ADC output, and calibration results. We will check the ADC output before CDR processing and analyze the calibration result. Further more, we will make a specification comparison.

4.1 Threshold Comparator

4.1.1 Threshold Comparator Corners

Conversion range of comparator is set from 600mV to 1200mV. In Figure 4.1, FF case has the sharpest slope, and it means the dynamic range becomes wider for signal coverage. Because the number of comparators does not increase, obviously the threshold gap becomes wider and resolution deteriorates. In contrast, dynamic range of SS corner decreases, but resolution improves. That is to say, the accuracy is getting better in self-calibration. Another in SF case, the dynamic range shifts upward due to strong PMOS. FS case is on the opposite way, but both resolutions are the same as TT case. The calibration automatically selects the threshold comparators closet to center of the eye diagram, so we can avoid process variation impact to the accuracy through calibration.

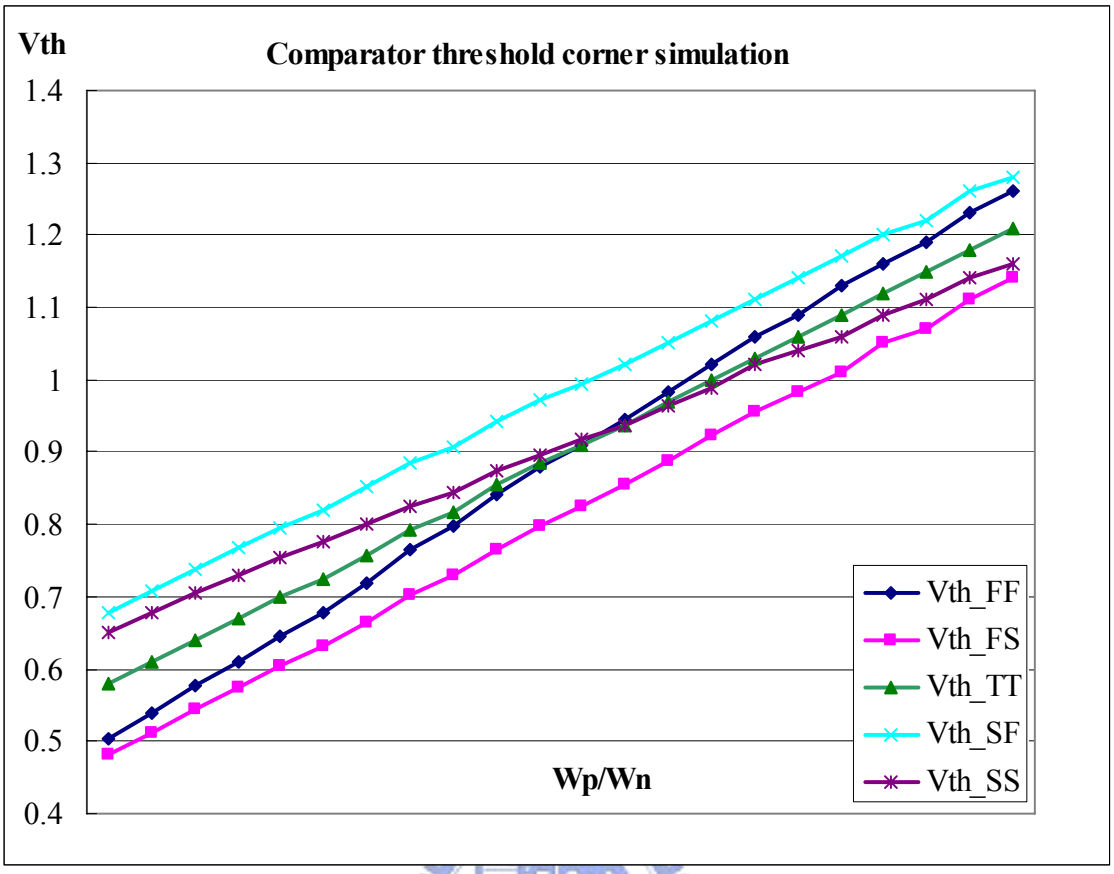


Figure 4.1 Comparator threshold corner

4.1.2 Gain Boosting

We mentioned that the inverter based MUX has gain boosting effects in previous chapter. In Figure 4.2, an initial input is amplified stage by stage from 100mV to 1300mV, and biased at DC level of 0.9V. Besides, we can see a light transition overshoot due to inductive peaking in the eye diagram.

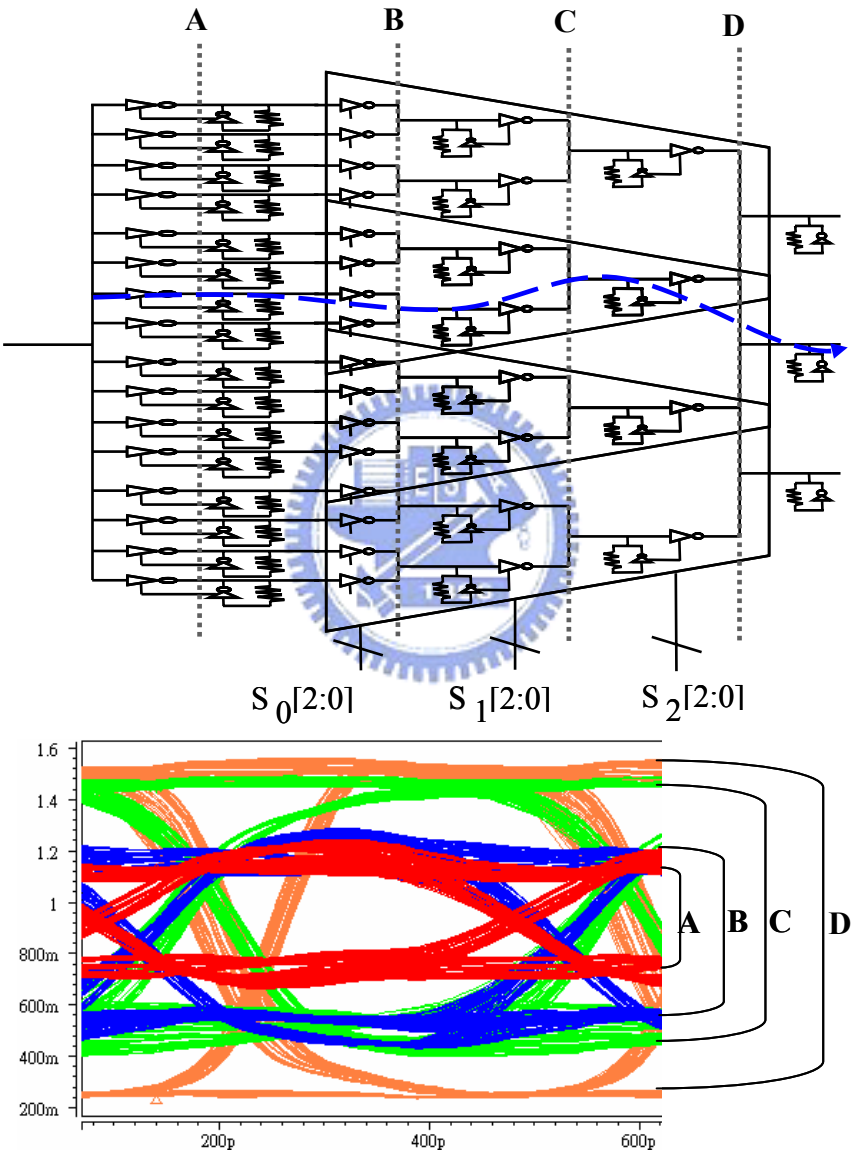


Figure 4.2 Gain boosting of TIQ ADC

4.2 ADC Simulation

4.2.1 2.5Gsps 4-PAM Input

We input a 2.5Gsps 4-PAM signal of 600mV swing to TIQ ADC through a fading channel by RC model. The ADC input waveform is simulated as shown in Figure 4.3. We extract three best channels out of three threshold levels from the simulations. The best channels have at least 0.5 *unit interval* (UI) eye-opening of 400ps period at the ends of outputs as shown in Figure 4.4.

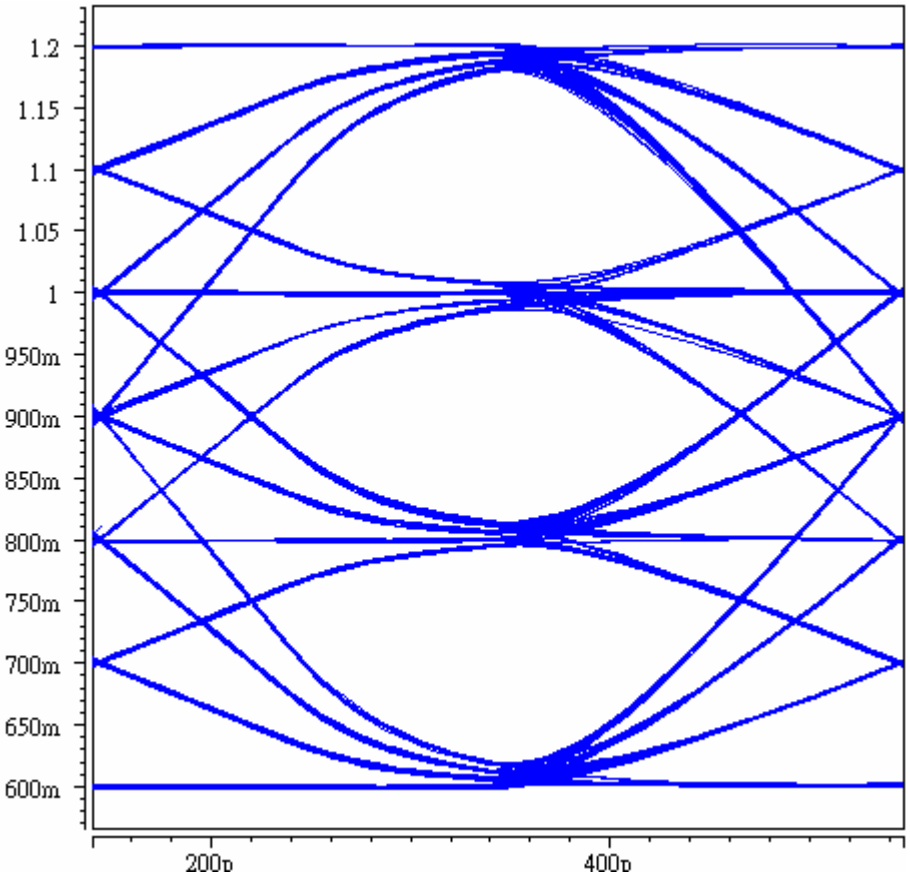


Figure 4.3 2.5Gsps 4-PAM signal

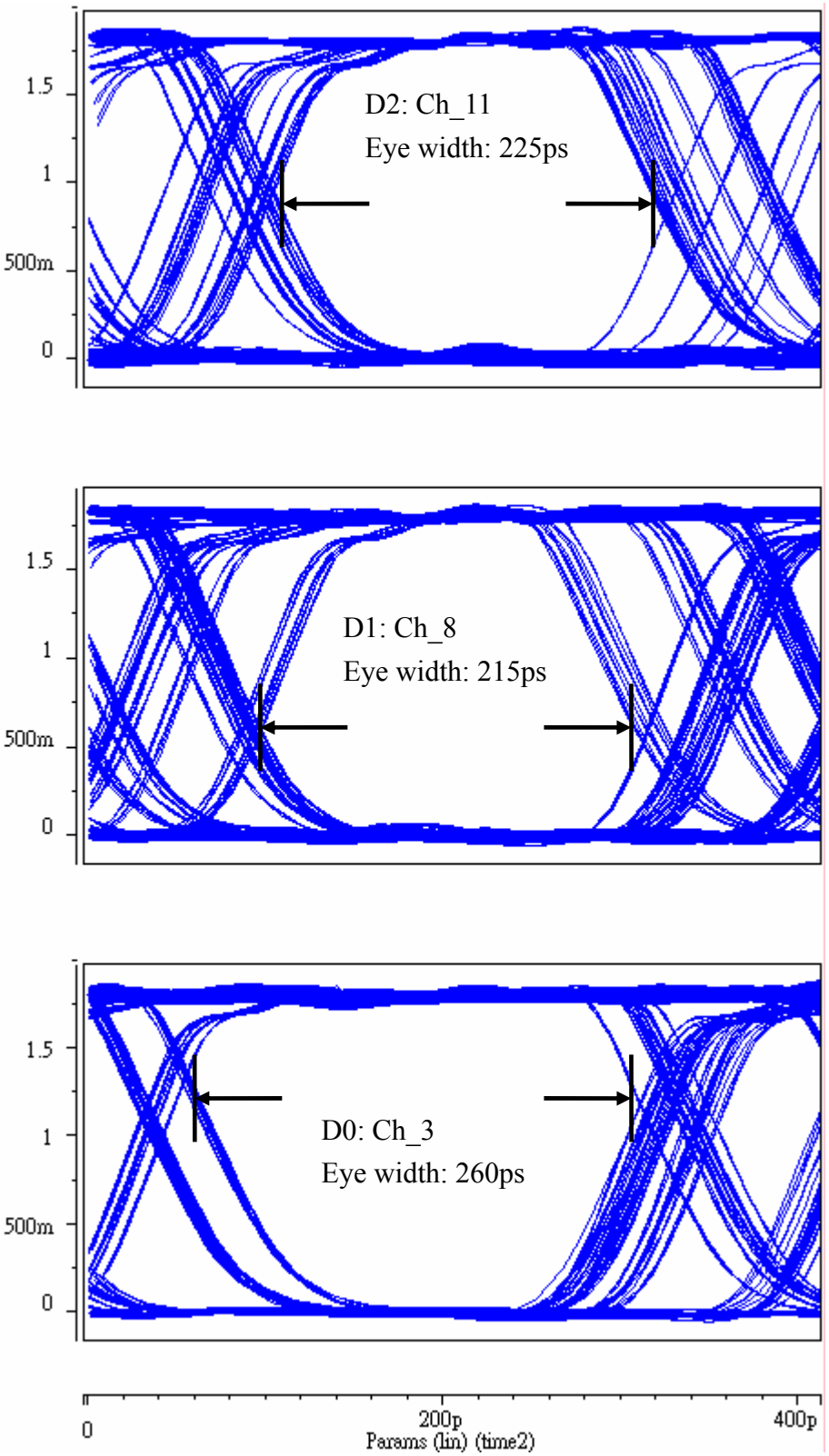


Figure 4.4 TIQ ADC output of 4-PAM input

4.2.2 2.5Gbps *Pseudo Random Binary Sequence* (PRBS) Input

We input PRBS of different level to replace 4-PAM, and get the three best eye-diagrams of ADC output as shown in Figure 4.5. The eye-openings are more than 330ps in the post simulation.

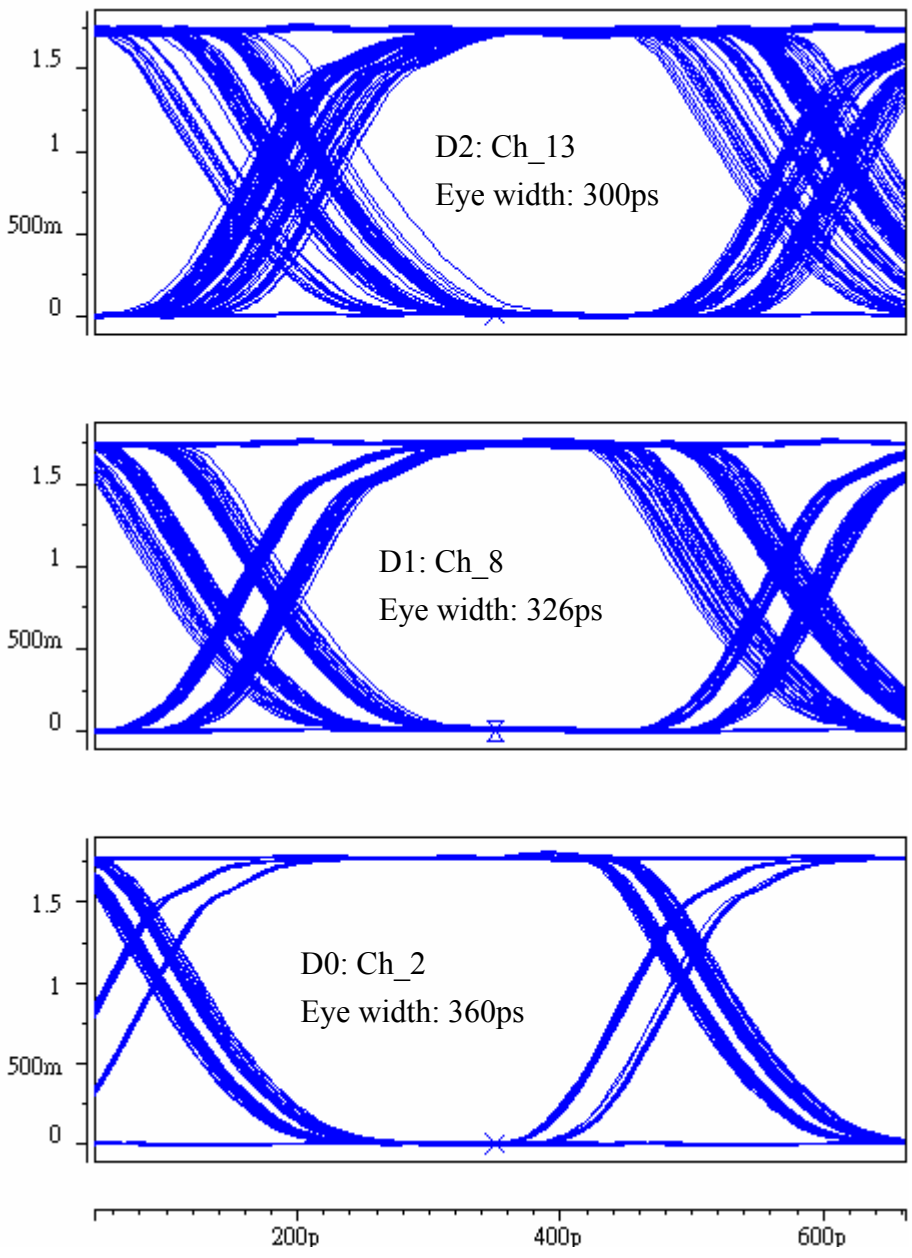


Figure 4.5 TT case of TIQ ADC output of PRBS input

Figure 4.6 shows the FF case of PRBS input, and it has wider eyes than those of TT case. Threshold gap becomes wider in FF case, so the channels of best eyes are getting closer.

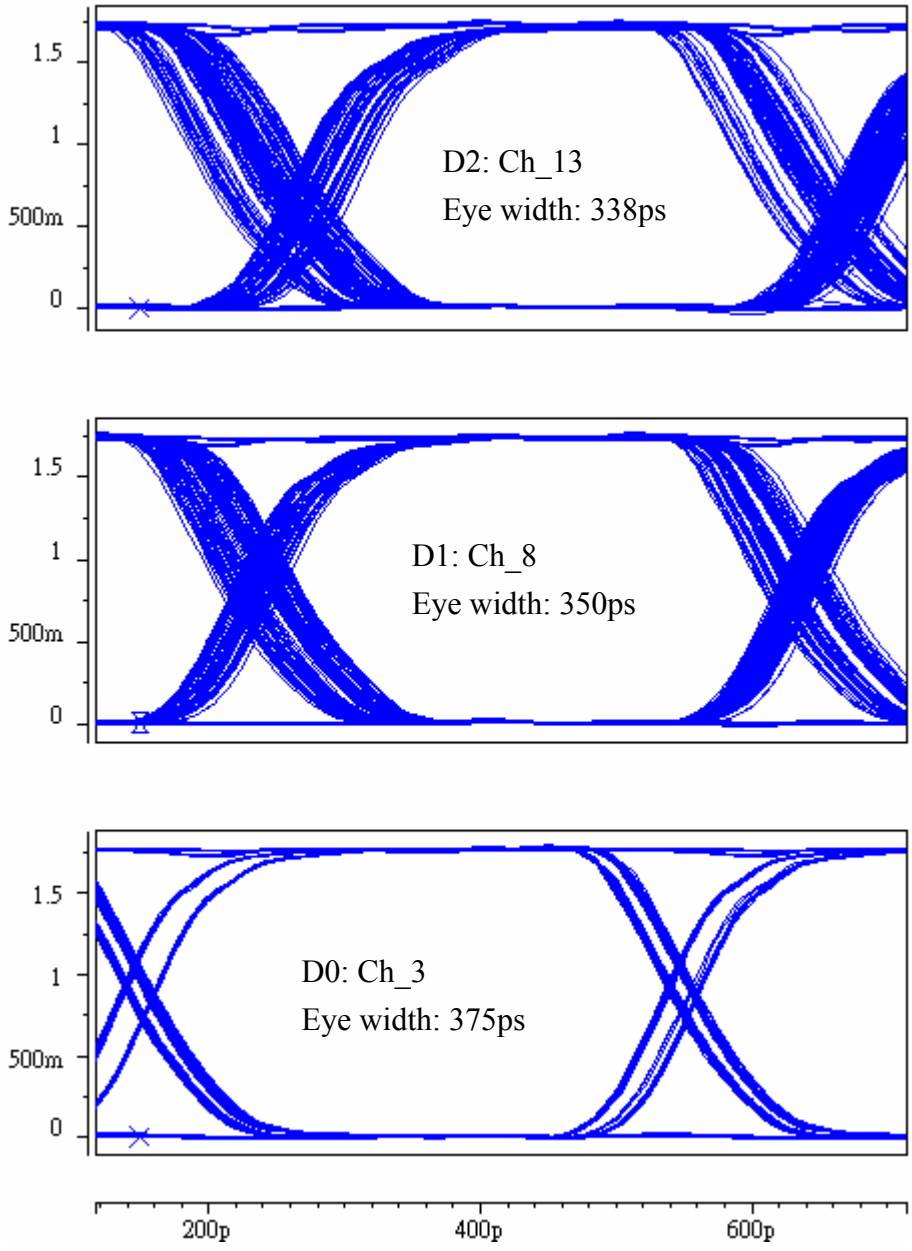


Figure 4.6 FF corner of TIQ ADC output of PRBS input

SS case as shown in Figure 4.7 stands opposite to FF case. The jitter grows due to slow transition, and outer channels for better eye-diagrams. Even though, the eye-opening is still enough for a CDR system.

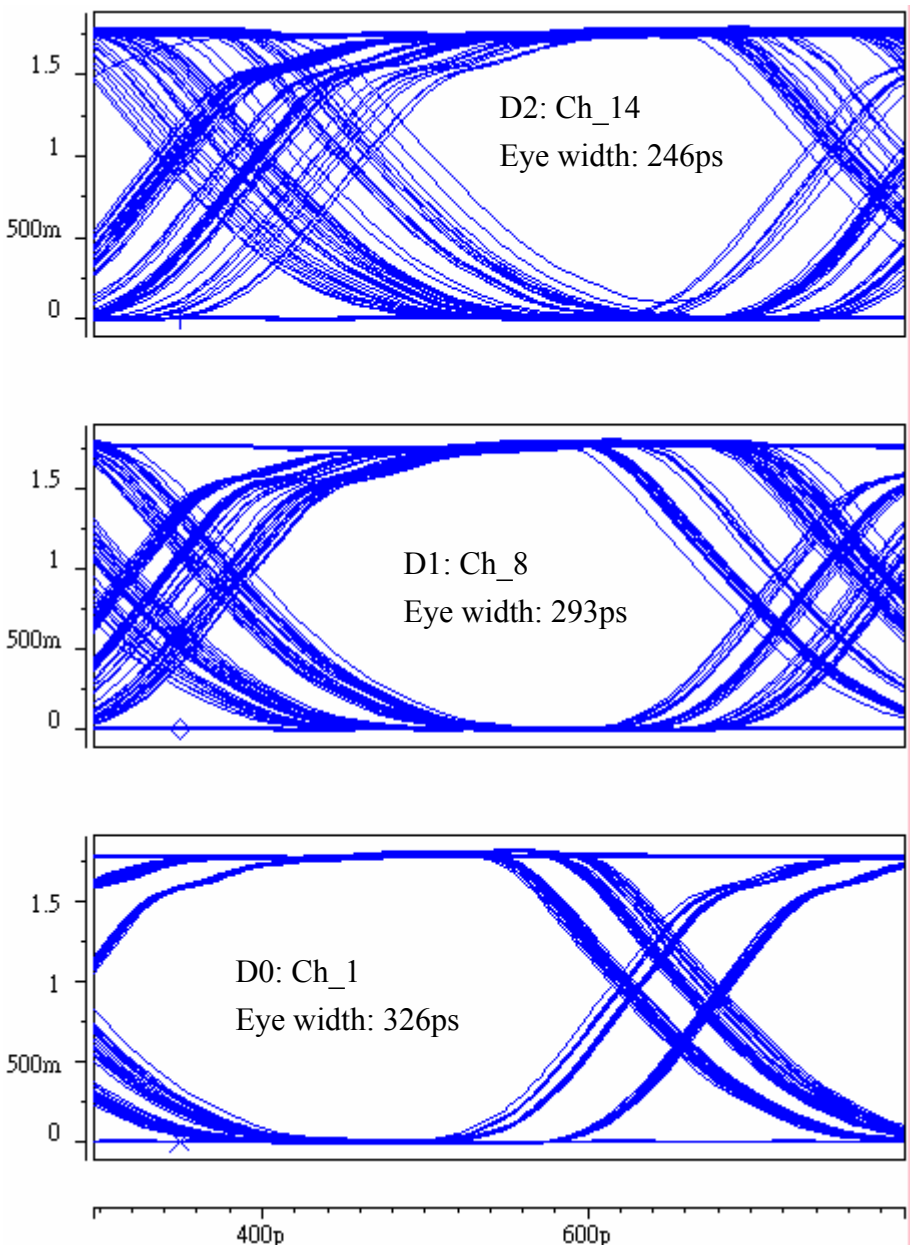


Figure 4.7 SS corner of TIQ ADC output of PRBS input

4.3 Calibration Simulation

For the sake of calibration verification, we simulate an 80MHz triangular input as fast as our available function generator. In Figure 4.8, we can see the calibrated channels of threshold levels and data outputs accordingly. With respect to Table 4.1, the selected threshold comparators are very close to ideal threshold voltages of eye center, and so do the duty cycles.

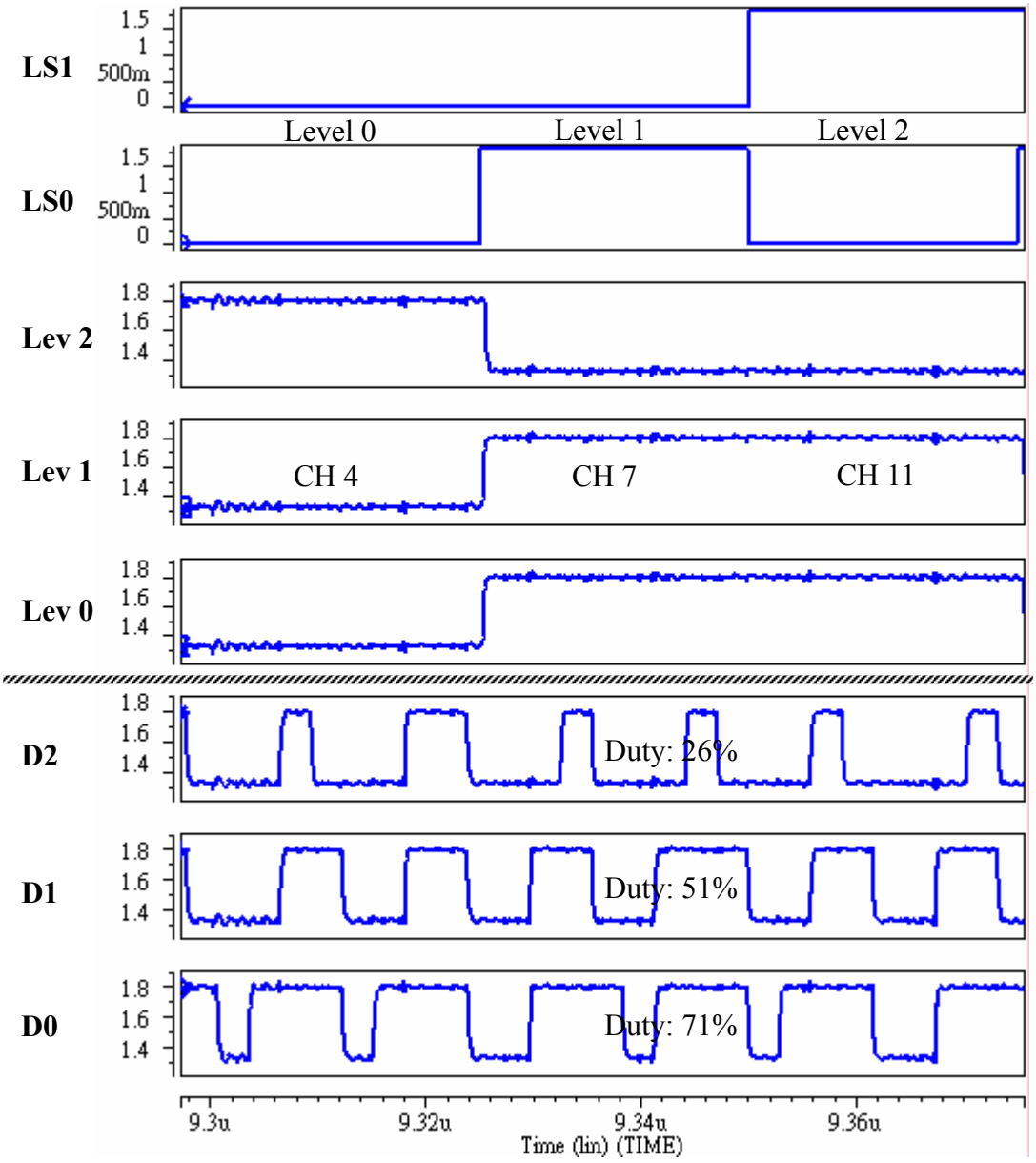


Figure 4.8 Calibration simulation of triangular input

345Msps	0.6~1.2V	Ideal Vth	Channel	Vth	duty%
80MHz triangular	**Level 2**	1.05	11	1.04	26%
	Level 1	0.9	7	0.88	51%
	Level 0	0.75	4	0.76	71%

Table 4.1 Calibration summary

Corner	Level 0	Level 1	Level 2
FF	CH4	CH7	CH8
TT	CH4	CH7	CH11
SS	CH3	CH7	CH12

Table 4.2 Corner cases calibration result

Further more, we compare the calibration resulting different corners as shown in Table 4.2. As we expect, FF case has wider conversion range, so it selects the closer channels as compare with other corners. In contrast, SS case selects the outer comparators.

4.4 Layout

The PAM receiver was fabricated in a six-level metal single poly 0.18um CMOS process. The layout of this chip is shown in Figure 4.9. The core area is $0.111mm^2$ ($370um \times 300um$), while the total area is $1.25mm^2$ ($1120um \times 1120um$). The pads close to the circuit layout are configured for high-speed I/Os, however, the pads far away are designated for control pins. The rest area is filled up with decouple capacitance in order to bypass power noise.

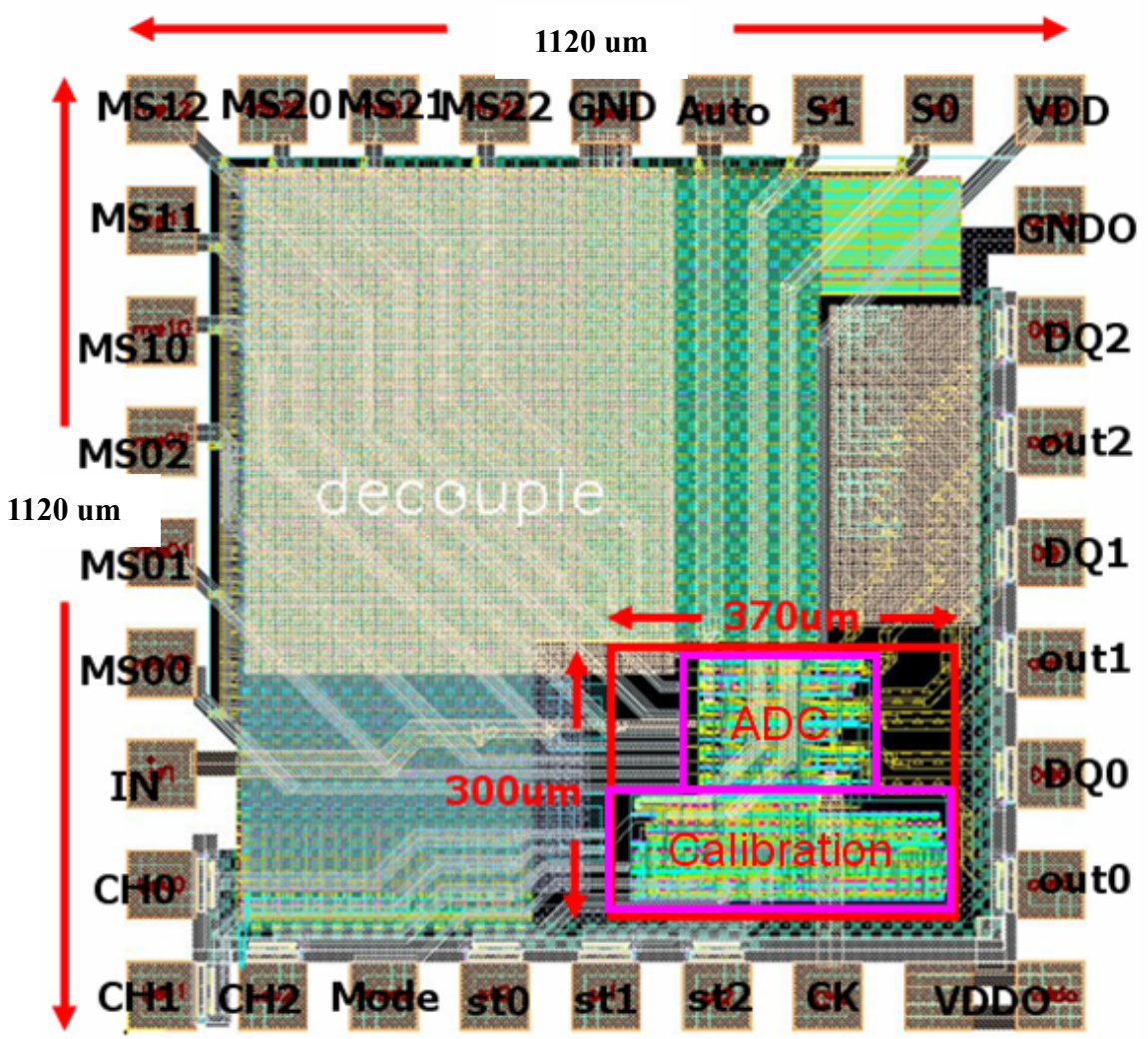


Figure 4.9 Layout of self-calibrating 4-PAM receiver

4.5 Specification Comparison

As shown in Table 4.5, this specification falls into two categories: normal mode and calibration mode. In normal operation, we get eye-openings over 0.75UI for PRBS source and 0.5UI for 4-PAM source. The power dissipation is only 3.2mW and 4.2mW for 2.5Gbps PRBS and 2.5Gsps 4-PAM input respectively. While operating in calibration mode, it consumes 3.9mW at 345MHz sampling rate, and 5.16mW in the worst case. Notice that the power consumption of calibration can be reduced by decreasing sampling rate.

Item	Spec (Normal)	Spec (Calibration)
Supply Voltage	1.8V	
Input	2.5Gbps PRBS 2.5Gsps 4PAM	80 MHz Triangular
PRBS jitter	100ps@ 2.5Gbps	N/A
4-PAM jitter	190ps@ 2.5Gsps	N/A
Power consumption	3.2mW @ 2.5Gbps PRBS 4.2mW @ 2.5Gsps 4PAM	3.9mW @ 345MHz CLK 5.16mW @ FF
Core area	$0.111mm^2$	

Table 4.3 Performance summary

In Table 4.4, *figure of merit* (FOM) shows the comparison with the other high-speed ADCs. For the convenience of comparison at the same level, we scale up to 6bit and 8bit to obtain estimated 67mW and 268mW power respectively at 2.5Gsps. Obviously, this work has least power consumption based on the same resolution, and the second minimum area.

ADC	Process	Resolution	Speed	Power	Area	Year
TIQ [4]	0.25um	6bit	1Gsps	44mW	$0.013mm^2$	2001
PRA-TIQ [20]	0.18um	6bit	2.66Gsps	97mW	$0.218mm^2$	2004
Flash [21]	0.25um	6bit	1.3Gsps	600mW	$0.12mm^2$	2003
Folding [22]	0.18um	8bit	1.6Gsps	774mW	$3.6mm^2$	2004
Proposed	0.18um	2bit	2.5Gsps	4.2mW	$0.11mm^2$	2006

Table 4.4 FOM comparison

Chapter 5

Measurement Considerations

In this chapter, we divide testing method into two parts: one is 4-PAM test, and the other is binary test. First, we introduce measurement considerations, inclusive of chip function implementation, and test configuration. Second, we illustrate how to generate signal sources in two ways: on-chip and off-chip test. Last, we describe both test flows.

5.1 Test Setup

5.1.1 Measurement Configurations

The test configuration is shown in Figure5.1 and we illustrate the purpose of each instrument. Power supply enables this chip, and pulse data generator provides stimulus input up to 5Gbps data rate. *Dual-in-line* (DIP) switches are used for channel selection, and switching mode. By a wide-band oscilloscope, we can observe the high-speed performance of ADC. Meanwhile, logic analyzer helps to check the calibrated channels and state. There is still an alternative way to measure channel characteristics by serial BERT. It stimulates the ADC and measures *bit error rate* (BER) with a feedback. [23]

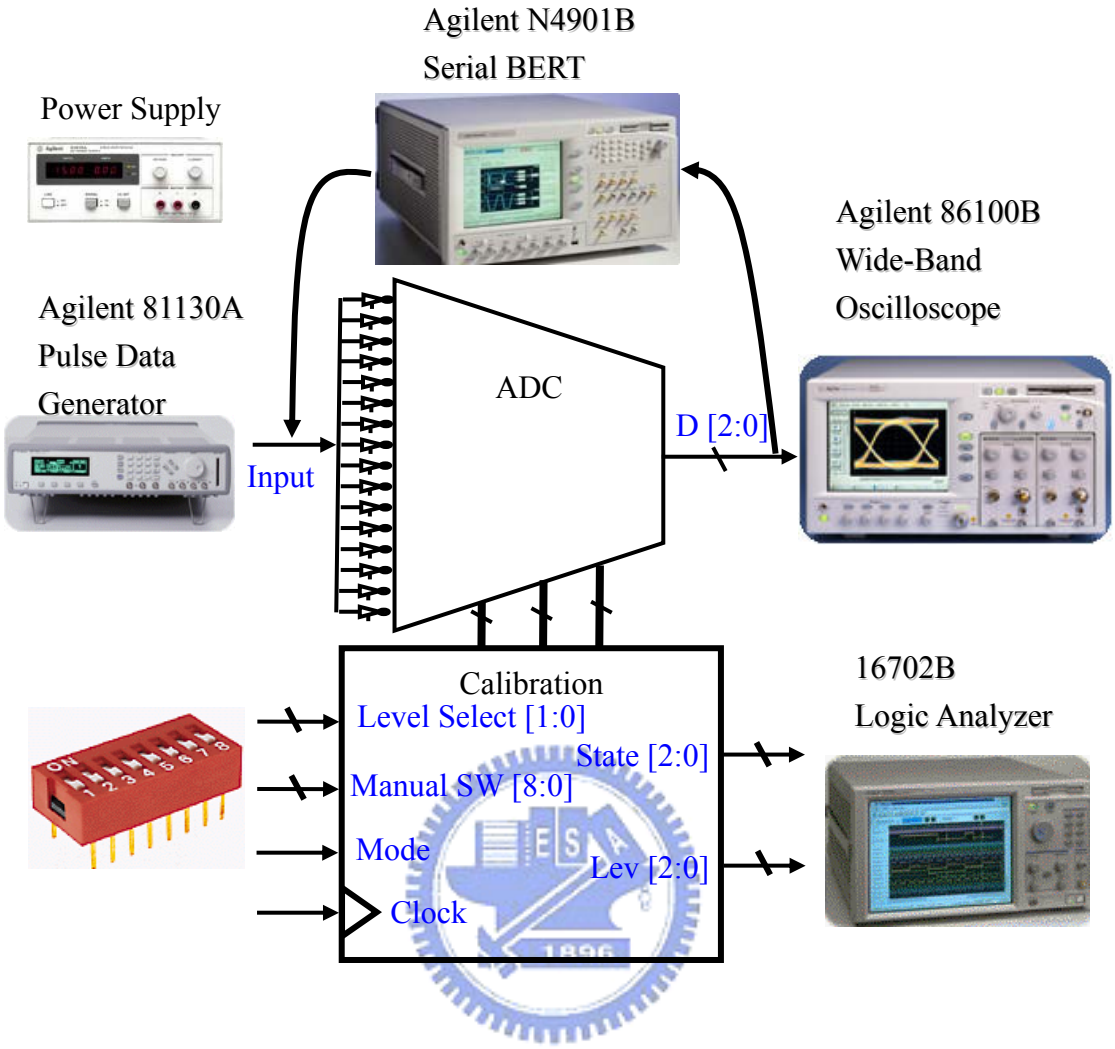


Figure 5.1 Measurement setup

5.1.2 Test Considerations

We illustrate the measure purpose of each pin, and explain what we want to observe as below:

1. MUX output: D [2:0]

   These are the output signals of some channels of some channels after a series of gain boosting. We judge if it is clear enough to operate in 2.5GHz or even higher after *clocked data recovery* (CDR), and observe ISI jitter.

2. DFF output: Q [2:0]

   These points are designated to observe the duty cycle after asynchronously random sampling. The sampled signal has only clock jitter, but no ISI jitter.

3. Level output: Lev [2:0]

   These pins tell us which channel of each level we select by switching level select signal LS [1:0].

4. State machine: State [2:0]

   By probing these pins, we realize current state of the system, and debug easier.

5. Manual channel select: MS [8:0]

   In the system measurement, we can manually control the channel for calibration verification. We measure not only BER, but also eye-diagram.

6. Level select: LS [1:0]

   To observe the selected channels, we switch it for three levels.

7. Auto:

   It is a control pin for MUX switch interface. It enables for self-calibration, or disables for manual control otherwise.

5.2 Signal Sources

In this section, we introduce two methods to generate signal for test. One is a built-in circuit for both 4-PAM and binary signal sources, and the other is an off-chip solution.

5.2.1 On-chip Solution

This self-generating signal source consists of *linear feedback shift registers* (LFSR), multiplexers, logic gates, and a 2-bit current mode *digital-to-analog converter* (DAC) in the circuitry which is shown in Figure 5.2. It generates not only 4-PAM signal, but also PRBS signal. The PRBS generated by LFSR is fed into binary-to-thermometer decoder via MUX to control the gates of current mode DAC for 4-PAM signal. We insert control logics between LFSR and MUX for different level binary signals.

The current mode DAC can generate high-speed signal, but drain a great deal of current. By switching on the gates, it sinks more current and lowers the output voltage. For our specification, its output swing ranges from 600mV to 1200mV and speed is up to 2.5Gsps. To consider the termination, the pull-up load is 50 ohm. The schematic of 2-bit current mode DAC is shown in Figure 5.3.

Table 5.1 is the code table of switching patterns. As shown in Figure 5.4, the eye of 2.5Gsps 4-PAM signal is wide-open. Figure 5.5 shows self-generating 2.5Gbps PRBS of various levels.

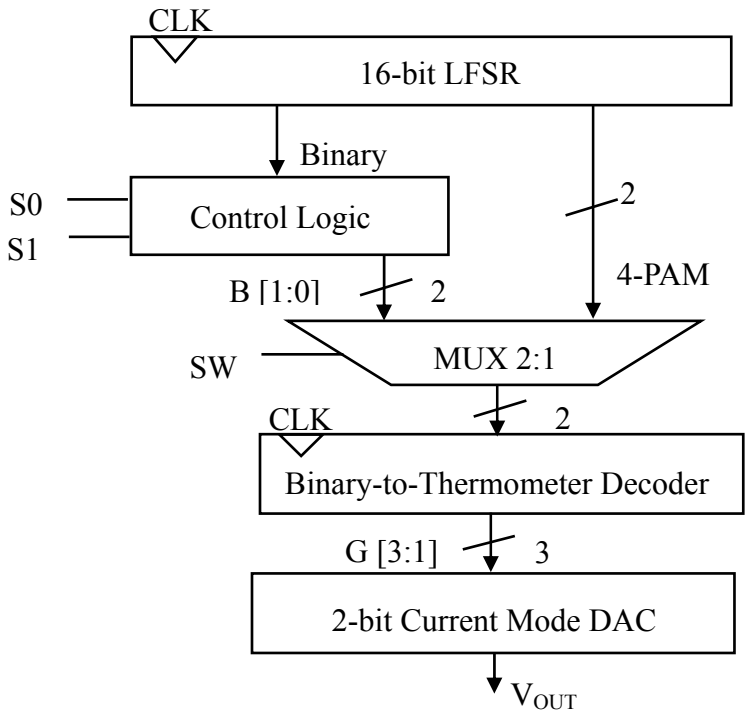


Figure 5.2 Block diagram of signal generator

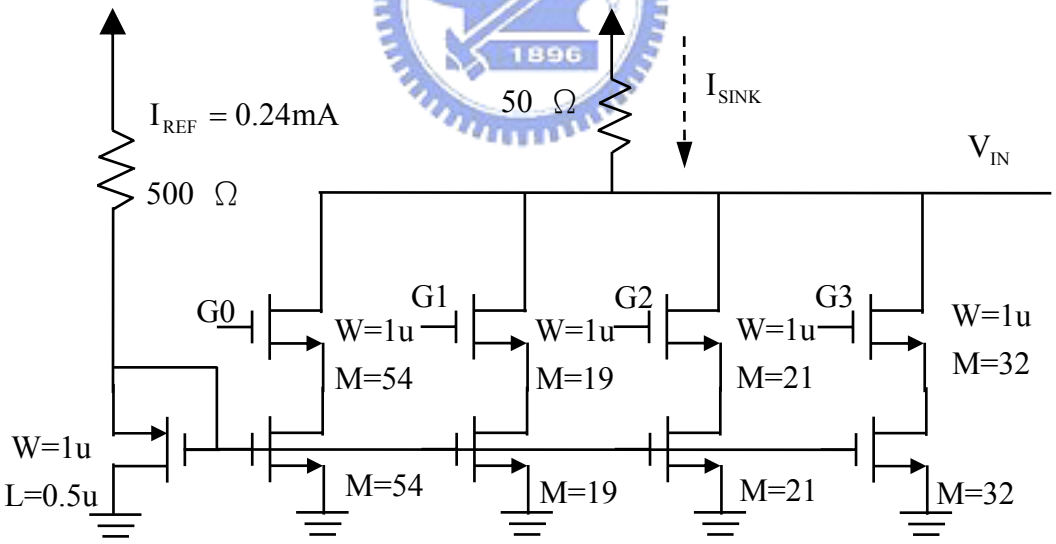


Figure 5.3 Schematic of 2-bit current mode DAC

Pattern	4-PAM	PRBS_0	PRBS_1	PRBS_2	PRBS_F
SW	0	1	1	1	1
S1	X	0	0	1	1
S0	X	0	1	0	1

Table 5.1 Signal generator switching code table

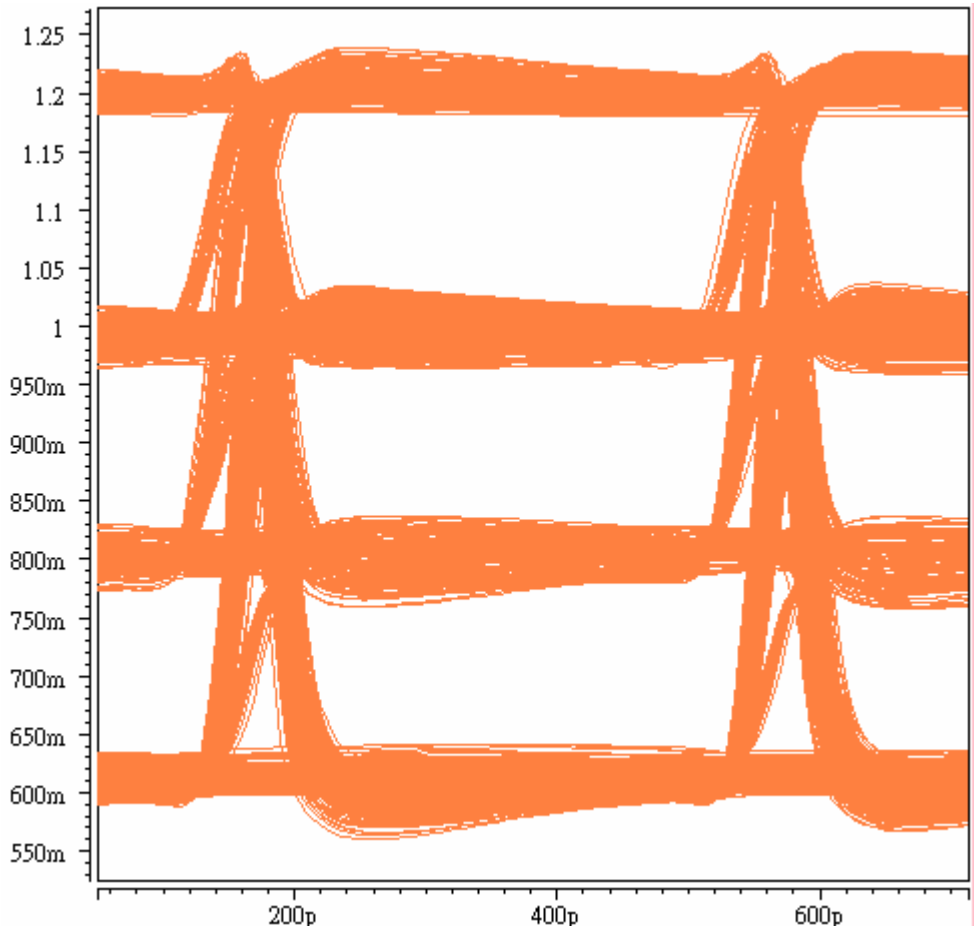


Figure 5.4 Self-generating 2.5Gsps 4-PAM signal

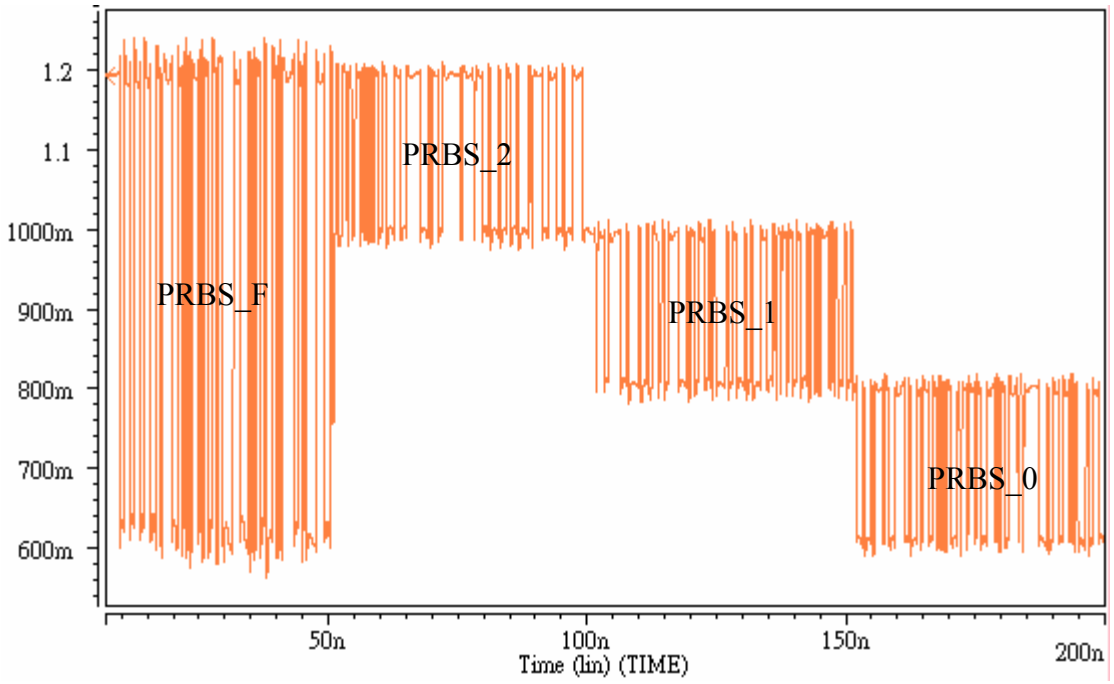


Figure 5.5 Self-generating 2.5Gbps PRBS signal

5.2.2 Off-chip Solution

There still an alternative way to generate 4-PAM signal by analog MUX inputs attached to resistor ladder. We can apply high-speed analog MUX and make random switches for random 4-PAM signal as shown in Figure 5.6. The key spec summary of analog MUX is shown in Table 5.2.

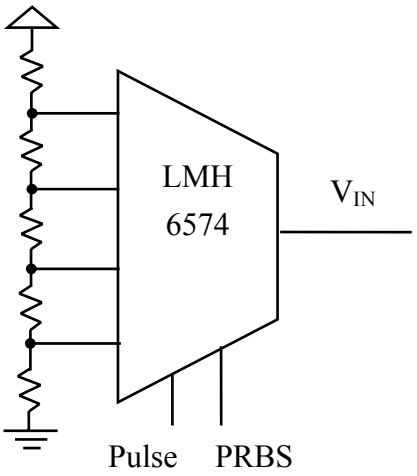


Figure 5.6 Off-chip 4-PAM generator

Parameter	Description	Condition	Typ. value	Unit
-3dB BW	-3dB BW	Vout =0.5Vpp	500	MHz
0.1dB BW	0.1 dB BW	Vout = 0.25Vpp	150	MHz
SR	Slew Rate	4V step	2200	V/us
T_{RS}	Channel switching time	Logic transition to 90% output	8	ns
OS	Overshoot	2V step	5	%

Table 5.2 NS LMH6574 spec summary

5.3 Test Flow

5.3.1 Test Flow of 4-PAM Input

Test flow of 4-PAM input is shown in Figure 5.7.

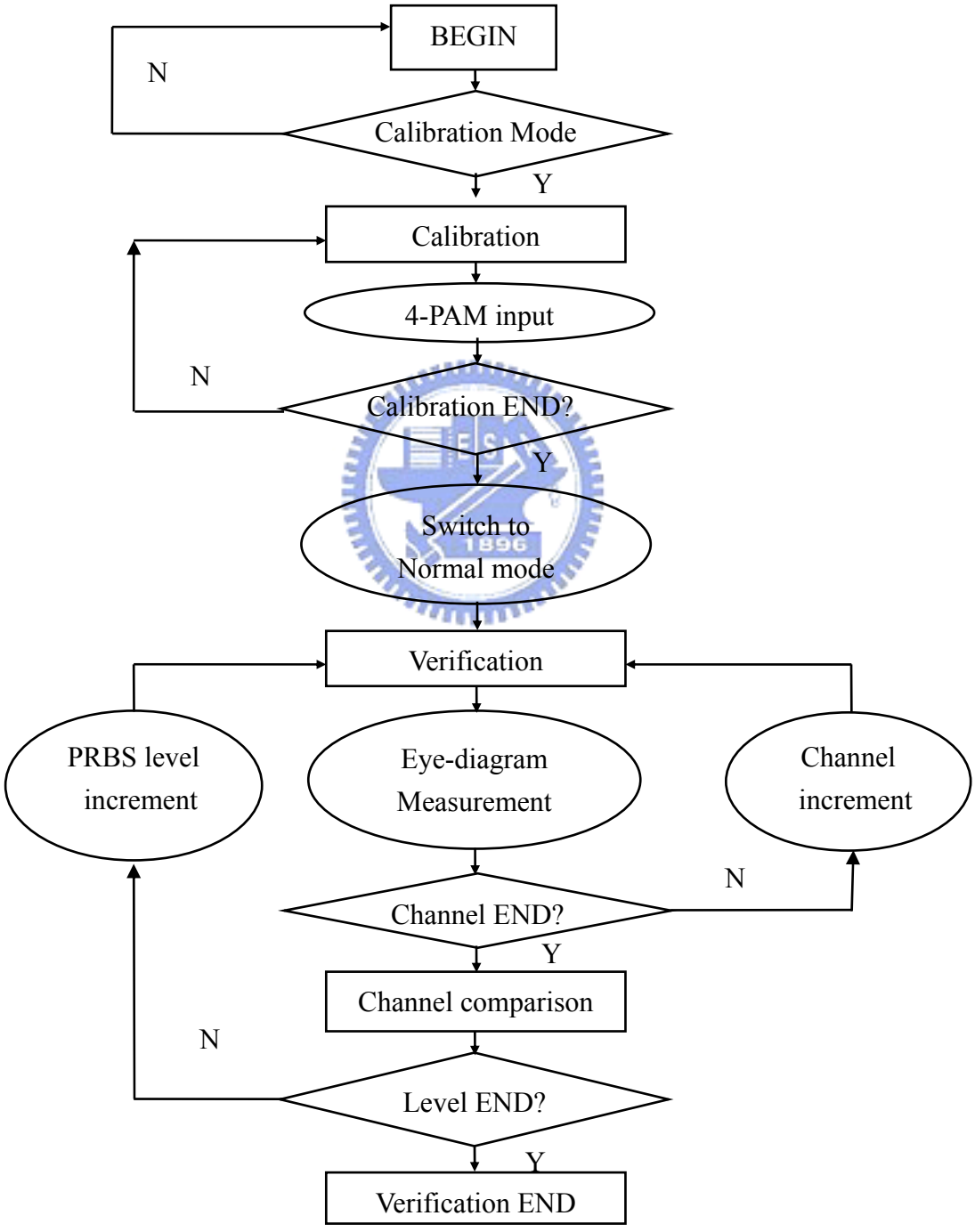


Figure 5.7 Test flow of 4-PAM Input

5.3.2 Test Flow of Binary Input

If we do not have 4-PAM source, there is an alternative way to replace 4-PAM with binary signal. First, it is fed with a PRBS which represents the lowest eye of 4-PAM signal while switching to calibration mode. After a period of calibration, we will get the selected channel number of the level. Record it and repeat the same procedure for the rest levels.

Second, we switch to normal mode when complete calibration is done, and feed the lowest binary sequence again and scan channels. It tells which channel is the best either by BER analysis or eye-diagram comparison. Last, we check the other two levels iteratively. The test flow is shown in Figure 5.8.

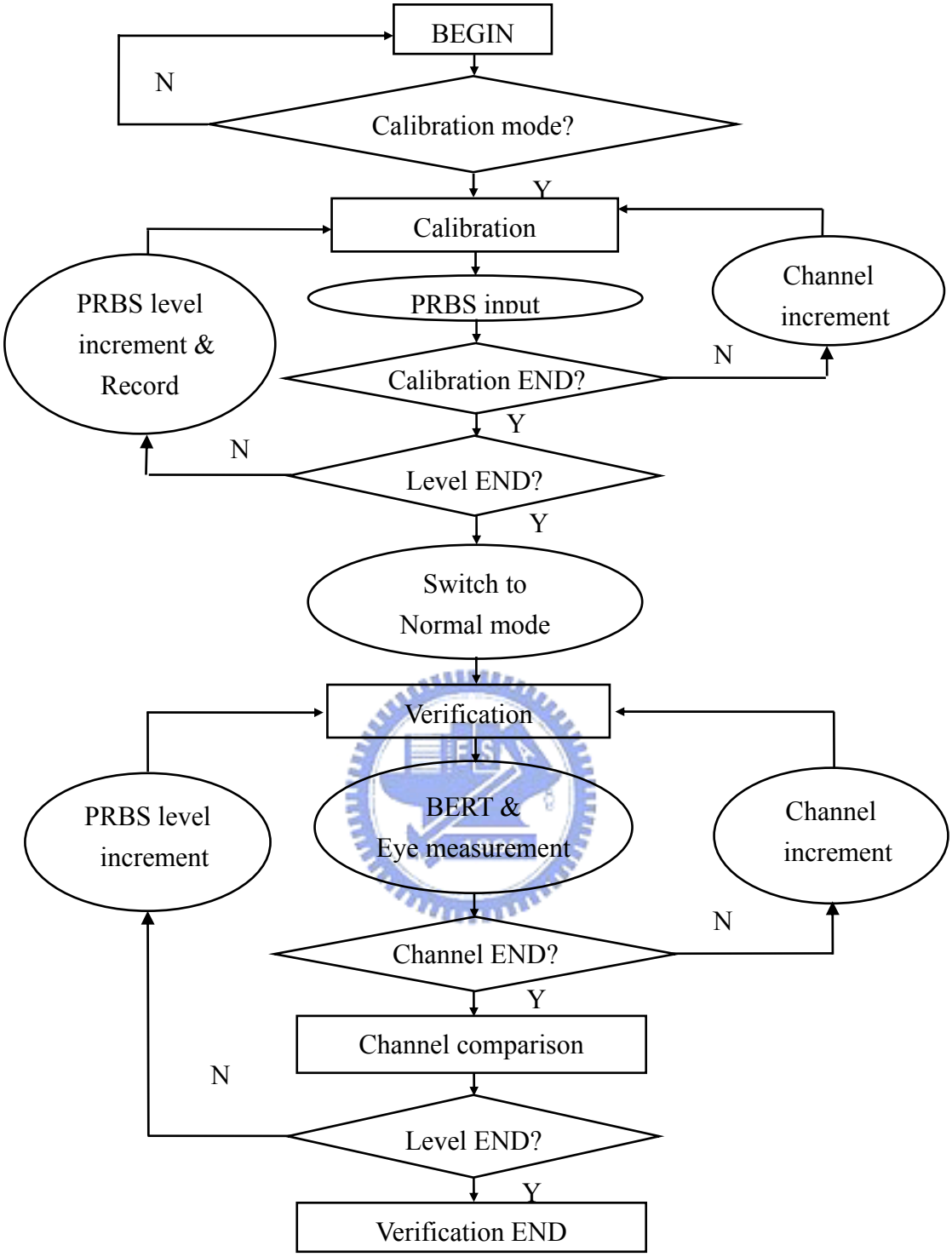


Figure 5.8 Test flow of binary input

Chapter 6

Conclusion

In this thesis, we have proposed an ADC with advantages of simple structure, high-speed, power-efficient, low hardware overhead, and immunity against process variation and temperature. We use tri-state inverters as comparator and building up multiplexers for the merit of power saving and gain and gain boosting. By proper overlap between comparators and multiplexers, we can enhance the accuracy of conversion. Because the threshold comparators are deeply impacted by process variation, we use an undersampling scheme for calibration. By means of duty cycle estimation, we can choose optimal comparators and channels for conversion. The numbers of sampling are evaluated by statistical analysis. For example, we can get 99.35% confidence level for a 300mV peak to peak input out of a 7-bit counter to acquire the best channels.

In verification, we propose PRBS and 4-PAM test. PRBS is a simpler way for data acquisition, but the test flow is more complicated for the three-eye iteration. As for 4-PAM source, we have on-chip and off-chip solutions. On-chip signal solution is a self-generating signal by LFSR and DAC. On the other hand, off-chip solution is configured as a resistor-ladder type DAC through a high slew rate analog MUX.

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Autobiography

I was born in Taichung and raised in a traditional family. After graduating from National Central University, I went to military service as a lieutenant officer. I had learned responsibility and led staffs to achieve missions.

My first job was a hardware engineer, developing switch hubs. Later I went on to devote myself to semiconductor field as a product engineer, dealing with yield improvement and new product verification. Being aggressive by nature, I had achieved some goals that other people could not. For instance, I was the youngest qualified statistical process control seed, and quality innovation team leader. Needless to say, team work spirit is important. I have cooperated with others to solve problems, such as shooting defective sources with integration staffs, and working out the returned parts with quality assurance staffs. I also applied Taguchi method and statistical analysis to improve product and testing quality.

Years later, I went back to campus for advance study, majoring in electric engineering and concentrating on integrated circuits design. My project is to make a 2.5Gsps self-calibrating 4-PAM receiver, and evaluate the accuracy by statistical method. During these years, I do appreciate my professor directs me both philosophy and profession. There goes an old saying: “No pain, no gain!” I will devote to work enthusiastically and extend my width and depth aggressively.