# Chapter 1

# Introduction

## 1.1 Background

Semiconductor device manufacturing or IC fabrication requires precisely controlled quantities of impurities to be introduced into tiny regions of the silicon substrate. Subsequently these regions must be interconnected to create components and electronic circuits. Lithographic processes create the patterns that define such regions. That is, a layer of photoresist materials is first spin-coated onto the wafer substrate. Next, this resist is selectively exposed to radiation such as ultraviolet light, electrons, or x-rays. An exposure machine, called stepper, and mask, called reticule, are used to effect the desired selective exposure. The patterns in the resist are formed when the wafer undergoes a subsequent development step. The areas of resist remaining after development protect the substrate regions, which they cover.

Locations from which resist has been removed can be subjected to a variety of subtractive (e.g. etching) or additive (e.g. ion implantation) processes that transfer the pattern onto the substrate surface. An advance integrated circuit can have up to 30 or more masking layers. Approximately one-third of the total cost of semiconductor manufacturing can be attributed to microlithographic processing; ref. Silicon Processing for the VLSI Era, S. Wolf and R. N. Tauber, Vol. 1, 2.sup.nd edition, Lattice Press, Sunset Beach, Calif., 2000, pp. 488, incorporated herein by reference. [ 5 ]

The photoresist has to be removed after etching or ion implantation process. There are different degrees of difficulty required to do this, depending on the prior process.

High-temperature hard bakes, plasma etch residues, sidewall polymers in contact holes and electrical interconnect trenches, ion implantation crusting, shrinking feature sizes, and new polymeric types of insulating material including low-k materials, all present challenges for the resist removal process. Both wet and dry stripping methods are being used. Plasma ashing as a dry method is currently the method of choice for the back-end of the fabrication process where the electrical interconnects are manufactured.

## 1.2 The issue of the existing process

During plasma ashing, photoresist is removed by oxygen energized in a plasma field, which oxidizes the resist components to gases that are removed from the process chamber by a vacuum pump. Microwave, RF and UV-ozone sources generate the plasma. The disadvantage of plasma resist stripping is its ineffectiveness in the removal of metal ions and residues after dry etching, or reactive ion etching (RIE), namely sidewall polymers in vias, contact holes and trenches; ref. Microchip Fabrication, P. van Zant, 3.sup.rd edition, McGraw Hill, New York, 1997, pp. 273, incorporated herein by reference. [ 6 ]

To complete the photoresist stripping process all residues have to be removed. This is typically done in wet chemical cleaning stations. After that the wafer has to be rinsed in deionized water and is finally dried. The process is called post-strip cleans.

The problems associated with the prior art methods of photoresist stripping by plasma ashing and residue removal can be summarized as follows:

（1） Plasma ashing is performed at high temperatures of 250℃ ~ 400℃, adding to the thermal budget of the wafer.

（2） After plasma ashing residues are left in vias and trenches that need additional

wet chemical treatment.

(3) Plasma ashing is not efficient for removing mobile metallic ion contamination;

(4) Plasma ashing can cause radiation damage of the electronic circuits;

(5) Plasma ashing of photoresist after ion implantation can lead to "resist popping" littering the wafer with particulate matter;

(6) With plasma ashing, selectivity between photoresist and low-k materials is bad and low-k material may be mechanically affected;

(7) Plasma ashing can modify the dielectric constant of low-k material due to charge damage;

(8) Post-strip wet chemical treatment may modify the low-k material in its electrical properties;

(9) Shrinking dimensions of features below 0.18 μm present a problem for wet chemistry as post-strip cleans method, because of surface tension issues. (Figure 1)

As semiconductor device dimensions approach the nanoscale, it will become increasingly difficult to use aqueous-based cleaning processes due to high surface tension and capillary forces. Effective penetration into the high aspect ratio trenches and via structures will be challenging. The rinsing and drying steps will also become more difficult. Cleaning of semiconductor wafers will require an innovative technology, significantly different from today's processes. A novel cleaning technology for removing photoresist and photoresist

residue from semiconductor wafers is introduced. This cleaning technology is a non-plasma, environmentally friendly technology using supercritical carbon dioxide (SCCO2) and co-solvents to clean the substrates.

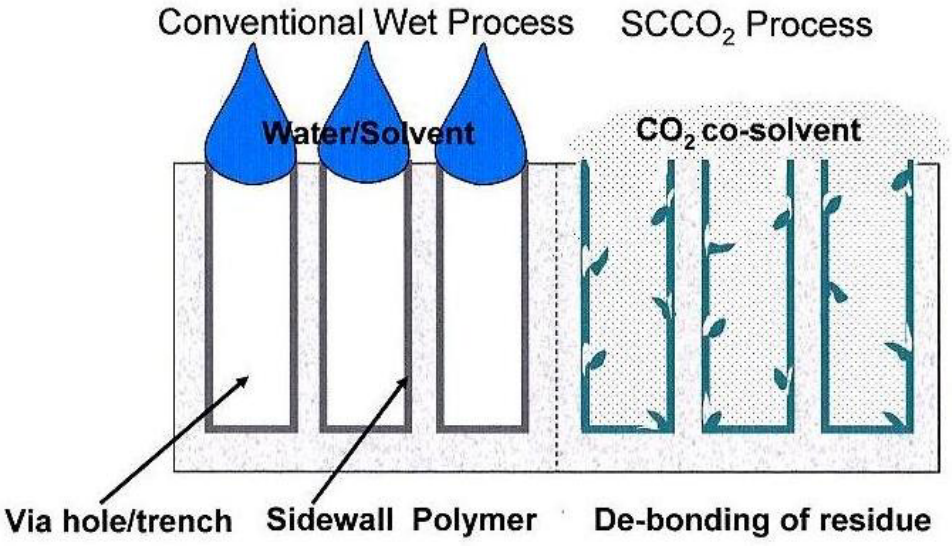


**Figure 1 Enable sub-130 nm residue removal [22]**

## 1.3 The advantage of the supercritical fluids process

Supercritical fluids provide the enabling capabilities for overcoming the process barriers encountered as we approach nanoscale dimensions. Supercritical state of a process chemical, which is another state of matter, also called phase, in addition to solid, liquid and gas. Sometimes the supercritical phase is referred to as “dense gas”, ”compressible liquid”, or ”supercritical fluid”. Supercritical fluids, compounds above their critical temperature and pressure, have transport properties similar to gases and solvating properties similar to liquids, as well as low surface tension (Table 1). Furthermore, they have been used in the food industry (decaffeinating coffee), pharmaceuticals (purification and extraction), waste treatment, textile and garment dry cleaning and precision cleaning of electronic components.

**Table 1 Comparsion of physical-chamical properties in vapor, liquid and supercritical fluid of typical organic fluid [ 1 ]**

| | Density ($g/cm^3$) | Viscosity (g/cm-s) | Diffusivity ($cm^2/s$) |
|---|---|---|---|
| Vapor | $(0.6\sim2)\times10^{-3}$ | $(1\sim3)\times10^{-4}$ | 0.1~0.4 |
| Liquid | 0.6~1.6 | $(0.2\sim3)\times10^{-2}$ | $(0.2\sim2)\times10^{-5}$ |
| Supercritical fliud | 0.2~0.9 | $(1\sim9)\times10^{-4}$ | $(2\sim7)\times10^{-4}$ |

Cleaning with supercritical carbon dioxide and co-solvents was successfully applied to a broad range of applications from front end applications (ion implant) to dual damascene Cu technology with standard oxides and low-k materials. Based on the results to date, cleaning with supercritical carbon dioxide and co-solvents has the potential to combine ashing, wet cleaning and rinsing/drying steps into one process step, is a " dry in – dry out " process technology. The potential shortcomings of ashing and wet cleaning with respect to high aspect ratio features, dual damascene and low-k technology, and reducing the amount of solvents and water dramatically, resulting in an enabling, very cost effective cleaning technology.

## 1.4 Thesis organization

The purpose in the study is removing photoresist and residue after RIE oxide etched with supercritical carbon dioxide in semiconductor manufacturing. In the chaper 2 will discuss the methode and apparatus of the experiment. In the chapter 3 will discuss the theory of supercritical fluid, and why we want to use carbon dioxide as the source of supercritical fluid. In chapter 4 will describe the preparation of samples, the steps of photoresist and residue removal, and the sample analysis after supercritical carbon dioxide treated (the

samples include after hard-baked, after ion implanted, RIE oxide etching). In chapter 5 will discuss the results of the experiment. In chapter 6 is the conclusion of the experiment.