國立交通大學

材料科學與工程研究所

博士論文

增強型

磷化銦鎵/砷化鋁鎵/砷化銦鎵

假晶高電子遷移率電晶體之研究

研 究 生：褚立新

指導教授：張　翼 博士

中華民國九十六年一月

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The study of Enhancement-mode InGaP/AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor

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指導教授：張　翼 博士　　Advisor: Dr. Edward Yi Chang

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摘要

近年來無線通訊(wireless communication)科技日新月異，已為世界科技產業重要之一環。無線通訊系統已由類比無線通訊進入數位無線通訊，同時數位無線通訊系統是世界公認的無線通訊系統發展主力。本論文即在研究應用於數位無線通訊系統之增強型砷化鎵高電子遷移率電晶體，以期提高其功能的相關元件及製程技術。

在此論文中，由磷化銦鎵/砷化鋁鎵/砷化銦鎵 所組成的結構首次應用於製造增強型的高電子遷移率元件。以磷化銦鎵/砷化鋁鎵/砷化銦鎵 所組成的結構取代傳統結構可進一步提升元件的特性。此磷化銦鎵/砷化鋁鎵/砷化銦鎵 結構優於傳統的磷化銦鎵/砷化銦鎵 有下列原因：第一， 砷化鋁鎵/砷化銦鎵 的導電帶的不連續性比磷化銦鎵/砷化銦鎵 來的高，對於電子的侷限性會較佳，此現象將可以增進元件的輸出功率。第二, 砷化鋁鎵/砷化銦鎵 的介面比磷化銦鎵/砷化銦鎵 更平滑，因為在磷化銦鎵/砷化銦鎵 的介面砷原子及磷原子會有交互擴散行為產生。此結果造成磷化銦鎵/砷化鋁鎵/砷化銦鎵 的高電子遷移率電晶體的電子遷移率比磷化銦鎵/砷化銦鎵 的高電子遷移率電晶體來的高。所製造出來的

0.5×160 μm^2 元件展現出很低的 0.3V knee voltage, 且當元件的偏壓在 V_{DS}＝2.5V 時，汲極電流為 375mA/mm（閘極電壓在 0.7V）和最大的轉導為 550mS/mm 。此元件亦展現及優之高頻特性;截止頻率為 60GHz 且 最大震盪頻率為 128GHz. 此增強型的磷化銦鎵/砷化鋁鎵/砷化銦鎵元件，在 2.4GHz 的頻率下亦展現很高的輸出功率密度 453mW/mm 及極高的線性增益 30.5 dB 。另外此增強型元件其最大的功率增加效率為 70%。

另一方面，先進的無線數位通訊系統，例 Wide-band Code-Division Multiple-Access (W-CDMA), 需要元件擁有高效率、良好的線性度及低消耗電壓等特性。因此，高效率且高線性度的增強型磷化銦鎵/砷化鋁鎵/砷化銦鎵元件極有發展的必要性。元件能夠在低電壓下操作必須有極低的 knee voltage ；線性度方面的改善，則需源自雙載子摻雜濃度的最佳化。本論文所製作之元件，當元件偏壓在 V_{DS} = 2V 時，最大轉導值為 448 mS/mm。 在 10 GHz 的頻率下，其最低雜訊指數為 0.86 dB 且增益為 12.21 dB 。此元件的 high output third order intercept point (OIP3)-P_{1dB} 為 13.2 dB ，且在 WCDMA 的調變訊號下有著極高的功率增加效率 35%。

另外，此論文也探討利用鉑作為蕭基接觸金屬的增強型的磷化銦鎵/砷化鋁鎵/砷化銦鎵元件。在依序濺鍍鉑/鈦/鉑/金為閘極金屬後，在 325℃ 下做退火處理，使得閘極金屬擴散下沈。退火後，元件的 threshold voltage (V_{th}) 自 0.17V 正向偏移至 0.41V，以及 源極漏電流從 1.56μA/mm 減低至 0.16μA/mm.這些特性

上的改善源自於 Schottky barrier height 的增高；在退火後，因為鉑擴散下沈的製程，使得閘極至通道的距離減低。而且 threshold voltage 的偏移非常均勻且具有相當高的再現性，並且在退火後，元件有著更好的 RF 功率特性。

最後，鉑金屬與磷化銦鎵 的界面反應也在此論文中討論。在濺鍍鉑金屬後，會有著約 7.5nm 厚的非晶系層存在。由穿透式電子顯微鏡的影像顯示，在 325℃ 下經過一分鐘的退火後，鉑 金屬會往磷化銦鎵層擴散至約 12.8nm 。且在 325℃ 下，經過十分鐘的退火後，成核現象開始於磷化銦鎵層中產生。另外，在相同溫度下，經過三小時的退火，即可發現新的相 Ga_2Pt (422) 及 $GaPt_3$ (422) 生成在鉑及磷化銦鎵的介面中。

The study of Enhancement-mode InGaP/AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor

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Abstract

In recent years, digital wireless communication technology develops rapidly around the world. It is believed that the digital wireless technologies are the major trends for the future wireless communication systems. The purpose of this dissertation is to develop the Enhancement-mode high-electron-mobility transistor (HEMT) for the digital wireless communication systems with improved device structures and the related process technologies.

In this dissertation, the InGaP/AlGaAs/InGaAs structure was used to fabricate the enhancement-mode high-electron-mobility transistors with the goal of further enhancement of the HEMT device performance. The attempt on using the InGaP/AlGaAs/InGaAs heterojunction instead of the InGaP/InGaAs is due to: Firstly, the conduction band discontinuity of the AlGaAs/InGaAs interface is superior to those form at the InGaP/InGaAs interface, the carrier confinement would be better. This will improve the output power performance of the InGaP PHEMTs. Secondly,

the interface between the AlGaAs/InGaAs interface is smoother than the InGaP/InGaAs interface due to the interdiffusion behavior of As and P atoms in the InGaP/InGaAs interface. As a result, the electron mobility of the InGaP/AlGaAs/InGaAs PHEMTs is higher than the electron mobility of the InGaP/InGaAs PHEMTs. The fabricated InGaP/AlGaAs/InGaAs HEMT 0.5×160 μm^2 device shows low knee voltage of 0.3V, a high drain-source current (I_{DS}) of 375mA/mm and a maximum transconductance of 550mS/mm when drain-source voltage (V_{DS}) was bias at 2.5V. High-frequency performance was also evaluated; the cut-off frequency (F_t) was 60GHz and the maximum oscillation frequency (F_{max}) was 128GHz. The E-mode InGaP/AlGaAs/InGaAs PHEMT also exhibited high output power density of 453mW/mm with high linear gain of 30.5dB at 2.4GHz. The maximum power-added-efficiency (PAE) of the device was 70%, when tuned for the maximum power added efficiency.

On the other hand, advanced digital wireless application systems, such as Wide-band Code-Division Multiple-Access (W-CDMA) system, has imposed stringent requirements on the devices while include high efficiency and high linearity operation with minimum DC power consumption. Thus, a high linearity and high efficiency Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT has to be developed. The low voltage operation is achieved by the very low knee voltage of the device and

the linearity is improved by optimizing the concentrations of the two delta-doped layers. Biased at a drain-to-source voltage V_{DS} = 2V, the fabricated device exhibited a maximum transconductance of 448 mS/mm. The measured minimum noise figure (NF_{min}) was 0.86 dB with 12.21 dB associated gain at 10 GHz. The device shows a high output third order intercept point (OIP3)-P_{1dB} of 13.2 dB and a high power efficiency of 35% when under wideband code-division multiple-access (W-CDMA) modulation signal.

In addition, an Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT using Platinum (Pt) as the Schottky contact metal was investigated for the first time. Following the Pt/Ti/Pt/Au gate metal deposition, the devices were thermally annealed at 325℃ for gate sinking. After the annealing, the device showed a positive threshold voltage (V_{th}) shift from 0.17V to 0.41V, and a very low drain leakage current of 0.16μA/mm which was reduced from 1.56μA/mm before gate sinking. These improvements are attributed to the Schottky barrier height increase and the decrease of the gate to channel distance as Pt sink into the InGaP Schottky layer during gate sinking process. The shift in the V_{th} was very uniform across a four inch wafer and was reproducible from wafer to wafer. The device also showed excellent RF power performance after the gate sinking process.

Finally, we had investigated the interfacial reaction between platinum and InGaP

in a Schottky diode structure. There was a 7.5 nm-thick amorphous layer formed at the interface between Pt and InGaP after metal deposition. After annealing at 325 ℃ for one minute, this amorphous layer increased to 12.8 nm and the reverse leakage current also decreased. The diffusion of Pt atoms and crystallization of amorphous layer took place after annealing at 325℃ for 10 minutes. Prolonging the annealing to 3 hours led to formation of Ga_2Pt and $GaPt_3$ phases in InGaP and Schottky diodes degraded after these new phases were observed.

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Chapter 1

Introduction

1-1 GaAs Material Propriety

Gallium arsenide is an III-V compound semiconductor; it is composed of Ga from column III of the periodic chart and As from the column V of the periodic chart. GaAs has some electronic properties which are superior to silicon's. It has a higher saturated electron velocity and a higher electron mobility which means that electrons can move faster in GaAs than in silicon, therefore, GaAs devices can operate at frequencies in excess of 250 GHz. Also, GaAs devices generate less noise than silicon devices when operated at high frequencies. GaAs devices also have higher power efficiency than Si devices when used as the devices.

The second major advantage of GaAs over silicon is the availability of the semi-insulating substrates. Silicon substrate generally can be made with resistivities above 100 Ω-cm. However, GaAs can be made with resistivities of 10^8Ω-cm. Therefore, the GaAs makes device isolation easier. The semi-insulating GaAs substrate greatly reduces parasitic capacitance and provides an ideal substrate on which to fabricate microwave monolithic integrated circuits.

GaAs devices exhibit higher radiation hardness than that of silicon devices due to that it has higher band-gap than silicon. Another advantage of GaAs is that it is a

direct band-gap semiconductor, which means that it can be used to emit light. Silicon is an indirect band-gap material can not be used as light emitting material (Nonetheless, recent advances may make silicon LEDs and lasers possible). These properties make GaAs applicable to mobile phone, satellite communication, microwave point-to-point link systems as well as optoelectronics applications. [1]- [4]

1-2 Pseudomorphic High Electron Mobility Transistor

Since the first AlGaAs/GaAs conventional high electron mobility transistor (HEMT) was introduced in 1980 [5], many researchers working on high frequency devices have gradually moved toward HEMT technology. HEMT technology is compelling because it provides improved carrier transport characteristics in the channel, and enhances the performance of the devices at higher frequencies.

Moreover, the adventages of molecular beam epitaxy (MBE) and metal-organic chemical vapor disposition (MOCVD) has improved the capability of composition, doping concentration and thickness control of the epitaxial materials. As a consequence, high quality epitaxial structures are realized for the design and development of the advanced high performance device structures. The research for realized the high performance device technology has moved HEMT structure from the conventional AlGaAs/GaAs material to more advanced Pseudomorphic

AlGaAs/InGaAs system due to the latter has higher electron mobility and current density. The AlGaAs/InGaAs Pseudomorphic HEMT is shown in Figure 1-1.

1-3 Enhancement-mode Pseudomorphic HEMT

The key advantage of Enhancement-mode Pseudomorphic HEMT (E-PHEMT) when used for wireless applications is that it can operate with a single positive voltage source. Ordinary depletion-mode PHEMTs conduct current at zero gate bias, or the drain current reaches a saturated level (Idss) when the applied gate voltage is zero volt. An E-PHEMT exhibited no conduction (zero current) at zero gate bias, so that Id=0 at V_{gs} =0V. Therefore, it can operate without the negative voltage required for the depletion-mode devices.

The energy band diagram for the E-PHEMT is as shown in Figure 1-2. At zero gate bias, the E-PHEMT structure is essentially fully depleted of conduction electron due to the conduction band is above the Fermi level. Therefore, the E-PHEMTs only require positive gate bias voltage for operation, and can be turned off with zero volts on the gate. Figure 1-3 illustrates how the electrons overcome the energy barriers with forward bias V_g. The dotted circles show where electrons accumulated. Below threshold ($V_g < V_{th}$), minor conduction occurs in the lower n-AlGaAs layer where the conduction band is slightly below the quasi-Fermi level F_{fn}. Between threshold and

turn-on ($V_{th}<V_g<V_F$), conduction occurs principally through the 2-DEG. At voltages above turn-on ($V_g>V_F$), the n-AlGaAs supply layer dips below E_{fn} and conduction transfers form the InGaAs 2-DEG to the n-AlGaAs layer and ,thus, the forward gate bias is limited by V_F [6]. Hence, the gate leakage current will dramatically increase when the forward gate bias is over V_F.

1-4 Outline of the Dissertation

In this dissertation, high performance Enhancement-mode InGaP/AlGaAs/InGaAs Pseudomorphic High electron mobility transistor with low noise figure, high gain, high power added efficiency (PAE) and high linearity operated at low bias voltage are realized for wireless communication system applications.

The brief descriptions of basic HEMT process and device characteristics are given in Chapter 2. Due to the devices are for millimeter wave application, sub-micro T-shape gates are required in this study and are realized by using e-beam lithography and Deep UV light. By using e-beam writer and bi-layer photo resist, the 0.15 μm gate length was developed. Also, in Chapter 3, the basic introductions of the DC and RF parameter for Low noise and power device are given. In addition, the power measurement system is also present.

Chapter 4 gived the 2-V operated Enhancement-mode InGaP/AlGaAs/InGaAs

PHEMT characteristics. In this study, the InGaP/AlGaAs/InGaAs PHEMTs instead of InGaP/InGaAs PHMETs are developed to further enhance the device performance. The attempt on using the InGaP/AlGaAs/InGaAs heterojunction instead of the InGaP/InGaAs is due to: Firstly, the conduction band discontinuity of the AlGaAs/InGaAs interface is superior to the InGaP/InGaAs, the carrier confinement would be better. This will improve the output power performance of the InGaP PHEMTs. Secondly, the interface between the AlGaAs/InGaAs interface is smoother than the InGaP/InGaAs interface due to the inter-diffusion behavior of As and P atoms in the InGaP/InGaAs interface.

Chapter 5 demonstrates a double delta-doped InGaP/AlGaAs/InGaAs E-mode PHEMT device capable of achieving low noise, high power efficiency, and high linearity with single voltage supply. For advanced high performance wireless application systems, such as Wide-band Code-Division Multiple-Access (W-CDMA) system, have imposed stringent requirements on the devices which include high power efficiency and high linearity operation with minimum DC power consumption. Conventional approaches in realizing both high linearity and high power simultaneously involve operating the power device at an output power level backed off from P_{1dB} by about 6 dB. In that sense, the efficiency at the operating power level usually suffers greatly from the power back-off for linearity considerations which in

turn consumes substantial system DC power. With low voltage operation achieved by the very low knee voltage of the device, the linearity is improved by optimal channel thickness and the use of double delta doping. This state-of-the-art device features a high PAE of 35% at maximum linear output power of 9.28 dBm under W-CDMA modulation.

Chapter 6 discusses the gate sinking effect of InGaP/AlGaAs/InGaAs E-mode PHEMT device with Pt/Ti/Pt/Au gate metals. The results show that Pt sinking is the dominant degradation mechanism. Pt sinking is caused by Pt diffusion into the InGaP Schottky barrier layer. Pt sinking explains the observed evolutions of the Schottky characteristics, Ids and gm transfer characteristic, and the S_{21} increase. Therefore, it is important to fully understand the gate sinking process techniques in order to further improve the reliability of the E-PHEMT devices.

In chapter 7, the interfacial reactions between Pt and InGaP are studied. Traditionally, the Ti/Pt/Au metals are used as Schottky contact metals on the InGaP layer. Although, the Pt exhibited a high Schottky barrier height on InGaP which can reduce the leakage current, but there are few reports using Pt/Ti/Pt/Au as the Schottky contact metals on InGaP. In the past few years, Pt/InP and Pt/GaAs interfacial reactions had been reported. After thermal annealing, both Pt-In phase and PtP_2 are present at the Pt and InP interface. Moreover, the PtGa and $PtAs_2$ are also observed

after the Pt and GaAs interfacial reaction. However, there are few reports investigating Pt and InGaP interfacial reactions; therefore the material analysis and current-voltage characterization are carried out to investigate the interactions between Pt and the InGaP Schottky barrier layer.

Finally, the results of the research in this dissertation are summarized and discussed in chapter 8 and also with suggestions to further impose the performance and reliability of the E-PHEMT devices.

Advantages of the GaAs HEMT

- **High electron mobility**
- **Small source resistance**
- **High F_t due to high electron velocity**
- **High transconductance due to high electron mobility and carrier concentration**
- **High output resistance**

Table 1-1 Advantages of HEMT device

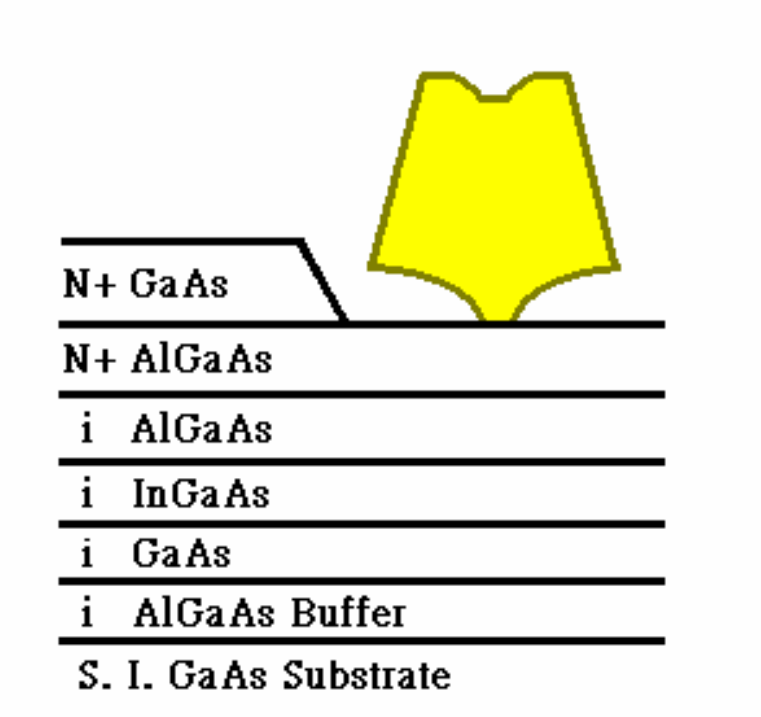


Figure 1-1 The structure of the low noise Pseudomorphic AlGaAs/InGaAs HEMT

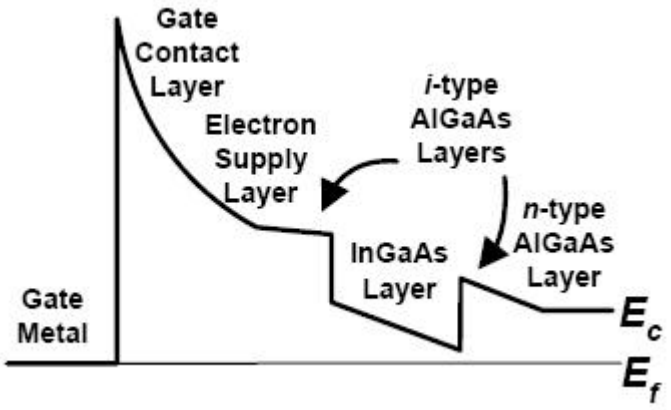


Figure 1-2 The energy band diagram of the E-PHEMT with no bias applied [6]

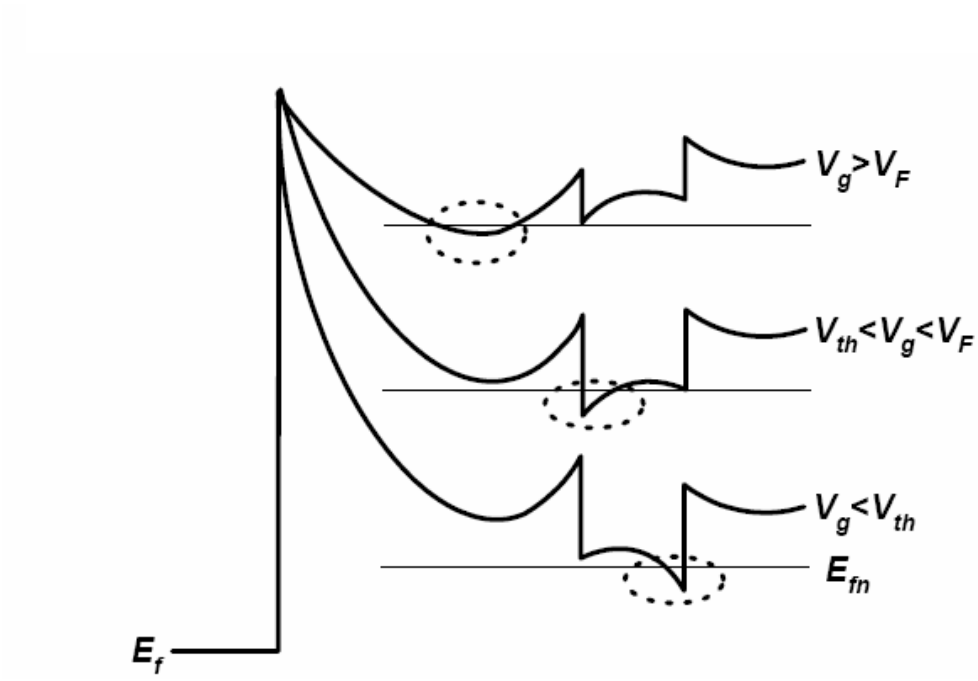


Figure 1-3 The band diagram of the E-PHEMT at three different gate voltages[6].

Chapter 2

Fabrication of Pseudomorphic HEMT

2-1 Introduction of PHEMT Structure

A high electron mobility transistor (HEMT) is a field effect transistor with a junction between two materials with different band gaps (i.e. a heterojunction). A commonly used combination is GaAs with AlGaAs. The large conduction-band discontinuity at AlGaAs/GaAs heterostructure allows for a high two-dimensional electron gas (2-DEG) concentration. The effect of this heterojunction is to create a very thin layer where the Fermi energy is above the conduction band, giving the channel very low resistance or high electron mobility. The high electron mobility transistor (HEMT) device takes advantages of the superior transport properties [2] and demonstrates superior low-noise performance over conventional Metal Semiconductor Field Effect Transistor (MESFET) [3]. Other names commonly applied to the device include heterojunction field-effect transistor (HFET); modulation-doped field-effect transistor (MODFET); selectively doped heterojunction transistor (SDHT); two-dimensional electron gas field-effect transistor (TEGFET). Table I summarize the advantages of the HEMT structure

A schematic diagram showing the HEMT conventional structure consists of

AlGaAs and GaAs layer is shown in Figure 2-1. The device structure composes of, from bottom to top, semi-insulating GaAs substrate; undoped GaAs buffer layer, undoped AlGaAs spacer, n^+ AlGaAs Schottky layer and n^+ GaAs cap layer. As in the MESFET, three metal electrode contacts – source, gate and drain are needed for the HEMT structure. The source and drain are ohmic contacts; the gate contact is a Schottky contact. Due to the higher conduction band discontinuity between AlGaAs and GaAs, free electrons diffuse from the doped AlGaAs Schottky layer into the undoped GaAs and form a two dimensional electron gas (2-DEG) at the hetero-interface [2].

For a clear understanding of the characteristics of the HEMT, it is necessary to realize the transport properties of the carriers. In the HEMT device, the electrons are transferred from the doped AlGaAs layer to the lower undoped GaAs layer, forming an accumulation layer of electrons in the potential well adjacent to the interface. Thus a 2-DEG with a high sheet carrier concentration exists at the hetero-interface and free to move in the other two spatial directions. In the HEMT device, this 2-DEG layer is used as the channel region, as shown in Figure 2-2. The electrons in the potential well are further separated from the ionized impurities so that the electron mobility is increased as compared to those in the doped semiconductor. The sheet carrier concentration is controlled by the application of a potential at the Schottky barrier

gate on the n-AlGaAs layer. The current which is in the channel region is via the drain and source ohmic contacts, and control by the Schottky barrier gate [3].

Other salient features of the HEMT active layer are thin “spacer layer” which composed of as undoped AlGaAs between the doped AlGaAs and undoped GaAs. The spacer layer further separates the 2-DEG form ionized donors at the interface which can increase electron mobility. The heavily doped GaAs cap layer was simply designed to form ohmic contacts to the device [3].

Conventional HEMT structure is consisted of AlGaAs/GaAs heterostructure. The band discontinuity improves as the Al content increases, the larger band discontinuity which results in better confinement of the electrons in the channel. However, when Al content is over 20%, the DX centers exists in the AlGaAs layer which trap the electrons and causes the reliability problem. To avoid the DX center problem and increase electron mobility, the AlGaAs/InGaAs HEMT was developed. As shown in Figure 2-3, there is a lattice constant mismatch between the InGaAs channel layer, AlGaAs spacer layer, and GaAs buffer layer. The strain from the lattice mismatch, it caused distortion of normal cubic crystalline InGaAs layer, as shown in Figure 2-4. The InGaAs layer is compressed to mirror the GaAs and is termed as “Pseudomorphic” layer [1]-[4].

The comparison of the conventional HEMT and the Pseudomorphic HEMT is

shown in Figure 2-5. With the same doping concentration and AlGaAs spacer thickness, the Pseudomorphic HEMT (PHEMT) structure exhibits higher electron mobility than the conventional HEMT due to the better carrier confinement and a true quantum well structure in the channel region [7] [8].

2-2 Device isolation

Device isolation is a fundamental step for all almost all GaAs MMIC or discrete device fabrication process. Isolation confines the electrically conductive portion of the wafer to specific areas and restricts the current flow in the "active" part of the device. There are three principal process used to achieve isolation: mesa etching, ion bombardment, and selective implantation. In this study, the wet mesa etching was used for device isolation [1].

Isolation serves a number of purposes:

(1) In active devices, it restricts the current flow to the desired path.

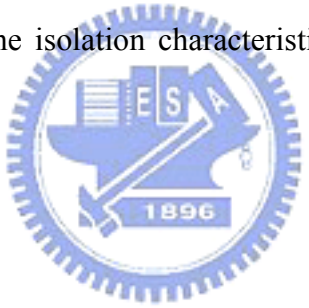
(2) Isolation reduces parasitic capacitances and resistances.

(3) Isolation provides a sufficiently insulating surface for construction of capacitors and transmission lines.

(4) Isolation also addresses the phenomenon know as backside gating or back-gating.

The simply device layout is illustrated in Figure 2-6. The source and drain metal

contact the active region and the current is forced to flow between source and drain and under the gate finger. In addition, the shape of the mesa edge is important. The presence of a step can cause difficulties in metal step coverage. If the edge profile is too steep or with undercut, these will be difficult for metallization over this edge. For the discrete device, the mesa isolation was performed by using HF-based solution and etched stop on buffer layer. The ideal profile for mesa isolation is shown in Figure 2-7. The isolation property can be inspected by the Current-Voltage measurement; the measured pattern and results are shown in Figure 2-8 and 2-9, respectively. According to the measurement results, the isolation characteristics and the epitaxy quality are excellent.



2-3 Ohmic Contact

The saturation voltage and the transconductance of the HEMT device are very sensitive to the contact resistance value of the device. The purpose of the ohmic contact on a semiconductor is allowing electrical current flow into or out of the semiconductor. The ohmic contact should have a linear I_V characteristics, be stable over time and temperature. Therefore, an ohmic contact is a low resistance junction providing conduction in both directions. Two general types of ohmic contacts are possible: The first type is the ideal none rectifying barrier, and the second is the

tunneling barrier [1]-[4].

In generally, if simply placing a metal in contact with the wide band-gap III-V semiconductor such as GaAs, it will result in a rectifying contact (a diode) rather than ohmic one [8] [9]. Theoretically, ohmic contacts are formed by joining an n-type semiconductor with work function ϕ_S to a metal with smaller work function ϕ_M, i.e., $\phi_S > \phi_M$. This situation is shown in Figure 2-10. The Fermi levels are aligned by the transfer electrons from the metal to the semiconductor. The excess electron charges in the n-type semiconductor exist essentially as a surface charge density which makes the surface of the semiconductor more n-type. If a positive voltage is applied to the metal, there is no barrier for electrons flowing from the semiconductor into the metal. If a positive voltage is applied to the semiconductor, the effective barrier height for the electrons flowing from the metal into the semiconductor will be approximately $\phi_{Bn} = \phi_n$, which is fairly small for a moderately to heavily doped semiconductor [9].

Figure 2-11a shows the energy band diagram when positive voltage is applied to the metal with respect to the semiconductor. Electrons can easily flow “downhill” from the semiconductor into the metal. Figure 2-11b shoes the case when a positive voltage is applied to the semiconductor with respect to the metal. Electrons can easily flow over the barrier from the metal into the semiconductor [9]. This junction is that

we called an “ohmic contact”.

Real ohmic contacts are fabricated by heavily doped semiconductor. If the doping is sufficiently high, the probability of tunneling through the barrier increases. Figure 2-12 shows a junction in which the metal is in contact with a heavily doped n-type epitaxial layer.

For ohmic metallization, the Au-Ge/Ni/Au system has been widely used as the ohmic contact to PHEMT. The alloyed AuGe ohmic contacts are formed through the alloying reaction of suitable metals with GaAs at temperatures higher than 400℃. As the annealing temperature increases, the AuGe alloy begins to melt and gallium diffuse into the metal. A small amount of arsenic evolves. Germanium atoms diffuses into the GaAs and act as dopants. The heavily Ge-doped GaAs layer formed below the contacts reduces the depletion layer width, resulting in the increase of the electron tunneling probability at the metal/GaAs interface [1]. In this contact system Nickel act as a wetting agent which prevents “balling up” of the metal and forms a conductive NiAs compound. In addition, the use of a top capping layer of gold can improve contact resistance. However, too much gold could getter more gallium than there is germanium available to replace it. It will result in gallium vacancies and cause a high resistance region [1].

The alloyed metal will have a very distinctive appearance when viewed using an

optical microscope. The metal will appear splotchy, having dark and light spots when viewed in a microscope. In fact, general experience is that such an appearance is necessary for forming the lowest resistance contacts. A contact that is either "over-alloyed" or "under-alloyed" will not only have a poorer contact resistance, but will also form a different morphology. Examples of these appearances are illustrated in Figure 2-13. From the experience, when there are 50 to 100 black spots in 100 μm^2, the contact resistance is usually better.

The basic technique used to measure contact resistance of planar ohmic contacts employs a test pattern composed of differently spaced ohmic contact pattern, as shown in Figure 2-14. A plot of the measured resistance as a function of spacing, L, will yield a straight line, as show in Figure 2-15. The slope leads to the sheet resistance with the contact width W independently measured. The intercept at L = 0 is $R_T = 2 R_C$ giving the contact resistance. The intercept at $R_T = 0$ gives $-d = 2L_T$, which in turn can be used to calculate the specific contact resistance. The transfer length method gives a complete characterization of the contact by providing the sheet resistance, the contact resistance, and the specific contact resistance. The optimization contact resistance is plotted as a function of alloy temperature as present in Figure 2-16.

2-4 Gate formation

In addition to the short gate length, a small gate resistance is essential for HEMTs for high gain, low noise, and high power applications. A short gate length is also important for high frequency and high speed HEMT devices. In general, one conventional approach for achieving low gate resistance is the use of a T-shaped or mushroom-shaped gate. In the T-shape structure, the small footprint defines the length and the wide top provides a low resistance. T-shape gates have been fabricated using Deep UV lithography or using multilayer resist technique with e-beam lithography. Figure 2-17 illustrates the process flow of using Deep-UV lithography. The SEM image of a 0.5 μm T-shaped gate is shown in Figure 2-18. The process flow of forming 0.15 μm T-gate bi-layer PMMA/PMMA-MAA photo-resist and the SEM image of lifted-off metal gate are shown in Figure 2-19 and 2-20, respectively.

The selective wet chemical gate recess etching has been widely used to achieve good current and threshold voltage uniformity for the HEMTs. From the previously reports, many efforts have been made to achieve a high selective etch between GaAs/AlGaAs. The etch Selectivity by using different solutions with various x values of the GaAs/$Al_xGa_{1-x}As$ structures are summarized in Table 2-2. In citric acid system, the selectivity of 2700, 159, 143, 137 for GaAs over $Al_xGa_{1-x}As$ with x=1, x=0.3, x=0.23, x=0.2, respectively, using the 1.5:1 solution of citric acid/H_2O_2 at 23℃.

The wet etching mechanisms generally include both diffusion limited and reaction rate limited process. Wet chemical etching proceeds through chemical reactions that occurred at the surface of the material. The etchant must reach the surface in order that appropriate reactions could occur and the reaction products should be removed from the surface. If the etching is reaction rate limited, then the material dissolution is a function of the chemical reaction rate between the etchant and the semiconductor.

For the reaction rate limited mechanism, etching rate is linearly proportional to the etching time, and is unaffected by stirring or agitation of the liquid etchant. If it is diffusion limited etching, the material dissolution depends on the transport of the active etching components to the material surface and on the removal of the reaction products away from the surface. Therefore, etching rate is proportional to the square root of the etching time, and increases with the agitation of the liquid etchants.

In generally, the etchants will contain oxidizer and the dissolving agent. The hydrogen peroxide is usually used as the oxidizing agent. The citric acid based solution is the dissolving agents in the selective etching solution. Most etchants for GaAs operate by oxidizing the surface first and then dissolve the oxides, thereby removing the reacted oxides. As a results, the lower etch rate was observed for $Al_xGa_{1-x}As$ with increasing x due to the formation of Al_xO_y which is difficult to remove by the citric acid.

After the gate lithography and resist development, the exposed HEMT channel area

is recessed to achieve the desired channel current and threshold voltage. In addition, the donor layer of the HEMT is very thin and heavily doped, therefore, the HEMT gate recess is more difficult to control than that of GaAs MESFET. The depth to which the gate is recessed is a critical parameter in FET performance. The method used to control the etch depth is to monitor the source-to-drain current during the etching process. The saturated current is reduced as the slot is etched into slice as shown in Figure 2-21 and the test key of current monitor as shown in Figure 2-22. The slot is etched until the target recess current is reached. This requires alternate steps of etching and current measurement, so it is not possible to monitor current while wet etching is proceeding. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over recess process, and reach the target current value without overshooting. Placing the metallization on the GaAs creates a zero-bias depletion zone in the GaAs and results in a saturated drain current drop after metallization. Therefore, the recess etching process must use a target current than that of the desired device current.

Pseudomorphic HEMTs have demonstrated exceptional power performance at millimeter frequency. The limiting factor of power performance has been the relatively low gate-drain breakdown voltage. The use of an undoped cap has been suggested to alleviate this limitation. However, this can increase both the source and

drain parasitic resistances leading to degraded microwave performance. A common technique used to improve the breakdown voltage while maintaining low source resistance is to use a doped cap and offset the gate toward the source side of a wide recess trench. This process requires two lithography steps, one to define the large area where the doped cap is to be removed, and the other to define the much narrower region for gate recess and metallization, as illustrated in Figure 2-23.

After gate recess process, the wafer was cleaned in the solution of HCL: H_2O = 1:10 solution to remove the native oxide and the gate metal Ti/Pt/Au was deposited by e-beam evaporator [1].

2-5 Device Passivation

HEMT devices are sensitive to surface effects in the device channel area. Long term degradation can occur due to oxidation or particulate contamination. Dielectric films are typically used in GaAs process for environmental encapsulation. The dielectric seals the surface, keeping humidity, chemicals, gases, and particles away from the sensitive areas of the device. Device passivation requires a pin-hole free, uniform, and low-loss dielectric film [3].

Silicon nitride (Si_3N_4) was used for passivation by using plasma-enhanced chemical vapor deposition (PECVD) after gate metal lift-off as shown in Figure 2-24. The film

thickness is about 100nm and the refraction index is 2.0. Figure 2-25 illustrates the dependence of the refraction index of a PECVD silicon nitride film with SiH_4. Then, passivation via-hole pattern was defined by lithography and reactive ion etching (RIE) was performed to etch the silicon nitride film.

2-6 Plating and Bridge Interconnections

Planting process is the last major step for the front-side process. This process is used to connect electrodes of the device with cross over the lower level metallization. Air has a dielectric constant of one; therefore the parasitic capacitance between the bridge and metallization beneath can be reduced.

Gold Plating are usually used for air bridges due to the fact that it has good electrical conductivity, is easily soldered or welded and is resistant to oxidation. Gold is not only ductile, but also resistant to the attack by most acids. Gold used in the microelectronics is very pure, usually 99.99% or even better [1].

Planting air Bridges are illustrated in Figure 2-26 and are widely used in the GaAs devices and MMICs for interconnections. They are used as interconnect for FETs to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor. Usually, there is only air between the bridge and the wafer beneath; this is why they are called air-bridges.

GaAs RF devices requires low parasitic resistance, therefore benefit from the metal thickness of the plated gold. Overall, air-bridge crossover is less capacitive than the crossover with dielectric layer by a factor of five to twenty typically [1].

The major typical steps of processes are illustrated in Figure 2-27. A layer of resist is spun and patterned for metal pads. The thickness of the first layer of resist determines the spacing between the bridge and material beneath. Hence, this layer of resist is usually rather thick – on the order of 2 to 4 μm. Then thin Ti/Au/Ti metal layers were deposited by evaporator. Next, a second coating of resist is applied and patterned. Then, the top of Ti layer would be removed by wet chemical etching, thus the thin Au metal layer could conduct the planting current through the whole wafer. After Au planting, the top resist, thin metal, and lower resist are removed, leaving the planting air-bridge.

2-7 Back- side process

As shown in Figure 2-28, the back side process of the HEMT consists of four major processing steps. The final steps in HEMT fabrication are wafer thinning and via-hole formation. The substrate is thinned from the backside to impose thermal impedance and to make it easy for chip separation. A final substrate thickness of 4 mils is typically used for microwave low noise HEMTs and MMICs. For power application, a

substrate thickness of 2 mils has been adopted for lower thermal impedance [3].

The via-holes provide low-inductance source grounding which is critically important for high frequency power HEMTs. Via-holes can be formed with a wet chemical etch or RIE dry etch. The RIE via-holes process is less sensitive to the uniformity of the final substrate thickness and also provides smaller vias with controlled etch profile [1] [3]. For a multi-fingers power device, small RIE via holes can be placed directly under each source finger or pad for better thermal inductance.

After the via hole formation, the backside of the wafer is metallized as shown in Figure 2-29. The chips are then separated through a wafer sawing or a scribe-and-break.

Al mole fraction of AlxGa1-xAs	Volume ratio of 50% citric acid/H2O2	Selectivity
1.0	1.5:1	2700
0.45	4:1	260
0.3	10:1	95
0.3	5:1	116
0.3	3:1	155
0.3	1.5:1	159
0.28	1:2	200
0.28	4:1	80
0.23	1.5:1	143
0.2	3:1	43
0.2	1.5:1	137
0.15	3:1	23

Table 2-1 Selectivity of using different solutions with various x values of the GaAs/$Al_xGa_{1-x}As$ structures.

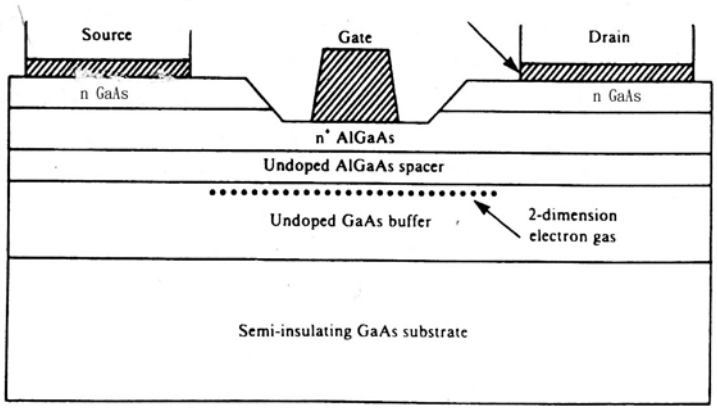


Figure 2-1 Schematic of the cross section of the conventional HEMT [3].

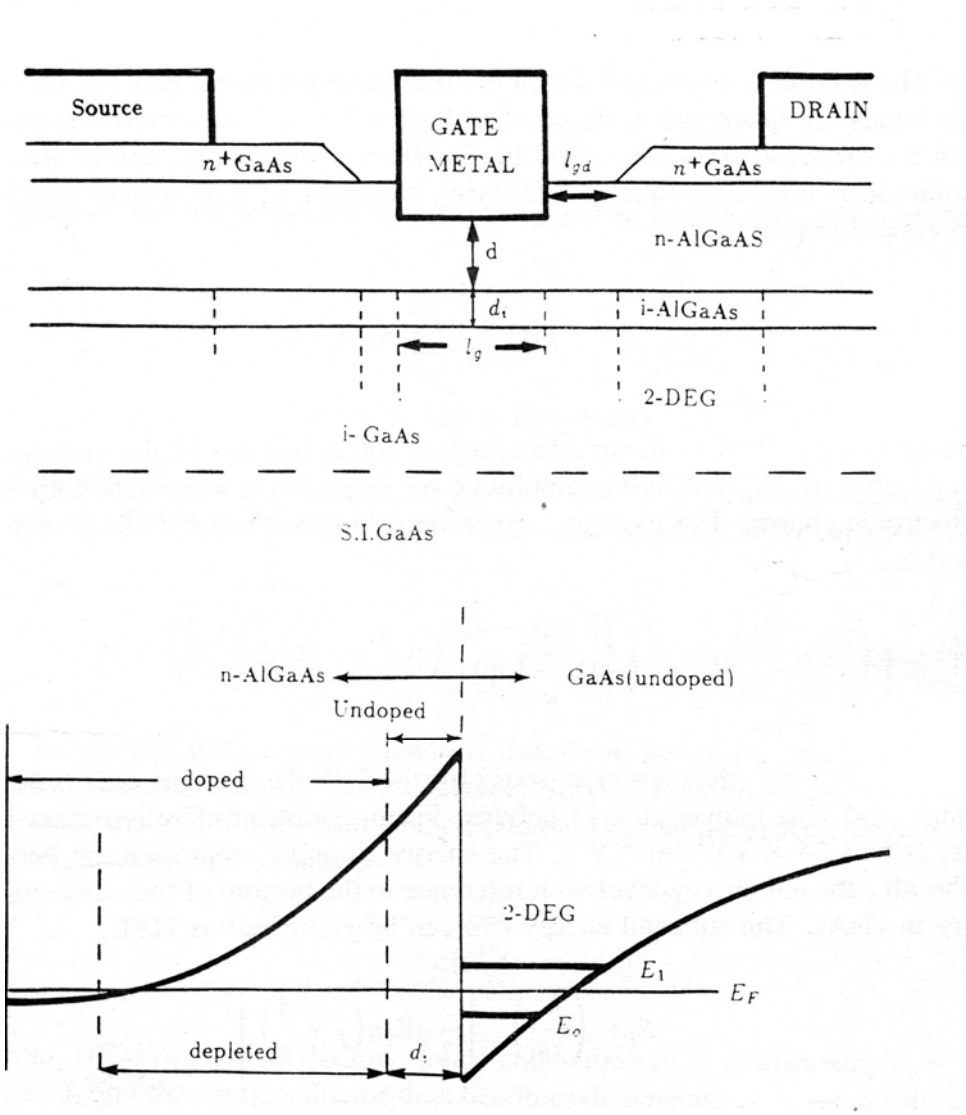


Figure 2-2 The energy-band diagram of the conventional HEMT [3]

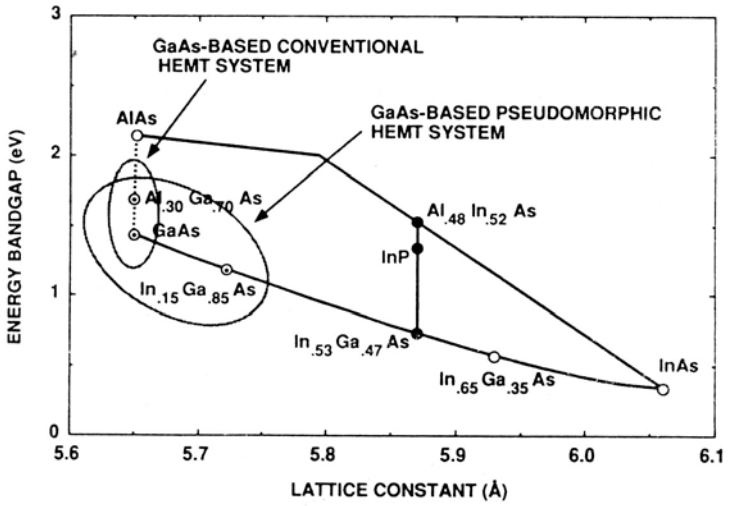


Figure 2-3 Lattice constant versus band-gap for III-V material[3]

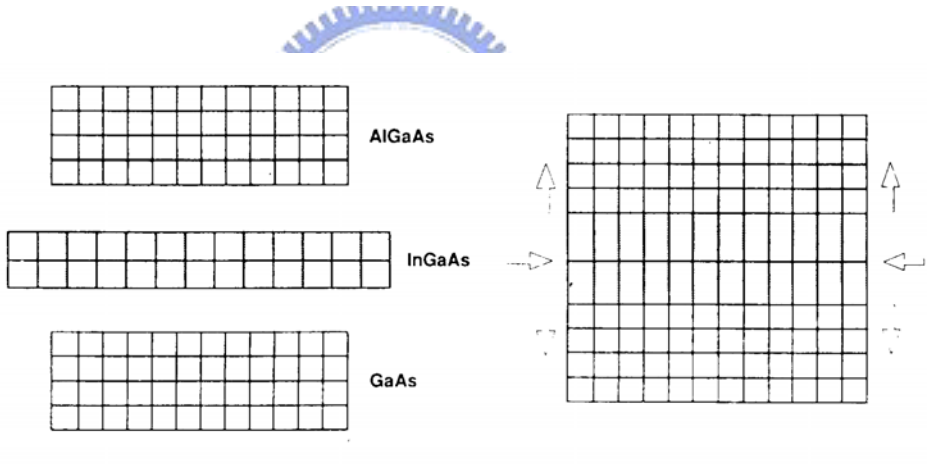


Figure 2-4 Schematic of the lattice of the Pseudomorphic HEMT structure [3].

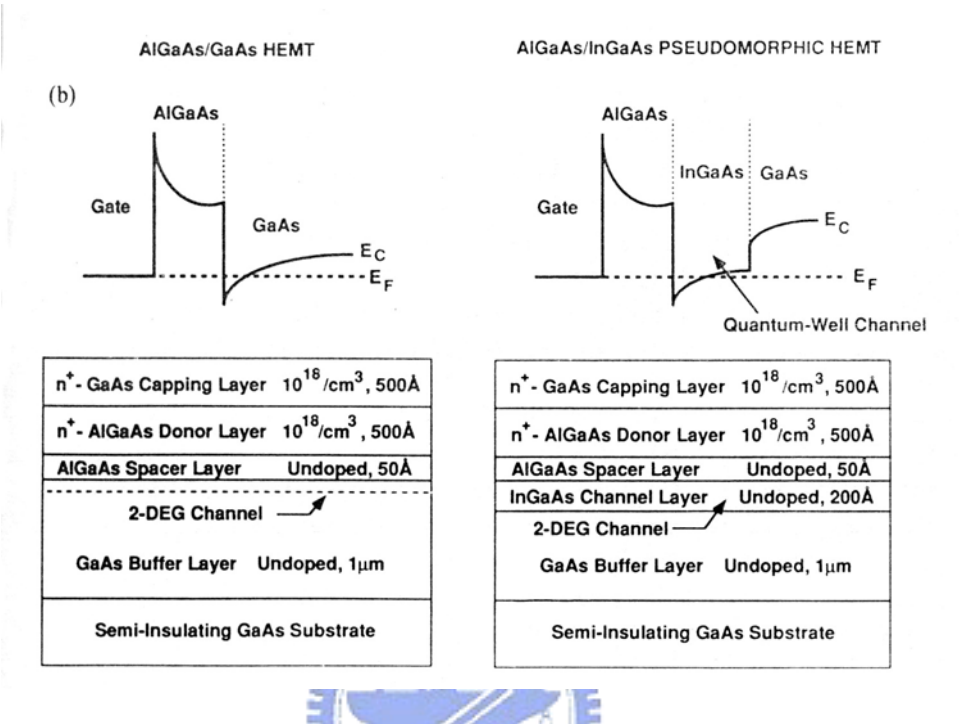


Figure 2-5 The comparison of the structure and the band diagram of the conventional HEMT and Pseudomorphic HEMT [3].

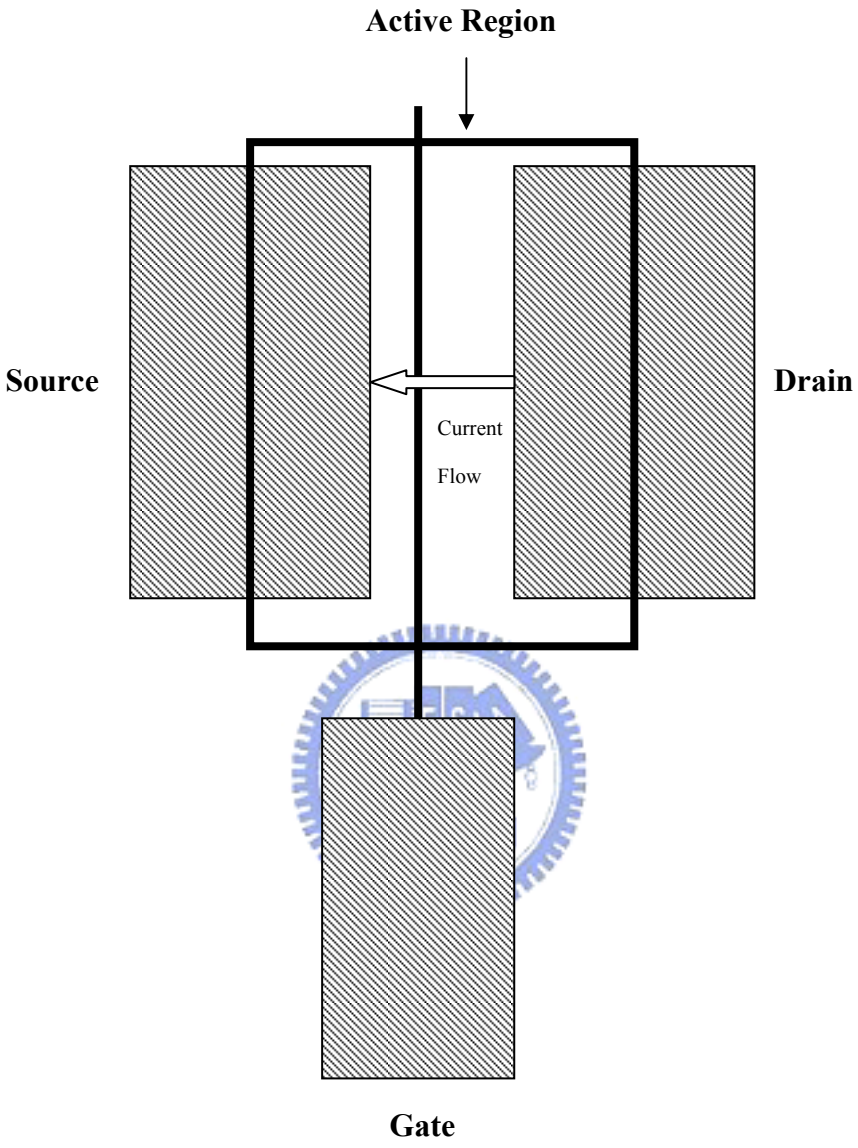


Figure 2-6 Schematic of the device layout

Figure 2-7 The ideal mesa edge profiles produced on (100) GaAs surfaces by using HF solution.

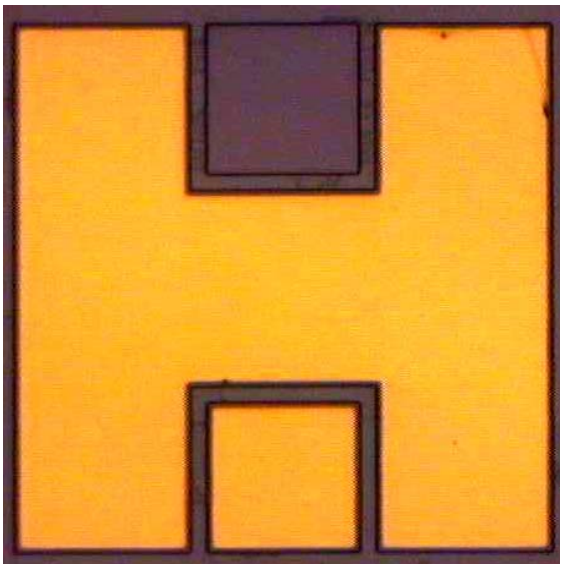


Figure 2-8 The test key for device isolation.

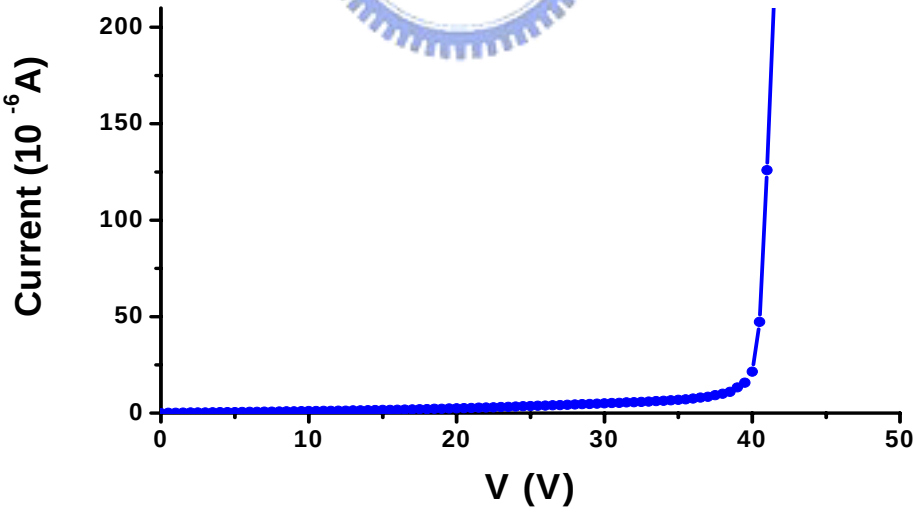


Figure 2-9 Device isolation I-V characteristic.

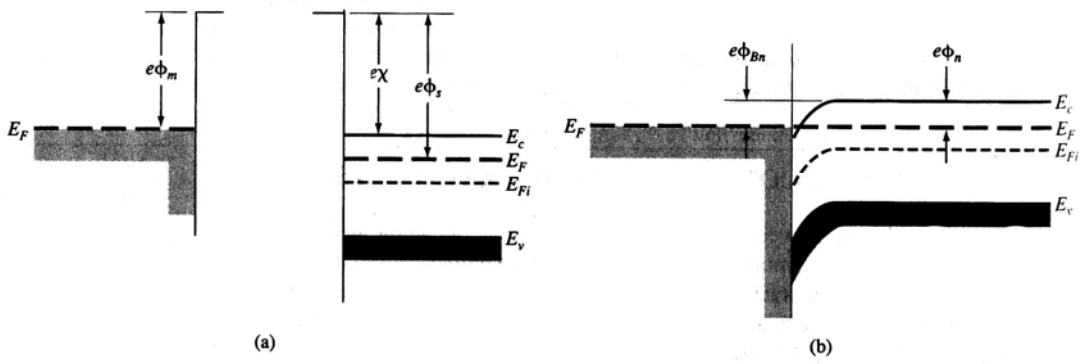


Figure 2-10 Band diagram for an idealized ohmic contact for a metal –N type-semiconductor junction (a) before contact and (b) after contact [9].

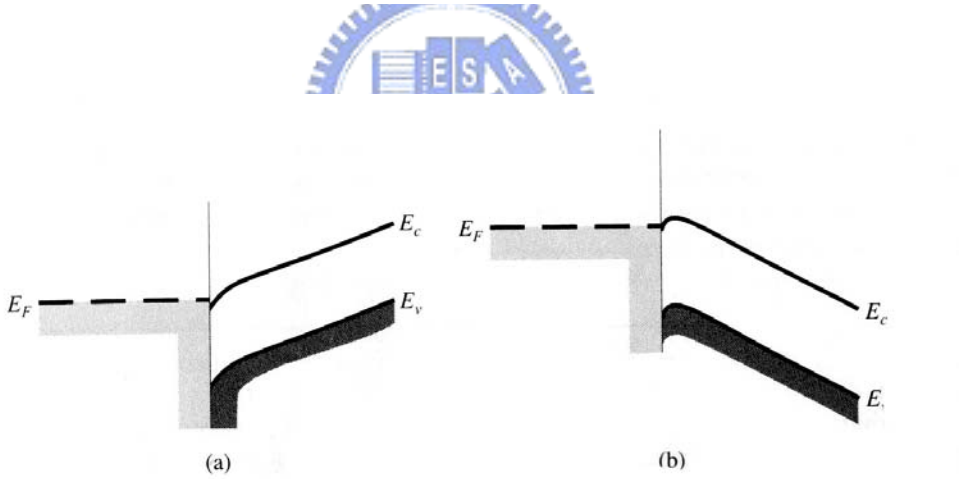


Figure 2-11 Ideal energy-band diagram of a metal- n type semiconductor ohmic contact. (a) with a positive voltage applied to the metal and (b) with a positive voltage applied to the semiconductor [9].

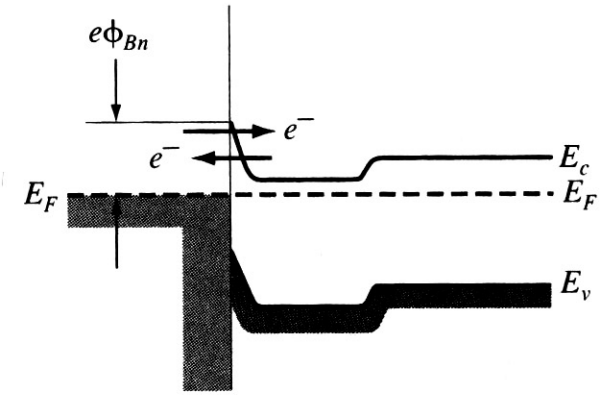
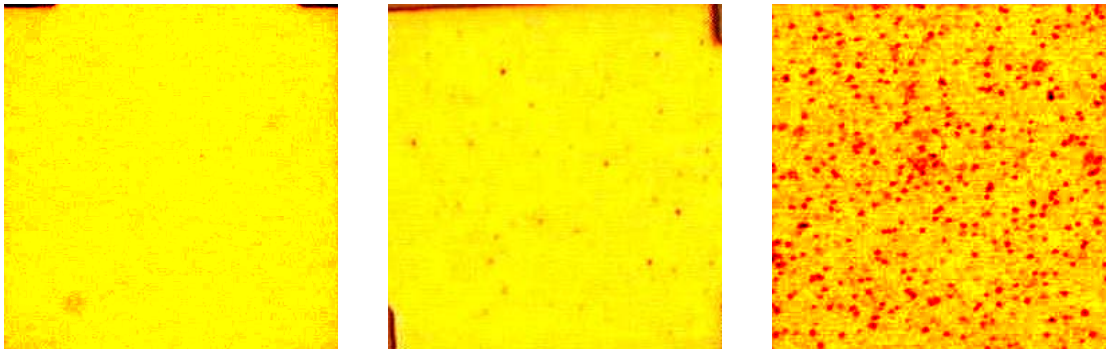


Figure 2-12 Energy band diagram of a heavily doped n-semiconductor to metal junction[9].



(a) (b) (c)

Figure 2-13 Alloyed AuGe/Ni/Au contacts, showing typical patterns if (a) under-alloyed; (b) alloyed correctly; (c) over-alloyed

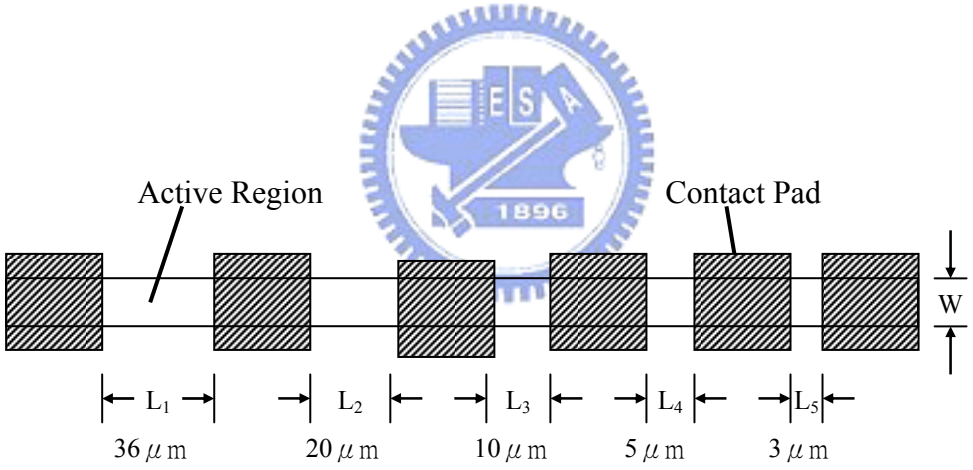


Figure 2-14 Ohmic contacts are separated by increasing distances.

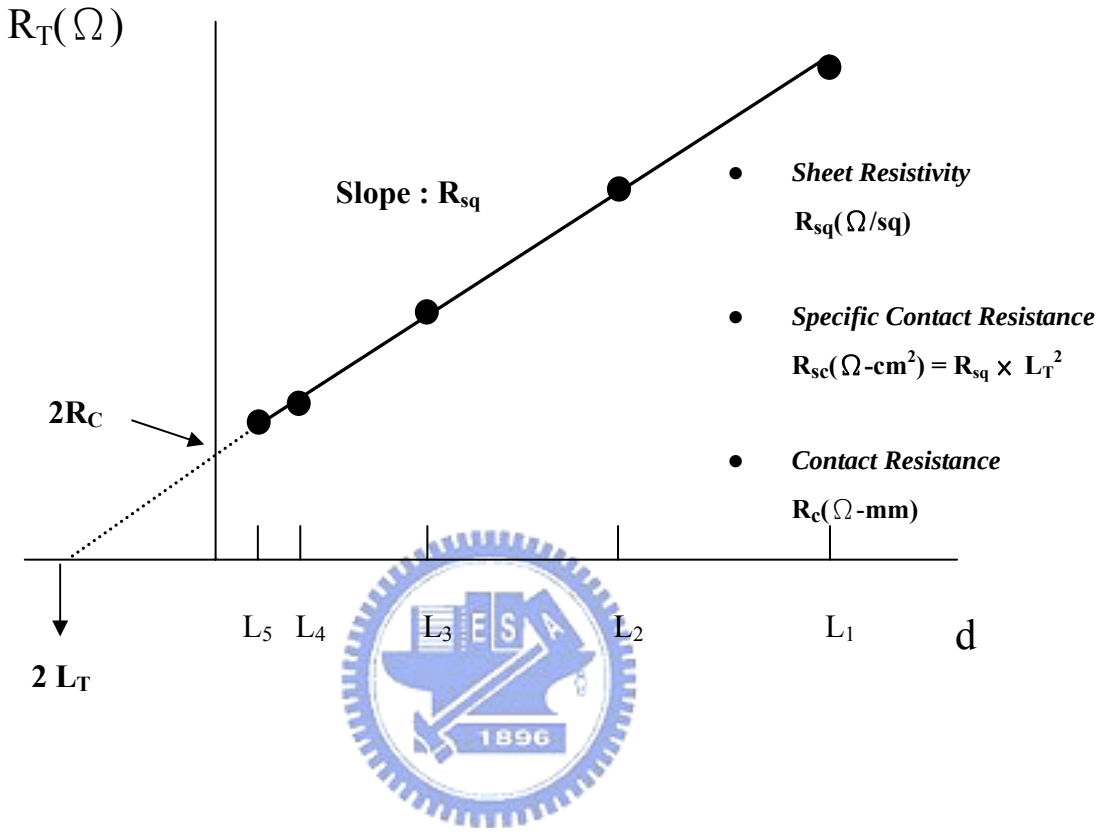


Figure 2-15 Plot of measured resistance as a function of contact separation

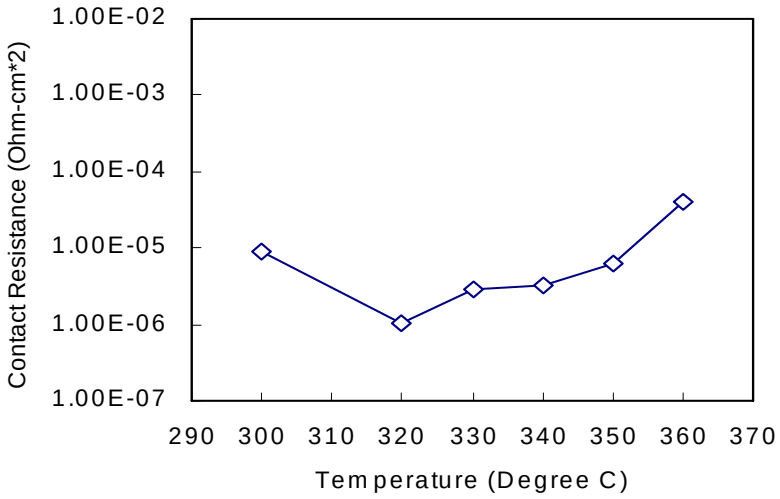
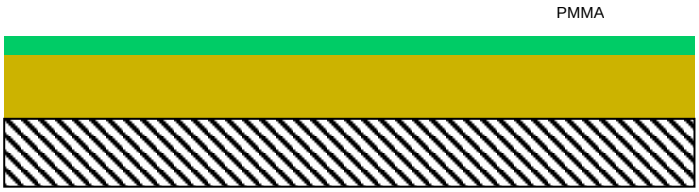


Figure 2-16 Plot of the contact resistance as a function of alloy temperature.

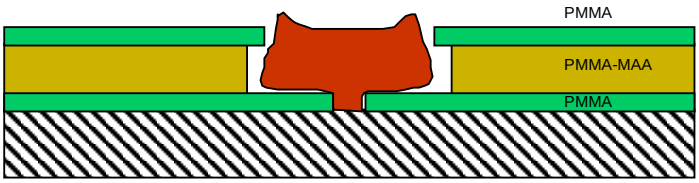
Spin 0.2um PMMA (Bake at 180℃)

Spin 0.6um PMMA-MAA (bake at 180℃)



Spin 0.2um PMMA (Bake at 180℃)

Exposure and Develop in developer MIBK:IPA – 180 sec



Gate Metalize, (Tape Lift and Solvent Clean not shown)

Figure 2-17 Process flow of the T-shape gate using Deep-UV aligner.

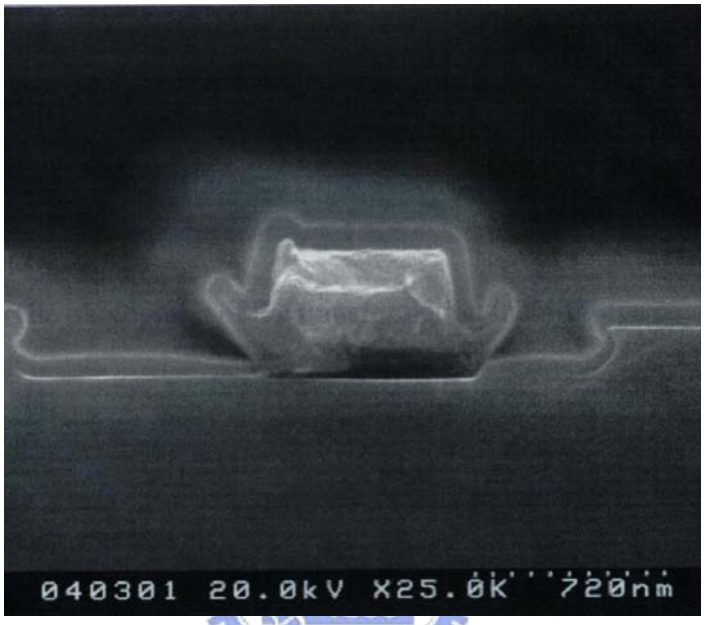


Figure 2-18 SEM image of the 0.5μm tri-layer T-shaped gate using D-UV aligner.

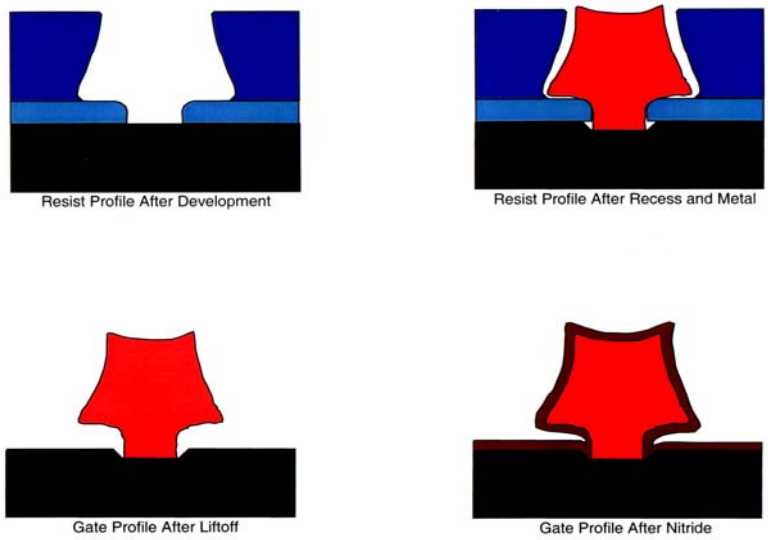


Figure 2-19 Process flow of the bi-layer T-shaped gate.

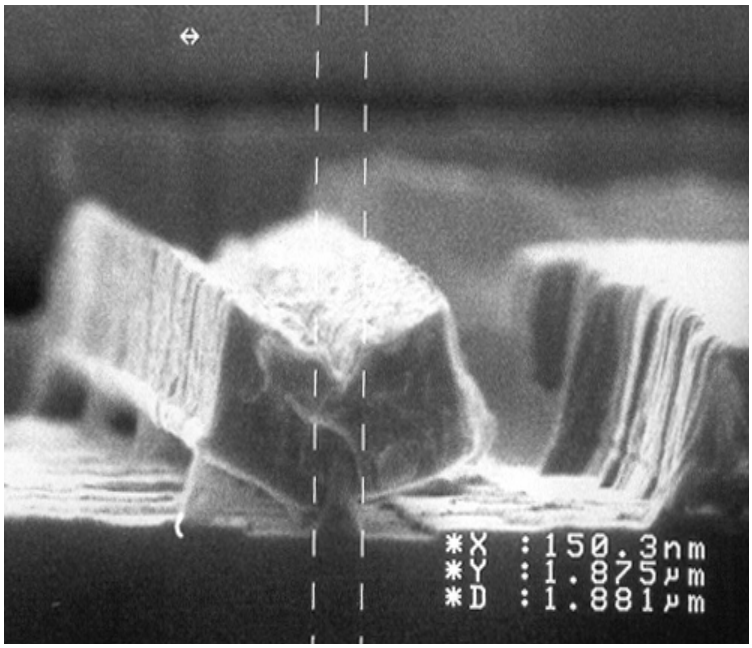


Figure 2-20 SEM image of the 0.15 μ m T-shaped gate using E-beam writer.

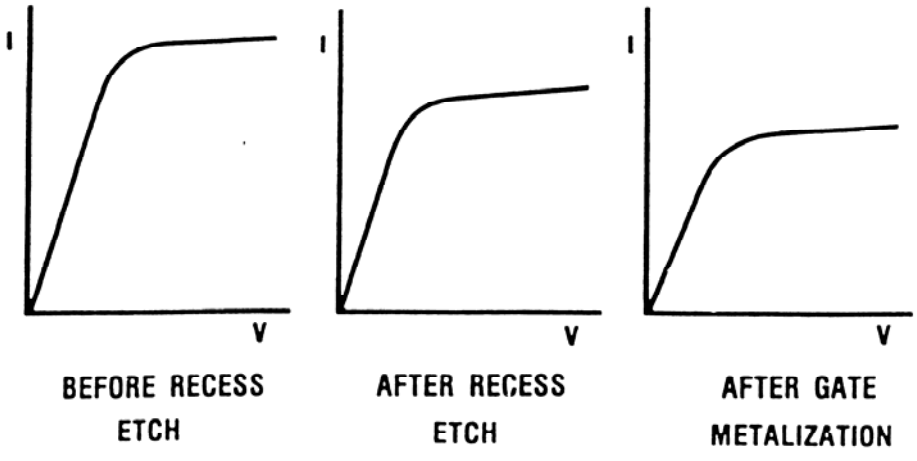


Figure 2-21 Saturation current before gate recess, after gate recess, and after gate metallization [1].

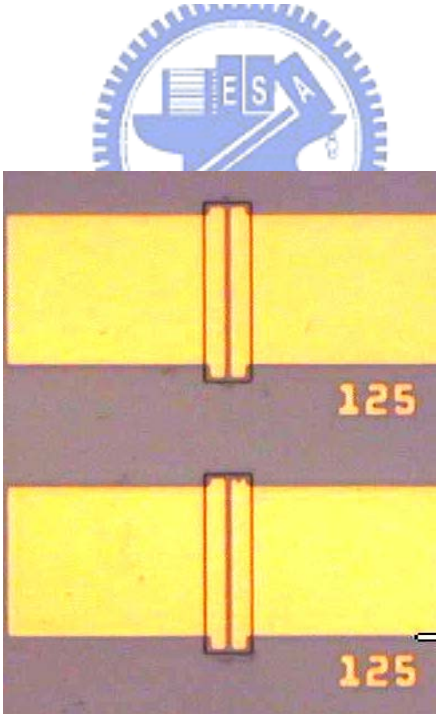


Figure 2-22 The test key for the current monitor after recess etch

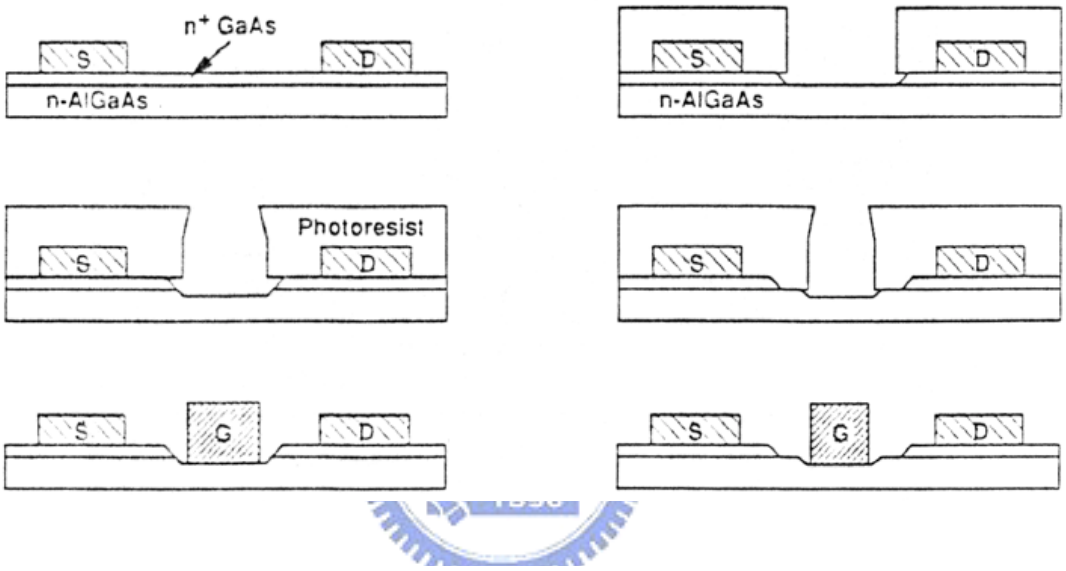


Figure 2-23 The comparison of single and double recess process

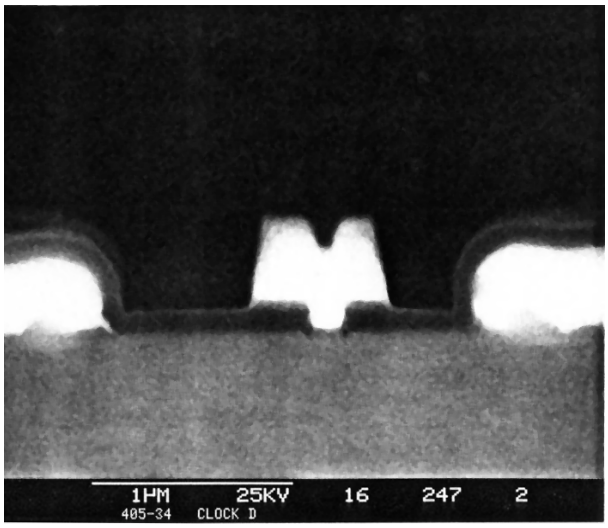


Figure 2-24 The SEM image of the device after Si_3N_4 deposition.

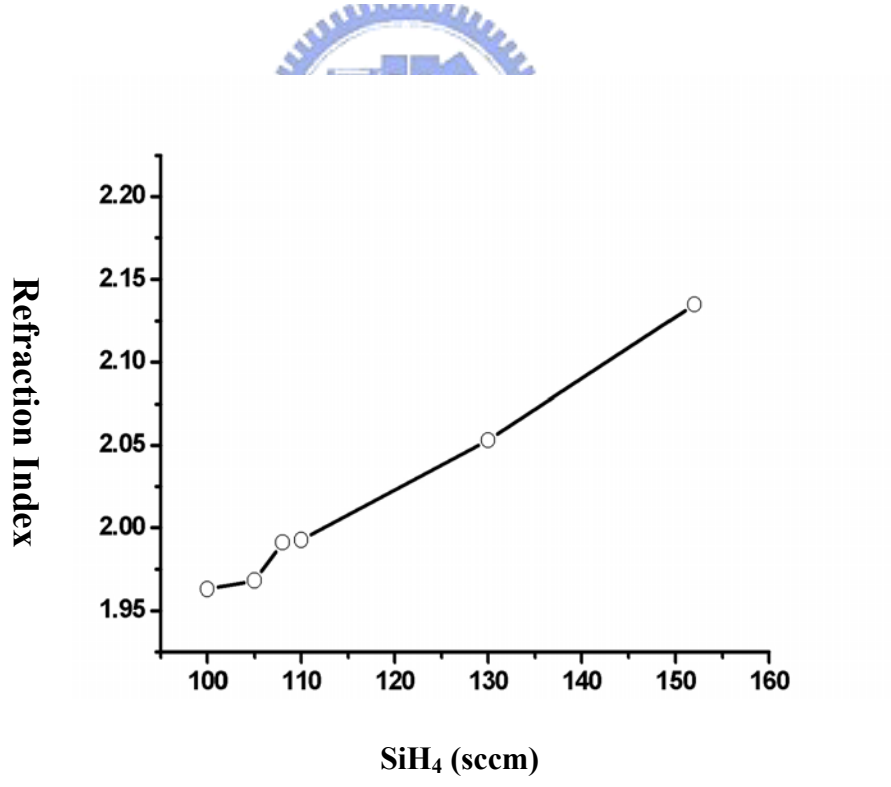


Figure 2-25 Dependence of the refracting index of a PECVD silicon nitride film on the of SiH_4 flow rate.

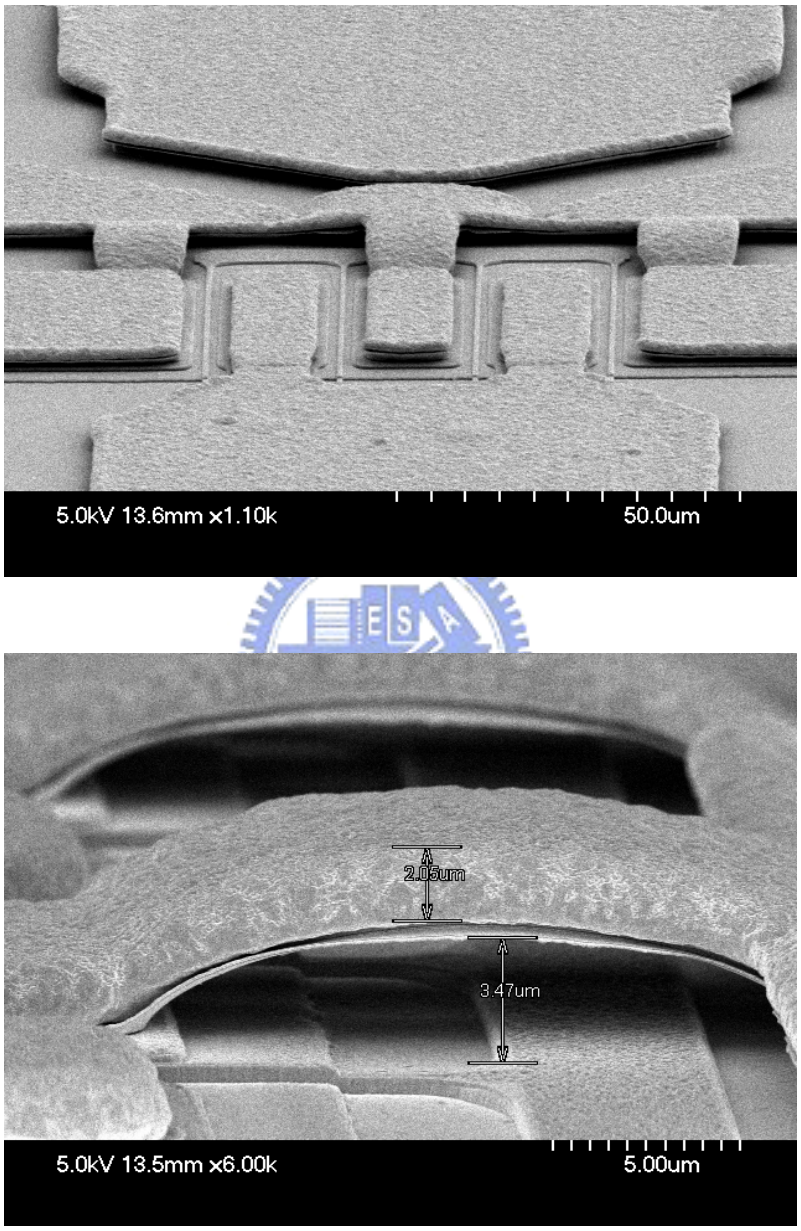


Figure 2-26 SEM images of a plated air bridge structure

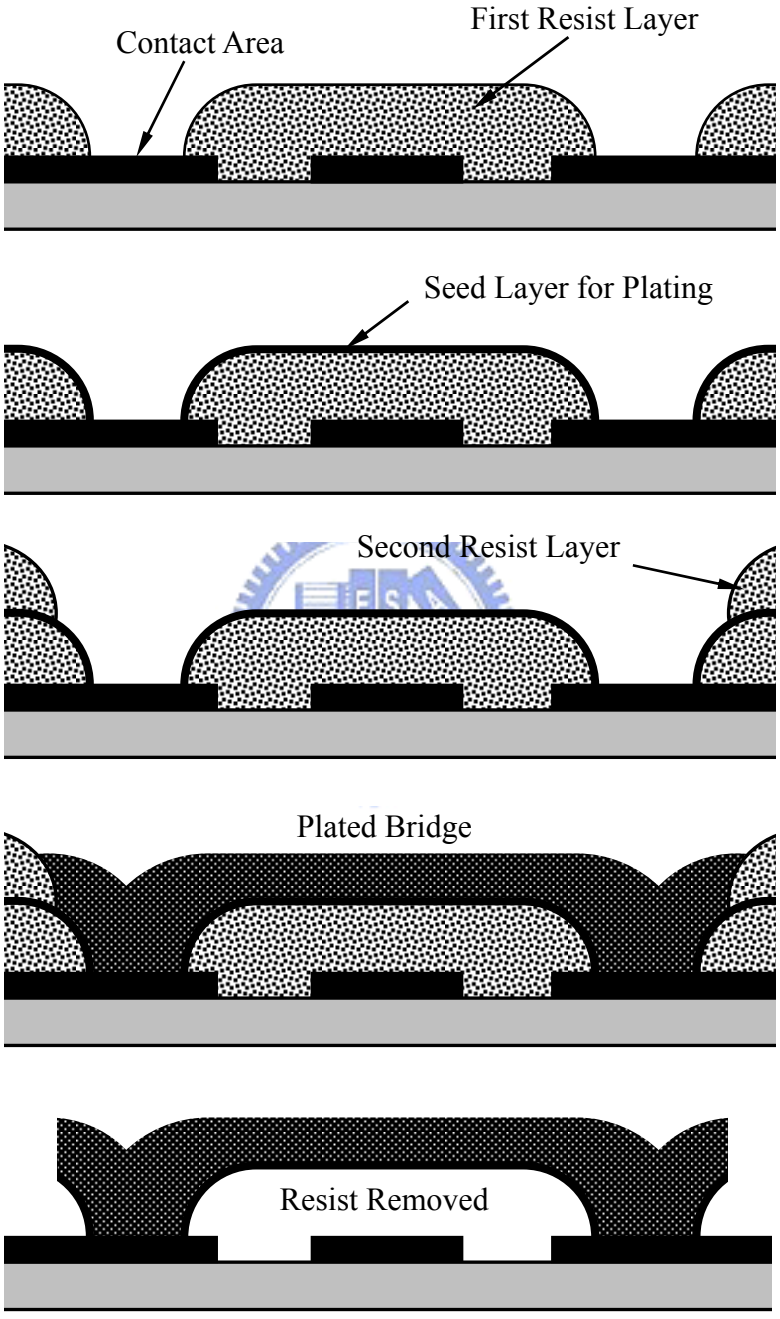


Figure 2-27 Major steps in air bridge process

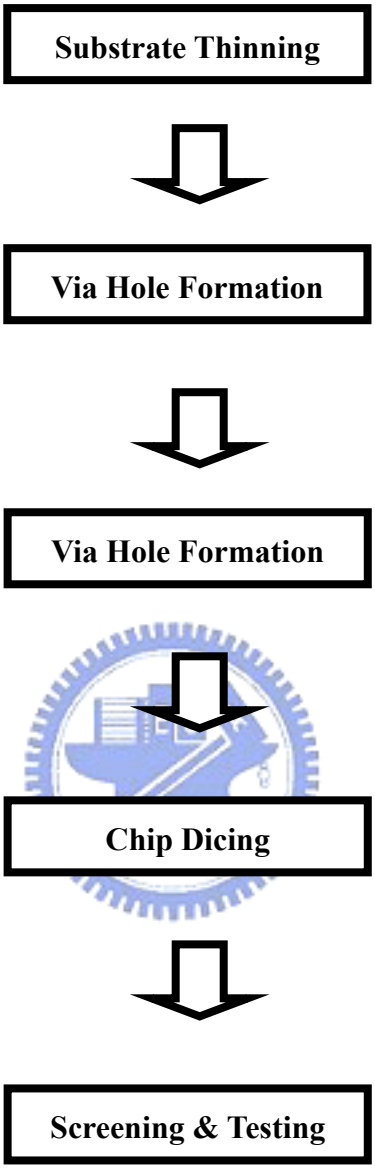


Figure 2-28 Typical back-side process flow chart for HEMTs

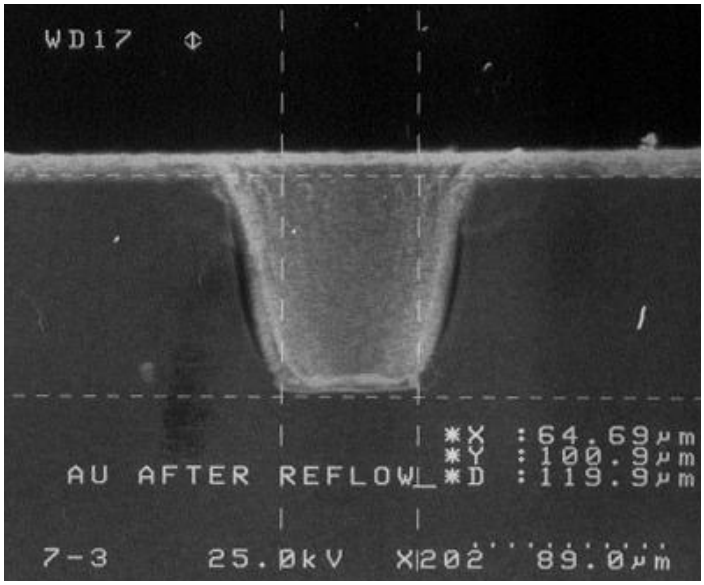


Figure 2-29 Cross section view of the metallized via-hole.

Chapter 3

Device Characterizations

3-1 DC characteristics

The DC characteristics also directly related to the high frequency performance, such as gain, noise figure, and power performance. The DC characteristics in this study are listed below.

Drain-to-Source Current (I_{DS})-The two currents of interest in HEMT are follows:

I_{DSS} = the saturate source drain current (Vgs = 0V)

I_{max}= the maximum source-drain current (under forward gate bias)

The methods normally used to specify I_{DSS} as the source-drain current at specified source-drain voltage with Vgs =0, as seen point A on the Figure 3-1. Figure 3-1 shows the conventional current-voltage characteristic of a 0.25μm × 160μm device. I_{max} is determined by forward biasing gate and limited by forward breakdown voltage. The preferred method is to specify the forward gate current (per unit gate width) and to define I_{max} to be the source-drain current at the forward gate current [1].

Knee voltage- This parameter is defined as the voltage source and drain at which current saturation occurs. The definition is illustrated point B on the Figure 3-1: the intersection of lines fitted to the linear and saturated parts of the trace [1]

Pinch-off voltage-This parameter is the gate voltage at which the drain-to-source current is reduced to a given value, usually 1mA/mm or 1%~2% of I_{DSS}. See point C on the curves in Figure 3-1.

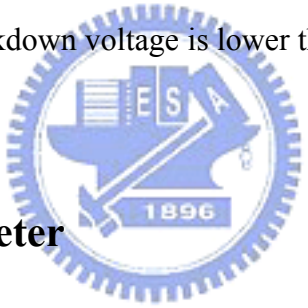
Transconductance (g_m)-This parameter is the DC common source conductance; that is the incremental change in drain current with a given change in gate voltage. The transconductance is defined as:

$$g_m = \Delta I_{ds} / \Delta V_{gs}$$

Figure 3-2 presents the measured transconductance of a 0.25μm × 160μm device as a function of the gate-source voltage. The transconductance is essentially zero for gate bias levels below the pinch-off voltage. As the gate bias is toward zero, the transconductance increases monotonically. The device transconductance is greatly affected by the device dimensions and the channel material property. Because of the drain current and the transconductance are directly proportional to the gate width. For this reason, comparisons between devices are often made by examining the transconductance per unit gate width [1].

Breakdown voltage-The breakdown characteristics of the gate can be measured in both directions (gate-to-drain and gate-to –source). In general, only one of the two is needed to verify device characteristics. Most often the gate-to-drain breakdown characteristic is used. The breakdown voltage is a function not only of material

parameters (doping level, energy band gap, Schottky barrier height, etc), but also are highly sensitive to surface conditions near the gate region. The breakdown voltage is also dependent on the device geometry, especially the gate-to-source spacing. If the gate is offset toward the source, the breakdown voltage on the drain side will be greater than that on the source side. There are two ways of characterizing the breakdown characteristic: Specifying the gate-to-drain current and measuring the voltage at that point (BV_{gd}), or specifying the voltage and measuring the reverse current (I_{gd}). In either case, they are failing when either the reverse current exceeds the specified value or the breakdown voltage is lower than the specified value [10].



3-2 Scattering Parameter

Scattering Parameters, generally referred to as S-parameter, are fundamental to microwave measurement. These parameters completely and uniquely define the small signal gain and input/output emittance properties of any linear two port network [10].

S-parameters are defined analytically by:

$$b_1 = S_{11}a_1 + S_{22}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

where (referring to Figure 3-4):

a_1 = (Incoming power at port 1)$^{1/2}$

b_1 = (Outgoing power at port 1)$^{1/2}$

a_2 = (Incoming power at port 2)$^{1/2}$

b_2 = (Outgoing power at port 2)$^{1/2}$

E_1,E_2 = Electrical stimuli at Port 1, Port 2

z_o = Characteristic Impedance = (50 +j0) Ohms

From Figure 3-4 and define linear equations for $E_2 = 0$, then $a_2 = 0$, and:

$S_{11} = \frac{b_1}{a_1}$ = input reflection coefficient

$S_{21} = \frac{b_2}{a_1}$ = forward transmission coefficient

$S_{12} = \frac{b_1}{a_2}$ = reverse reflection coefficient

$S_{22} = \frac{b_2}{a_2}$ = output reflection coefficient

$|S_{21}|^2$ = power gain with load and source impedance

With this information, the functional relationships to gain, stability, input and output matching impedance can be readily derived from the S-parameters. Table 3-1 lists the most useful relationships required for device characterization.

Available power gain - It is the ratio of the power available at the output of a network to the power available from the generator. Available gain is a function of the network s-parameters and the source reflection coefficient. It is independent on the load reflection coefficient.

Stability factor (K factor) - A two port network is unconditionally stable (K>1) if there exists no combination of passive load or source impedances which will allow the circuit to oscillate [10].

Maximum available gain - It is the power gain obtained when the input and output ports are simultaneously conjugated matched to source and load impedances, respectively. Implicit in the definition is the assumption that two port device is unconditionally stable. On the other hand, the maximum available gain (MAG) of a device is only defined where K is greater than one. This is because the term under the square-root becomes negative for values of K less than 1. Another way to look at it is that maximum available gain is infinite. Infinite gain means oscillator.

Maximum stable gain - The maximum stable gain (MSG) of a device is defined when maximum available gain is undefined (K<1). It is merely the ratio of $|S_{21}|/|S_{12}|$. Under no circumstances should you try to treat more than this amount of gain from a conditionally stable device. The MSG can be obtained if the transistor is potentially unstable according to the equation:

$$MSG = MAG\big|_{K=1} = \frac{|S_{21}|}{|S_{12}|}$$

Unilateral power gain - The power gain of a transistor amplifier when lossless feedback has been used to neutralize the reverse transfer coefficient (S12) to zero; the input reflection coefficient (S11) has been matched to zero with lossless circuit elements; and the output reflection coefficient has been matched to zero with lossless circuit elements. The unilateral power gain is the highest power gain which can be achieved from the transistor, and the frequency where this gain is zero dB is f_{max} [10].

3-3 F_t and F_{max}

Two parameters often used to characterize devices are F_t and F_{max}. These quantities represent the unity gain intercept point of the short circuit current gain (h_{21}) and unilateral power gain, respectively. Table 3-2 lists the y and h parameters in terms of S-parameters. The unity short-circuit current gain frequency (F_t) is defined to be a frequency at which h_{21} becomes equal to 0 dB. In addition, F_t is also measured by extrapolating $|h_{21}|$ to unity gain with 20dB/decade slope as shown in Figure 3-5.

The maximum frequency of oscillation, *fmax*, is the frequency at which a curve of unilateral power gain (U) vs. frequency intercepts zero dB gain as shown in Figure 3-5. The unilateral power gain of HEMT transistors decay at a slope of approximately 20dB/decade. If gain is measured at convenient frequencies between 2 and 12 GHz the points will approximately fit a straight line curve when gain in dB is plotted on a

linear vertical scale against frequency plotted on a log scale horizontally [10]. The frequency at which the unilateral power gain extrapolates to 0 dB gain is $f_{max.}$

3-4 Noise Figure

Modern wireless receiver needs to deal with very weak signals, but the noise added by the system components tends to obscure those very weak signals. Sensitivity, bit error ratio (BER) and noise figure are system parameters that characterize the ability to process low level signals. Of these parameters, noise figure is not only for characterizing the entire system but also the system components such as the pre-amplifier, mixer, and IF amplifier that make up the system. Noise figure is often the key parameter that differentiates one system from another, one amplifier from another and one transistor from another [10].

The reason for measuring noise properties of the networks is to minimize the problem of noise generated in receiving systems. One approach to overcome noise is to make the weak signal stronger. This can be accomplished by raising the signal power transmitted in the direction of the receiver, or by increasing the amount of power the receiving antenna intercepts, for example, by increasing the aperture of the receiving antenna. Raising antenna gain, which usually means a larger antenna, and raising the transmitter power, are eventually limited by government regulations,

engineering considerations, or economics. The other approach is to minimize the noise generated within receiver components. Noise measurements are keys to assuring that the added noise is minimal. Once noise joins the signals, receiver components can no longer distinguish noise in the signal frequency band from legitimate signal fluctuations. The signal and noise get processed together. Subsequently raising of the signal level with gain, for example, will raise the noise level an equal amount. Figure 3-6 shows a generalized block diagram of a typical noise figure setup used to obtain noise parameters [10].

Today, conventional AlGaAs/InGaAs HEMTs have demonstrated unprecedented noise performance at cryogenic temperatures, good microwave and millimeter-wave noise performance at room temperature at frequencies up to 60 GHz, and very high gate-switching speeds in digital circuits. The minimum noise figure of a HEMT can be expressed as:

$$F_{\min}(dB) = 10\log(1 + kfC_{gs}\sqrt{\frac{R_g + R_s}{g_m}})$$

Where F_{min} is the minimum noise figure, k is the Fukui constant, F is frequency, C_{gs} is input gate capacitance, and R_g and R_s are the gate and source resistances, respectively. For superior low-noise performance, the device must have low Fukui constant, high transconductance, and low parasitic gate resistance, source resistance, and capacitance.

The HEMTs have consistently demonstrated 0.5-1 dB lower noise figure over the millimeter wave range. The major reasons for the better noise performance of HEMTs than MESFETs are higher sheet carrier density, electron mobility, and velocity in the undoped GaAs channel for lower parasitic source resistance and higher transconductance. It is important to note that the HEMT has a smaller Fukui constant than the MESFET due to the thinner doping layer.

In addition to the low noise figure, HEMTs also have several characteristics that make them more attractive for low noise applications. The HEMTs exhibits lower $|S_{22}|$ and higher $|S_{21}|$ value than MESFETs at the same size. Over all, the HEMTs provide a better output impedance match, larger gain-bandwidth product and lower noise conductance. Figure 3-7 shows noise performance of 0.25μm D-mode PHEMT. Device minimum noise figures range from 0.31dB at 2 GHz to 0.89 at 18 GHz. With proper design and fabrication, it is possible to obtain the minimum noise figure close to the maximum g_m point in the HEMT for a high associated gain. Associated gain is the available gain of a device when the source reflection coefficient is the optimum reflection coefficient G_{opt} corresponding with F_{min}. Hence, noise figure measurements are often accompanied by associated gain, the gain achieved at that impedance match. It also has been found that the noise figure of HEMT is less sensitive to the drain current variations, as shown in Figure 3-8.

3-5 Power and Power added efficiency

All previous discussion such likes, S-parameter and noise, has centered on measurements normally made at small signal condition. One direct large-signal measurement technique designed to characterize device properties is the load pull measurement. The measurement system simultaneously monitors the tuned impedance of the performance of the device. Device response is then recorded under the variable load conditions. The resulting loci of impedances required to obtain a constant performance parameter (i.e., output power, power added efficiency, etc) are typically displayed on a Smith chart in the form of closed contours. The load-pull contours are determined for one frequency at a time, as show in Figure 3-9. Figure 3-10 illustrates a typical equipment configuration that can be used to realize a traditional load-pull system. When amplifier is operating well within its linear region and it is in which an increase in input power results in an equal increase in output power. However, the output power will begin to “saturate”, as show in Figure 3-11. Power performance is often characterized by quoting the gain at one dB departure from linear gain [1]. As in all other RF measurements, power gain is dependent on input and output impedance matching.

Another quantity used to characterize power performance of the amplifiers is the efficiency. There are two kinds of efficiency which we will consider here. The

conversion efficiency (drain efficiency) is the RF output power divided by the input dc power to the DUT. This measures how well the device converts dc into RF power. For class-A operation under sinusoidal input signals, the maximum theoretical conversion efficiency is 50%; for class-B, it is 78.5%. For square waves, efficiency can approach 100% in both cases [1].

Conversion efficiency is not the most commonly quoted efficiency in GaAs applications. More commonly used in GaAs applications is power added efficiency. This is the RF power that is added to the input power, divided by the average dc power supplied to the DUT. The power added efficiency can be characterized as follows:

$$\textit{Power added efficiency} = (P_{out} - P_{in})/IV$$

Where P_{out} and P_{in} are the input and output power, and I and V are drain current and voltage. Efficiency is also a function of impedance match and DC bias. The impedance match between the circuit and the source or load is critical in determining performance. Ideally, the source and load impedance are known, and appropriate matching networks are used to optimize the desired performance.

To provide power amplification at high frequencies, high gain of the device is necessary, because under large-signal conditions the gain will be reduced to the small signal value due to gain compression and an output matching which provides the

appropriate impedance for output power, rather than gain [3]. High gain is realized by employing short gate length, resulting in higher transconductance and reduced input capacitance, and by using thin, high carrier density channels within which carrier flow is confined and efficiently modulated by the gate. There is a trade-off between maximum efficiency and power density: maximum efficiency is a direct consequence of high gain (short gate length, high doping, and thin channel), while maximum power arises from a high breakdown voltage and high drain current [11]. In addition, a good power transistor should have low knee voltage, high current density, high breakdown voltage, low gate leakage current, high transconductance and good gain linearity [3].

1. Available Power Gain = $\dfrac{\text{Power Available from Network}}{\text{Power Available from Generator}}$

$$G_A = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{(1-|S_{22}|^2) + |\Gamma_S|^2(|S_{11}|^2 - |D|^2 - 2\,\mathrm{Re}\,(\Gamma_S C_1)}$$

2. Stability

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|}$$

3. Maximum Stable Gain

$$G_{msg} = \left| \frac{S_{21}}{S_{12}} \right|$$

4. Maximum Available Gain (for K>1)

$$G_{max} = \left| \frac{S_{21}}{S_{12}} (K \pm \sqrt{K^2 - 1}) \right|$$

5. Maximum Unilateral Power Gain

$$U = \frac{|S_{21}|^2}{(1 - |S_{11}|)^2 (1 - |S_{22}|)^2}$$

6. Source and Load Match for Maximum Available Power Gain

$$\Gamma_{ms} = C_1^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2|C_1|^2} \right]$$

$$\Gamma_{mL} = C_2^* \left[\frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2|C_2|^2} \right]$$

Use minus sign when B_1 or B_2 is positive, plus sign when B_1 or B_2 is negative.

where:

$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |D|^2$

$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |D|^2$

$C_1 = S_{11} - D(S_{22}^*)$

$C_2 = S_{22} - D(S_{11}^*)$

$D = \det [s] = S_{11} S_{22} - S_{12} S_{21}$

Table 3-1 The most frequency used RF parameters for device characterization

$$y_{11} = \frac{S_{12}S_{21} + (1 - S_{11})(1 + S_{22})}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} Z_o^{-1}$$

$$y_{22} = \frac{S_{21}S_{12} + (1 + S_{11})(1 + S_{22})}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Z_o^{-1}$$

$$h_{11} = \frac{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} Z_o$$

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$h_{12} = \frac{+2S_{12}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

$$h_{22} = \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} Z_o^{-1}$$

Table 3-2 The y and h parameters in terms of the S-parameters[10]

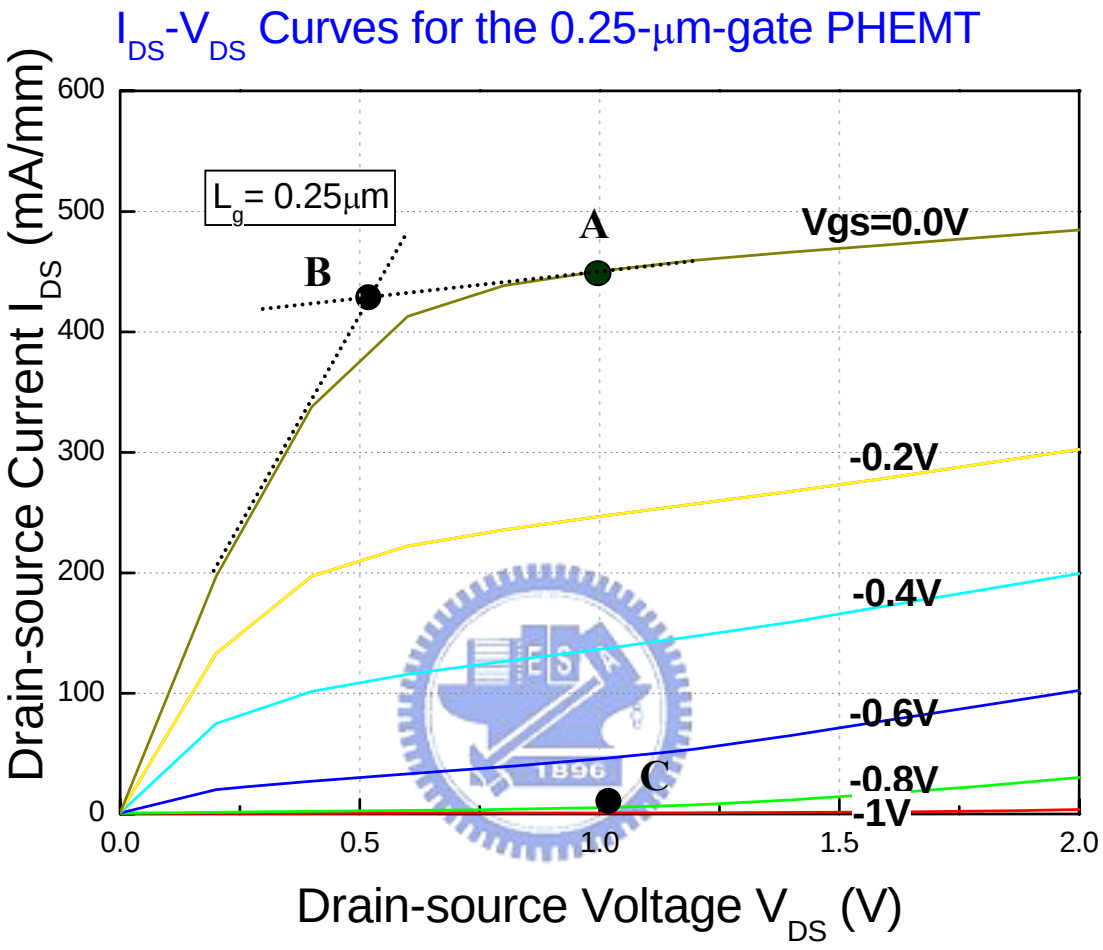


Figure 3-1 Current-Voltage characteristics of the 0.25 μm × 160μm D-mode AlGaAs/InGaAs PHEMT .

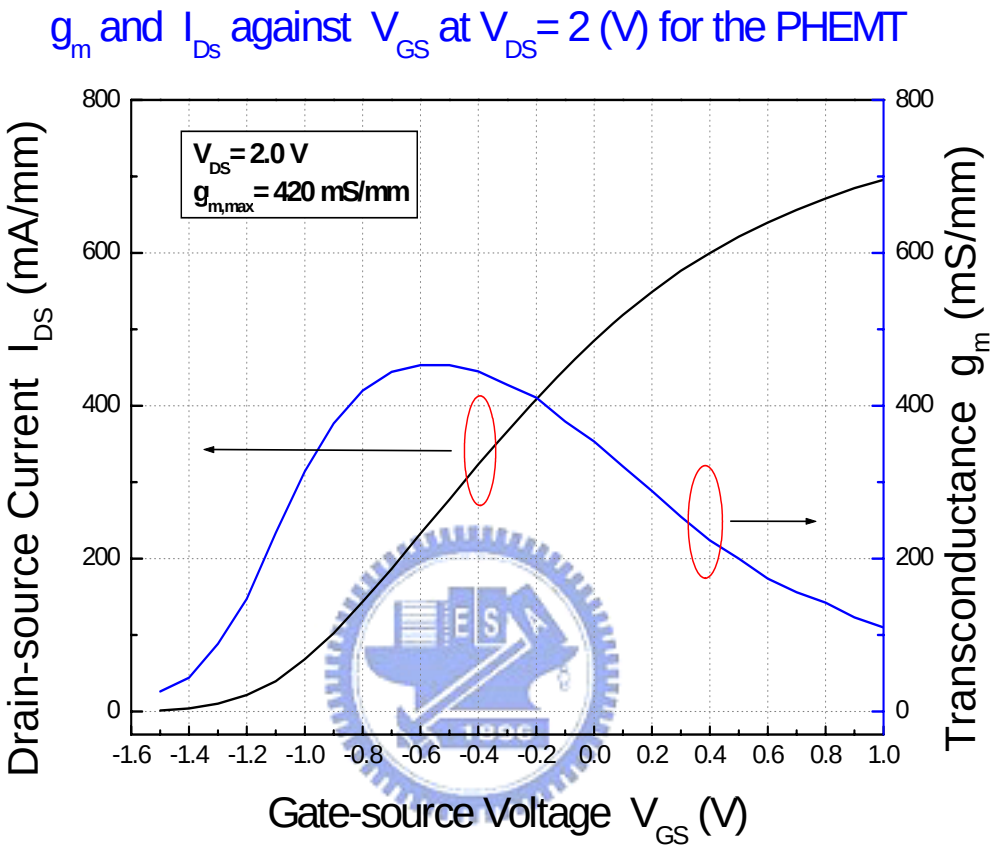


Figure 3-2. Transconductance and drain-source current vs. V_{GS} of the 0.5 μm × 160μm D-mode PHEMT.

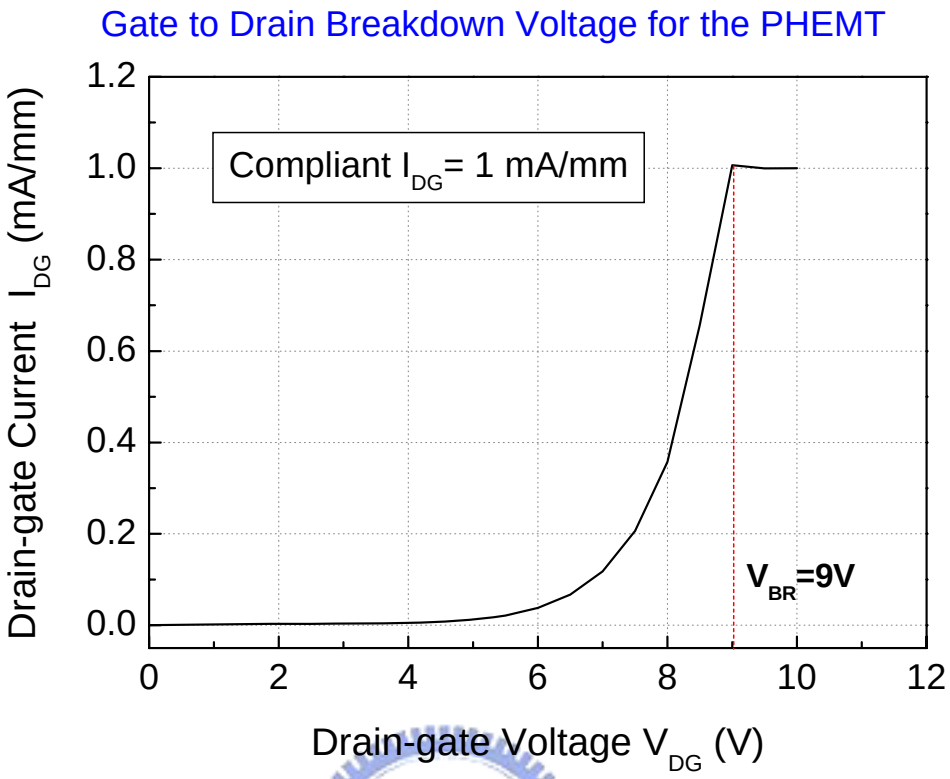


Figure 3-3 Gate-to-drain breakdown voltage. Specifying the gate-to-drain current is 1mA/mm.

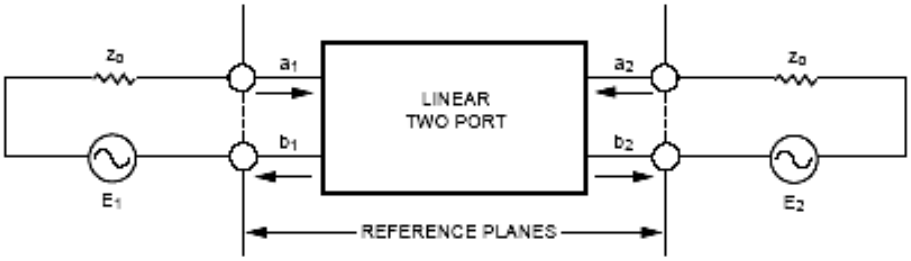


Figure 3-4 S-parameters definition Schematic[10]

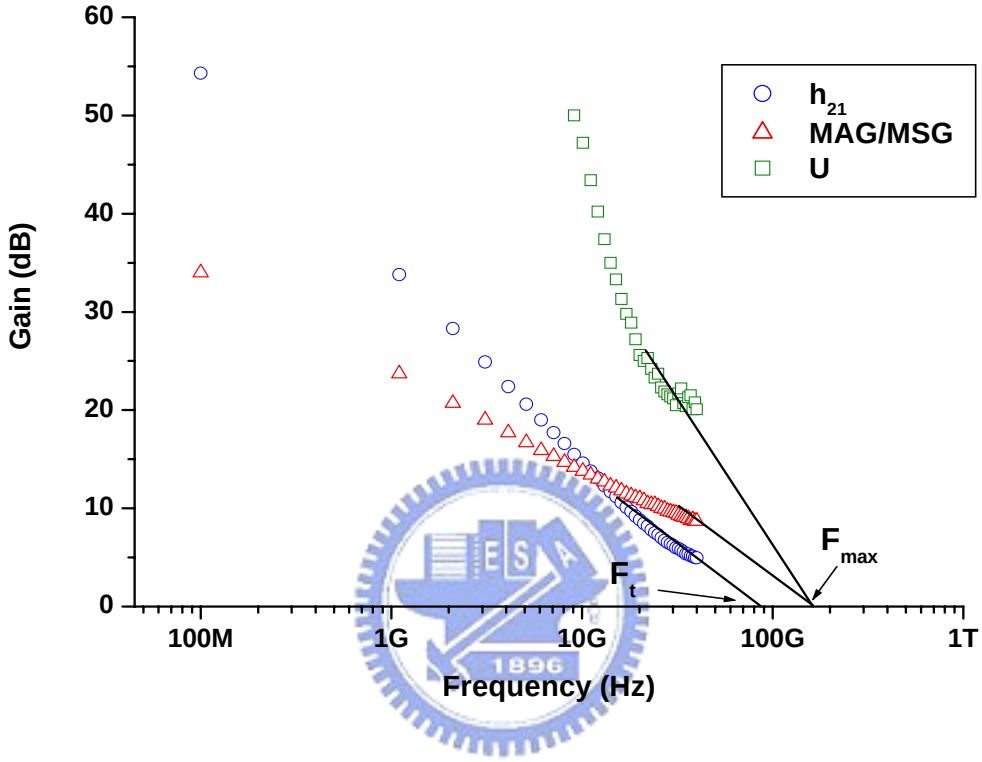


Figure 3-5 **Typical H_{21}, MAG/MSG and U as a function of the frequency for the 0.25μm × 160μm D-mode PHEMT when biased at V_{DS} = 2V and V_{GS} = -0.5V**

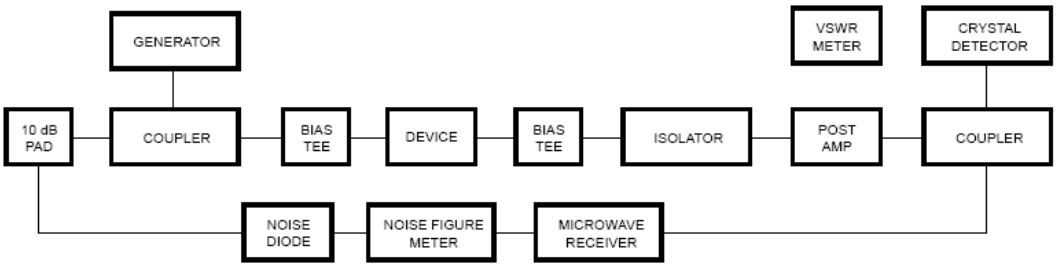


Figure 3-6 A generalized block diagram of a typical noise figure setup used to obtain noise parameters [10].

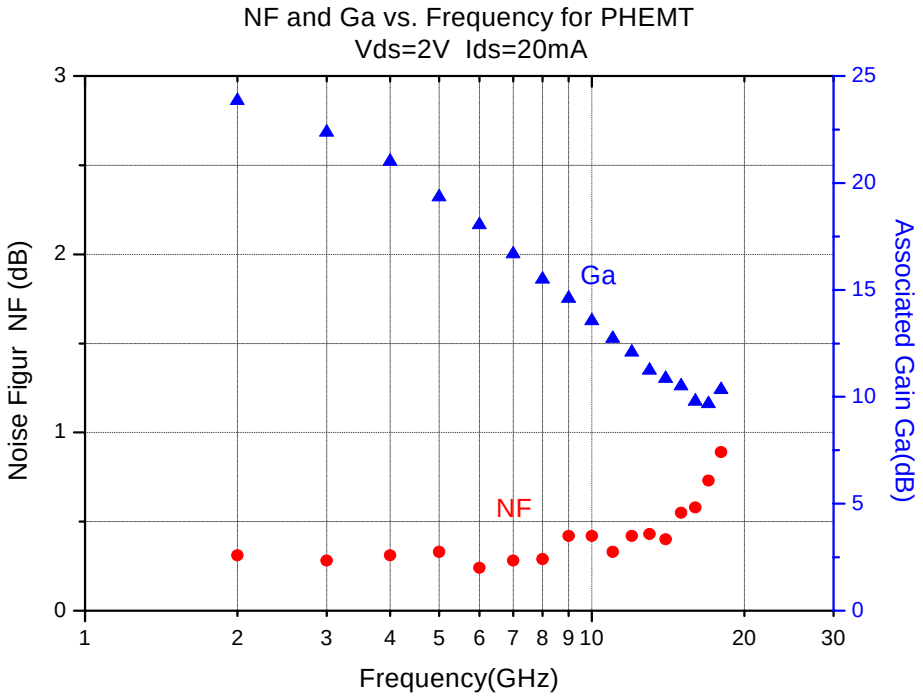


Figure 3-7 Noise performance of a 0.25μm D-mode PHEMT

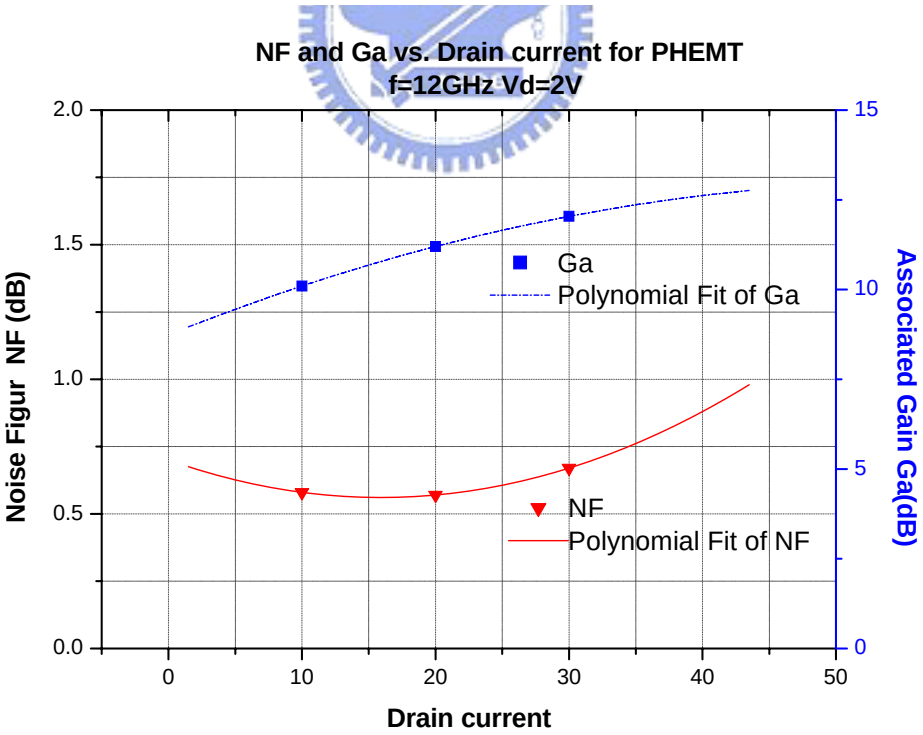


Figure 3-8 NF and Associated gain vs. Drain current for the PHEMT

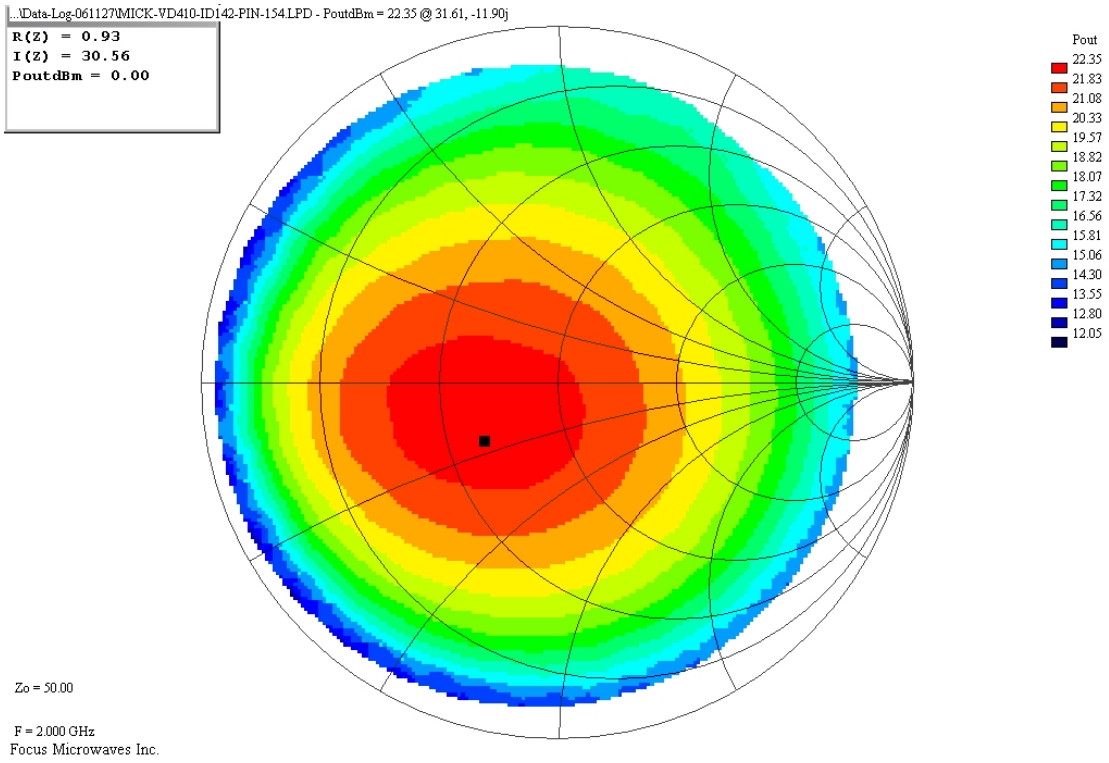


Figure 3-9 The power contours of a 0.25μm D-mode PHEMT.

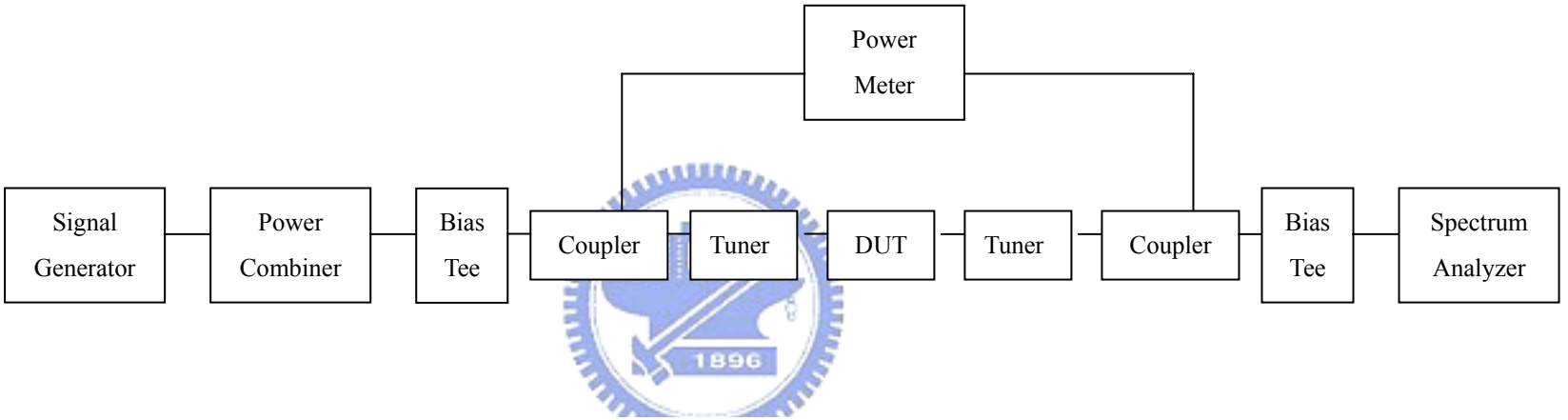


Figure 3-10 Typical test equipment configuration used to make traditional load-pull measurement.

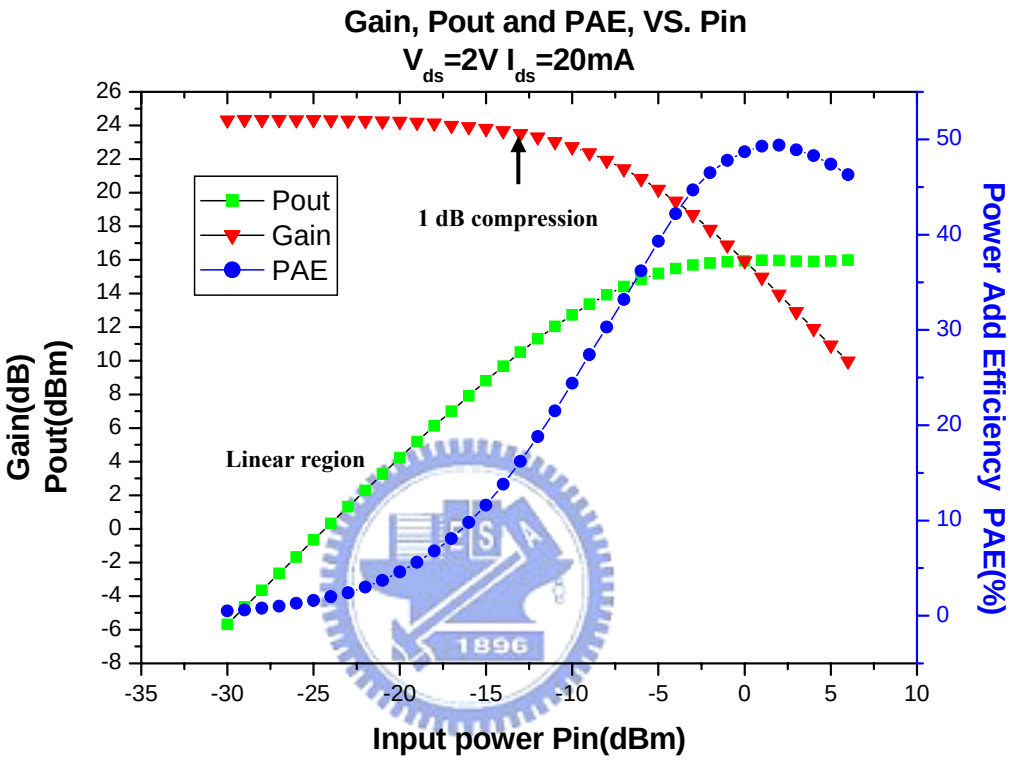


Figure 3-11 Typical power, Gain and Power added efficiency performance of a power HEMT device.

Chapter 4

Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT

4-1 Introduction

For cellular phone applications, microwave devices require high power-added efficiency (PAE) and high output power operated at low DC power supply [12]. Enhancement-mode Pseudomorphic high electron mobility transistors (E-mode PHEMTs) are suitable for cellular phone applications due to single voltage supply operation and low knee voltage characteristic. These advantages can reduce the DC power consumption, improve the efficiency, and increase the operation time. In the past few years, many reports on the enhancement-mode AlGaAs/InGaAs PHEMTs have quoted high power density and high PAE at low voltage operation [13]-[15].

Recently, the use of InGaP instead of AlGaAs in the device structure has become very popular [16] [17] [18] because the InGaP/InGaAs PHEMTs have many advantages over the AlGaAs/InGaAs PHEMTs. These advantages include excellent etching selectivity between InGaP and GaAs, it increases the device manufacturability; moreover high energy band-gap of InGaP results in low microwave noise and reduces the Gunn oscillation effects [16]. In addition, InGaP does not form DX-center, and causes less deep level defects ,the DX center has great potential to improve the

reliability of the PHEMTs [16] [19].

In this study, InGaP/AlGaAs/InGaAs PHEMTs were developed to further enhance the device performance. The attempt to use InGaP/AlGaAs/InGaAs heterojunction instead of InGaP/InGaAs is due to: Firstly, the conduction band discontinuity of the AlGaAs/InGaAs interface is greater than the InGaP/InGaAs interface [20], the carrier confinement is better, which will improve the output power performance of the InGaP PHEMTs. Secondly, an $In_yGa_{1-y}P_xAs_{1-x}$ layer exists in the InGaP/InGaAs or InGaP/GaAs interface due to the intermixing behavior of As and P atoms during the growth [21][22] as illustrated in Figure 4-1. The InGaP-on-GaAs interface has two distinct components. The first one is the small amount of P in GaAs and of As at the surface of InGaP due to the segregation of As atoms through InGaP during the growth. The second one is the large amount of As in InGaP. The origin of this interface broadening could be driven by the chemical bond strength difference between Ga–P and Ga–As. However, the intermixing of P and As atoms for the InGaP-on-GaAs interface is not sufficient to explain the large amount of As in InGaP. The main part of As atoms in InGaP is then probably due to a gas mixture during the gas commutation procedure [23]. The formation of a parasitic well in the interface reduced the electron mobility due to the trapping effect of the transferred electrons in the parasitic well [23]. Table 3-1 summarizes the 2DEG sheet carrier concentration

and mobility for the PHEMT structure. As a result, the Hall mobility of the InGaP/AlGaAs/InGaAs PHEMTs is higher than the InGaP/InGaAs PHEMTs [24]. In this study, the electron mobility of the InGaP/AlGaAs/InGaAs structure is 6410 cm^2/Vs at room temperature as illustrated in Table 3-2.

4-2 Device structure and Fabrication

The E-mode InGaP/AlGaAs/InGaAs PHEMT structure was grown by the MOCVD method on a 4 inch GaAs substrate. The device structure was composed of, from bottom to top, 2500Å GaAs buffer layer , 2200Å GaAs/AlGaAs super-lattice, 200Å $Al_{0.24}Ga_{0.76}As$ layer, followed by undoped 30Å $Al_{0.24}Ga_{0.76}As$ spacer, lower Si δ-doped layer, 100Å $In_{0.2}Ga_{0.8}As$ channel, 30Å $Al_{0.24}Ga_{0.76}As$ spacer, upper Si δ-doped layer, 120Å undoped $In_{0.49}Ga_{0.51}P$ layer and 700Å heavily doped n^+ GaAs cap layer. The epi-structure of the device is as shown in Figure 4-2. The $In_{0.49}Ga_{0.51}P$ layer was used as the Schottky layer, and the InGaP layer also achieved a high etching selectivity with the GaAs layer during the cap layer etching process. The mesa isolation was done by wet chemical etching. Ohmic contacts were formed by evaporating Au/Ge/Ni/Au on n^+ GaAs layer and then alloyed at 350°C using RTA (Rapid Thermal Annealing). The contact resistance measured by the transmission line model (TLM) method was 1×10^{-6} Ω-cm^2. For T-gate definition, the bi-layer resist

structure consisting of PMMA (polymethylmethacrylate) and P (MMA-MAA) (polymethyl methacrylate-methacrylic) were exposed by E-beam lithography (Leica EBML300) with footprint of 0.5 μm. Citrate acid/H_2O/H_2O_2 solution were used for gate recess process, and the recess was stopped at the InGaP layer. Then, gate metals Ti/Pt/Au (100/100/300 nm) were deposited sequentially as the Schottky metal of the T-shaped gate. After T-gate formation, 100-nm-thick silicon nitride film was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer. Finally, 2 μm thick Au plated air-bridges were formed for multi-finger device interconnections.

4-3 DC Characteristics

The I-V characteristics of the fabricated 0.5 × 160 μm^2 E-mode InGaP/AlGaAs/InGaAs PHEMTs as shown in Figure 4-3. The drain-to-source current (I_{ds}) was 375 mA/mm at V_{GS}=0.8V and a low knee voltage of 0.3V. The device has a threshold voltage (V_{th}) of 0.14V with small standard deviation of 30mV across the 4 inch wafer. The threshold voltage is defined as V_{GS} when the I_{DS} is 1mA/mm.The high threshold voltage uniformity of the E-mode PHEMT was due to the high etching selectivity between InGaP and GaAs layer. The maximum transconductance measured at V_{DS} =2.5V was 550mS/mm, as shown in Figure 4-4. The drain-to-gate breakdown

voltage (V_{BK}) was 10V, which was defined at a gate current of 1mA/mm, as shown in Figure 4-5. The uniformity of the threshold voltage (Vth) across the 4 inch wafer was shown in Figure 4-6.The E-mode PHEMT demonstrated small standard deviation of 30mV. The high uniformity of the E-mode PHEMT was due to the high etching selectivity between InGaP and GaAs layer.

4-4 RF Performance

For RF performance, the S parameters of the E-mode PHEMTs were measured by on-wafer testing from 1 to 35GHz .The current gain (H_{21}) and the maximum available gain/maximum stable gain (MAG/MSG) as a function of frequency are shown in Figure 4-7. The calculated f_T and f_{max} of the E-mode PHEMT measured at the V_{DS}=2.5V and V_{GS}=0.5V were 60 GHz and 128 GHz, respectively, by a -20dB/decade slope extrapolation. The outstanding RF performance of the Enhancement-mode device is due to the use of InGaP/AlGaAs/InGaAs heterojunction which produce high electron mobility in the channel region. Figure 4-8 illustrated the measured minimum noise figure (F_{min}) was 1.13dB with 10.35dB associated gain at 17GHz under V_{DS}=2V and V_{GS}=0.3V.

4-5 Power Performance

The power performance measurement was also performed by an ATN load-pull system. The power performances of the 0.5×160μm^2 devices measured at 2.4GHz are shown in Figure 4-9 (a). When tuned for maximum power-added efficiency (PAE) match, the output power (P_{out}) was 10.88dBm and the maximum PAE was 70%, when the DC bias condition was V_{DS}=2V, V_{GS}=0.2V. If the device was biased at V_{DS}=2V, V_{GS}=0.4V and tuned for maximum output power match, the output power (P_{out}) of 18.61dBm (453mW/mm) with 32.5% PAE was obtained and the device had a linear gain of 30.5dB, as shown in Figure 4-9 (b). The power performances of the 0.5×160μm^2 devices measured at 6GHz are illustrated in Figure 4-10. When tuned for maximum power-added efficiency (PAE) match, the output power (P_{out}) was 13.39dBm and the maximum PAE was 63.8%, when the DC bias condition was V_{DS}=2V, V_{GS}=0.2V. If the device was biased at V_{DS}=2V, V_{GS}=0.4V and tuned for maximum output power match, the output power (P_{out}) of 16.2dBm with 52% PAE was obtained and the device had a high linear gain of 25.3dB. Overall, the state-of-the-art, InGaP/AlGaAs/InGaAs E-mode PHEMT is demonstrated with a much lower operating voltage than the reported AlGaAs/InGaAs [12]-[11] and InGaP/InGaAs E-mode PHEMTs[16][21]. The developed E-mode InGaP PHEMT shows excellent DC and RF performance. We believed the improved device performance is the results of the introduction of the InGaP/AlGaAs/InGaAs

heterojunction.

4-6 Summary

A single voltage supply, high frequency and high power density Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT was developed for low-voltage wireless application. The calculated f_T and f_{max} of the E-mode PHEMT were 60 GHz and 128 GHz. The F_{min} at 17GHz was measured to be 1.13dB with 10.35dB associated gain. High power performance was achieved, the E-mode PHEMT exhibited maximum PAE of 70%, and maximum power density of 18.61dBm at 2.4GHz. The excellent threshold voltage uniformity and performance of the E-mode PHEMT were due to the use of InGaP/AlGaAs/InGaAs layer structure which took advantages of high etching electivity between InGaP/GaAs and high electron mobility due to the use of AlGaAs spacer layer.

No.	*Schottky layer (Å)*	*Spacer layer (Å)*	*μ(300K)*	*μ(77K)*	*n2DEG (300K)*	*n2DEG (77K)*
1	AlGaAs 220	AlGaAs 30	6310	24000	2.27	1.69
2	InGaP 120 /AlGaAs 100	AlGaAs 30	6100	20800	2.27	1.96
3	InGaP 220	AlGaAs 30	2330	2680	3.01	2.88
4	InGaP 220	InGaP 30	1700	1790	3.30	3.06

Table 4-1 2DEG sheet carrier concentration and mobility for the PHEMT structure [22]

No.	*Device structure* *Schottky/spacer/channel*	*Layer* *thickness(Å)*	*μ* *(cm2/Vs)*
1	$In_{0.49}Ga_{0.51}P/Al_{0.24}Ga_{0.76}As/\ In_{0.2}Ga_{0.8}As$	120/30/100	6410
2	$In_{0.49}Ga_{0.51}P/In_{0.49}Ga_{0.51}P/\ In_{0.2}Ga_{0.8}As$	120/30/100	4100

Table 4-2 The electron mobility of InGaP/AlGaAs/InGaAs PHEMT and InGaP/InGaAs PHEMT

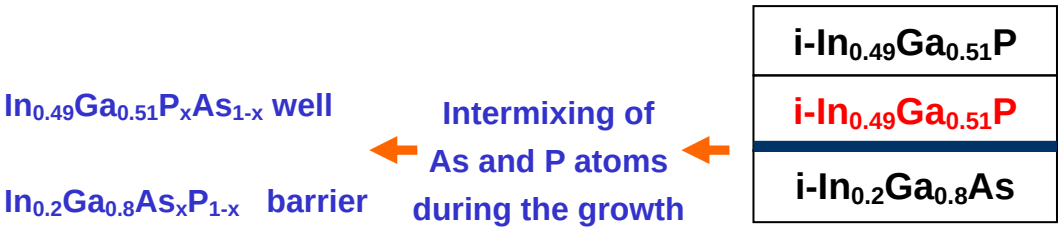


Figure 4-1 Schematic showing the reactions and products between the InGaP/InGaAs layers during the growth.

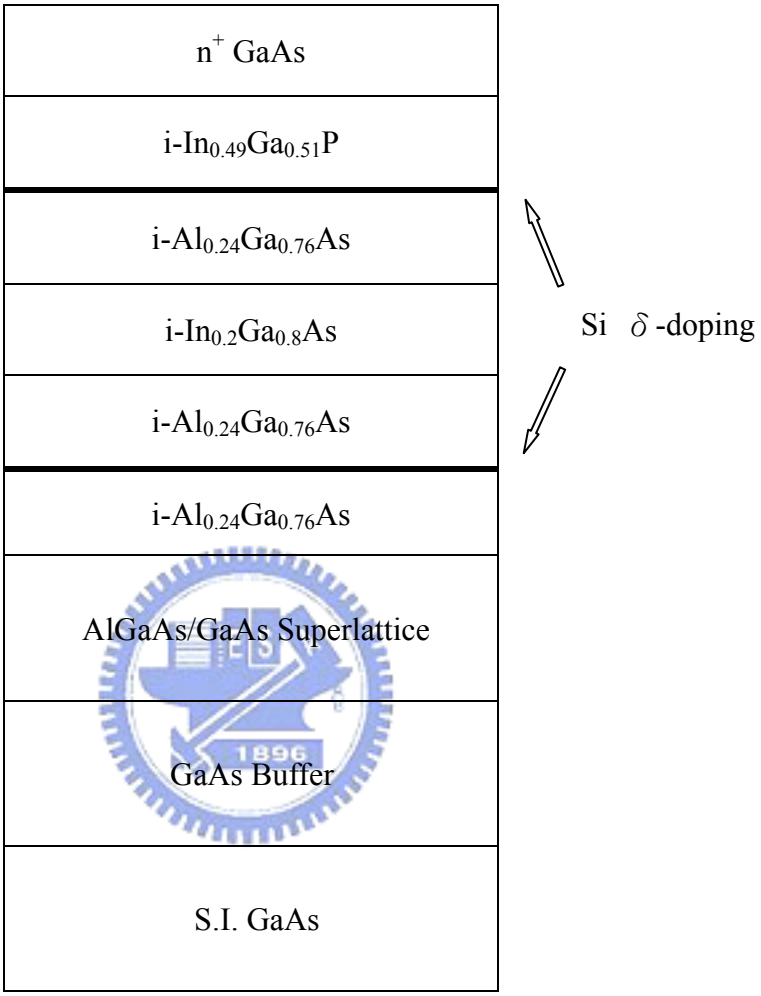


Figure 4-2 Device structure of the Enhancement mode InGaP/AlGaAs/InGaAs PHEMT.

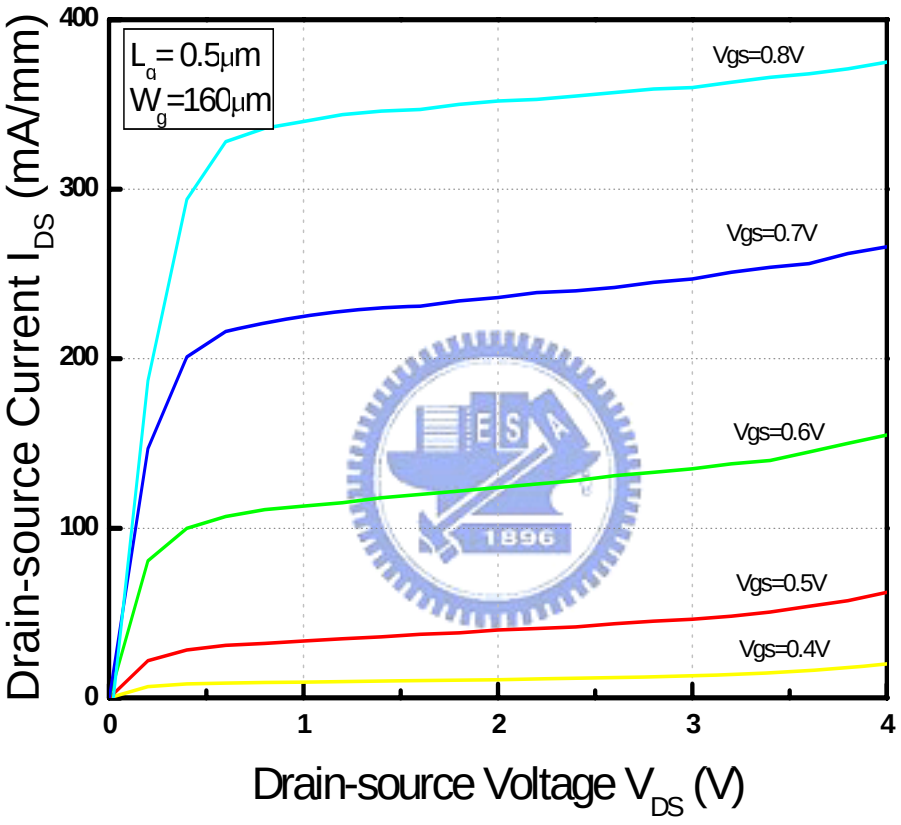


Figure 4-3 I-V characteristics of the 0.5 μm × 160μm E-mode InGaP/AlGaAs/InGaAs PHEMT .

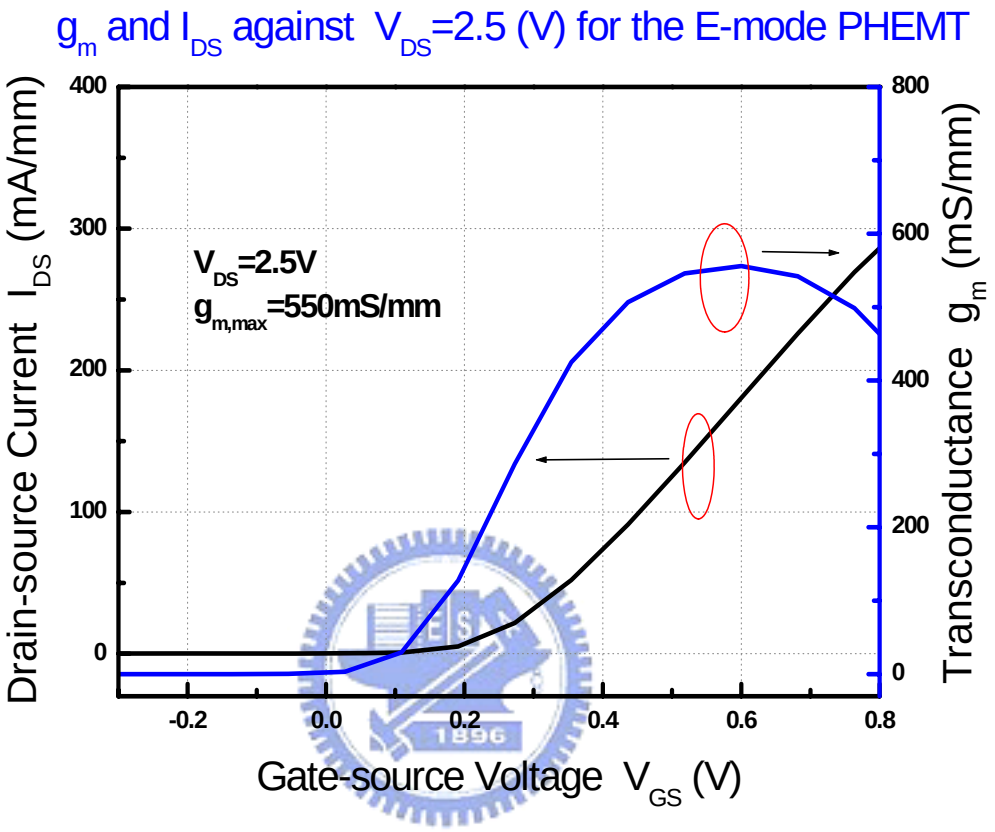


Figure 4-4 Transconductance and drain-source current vs. V_{GS} of the 0.5 μm × 160μm E-mode PHEMT

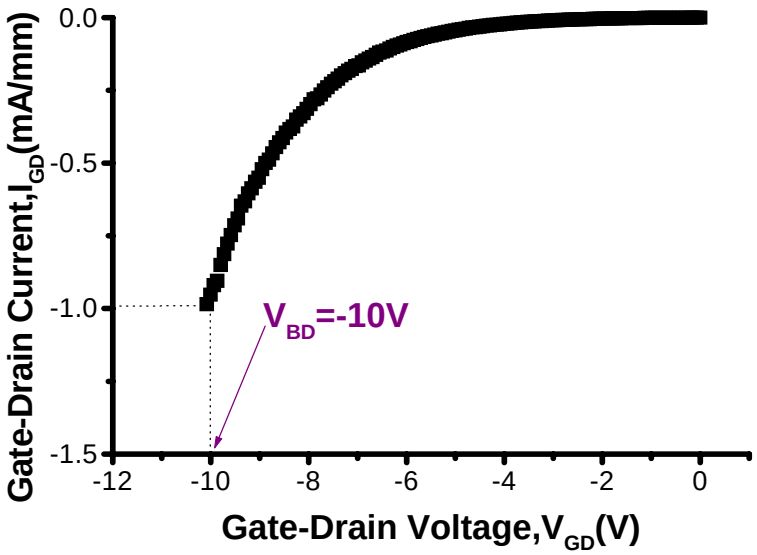


Figure 4-5 The gate-to-drain breakdown voltage of E-mode PHEMT.

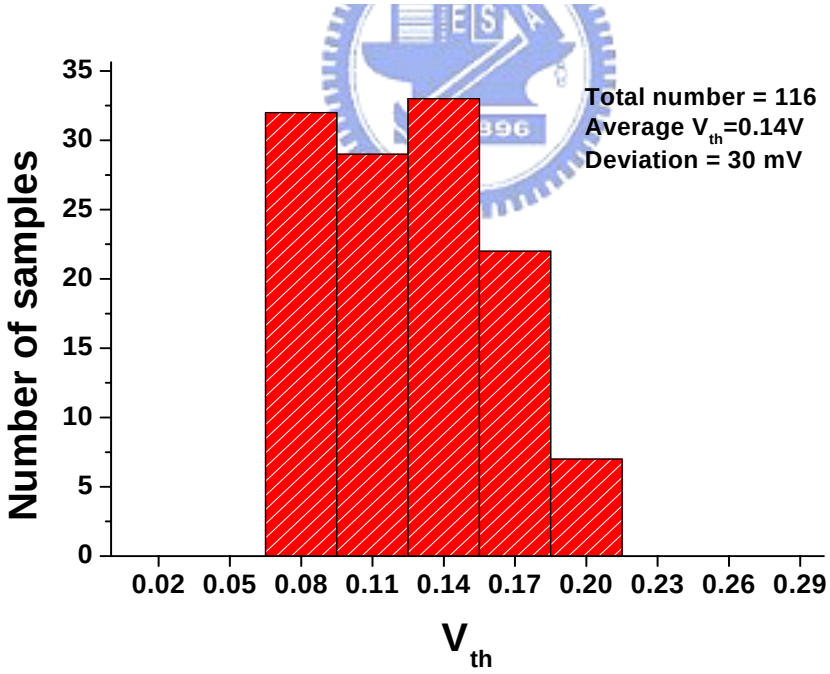


Figure 4-6 Distribution of V_{th} for E-mode PHEMT across 4 inch wafer.

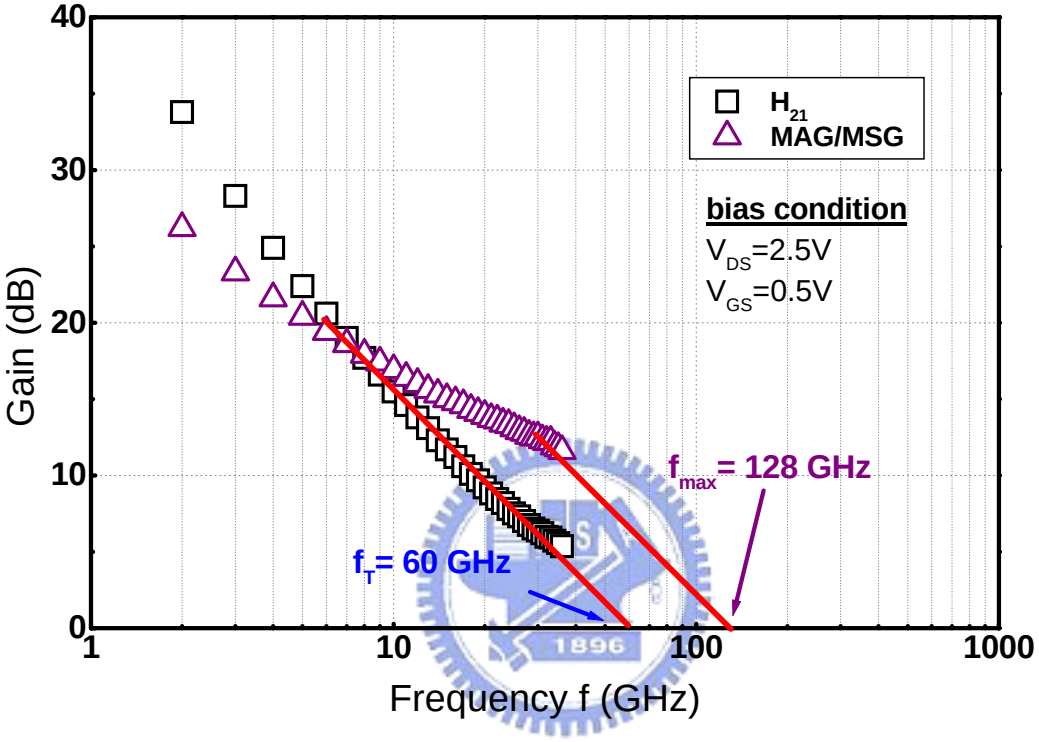


Figure 4-7 **Typical H_{21}, MAG/MSG, as a function of the frequency for the 0.5 μm × 160μm E-mode PHEMT biased at V_{DS} = 2.5V and V_{GS} = 0.5V**

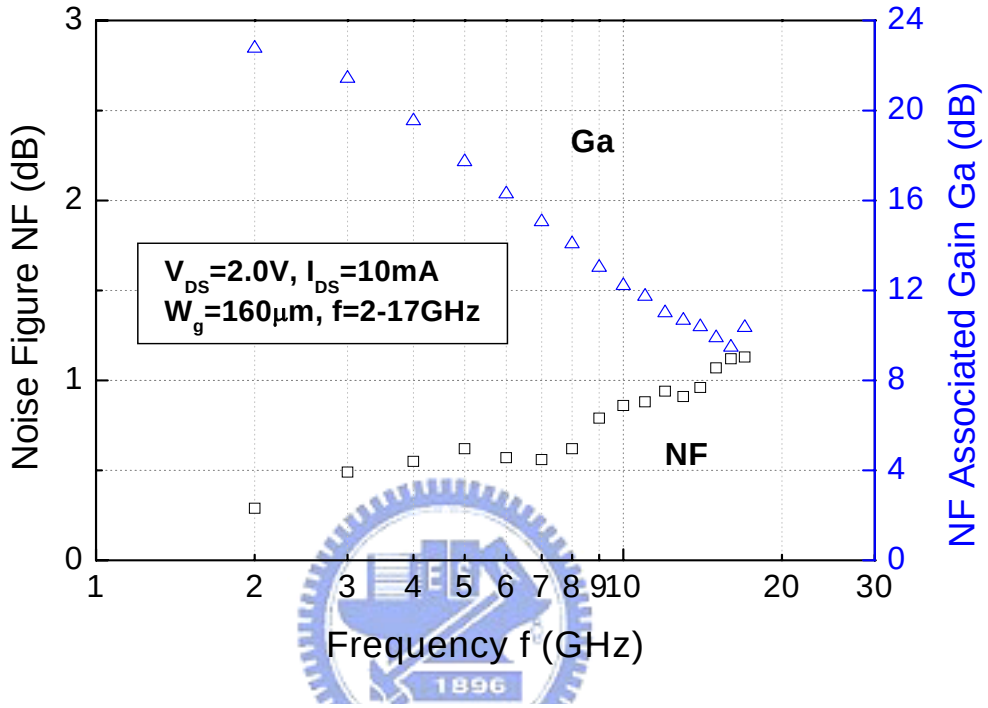
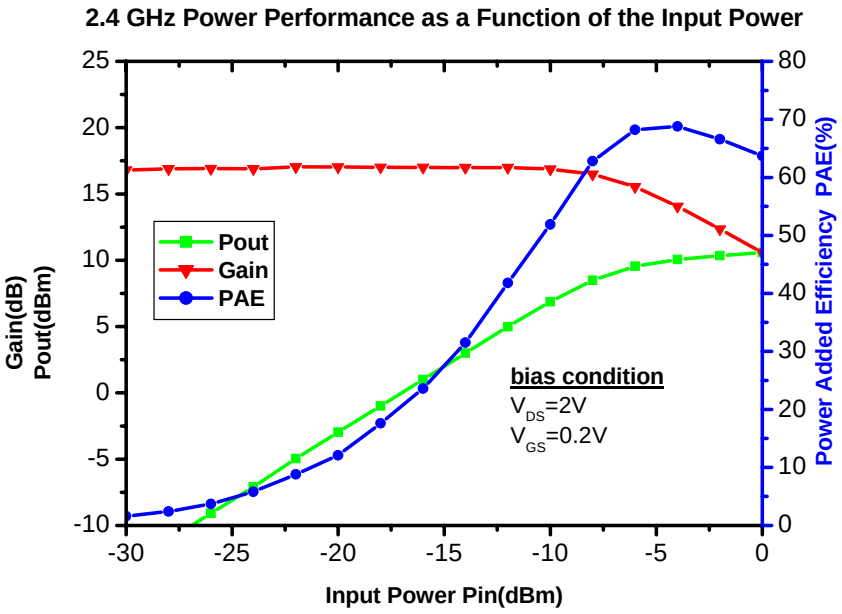
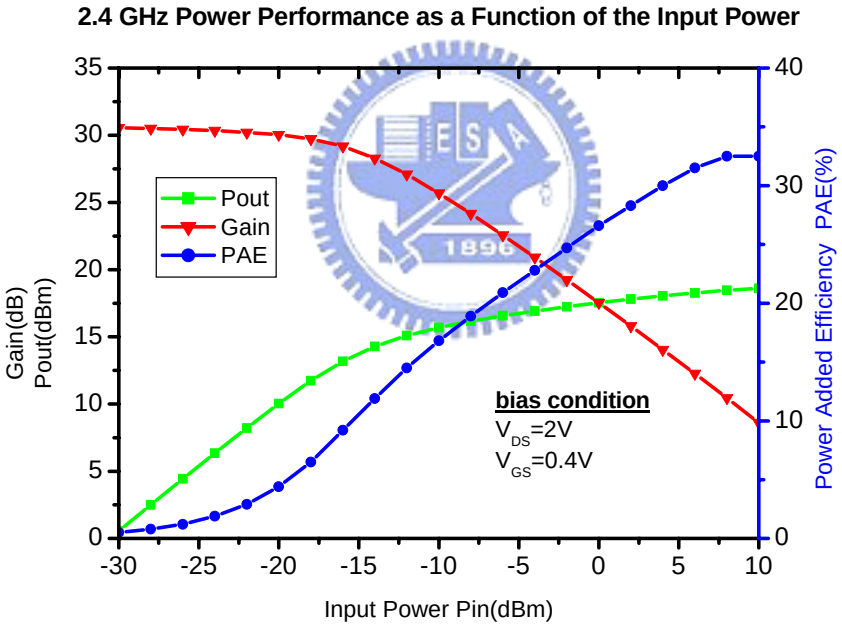


Figure 4-8 Noise Figure and associated gain as a function of frequency at V_{DS} = 2V and I_{DS} = 10 mA of the 0.5 μm × 160 μm E-mode PHEMT

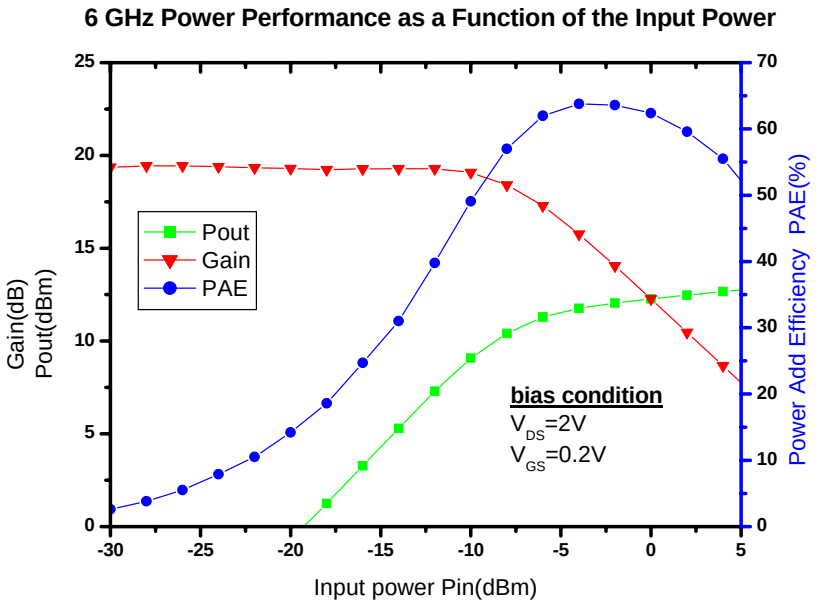


(a)

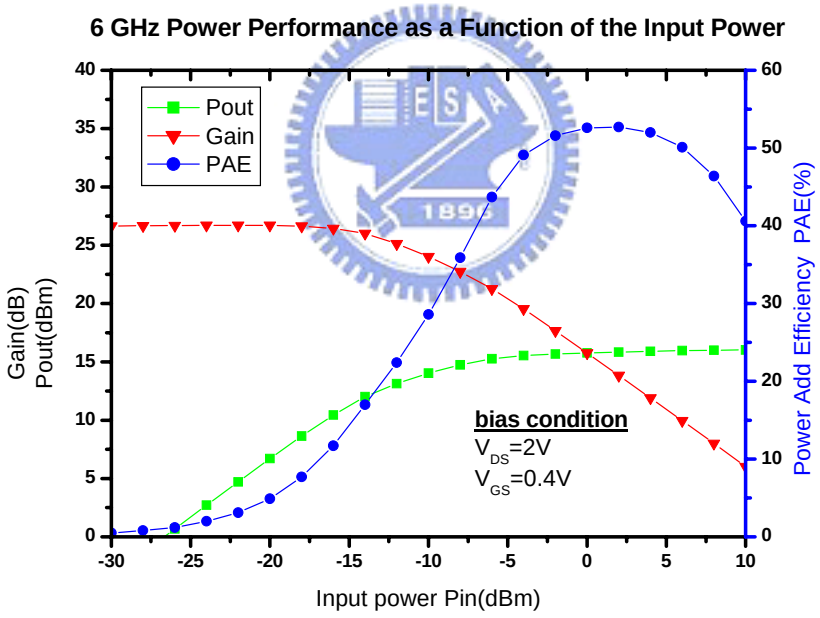


(b)

Figure 4-9 **2.4 GHz power performance as a function of the input power for the 0.5 μm × 160μm E-mode PHEMT. (a) V_{DS}=2V, V_{GS}=0.2V. The device was tuned for maximum power added efficiency.(b) V_{DS}=2V, V_{GS}=0.4V. The device was tuned for maximum output power.**



(a)



(b)

Figure 4-10 6 GHz power performance as a function of the input power for the 0.5 μm × 160μm E-mode PHEMT. (a) V_{DS}=2V, V_{GS}=0.2V. The device was tuned for maximum power added efficiency.(b) V_{DS}=2V, V_{GS}=0.4V. The device was tuned for maximum output power.

Chapter 5

Double δ-Doped Enhancement-Mode Pseudomorphic HEMT for High Linearity Application

5-1 Introduction

Advanced high performance wireless application systems, such as wideband code-division multiple-access (W-CDMA) system, have imposed stringent requirements on the devices including high efficiency and high linearity operation with minimum DC power consumption. The linearity has been an important figure of merit for low noise or power amplifiers to guarantee minimum signal distortion for modern communications systems. Conventional approaches in realizing both high linearity and high efficiency simultaneously involve operating the device at an output power level backed off from P_{1dB} by about 6-10 dB. In that sense, the efficiency at the operating power level usually suffers greatly from the power back-off for linearity considerations which in turn consumes substantial system DC power. Over the years, effort has been devoted to achieving both high linearity and efficiency through complicated circuit design approaches such as controlling supply voltage and implementation of pre-distorters[25]-[27].

Enhancement-mode pseudomorphic high electron mobility transistors (E-mode PHEMTs) are suitable for wireless application systems due to single voltage supply operation and low knee voltage characteristics, along with high efficiency and long standby-time. Two delta-doped layers were used above and below the quantum well region to improve the transconductance flatness of the device[28][29]. The double δ-doped InGaP/AlGaAs/InGaAs PHEMTs was designed to further enhance the Hall mobility as compared to the InGaP/InGaAs PHEMTs[30]. In this chapter, the InGaP/AlGaAs/InGaAs E-mode PHEMTs with double delta-doped of two different doping concentrations were fabricated and characterized, these two doping concentrations were designed for achieving high efficiency and high linearity operating at low voltage supply.

5-2 Device Structure and Fabrication

Two structures, denoted as structure A and B of E-mode InGaP/AlGaAs/InGaAs PHEMTs were grown by molecular beam epitaxy (MBE) on 3 in. GaAs substrates for performance comparison, as shown in Figure 5-1. The only difference between the two structures is the concentration of the upper Si δ-doped. For the structure A, the Si δ-doped concentration was $4.5\times10^{12}cm^{-2}$ and for the structure B it was $3.5\times10^{12}cm^{-2}$. The electron concentration in the two dimensional electron gas electron (2DEG) of

structures A and B were 2.64×10^{12} and $2.20\times10^{12}cm^{-2}$, respectively. The active area of the device was defined by wet chemical etching. Following Au/Ge/Ni/Au Ohmic metals evaporation, the Ohmic contact was formed by Rapid Thermal Annealing at 350 ^{o}C for 1 min. For T-gate formation, the bi-layer resist structure consisting of polymethylmethacrylate (PMMA) and polymethyl methacrylate-methacrylic (P(MMA-MAA))was used and the 0.5 μm gate length was defined by E-beam lithography. Citrate acid/H_2O/H_2O_2 solution was used for gate recess process, and the recess was controlled to stop at the InGaP layer. Then, 0.5 μm-thick Ti/Pt/Au (100/100/300 nm) gate metals were deposited by electron beam evaporator. After gate metal lift-off, 100-nm-thick silicon nitride film was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer. Finally, the 2 -μm-thick Au plated air-bridges were formed as the device interconnections.

5-3 DC and RF Performance

Figure 5-2 shows the transconductance and the drain-source current vs. V_{GS} curves of the $0.5 \times 200\mu m^2$ E-mode PHEMT for the two structures. Structure A shows a more flat transconductance curve than that of structure B, which indicates better linearity of the device. The maximum transconductance of structure A measured at V_{DS} =2.0 V was 448mS/mm, the drain-to-source current (I_{ds}) was 340 mA/mm at

V_{GS}=1 V and the knee voltage was 0.4 V. The drain-to-gate breakdown voltage (V_{BK}) was 12 V, which was defined at a gate current of -1mA/mm.

For RF performance, the S parameters of the E-mode PHEMTs were measured by on-wafer probing system up to 40 GHz. The calculated f_T and f_{max} for structure A were 62 and 94 GHz, respectively, by a -20 dB/decade slope extrapolation. Meanwhile, for structure B, they were 54 and 83 GHz, respectively. The measured minimum noise figure (F_{min}) of structure A was 0.94 dB with 9.42 dB associated gain at 12 GHz under V_{DS}=2 V and V_{GS}=0.24 V, as shown in Figure 5-3

5-4 Third-Order Inter-Modulation Distortion

Intermodulation distortion (IMD) has become increasingly important in microwave and RF circuits design. Unlike harmonic and second order distortion products, third order intermodulation distortion products (IP3) are in-band and cannot be easily filtered. Harmonic distortion can be defined as a single-tone distortion product caused by device non-linearity. When a non-linear device is stimulated by a signal at frequency f1, spurious output signals can be generated at the harmonic frequencies 2f1, 3f1, 4f1,...Nf1. The order of the distortion product is given by the frequency multiplier; for example, the second harmonic is a second order product, and the third harmonic is a third order product, Harmonics are usually measured in dBc, dB below

the carrier (fundamental) output signal as shown in Figure 5- 4[31].

Intermodulation distortion is a multi-tone distortion product that results when two or more signals are present at the input of a non-linear device. All semiconductors inherently exhibit a degree of non-linearity, even those which are biased for “linear” operation. The spurious products which are generated due to the non-linearity of a device are mathematically related to the original input signals. Analysis of several stimulus tones can become very complex so it is a common practice to limit the analysis to two tones. The frequencies of the two-tone intermodulation products can be computed by the equation: M f1 ± N f2, where M, N = 0, 1, 2, 3, .The order of the distortion product is given by the sum of M + N. The second order intermodulation products of two signals at f1 and f2 would occur at f1 + f2, f2 – f1, 2f1 and 2f2, as shown in Figure 5-5. Third order intermodulation products of the two signals, f1 and f2, would be:

2f1 + f2

2f1 – f2

f1 + 2f2

f1 – 2f2

Where 2f1 is the second harmonic of f1 and 2f2 is the second harmonic of f2.This same relationship holds with intermodulation products. The second order product will

increase at a rate of the input signal squared (or twice the rate in dB) and the third order product will increase at a rate of the input signal cubed (or three times the rate in dB). This relationship can be shown by the following:

Type of Intermodulation	**Product Frequency**	**Amplitude**
Second Order:	f1 + f2	$a_2 \bullet A_1 \bullet A_2$
	f1 – f2	$a_2 \bullet A_1 \bullet A_2$
Third Order:	2f1 + f2	$a_3 \bullet A1^2 \bullet A2$
	2f1 – f2	$a_3 \bullet A1^2 \bullet A2$
	f1 + 2f2	$a_3 \bullet A1 \bullet A2^2$
	f1 – 2f2	$a_3 \bullet A1 \bullet A2^2$

Where A1 and A2 are the amplitudes of the two input signals.

Note that the amplitude of the second order intermodulation product is a function of the product of the two input signals. If the amplitudes of A1 and A2 remain equal to each other then the amplitude of the second order products is a function of the product of the two input amplitudes, equivalent to the square of either one. Therefore, if both input signals change by the same amount, then the second order intermodulation product will change by a rate equal to the square of that change. Similarly, the third order intermodulation product is a function of the square of one of the input signals, representing the second harmonic, and the fundamental of the other applied signal. If

both signals are kept at the same level, then the third order intermodulation product will track changes to the applied signals by a rate equal to the cube of the input change [31].

This exponential effect will hold true as long as the device is in the linear region, usually at 10 dB or more below the 1 dB gain compression point. As shown in Figure 5-6, one plots Pout (fundamental) and Pout (third order product) as a function of Pin, the slopes of the curves will be approximately 1:1 and 3:1, respectively, at sufficiently low power where the system is linear. With these disparate slopes, the lines will eventually intersect and the point of intersection is termed the third order intercept point (TOI). The amplitude of Pout (third order) relative to Pout (fundamental) at a given input power level is termed the IMD level [31].

Load-pull measurement was performed for device power performance. Figure 5-7 shows the single tone output power, gain and PAE curves as functions of the input power at 1.95 GHz for the device biased at V_{DS}=2.0V and V_{GS}=0.243V. A maximum PAE of 64% and 12.61 dBm P_{1dB} were observed when the device was tuned for maximum power at $\Gamma_{source} = 0.643 \angle 83.2^{o}$ and $\Gamma_{load} = 0.062 \angle -144^{o}$ .Figure 5-8 shows the measured two-tone output power and third-order inter-modulation distortion (IM3) level vs. input power of structure A. The device was biased at V_{DS}=2 V, I_{DS}=10 mA and tuned for high linearity, the output power at 1 dB gain compression (P_{1dB}) was

10.5 dBm with linear gain of 24 dB and the device had a maximum power added efficiency (PAE) of 52.35% at saturate. Meanwhile, the PAE at P_{1dB} was 40%. Table I summaries the two tone output power performance of the two structures. The higher upper δ-doped device (structure A) exhibited higher linearity characteristics then structure B with output third order intercept point (OIP3) - P_{1dB} of 13.2 dB and linearity figure-of-merit ($OIP3/P_{DC}$) of 11.72, this is due to the flatter transconductance vs. V_{GS} distribution of the device.

5-5 Wideband Code-Division Multiple-Access Power Performance

As the real demand for the receiver applications lies in the linear characteristics of the low noise device, W-CDMA power performance of the 0.5 μm x 200 μm E-mode PHEMT was evaluated using the load pull system with W-CDMA modulation signal as the input. For the case when the device was terminated at the load impedance for maximum power, a 4.74 dB back-off from P_{1dB} (12.1 dBm) was necessary to meet the ACPR specifications of W-CDMA systems, i.e., <-30 dBc at +/- 5 MHz offset and <-40 dBc at +/- 10 MHz offset from the center frequency. The PAE of the device operating under such condition was measured to be 22.45%. To further improve the PAE of the device at linear output power level, the load

impedance was re-optimized to be Γ_{load} = 0.492∠-99.9°. The measured maximum linear output power meeting ACPR specifications at this load was 9.28 dBm (1.25 dB backed-off from P_{1dB}) with 35% PAE achieved which is lower than the previously reported data[27][32][33].

5-6 Summary

A high linearity and low noise Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT was developed for low-voltage operation wireless application. The E-mode PHEMT exhibited 0.94 dB with 9.42 dB associated gain at 12 GHz. The device demonstrated the high linearity characteristics due to the optimal double delta doping structure. The Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT demonstrated only 1.25 dBm back-off from P_{1dB} and achieved excellent linearity with OIP3 - P_{1dB} of 13.2 dB and a high linear power efficiency of 35% when under W-CDMA modulation. The developed Enhancement-mode InGaP/AlGaAs/InGaA PHEMTs with low noise and high OIP3 are of great use for wireless communication applications.

Device type	Gate Width (μm)	VD (V)	ID (mA)	P_{1dB} (dBm)	Gain (dB)	Efficiency (%) at P_{1dB}	OIP3 (dBm) at P_{1dB}	OIP3/P_{DC}
$4.5\times10^{12}cm^{-2}$ (structure A)	200	2	10	10.5	24	40	23.7	11.72
$3.5\times10^{12}cm^{-2}$ (structure B)	200	2	10	9.72	20.6	37	21.8	7.56

Table I Comparison of two tone output power performance for the two different structures

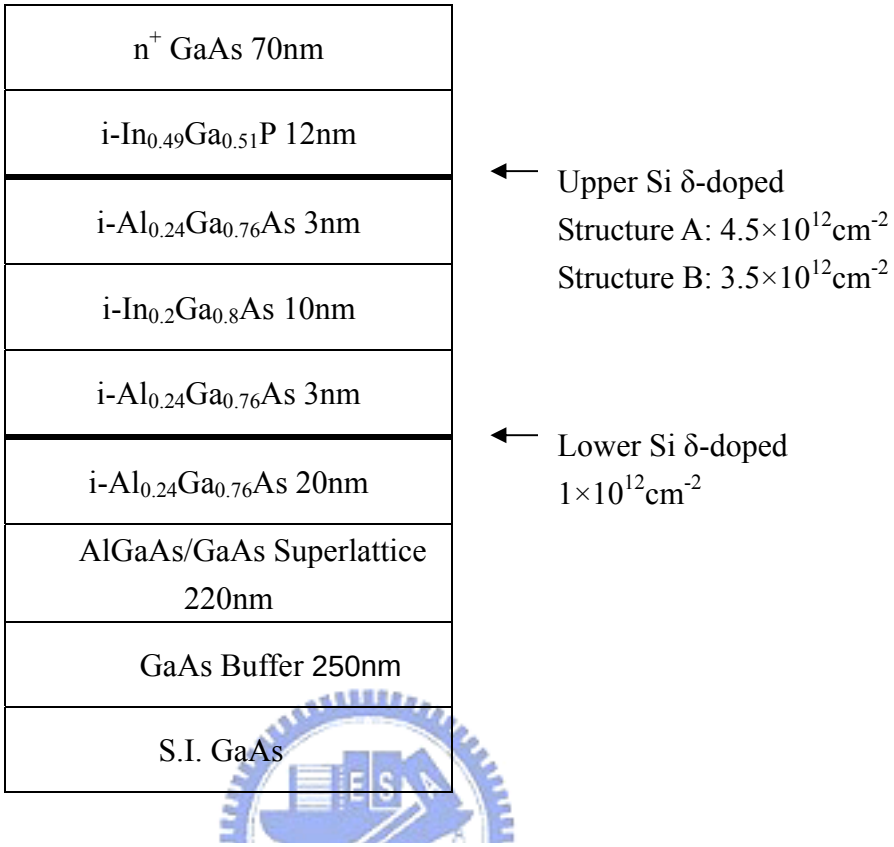


Figure 5-1 The structure of E-mode InGaP/AlGaAs/InGaAs PHEMT. Upper Si δ-doping: $4.5\times10^{12}cm^{-2}$ (structure A) and $3.5\times10^{12}cm^{-2}$ (structure B). Lower Si δ-doping : $1\times10^{12}cm^{-2}$

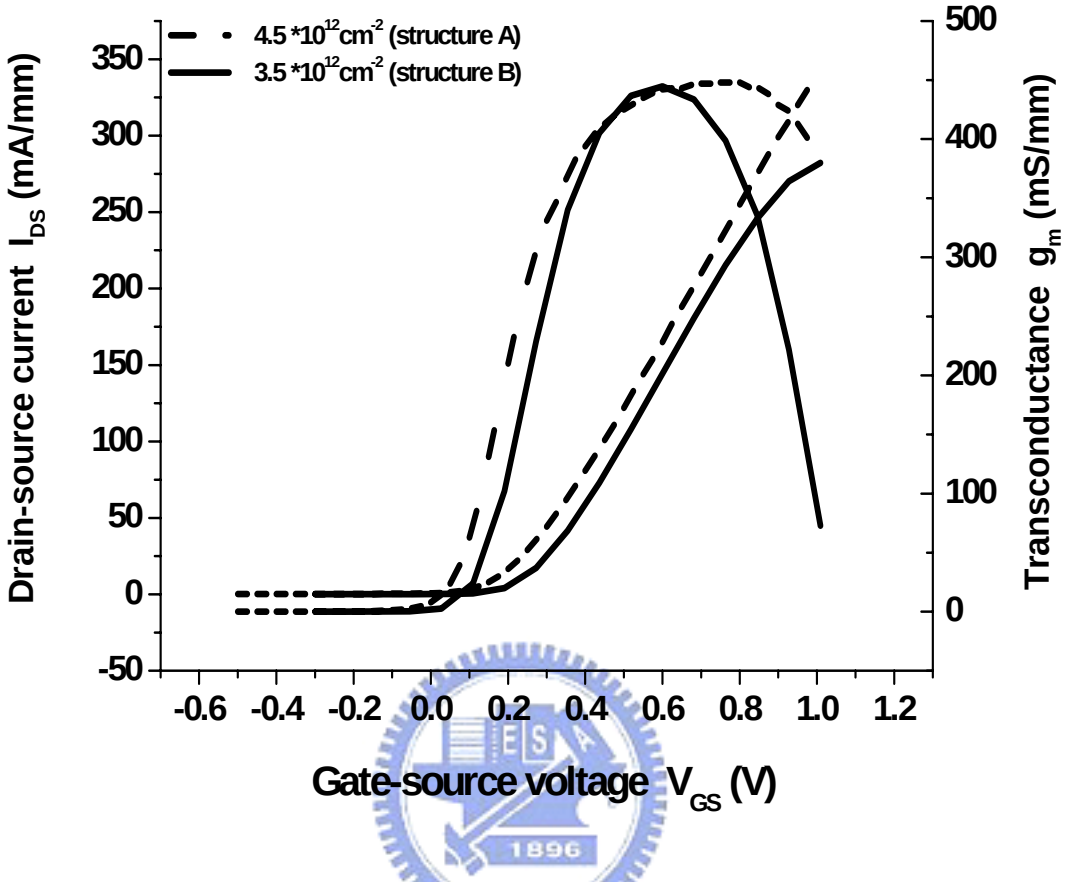


Figure 5-2 Transconductance and drain-source current vs. V_{GS} for the 0.5 × 200 μm^2 E-mode PHEMT.

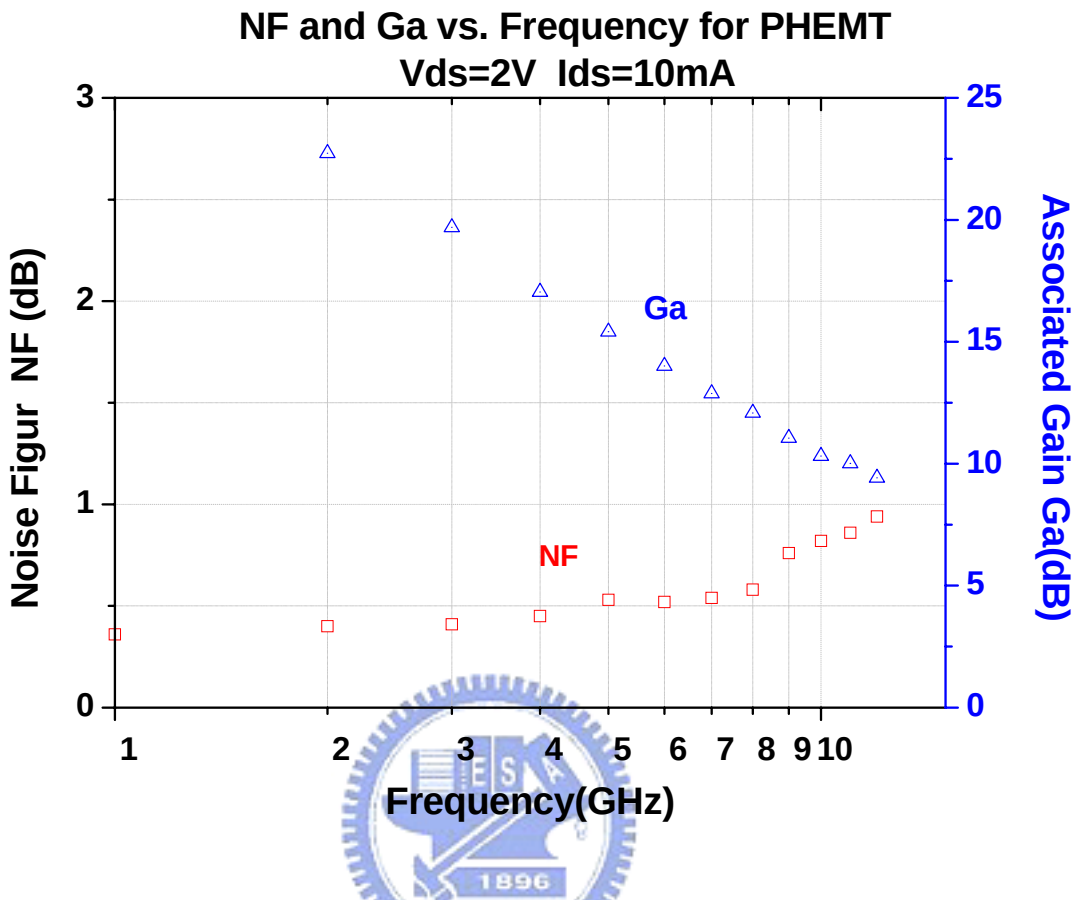


Figure 5-3 Noise Figure and associated gain as a function of frequency at V_{DS} = 2V and I_{DS} = 10 mA of the 0.5 μm × 200 μm E-mode PHEMT.

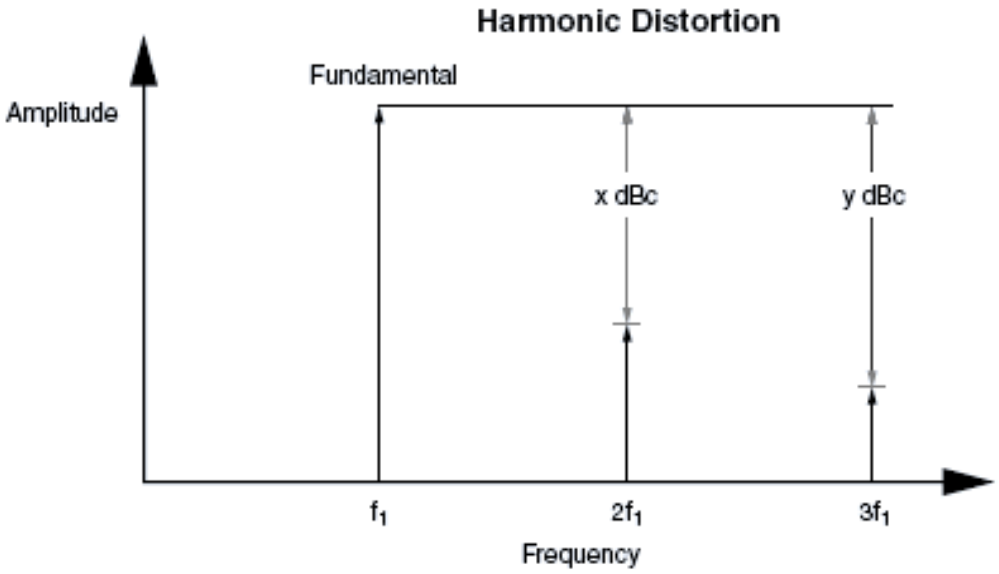


Figure 5-4 The harmonic distortion plot[31]

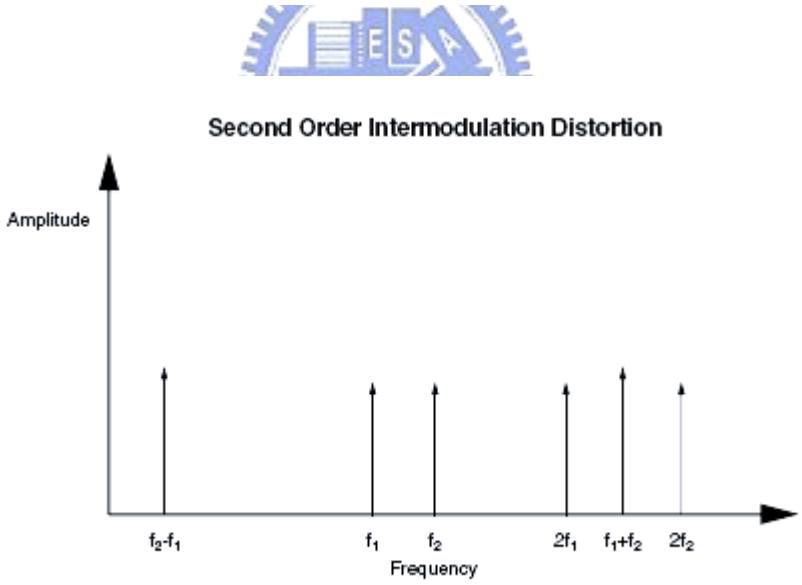


Figure 5-5 The second order intermodulation distortion plot[31]

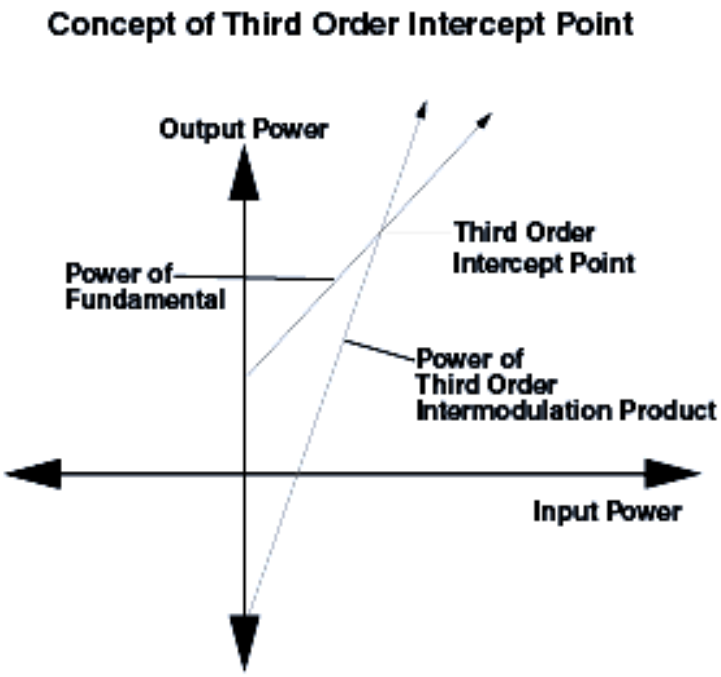


Figure 5-6 Pout (fundamental) and Pout (third order product) as a function of Pin [31]

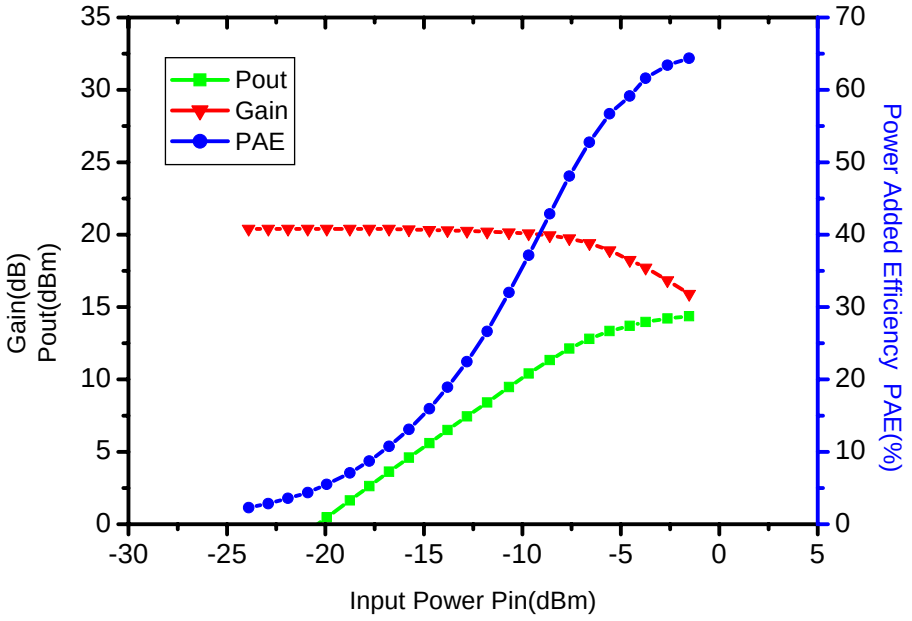


Figure 5-7 1.95 GHz one tone power performance as a function of the input power for the 0.5 μm × 200μm E-mode PHEMT. The device was tuned for maximum output power match.

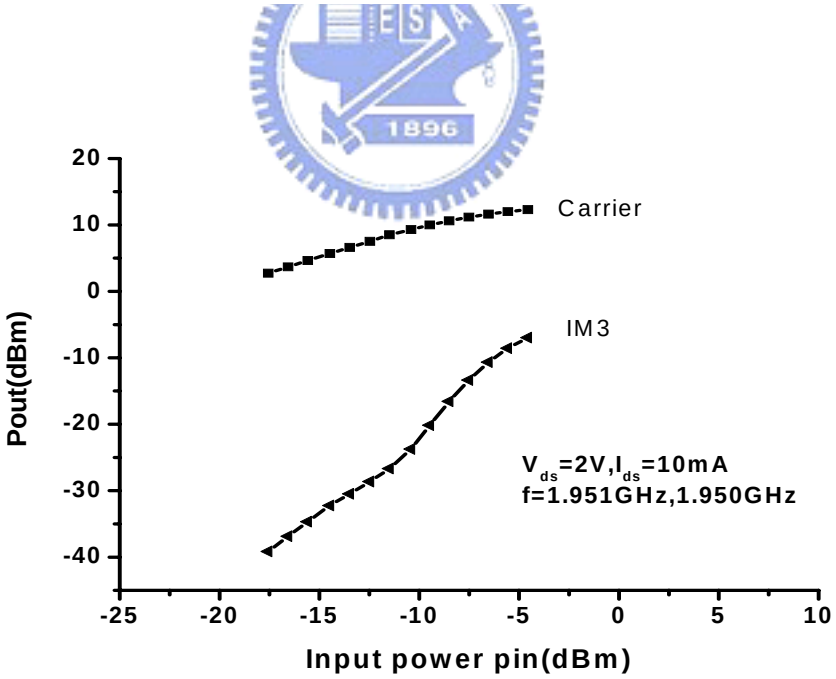


Figure 5-8 Two tone output power and the third order products against input power. The device was biased at V_{DS}=2 V, I_{DS}=10 mA and tuned for maximum linearity match.

Chapter 6

Effect of gate sinking on the device performance of the InGaP/AlGaAs/InGaAs E-mode PHEMT

6-1 Introduction

Advanced wireless communication systems require high RF performance power amplifier with low supply voltage, high power added efficiency (PAE) and long stand-by time. Enhancement-mode Pseudomorphic high electron mobility transistor (E-mode PHEMT) is getting popular as power device for wireless communication due to single-voltage operation, low knee voltage and high power added efficiency (PAE) at low drain bias. The E-mode PHEMTs also have adequate low drain leakage current during stand-by time and can be used with the elimination of the negative bias voltage, all these can extended the battery life time used in the E-PHEMT power amplifiers[34]-[37].

The InGaP/AlGaAs/InGaAs PHEMTs take the advantages of the high energy band-gap of InGaP and the excellent etching selectivity between InGaP and GaAs. These advantages result in higher breakdown voltage, low gate leakage current and high etching selectivity for the device. Furthermore, the use of InGaP/AlGaAs/InGaAs structure enhances the conduction band discontinuity between

the spacer and the channel layer than that of the conventional InGaP/InGaAs structure which improves the carrier confinement and result in higher current density of the devices [38] [39]. The Hall mobility of the InGaP/AlGaAs/InGaAs PHEMTs is also higher than that of the InGaP/InGaAs PHEMTs due to the smoothness of the AlGaAs/InGaAs interface [40].

In this study, Pt buried gate technology is used in E-mode InGaP PHEMT fabrication. The motivations are more flexibility to reduce source resistance (R_s) [41] and a high Schottky barrier height demonstrated in the Pt/InGaP [42] In addition, the Schottky barrier height increase as Pt diffused into the Schottky layer also caused the gate leakage current reduction [43]. However, the use of Pt buried gate on GaAs based E-mode PHEMT fabrication was never reported. In this study, the Platinum (Pt) buried gate technology was used to fabricate the InGaP/AlGaAs/InGaAs E-mode PHEMTs.

6-2 Device Structure and Fabrication

The E-mode InGaP/AlGaAs/InGaAs PHEMT structure was grown by Metal Organic Chemical Vapor Deposition (MOCVD) on a 4 inch GaAs substrate. The epi-layers consist of, from bottom to top, GaAs buffer layer, AlGaAs/GaAs supper-lattice layers, 200Å $Al_{0.24}Ga_{0.76}As$ layer, lower Si δ-doped layer, followed by

undoped 30Å $Al_{0.24}Ga_{0.76}As$ spacer, 150Å $In_{0.2}Ga_{0.8}As$ channel, 20Å $Al_{0.24}Ga_{0.76}As$ spacer, 20Å undoped $In_{0.49}Ga_{0.51}P$, upper Si δ-doped layer, 160Å undoped $In_{0.49}Ga_{0.51}P$ Schottky layer and 750Å heavily doped n^+ GaAs cap layer. The active area of the device was defined by wet chemical mesa etching. The Au/Ge/Ni/Au ohmic contacts were formed by e-beam evaporation. After rapid thermal annealing (RTA) at 350°C for 1 min, the contact resistance measured by the transfer length method was 0.1448 Ω-mm. The bi-layer resists which consisted of polymethylmethacrylate (PMMA) and polymethylmethacrylate-methacrylic acid P(MMA-MAA) were used for gate formation. Citrate acid/H_2O/H_2O_2 solution was used for gate recess, and the recess etching was stopped at the InGaP layer due to the high selectivity between InGaP and GaAs. The gate metals consist of Pt(20nm)/Ti(100nm)/Pt(100nm)/Au(300nm), which were deposited by electron beam evaporator. After T-gate formation, 100-nm-thick silicon nitride film was deposited by plasma enhanced chemical vapor deposition (PECVD) at 250℃ for 10min as the passivation layer. Finally, thermal annealing at 325℃ for 1 min was performed for gate sinking to further reduce the drain and gate leakage current. The sinking of Pt into the InGaP shift the gate metal front closer to the InGaAs channel, as illustrated in Figure 6-1 (a).

6-3 Gate sinking process and Schottky Characteristics

In order to understand the interfacial reaction between the Pt contact metal and the InGaP layer, samples with Pt/Ti/Pt/Au metals deposited on the InGaP layer without SiN deposition were prepared for transmission electron microscopy (TEM) analysis and the energy dispersive X-ray (EDX) analysis. The cross-sectional TEM image of the as-deposited sample showing the Pt and InGaP interface is shown in Figure 6-1 (b). About 5nm-thick amorphous layer exists in the InGaP layers and this amorphous layer was formed during the deposition of platinum. Earlier reports on Pt/GaAs system showed that amorphous layers were also found in the as-deposited Pt/GaAs interfaces [44] [45]. After annealing at 325℃ for 1 min, the amorphous layer which consists of Pt and InGaP mixture (the ratio of Pt is 51.83%) increased to 10nm, i.e. the InGaP layer thickness decreased by 5nm due to the amorphous layer thickness increase as shown in Figure 6-1(c).

Figure 6-2 shows the I-V characteristics of the diodes before and after annealing. The Schottky barrier height, which was evaluated by I-V measurement, increased from 0.78 to 0.84eV and the ideality factor changed from 1.09 to 1.12, after annealing. After 325℃ annealing for 3hr, new phase of $Ga_2Pt(111)$ formed as indicated by the XRD data in Figure 6-3 and device performance degraded. This implies that after sufficient thick amorphous layer was formed at 325℃, the thermal energy received

from the annealing was used for the nucleation and the formation of the new crystalline phase. This process will limit further inter-diffusion of the Pt into the InGaP layer. In addition, the formation of the amorphous layer caused the gate capacitance increase due to the decrease of the gate to channel distance [46].

6-4 DC Characteristics

Figure 6-4 shows the transconductance and the drain-source current vs. V_{GS} of the 0.7 μm × 240μm E-mode PHEMT before and after annealing at 325℃ for 1min. The peak transconductance of the device measured before annealing was 287mS/mm at V_{DS} =2V and the V_{th} was 0.17V. After annealing, the peak transconductance was increased to 373mS/mm and V_{th} was increased to 0.41V when V_{DS} = 2V. The threshold voltage is defined as V_{GS} when the I_{DS} reach 1mA/mm. After annealing, the gate leakage current slightly reduced from -1.3 μA/mm to -0.79 μA/mm when biased at V_{DS} = 2V and V_{GS}=0V. Therefore, the drain leakage current also decreased from 1.56μA/mm to 0.16μA/mm when biased at V_{DS} = 2V and V_{GS}=0V.

The threshold voltage can be obtained by solving Poisson's equation in one dimension [42]. After annealing, the measured Schottky barrier height and effective distance between the gate and the channel region changed. We believe that the threshold voltage increases related to the Schottky barrier height increase and the decrease in the distance between the gate and the channel layer. As a result, the device

can be biased at higher forward gate voltage due to lower gate leakage current and has higher saturation current even though the current density is lower at the same gate bias point as compared to the devices without gate sinking.

The threshold voltage (V_{th}) vs. annealing temperature is shown in Figure 6-5. The threshold voltage stabilized after 1 min annealing and remained almost the same after 325℃ annealing for 10 min. The threshold voltage of the HEMT device was very uniform after the gate sinking process and demonstrated good reproducibility as shown in Figure 6-6. The V_{th} of the devices has a small standard deviation of 30mV across the 4 inch wafer. For the two wafers under study, the range of the standard deviation of V_{th} remained almost the same.

6-5 RF and Power Performance

The S parameters of the E-mode PHEMTs were measured by on-wafer testing from 1 to 40GHz. The calculated best f_T and f_{max} of the before and after annealed E-mode PHEMT were measured. Before annealing, the calculated f_T and f_{max} were 18 GHz and 29 GHz, respectively, when device was biased at Vgs=0.6V and Vds=2V. After annealing, the calculated f_T and f_{max} were 21 GHz and 38 GHz, respectively, when device was biased at Vgs=0.8V and Vds=2V. The RF performance improvement after gate sinking was due to the transconductance increase which was caused by the Pt

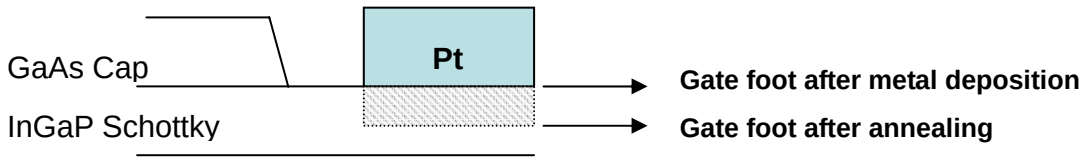
sinking into the InGaP layer after annealing.

The power performances of the 0.7×240 μm^2 device was measured at 2GHz and tuned for maximum power added efficiency (PAE) match. Figure 6-7 shows the power performance before and after annealing. From Figure 6-7(a), it is clearly observed that for the device before-annealing, the gate current increased drastically with RF input level; which in turn could imply worse RF reliability under highly driven operation for such devices. Figure 6-7 (b) shows the device after annealing, the P_{out} was 13.59 dBm (95.23mW/mm) with 54% PAE and 21.77dB linear gain, when biased at V_{DS}=2V, I_{DS}=20mA. In contrast to the before-annealing device, the gate current was quite low and remained almost constant over the whole input power range up to 10-dB compression, implying a much better RF reliability performance.

6-6 Summary

The use of the Pt buried gate technology on the fabrication of the InGaP/AlGaAs/InGaAs E-mode PHEMT was realized successfully. The threshold voltage distribution of the device after gate sink was very uniform and reproducible. The amorphous layer formation between Pt and InGaP layer after gate sinking as observed by TEM was believed to be the cause of the threshold voltage shift and the Schottky barrier height increase. The fabricated E-mode PHEMT device with gate

sinking showed excellent RF performance, good threshold voltage uniformity and reduced gate and drain leakage currents, the use of the gate sinking technology is believed to be very useful for the E-mode InGaP/AlGaAs/InGaAs PHEMTs fabrication.



(a)

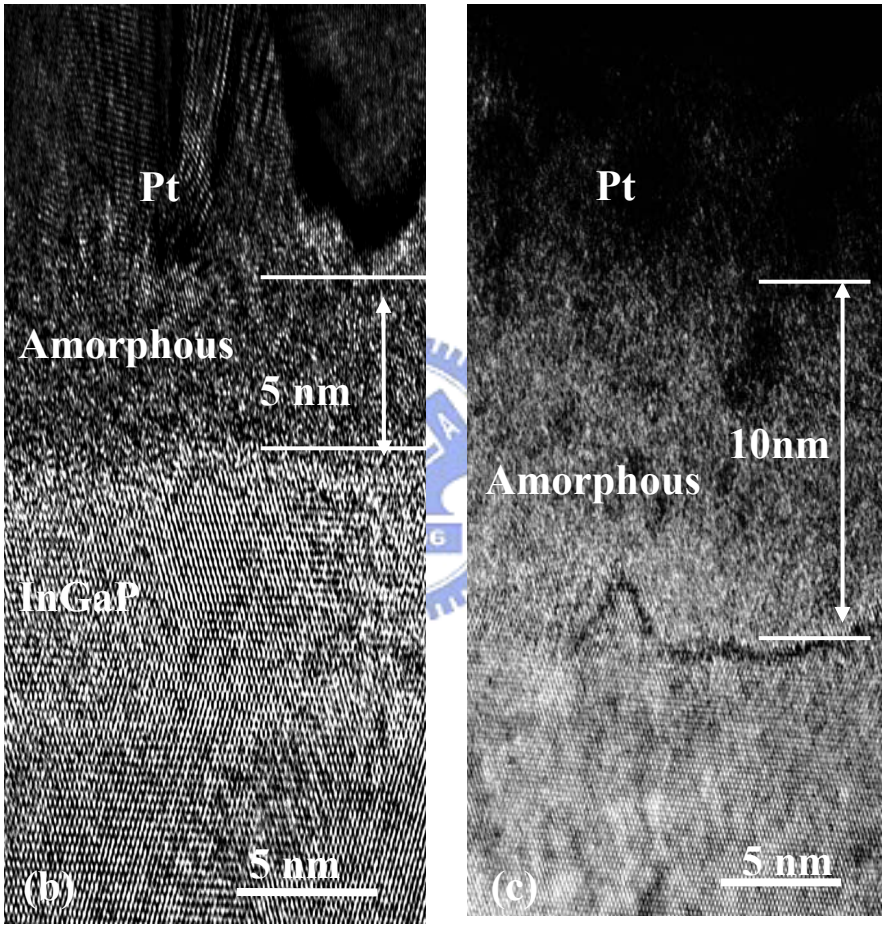


Figure 6-1 (a) The positions of the gate metal foot before and after annealing

(b) The cross-sectional TEM image of the as deposited Pt/InGaP interface

(c) The cross-sectional TEM image of Pt/InGaP interface after 325℃ annealing for 1min.

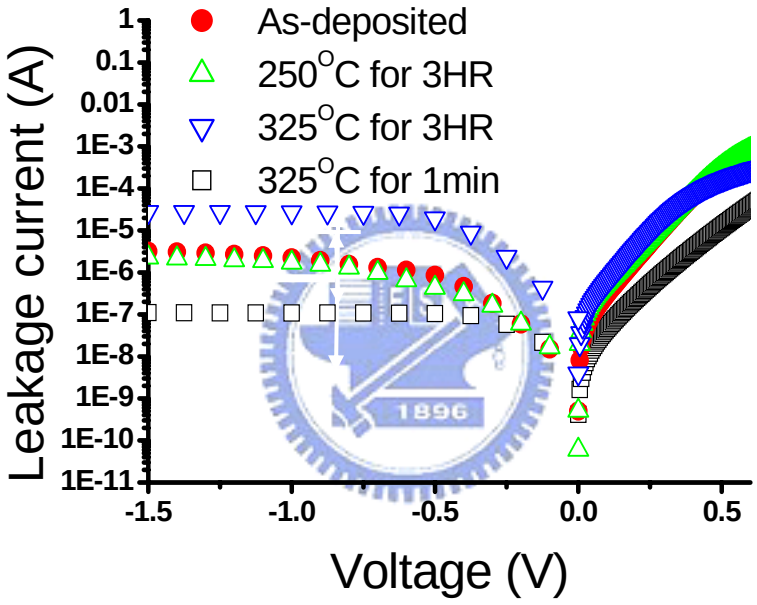


Figure 6-2 I-V characteristics of the diodes before and after annealing

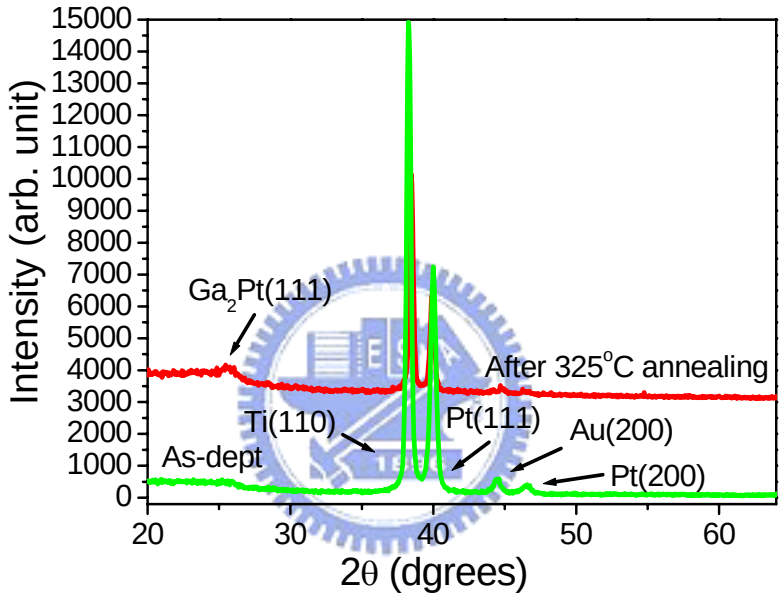


Figure 6-2 **X–ray diffraction spectra of the Pt/Ti/Pt/Au and InGaP/AlGaAs/InGaAs PHMET sample before and after annealing at 325℃ for 3 hours. Main component: Ti, Pt, Au, Ga_2Pt (JCPDS PDF 44-1288, 04-0802, 04-0784, 03-1007)**

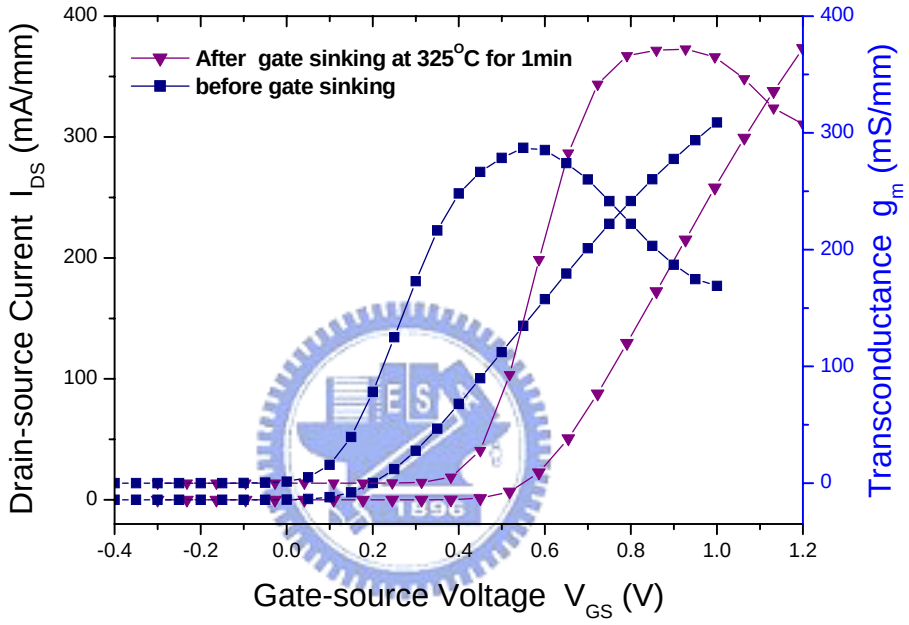


Figure 6-4 **The transconductance and the drain-source current vs. V_{GS} curves of the 0.7 μm × 240 μm E-mode PHEMT at V_{DS} = 2V with 20nm thick Pt before and after gate sinking at 325℃ for 1 min.**

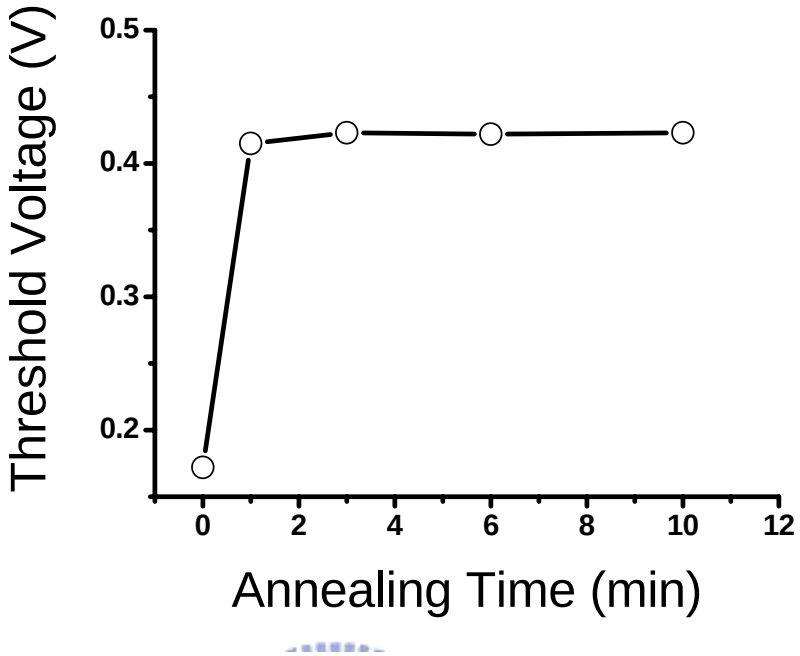


Figure 6-5 Threshold voltage of the Pt/Ti/Pt/Au E-mode PHEMT vs. annealing time when annealed at 325℃

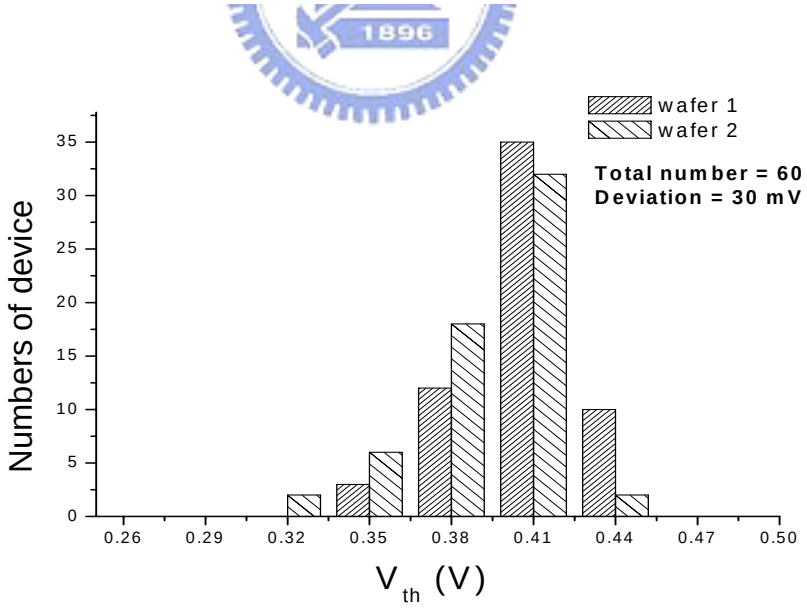
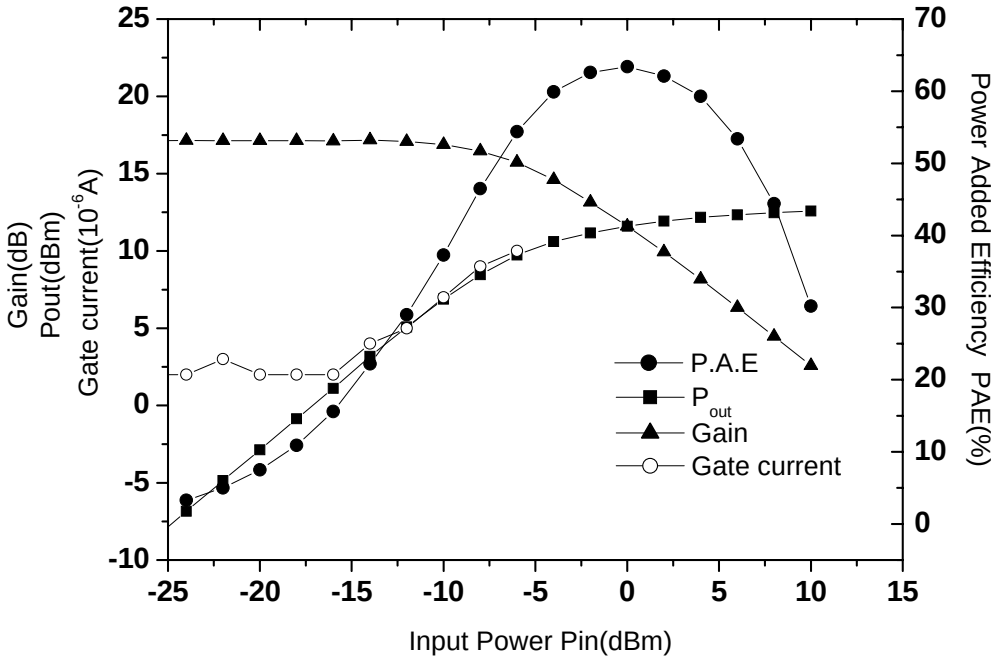
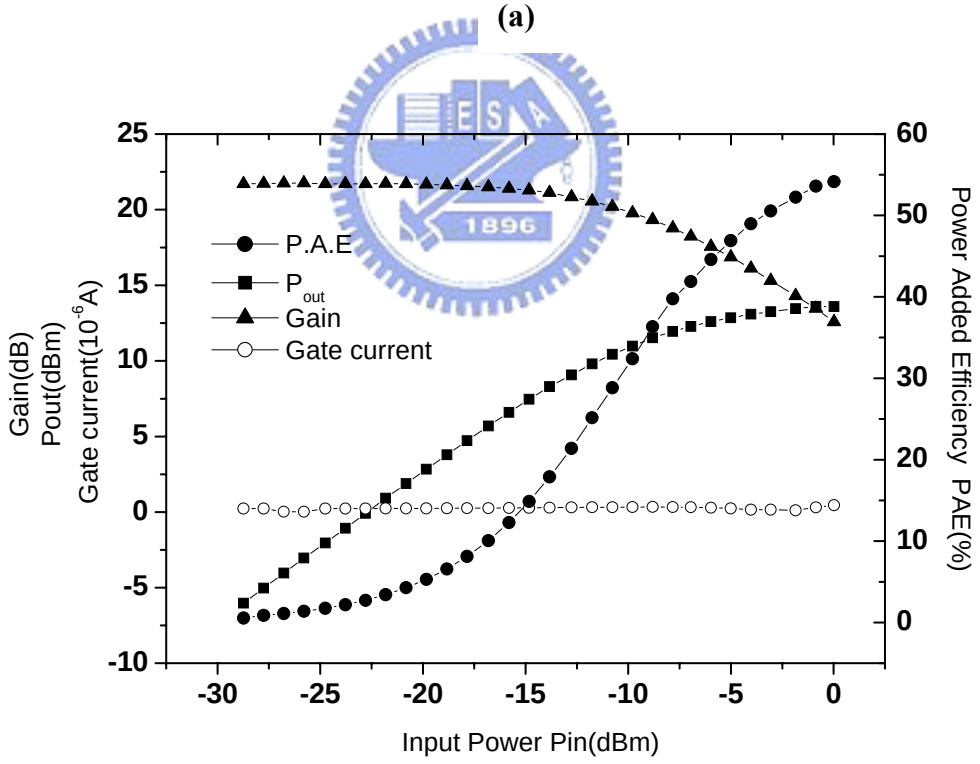


Figure 6-6 Distribution of V_{th} for the E-mode PHEMT across 4 inch wafer for two different wafers



(a)



(b)

Figure 6-7 (a) Power performance and gate leakage current of the 0.7 μm × 240μm E-mode PHEMT before gate sinking

(b) Power performance and gate leakage current of the 0.7 μm × 240μm E-mode PHEMT after gate sinking

Chapter 7

Interfacial reactions of Pt-based Schottky contacts on InGaP

7-1 Introduction

Aluminum-free InGaP semiconductor on GaAs has recently attracted a great deal of attention because of its microwave-device application possibilities[47]-[51].InGaP has an edge over conventional AlGaAs for its wider band gap, high etching selectivity, low surface recombination velocity, less susceptibility to surface oxidation, and the absence of DX-centers[52]. In the past few years, interfacial reactions of various Schottky-contact metals, such as Pt/Ti/Pt/Au[51], Ti/Pt/Au[53][54], WSiN[55], and Cu/Au[56]-[58] with the semiconducting InGaP have been extensively studied, but none were proven perfect for technological implementations. The Schottky-contact qualities of InGaP/Ti/Pt/Au[53] and InGaP/WSiN[54], for example, were found to degrade after a 500 ℃ heat treatment at which spurious CuP_2 for InGaP/Cu/Au has also been reported[58].

In seeking solutions to surmount such interface-reaction problems, Pt has lately been used as a gate-sinking metal to keep the threshold voltage and leakage current under control for InGaP HEMT devices[50] because of their higher Schottky barrier

which could translate directly into reduced leakage current and thus also enhanced RF device performance [51][59]. Unfortunately, Nebauer et al[49] has observed $GaPt_x$ compounds and other multi-component phases while Ga_2Pt compound has also been detected using X-ray diffractometry (XRD)[50] in the annealed Pt/InGaP junctions. Whether Pt can be an enabling Schottky metal or not would hence depend on how resilient it is to the thermal processing without interacting with the semiconductor. Nevertheless, the exact nature of this interface reaction remains unclear. This is possibly due to the difficulty in properly labeling Ga atoms in the InGaP/GaAs heterostructure and the lack of clear electron diffraction patterns necessary to help determine the zone-axis of the InGaP semiconductor layer. There is thus an incentive to continue to better understand the Pt/InGaP interface properties to help shed some light on why Pt/Ti/Pt/Au metals fail as a good Schottky contact and whether a solution to can be found to prevent it.

7-2 Schottky Diodes Fabrication

In this work, the material stability and the interfacial reactions between Pt and InGaP were analyzed with high resolution transmission electron microscopy (HRTEM) while the current-voltage characteristics of Pt/InGaP Schottky diodes were also measured to seek correlations between the material structures and device

performances. The heterostructure consists of, from bottom to top, a GaAs buffer layer, a 200-Å thick undoped $In_{0.49}Ga_{0.51}P$ Schottky layer, and a 750Å thick heavily doped n^+-GaAs cap layer. The Schottky diodes schematic were shown in Figure 6 and fabricated by following steps: Firstly, the Ohmic metal-contact metals Au/Ge/Ni/Au were deposited on the cap layer in sequence, and subsequently, the samples were annealed at 350℃ for 1 minute. The contact resistance (Rc) was measured via the transmission line model (TLM) method using 100μm (Wx) x 75μm (Wy) pads with inter-edge spacing of the neighboring pads (L) ranging from 36, 20, 10, 5, to 3 μm sequentially. The total resistance $R(L)=2Rc+Rs$, where Rs is the resistance of the sample of length L, width Wy ad thickness t and $Rs=\rho_s L/tWy$. The sample sheet resistance $R_{sheet} = \rho_s/t$,, hence $R(L)=2Rc+ (R_{sheet}/Wy)L$. Hence, one can obtain $R(0)=2Rc$ by extrapolating the supposedly linear relation to L=0 to find the intercept of the R-axis, while the slope represents R_{sheet}/Wy. Meanwhile, from the L-axis intercept $R(2Lt)=0$, one obtains $Lt=-RcWy/R_{sheet}$. Both Rc and the sample sheet resistance R_{sheet} of the semiconductor being measured follow naturally once the two intercepts are known. In the TLM method all the voltage drops from the pads to the sample are assumed to be across the two neighboring edges of the pads on which the electrodes are placed (thus only Wy is relevant, but not Wx). With this in mind, we have Rc=2.56Ω, L_T= −1.06μm, and R_{sheet}=180Ω/□ for the InGaP. These give the

figure of merit RcWy=0.19Ω-mm, as compared to the previously reported 0.14Ω-mm in Ref. 4 for a device structure of similar materials though somewhat differently structured, where the associated numbers are Wy=75μm, Rc=1.93 Ω, Lt=–1.18μm and R_{sheet}=123Ω/□ for the InGaP. Secondly, the Schottky electrode which consists of Au(300nm)/Pt(100nm)/Ti(100nm)/Pt(20nm) stack was placed directly on InGap after the n^+ GaAs layer was removed by a citric-acid/H_2O/H_2O_2 solution, all by e-beam evaporation. The 300-nm Au layer serves to lower the overall Schottky-metal resistance while the 100-nm Pt layer acts a diffusion barrier to prevent Au from diffusing into the Au/Pt/Ti/Pt/InGaP Schottky diode structure[60], largely because of its high melting point and compatibility with the lift-off process. Note that in order to optimize the Schottky barrier height [51], placed at the bottom of the metal stack is a 20-nm layer of Pt separated from the other 100-nm Pt layer by an also-100-nm thick Ti layer as shown in Figure 1. Finally, these Schottky diodes were annealed, for various durations at 325℃, which is 25 ℃ below ohmic RTA temperature, avoiding affecting ohmic contact resistance.

7-3 Experiment results and Discussions

Energy dispersive x-ray (EDX) with electron beam of 2-nm spot size equipped on an HRTEM was performed for composition analysis. The cross-sectional TEM

(XTEM) image showing the Pt/InGaP interface for an as-deposited sample is presented in Figure 2(a). Each layer was identified by the nano-beam EDX analysis. As is obvious, there is a 7.5 nm-thick amorphous layer existing at the Pt/InGaP interface and similar results were also found in the as-deposited Pt/GaAs interfaces [45] even for samples as-deposited at room temperature. The amorphous phase formation implicates the enormous inherent thermodynamic driving forces [45] that push the Pt atoms over the diffusion barrier to migrate into the InGaP layer. After annealing at 325℃ for 1minute, the thickness of the amorphous layer increased from 7.5 nm to 12.8 nm. The diminution of the InGaP layer is due to the fact that more Pt atoms diffused into the pristine InGaP layer after thermal annealing. The diffusion boundary between InGaP and the amorphous layer was non-uniform, which could be caused by the non-uniform thermal process due to the short-time annealing.

Figure 3 (a) shows the cross-sectional HRTEM image of the Pt and InGaP interface reaction, whereas Figure 3(b) gives the selected area diffraction patterns of the amorphous layer after 325℃ annealing for 10 minutes. The nucleation of the crystalline phase occurred in the amorphous layer after annealing for 10 minutes at 325℃ as shown in Figure 3(c). The HRTEM image of the InGaP/GaAs interface after annealing at 325℃ for three hours is provided in Figure 4(a). The crystalline grains were observed in the amorphous layer near its interface with InGaP and were

identified as an orthorhombic Ga_2Pt (422) phase, judged from the nano beam selected area diffraction patterns shown in Figure 4(b). The STEM image of the Pt/InGaP interface after annealing at 325℃ for three hours is presented in Figure 5(a). However, near the interface of the amorphous layer with Pt, a tetragonal $GaPt_3$ (422) phase was observed as identified, as shown in Figure 5(b). On the basis of these observations, this thin amorphous layer, it can be concluded, could be a precursory step to forming more stable Ga_2Pt (422) and $GaPt_3$ (422) phases at the later stage of annealing. The new phases of the Ga_2Pt (422) and $GaPt_3$ (422) existed in different locations of the amorphous layer. The Ga_2Pt (422) near the InGaP layer was a result of the out-diffusion of Ga from InGaP into the amorphous layer, and $GaPt_3$ (422) was present near the alloy-Pt interface.

Figure 6 shows the I-V characteristics of the diodes before and after annealing, the leakage current decreased after 325℃, 1 minute annealing, possibly due to Pt diffusion [46]. After 325℃ annealing for 10 minutes, the diodes' performance remained almost unchanged even with the crystalline phase nucleated at the amorphous layer as shown in Figure 3(b). The diodes performance degradation after the 325℃3-hour annealing is attributed to the formations Ga_2Pt (422) and $GaPt_3$ (422).

7-4 Summary

The interfacial reactions between the Pt and the InGaP layers after thermal annealing were investigated in this study. An amorphous layer approximately 7.5nm-thick formed between the Pt and InGaP layers after gate metal deposition due to the release of latent heat. After annealing at 325℃ for 10 minutes, the nucleation occurred in the amorphous layer located at InGaP and Pt interface. This amorphous layer represents the intermediate step for the formation of a new phase. Moreover, the thickness of the amorphous layer remained unchanged, indicating that the insertion of Ti layer at 325℃ was effective as a diffusion barrier. After annealing for three hours at 325℃, the stable Ga_2Pt(422) and $GaPt_3$(422) phases formed in the InGaP layer; moreover, apart from the bottom Pt, Au, middle Pt and Ti reflexes, no other phases could be found. Therefore, it can be concluded that these new phase formations have a degrading effect on electrical characteristics. Moreover, the Ga_2Pt (422) phase observed at the InGaP/GaAs interface exhibited a continuous diffusion of Pt atoms even after three hours of annealing. Thus, further study of Pt diffusion with a thinner bottom Pt layer thickness at various annealing temperatures and durations may be required to optimize the Schottky characteristics stabilization. In short, the thermal degradation mechanism of Pt/InGaP Schottky contacts was caused by formation of

the $Ga_2Pt(422)$ and $GaPt_3(422)$ compounds due to the Pt diffusion during thermal annealing.

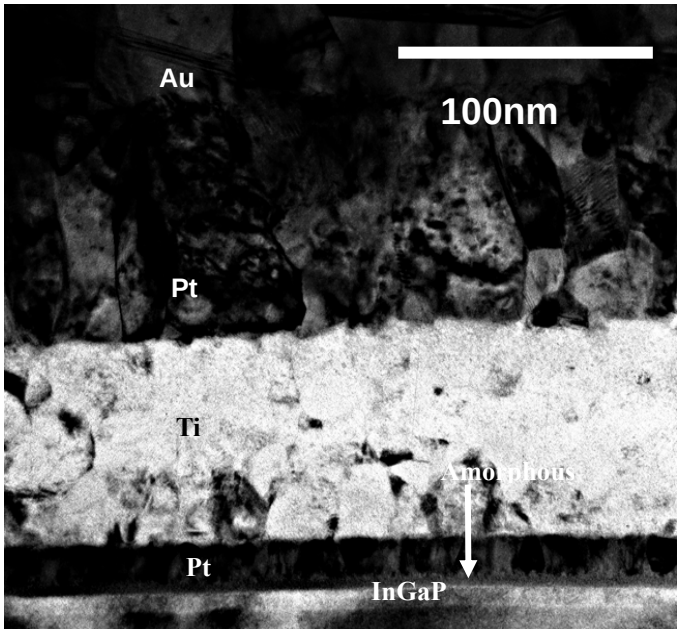


Figure 7-1 The HRTEM image of InGaP/Pt/Ti/Pt/Au

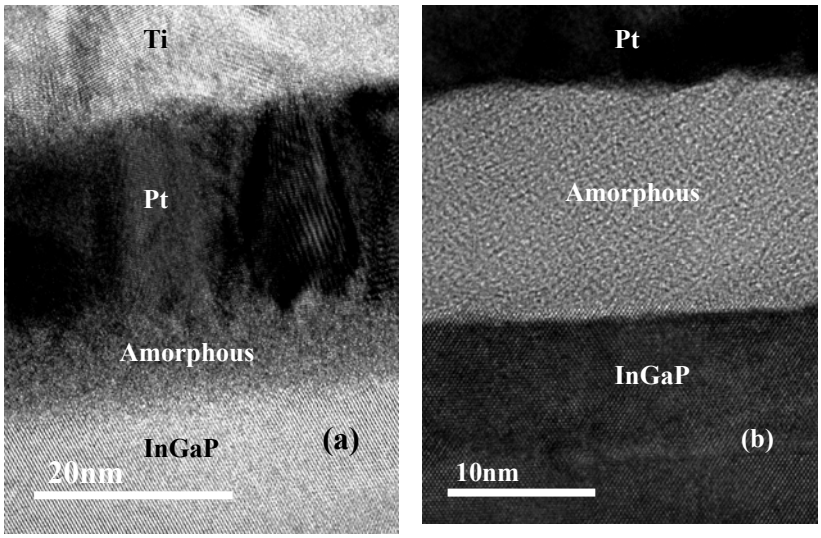


Figure 7-2 (a) The cross-sectional HRTEM image of Pt and InGaP interface after metal deposition. (b) The cross-sectional HRTEM image of the Pt and InGaP interface after annealing at 325℃ for 1 minute.

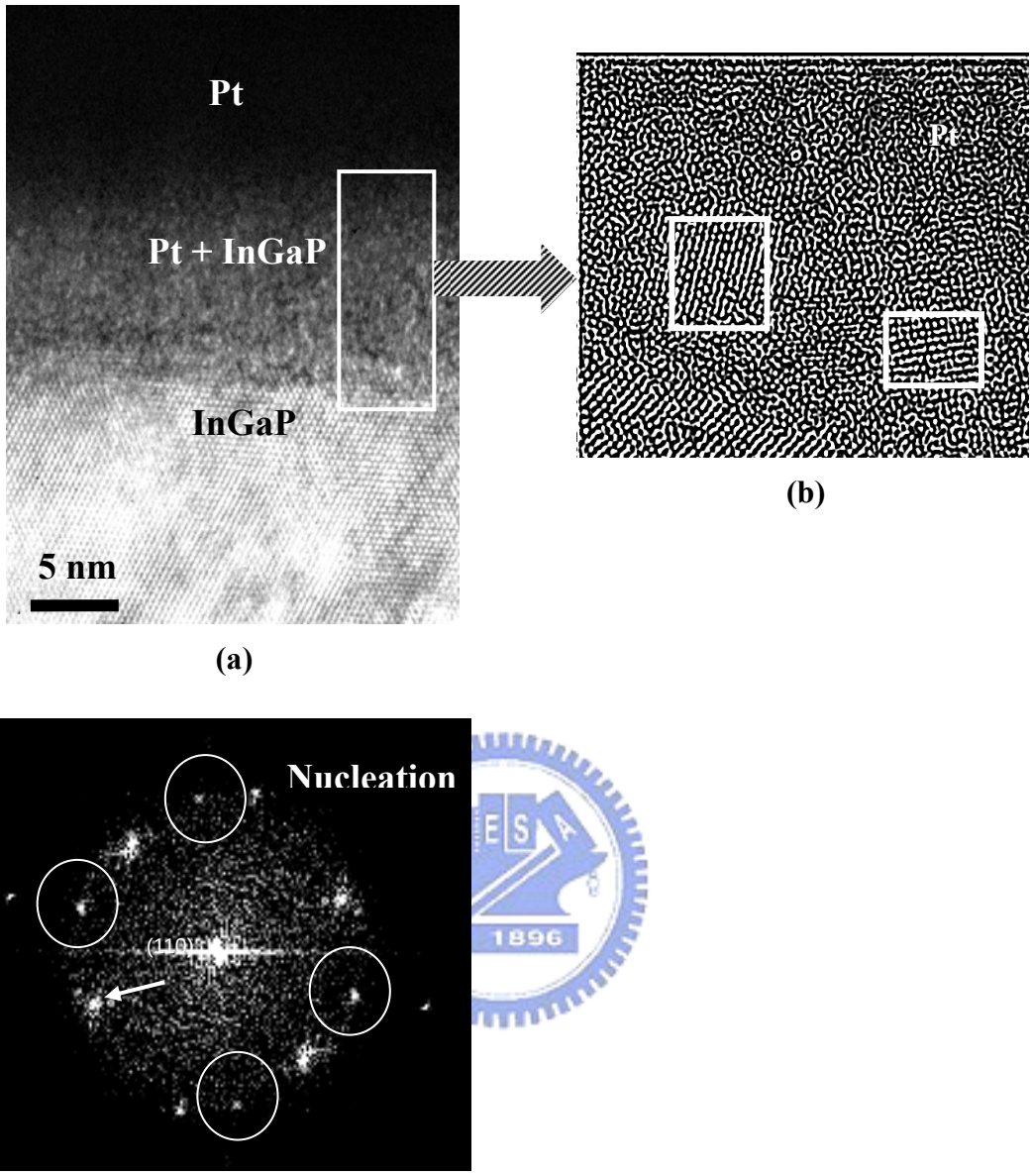


Figure 7-3 **(a) The cross-sectional HRTEM image of the Pt and InGaP interface after annealing at 325℃ for 10 minutes.**
(b) The Fast Fourier transform (FFT) lattice image of the amorphous area which was shown in Figure 2(a). The nucleation area was labeled by white square.
(c) Nano –beam selected area electron diffraction pattern of the amorphous area shown in Figure 2(a).

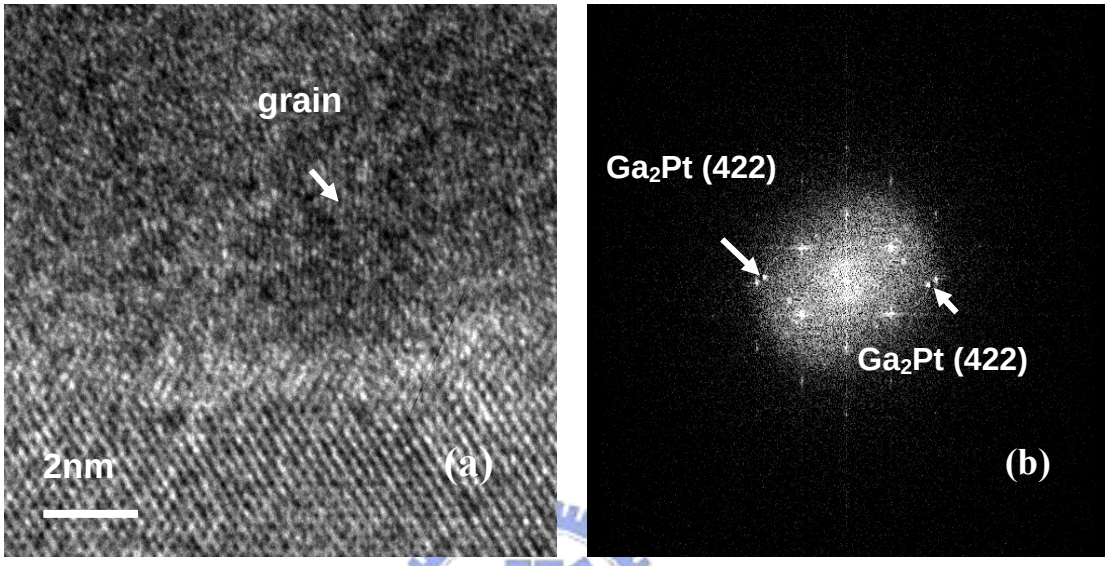


Figure 7-4 **(a) The cross-sectional HRTEM image of Pt and InGaP interface after 325℃ for 3 hours annealing.**
(b) Nano-beam selected area diffraction pattern of Ga_2Pt (422)

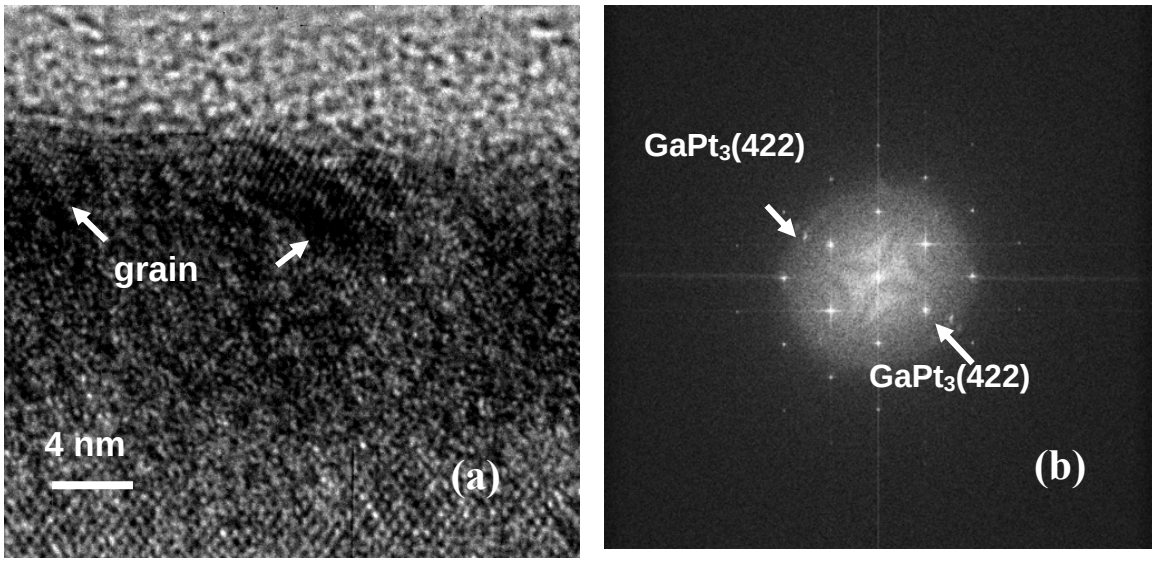


Figure 7-5 **(a) The cross-sectional HRTEM image of Pt and InGaP interface after 325℃ for 3 hours annealing.**
(b) Nano-beam selected area diffraction pattern of $GaPt_3$ (422)

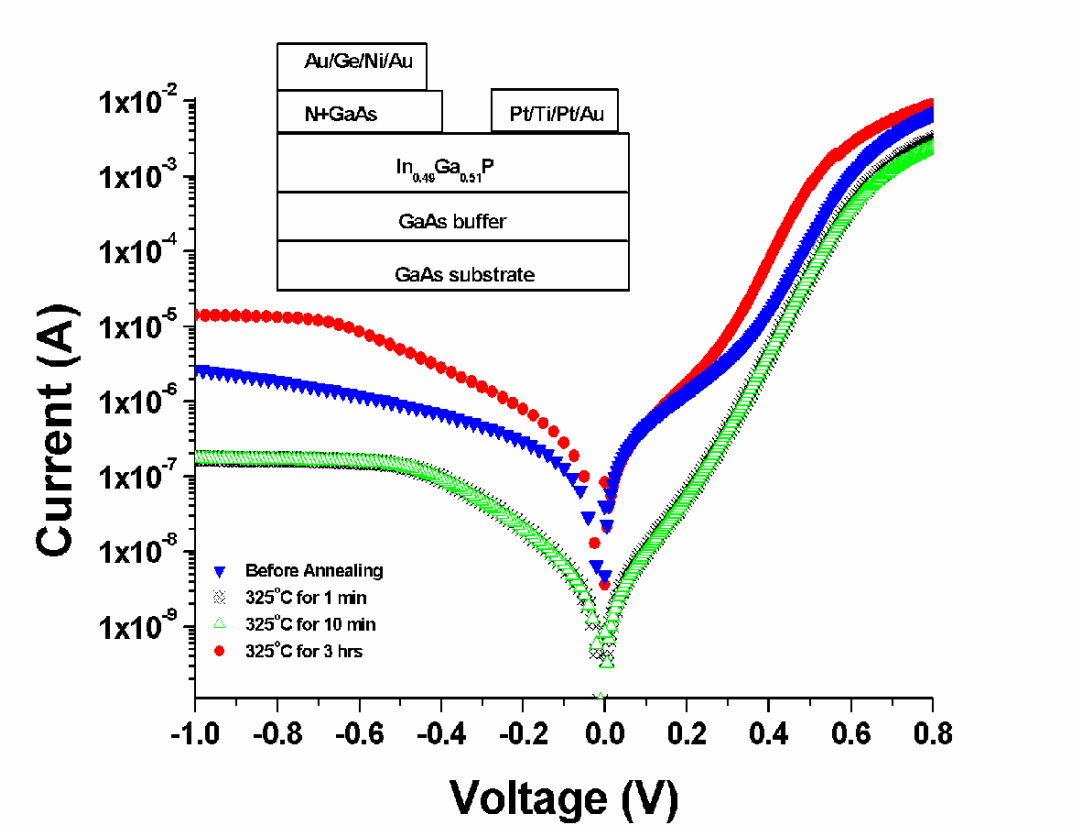


Figure 7-6 I-V characteristics of the Schottky diodes before and after annealing.

Chapter 8

Conclusions

A single voltage supply, high frequency and high power density Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT was developed for low-voltage wireless application. The excellent threshold voltage uniformity and performance of the E-mode PHEMT were due to the use of InGaP/AlGaAs/InGaAs layer structure which took advantages of the high etching electivity between InGaP/GaAs and high electron mobility due to the use of AlGaAs spacer layer. The calculated f_T and f_{max} of the E-mode PHEMT were 60 GHz and 128 GHz, respectively. The noise figure of the device at 17GHz was measured to be 1.02dB with 10.12dB associated gain. High power performance was also achieved, the E-mode PHEMT exhibited a maximum PAE of 70% with maximum power density of 18.61 dBm at 2.4GHz.

However, advanced high performance wireless application systems, such as Wide-band Code-Division Multiple-Access (W-CDMA) system has imposed stringent requirements on the devices efficiency, linearity and power consumption. While linearity has been an important figure of merit for devices, it is also necessary for the device to meet the noise characteristics to guarantee minimum signal distortion at the receiving end of modern communication systems. In this study, high linearity and low

noise Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT was developed for low-voltage operation wireless application. To improve the device linearity, it is required for the transconductance of the device to remain constant over the operating gate bias range to minimize the third-order distortion. Therefore, flatten transconductance (Gm) profile will result in lower IM3 levels and higher third-order intercept point (IP3), and thus improve the device linearity. The developed E-mode PHEMT exhibited F_{min} of 0.86 dB with 12.21 dB associated gain at 10 GHz. The device also demonstrated high linearity characteristics due to the optimal double delta doping structure. The Enhancement-mode InGaP/AlGaAs/InGaAs PHEMT demonstrated only 1.25 dBm back-off from P_{1dB} and achieved excellent linearity with OIP3 - P_{1dB} of 13.2 dB and a high linear power efficiency of 35% when under W-CDMA modulation. The developed Enhancement-mode InGaP/AlGaAs/InGaA PHEMTs with low noise and high OIP3 are of great use for the wireless communication applications.

In addition, the use of the Pt buried gate technology on the fabrication of the InGaP/AlGaAs/InGaAs E-mode PHEMT was realized successfully. The threshold voltage distribution of the device after gate sink was very uniform and reproducible. The amorphous layer formation between Pt and InGaP layer after gate sinking as observed by TEM was believed to be the cause of the threshold voltage shift and the

Schottky barrier height increase. The fabricated E-mode PHEMT device with gate sinking showed excellent RF performance, good threshold voltage uniformity and reduced gate and drain leakage currents. Thus, the use of the gate sinking technology is proved to be very useful for the E-mode InGaP/AlGaAs/InGaAs PHEMTs fabrication.

Finally, the interfacial reactions between the Pt and the InGaP layer after thermal annealing had been investigated. A 7.5nm-thick amorphous layer was formed between Pt and InGaP layer after the room-temperature gate-metal deposition. After annealing at 325℃ for 10 minutes, crystallizations took place in the amorphous layer. At this stage, the thickness of amorphous layer remained unchanged; indicating that insertion of the Ti layer was effective as a diffusion barrier at 325℃. After annealing for 3 hours at 325℃, however, stable phases of Ga_2Pt(422) and $GaPt_3$(422) formed in the InGaP layer, though not in the Schottky metal stack, leading to degradation of the diode performances. However, the Ga_2Pt (422) phase was observed at the InGaP/GaAs interface, exhibiting continuing diffusion of Pt atoms beyond the 3-hour annealing. Thus, further study on the Pt diffusion at various annealing temperatures and durations for the contact metal stacks with, for example, thinner bottom Pt layers may be necessary to optimize the Schottky characteristics stabilization.

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博士論文題目：

增強型磷化銦鎵/砷化鋁鎵/砷化銦鎵假晶高電子遷移率電晶體之研究

The study of Enhancement-mode InGaP/AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor

Publication List

Journal Papers

1. H. C. Chang, E. Y. Chang, Y. C. Lien, L. H. Chu, S. W. Chang, R. C. Huang and H. M. Lee, "Use of WN_x as diffusion barrier for copper airbridged low noise GaAs PHEMT", ***IEE Electronics Letters**, vol. 39, no. 24, 2003, pp. 1763-1765*

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Conference Papers

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