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博 士 論 文

氮氧化層及高介電常數介電層在金氧半元件及快閃記憶體上之特性研究

Investigation of Nitrided Oxides and High-κ Dielectrics on MOS Devices and Flash Memories

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摘要

隨著系統晶片（SOC）的發展，持續降低 CMOS 元件中的閘極介電層及非揮發性記憶體中的複晶矽層間介電層（inter-poly dielectric）厚度以提高元件密度及降低操作電壓變得十分重要。為了滿足以上的需求並獲得較低的漏電流及較高的可靠度，利用氮氧化層（nitrided oxide）及高介電常數材料（high-κ）來取代二氧化矽變成是不可或缺的趨勢。

本篇論文首先研究利用成長氧化層前的氮原子離子佈植（nitrogen-implanted Si substrate）及氧化層成長後的一氧化氮（NO）高溫退火來改善傳統二氧化矽閘極介電層的可靠度。其次，經由模擬工具將高介電常數材料做為堆疊式快閃記憶體（stacked-gate flash memory）的複晶矽層間介電層和穿隧介電層（tunnel dielectric），並討論其對快閃記憶體寫入／抹除的效率。最後，探討表面氨氣（NH_3）氮化處理及沉積後高溫退火（post-deposition annealing）溫度對反應式濺鍍（reactive sputtering）及有機金屬化學氣相沉積（metal organic chemical vapor

deposition）之高介電常數材料三氧化二鋁（Al_2O_3）及二氧化鉿（HfO_2）複晶矽層間電容的影響。

首先，研究利用成長氧化層前的氮原子離子佈植及氧化層成長後的一氧化氮高溫退火來改善傳統二氧化矽閘極介電層的可靠度。研究結果顯示成長後的一氧化氮高溫退火會在界面處造成氮原子聚集，而成長氧化層前的氮原子離子佈植則會造成氮原子均勻分布在氮氧化層裡。摻雜進入氧化層的氮濃度也會隨著氧化層厚度而變；氧化層厚度愈薄，氮濃度愈高。聚集在界面處的氮原子有助於增強二氧化矽介電層的可靠度，包括較平整的界面、較小的電洞捕捉（hole trapping）、改善崩潰時間（time-to-breakdown）及崩潰電荷（charge-to-breakdown）等。此外，介電層的可靠度還可由氮離子佈植濃度決定。當濃度小於 1×10^{14} cm^{-2} 時，氧化速率不但不會降低，還會造成介電層可靠度劣化；相反的，若將濃度提高至 1×10^{15} cm^{-2}，氧化速度可以很明顯的被抑制並用來成長多種不同介電層厚度以滿足系統晶片需求，還可同時改善介電層可靠度。配合成長氧化層前的氮原子離子佈植和氧化層成長後的一氧化氮高溫退火更可大幅提高閘極介電層的可靠度，用以取代 0.13 微米以下製程的二氧化矽閘極介電層。

其次，經由模擬工具將高介電常數材料做為堆疊式快閃記憶體的複晶矽層間介電層和穿隧介電層，並討論其對快閃記憶體寫入／抹除的效率。模擬結果指出利用高介電常數材料取代傳統堆疊式快閃記憶體中的氧化層－氮化層－氧化層（oxide-nitride-oxide）複晶矽層間介電層可明顯的提高寫入／抹除的速度，且寫入／抹除的速度在 Fowler-Nordheim 穿隧上比熱電子（hot electron）注入的方式更有效。選擇二氧化鉿做為複晶矽層間介電層並採用 Fowler-Nordheim 穿隧來寫入／抹除，可大幅降低外加電壓達 48%。然而，高介電常數材料在穿隧介電層上的應用結果卻截然相反。由於採用高介電常數材料做為穿隧介電層會降低閘極的電壓藕合率（gate coupling ratio），利用 Fowler-Nordheim 穿隧反而會劣化寫入／抹除速度。雖然分壓在高介電常數穿隧介電層的電場會比傳統二氧化矽穿隧介

電層的電場還低，但較低的電子位障高（barrier height）及增強的碰撞游離發生率（impact ionization rate）卻使得高介電常數穿隧介電層在熱電子注入方式下有較快的寫入／抹除速度。由於適用的寫入／抹除方式不同，高介電常數材料複晶矽層間介電層及穿隧介電層可分別應用於NAND和NOR型式的堆疊式快閃記憶體。

最後，探討表面氨氣氮化處理及沉積後高溫退火溫度對反應式濺鍍及有機金屬化學氣相沉積之高介電常數材料三氧化二鋁及二氧化鉿複晶矽層間電容的影響。表面氮化處理和高溫退火溫度都會造成反應式濺鍍的三氧化二鋁複晶矽層間電容的特性和電壓極性相關。表面氮化處理會在界面處形成薄 Si-N 界面層，抑制低介電常數界面層成長、形成較平滑的界面並讓後續的高溫退火更有效率的消除原本存在的缺陷，得到較低的漏電流、較大的崩潰電場、較小的電子捕捉率和較大的崩潰電荷。再者，反應式濺鍍的三氧化二鋁複晶矽層間電容的特性也受高溫退火溫度影響甚巨。實驗結果顯示，不論是漏電流、電子捕捉率或崩潰電荷，900^{o}C 都是最佳化條件。根據 X 光光電子頻譜（X-ray photoelectron spectroscopy）和 Auger 電子頻譜（Auger electron spectroscopy）的分析，發現溫度效應會造成三氧化二鋁的組成比發生明顯的變化，其中氧原子的成份比將會決定複晶矽層間介電層的特性。有鑑於反應式濺鍍的三氧化二鋁複晶矽層間電容的崩潰電荷過低，我們也研究利用有機金屬化學氣相沉積方式沉積三氧化二鋁和二氧化鉿來改善崩潰電荷的可能性。實驗結果證明，利用有機金屬化學氣相沉積除了可大幅改善崩潰電荷外，也能有效的降低漏電流和增加崩潰電壓（breakdown voltage）和有效崩潰電場（effective breakdown field）。因此，等效氧化層厚度為 5 奈米及 3 奈米的三氧化二鋁和二氧化鉿將是 45 奈米及 32 奈米世代以下堆疊式快閃記憶體的絕佳候選複晶矽層間介電層。

Investigation of Nitrided Oxides and High-κ Dielectrics on MOS Devices and Flash Memories

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Abstract

For the system on a chip (SOC) application, a continuously scaling of the gate dielectrics for complementary metal oxide semiconductor (CMOS) and inter-poly dielectrics (IPDs) for electrically-erasable programmable read only memory (EEPROM) and stacked-gate flash memory is needed to obtain high density and low operation voltage. To meet the above requirements and exhibit a low leakage current and a good reliability, the replacement of nitrided oxides and high dielectric constant (high-κ) materials for the silicon dioxide (SiO_2) and additional treatment have become indispensable.

The first objective of this dissertation is to apply the pre-oxidation nitrogen implanted Si substrate (NIS) and post-oxidation nitric oxide (NO) annealing to improve reliabilities of conventional SiO_2 gate dielectric. Then, investigates the impact of high-κ materials serving as the IPDs and tunnel dielectrics (TDs) on the

programming/erasing performances of stacked-gate flash memories through 2-D Medici simulation. Finally, the surface NH_3 nitridation and post-deposition annealing (PDA) temperature effects of the reactive-sputtered (RS) and metal organic chemical vapor deposition (MOCVD) high-κ IPDs is studied.

Firstly, we focused on the dielectric characteristics and reliability phenomena of NIS nitrided oxides with NO- and N_2-annealing comparing to conventional SiO_2 gate oxide. It was found that a nitrogen pile-up occurred near the interface after NO-annealing, while NIS produced a uniform nitrogen distribution in the dielectric bulk. Incorporated nitrogen atomic concentration is also affected on the initial oxide thickness; thinner oxide thickness, higher nitrogen atomic concentration. Nitrogen pile-up near the interface is beneficial to enhance dielectric reliabilities in terms of smoothen interface roughness, reduced hole trapping, improved time-to-breakdown (t_{BD}) and charge-to-breakdown (Q_{BD}). Moreover, it was found that the dielectric reliability is strongly dependent on the NIS dosage. NIS with a dosage smaller than 1×10^{14} cm^{-2} is found to be useless in the oxidation rate suppression but degrades dielectric reliability simultaneously. On the contrary, the samples with 1×10^{15} cm^{-2} NIS dosage not only exhibit a significantly reduced oxidation rate, which can be used to grow multiple oxide thicknesses to meet the SOC requirement, but also improve stress immunity. NIS nitrided oxides with NO-annealing depict superior dielectric reliability and this technique appears suitable to replace the traditional SiO_2 at 0.13 μm technology node and beyond.

Secondly, the effects of high-κ IPDs and TDs on a flash memory performance will be presented. By 2-D MEDICI simulation, flash memories with high-κ IPDs clearly exhibit significant improvement in programming/erasing speed over those with conventional ONO IPD. Moreover, it is found that high-κ IPDs are more effective for

the memories programmed/erased with Fowler-Nordheim (FN) tunneling rather than channel hot electron (CHE) injection. Choosing HfO_2 as the IPD and using F-N programming/erasing scheme, the operating voltage can be reduced 48% at a typical program time of 10 μs and 0.1 ms erasing time. Our results also show that dielectrics with very high permittivity ($\kappa > 25$) may not be necessary for the IPD in stacked-gate flash memories. On the other hand, the effect of high-κ TDs is quite contrary to the high-κ IPDs. Due to the reduced gate coupling ratio, the programming/erasing speed of stacked-gate flash memories with high-κ TDs by using FN tunneling is helpless in operation voltage reduction. Although the electric field on high-κ tunnel dielectrics is lower than SiO_2 tunnel oxide, enhanced impact ionization rate and lower barrier height contribute to higher CHE injection current and efficiency. Consequently, high-κ TDs are only effective for the memories programmed/erased with hot electron injection rather than FN tunneling. Due to the contrary programming/erasing schemes, high-κ IPDs and TDs are suitable for NAND- and NOR-type stacked-gate flash memories, respectively.

Finally, the effects of surface NH_3 nitridation of the bottom poly-Si film and PDA temperature on the electrical properties and reliability characteristics of RS and MOCVD high-κ inter-poly capacitors were evaluated. The polarity-dependent dielectric properties of RS Al_2O_3 IPD were strongly affected by the surface nitridation and the annealing temperature. For positive gate bias, IPD with NH_3 surface nitridation were found to significantly suppress the formation of an additional layer with lower dielectric constant during the post-annealing process and obtain a smoother interface, compared to those without nitridation treatment. Furthermore, the presence of a thin Si-N layer can make PDA more effective in eliminating traps existing in the as-deposited films and improve dielectric characteristics under negative

polarity. As a result, the smoother interface and smaller electron trapping rate contribute to the drastically reduced leakage current, enhanced breakdown field, and Q_{BD} of the RS Al_2O_3 inter-poly capacitors with surface NH_3 nitridation. Moreover, the electrical properties of RS Al_2O_3 IPD are heavily dependent upon the PDA temperature. The sample exhibits optimal quality in terms of leakage current, electron trapping rate and Q_{BD} when annealed at 900°C. X-ray photoelectron spectroscopy and Auger electron spectroscopy analyses have shown that this occurrence arises from the composition variations under different annealing conditions and excess oxygen, which can act as an electron trapping center, playing an important role in determining the IPD electrical properties. The results apparently demonstrate Al_2O_3 IPD with surface nitridation and optimized PDA temperature can effectively reduce charge transfer between CG and FG, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD. MOCVD Al_2O_3 and HfO_2 IPD are investigated in order to further promote Q_{BD} of RS Al_2O_3 IPD. The Q_{BD} can be significantly improved as well as reduced leakage current density, enhanced breakdown voltage and effective breakdown field by using MOCVD replacing RS. As thin as 5nm and 3nm EOT of Al_2O_3 and HfO_2 IPD is suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories, respectively.

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CHAPTER 1

Introduction

1.1 Background

The rapid progress of complementary metal-oxide-semiconductor (CMOS) integrated circuit technology since the late 1980's has enabled the Si-base microelectronics industry to simultaneously meet several technological requirements to fuel market expansion. These requirements include performance (speed), low static (off-state) power and a wide range of power supply and output voltages [1]. This has been accomplished by developing the ability to perform a calculated reduction of the dimensions of the fundamental active device in the circuit, following the "Moore's law", doubling about every two or three years since about 1980 [2]-[4]. The result has been a dramatic expansion in technology and communications markets including the market associated with high-performance microprocessors as well as low static-power applications, such as wireless systems.

It can be argued that the key element enabling the scaling of the Si-based metal-oxide-semiconductor field effect transistor (MOSFET) is the materials and resultant electrical properties associated with the dielectric employed to isolate the transistor gate from the Si channel for decades: silicon dioxide (SiO_2). The use of amorphous, thermally grown SiO_2 as a gate dielectric offers several key advantages in CMOS processing including a stable (thermodynamically and electrically),

high-quality Si-SiO_2 interface as well as superior electrical isolation properties. In modern CMOS processing, defect charge densities are on the order of 10^{10} cm^{-2}, midgap interface state densities are ~ 10^{10} $cm^{-2}eV^{-1}$ and hard breakdown fields of 15 MV/cm are routinely obtained and are therefore expected regardless of the device dimensions. These outstanding electrical properties clearly present a significant challenge for any alternative gate dielectric candidate [5], [6].

Over the years, there have been several major evolutions in silicon digital logic technology. CMOS technology has become the most popular digital logic technology for all IC industry, owing to its low standby power dissipation and scaling properties. Oxide thickness scaling has long been recognized as one of major keys for devices scaling. High drive current and thereby improved device performance can be achieved by reducing oxide thickness. It suggests that at the current rate of progress, Fig. 1.1 stresses the urgent need for a nitrided oxides (SiO_xN_y) and high dielectric constant (κ) gate dielectrics for low stand-by power application after the year 2002 and 2006, respectively [7]. Besides, the direct tunneling current increases exponentially by about one order of magnitude for every 0.2nm ~ 0.3nm reduction in oxide thickness. This additional leakage current not only causes increased power dissipation but also may affect the circuit functionality due to the decreased operation margins.

For this reason, several alternative materials for silicon dioxide are currently being investigated. Ultrathin nitrided oxides are the leading candidates to replace pure SiO_2 [8]-[14]. Figure 1.2 shows the expected equivalent oxide thickness (EOT) trends from the published 2003- ITRS roadmap. It suggests nitrided oxides can extend SiO_2 limitation to 2006 without massive change in production technologies. Nitrided oxides exhibit several properties superior to those of conventional thermal SiO_2, the more important being suppression of boron penetration from the poly-Si gate and enhanced

reliability. Nitrogen also reduces hot-electron-induced degradation [15]. The dielectric constant of the oxynitride increases linearly with the percentage of nitrogen from κ (SiO_2) = 3.9 to κ (Si_3N_4) = 7.8 [16], though one should note that most SiO_xN_y films grown currently by thermal methods are lightly doped with N (< 10 at.%) and therefore have a dielectric constant only slightly higher than that of pure SiO_2. The other potential candidates to replace silicon dioxide are high-κ materials, including aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) etc [17]-[20]. The most benefic for high-κ dielectrics is leakage current reduction by several orders of magnitude at the same EOT compared to SiO_2. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, including high thermal stability, high carrier mobility, small oxide charges, good stress immunity and CMOS compatible.

On the other hand, high-κ dielectrics are paid much attention on the flash memory applications [21]-[27]. The thickness of inter-poly dielectric (IPD) and tunnel dielectric (TD) in stacked-gate flash memory had meet intrinsic limitation [28]. It is not sufficient to meet the stringent data retention requirement of IPD while applying thermal or CVD oxynitride technologies due to the unavoidable leakage current [29]-[32]. By increasing the floating gate coupling ratio, high-κ IPD can lead to a high electric field across tunnel oxide (TOX) even at very low control gate voltage. For the tunnel dielectric engineering of stacked-gate flash memories, the issue is closely related to dielectric material selection itself. Flash tunnel dielectric has two roles. One is a barrier to suppress charge leakage under read and retention. Second role is a charge transfer path. In order to avoid trap-assisted tunneling via one trap site, the minimum TOX thickness of conventional FG structure will be limit to 8 nm. This limits the tunnel SiO_2 scaling and program/erase voltage reduction. Nitrided oxide

have been intensively studied, but so far only 5 to 10 times improvement for low field leakage is achieved [33]. This is not enough, because it only achieves 1 nm reduction even with heavy nitridation.

To successfully employ the high-κ IPD and TD into flash memory, one must take charge retention issues into consideration and make sure that the barrier height (φ_B) between Si and the new adopted high-κ dielectrics should be larger than 1.5eV for effectively suppressing the loss of floating gate charges through electron thermal emission [33]. Usually, dielectrics with higher κ inherently have lower φ_B. Therefore a trade-off between dielectric constant and barrier height is inevitably required in trying to implement the high-κ dielectrics in flash memories.

1.2 Motivation

Recent publications suggest that the performance of CMOS-based devices depends on both the concentration and distribution of the nitrogen atoms incorporated into the gate dielectric [9]-[11], [34]-[36]. For example, excessive nitrogen at the interface may reduce peak carrier mobility in the channel of MOSFETs and may allow boron accumulation in the oxide, which, in turn, may result in device instabilities [34]. One possibility is an SiO_xN_y film with two nitrogen-enhanced layers: first, nitrogen at or near the Si/SiO_xN_y interface to improve hot-electron immunity, and second, an even higher nitrogen concentration at the SiO_xN_y/polysilicon interface, as this is where it can best be used to minimize the penetration of boron from the heavily doped p^+ poly-gate electrode [37]. Thermal nitridation of SiO_2 in nitric oxide (NO) or nitrous oxide (N_2O) is a commonly used method to incorporate nitrogen near the interface

[37]-[39]. Although N_2O processing similarity to O_2 permits N_2O to replace oxygen in oxidation reactors/furnaces, oxynitridation in N_2O is complicated by the fast gas-phase decomposition of the molecule into N_2, O_2, NO and O at typical oxidation temperatures, 800 - 1100^oC [13]. Therefore, NO-annealing of an initial oxide is preferred to prepare nitrided oxide with sufficient concentration in a reasonable thermal cycle [9], [14], [36], [39]. Compared to N_2O, oxynitridation in NO results in more nitrogen incorporation at equivalent temperatures [9], [40], [41]. In addition, NO oxynitrides exhibit lower leakage currents and interface defect densities, as well as improved electrical stress properties [9], [36], [40]. On the other hand, system-on-a-chip has gradually become the trend of CMOS technologies. As a result, circuit architecture and material reliability are both mixed into the design consideration. In these applications, minimizing process steps and forming thermally stable dual oxide thickness CMOSFETs are essential. One of the ways for reducing the number of process steps is to implant nitrogen into Si substrate in order to obtain two gate oxide thickness on the same thermal cycle [42], [43].

Recently, aluminum oxide (Al_2O_3) [17], [44]-[46] and hafnium oxide (HfO_2) [20], [47]-[50] had been proved as promising candidates for the gate dielectrics of sub-0.1 μm device due to their higher κ, relatively high φ_B and superior thermal stability, shown in Table 1.1. Thanks to the high dielectric constant and high thermal stability, Al_2O_3 and HfO_2 are suitable to be integrated into stacked-gate flash memories. Nonetheless, the effects of these kinds of high-κ dielectrics on flash memories are seldom investigated. To further realize the dielectric properties of these high-κ dielectrics, some reliability issues such as breakdown field, charge trapping and temperature-dependence behaviors are extensively studied for both gate dielectric and flash memories applications.

1.3 Organization of the Dissertation

There are nine chapters in this dissertation. Chapter 1 shows the background and motivation for the application of the ultrathin nitrided oxides and high-κ dielectrics.

In Chapter 2, the reliabilities of sub-3nm nitrided oxides formed by NO-annealing are shown. In our study, N atomic concentration is shown to depend on the initial oxide thickness, i.e., concentration increases as oxide thickness decreases, which was desired for the improvement of dielectric reliability in the ultra-thin thickness region. NO-annealing can achieve better SILC immunity for both constant voltage and constant current stress. Moreover, NO-annealing also improves interface smoothness and results in tighter TDDB distribution.

In Chapter 3, the reliabilities of sub-3nm nitrided oxides formed by nitrogen-implanted silicon substrate (NIS) are investigated. NIS dosage less than 1×10^{14} cm^{-2} is helpless to oxidation rate suppression and degrades dielectric reliability simultaneously. On the contrary, samples with 1×10^{15} cm^{-2} NIS not only can use to grow multiple oxide thickness to meet SOC requirement, but also improve stress immunity apparently. Nitrogen implantation also generates a uniform distribution nitrogen profile in the dielectric bulk, which can be used as an effective diffusion barrier to resist boron penetration. In conclusion, both NO-annealed and NIS nitrided oxides can improve dielectric reliability and are suitable to replace traditional SiO_2 at 0.13μm and beyond.

In Chapter 4, the program/erase performance of stacked-gate flash memory with high-κ IPDs and SiO_2 TOX are compared to ONO IPD. From MEDICI simulation, Al_2O_3 IPD and HfO_2 IPD can increase gate-coupling ratio by 45% and 92%,

respectively. By 2-D MEDICI simulation, flash memories with high-κ IPD clearly exhibit significant improvement in programming/erasing speed over those with conventional ONO IPD. Moreover, it is found that high-κ IPD is more effective for the memories programmed/erased with Fowler-Nordheim (FN) tunneling rather than channel hot carrier (CHE) injection. Choosing HfO_2 as the IPD and using FN programming/erasing scheme, the operating voltage can be reduced 48% at a typical program time of 10 μs and 0.1 ms erasing time.

In Chapter 5, the program/erase performance of stacked-gate flash memory on the κ-value of tunnel dielectric are studied. The effect of high-κ TD is quite different with high-κ IPD. Due to the reduced gate coupling ratio, the programming/erasing speed of stacked-gate flash memories with high-κ TD by using FN tunneling is helpless in operation voltage reduction. On the other hand, the increased electric field on HfO_2 IPD would produce excess charge loss and narrow the operation window between programmed and erased state. Although the electric field on high-κ tunnel dielectrics is lower than SiO_2 TOX, enhanced impact ionization rate and lower electron barrier height contribute to higher CHE injection current and efficiency. Consequently, high-κ TD is more effective for the memories programmed/erased with hot electron injection rather than FN tunneling. Due to the contrary improvement in programming/erasing schemes, high-κ IPD and TD is suitable for next-generation NAND and NOR type stacked-gate flash memories, respectively.

In Chapter 6, the effects of surface ammonia (NH_3) nitridation on inter-poly characteristics of reactive-sputtered (RS) Al_2O_3 dielectrics are evaluated. With surface NH_3 nitridation, the formation of an additional layer with lower dielectric constant during post-annealing process can be significantly suppressed and reduced, compared to that without nitridation treatment. Furthermore, the presence of a thin Si-N layer

can make post-deposition annealing more effective in eliminating traps existing in the as-deposited films. As a result, a smoother interface and smaller electron trapping rate can contribute to the drastically reduced leakage current, enhanced breakdown field and Q_{BD} of Al_2O_3 interpoly capacitors with surface NH_3 nitridation for both polarities.

In Chapter 7, the effects of post-deposition annealing (PDA) temperature on inter-poly characteristics of RS Al_2O_3 dielectrics are examined. It was found that the electrical properties of Al_2O_3 IPD strongly depend upon the PDA temperature. 900°C annealing is the best condition for the Al_2O_3 IPD electrical characteristic in terms of leakage current, electron trapping rate and charge-to-breakdown. The XPS and AES analyses indicate that this consequence is closely related to the compositional changes and excess oxygen concentration when changing annealing temperature. The results apparently demonstrate Al_2O_3 IPD with surface nitridation and optimized PDA temperature can effectively reduce charge transfer between CG and FG, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD.

In Chapter 8, thickness scaling down and reliability promotion of next-decade suitable IPD are inspected. The results clearly indicates high-κ IPDs, regardless of deposition tools, exhibits high potential to replace TEOS IPD. Moreover, MOCVD deposition demonstrates significant reliability improvement compared to RS deposition. As thin as 5nm and 3nm EOT of MOCVD-deposited Al_2O_3 and HfO_2 IPD is suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories, respectively.

Finally, in Chapter 9, the conclusions are made and the recommendation describes the topics which can be further researched.

Table 1.1 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2 and HfO_2.

	High-κ Dielectrics		
	Al_2O_3	**ZrO_2**	**HfO_2**
Bandgap (eV)	**8.3**	**5.82**	**6.02**
Barrier Height to Si (eV)	**2.9**	**1.5**	**1.6**
Dielectric Constant	**9**	**~ 25**	**~ 25**
Heat of Formation (Kcal/mol)	**399**	**261.9**	**271**
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	**63.4**	**42.3**	**47.6**
Thermal expansion coefficient (10^{-6} $^oK^{-1}$)	**6.7**	**7.01**	**5.3**
Lattice Constant (Å) (5.43 Å for Si)	**4.7 - 5.2**	**5.1**	**5.11**
Oxygen Diffusivity at 950°C (cm^2/sec)	**5×10^{-25}**	**1×10^{-12}**	

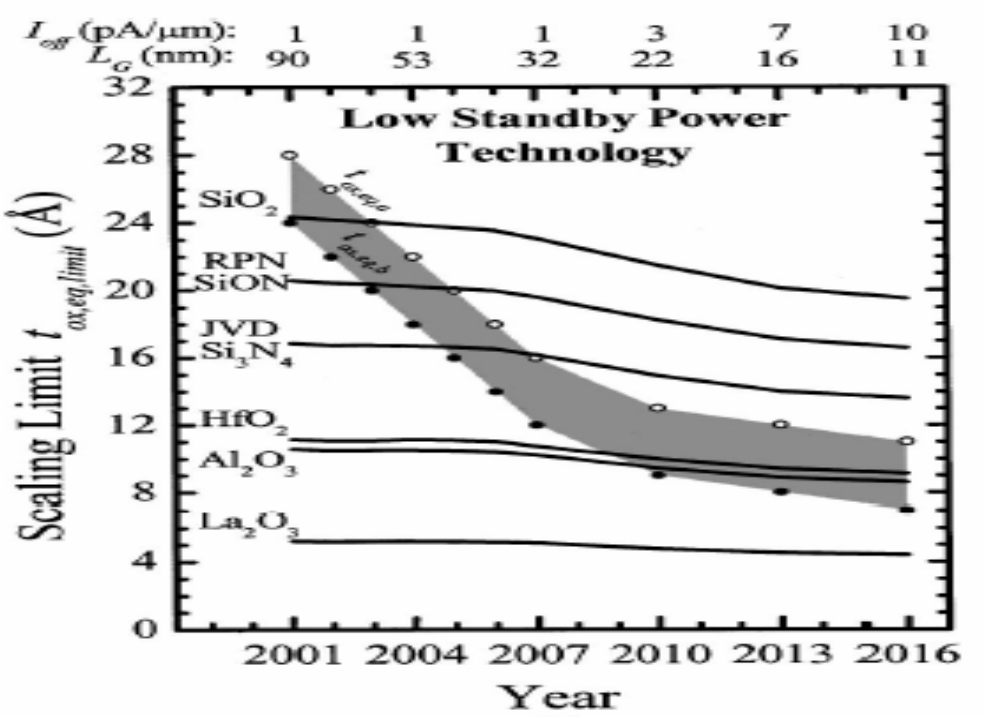


Fig. 1.1 Scaling limits of various gate dielectrics as a function of the technology specifications for low stand-by power technologies [Ref. 7].

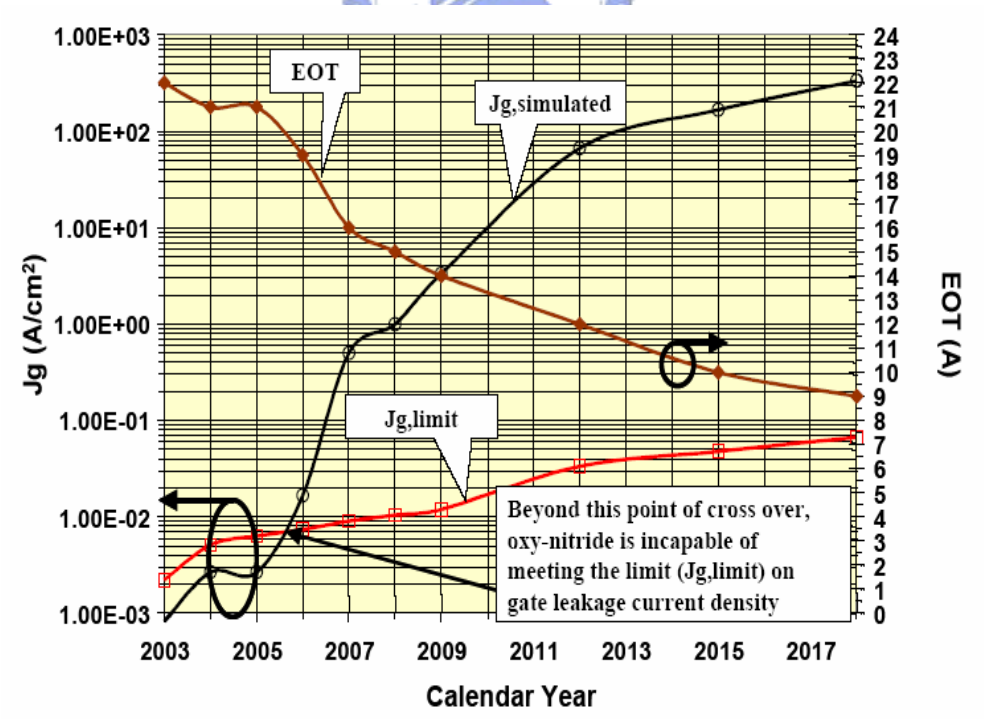


Fig. 1.2 Leakage current density and EOT projection of nitrided oxides from ITRS roadmap 2003.

CHAPTER 2

Characteristics and Reliabilities of Sub-3nm High Temperature NO-Annealed Nitrided Oxides

2.1 Introduction

In order for a MOSFET to behave as a transistor, the gate must exert greater control over the channel than the drain does, i.e., the gate to channel capacitance must be larger than the drain to channel capacitance. A simple model suggests

$$L_{\min} \alpha \ T_{ox} \times X_j^{1/3} \qquad (2\text{-}1)$$

The scaling limit of T_{ox} is therefore of paramount importance. Besides suppressing the short channel effect, reducing T_{ox} improves drive current and generally but not always raises circuit speed.

The continuous shrinkage of device dimensions below a quarter-micron requires highly reliable ultra-thin dielectric films. In this thickness range, not only breakdown but also wearout of dielectric films is one of the key technological issues. As an alternative gate dielectric, nitrided oxides have drawn considerable attention due to their superior performance and reliability properties over conventional SiO_2 [12]-[14], [51]-[56]. On possible approach to form nitrided oxides was post-oxidation annealing, including ammonia (NH_3), nitrous oxide (N_2O) and nitric oxide (NO) annealing. NH_3 annealing will incorporate too large amount nitrogen into the gate oxide to reduce

carrier mobility, but simultaneously incorporate large amount of hydrogen into which will degrade hot carrier immunity [51]-[53]. N_2O-annealing is another candidate for nitrogen incorporation, but requires a much higher thermal budget for sufficient nitrogen incorporation [12], [13], [54]. As a result, NO-annealing of an initial oxide is preferred to prepare nitrided oxide with sufficient concentration in a reasonable thermal cycle, considering the self-limiting nature of the growth proves in an NO ambient [13], [14], [55], [56].

In this chapter, characteristics and reliabilities of NO-annealed nitrided oxides are studied. Although NO-annealing will induce significant flat-band voltage shift and increase of the interface state density due to the pile-up of nitrogen near the interface, incorporation of nitrogen still can effectively suppress trap generation and improve time-to-breakdown and charge-to-breakdown.

2.2 Experiment Details

LOCOS isolated MOS capacitors were fabricated on p-type (100) silicon wafers. After forming LOCOS isolation, wafers were cleaned and HF dipped before oxidation. The gate dielectrics were grown at 750^{o}C followed by either NO or N_2 annealing at 850^{o}C for an hour. Then 1500Å polysilicon was deposited with in-situ doped phosphorus of 2.5×10^{20} cm^{-3}. Dopants were then activated at 950^{o}C for 30sec. After gate electrodes patterned and contact holes etched, aluminum metallization was done followed by sintering at 450^{o}C in N_2 ambient.

Square or circular capacitors of different areas, ranging from 2.5×10^{-5} to 1×10^{-2} cm^2, with LOCOS isolation are used to evaluate the gate oxide integrity. The physical

gate oxide thickness was determined by spectroscopic ellipsometer and compared with high-resolution transmission electron microscopy (HRTEM). The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under an accumulation condition with quantum mechanical correction. The tunneling leakage current density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP4145A. Nitrogen depth profiles and compositions were analyzed by secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS). The micro-roughness of the wafer surface and the interface between nitrided oxides/silicon were detected by atomic force microscopy (AFM).

2.3 Results and Discussions

2.3.1 Accurate Models for Oxide Thickness Extraction

To meet the device requirement of the deep-submicron generation, the gate oxide thickness must be scaled down below 30Å. However, as oxide thickness scaled below 30Å, traditional *C-V* method is more and more difficult to extract the accurate oxide thickness due to large direct tunneling current and quantum confinement effect. There are several reports used to extract the physical oxide thickness [57]-[61]. Oxide thickness extraction using different methods was summarized in Table 2.1.

2.3.1.1 Corrected Two-Frequency Method for High Leakage Dielectrics

Figure 2.1 shows *C-V* curves of 19Å NO-annealed GOX under 10kHz, 50kHz

and 100kHz measurement, a clear frequency dispersion was observed at the strong accumulation region due to series resistance ignoring [57]. Since capacitance is proportional to $1/f^2$, higher measurement frequency will decrease oxide capacitance. For example, 19Å NO-annealed GOX shows a 5% decrease in gate capacitance with 50kHz and 15% decrease with 100kHz, both comparing to 10kHz. The accurate model published by C.Hu [57] can eliminate this frequency-dependent capacitance measured at two different frequencies using (2-2) :

$$C = \frac{f_1^2 C_1^{'}(1+D_1^{'2}) - f_2^2 C_2^{'}(1+D_2^{'2})}{f_1^2 - f_2^2} \qquad (2\text{-}2)$$

where $C_1^{'}$, $D_1^{'}$ refer to the capacitance and dissipation factor ($\frac{G}{2\pi fC}$) measured at the frequency f_1 and $C_2^{'}$, $D_2^{'}$ refer to the capacitance and dissipation factor measured at the frequency f_2 , respectively. Inset also shows the *C-V* curves after modification, dispersion between three frequencies was disappeared. Unless stated otherwise, all *C-V* curves used in this report are the modified 50kHz-100kHz curve.

2.3.1.2 Quantum Confinement Effect Correction

As the channel length shrink, oxide thickness must be scaled to avoid severe short channel effect. However, when oxide thickness becomes thinner and the electric field becomes stronger, quantum confinement effect becomes more and more critical in the oxide thickness extraction. Quantum effect occurs when the vertical electric field is large enough to confine conduction carriers into the potential well at the surface, generates discrete band diagram. Since the capacitor structure was used in our experiments, only accumulation charge centroid is needed to be calculated. According

to [58], charge centroid at strong accumulation region (X_{acc}) can be calculated using eq. (2-3) :

$$X_{acc} = \frac{X_2}{1+\left\{\frac{|\ V_G - V_{FB}\ |}{[\ 0.02\ (\ T_{phys} + T_{\Delta}\ )]}\right\}^{0.6}} \qquad (2\text{-}3)$$

where T_{Δ} is determined to be 6Å from quantum simulation using heavily doped silicon, T_{phys} is the physical oxide thickness, X_2 = 10.8 for electrons and X_2 = 13.5 for holes. V_{FB} used in eq. (2-3) is roughly -1V since n^+ polysilicon gate electrode and p-type substrate are used. After fitting *C-V* (calculated from 50kHz-100kHz *C-V* curve) with X_{acc}, T_{phys} (named QMCV) can be calculated as shown in Table 2.1.

Figure 2.2 compares the EOT and QMCV thickness extracted at V_G = -2V of NO- and N_2-annealed GOX. The difference can be calculated by the following expression:

$$\text{NO-annealed GOX}: \quad \Delta T_{ox} = -0.03\ T_{TEM} + 7.5 \ \ (\text{Å}) \qquad (2\text{-}4)$$

$$N_2\text{-annealed GOX}: \quad \Delta T_{ox} = -0.05\ T_{TEM} + 8.1 \ \ (\text{Å}) \qquad (2\text{-}5)$$

where T_{TEM} refers to the physical oxide thickness from HRTEM. The difference is about 7~8Å due to the quantum confinement effect. Otherwise, as oxide thickness decreases, the difference between EOT and QMCV will be more obvious since X_{acc} will contribute more significant portion in total oxide thickness. In addition, the model mentioned above is published for pure oxide, i.e., N_2-annealed GOX in our experiment. It would be a little change in parameters fitting with nitrided oxide. Furthermore, post-oxidation NO-annealing will incorporate additional nitrogen into GOX and slightly increase the dielectric constant (κ) from 4.0 to 4.2.

2.3.1.3 Extract T_{ox} using Accumulation Direct-Tunneling Currents

As oxide thickness shrinkage down to the direct-tunneling region, tunneling current will strongly dependent on the oxide thickness [62]. For example, tunneling current will be increased by 10 times as oxide thickness decreases from 22Å to 20Å. Therefore, using direct-tunneling current to extract oxide thickness becomes feasible solution. Since gate current in inversion mode is strongly dependent on the poly depletion effect (polysilicon doping concentration) and threshold shifts (substrate doping condition), using inversion gate current to determine oxide thickness becomes more difficult [59]. On the other hand, using accumulation gate current to determine oxide thickness is much easier since it will be independent on the poly depletion and the substrate condition. As a result, a simple model can be used to evaluate T_{ox} from accumulation gate current at different gate bias, (named DTIV):

$$\text{For } V_G = -1.5V: \quad T_{ox} = \frac{[10.1 - \log(J_G)]}{6.2} \tag{2-6}$$

$$\text{For } V_G = -1V: \quad T_{ox} = \frac{[9.6 - \log(J_G)]}{6.5} \tag{2-7}$$

where J_G is the accumulation gate current density united A/cm^2 and T_{ox} united nm.

Figure 2.3 compares the physical oxide thickness extracting from QMCV and DTIV method with TEM thickness as the reference. As the oxide thickness thicker than 30Å, DTIV would become improper since the Fowler-Nordheim tunneling starts to contribute the leakage current, and the current dependence on oxide thickness becomes significantly weaker than direct-tunneling dominant region. Except for 30Å gate oxide, both the extracted QMCV and DTIV thicknesses reveal highly agreement with the TEM physical thickness.

2.3.2 Basic Characteristics of Sub-3nm NO-Annealed Nitrided Oxides

As shown in Table 2.1, NO-annealed GOX always had thinner EOT and QMCV thickness than N_2-annealed GOX. Since NO-annealing will incorporate nitrogen into gate oxide and pile- up at SiO_2/Si-sub interface [62]-[64], this will slightly increase the dielectric constant and result in thinner oxide thickness.

Figure 2.4 compares the magnitudes of direct tunneling current of both 19Å and 22Å N_2- and NO-annealed GOX. The samples with NO-annealing do not introduce higher leakage current density than the control samples at higher electric field. In addition, small current peak can be observed in gate oxides due to traps assisted tunneling (TAT) at E < 1 MV/cm. After filling of the existed neutral traps with electrons, tunneling current will drop and return to the direct tunneling behavior. Figure 2.5(a) compares the normalized *C-V* curves of N_2- and NO-annealed GOX. Slightly stretch-out and negative flat-band voltage shift (ΔV_{FB}) is observed for the samples with NO-annealing, which can be observed more clearly in Fig. 2.5(b).

Figure 2.6(a) shows XPS nitrogen distribution profiles of nitrided oxides after NO-annealing by XPS analyses. N is preferably piled up at the Si/dielectric interface with $Si_3{\equiv}N$ bonds [65], [66]. Due to lower electronegativity of N compared to O, N incorporation causes an increase in positive fixed charges and thereby, lowers the V_{FB}. Moreover, nitridation also increases interface state densities due to $Si_3{\equiv}N$ bonding [62]. Figure 2.6(b) indicates the dependence between nitrogen peak concentration and initial oxide thickness. As the oxide thickness decreases, nitrogen will be incorporated more efficient because of less diffusion distance of NO gas [64]. Consequently, one can use the initial oxide thickness to control the peak nitrogen concentration at the same annealing condition. Moreover, as the oxide thickness less than 20Å, 850^{o}C 60min NO-annealing may incorporate too much nitrogen and reduce carrier mobility

significantly. As a result, reduced thermal budget is necessary for such ultra-thin gate oxide annealing from device performance point of view. Table 2.2 summarizes V_{FB} and D_{it} extracted from *C-V* curves and in-line Quantox non-contact *C-V*, respectively. The results clearly indicate both ΔV_{FB} and ΔD_{it} increases as decreasing initial oxide thickness, which is strongly affected by nitrogen concentration, under the same post-oxidation NO-annealing.

2.3.3 Reliability Characteristics of Sub-3nm NO-Annealed Nitrided Oxides

As the oxide thickness scales to the direct tunneling region, stress-induced leakage current (SILC) will become less and less significant because of insufficient energy of tunneling electrons, which will results in lower trap generation rate. In our experiment, all oxides had been measured using both constant voltage stress (CVS) and constant current stress (CCS). Figure 2.7 shows the *J-V* curves of 19Å gate oxides after -3.8V CVS for 100sec. The *J-V* curves of 22Å gate oxides after -4V CVS for 100sec is seen in Fig. 2.8(a). The most current increment after constant voltage stress occurs near -1V, i.e. flat-band voltage [67]. Since stress will generate extra interface state and bulk electron traps, leakage current will increase through tunneling via these traps. As the gate voltage increases from 0V to V_{FB}, more and more amount of interface states are available for the electron tunneling from the gate after stress, thus more current increment is observed. As shown in the Fig. 2.7 and 2.8, both NO-annealed GOX have higher stress immunity than N_2-annealed GOX which can be attributed to the formation of stronger $Si_3{\equiv}N$ bonds near the SiO_2/Si-substrate interface [62]-[64], [68]. Figure 2.8(b) compares hole trapping rate during CVS. It should be reminded that as the oxide thickness thinner than 50~60Å, only hole trapping can be observed during stress [63], [64], [68]. During voltage stress, the gate

current monotonic increase over time clearly indicates that only the hole trapping is occurred. NO-annealed GOX can effectively suppress hole trapping rates during CVS.

For going into details about reliability phenomenon, Fig. 2.9 demonstrates maximum trap generation rates (G_{trap}) under both CVS and CCS with various injection charges used to compare the oxide quality of 22Å N_2-annealed and NO-annealed GOX. The relationship between G_{trap} and injection charges are parabolic, SILC will increase more rapidly and then tends to saturate until breakdown occurs. Regardless of constant voltage or current stress, NO-annealed GOX can effectively eliminate hole trapping generation compared to N_2-annealed GOX due to stronger $Si_3{\equiv}N$ bonding, which is consistent with Fig. 2.8(b). Figure 2.10(a) compares the TDDB characteristics of 19Å and 22Å gate dielectrics stressed at -4.3V constant voltage stress. After Weibull plotting, NO-annealed GOX exhibits better t_{BD} (time-to-breakdown) compared to N_2-annealed GOX. The 63% accumulative failure rate for 19Å N_2- and NO-annealed GOX are 149sec and 518sec, respectively. NO-annealed GOX improves larger than 3 times of t_{BD} than N_2-annealed GOX. While increasing initial oxide thickness to 22Å, the 63% accumulative failure rate for NO- and N_2-annealed GOX are 1600sec and 683sec, respectively. t_{BD} improvement becomes smaller than thin oxide, but still larger than 2 times. Q_{BD} Weibull distribution of 22Å gate dielectrics stressed at -20 mA/cm^2 constant current stress is shown in Fig. 2.10(b). The 63%-failure Q_{BD} for NO- and N_2-annealed GOX are 42.4 C/cm^2 and 16.1 C/cm^2, respectively. NO-annealing not only improves Q_{BD} larger than 2 times but also results in larger Weibull distribution slope (β) under CCS, consistent with CVS results. The HRTEM images of N_2- and NO-annealed GOX, as seen in Fig. 2.11, reveal NO-annealing can help to smooth interface roughness and reduce interfacial layer (IL) thickness [69], as well as forming stronger $Si_3{\equiv}N$ bonding, we expect post-oxidation

NO-annealing will effectively improve dielectrics reliability characteristics.

Figure 2.12 compares β as function of dielectric thickness and stress voltage. β decreases with decreasing oxide thickness and increasing stress voltage [70]-[72]. In thin oxides, the conductive breakdown path consists of only a few traps and consequently there is a large statistical spread on the average density to form such a short path. In thick oxides, the breakdown path consists of a larger number of traps, and the spread on the trap density need to generate such a large path is smaller. This means that β as a function of oxide thickness is an intrinsic property of the degradation and breakdown mechanism. On the other hand, increasing stress voltage accelerates trap generation and has higher probability of forming conductive breakdown path. Moreover, NO-annealing also enhances β due to smoother interface and stronger $Si_3{\equiv}N$ interface bonding. Figure 2.13 predicts the 10-year lifetime using 63% accumulative failure rate. Thanks to N incorporation, 19Å and 22Å NO-annealed nitrided oxides can sustain 10-year stressing time at V_G = -2.5V and -2.8V, respectively, which can meet 0.15μm requirement [73]. Voltage acceleration factor (γ) is also increased for NO-annealed nitrided oxides, as shown in the inset.

2.4 Summary

According to SIA roadmap, the oxide thickness smaller than 20Å is necessary for deep sub-quarter micron devices. However, pure SiO_2 can not meet the requirement due to the large tunneling current. In our study, N atomic concentration is shown to depend on the initial oxide thickness, i.e., with decreasing oxide thickness from 63Å to 22Å, the N concentration increases from 2.12 to 4.45 at.% in the interface, which was desired for the improvement of dielectric reliability in the

ultrathin region. NO-annealing can achieve better SILC immunity for both constant voltage and constant current stress. Moreover, NO-annealing also improves interface smoothness and results in tighter TDDB distribution. Even after process optimization in the future, NO-annealing can be used to improve device performance more apparent, as predicting in mind. Although boron penetration is lack in our project, many studies have been shown the improvement of NO-annealing on pMOSFET performance. As a result, NO-annealed nitrided oxides can improve dielectric reliability and are suitable to replace traditional SiO_2 at 0.13μm and beyond.

Table 2.1 Comparison of thickness extraction from various methods of NO- and N_2-annealed GOX.

	Rudolph	DTIV		QMCV	TEM	Quantox	EOT
		-1V	-1.5V	@ -2V			@ -2V
NO-30Å	30.6Å	25.7Å	25.4Å	33.9Å	33.7Å	33.7Å	42.0Å
NO-22Å	21.5Å	26.1Å	25.3Å	24.9Å	25.8Å	28.2Å	32.0Å
NO-19Å	19.7Å	24.6Å	23.3Å	22.6Å	23.8Å	24.7Å	27.5Å
N_2-30Å	30.7Å	28.1Å	29.6Å	36.0Å	35.7Å	37.9Å	44.3Å
N_2-22Å	22.7Å	26.8Å	25.5Å	26.3Å	27.3Å	29.8Å	33.6Å
N_2-19Å	18.9Å	25.3Å	24.2Å	25.2Å	26.3Å	27.4Å	32.4Å

Table 2.2 Flat-band voltages and interface state densities of NO- and N_2-annealed GOX.

T_{OX} \ V_{FB}	NO-GOX (V)	N_2-GOX (V)	ΔV_{FB} (mV)
30Å	-1.065	-1.052	-13
22Å	-1.085	-1.055	-30
19Å	-1.104	-1.06	-44

T_{OX} \ D_{it}	NO-GOX (V)	N_2-GOX (V)	ΔD_{it} (cm^{-2} eV^{-1})
30Å	6.31×10^{11}	5.47×10^{11}	0.84×10^{11}
22Å	7.06×10^{11}	4.88×10^{11}	2.18×10^{11}
19Å	8.66×10^{11}	4.59×10^{11}	4.07×10^{11}

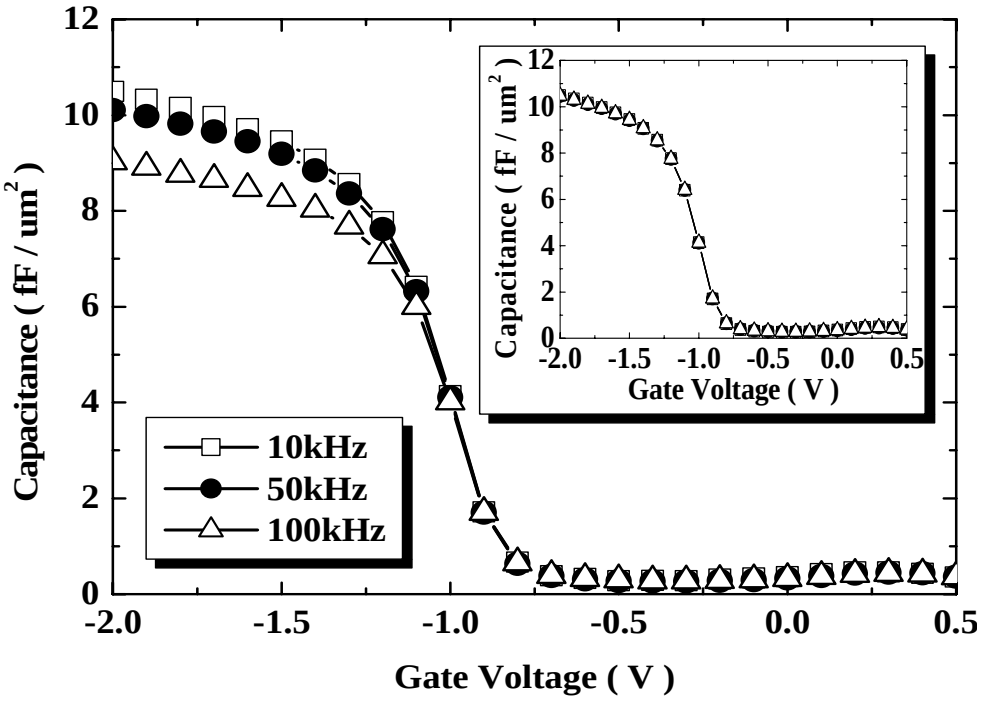


Fig. 2.1 The *C-V* curves of the 19Å NO-annealed GOX. Inset shows corrected *C-V* curves by two-frequency method.

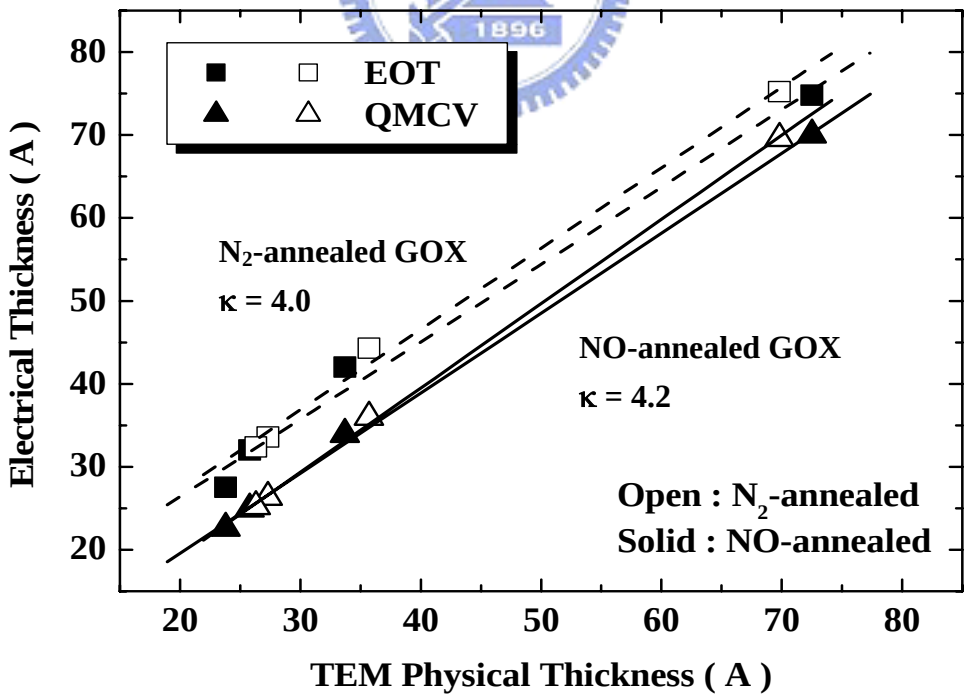


Fig. 2.2 Extracted dielectric constants of NO- and N_2-annealed GOX. NO-annealed GOX has higher dielectric constant than N_2-annealed GOX.

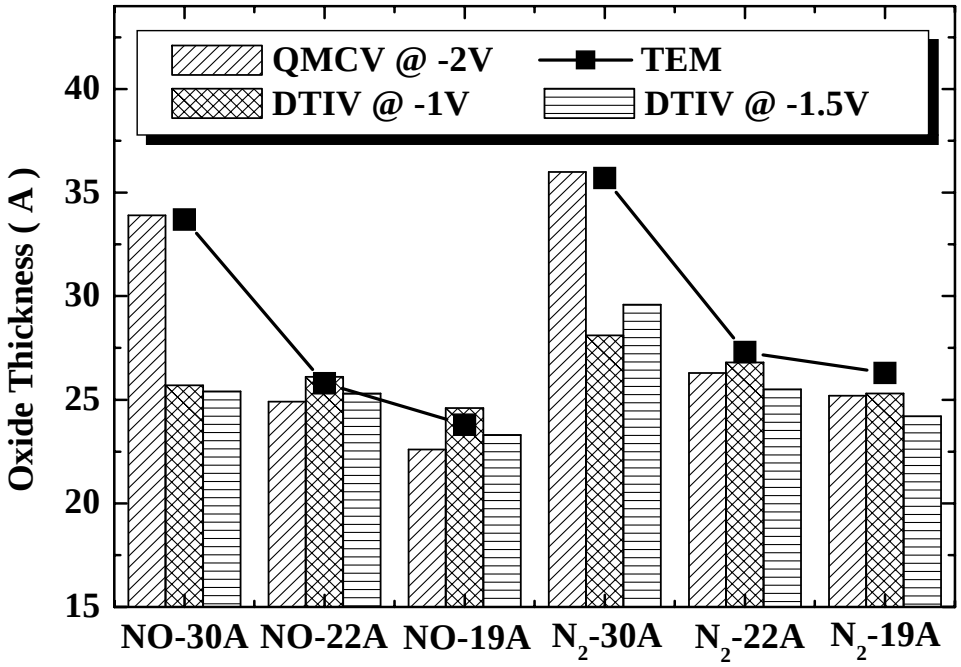


Fig. 2.3 Extracted oxide thickness variations between DTIV and QMCV of NO- and N_2-annealed GOX. Both DTIV and QMCV thickness show highly agreement with TEM thickness.

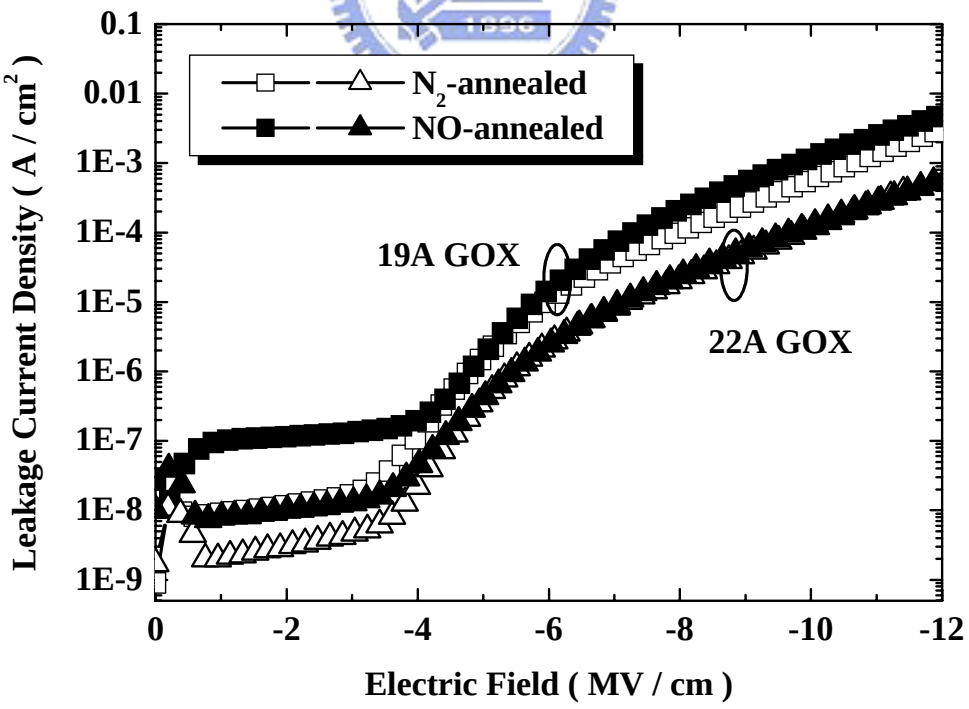
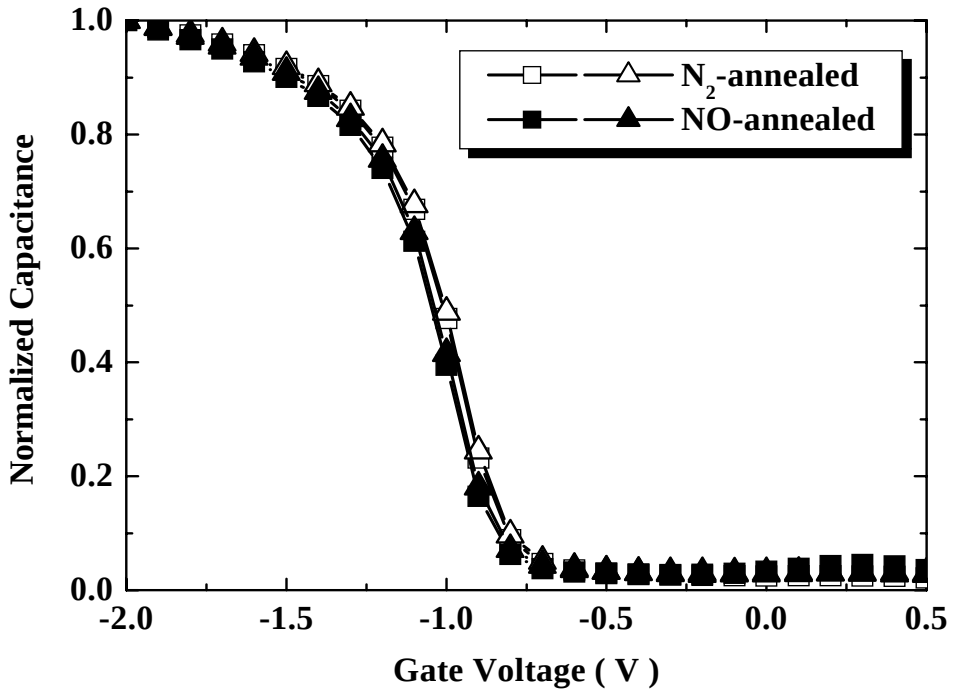
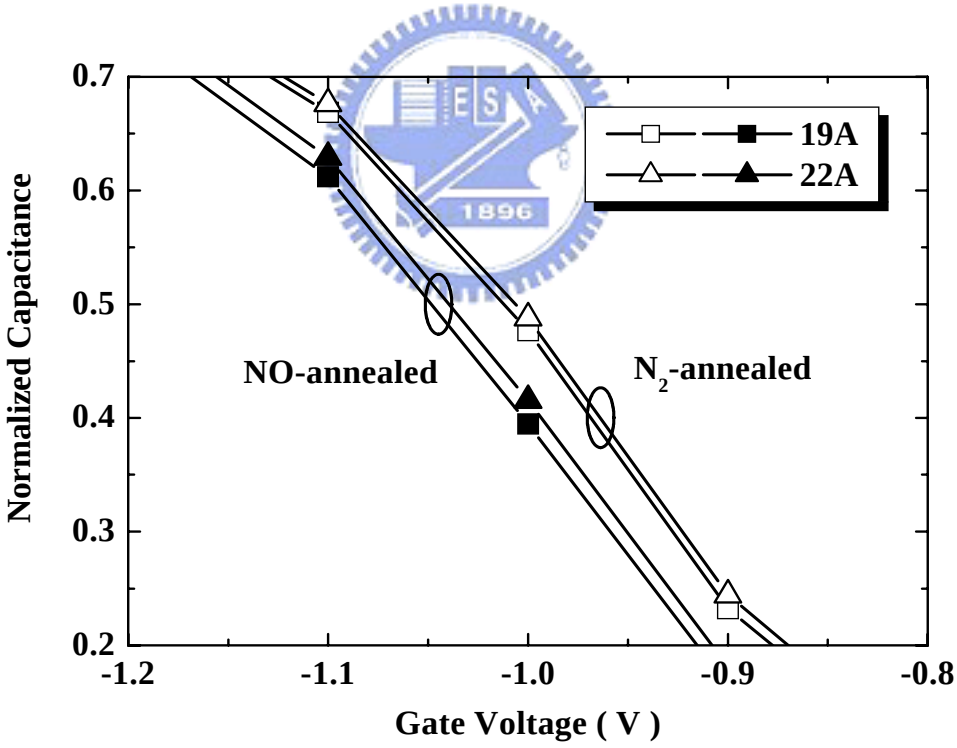


Fig. 2.4 Direct tunneling current density of 19Å and 22Å NO- and N_2-annealed GOX. NO-annealing does not deteriorate leakage current.

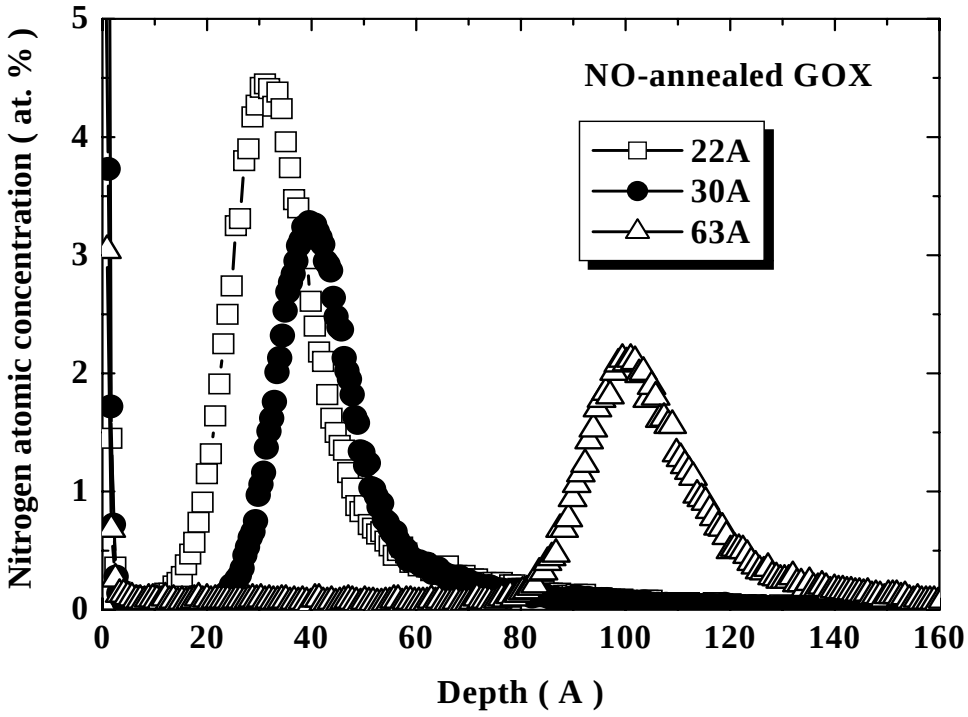


(a)

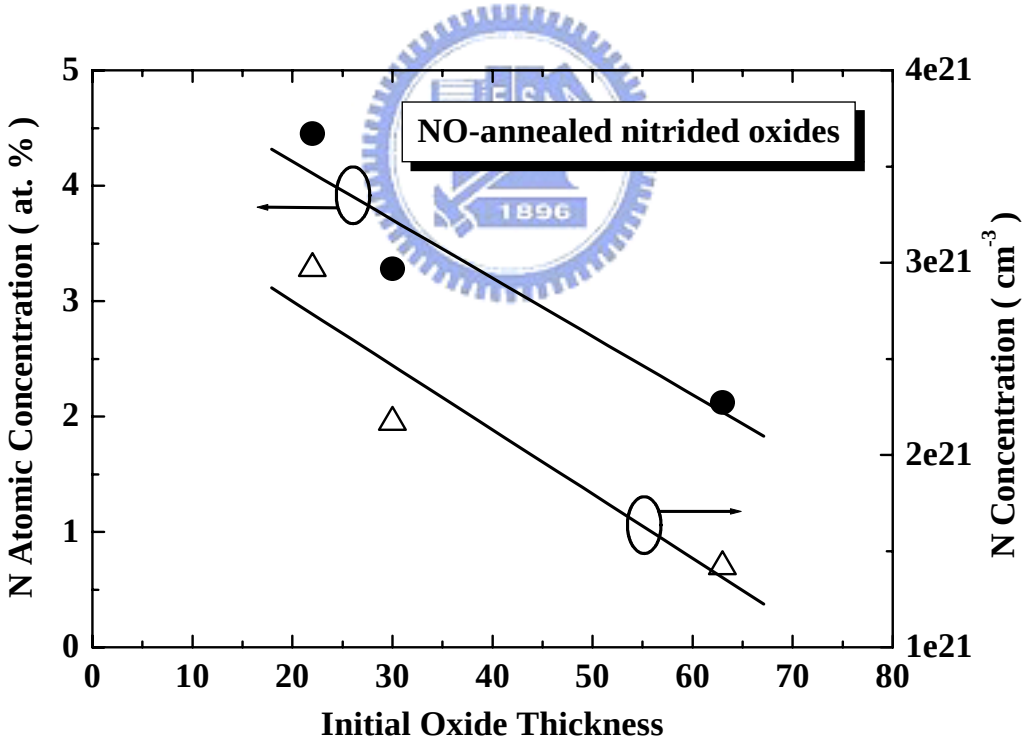


(b)

Fig. 2.5 (a) Normalized *C-V* curves of 19Å and 22Å NO- and N_2-annealed GOX. (b) Magnify (a) for clearly comparison between NO- and N_2-annealed GOX. NO-annealing exhibits negative flat-band voltage shift and slightly increases interface state density.



(a)



(b)

Fig. 2.6 (a) XPS nitrogen depth profiles (b) nitrogen peak concentrations of NO-annealed nitrided oxides varied with initial oxide thickness. NO-annealing piles-up nitrogen near the interface and more N incorporates as oxide thickness decreasing.

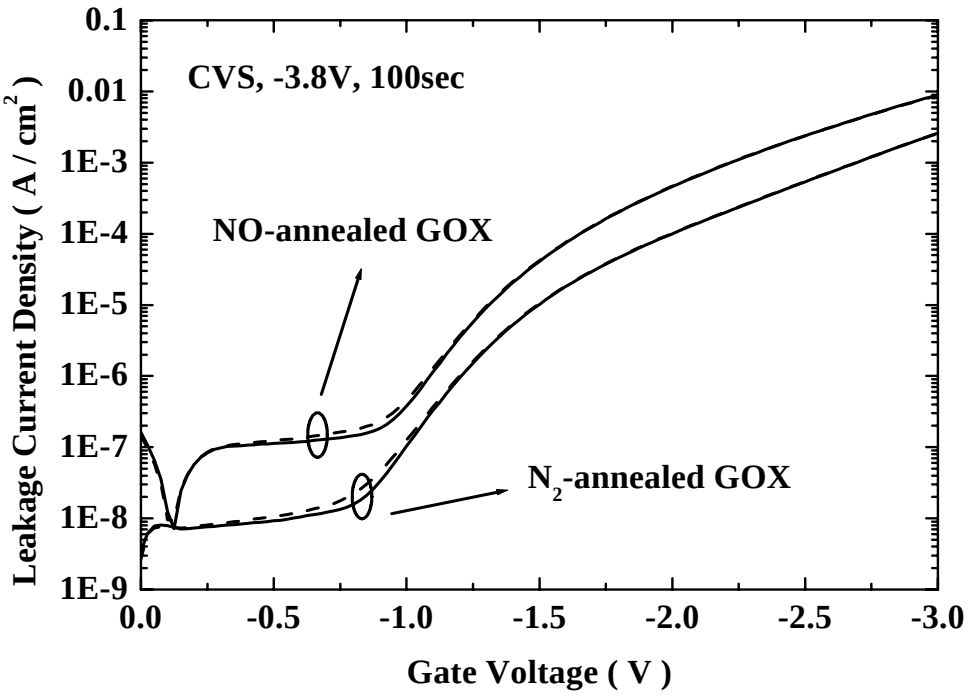
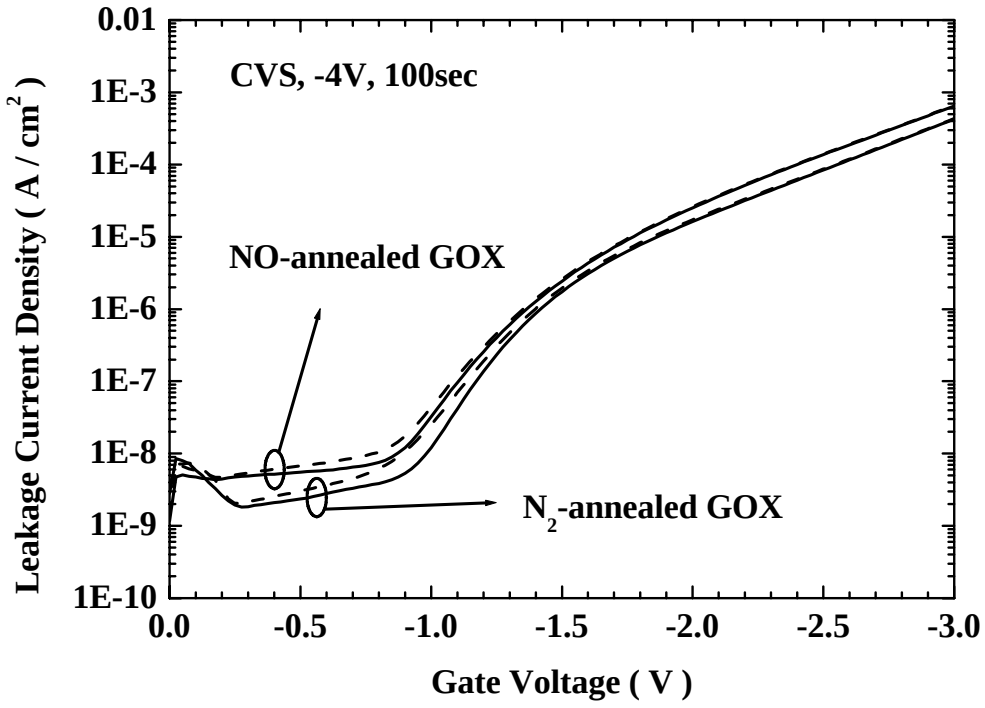
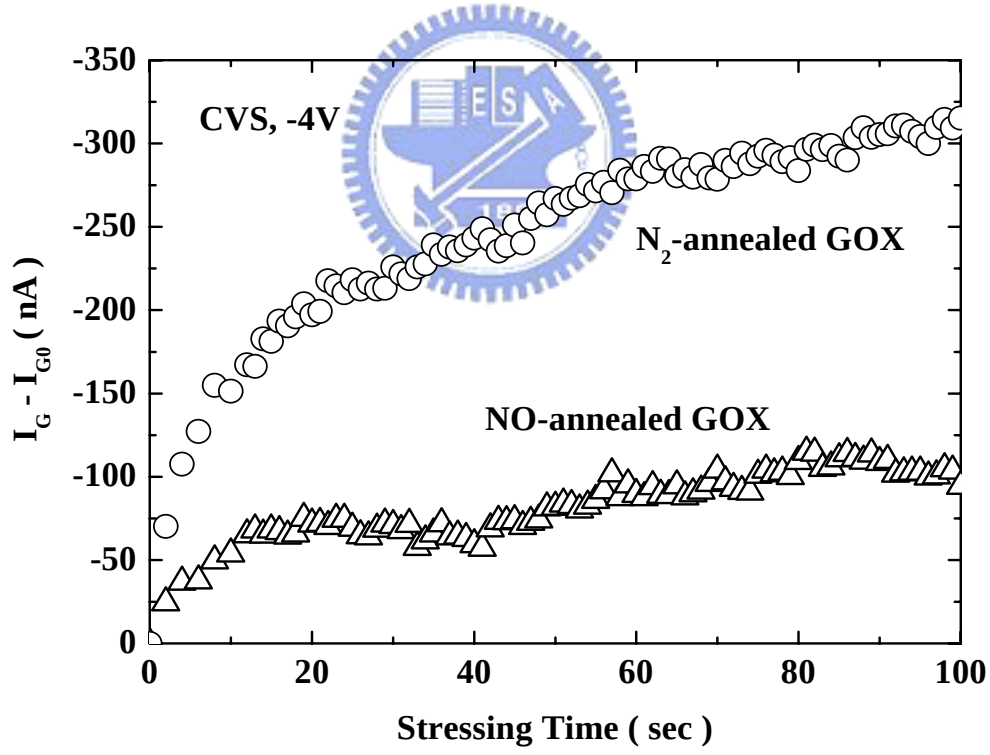


Fig. 2.7 SILC characteristics of 19Å NO- and N_2-annealed GOX at -3.8V CVS for 100sec. Maximum current increment after CVS occurs near flat band region.

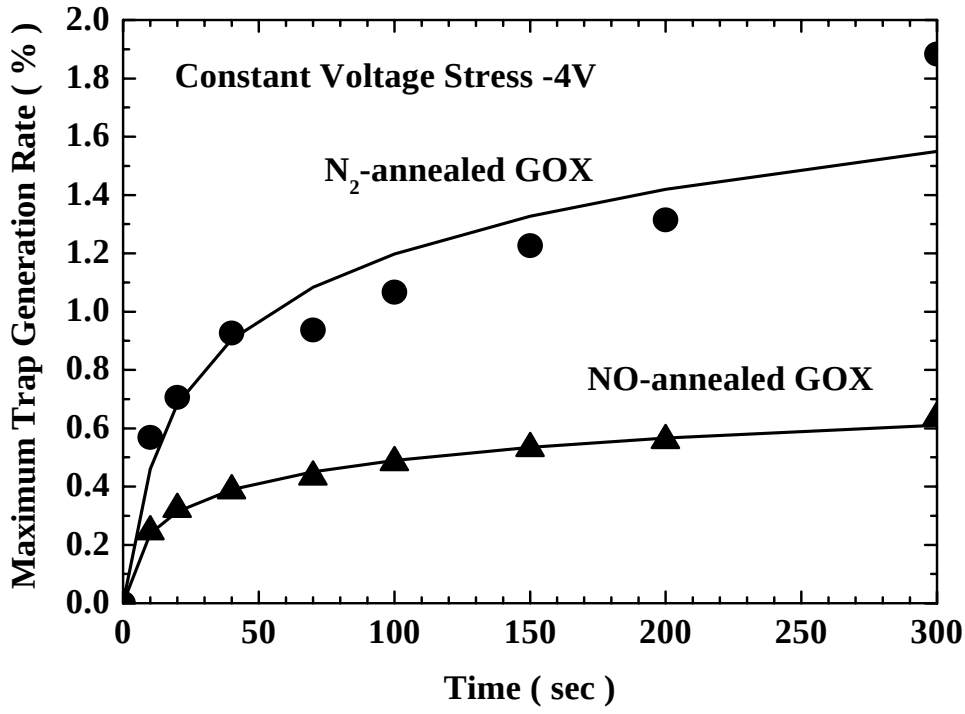


(a)

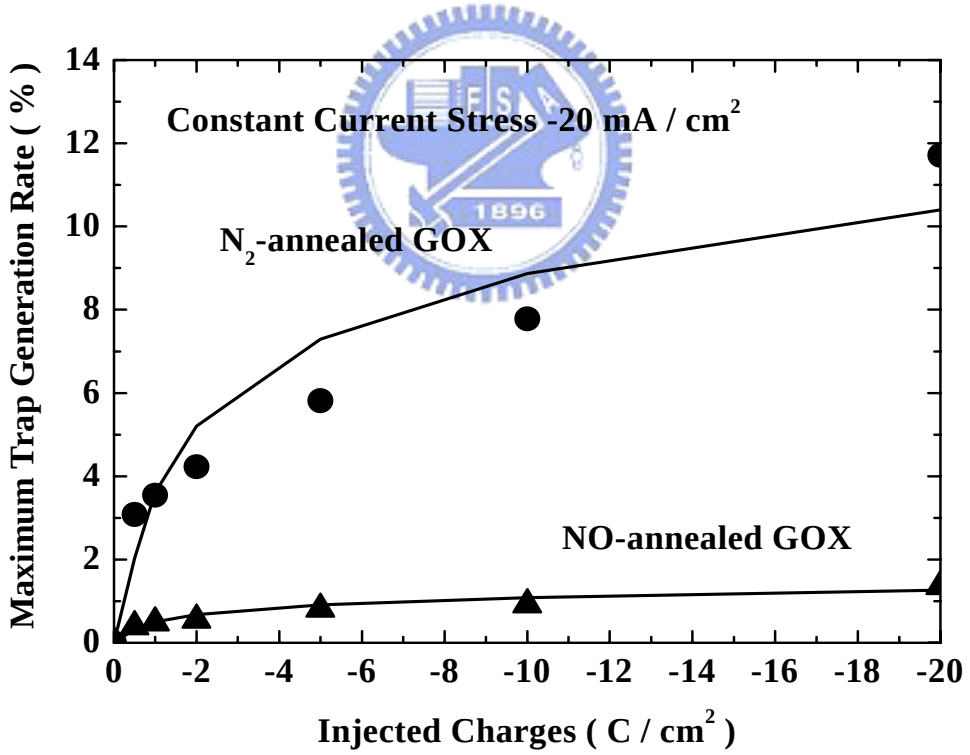


(b)

Fig. 2.8 (a) SILC characteristics (b) transient hole-trapping behavior of 22Å NO- and N_2-annealed GOX at -4V CVS. NO-annealing can suppress both hole-trapping and maximum trap generation rate occurred near flat-band region during constant voltage stress.

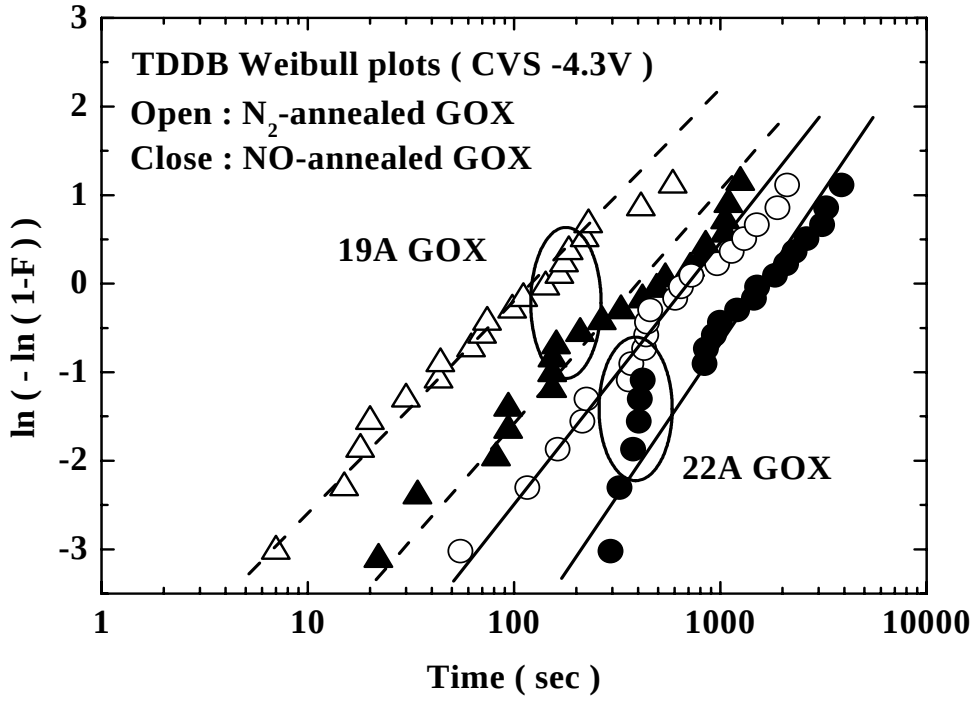


(a)

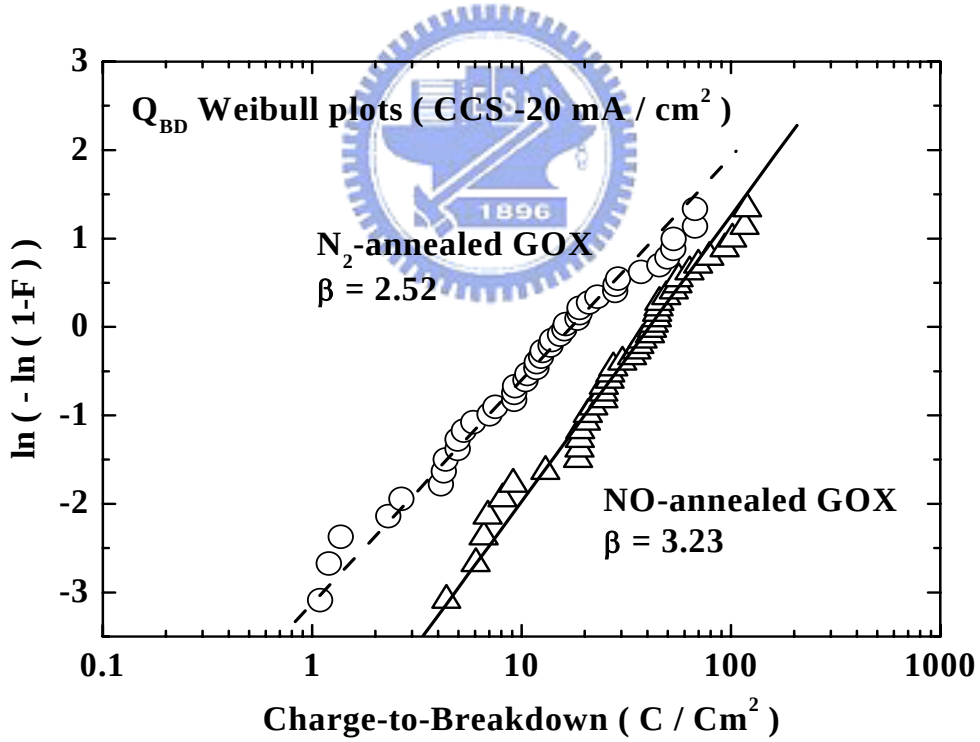


(b)

Fig. 2.9 Maximum trap generation rate of 22Å N_2- and NO-annealed GOX stressed at (a) -4V constant voltage stress (b) -20 mA/cm^2 constant current stress. NO-annealing can reduce hole-trap generation rate during both voltage and current stress.



(a)



(b)

Fig. 2.10 (a) TDDB Weibull plots of 19Å and 22Å N_2- and NO-annealed GOX at -4.3V CVS. (b) Q_{BD} Weibull plots of 22Å N_2- and NO-annealed GOX at -20 mA/cm^2 CCS. NO-annealed nitrided oxides exhibits higher stress immunity than N_2-annealed oxides.

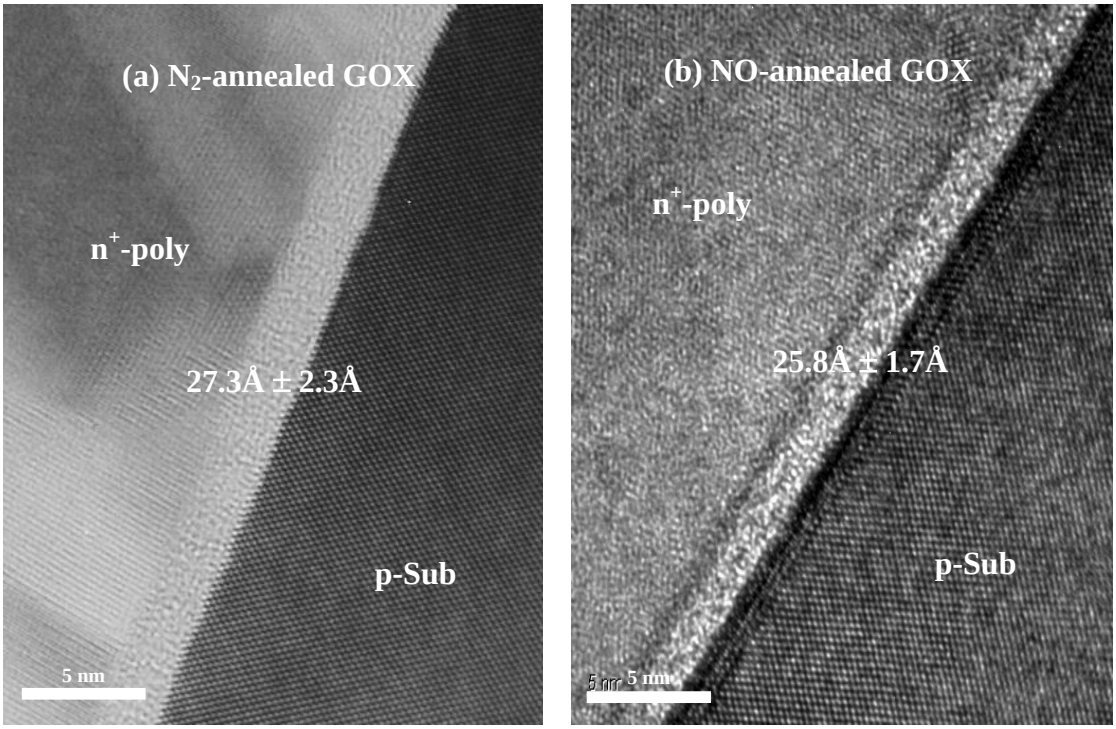


Fig. 2.11 The HRTEM cross-sectional images of 22Å (a) N_2- and (b) NO-annealed GOX. NO-annealing has smoother interface than N_2-annealing.

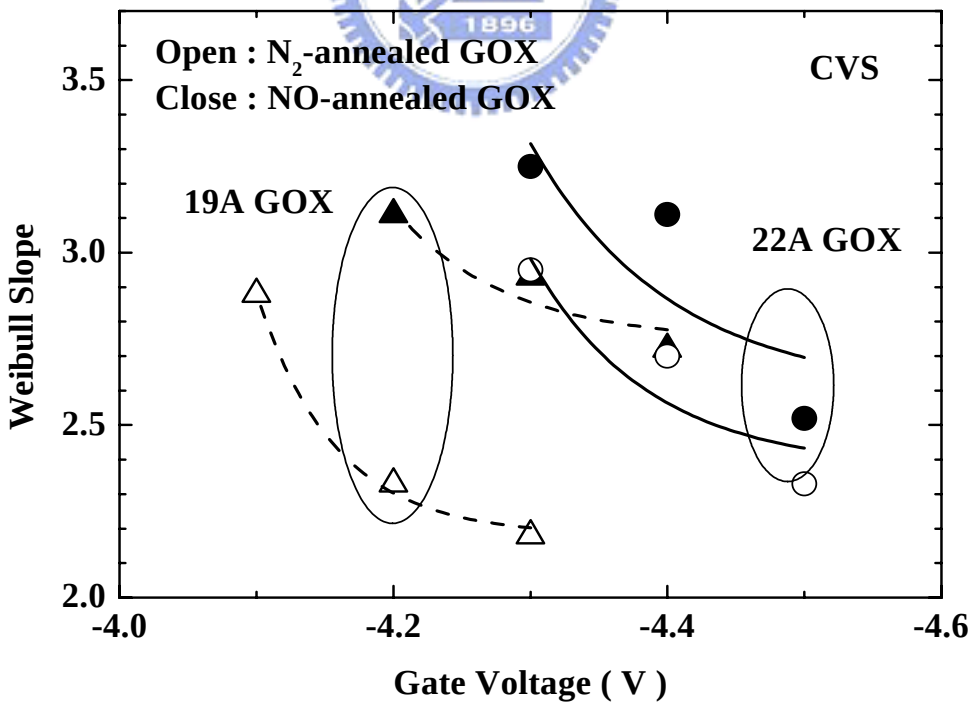


Fig. 2.12 Plots of weibull slope of 19Å and 22Å N_2- and NO-annealed GOX. NO-annealing clearly enhances Weibull slope.

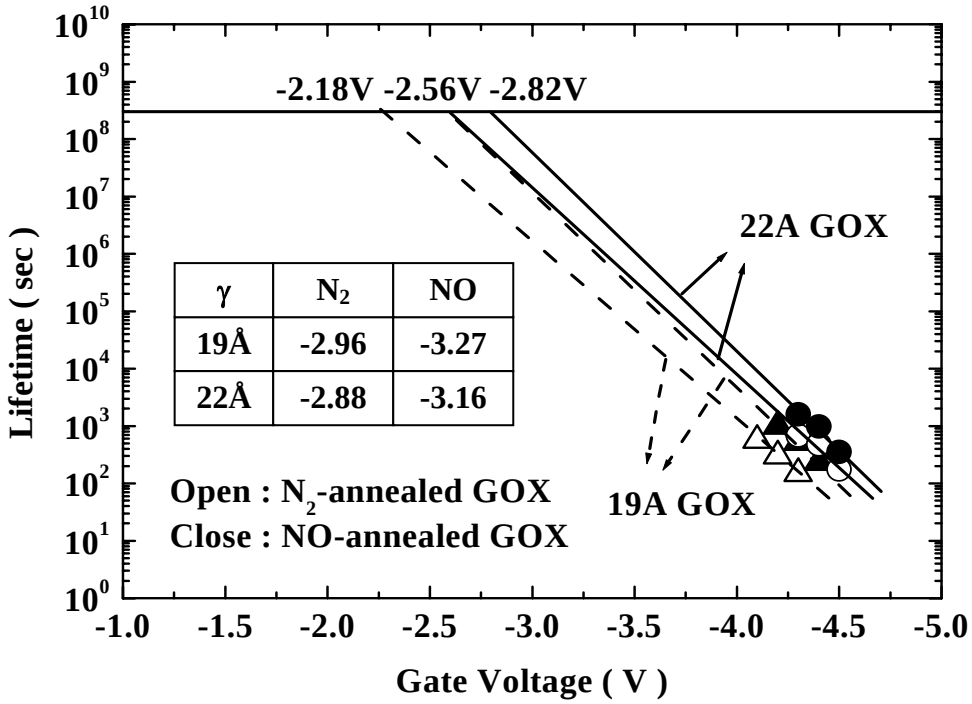


Fig. 2.13 10-year lifetime projection of 19Å and 22Å N_2- and NO-annealed GOX. Inset also indicates voltage acceleration factors.

CHAPTER 3

Characteristics and Reliabilities of Sub-3nm Nitrided Oxides with Nitrogen-Implanted Silicon Substrates

3.1 Introduction

Recently, many efforts including oxygen, argon and nitrogen implantation prior to thermal oxidation, were used to form multiple gate oxide thickness in one thermal cycle to meet system-on-a-chip (SOC) requirement [73]-[78]. Oxygen implantation can improve the oxide quality [73], but it seems unsuitable to apply in the deep-submicron generation since oxygen implantation will enhance oxidation rate and limit the minimum oxide thickness. There are a few reports on argon implantation, however, it is able to provide more thinner oxides than the oxygen implantation [74]. One of the concerns about argon implantation is that the implantation damage caused by heavy mass argon ions may need longer thermal cycle to annealing gate oxides. On the other hand, the nitrogen-implanted Si substrate (NIS) prior to gate dielectrics growth seems the most proper technology to meet the requirement of deep submicron devices [55], [75]-[78]. Since the nitrogen implantation can retard oxidation rate and enhance the control ability of thinner oxide thickness, it is much more suitable to be implemented in SOC technologies. Moreover, nitrogen will pile up at the oxide/substrate interface and suppress boron penetration [78]-[80], which was not observed in both oxygen and argon implantation techniques. In this chapter, the

characteristics and reliabilities of NIS nitrided oxides are studied. NO-annealing will pile-up nitrogen near the interface, while NIS will introduce uniformly distribution nitrogen in the dielectric bulk. With optimized implantation dosage and post-oxidation annealing temperature, NIS nitrided oxides could effectively suppress trap generation and improve both time-to-breakdown (t_{BD}) and charge-to-breakdown (Q_{BD}), also suitable to reduce process steps of the SOC technology.

3.2 Experiment Details

All experimental split conditions of nitrided oxides are detailed in Table 3.1. LOCOS isolated MOS capacitors were fabricated on p-type (100) silicon wafers. After forming LOCOS isolation, nitrogen was implanted into the Si substrates at the split dosage of 1×10^{13}, 1×10^{14} and 1×10^{15} cm^{-2} with 10keV. In addition, some wafers without nitrogen implantation were used for comparison. Wafers were then cleaned and HF dipped before oxidation. The gate dielectrics were grown at 750^{o}C followed by either NO or N_2 annealing at 850^{o}C for an hour. Then 1500Å polysilicon was deposited with in-situ doped phosphorus of 2.5×10^{20} cm^{-3}. Dopants were then activated at 950^{o}C for 30sec. After gate electrodes patterned and contact holes etched, aluminum metallization was done followed by sintering at 450^{o}C in N_2 ambient.

Square or circular capacitors of different areas, ranging from 2.5×10^{-5} to 1×10^{-2} cm^2, with LOCOS isolation are used to evaluate the gate oxide integrity. The physical gate oxide thickness was determined by spectroscopic ellipsometer and compared with high-resolution transmission electron microscopy (HRTEM). The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency

capacitance-voltage (*C-V*) data from Hewlett-Packard (HP) 4284 LCR meter under an accumulation condition with quantum mechanical correction. The tunneling leakage current density-electric field (*J-E*) and the reliability characteristics of MOS capacitors were measured by semiconductor parameter analyzer HP4145A. Nitrogen depth profiles and compositions were analyzed by secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS). The micro-roughness of the wafer surface and the interface between nitrided oxides/silicon were detected by atomic force microscopy (AFM).

3.3 Results and Discussions

Recently, the technique of nitrogen-implanted into Si substrate has been paid more and more attention on nitrided oxide growth and SOC application [56], [75]-[78]. NIS has the advantage in growing multiple gate oxide thickness at one thermal cycle and is suitably applied to SOC technology. However, the most concerning issue for NIS is the surface damage during nitrogen implantation. Thus, post-implantation thermal cycle must be very careful in order to fully anneal out the damage to guarantee the oxide quality.

3.3.1 Basic Characteristics of Sub-3nm NIS Nitrided Oxides

The *C-V* curves of 22Å N_2- and NO-annealed NIS nitrided oxides are shown in Fig. 3.1(a) and (b), respectively. For low implantation dose, 1×10^{13} and 1×10^{14} cm^{-2}, no obvious difference in *C-V* curves has been seen. However, significant V_{FB} recovery and D_{it} degradation observes with heavy implanted nitrided oxide, i.e. 1×10^{15} cm^{-2},

with respect to sample without NIS. Since N is a donor-type impurity, the substrate acceptor concentration will decrease by the implanted N atoms before oxidation, and results in smaller V_{FB} [75]. Table 3.2 lists the flat-band voltages and interface state densities of NO- and N_2-annealing NIS nitrided oxides.

Figure 3.2(a) compares oxide thickness as a function of nitrogen implantation dose into the Si substrate. The oxidation rate drops continuously with increasing nitrogen dose [74]-[80], [81], [82]. In our study, slightly enhanced oxidation rate with NIS smaller than 1×10^{14} cm^{-2} is ascribed to insufficient annealing out the damage by ion bombardment. Significant oxidation rate suppression only has been observed with NIS larger than 1×10^{14} cm^{-2}. Accordingly, the oxidation rate is trade-off by the residual damage annealing and oxidant diffusion rate constraint, resulting in the increased oxidation rate firstly and then decreased. With a heavy implant dose of 1×10^{15} cm^{-2}, the growth rate can be reduced by 15%, which is smaller than that reported in Ref. 76, probably due to lower oxidation temperature (750^{o}C) in our study. The difference between TEM and QMCV thickness is larger for sample with 1×10^{15} cm^{-2} NIS than 1×10^{13} and 1×10^{14} cm^{-2} NIS, which can be ascribed to the heavier N concentration induced larger dielectric constant for sample with 1×10^{15} cm^{-2} NIS.

Dielectric constant (κ) as a function of nitrogen implantation dosage into the Si substrate is shown in Fig. 3.2(b). The κ-value of samples without NIS is extracted by extra-plotting of QMCV and TEM thickness (shown in Fig. 2.2), while the κ-value of samples with NIS is extracted directly from the QMCV and TEM thickness. κ-value increase has only been observed in the sample with the heavy implant. Post-oxidation NO-annealing can further increases κ values. Thickness and κ variation for NIS nitrided oxides is summarized in Table 3.3. As the nitrogen dose increases, dielectric constant will slightly increase from 3.9 of pure SiO_2 to 4.6 of sample with

NO-annealing and 1×10^{15} cm^{-2} NIS. NO-annealed GOX still has higher dielectric constant than N_2-annealed GOX due to higher nitrogen concentration.

Figure 3.3 compares the leakage current density for 22Å N_2-annealed and NO-annealed NIS nitrided oxides at negative gate bias polarity. When NIS is less than 1×10^{14} cm^{-2}, the leakage current increases slightly due to the residual implantation damages. Nevertheless, as NIS dosage increases to 1×10^{15} cm^{-2}, the leakage current will increase more obvious since the oxidation rate will be suppressed by the heavy nitrogen-passivated surface and result in thinner oxide thickness. In short, post oxidation NO-annealing will introduce N into the gate oxides/substrate interface, increase V_{FB} shift and D_{it}. On the contrary, while nitrogen is donor impurity to Si, partial implanted-nitrogen may retain on Si substrate without forming $Si_3{\equiv}N$ bonding and counter-doping substrate concentration. Consequently, NIS before oxidation will reduce substrate doping, and slightly recover V_{FB} shift.

3.3.2 Reliability Characteristics of Sub-3nm NIS Nitrided Oxides

Figure 3.4(a) displays the XPS depth profiles of NO-annealed nitrided oxide with 4×10^{15} cm^{-2} NIS dosage. Not alike to Fig. 2.6(a), pre-oxidation NIS will incorporate N into dielectric bulk rather than pile-up at interface. Figure 3.4(b) compares nitrogen distribution profiles with and without NIS. Without NIS, dielectric bulk is devoid of nitrogen. After post-oxidation NO annealing NIS nitrided oxides, more N will diffuse to interface, form $Si_3{\equiv}N$ bonding. Moreover, sample with 1×10^{15} cm^{-2} NIS not only exhibits higher peak concentration at interface, but also has tighter N distribution than samples with lighter NIS, which is beneficial to obtain an uniformly distributed reliabilities. Figure 3.5 indicates the leakage current density of 22Å N_2- and NO-annealed NIS nitrided oxides with and without nitrogen implantation

under constant voltage stress (CVS) at -4V for 100sec. The major difference between fresh and stressed curves occurs near flat-band conditions, as described in Chapter 2. Comparing to gate oxides without NIS, apparent SILC increment for low and medium dose NIS is exhibited. However, there is almost no leakage current increase for heavy NIS during voltage stress. The reasons for dosage-dependent SILC immunity will be explained below.

Figure 3.6(a) compares transient trapping behavior of 22Å NO-annealed NIS nitrided oxides during CCS. It should be noted all samples show an obvious hole trapping characteristics. For NIS smaller than 1×10^{14} cm^{-2}, pre-oxidation nitrogen implantation will enhance the hole trapping. As NIS increases to 1×10^{15} cm^{-2}, the hole trapping becomes negligible. The trap generation rate as a function of injected charges is seen in Fig. 3.6(b). Similar trend is examined. Eliminated trap generation rate appears only at heavy N implantation case, i.e. 1×10^{15} cm^{-2}. Figure 3.7(a) presents the time-dependent dielectric breakdown (TDDB) Weibull distribution of 22Å NO-annealed NIS nitrided oxides during CVS at -4.3V. Nitrided oxides with NIS less than 1×10^{14} cm^{-2} reveal poorer t_{BD} than the samples without NIS due to the larger hole generation rate. As consistent to Fig. 3.6, heavy NIS is expected to exhibit the highest t_{BD}. The Weibull slope is also dependent on the NIS dosage, which is plotted in Fig. 3.7(b). β shows a valley at the NIS dosage of 1×10^{13} cm^{-2} from residual implantation damage and a peak at 1×10^{15} cm^{-2} due to the tighten nitrogen distribution profiles in the dielectric bulk. As shown in Fig. 3.4(b), 1×10^{15} cm^{-2} NIS will retard oxidation rate and generate uniform N distribution, higher β is expected for heavy NIS. Although thinner oxide thickness of sample with 1×10^{15} cm^{-2} NIS would partially contribute to less SILC characteristics, only 3~4Å thickness reduction may not enhance SILC immunity significantly than samples with 1×10^{13} and 1×10^{14} cm^{-2} NIS. As a result, the

drastic SILC immunity improvement is accredited to uniform nitrogen distribution in the dielectric bulk.

In our study, NIS dosage smaller than 1×10^{14} cm^{-2} will slightly increase the oxidation rate due to insufficient post-oxidation annealing out the damage from ion bombardment, which is shown in Fig. 3.1. The residual damage may increase weak bonding during oxidation and result in less SILC immunity, enhanced trap generation rate and poor t_{BD}. Inferior surface roughness will also response for degraded dielectric reliability, as seen in Fig. 3.8 and 3.9 for N_2- and NO-annealed NIS nitrided oxides, respectively. On the other hand, samples with 1×10^{15} cm^{-2} NIS not only can use to grow multiple oxide thickness but also improve reliability significantly. The results are quite opposite to samples with lighter implantation dose, which can attribute to several reasons.

First, surface is abounded with N atoms for heavy NIS implantation dosage, which may easily replace the weak Si-O bonds damaged by ion bombardment in the transition region by the strong $Si_3{\equiv}N$ bonds during oxidation. Secondly, implantation would change interface morphology [70]. From HRTEM photos exhibited in Fig. 3.8 and 3.9, surface roughness is increased while NIS increases from 0 to 1×10^{14} cm^{-2}, which may be due to faster oxidation rate and less N area density. On the other hand, surface RMS roughness is decreased to 0.87nm with further increasing NIS to 1×10^{15} cm^{-2}. It can be seen that the nitrided oxide/silicon interface is very smooth and exhibits a highly uniform transition region from the crystalline silicon to the amorphorous nitrided oxide. This is beneficial for the electrical properties of the MOS device as described above. Surface roughness is also evidenced by AFM images and summarized in Fig. 3.10. A smoother interface is helpful in reducing the localized field and, hence, results in stronger SILC immunity and larger t_{BD}. Thirdly, it is

known that SILC becomes negligible as the oxide thickness down to the direct-tunneling dominate regime. The heaviest NIS can retard oxidation rate significantly and grow the thinnest oxide, as seen in Fig. 3.2. In consequence, nitrided oxides with NIS dosage of 1×10^{15} cm^{-2} possesses stronger SILC immunity and better TDDB characteristics than others, regardless of post-oxidation N_2- or NO-annealing.

3.4 Summary

The dielectric properties and reliability characteristics of NIS nitrided oxides are investigated in this chapter. An obvious oxidation rate retardation effect is observed for the nitrided oxides with nitrogen-implanted Si substrate. Dielectric property is strongly depended on NIS dosage and post-oxidation annealing temperature. NIS dosage less than 1×10^{14} cm^{-2} is helpless to oxidation rate suppression accompanying with degraded dielectric reliability. On the contrary, the samples with 1×10^{15} cm^{-2} NIS not only can use to grow multiple oxide thickness to meet SOC requirement, but also improve stress immunity apparently. Nitrogen implantation also generates a uniform distribution nitrogen profile in the dielectric bulk, which can be used as an effective diffusion barrier to resist boron penetration. NIS nitrided oxides could effectively suppress trap generation and improve time-to-breakdown and charge-to-breakdown, also suitable to reduce process steps of the SOC technology.

Table 3.1 Experimental conditions of nitrided gate oxides formed by pre-oxidation NIS and post-oxidation NO-annealing.

Anneal Gas	T_{OX} (Å)	NIS dosage (cm^{-2})			
		0	1×10^{13}	1×10^{14}	1×10^{15}
NO anneal	30	√	√	√	√
	22	√	√	√	√
	19	√	N/A	N/A	N/A
N_2 anneal	30	√	√	√	√
	22	√	√	√	√
	19	√	N/A	N/A	N/A

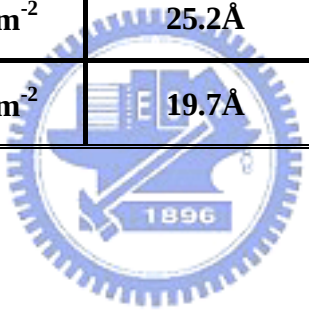
Table 3.2 Flat-band voltages and interface state densities of NO- and N_2-annealed NIS nitrided oxides.

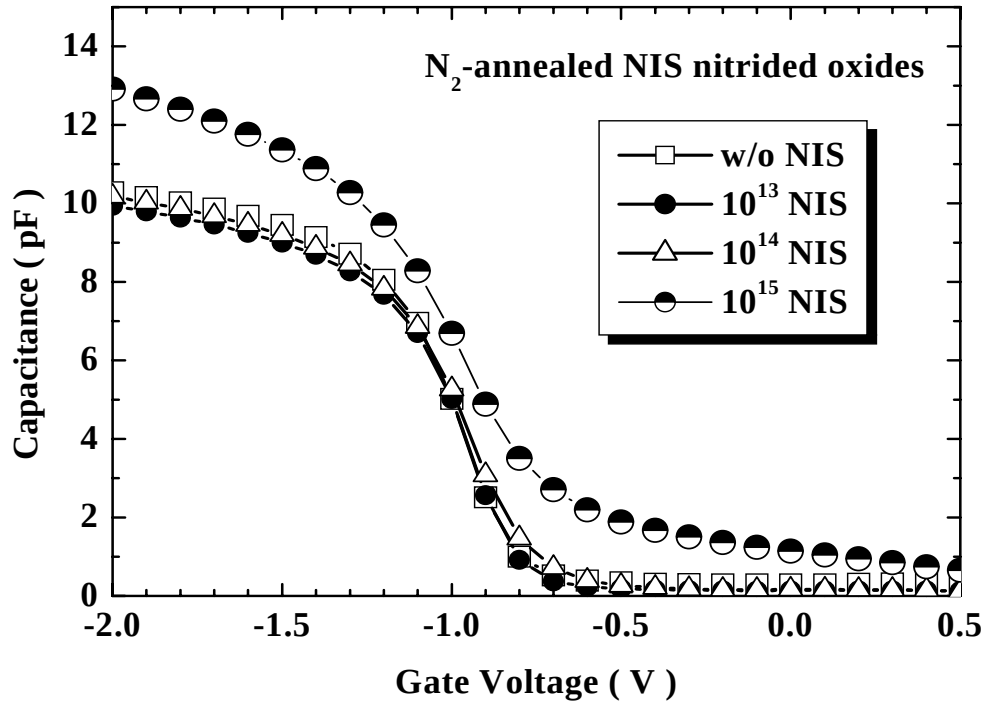
NIS \ V_{FB}	NO-GOX (V)	N_2-GOX (V)	ΔV_{FB} (mV)
0	-1.085	-1.055	-30
1×10^{13} cm^{-2}	-0.992	-0.958	-34
1×10^{14} cm^{-2}	-0.925	-0.896	-29
1×10^{15} cm^{-2}	-0.825	-0.816	-9

NIS \ D_{it}	NO-GOX (V)	N_2-GOX (V)	ΔD_{it} (cm^{-2} eV^{-1})
0	7.06×10^{11}	4.88×10^{11}	2.18×10^{11}
1×10^{13} cm^{-2}	8.82×10^{11}	4.93×10^{11}	3.89×10^{11}
1×10^{14} cm^{-2}	9.11×10^{11}	5.11×10^{11}	4.00×10^{11}
1×10^{15} cm^{-2}	2.45×10^{12}	1.90×10^{12}	5.50×10^{11}

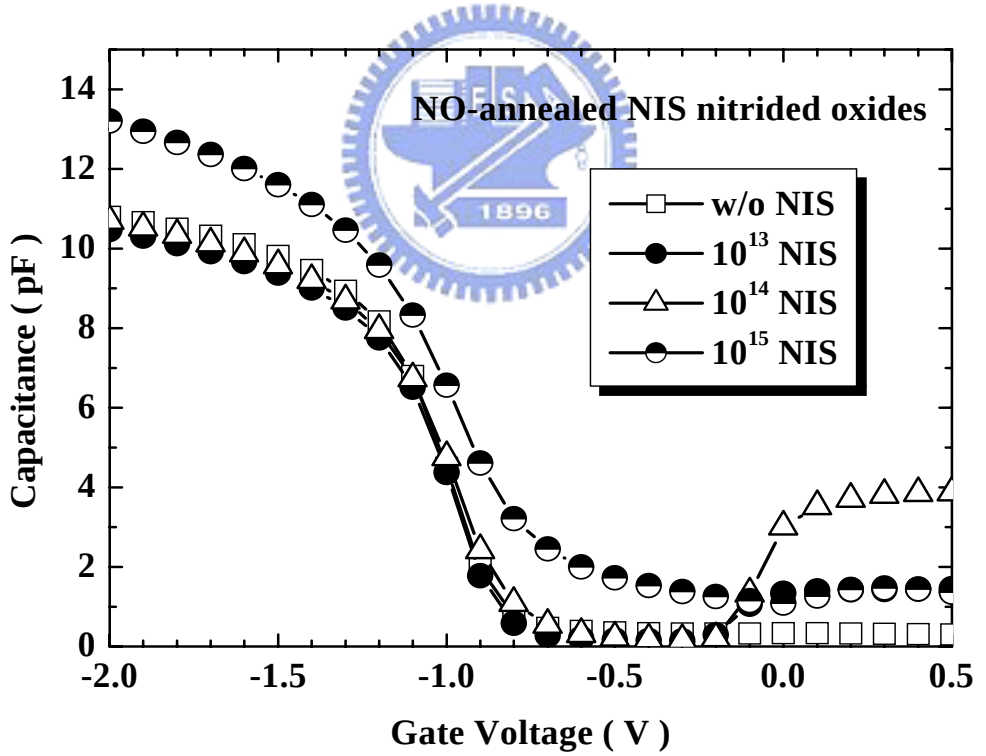
Table 3.3 Thickness and dielectric constant variation for NO- and N_2-annealed NIS nitrided oxides.

	NIS Dosage	QMCV	TEM	κ
N_2 anneal	**0**	**26.3Å**	**27.3Å**	**4.01**
	1×10^{13} cm^{-2}	**27.3Å**	**27.6Å**	**3.94**
	1×10^{14} cm^{-2}	**26.6Å**	**27.2Å**	**3.99**
	1×10^{15} cm^{-2}	**20.2Å**	**23.3Å**	**4.50**
NO anneal	**0**	**24.9Å**	**25.8Å**	**4.20**
	1×10^{13} cm^{-2}	**25.7Å**	**27.2Å**	**4.13**
	1×10^{14} cm^{-2}	**25.2Å**	**26.8Å**	**4.15**
	1×10^{15} cm^{-2}	**19.7Å**	**23.2Å**	**4.60**



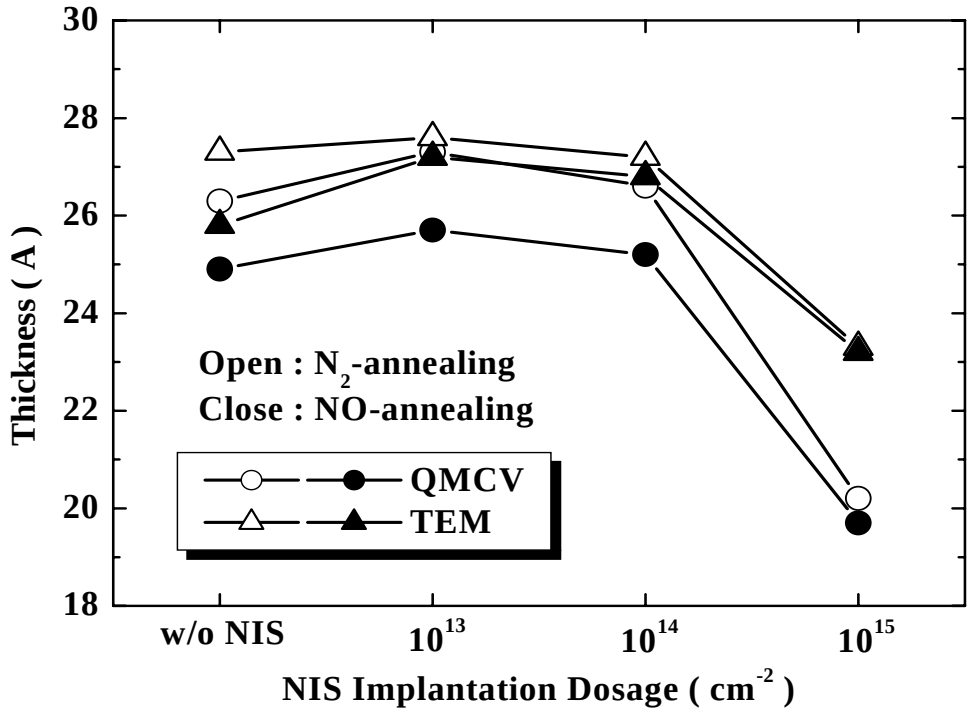


(a)

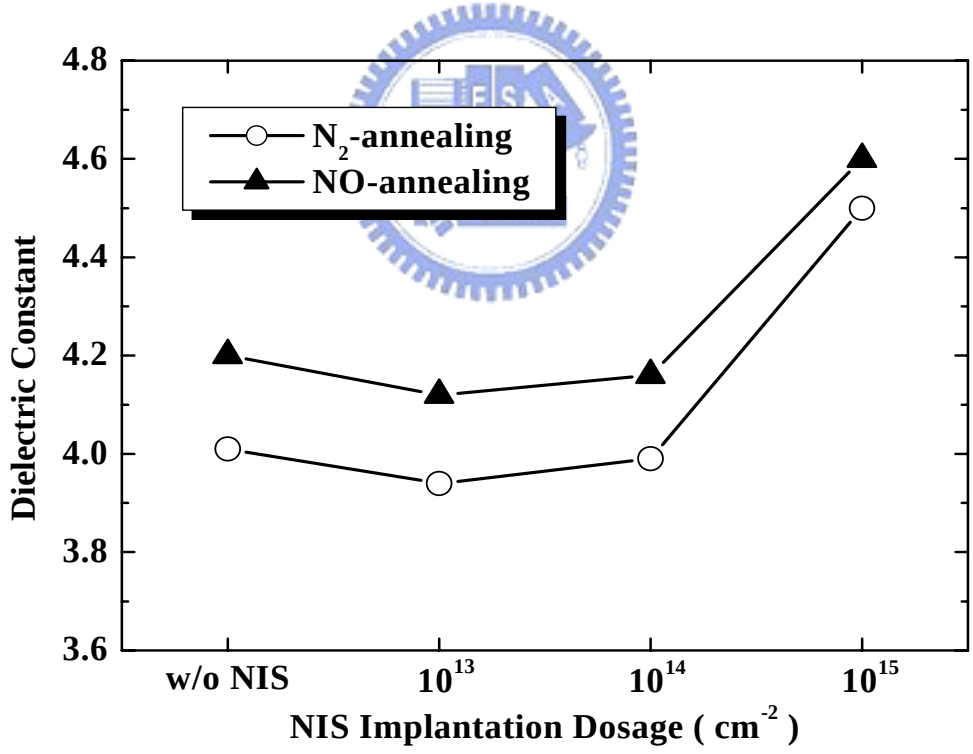


(b)

Fig. 3.1 Plots of high frequency *C-V* curves of 22Å (a) N_2-annealed (b) NO-annealed NIS nitrided oxides. Significant oxidation rate retardation is inspected as NIS dosage larger than 1×10^{14} cm^{-2}. As NIS dosage larger than 1×10^{15} cm^{-2}, clear V_{FB} shift and D_{it} increment is observed.

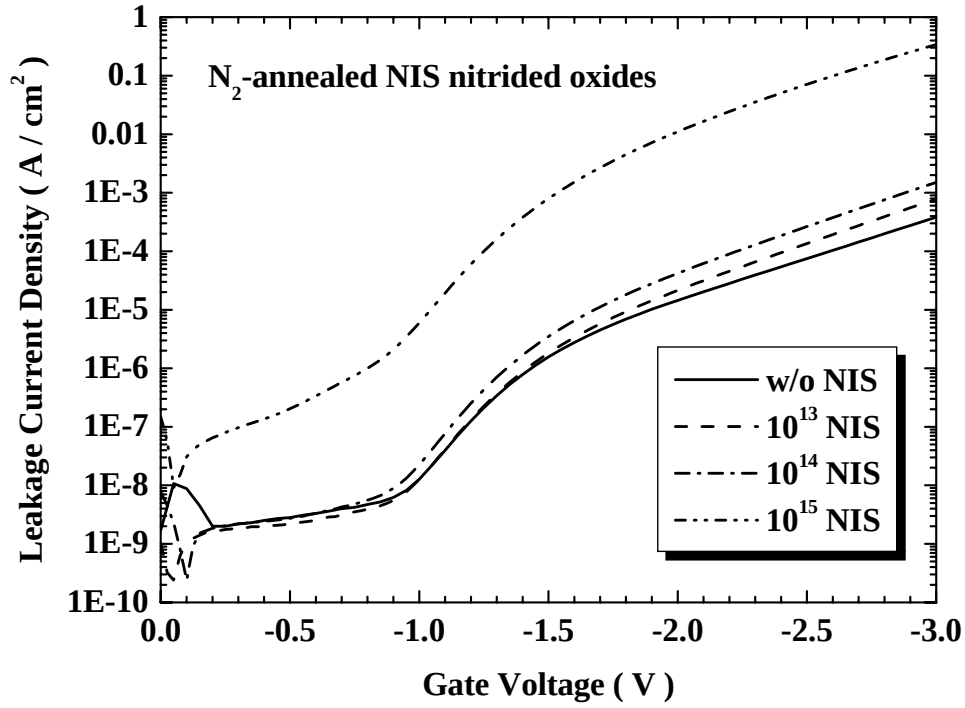


(a)



(b)

Fig. 3.2 (a) Oxide thickness (b) dielectric constant as a function of nitrogen dosage implanted into the silicon substrate before oxidation. Dielectric constant increases from 3.9 to 4.6 for NO-annealed NIS nitrided oxides with heavy implantation dosage.



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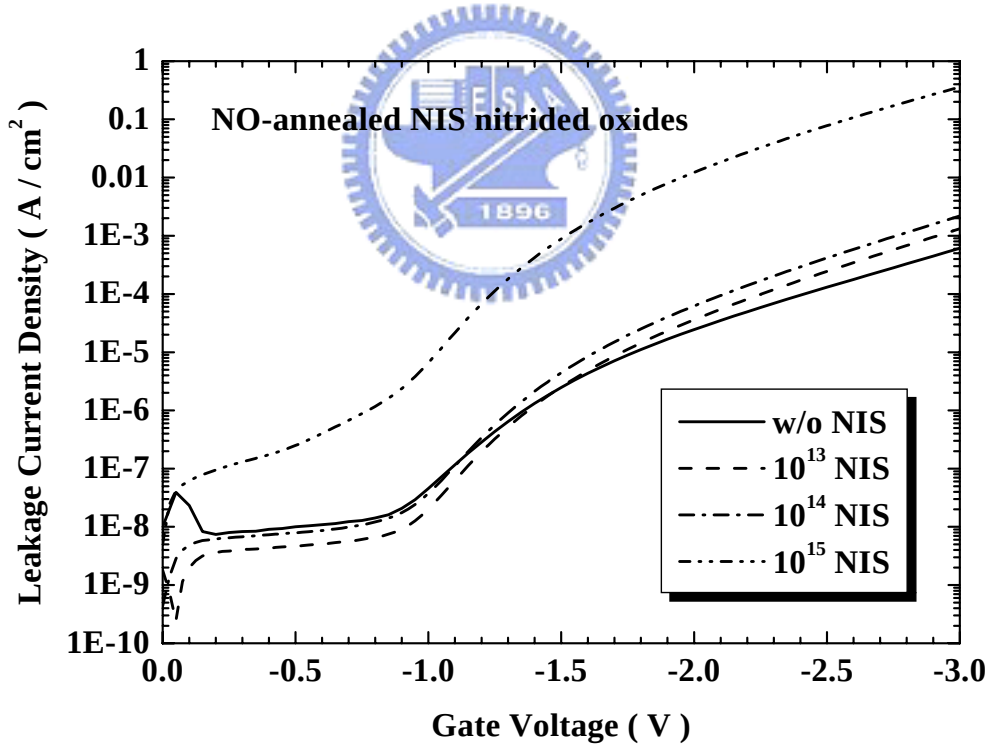
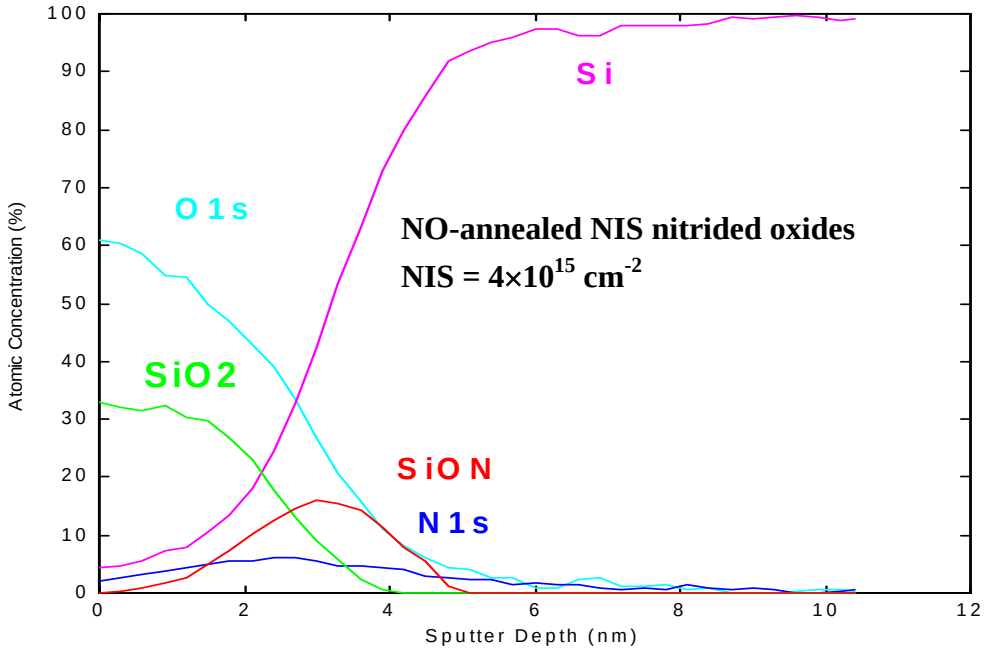
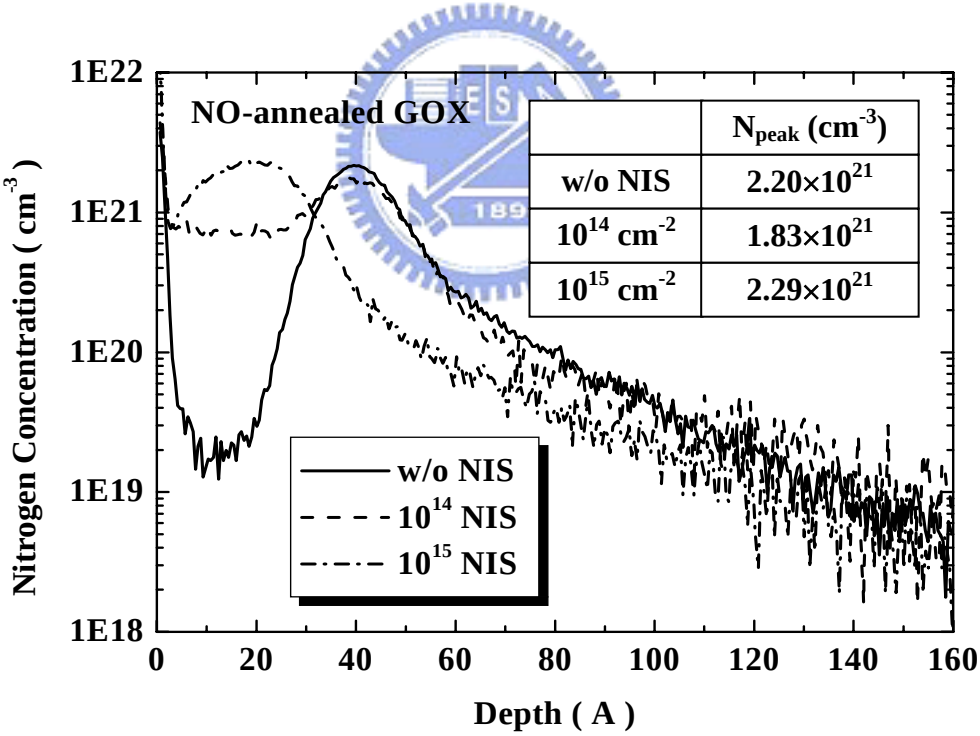


(b)

Fig. 3.3 Direct tunneling leakage current density as a function of gate voltages of 22Å (a) N_2-annealed (b) NO-annealed NIS nitrided oxides. Direct tunneling leakage current density is strongly dependent on the dosage of nitrogen implanted into Si substrate..

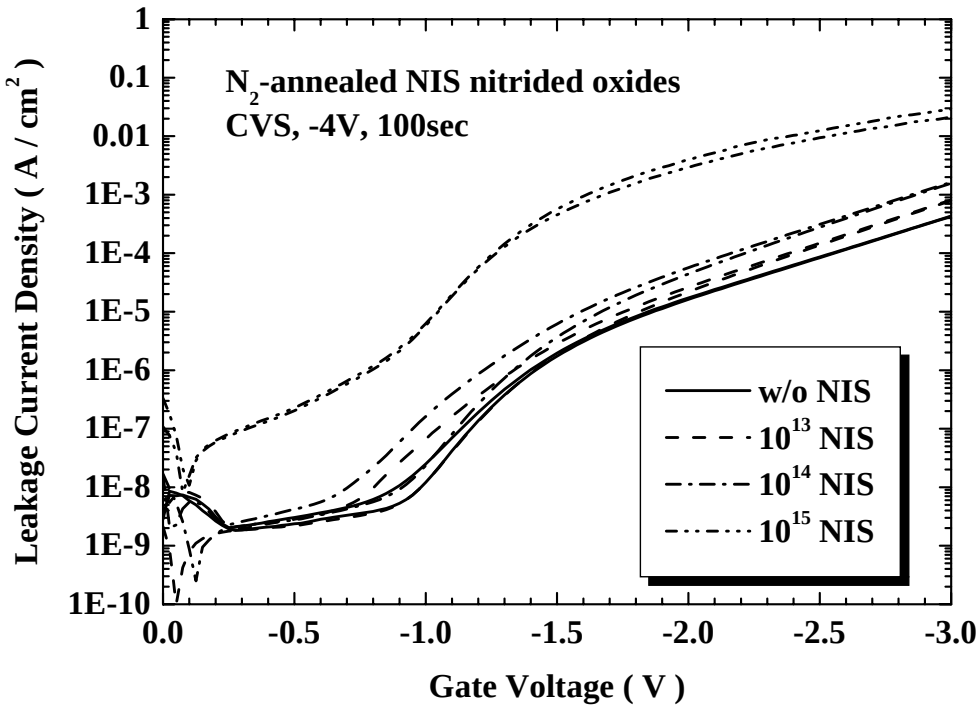


(a)

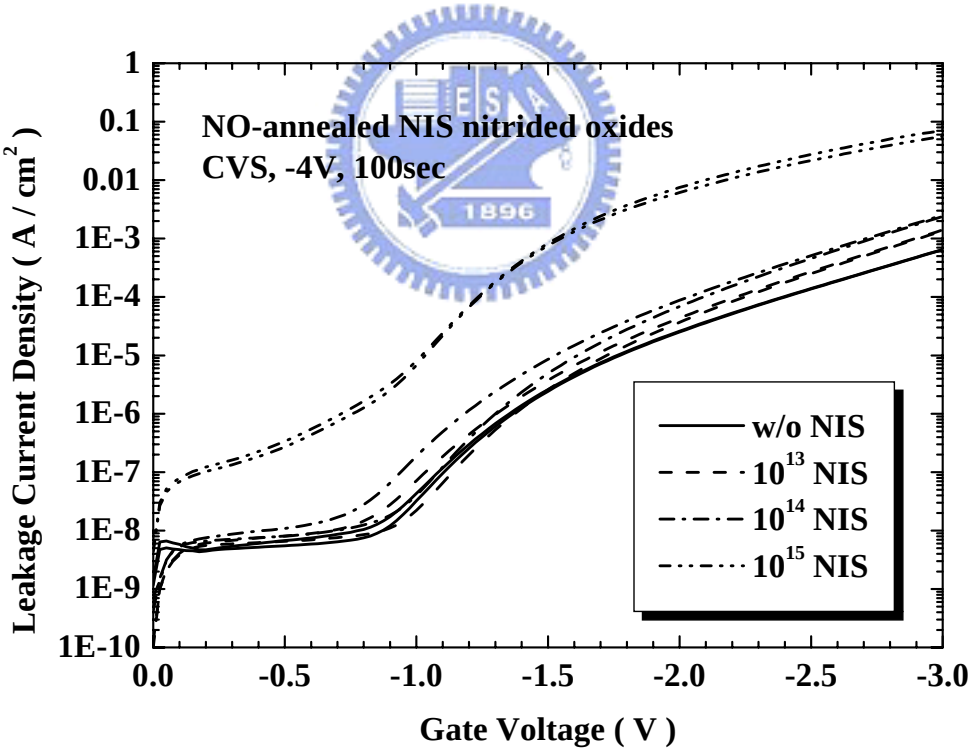


(b)

Fig. 3.4 (a) XPS depth profiles of 22Å NO-annealed nitrided oxides with 4×10^{15} cm^{-2} NIS. Evidence of Si_3N_4-like interface is observed. (b) SIMS nitrogen depth profiles of 30Å NO-annealed NIS nitrided oxides. NIS incorporates uniform nitrogen distribution in the bulk.

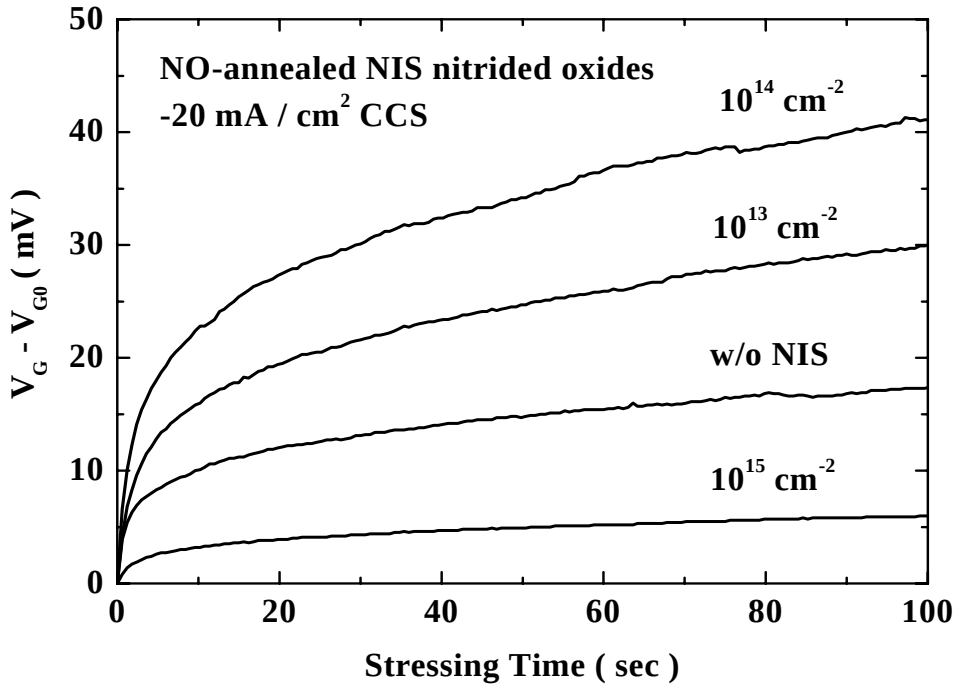


(a)

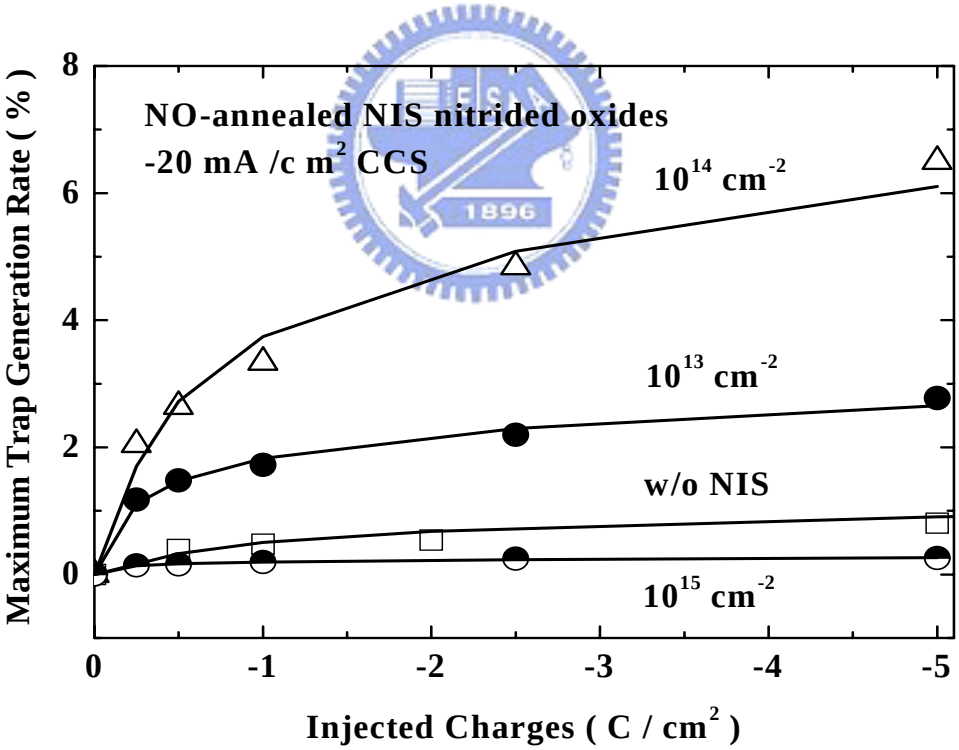


(b)

Fig. 3.5 SILC characteristics of 22Å (a) N_2-annealed (b) NO-annealed NIS nitrided oxides at -4V CVS for 100sec. Maximum current increase after CVS occurs near flat band region. Increased SILC is negligible for 1×10^{15} cm^{-2} NIS nitrided oxides.

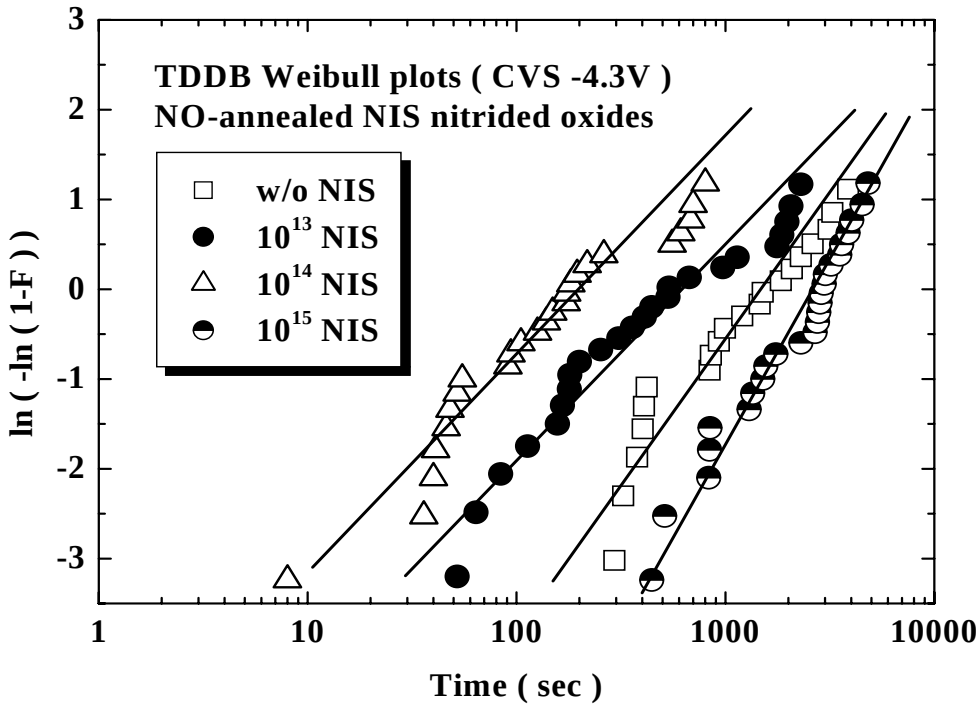


(a)

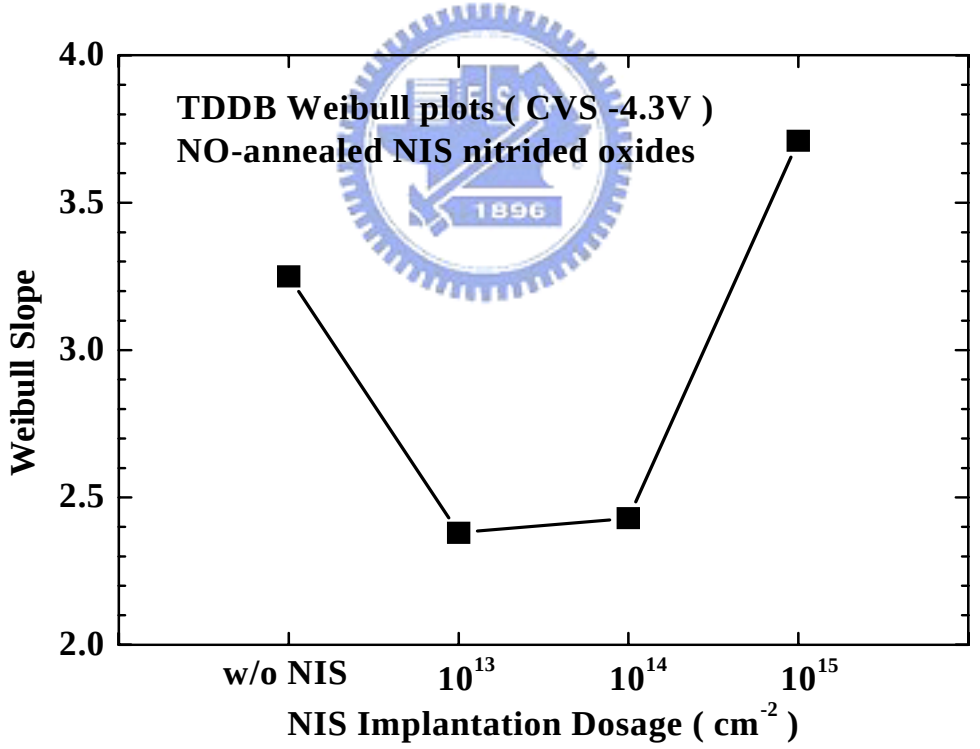


(b)

Fig. 3.6 (a) Transient hole-trapping behaviors (b) maximum trap generation rates of 22Å NO-annealed NIS nitrided oxides at -20 mA/cm^2 constant current stress. NIS nitrided oxides with 1×10^{15} cm^{-2} dosage has negligible trap generation rate for both CVS and CCS.



(a)



(b)

Fig. 3.7 (a) t_{BD} Weibull distribution (b) Weibull slopes of 22Å NO-annealed NIS nitrided oxides under -4.3V constant voltage stress. The reliability of NIS nitrided oxides is substantially relied on NIS dosage, t_{BD} and Weibull slope are increased only for NIS nitrided oxides with 1×10^{15} cm^{-2} dosage.

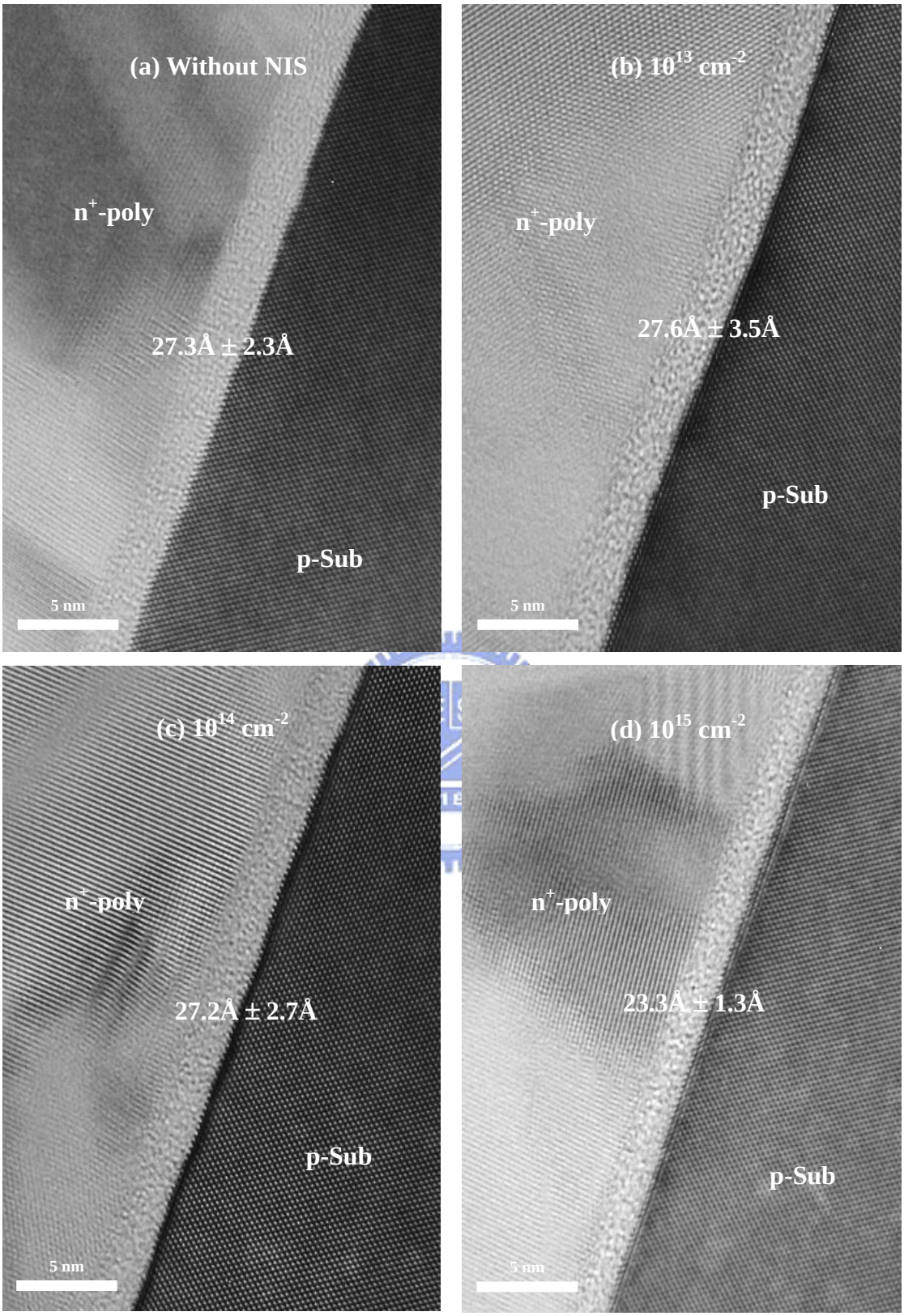


Fig. 3.8 The HRTEM cross-sectional images of 22Å N_2-annealed NIS nitrided oxides. (a) without NIS (b) 10^{13} cm^{-2} (c) 10^{14} cm^{-2} (d) 10^{15} cm^{-2}. Sample with 10^{15} cm^{-2} NIS not only smoothes interface but also reduces physical thickness.

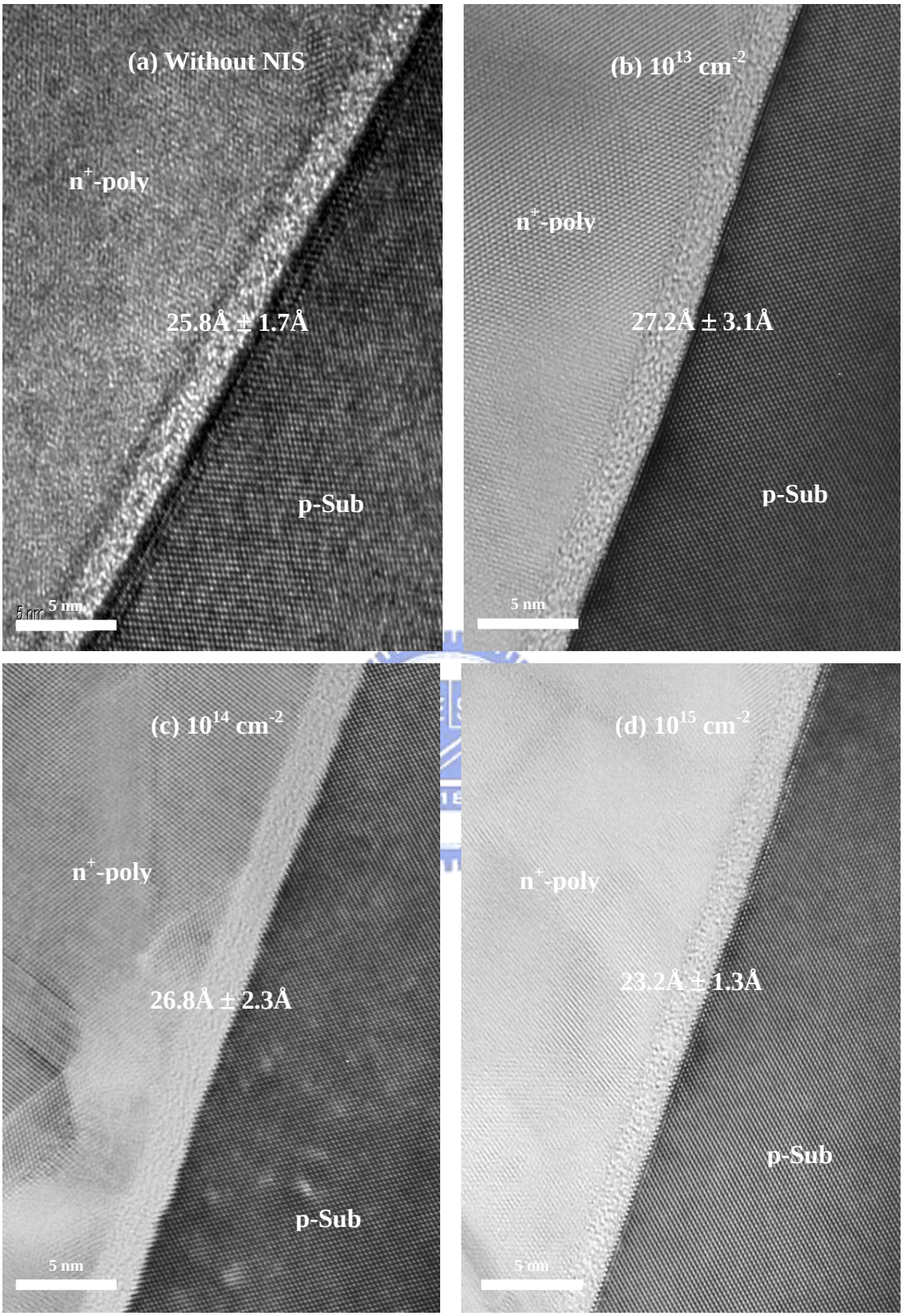


Fig. 3.9 The HRTEM cross-sectional images of 22Å NO-annealed NIS nitrided oxides. (a) without NIS (b) 10^{13} cm^{-2} (c) 10^{14} cm^{-2} (d) 10^{15} cm^{-2}. Sample with 10^{15} cm^{-2} NIS not only smoothes interface but also reduces physical thickness.

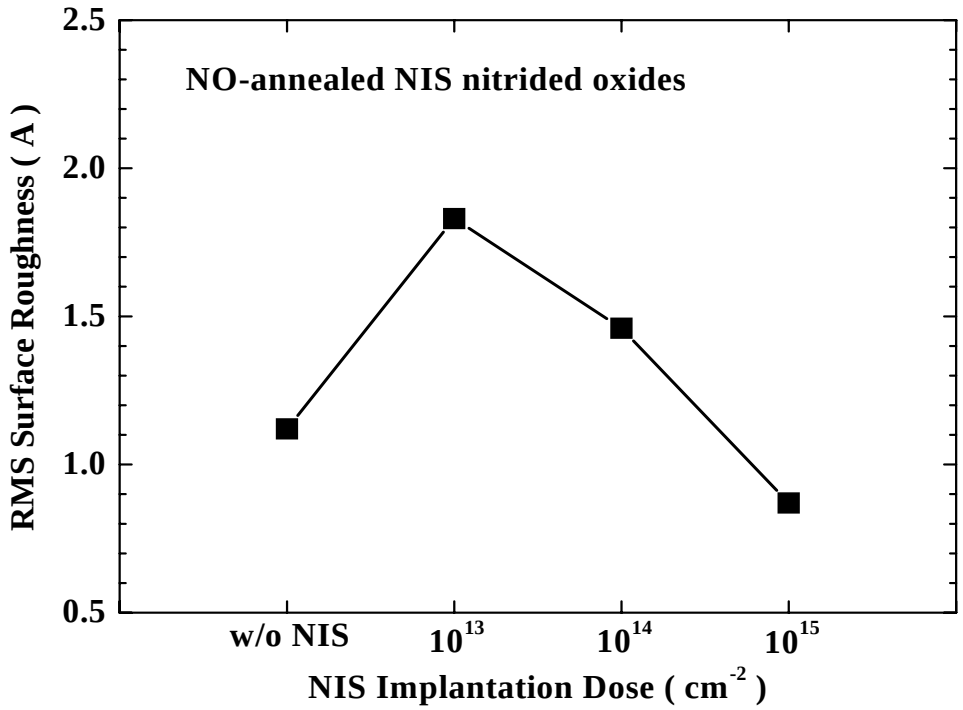


Fig. 3.10 Substrate surface roughness of NO-annealed NIS nitrided oxides after dielectrics removal by diluted HF solution. Evidence of smooth interface is revealed for samples with 10^{15} cm^{-2} NIS and post-oxidation NO annealing.

CHAPTER 4

Simulated Characteristics of Stacked-Gate Flash Memories with Inter-Poly High-κ Dielectrics

4.1 Introduction

In pursuing the high speed and low power operation of flash memory technologies, the employment of high-permittivity (κ) inter-poly dielectrics (IPDs) into flash memories has attracted much attention recently [21]-[23]. By increasing the floating gate coupling ratio, high-κ IPDs can lead to a high electric field across tunnel oxide even at very low control gate voltage. To successfully employ high-κ IPDs in flash memory, one must take charge retention issues into consideration and make sure that the barrier height (φ_B) between Si and the new adopted high-κ dielectrics should be larger than 1.5eV for effectively suppressing the loss of floating gate charges through electron thermal emission [33]. Usually, dielectrics with higher κ inherently have lower φ_B. Therefore a trade-off between dielectric constant and barrier height is inevitably required in trying to implement the high-κ dielectrics in flash memories.

Recently, aluminum oxide (Al_2O_3) [17], [44]-[46] and hafnium oxide (HfO_2) [20], [47]-[50] had been proved as promising candidates for the gate dielectrics of sub-0.1 μm device due to their higher dielectric constant (κ), relatively high φ_B and superior thermal stability. Nonetheless, the effects of these kinds of high-κ dielectrics on flash memories are seldom investigated. In this chapter, the effects of Al_2O_3 and

HfO_2 serving as the IPD of flash memories were studied with different programming and erasing schemes through 2-D MEDICI simulator. We found that dielectric with medium κ value is the most promising IPD candidate because the gate coupling ratio would be rapidly saturated as κ is greater than 25. It is also demonstrated that the improvement of high-κ IPDs is more effective with Fowler-Nordheim (FN) injected programming and erasing than hot electron (HE) injection. As a result, high-κ IPDs are suitable for next generation NAND-type stacked-gate flash memories.

4.2 Simulation Details

To examine the impact of high-κ IPDs, simulations are carried out using the conventional stacked-gate flash cell with SiO_2 tunnel oxide (TOX). Two-dimensional MEDICI [83] simulator is employed for the performance simulations of a 0.45μm stacked-gate n-channel flash memory with several kinds of high dielectric constant IPD. They are Al_2O_3 and HfO_2. The barrier heights of Al_2O_3 and HfO_2 are extracted from [84], which are 2.8eV and 1.5eV, respectively. The permittivity is 9 for Al_2O_3 and 25 for HfO_2, which are referred from [85]. The TOX thickness is 100Å. Equivalent oxide thickness (EOT) of oxide-nitride-oxide (ONO) and the physical thickness of other two high-κ IPDs are defined as 140Å. Dielectric parameters of various IPDs are listed in Table 4.1. For comparison, programming of the devices is achieved either by channel-hot-electron injection (CHE) or channel-Fowler-Nordheim injection (CFN). All of the devices are erased by the source-side Fowler-Nordheim (SFN) ejection from the floating gate (FG), by assuming 1×10^{-13} C/μm charges pre-existed in FG. In order to enhance the efficiency of SFN ejection, deeper source junction than drain junction is formed. Cross-sectional view of simulated device

structure is shown in Fig. 4.1. The programming and erasing time is defined as the shift of device threshold voltage (V_{TH}) reaches 3 volts during measurement. After extracting from MEDICI simulator, Al_2O_3 and HfO_2 IPD can increase the gate coupling ration by 45% and 92%, respectively, which can be used to scale down the operation voltage effectively.

4.3 Results and Discussions

According to International Technology Roadmap for Semiconductor (ITRS) criteria, the required IPD thickness for NOR- and NAND-type flash memories is 10-13 nm for next year [28]. However, thickness scaling of ONO IPD using current thermal and/or CVD oxynitride technologies is not sufficient to meet the stringent data retention requirement due to the unavoidable leakage current [30], [32]. Therefore, there is a strong demand to incorporate alternative high-κ dielectrics on nonvolatile memories for enhancing performance while suppressing charge loss.

4.3.1 Basic Characteristics of Flash Memories with High-κ IPDs and SiO_2 TOX

Figure 4.2(a) compares the erased state IPD electric field, defined as IPD voltage/140Å physical thickness, of stacked-gate flash memories as a function of control gate voltage (V_{GS}). The IPD electric field tends to decrease rapidly as κ increases. Since the large IPD electric field across on the erased-state cells will result in more severe charge loss from floating gate to control gate, the flash memories with ONO IPD are expected to possess small programming window than high-κ IPDs. The flash memories with ONO IPD also reduce the electric field on the TOX, as shown in

Fig. 4.2(b). For device performance consideration, flash memories should be fabricated with small IPD electric field and large TOX electric field to obtain superior charge retention and high program/erase (P/E) speed simultaneously. Conventional ONO IPD is charge leaky and hard to P/E, which can not meet the stringent charge retention and flash P/E requirement. Fortunately, flash memories with high-κ IPDs can couple large amount of control gate bias to the floating gate, exhibit small IPD electric field as well as large TOX electric field, which are prone to retain charges and to scale down applied voltages.

The linear region and saturation region transfer characteristics (I_{DS}-V_{GS}) of the stacked-gate flash memories with high-κ IPDs and SiO_2 TOX are displayed in Fig. 4.3. The flash memories with ONO IPD exhibits larger subthreshold swing (SS) and significant off-state current, especially for higher drain biases, which are caused by inevitable drain turn-on. It is known drain turn-on is proportional to the drain coupling ratio (α_D) and inversely proportional to the gate coupling ratio (α_G), which are defined as below [86].

$$C_{total} = C_{IPD} + C_D + C_S + C_{TD} \tag{4-1}$$

$$\text{Drain coupling ratio (GCR)} \quad \alpha_D = \frac{C_D}{C_{Total}} \tag{4-2}$$

$$\text{Gate coupling ratio (DCR)} \quad \alpha_G = \frac{C_{IPD}}{C_{Total}} \tag{4-3}$$

Smaller C_{IPD} in ONO IPD results in smaller α_G and larger α_D, which makes floating gate transistor can go into depletion-mode operation and can conduct current even when $V_{GS} < V_{TH}$. Moreover, drain current of stacked-gate flash memories is also controlled by α_G and capacitive coupling ratio *f*, not as simple as conventional

MOSFET. The relation between I_{DS} and V_{GS} is given by:

$$\text{Linear region} \quad I_{DS}^{Lin} = \mu C_{TD} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - (f - \frac{1}{2\alpha_G}) V_{DS}^2 \right] \quad (4\text{-}4)$$

$$\text{Saturation region} \quad I_{DS}^{Sat} = \frac{\alpha_G}{2} \mu C_{TD} \frac{W}{L} (V_{GS} + f V_{DS} - V_{TH}^2) \quad (4\text{-}5)$$

where $f = \frac{\alpha_D}{\alpha_G} = \frac{C_D}{C_{IPD}}$. As a result, the channel can be turned on by the drain voltage through large *f*, and drive-in current be strongly dependent on the drain voltage, namely drain turn-on phenomenon. With increasing the permittivity of high-κ IPD, both SS and drive current are improved due to higher α_G and higher gate controllability. However, large α_G will increase electric filed on the tunnel dielectrics and enhance gate-induced drain leakage (GIDL).

Figure 4.4 indicates the output characteristics of the stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. Thanks to higher gate coupling, flash memories with high-κ IPDs not only exhibit higher drive-in current than conventional ONO IPD, but also suppress the drain turn-on. Figure 4.5 exhibits the substrate current of flash memories with high-κ IPDs and SiO_2 TOX. Equivalent maximum substrate current is obtained regardless of the κ-value of the IPDs. The maximum channel electric field is determined by the voltage difference between V_{GS} and V_{Dsat}, which is defined as the drain voltage when pinch-off occurs, and expressed by:

$$\text{Channel electric field} \quad E_{\max} \propto V_{DS} - V_{Dsat} \quad (4\text{-}6)$$

$$V_{Dsat} = \alpha_G (V_{GS} + f V_{DS} - V_{TH}) \quad (4\text{-}7)$$

For high-κ IPDs, the channel electric field is suppressed by high gate coupling ratio and generates less impact ionization near drain junction. Since the substrate current is

proportional to the I_{DS} and impact ionization rate, high drain current of high-κ IPDs will be compensated by less impact ionization. Consequently, equivalent substrate current is expected regardless of the κ-value of the IPDs.

4.3.2 Program/Erase Characteristics of Flash Memories with High-κ IPDs and SiO_2 TOX

The CHE current injected to FG of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX is compared in Fig. 4.6(a). Although high-κ IPDs exhibit higher CHE current injection to the FG, the contribution of high-κ IPDs seems unobvious. Figure 4.6(b) calculated CHE injection efficiency, defined as CHE current injected to FG/I_{DS}, similarly unapparent improvement is observed. Merely 2 times improvement of CHE injection efficiency is obtained by changing ONO IPD to high-κ IPDs. Since V_{TH} shift after programming is controlled by injected charges/C_{IPD}, only slightly improvement of programming speed is expected with CHE injection. The CHE programming times as a function of V_{GS} for various IPDs are shown in Fig. 4.7. For the 10 μs programming time, the control gate voltage can be reduced by 16% and 11% with replacing ONO IPD by Al_2O_3 and HfO_2 IPD, respectively. Noteworthy, the improvement of high-κ IPDs disappears at larger control gate voltage.

Figure 4.8 compares the FN tunneling current injected to FG under CFN programming schemes of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. Injected FN current reveals a stronger dependence on the permittivity of the IPDs than HE current. Larger than 80 times FN current increased is observed while replacing ONO IPD to high-κ IPDs. Figure 4.9 shows the relationships between CFN programming time and V_{GS} for flash memories with different IPDs. Obviously, the

programming speed of CFN can be significantly improved using high-κ IPDs. Al_2O_3 can enhance programming speed by one order of magnitude and HfO_2 can improve even further by two orders of magnitude. For the 10 μs programming time, 28% and 51% of V_{GS} reduction can be achieved by changing ONO IPD with Al_2O_3 and HfO_2 IPD, respectively. Compared to the results in Fig. 4.7, the benefit of employing high-κ IPDs is obviously more effective in CFN programming than CHE programming. This is ascribed to that FN tunneling current is exponentially dependent on the electric field, the larger electric field on TOX coupled through high-κ dielectrics, thus, is more efficient in electron injection [21]. On the other hand, CHE injection is controlled by both the electric field on TOX and impact ionization rate. Higher injection efficiency resulting from the higher vertical electric field on TOX will be compensated by the decreasing impact ionization rate, as seen in Fig. 4.5. Therefore, the improvement of CHE programming in operation speed with high-κ IPDs is not as remarkable as that of CFN programming.

Figure 4.10(a) compares the programmed state IPD electric field of the stacked-gate flash memories as a function of V_{GS} with floating drain and substrate. The programmed state has small negative electric field (electrons tunneling to control gate) at zero V_G due to pre-existed negative charges in the FG, and then change to positive electric field (electrons tunneling from control gate) at high negative control gate bias. High positive IPD electric field will result in unwanted carrier injection from control gate to floating gate, flash memory with ONO IPD is expected to possess poor erase window than high-κ IPDs, especially for high voltage erasing. Flash memories with ONO IPD also reduce electric field on TOX and degrade erasing speeds, as shown in Fig. 4.10(b). The corresponding band diagrams of programmed state flash memories with high-κ IPDs and ONO IPD during erasing are shown in Fig.

4.11(a) and (b), respectively. For flash memories with high-κ IPDs, small negative electric field on IPD and large positive electric field on SiO_2 TOX induced by high gate coupling ratio will enhance electron ejection from FG to control gate and source region simultaneously, which is expected to exhibit fast erasing speed and large erasing window. However, large positive electric field across on ONO IPD will degrade both erasing speed and erasing window due to unwanted electron injection from control gate to FG.

Figure 4.12 compares the FN tunneling current ejected from FG under SFN erasing schemes of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. Ejected FN current reveals a strong dependence on the permittivity of the IPDs. Similar to CFN programming, larger than 80 times FN current increase is observed while replacing ONO IPD to high-κ IPDs during erase. SFN erasing time verse V_G for memories with high-κ IPDs and SiO_2 TOX is shown in Fig. 4.13. Employing high-κ dielectrics as the IPD can also tremendously improve erasing speed. Al_2O_3 and HfO_2 IPD can reduce erasing time by one and two order of magnitude, respectively. For the 0.1 ms erasing time, Al_2O_3 can reduce the erasing voltage by 31% while HfO_2 can further diminish erasing voltage by more than 48%. In summary, operation voltage reductions are listed in Table 4.2. Even though the improvement is more obvious in FN injection than HE injection, our simulation results clearly indicate stacked-gate flash memories with high-κ IPDs and SiO_2 TOX can be used to replace both NAND- and NOR-type flash cells, in terms of control gate voltage reduction and operation speed promotion.

The improvement of P/E speed is found to be more significant between ONO IPD and Al_2O_3 IPD than between Al_2O_3 IPD and HfO_2 IPD. In order to investigate the effect of dielectrics with higher κ value, an artificial dielectric with κ equal to 50 and

φ_B larger than 1.5eV is employed for comparison. The results in Fig. 4.2 - 4.13 show that only slightly improvement in P/E speed is observed when κ is changed from 25 to 50. Voltage reduction ratio will be rapidly saturated as κ becomes larger than 25. Hence, it can be claimed that very high-κ dielectrics may not be an effective IPD candidates for stacked-gate flash memories even though they have a φ_B larger than 1.5eV.

4.4 Summary

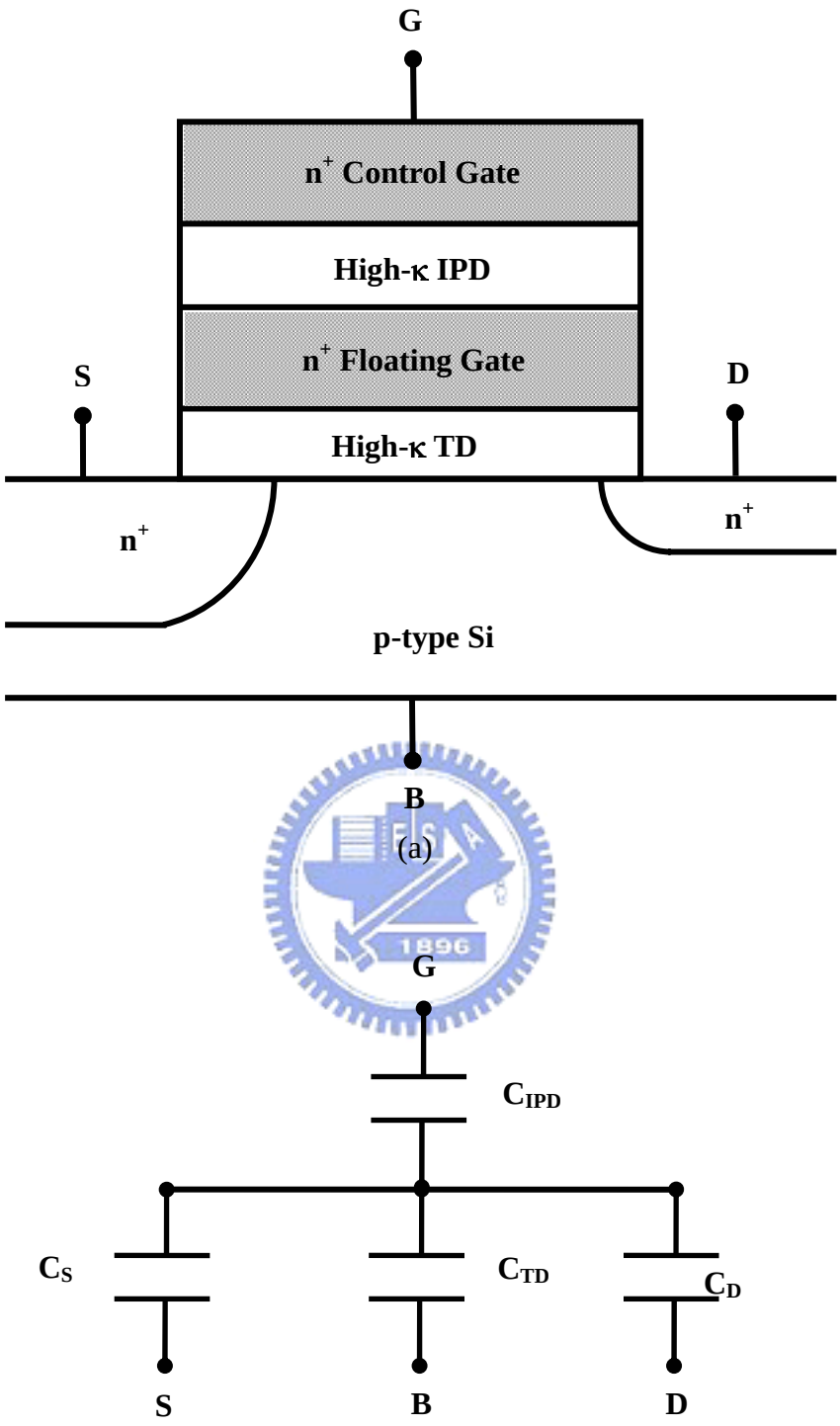
In order to realize high speed and low power operation of flash memory technologies, devices with high coupling ratio are necessary. From MEDICI simulation, Al_2O_3 IPD and HfO_2 IPD can increase gate-coupling ratio by 45% and 92%, respectively. By 2-D MEDICI simulation, flash memories with high-κ IPDs clearly exhibit significant improvement in programming/erasing speed over those with conventional ONO IPD. Moreover, it is found that high-κ IPDs are more effective for the memories programmed/erased with FN tunneling rather than channel hot carrier injection. Choosing HfO_2 as the IPD and using FN programming/erasing scheme, the operating voltage can be reduced 48% at a typical program time of 10 μs and 0.1 ms erasing time. Therefore, Al_2O_3 and HfO_2 with medium high κ value and sufficient barrier height show the great potential for the application of high seed and low voltage flash memories. Our results also show that dielectrics with very high permittivity (κ > 25) may not be necessary for the IPD in stacked-gate flash memories. As a result, high-κ IPDs are suitable for next generation NAND-type stacked-gate flash memories.

Table 4.1 Dielectric constants and conduction band offsets with respect to Si of the IPD materials with fixed SiO_2 TOX for simulated stacked-gate flash memories. * : physical thickness ~180Å, EOT ~ 140Å. ** : artificial high-κ material with sufficient κ-value and ΔE_C.

	IPD Thickness	κ	ΔE_C (φ_B)
ONO	**140Å***	**~ 5**	
Al_2O_3	**140Å**	**9**	**2.8**
HfO_2	**140Å**	**25**	**1.5**
κ = 50**	**140Å**	**50**	**1.5**

Table 4.2 Operation voltage reduction of stacked gate flash memories with high-κ IPDs and SiO_2 TOX.

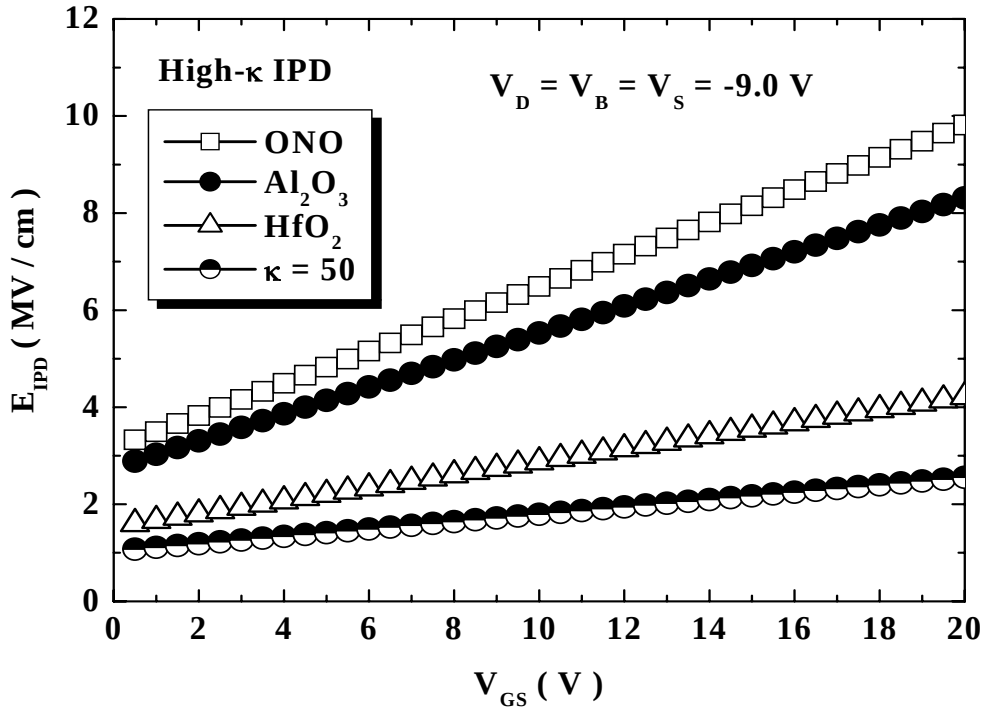
		κ = 50	HfO_2	Al_2O_3	ONO
GCR		**0.895**	**0.814**	**0.615**	**0.424**
DCR		**0.016**	**0.029**	**0.067**	**0.112**
SCR		**0.041**	**0.076**	**0.171**	**0.266**
GCR Improvement		**110.91%**	**91.87%**	**44.98%**	
DCR Improvement		**85.68%**	**73.77%**	**39.75%**	
SCR Improvement		**84.56%**	**71.56%**	**35.56%**	
10μs CHE Program	**V_{GS}**	**11.01**	**10.05**	**9.5**	**11.35**
	Improvement	**3.00%**	**11.45%**	**16.30%**	
10μs CFN Program	**V_{GS}**	**6.89**	**7.65**	**11.41**	**15.88**
	Improvement	**56.61%**	**51.83%**	**28.15%**	
0.1ms SFN Erase	**V_{GS}**	**-5.74**	**-6.23**	**-8.2**	**-12.04**
	Improvement	**52.33%**	**48.20%**	**31.83%**	



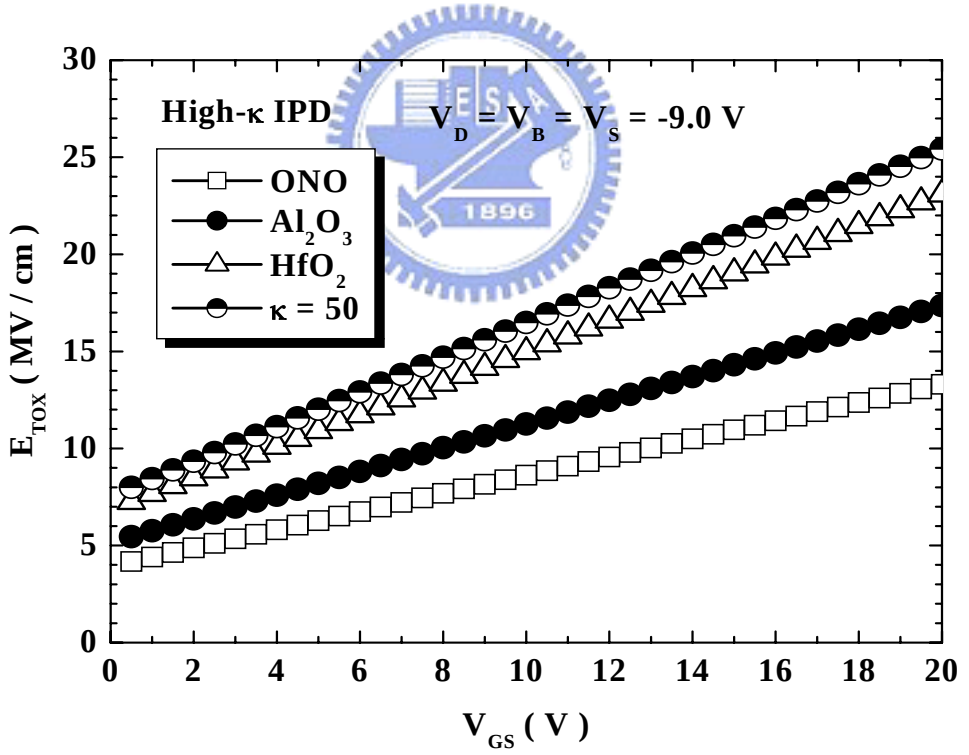
(a)

(b)

Fig. 4.1 (a) Simulated 0.45μm n-channel device structure (b) equivalent electrical model of stacked-gate flash memories with several high-κ IPDs and TDs. Asymmetry source/drain junction for enhanced source-side erasing efficiency. Programming by either CHE or CFN injection; erasing by SFN erasing.

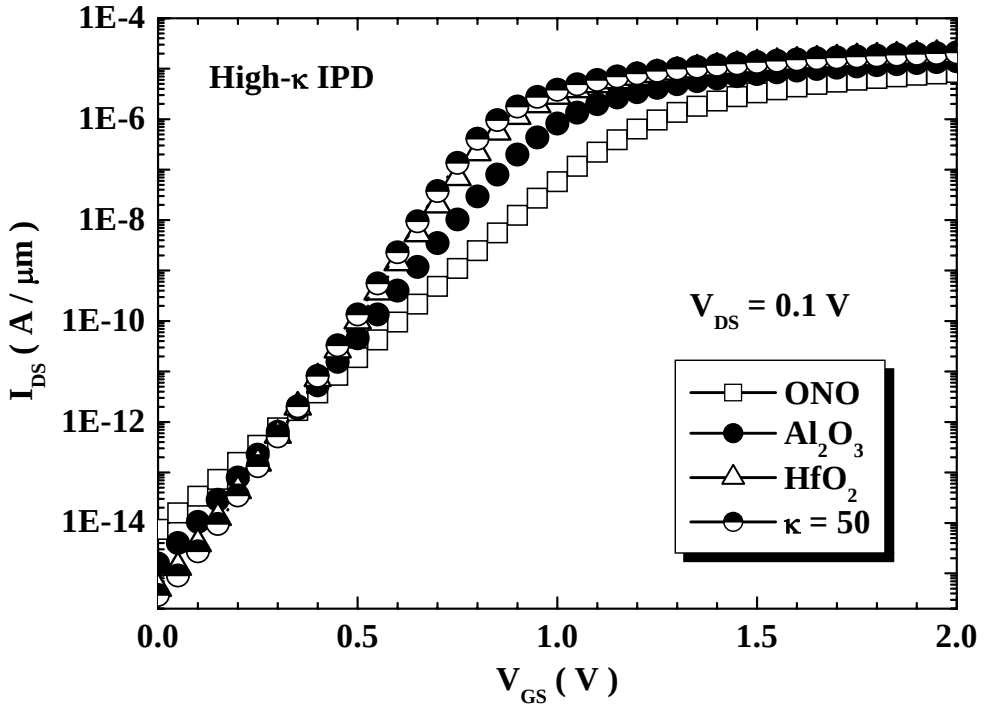


(a)

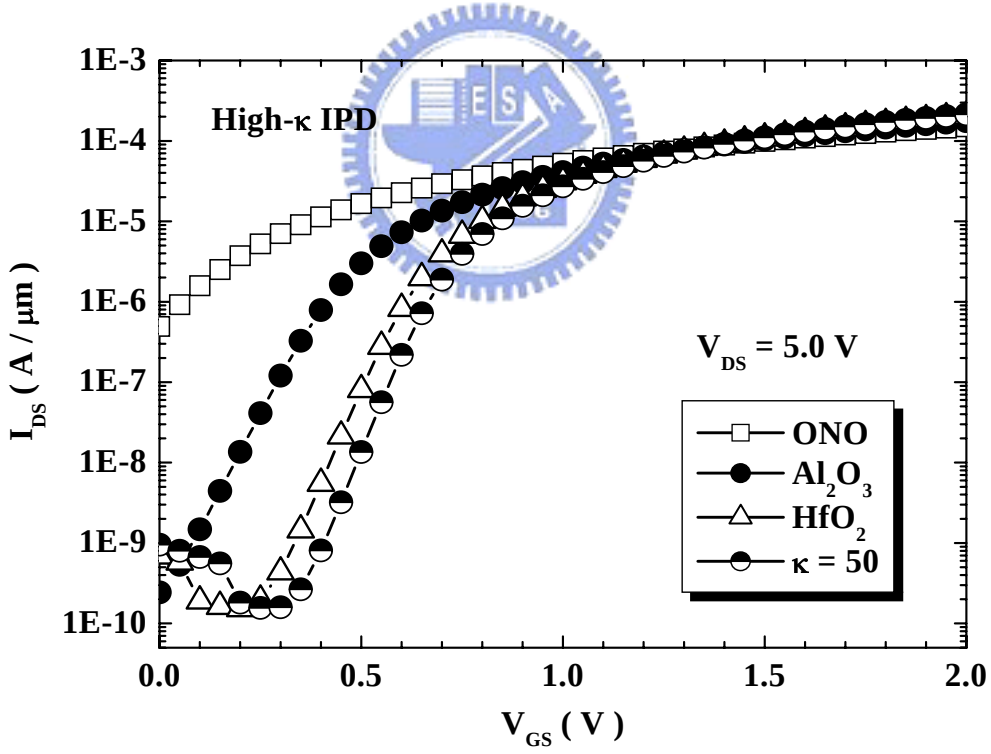


(b)

Fig. 4.2 (a) IPD (b) TOX electric field as a function of control gate voltages of erased state stacked-gate flash memories with high-κ IPDs and SiO_2 TOX under $V_D = V_B = V_S = -9.0$V. High-κ IPDs can reduce IPD electric field as well as enhance TOX electric field.



(a)



(b)

Fig. 4.3 (a) Linear region (b) saturation region transfer characteristics of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. High-κ IPDs can increase drive-in current as well as enhance gate control ability, especially at high drain voltage.

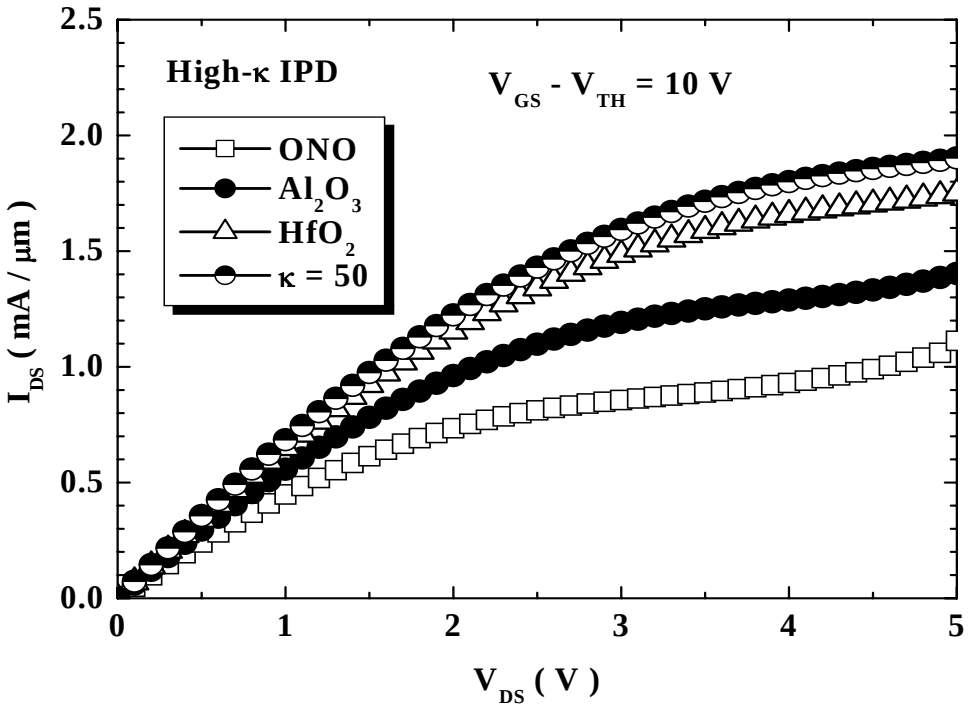


Fig. 4.4 Output characteristics of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX at (V_{GS} - V_{TH}) = 10V.

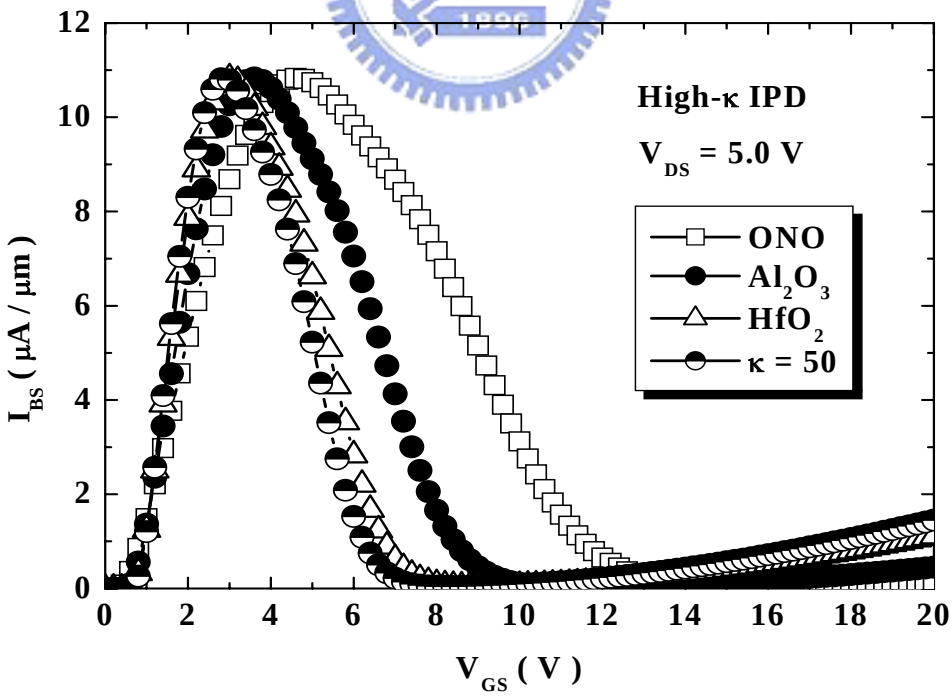
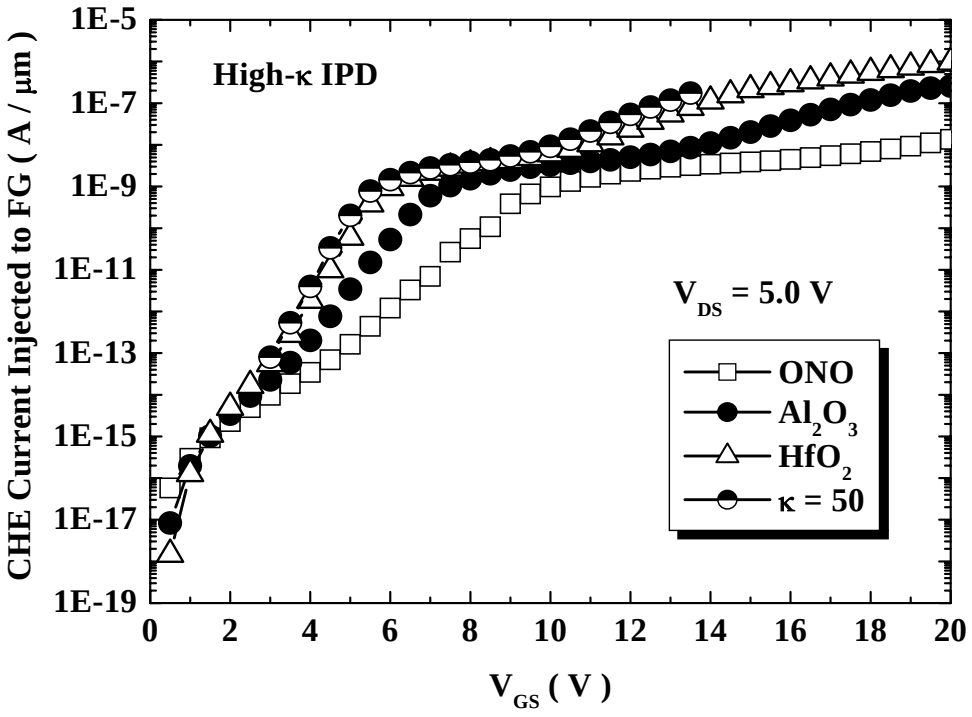
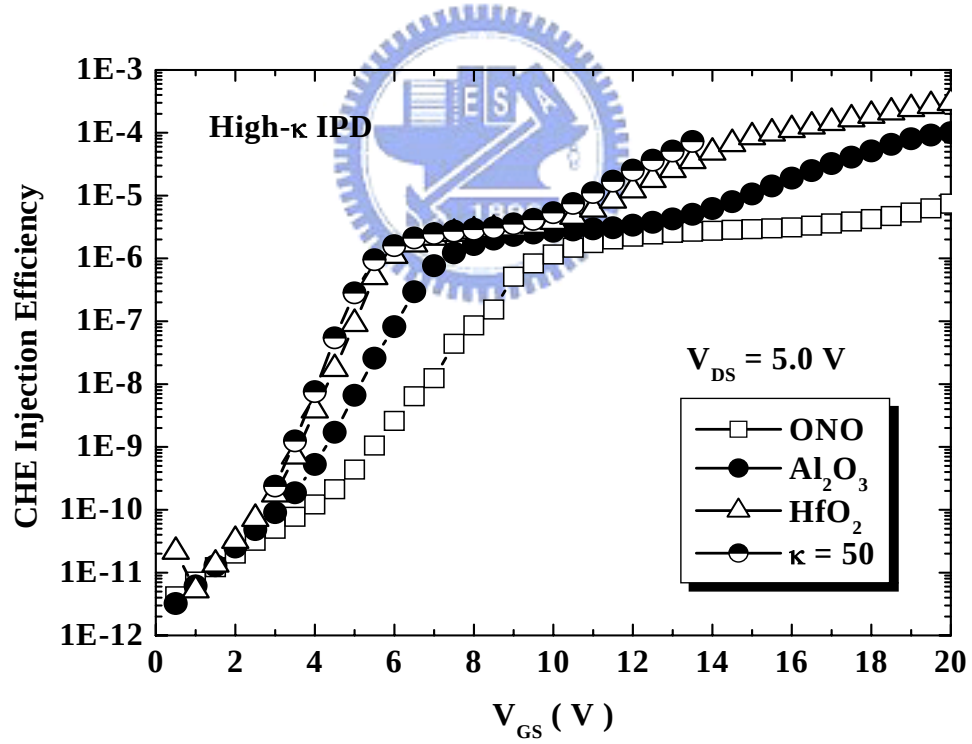


Fig. 4.5 Substrate current of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. Maximum substrate current is independent of the κ-values.



(a)



(b)

Fig. 4.6 (a) CHE current injected to FG (I_{FG}) (b) CHE injection efficiency (defined as I_{FG}/I_{DS}) as a function of control gate voltages of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. High-κ IPDs slightly enhance injection efficiency than ONO IPD, but not significantly.

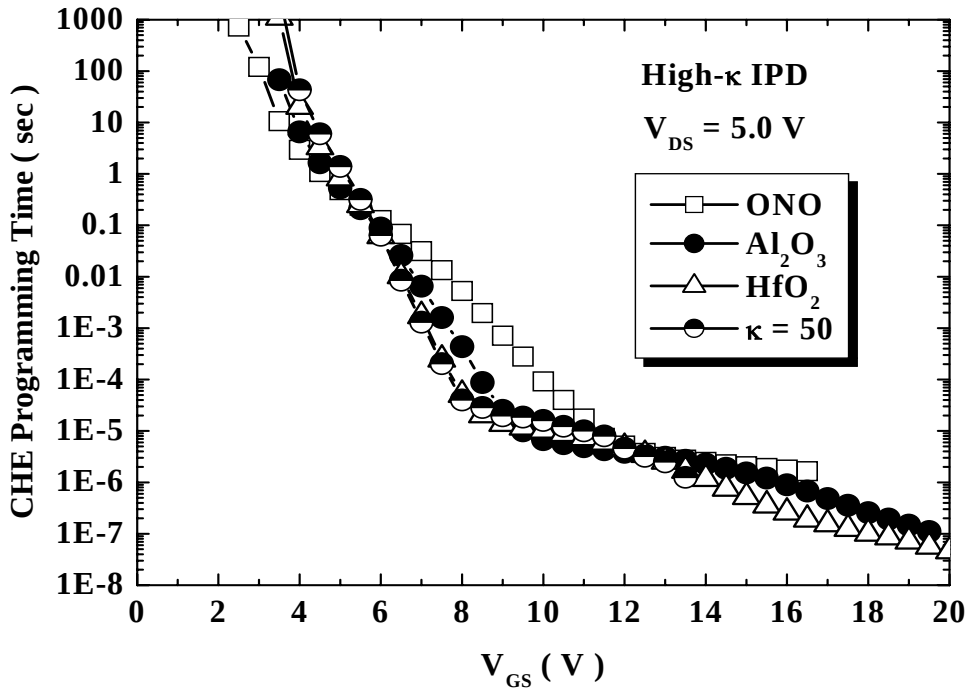


Fig. 4.7 CHE programming time as a function of control gate voltages of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX.

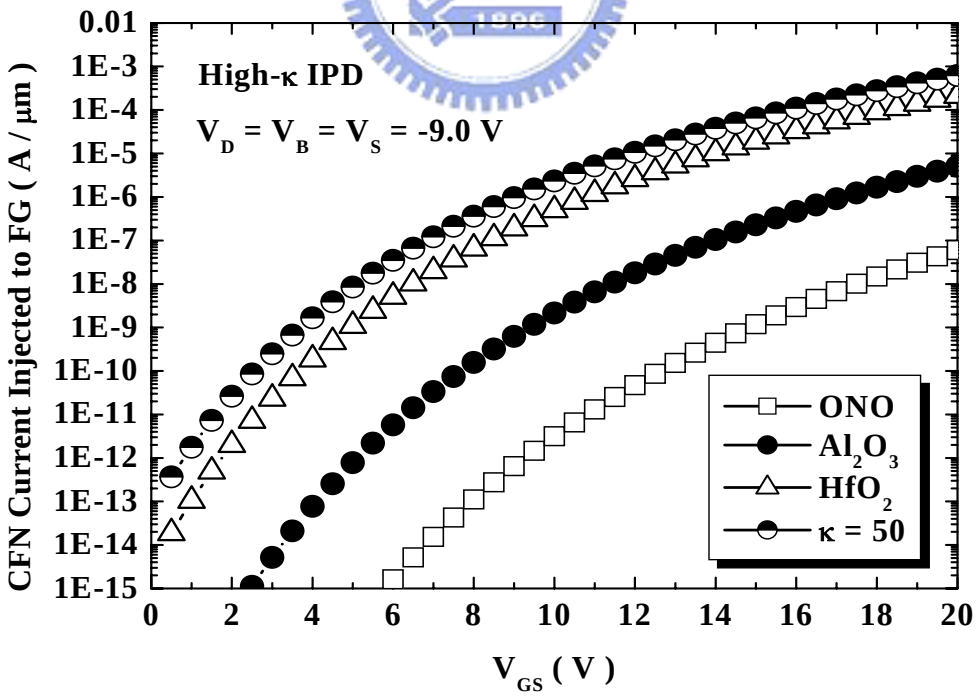


Fig. 4.8 CFN current injected to FG as a function of control gate voltages of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX.

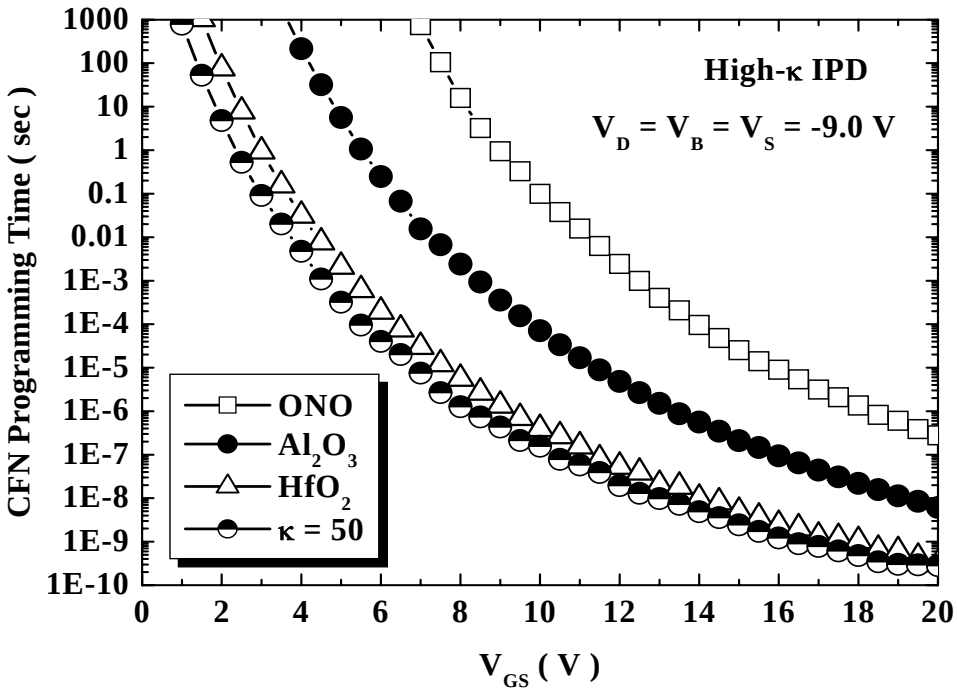
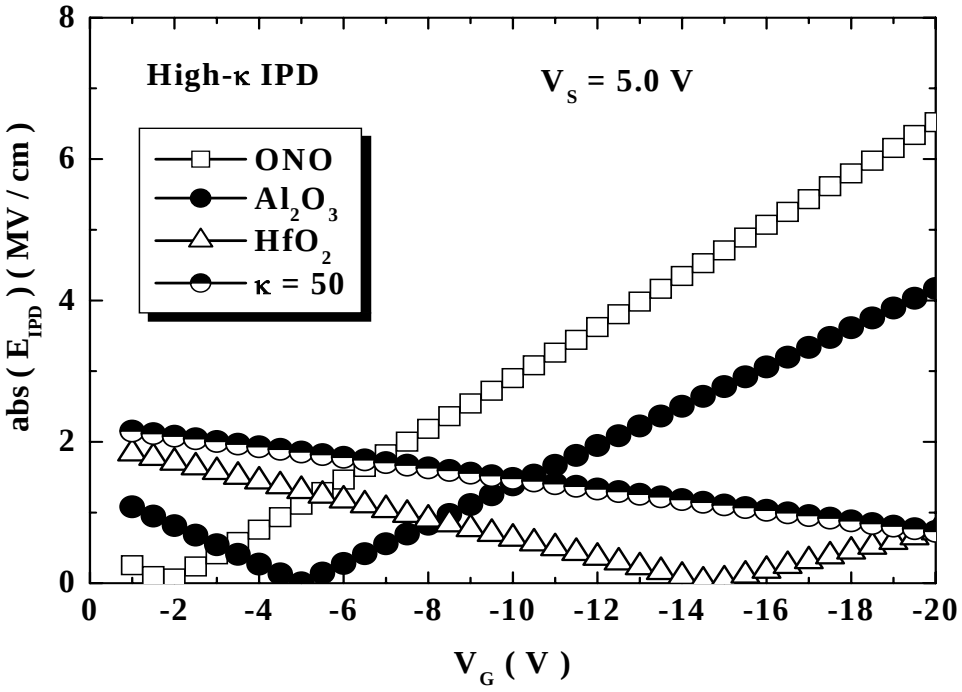
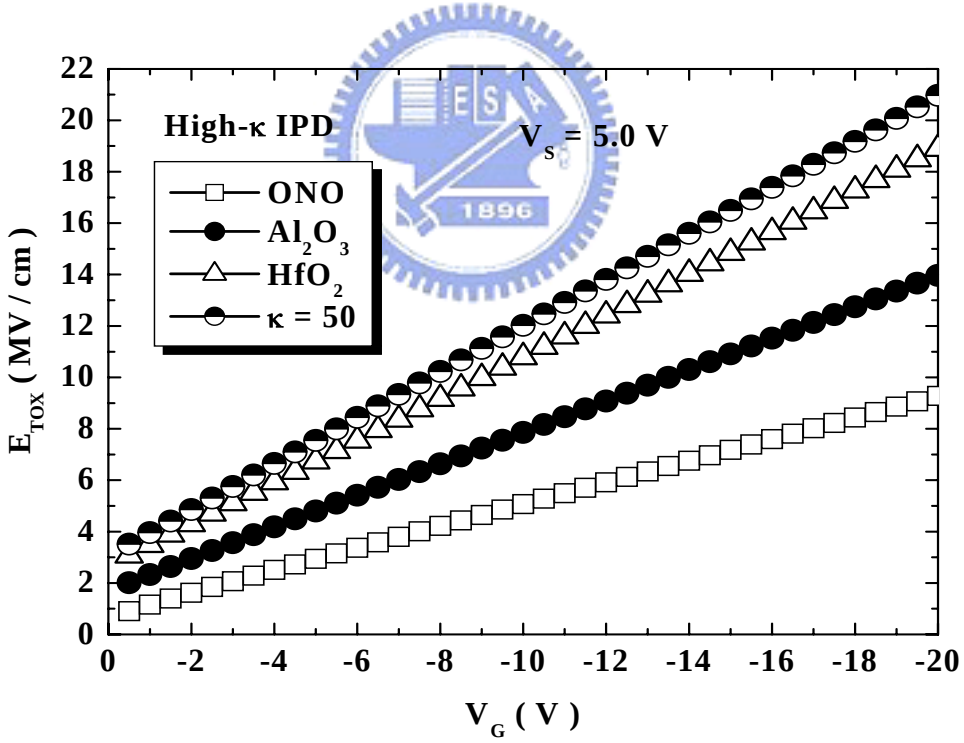


Fig. 4.9 CFN programming time as a function of control gate voltages of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. Significant improvement in CFN programming speed for high-κ IPDs is indicated.

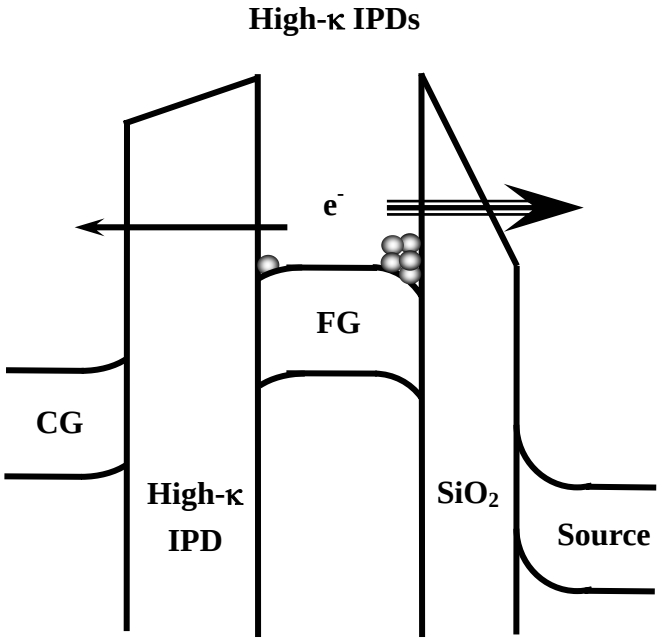


(a)

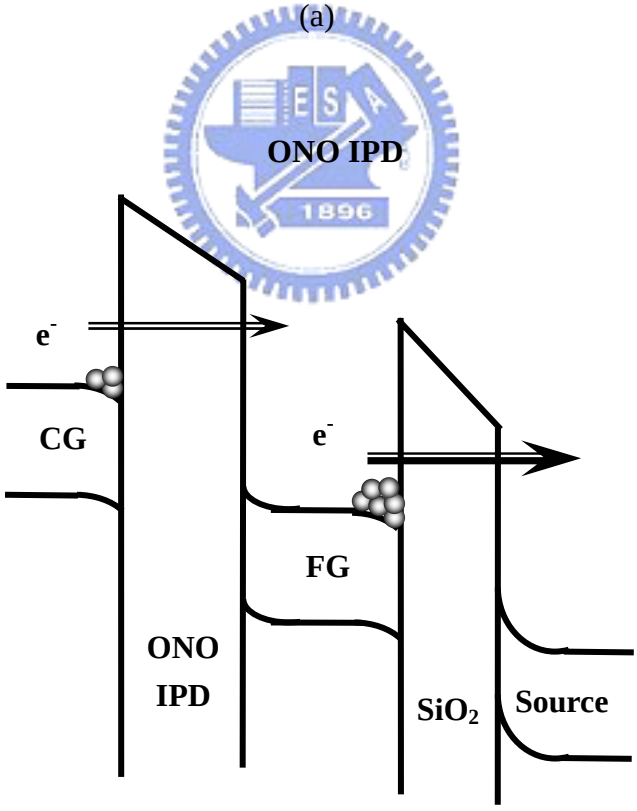


(b)

Fig. 4.10 (a) Absolute IPD (b) TOX electric field as a function of control gate voltages of programmed state stacked-gate flash memories with high-κ IPDs and SiO_2 TOX under V_S = 5.0V. Drain and substrate terminals are floating. High-κ IPDs can reduce IPD electric field as well as enhance TOX electric field.



(a)



(b)

Fig. 4.11 Band diagrams of programmed state flash memories at the outset of erase for (a) high-κ IPDs and (b) ONO IPD.

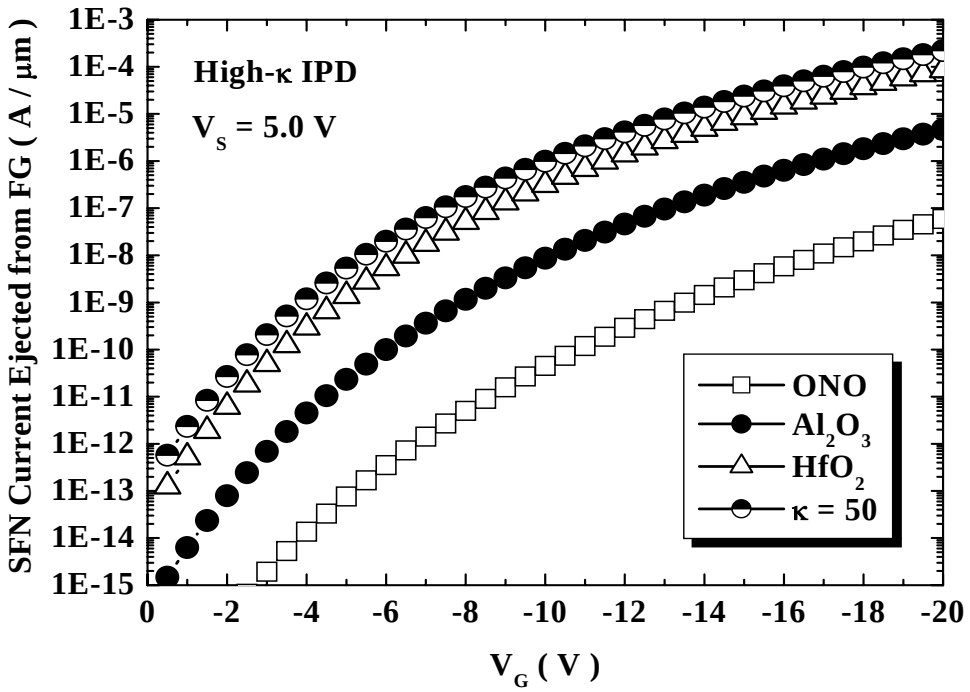


Fig. 4.12 SFN current ejected from FG of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX under V_S = 5.0V, floated drain and substrate terminal.

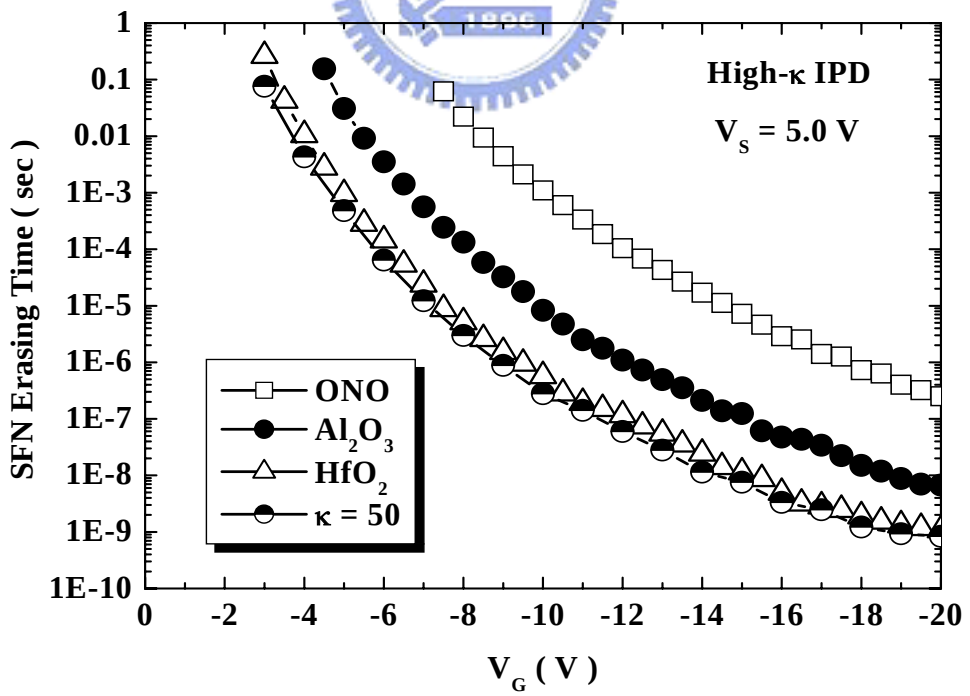


Fig. 4.13 SFN erasing time of stacked-gate flash memories with high-κ IPDs and SiO_2 TOX. High-κ IPDs crucially improve SFN erasing speed.

CHAPTER 5

Simulated Characteristics of Stacked-Gate Flash Memories with HfO_2 IPD and High-κ Tunnel Dielectrics

5.1 Introduction

In recognizing the high speed and low power operation of flash memory technologies, the employment of high-permittivity (κ) tunnel dielectrics (TDs) in flash memories has attracted much attention in order to reduce stress-induced reliability degradation in conventional SiO_2 tunnel oxide (TOX) [28], [33]. The tunnel dielectric of flash memories has two roles. One is playing as a barrier to suppress charge leakage under ~3 MV/cm equivalent oxide field of read and retention. Hence, we need an appropriate barrier height and thickness. Second role is a charge transfer path. It must be robust enough under 10 MV/cm high field or 5V hot electron energy during charge injection mode, and both trapping and detrapping sites creation rates should be substantially suppressed. In order to avoid trap-assisted tunneling via one trap site, the minimum TOX thickness of conventional FG structure will be limit to 8 nm. This limits the tunnel SiO_2 scaling and program/erase voltage reduction. Nitrided oxides have been intensively studied, but so far only 5 to 10 times improvement for low field leakage is achieved [33]. This is not enough, because it only achieves 1 nm reduction even with heavy nitridation.

Among various materials, both Ta_2O_5 and TiO_2 have narrow band gap resulting

in too low electron barrier height (φ_B) [84]. These films are not suitable from the viewpoint of flash reliability and thermally excited current. On the other hand, Si_3N_4, Al_2O_3, ZrO_2 and HfO_2 have reasonable bandgaps and barrier heights, these dielectrics are then the potential candidates [84]. In this chapter, the effects of high-κ materials Si_3N_4, Al_2O_3 and HfO_2 serving as the TD of flash memories were studied with different programming and erasing schemes through 2-D MEDICI simulator. High-κ dielectrics served as the TD to replace SiO_2 TOX can improve tunneling probability due to smaller φ_B. However, gate coupling ratio degrades as the dielectric constant of the TD increasing, which confines the high-κ TDs to be programmed and erased with hot-electron injection. Due to the contrary programming/erasing schemes compared to the high-κ IPDs, high-κ TDs are suitable for next decade NOR-type stacked-gate flash memories in terms of voltage reduction.

5.2 Simulation Details

To examine the impact of high-κ TDs, simulations are carried out using the conventional stacked-gate flash cell with fixed HfO_2 IPD. Two-dimensional MEDICI [83] simulator is employed for the performance simulations of a 0.45μm stacked-gate n-channel flash memory with several kinds of high dielectric constant TD. They are Si_3N_4, Al_2O_3 and HfO_2. The barrier heights of Al_2O_3 and HfO_2 are extracted with the technique used in Ref. 84, which are 2.8eV and 1.5eV, respectively. The permittivity is 9 for Al_2O_3 and 25 for HfO_2, which are referred from Ref. 85. The physical thickness of HfO_2 IPD and various tunnel dielectrics is 140Å and 100Å, respectively. Dielectric parameters of various tunnel dielectrics are listed in Table 5.1. For comparison, programming of the devices is achieved either by channel-hot-electron

injection (CHE) or channel-Fowler-Nordheim injection (CFN). All of the devices are erased by the source-side Fowler-Nordheim (SFN) ejection from the floating gate (FG), by assuming 1×10^{-13} C/μm charges pre-existed in FG. In order to enhance the efficiency of SFN ejection, deeper source junction than drain junction is formed. Cross-sectional view of simulated device structure is the same with Fig. 4.1. The programming and erasing time is defined as the shift of device threshold voltage (V_{TH}) reaches 3 volts during measurement.

5.3 Results and Discussions

According to International Technology Roadmap for Semiconductor (ITRS) criteria, the required TD thickness for NOR- and NAND-type flash memories is less than 7nm for next year [28]. However, thickness scaling of SiO_2 tunneling oxide has been strongly limited by the unavoidable stress-induced leakage current caused by 1×10^5 program/erase cycling [87], [88]. Therefore, there is a strong demand to incorporate alternative high-κ dielectrics on nonvolatile memories for enhancing performance while suppressing charge loss.

5.3.1 Basic Characteristics of Flash Memories with HfO_2 IPD and High-κ TDs

Figure 5.1(a) compares the HfO_2-IPD electric field of stacked-gate flash memories as a function of control gate voltage (V_{GS}) with various high-κ TDs. Since larger IPD electric field across on erased-state cells will result in more severe charge loss from floating gate to control gate, the flash memories with high-κ TDs are expected to possess smaller programming window than SiO_2 TOX. The flash

memories with high-κ TDs also reduce the electric field on the TD, defined as TD voltage/100Å physical thickness, as shown in Fig. 5.1(b). Therefore, the flash memories with high-κ TDs will reduce capacitive coupling from control gate to floating gate, exhibit large IPD electric field as well as small TD electric field.

Linear and saturation region transfer characteristics of the stacked-gate flash memories with various high-κ TDs are shown in Fig. 5.2. The flash memories with high-κ TDs not only depict the degraded subthreshold swing but also exhibit significantly large off-state current, especially for high drain bias, which are caused by the inevitable drain turn-on and the reduced gate coupling ratio. As the permittivity of tunnel dielectrics increases, more amount of drain voltage is coupled to floating gate, and deteriorates control gate controllability. Figure 5.3 indicates the output characteristics of stacked-gate flash memories with high-κ TDs. Albeit the high-κ TDs increase the drive current, remarkable drain turn-on are also observed. Figure 5.4 exhibits the substrate current of the flash memories with HfO_2 IPD and high-κ TDs. Referring to eq. (4-6) and (4-7), the maximum channel electric field of the high-κ TDs is larger than SiO_2 TOX due to reduced gate coupling. Consequently, the high-κ TDs will increase drain current as well as enhance impact ionization, contributing to larger than 2 times maximum substrate current increment. This result clearly reveals that the high-κ TDs can increase hot electron injection and the improvement in CHE programming can be predicted.

5.3.2 Program/Erase Characteristics of Flash Memories with HfO_2 IPD and High-κ TDs

The CHE current injected to the FG of the stacked-gate flash memories with

HfO_2 IPD and high-κ TDs is compared in Fig. 5.5(a). By replacing SiO_2 TOX to high-κ tunnel dielectrics, the injected hot electron current from the substrate to the FG is obviously increased. Figure 5.5(b) shows the calculated CHE injection efficiency of the stacked-gate flash memories with HfO_2 IPD and high-κ TDs. Similarly, the enhanced injection efficiency is obtained by increasing the κ-value of the tunnel dielectrics. The CHE programming times as a function of V_{GS} for various TDs are shown in Fig. 5.6. For the 10 μs programming time, the control gate voltage can be reduced by 16%, 18% and 27% with replacing SiO_2 TOX to Si_3N_4, Al_2O_3 and HfO_2 TD, respectively. Although the electric field on high-κ tunnel dielectrics is lower than SiO_2 TOX, enhanced impact ionization rate and lower φ_B contribute to higher CHE programming speed. As a result, the flash memories with HfO_2 IPD and high-κ TDs are suitable to supplant presently tunneling oxide in NOR-type array architectures.

Figure 5.7 compares the FN tunneling current injected to FG under CFN programming schemes of the stacked-gate flash memories with HfO_2 IPD and high-κ TDs. Injected FN current reveals a stronger dependence on the permittivity of the TDs than HE current. More than 10 times FN current reduction is observed while replacing tunneling oxide to high-κ TDs. Figure 5.8 shows the relationships between CFN programming time and V_{GS} for flash memories with different TDs. Obviously, the degradation of CFN programming speed can be ascribed to the reduced tunneling current from substrate into the FG. Compared to the results in Fig. 5.6, the benefit of employing high-κ TDs is obviously only effective in CHE programming rather than in CFN programming. This is ascribed to that FN tunneling current is exponentially dependent on the electric field, the smaller electric field on high-κ TDs reduces electron injection efficiency than SiO_2 TOX. Therefore, the application of the high-κ TDs in the stacked-gate flash memories with CFN programming is unbeneficial,

contrary to the CHE programming.

Figure 5.9(a) compares the programmed state IPD electric field of the stacked-gate flash memories as a function of V_{GS} with floating drain and substrate. Increasing the κ-value of the TDs will lead to undesired IPD electric field increment, the high-κ TDs may deteriorate erase window through charge injection between the FG and the control gate. As seen in Fig. 5.9(b), the flash memories with high-κ TDs also reduce electric field on the TDs and degrade erasing speeds, similar to the CFN programming. Referring to Fig. 4.11, large positive electric field for flash memories with high-κ TDs will limit electron in the FG to be erased through tunnel dielectrics while enhance unwanted electron injection from control gate to FG. Consequently, flash memories with HfO_2 IPD and high-κ TDs are therefore expected to reduce erasing speed as well as narrow down erasing window. Figure 5.10 compares the FN tunneling current ejected from the FG under SFN erasing schemes of the stacked-gate flash memories with HfO_2 IPD and high-κ TDs. Ejected FN current reveals a strong dependence on the permittivity of the TDs. Similar to the CFN programming, larger than 80 times FN current reduction is observed while replacing SiO_2 TOX to high-κ TDs during erase. The SFN erasing time verse V_G for flash memories with HfO_2 IPD and high-κ TDs is shown in Fig. 5.11. Employing high-κ dielectrics as the TD also tremendously degrades erasing speed directly ascribed to the decreased gate coupling ratio, which is larger than 18% and 48% for Al_2O_3 TD and HfO_2 TD, respectively. In summary, operation voltage reductions are listed in Table 5.2.

Consider CHE programming scheme, the flash memories with HfO_2 IPD and high-κ TDs exhibit larger than 18% and 27% voltage reduction for Al_2O_3 TD and HfO_2 TD, respectively. The improvement is apparently greater than the flash memories with high-κ IPDs. Our simulation results clearly indicate stacked-gate flash

memories with HfO_2 IPD and high-κ TDs can be used to replace conventional NOR-type flash cells, in terms of control gate voltage scaling and operation speed promotion.

5.4 Summary

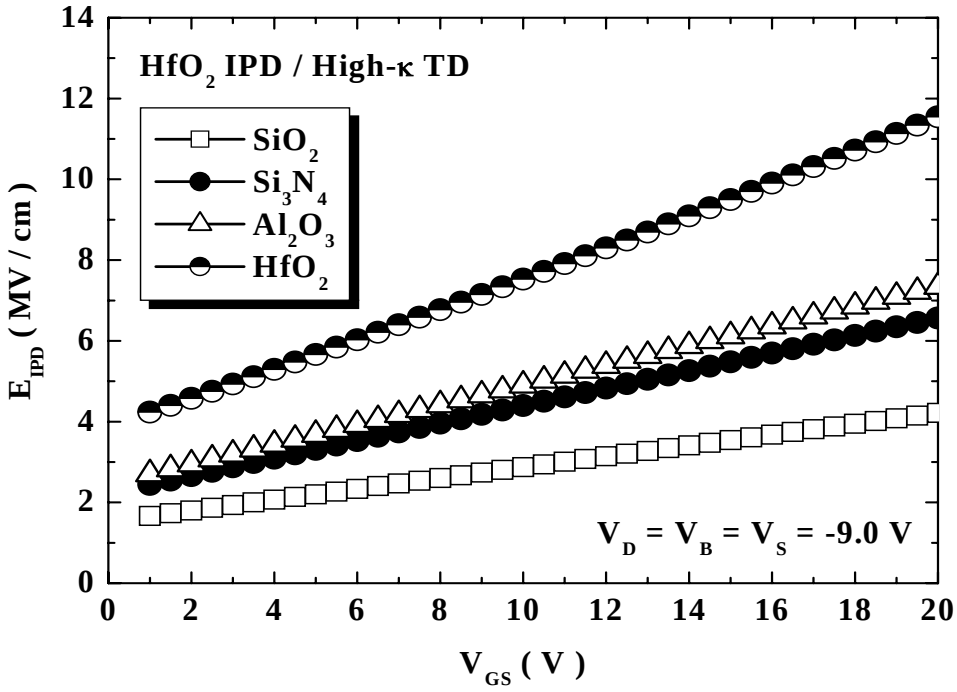
The effects of high-κ TDs on program/erase performance of the stacked-gate flash memories are investigated. The results are quite contrary with respect to high-κ IPD. Due to the reduced gate coupling ratio, the programming/erasing speed of the stacked-gate flash memories with high-κ TDs by using FN tunneling is helpless in operation voltage reduction. On the other hand, the increased electric field on HfO_2 IPD would produce excess charge loss and narrow the operation window between programmed and erased state. Although the electric field on high-κ tunnel dielectrics is lower than SiO_2 TOX, enhanced impact ionization rate and lower φ_B contribute to higher CHE injection current and efficiency. Consequently, high-κ TDs are only effective for the memories programmed/erased with hot electron injection rather than FN tunneling. Due to the contrary improvement in programming/erasing schemes with respect to high-κ IPDs described in Chapter 4, high-κ TDs are suitable for next decade NOR-type stacked-gate flash memories.

Table 5.1 Dielectric constants and conduction band offsets with respect to Si of the TD materials with fixed HfO_2 IPD for simulated stacked-gate flash memories.

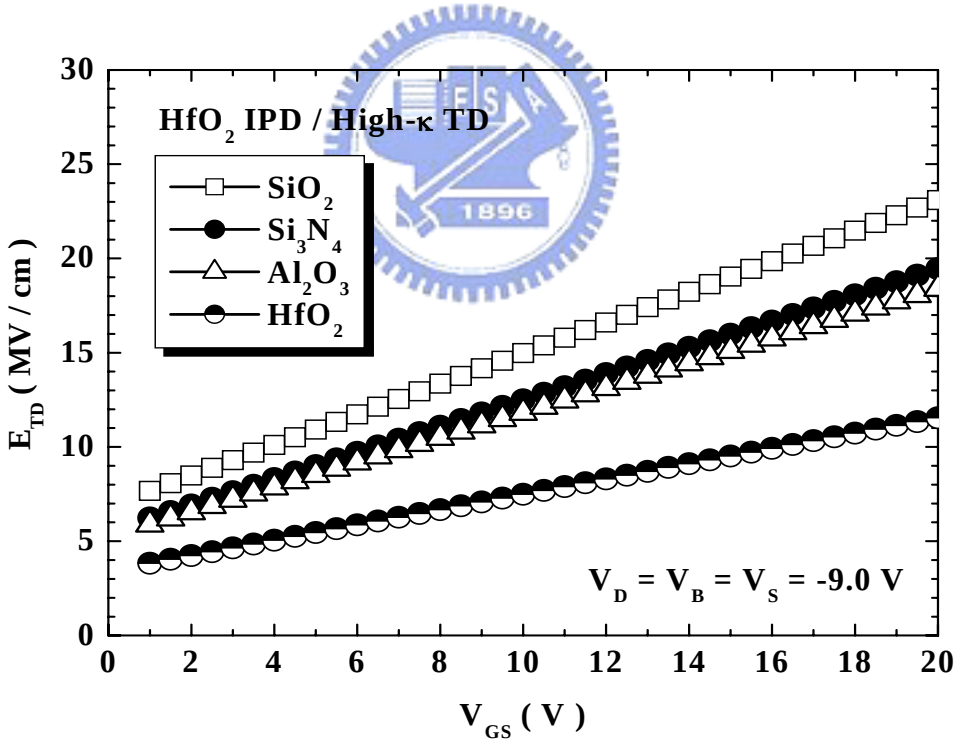
	TD Thickness	κ	ΔE_C (φ_B)
SiO_2	**100Å**	**3.9**	**3.2**
Si_3N_4	**100Å**	**7.5**	**2.1**
Al_2O_3	**100Å**	**9**	**2.8**
HfO_2	**100Å**	**25**	**1.5**

Table 5.2 Operation voltage reduction of stacked gate flash memories with HfO_2 IPD and high-κ TDs.

		HfO_2	Al_2O_3	Si_3N_4	SiO_2
GCR		**0.422**	**0.662**	**0.701**	**0.814**
DCR		**0.056**	**0.042**	**0.039**	**0.029**
SCR		**0.236**	**0.138**	**0.122**	**0.076**
GCR Degradation		**-48.03%**	**-18.37%**	**-13.72%**	
DCR Degradation		**-86.29%**	**-39.80%**	**-30.77%**	
SCR Degradation		**-206.89%**	**-79.71%**	**-59.04%**	
10μs CHE Program	**V_{GS}**	**7.33**	**8.25**	**8.42**	**10.05**
	Improvement	**27.08%**	**17.91%**	**16.19%**	
10μs CFN Program	**V_{GS}**	**13.72**	**10.92**	**9.97**	**7.65**
	Degradation	**-79.35%**	**-42.75%**	**-30.33%**	
0.1ms SFN Erase	**V_{GS}**	**-11.01**	**-8.83**	**-7.82**	**-6.23**
	Degradation	**-76.73%**	**-41.73%**	**-25.52%**	

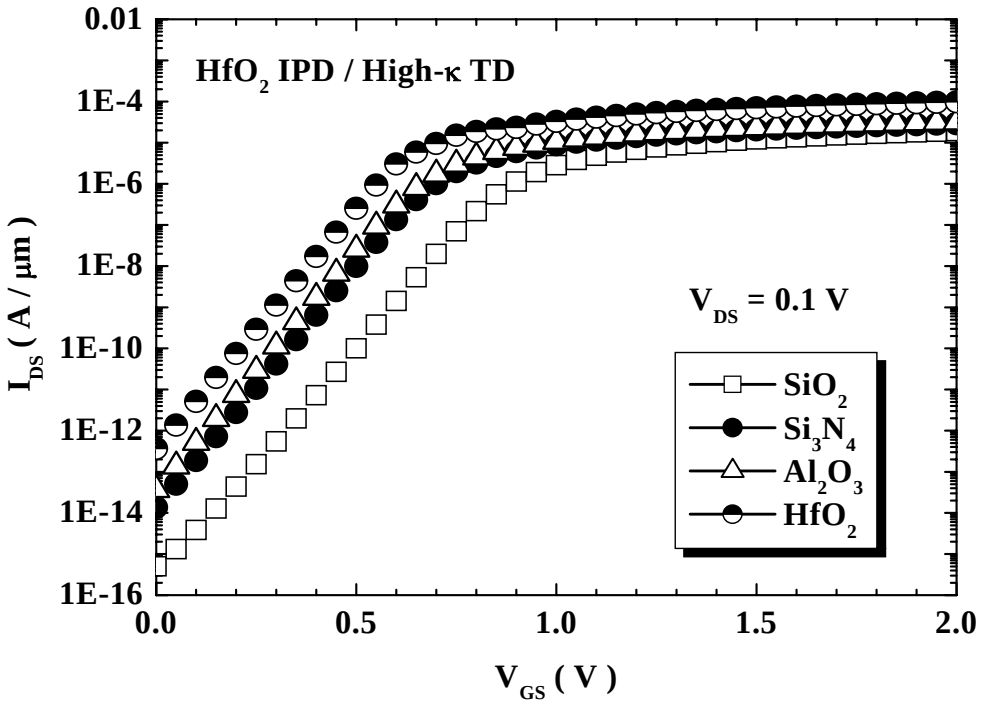


(a)



(b)

Fig. 5.1 (a) IPD (b) TD electric field as a function of control gate voltages of erased state stacked-gate flash memories with HfO_2 IPD and high-κ TDs under $V_D = V_B = V_S = -9.0V$. High-κ TDs can increase IPD electric field as well as reduce TD electric field.



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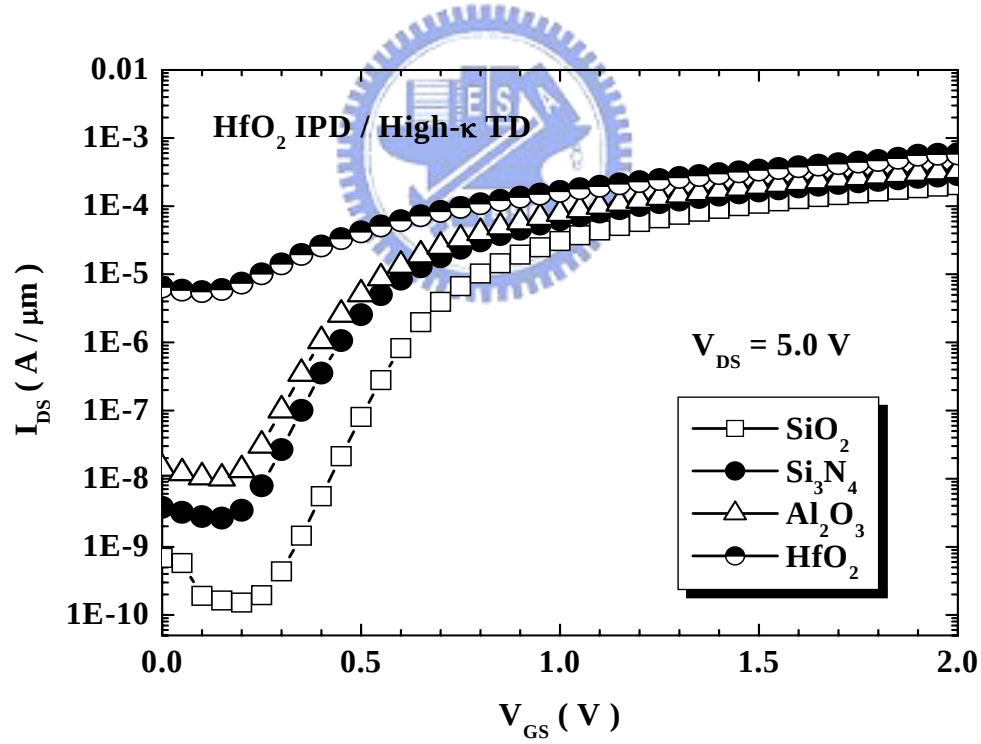


(b)

Fig. 5.2 (a) Linear region (b) saturation region transfer characteristics of stacked-gate flash memories with HfO_2 IPD and high-κ TDs. The flash memories with HfO2 IPD and high-κ TDs not only depict the degraded subthreshold swing but also exhibit significantly large off-state current.

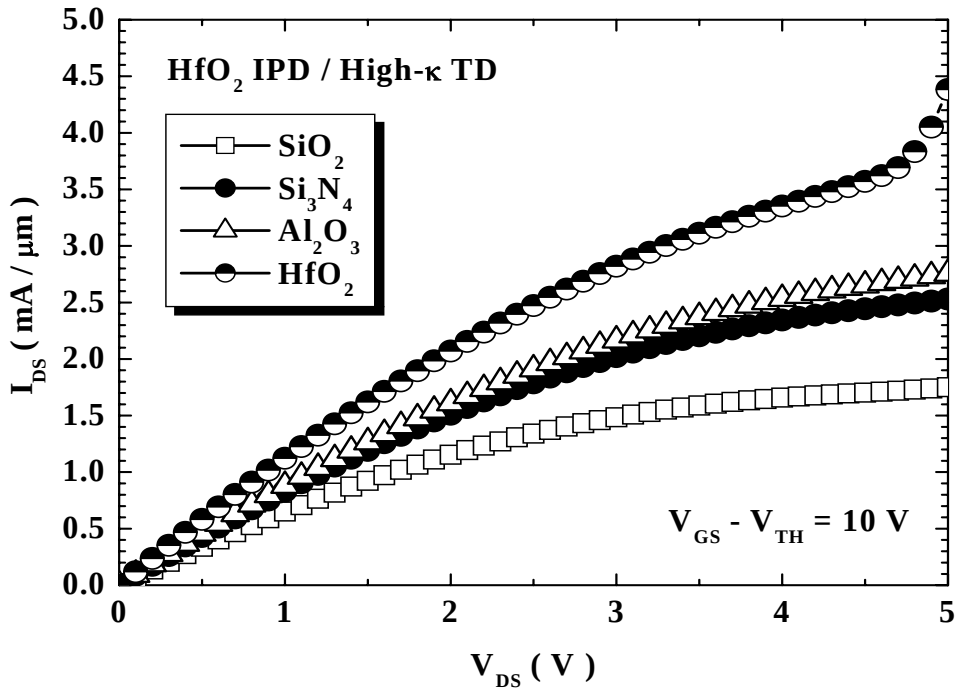


Fig. 5.3 Output characteristics of stacked-gate flash memories with HfO_2 IPD and high-κ TDs.

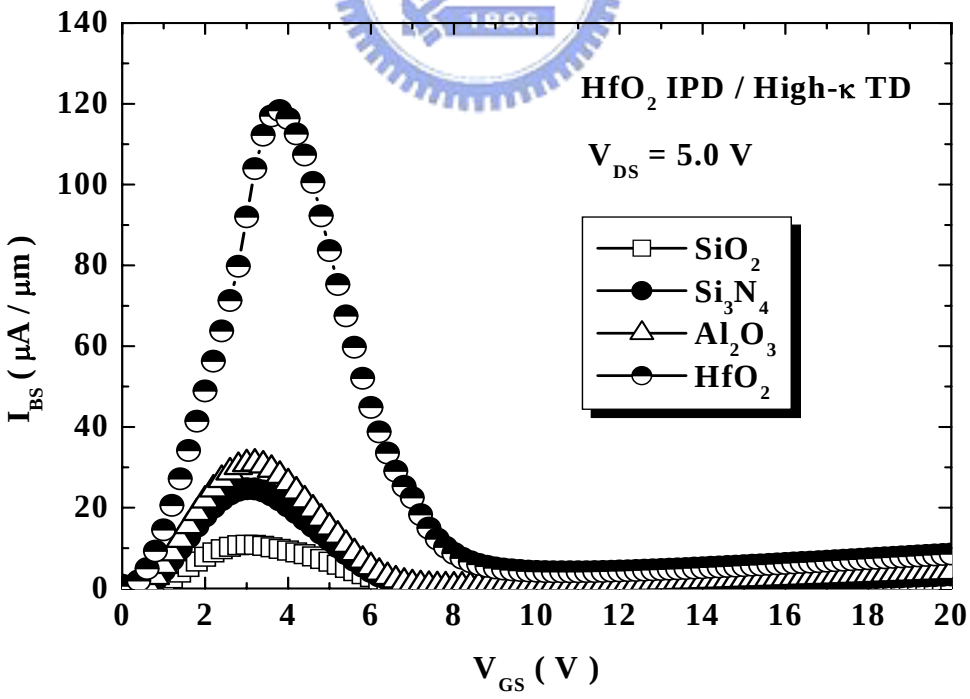
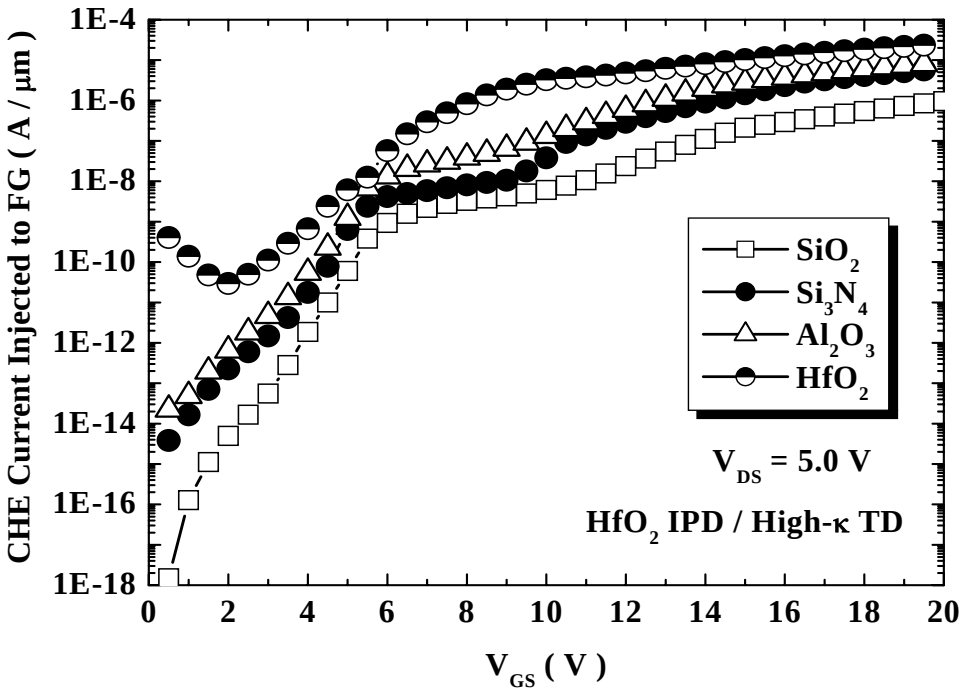
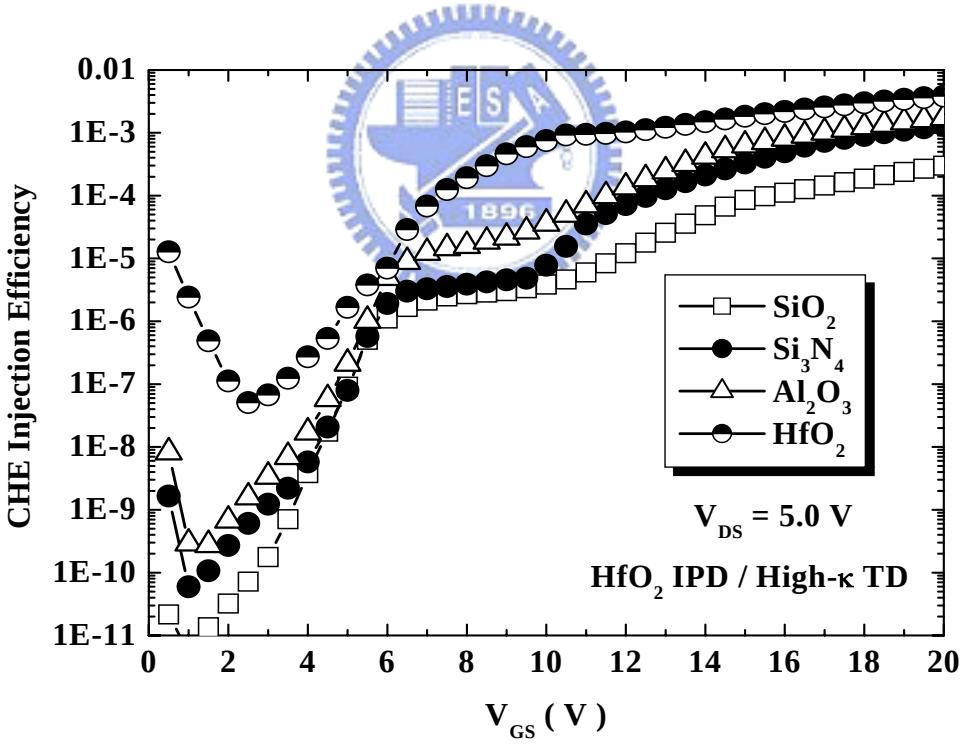


Fig. 5.4 Substrate current of stacked-gate flash memories with HfO_2 IPD and high-κ TDs. Maximum substrate current is substantially dependent of the κ-values of TDs.



(a)



(b)

Fig. 5.5 (a) CHE current injected to FG (b) CHE injection efficiency as a function of control gate voltages of stacked-gate flash memories with HfO_2 IPD and high-κ TDs at V_{DS} = 5.0V. Flash memories with high-κ TDs dramatically enhance injection efficiency than SiO_2 TOX.

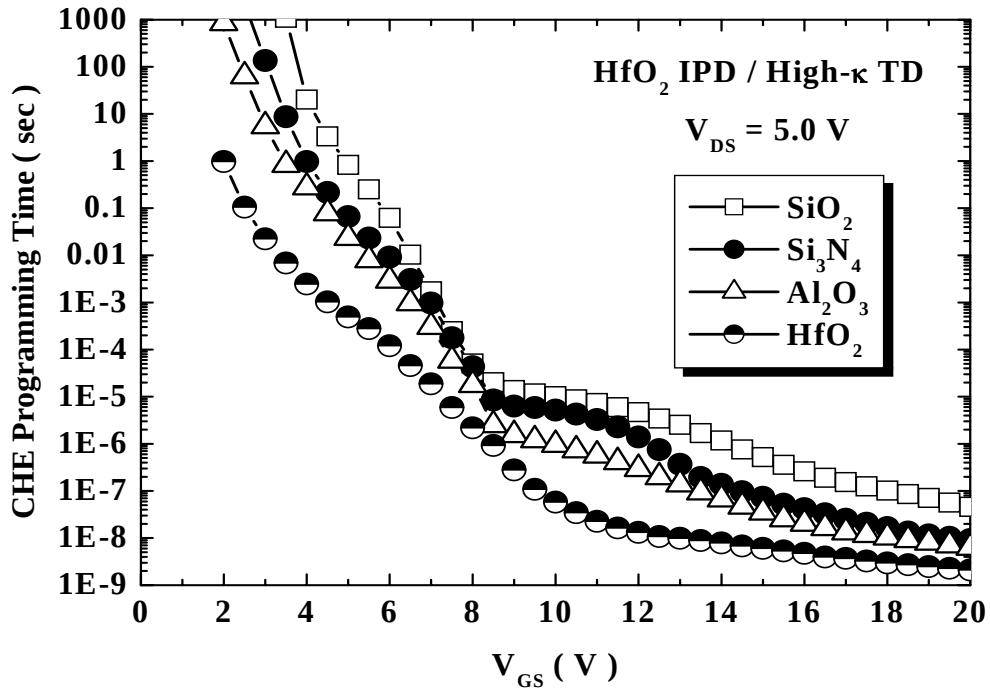


Fig. 5.6 CHE programming time as a function of control gate voltages of stacked-gate flash memories with HfO_2 IPD and high-κ TDs at V_{DS} = 5.0V.

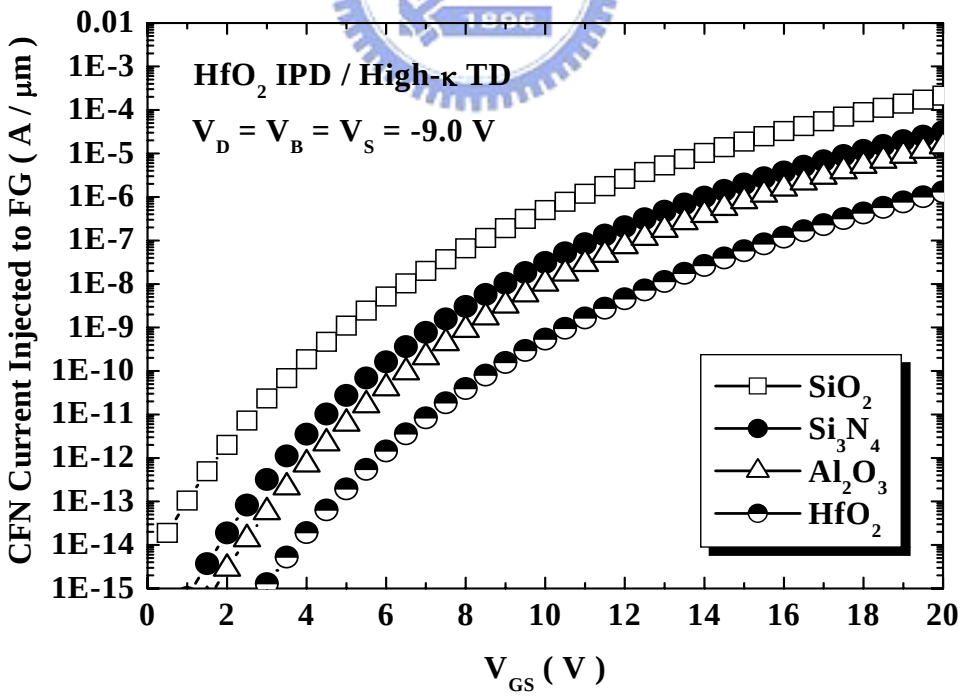


Fig. 5.7 CFN current injected to FG as a function of control gate voltages of stacked-gate flash memories with HfO_2 IPD and high-κ TDs at V_{DS} = 5.0V.

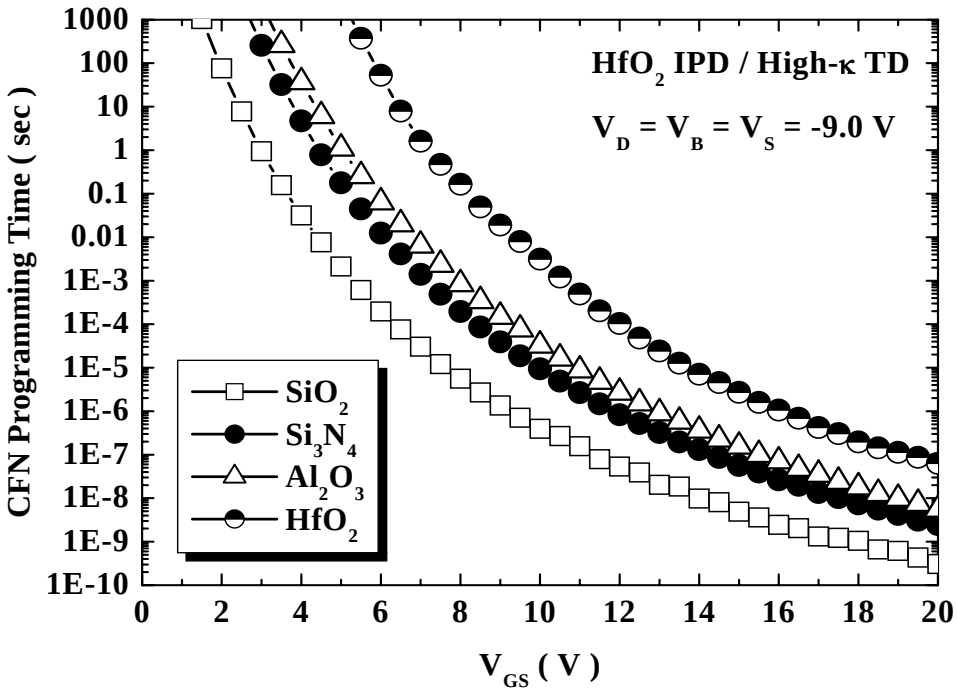
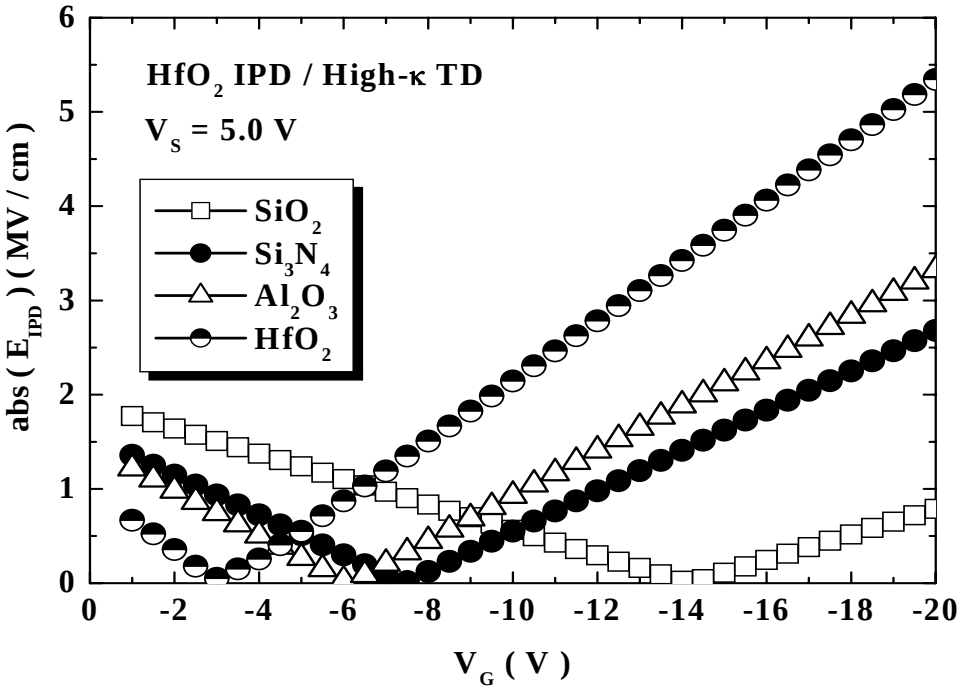


Fig. 5.8 CFN programming time as a function of control gate voltages of stacked-gate flash memories with HfO_2 IPD and high-κ TDs at $V_D = V_B = V_S = -9.0V$. Obvious degradation in CFN programming speed for high-κ TDs is indicated.



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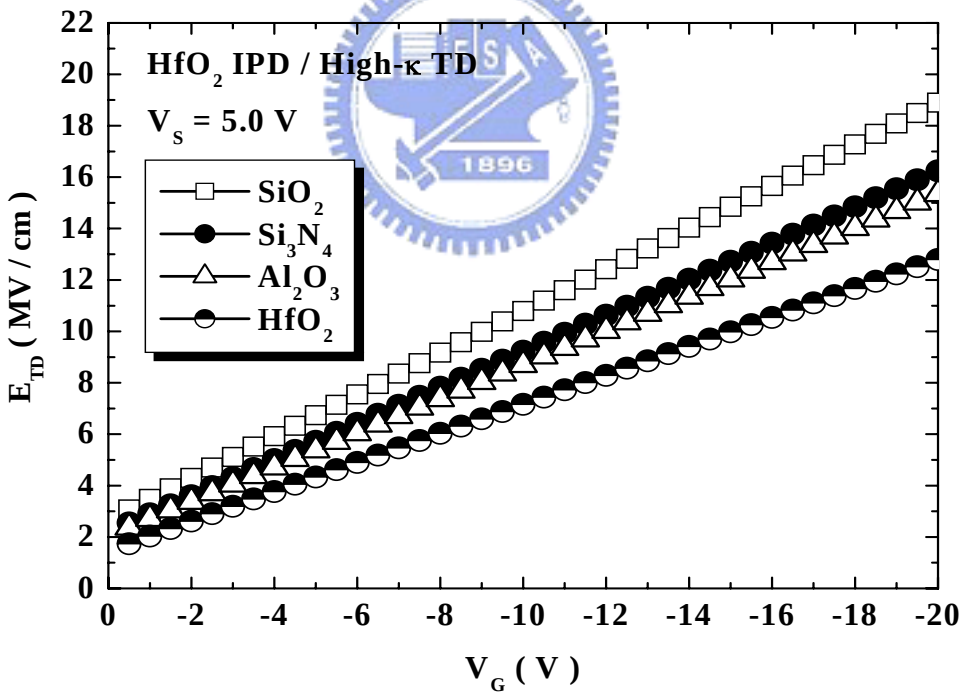


(b)

Fig. 5.9 (a) Absolute IPD (b) TD electric field as a function of control gate voltages of programmed state stacked-gate flash memories with HfO_2 IPD and high-κ TDs under V_S = 5.0V. Drain and substrate terminals are floating. High-κ TDs would increase IPD electric field as well as reduce TD electric field.

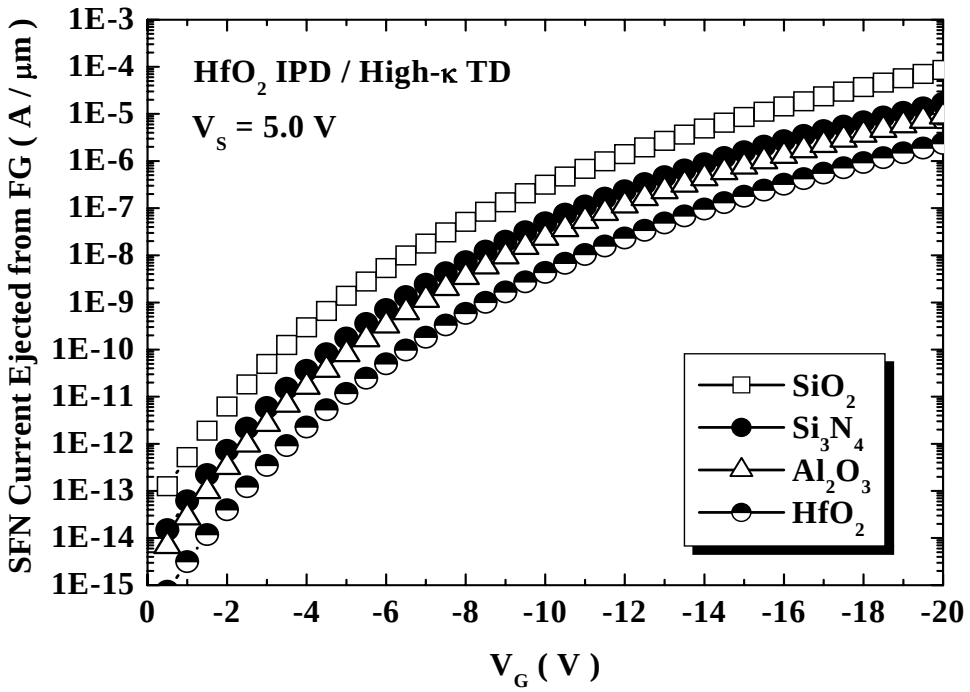


Fig. 5.10 SFN current ejected from FG of stacked-gate flash memories with HfO_2 IPD and high-κ TDs under V_S = 5.0V, floated drain and substrate terminal.

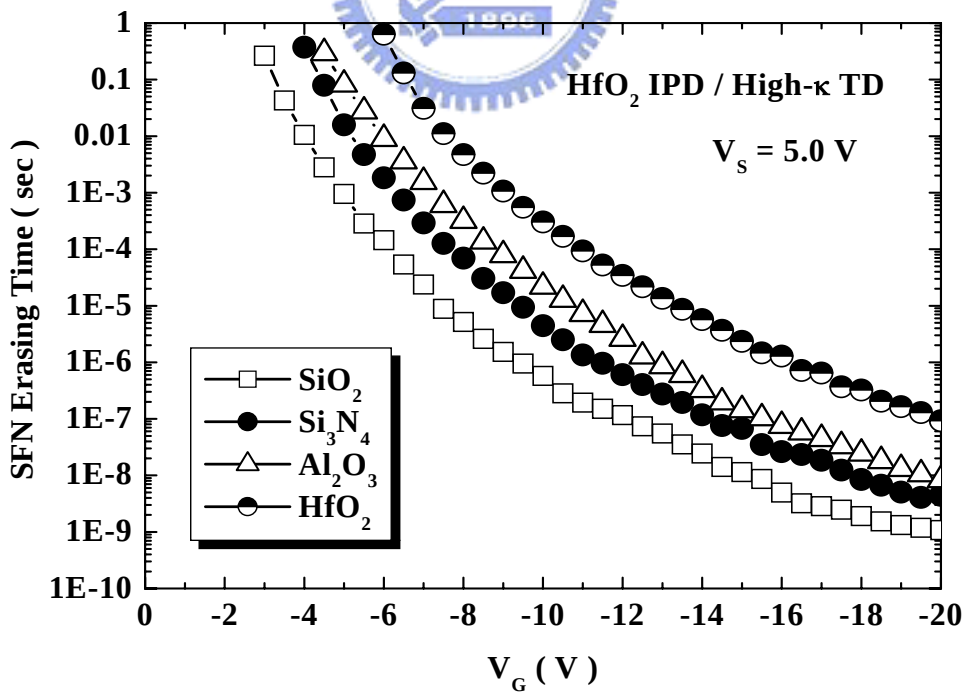


Fig. 5.11 SFN erasing time of stacked-gate flash memories with HfO_2 IPD and high-κ TDs. High-κ TDs crucially deteriorate SFN erasing speed.

CHAPTER 6

Study of Surface NH_3 Nitridation on the Trapping Characteristics and Dielectric Reliabilities of Al_2O_3 IPD

6.1 Introduction

Fast low-power nonvolatile memories are required for future wireless communication products. In the recent flash memory technologies, short program/erase times and operating voltage reductions are the most important issues to realize high speed/low power operation [28], [89]-[91]. For EEPROM and flash memory devices, the inter-poly dielectric (IPD) requires a high charge-to-breakdown (Q_{BD}), high breakdown field and low leakage current to obtain good data retention characteristics [92]-[94]. It is not sufficient to meet the stringent data retention requirement of IPD while applying thermal or CVD oxynitride technologies due to the unavoidable leakage current [29]-[32], [95]. In order to accomplish this without a trade-off between low power and high speed operations, high coupling ratio should be achieved by increasing the floating gate capacitance [89], [90], [96]-[103].

There are three different approaches can be used to increase coupling ratio. First, decrease the IPD thickness. Oxide/nitride/oxide (ONO) multi-layered films had been extensively investigated and frequently used as the dielectric layer in the flash memory devices and other applications [104]-[106]. However, decreasing the

thickness of the IPD to increase the coupling ratio may cause serious leakage and reliability problems which are fatal in the retention time of flash memories. Secondly, increase the area of the IPD capacitor. High capacitive-coupling ratio cell [96]-[98], 3-dimension interpoly dielectric [100], and hemisphere grain [101], [102] had been proposed to effective increase the capacitance area and lower the control gate bias. Although the coupling ratio of above mentioned cell structures could be dramatically improved, they must be fabricated with many additional process steps for fabrication such complex structures and be difficult to control well. The final approach is to increase the dielectric constant (κ) of IPD materials [22], [23], [27], [107]-[114]. Therefore, it is straightforward and effective to incorporate alternative high dielectric constant (high-κ) materials on nonvolatile memories to replace oxide/nitride/oxide IPD for increasing floating gate capacitance without increasing cell area and complexity of fabrication while suppressing charge loss.

In Chapter 4, we have demonstrated that the control gate voltage can be reduced greater than 30% with high-κ IPDs through MEDICI simulation. Among those potential candidates, aluminum oxide (Al_2O_3) is the most attractive for IPD applications in nonvolatile flash memories because of its higher conduction band offset with respect to the underlying poly-Si electrode and its higher permittivity with respect to Si_3N_4 [17], [21], [84], [85], [112], [115]. Previously, Lee *et al.* had been shown the benefits of using an Al_2O_3 IPD for low voltage/high speed flash memories in simulations [21]. In this chapter, the effect of surface NH_3 nitridation on the electrical properties and reliability characteristics of dc reactive-sputtered (RS) Al_2O_3 inter-poly capacitors are studied. It is found that the incorporation of nitrogen on the bottom poly-Si surface can not only reduce leakage current by one order of magnitude, but also enhance the breakdown field and the Q_{BD} as well. This is ascribed to the

resultant smoother interface between the dielectric and the floating gate by surface nitridation and less electron traps in the bulk. Auger electron spectroscopy (AES) depth profile also shows that the surface nitridation can effectively eliminate inter-diffusion between Al_2O_3 IPD and underneath poly-Si.

6.2 Experimental Details

The n^+-polysilicon/Al_2O_3/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 950^{o}C to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620^{o}C and subsequently implanted with phosphorous at 5×15cm^{-2}, 20keV, then activated with RTA at 950°C for 30s. Prior to the growth of Al_2O_3 IPDs, the native oxide covered Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, several samples were subjected to ammonia (NH_3) nitridation in the LPCVD furnace at 800°C for 1hour. Then, 10nm Al_2O_3 IPD was deposited by reactive sputtering (RS) in an Ar/O_2 ambient. Annealing of Al_2O_3 IPDs was carried out by rapid thermal annealing at 800^{o}C in an O_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD and implanted with phosphorous at 5×15cm^{-2}, 20keV. Dopants were then activated with RTA at 950°C for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional

view and key process steps of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition oxygen annealing are shown in Fig. 6.1 and 6.2, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (100kHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284. Moreover, the physical thickness was estimated by high resolution transmission electron microscopy (HRTEM). The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer. The atomic concentrations and depth profiles of the Al_2O_3 IPD were extracted by AES. The blanket wafers with Al_2O_3 dielectric deposition on top of the Poly-I annealed at various PDA temperatures were also prepared for surface roughness measurement by atomic force microscopy (AFM).

6.3 Results and Discussions

In this chapter, the effects of surface NH_3 nitridation on the dc reactive-sputtered Al_2O_3 IPD are investigated in terms of leakage current, surface roughness and dielectric reliabilities.

6.3.1 Investigation of Surface NH_3 Nitridation Effects on the RS Al_2O_3 IPD

The current density-effective electric field (breakdown voltage/EOT) (*J-E*) characteristics of the 800°C-annealed Al_2O_3 inter-poly capacitors with and without NH_3 nitridation on the Poly-I surface at 800°C for 1hr are seen in Fig. 6.3(a). The *J-E* curves reveal a rapid rise in leakage current at electric field beyond 5 MV/cm due to

Fowler-Nordheim (FN) tunneling through the Al_2O_3 IPD. It is found that the sample with NH_3 nitridation results in an almost one order of magnitude reduction in positive-biased leakage current density, compared to the sample without NH_3 nitridation. Similarly, a leakage current with 10 times reduction is also observed in negative polarity. Figure 6.3(b) indicates *C-V* curves of 800°C-annealed Al_2O_3 inter-poly capacitors with and without surface NH_3 nitridation. Comparing to conventional MOS-capacitors, inter-poly capacitors have large minimum capacitance due to heavy doping in Poly-I. The EOT of sample with and without nitridation is 4.6nm and 5.6nm, respectively. Surface nitridation can effectively suppress the interfacial layer (IL) growth, and results in 1nm EOT thinning, which can be evidenced by HRTEM images shown in Fig. 6.4.

It is important to monitor both the leakage current uniformity and breakdown field of IPD to inspect the charge loss conditions through low and high electric field for flash memories biased at read and program/erase scheme, respectively. According to the simulated electric field shown in Fig. 4.2, leakage current density at 3 MV/cm and 8 MV/cm is chosen to be the indicators of charge loss through Al_2O_3 IPD at read and program scheme, respectively. Figure 6.5 compares the Weibull distributions of the leakage current density of Al_2O_3 inter-poly capacitors after 800°C PDA with and without NH_3 nitridation in both polarities. Strong polarity dependence between positive and negative bias is evident in Al_2O_3 IPD with and without nitridation, leakage current at positive bias is higher than negative bias, which can be partially explained by asymmetric band diagrams for electron injection. Although the leakage current reduction at low electric field is inconspicuous, surface nitridation can effectively suppress high electric field leakage current, especially for positive gate voltage. The results apparently demonstrate Al_2O_3 IPD with surface nitridation can

effectively reduce charge loss from floating gate to control gate as well as carrier injection from control gate to floating gate, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD.

Figure 6.6 examines the Weibull distributions of the effective breakdown field in the Al_2O_3 inter-poly capacitors after 800^{o}C PDA with and without surface NH_3 nitridation for both polarities. A breakdown field improvement of more than 2 MV/cm is clearly observed on the nitridated samples for both positive and negative polarities. Higher breakdown is helpful to reduce charge transportation path between control gate and floating gate. Dielectric relaxation current (transient gate current) for the 800^{o}C-annealed Al_2O_3 IPDs with and without NH_3 nitridation was measured instantly after a 2V voltage step, which is shown in Fig. 6. 7. J(t) follows a t^{-n} dependence with n close to 1 for 10 decades of times, which can be explained by Curie-von Schweidler law and double potential well model [116]-[118]. Due to the asymmetry of the energy band structure, electron transport is easier in positive polarity than negative polarity. As a result, positive polarity shows larger relaxation current. Moreover, samples with NH3 nitridation apparently reduce relaxation current, which can be ascribed to the reduced bulk defects. Al_2O_3 IPD with surface nitridation clearly suppresses the relaxation current due to smaller trapping density and trapping rate, as shown in below.

Figure 6.8(a) depicts the charge trapping curves of the 800^{o}C-PDA Al_2O_3 inter-poly capacitors with and without nitridation under a constant current stress (CCS) of 5 mA/cm^2 and 1 mA/cm^2, respectively, in both polarities. The increase in the absolute gate voltage is obviously coming from electron trapping. It is noted that the Al_2O_3 inter-poly capacitors with surface nitridation, albeit subjected to a larger stressing current, show a much smaller electron-trapping rate than those without

nitridation. Figure 6.8(b) demonstrates the corresponding Weibull distributions of Q_{BD} for two splits. Clearly, the Al_2O_3 inter-poly capacitor with NH_3 nitridation has a nearly one order of magnitude improvement. This trend is fully consistent with the results in Fig. 6.8(a), i.e., higher trapping rate will lead to lower Q_{BD}. The relatively reduced electron trapping rate is also consistent to the suppressed dielectric relaxation current for the IPD with NH_3 nitridation.

6.3.2 Conduction Mechanism of the RS Al_2O_3 IPD

Figure 6.9(a) shows the *J-E* characteristics of 800°C-annealed Al_2O_3 inter-poly capacitors with and without NH_3 nitridation measured at four different temperatures, 25°C, 75°C, 100°C and 125°C. The effect on the leakage current as the temperature rises from room temperature to 125°C is minor, which confirms that the FN tunneling dominates the conduction mechanism, rather than Frenkel-Poole tunneling. Moreover, despite measuring temperatures, positive-biased leakage current is always higher than negative-biased current. Effective barrier heights (φ_B) of the 800°C-annealed Al_2O_3 IPD with and without NH_3 nitridation in both polarities are extracted in Fig. 6.9(b). In positive polarity, the φ_B of the Al_2O_3 IPD with and without NH_3 nitridation are 1.54eV and 1.25eV, respectively, from fitting the voltage dependence of the FN tunneling current by assuming effective electron mass in Al_2O_3 of being $0.2m_0$ [119]. Higher φ_B can reduce electron tunneling probability and lead to lower leakage current density. However, the barrier heights in negative polarity are 1.62eV with nitridation and 1.59eV without. The nearly identical φ_B value cannot account for the reduction of the lower leakage current of nitridated IPD in negative polarity, as compared with non-nitridated IPD. We ascribe this result to the small concentration of oxygen vacancies existed in the Al_2O_3 IPD after 800°C PDA in oxygen ambient, which will be

further discussed later.

6.3.3 Polarity Dependence of the RS Al_2O_3 IPD

Although Poly-I and Poly-II have similar fabrication process, our results clearly indicate asymmetric polarity characteristics. The enhanced breakdown field and reduced leakage current of nitrided samples in positive polarity may be attributed to the reduced interfacial reaction between the IPD and Poly-I films and smoother surface roughness of the Poly-I films. This speculation is supported by the results of the AFM images, shown in Fig. 6.10. Before IPD deposition, the RMS roughness of the Poly-I surface is 2.57nm and 2.64nm, respectively, with and without nitridation. After a 150^{o}C hot phosphoric acid (H_3PO_4) etching step with the Al_2O_3/Poly-Si selectivity larger than 60, the RMS roughness of the bottom interface with and without surface nitridation are 2.76nm and 3.32nm, respectively. Significantly rough surface is observed for the sample without NH_3 nitridation. A smoother interface is helpful in reducing the localized field and, hence, results in lower leakage current and higher breakdown field [120], [121].

The origin of the resulting smoother interface is hypothesized to be closely related to the capability of Si-N layer in blocking oxygen diffusion during post-deposition O_2 annealing. From the high-frequency *C-V* measurements, the EOTs of the Al_2O_3 IPD layers after 800^{o}C PDA with and without NH_3 nitridation are 4.6nm and 5.6nm, respectively, as seen in Fig. 6.3(b). In addition, from the AES analyses of the Al_2O_3 inter-poly capacitors after 800^{o}C annealing, shown in Fig. 6.11, the profiles of Si and oxygen at Al_2O_3/Poly-I interface indicate that the NH_3 nitridation can block the inter-diffusion of Si and O. Without surface passivation, Al and O atoms are more

likely to react with Si and may form additional silicon dioxide and/or aluminum silicate with relatively lower κ value [122]. High resolution TEM images of Al_2O_3 inter-poly capacitors after 800^oC annealing with and without surface NH3 nitridation are inspected in Fig. 6.4. Further evidence from TEM images also reveals a thicker interface layer and rough interface for the non NH_3-nitrided sample. As a result, higher EOT value and a rougher surface are therefore obtained. As indicated in Fig. 6.3 and 6.5, the asymmetry in the gate current with respect to the injection polarity can only be partly explained by the difference in barrier heights between Poly-Si and Al_2O_3 IPD. The asymmetric leakage current dependence can be ascribed to asymmetric band diagram for carrier tunneling [123]. For negative polarity, the interfacial layer acts as a capacitive voltage divider and reduces the injection fields. For positive polarity, the interfacial layer appears to be transparent and can be neglected.

Second, the improvement of electrical properties in negative polarity cannot be fully attributed to the smooth surface roughness and large barrier height. Thus, we suspect that surface nitridation may effectively reduce the concentration of oxygen vacancies during post-deposition high temperature annealing due to its capability to block oxygen diffusion; in this case, oxygen molecules could have higher probability to compensate or exchange the unsaturated/strained bonds in the as-deposited Al_2O_3. In addition, strained Si-O bonds in the as-deposited film can be replaced with un-strained Si-O bonds due to oxygen exchange during post-deposition annealing [124]. Consequently, nitridation will cause more oxygen vacancies to be compensated during post-deposition oxygen annealing, resulting in a smaller tunneling current and higher Q_{BD} for negative polarity. Surface NH_3 nitridation therefore exhibits a highly potential to diminish charges transfer between control gate and floating gate of the

stacked-gate flash memories.

6.4 Summary

The effect of NH_3 nitridation of Poly-I on the electrical properties and reliability characteristics of the Al_2O_3 inter-poly capacitors are evaluated in this chapter. With surface NH_3 nitridation, the formation of an additional layer with lower dielectric constant during post-annealing process can be significantly suppressed and reduced the EOT to 4.6nm, compared to that without nitridation treatment. For positive gate bias, IPD with NH_3 surface nitridation can significantly suppress the formation of an additional layer with lower dielectric constant during post-annealing process and obtain smoother interface, compared to that without nitridation treatment. Furthermore, the presence of a thin Si-N layer can make PDA more effective in eliminating traps existing in the as-deposited films and improve dielectric characteristics under negative polarity. As a result, a smoother interface and smaller electron trapping rate can contribute to the drastically reduced leakage current, enhanced breakdown field and Q_{BD} of Al_2O_3 interpoly capacitors with surface NH_3 nitridation for both polarities. AES depth profile also showed that the surface nitridation can effectively eliminate inter-diffusion between Al_2O_3 IPD and underneath poly-Si. Surface NH_3 nitridation therefore is expected to exhibit a highly potential to diminish charges transfer between control gate and floating gate of the stacked-gate flash memories.

Table 6.1 EOT, Poly-I surface roughness and 63%-failure Q_{BD} values of the 800°C-annealed Al_2O_3 inter-poly capacitors with and without surface NH_3 nitridation.

NH_3 nitridation	**EOT (Å)**	**Poly-I surface roughness (nm)**	**63% Q_{BD} (mC/cm^2)**	
			positive	**negative**
with	**46**	**2.76**	**65.1**	**170.5**
without	**56**	**3.32**	**5.4**	**9.2**

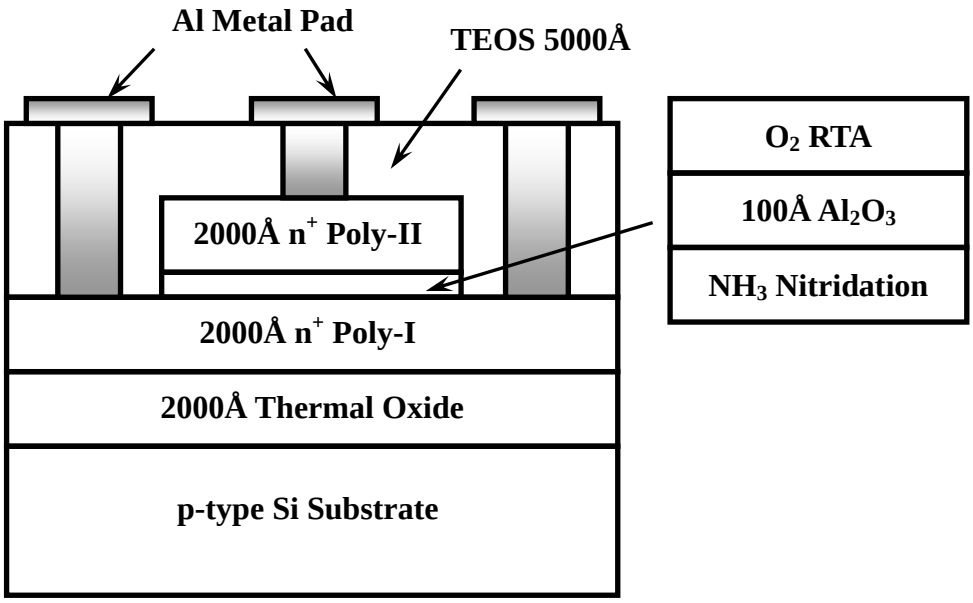


Fig. 6.1 Cross-sectional view of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition oxygen annealing.

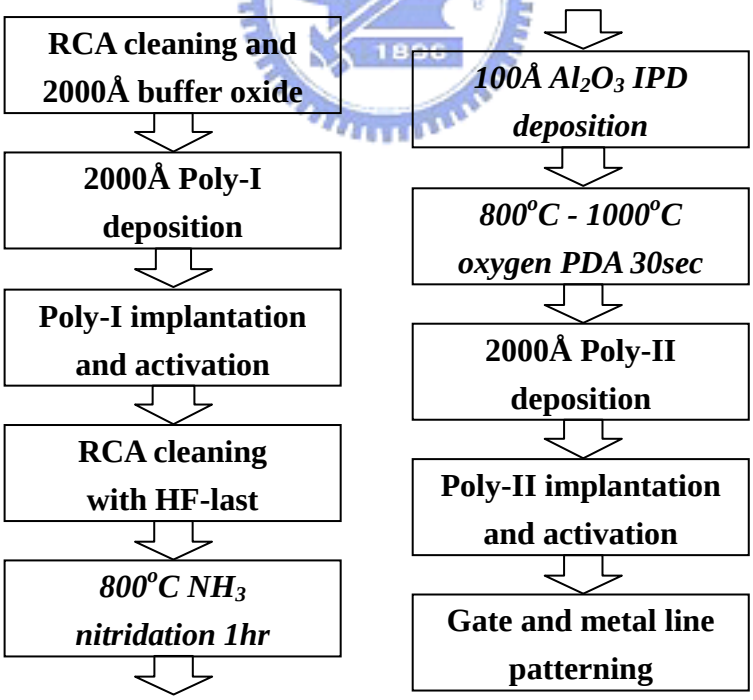
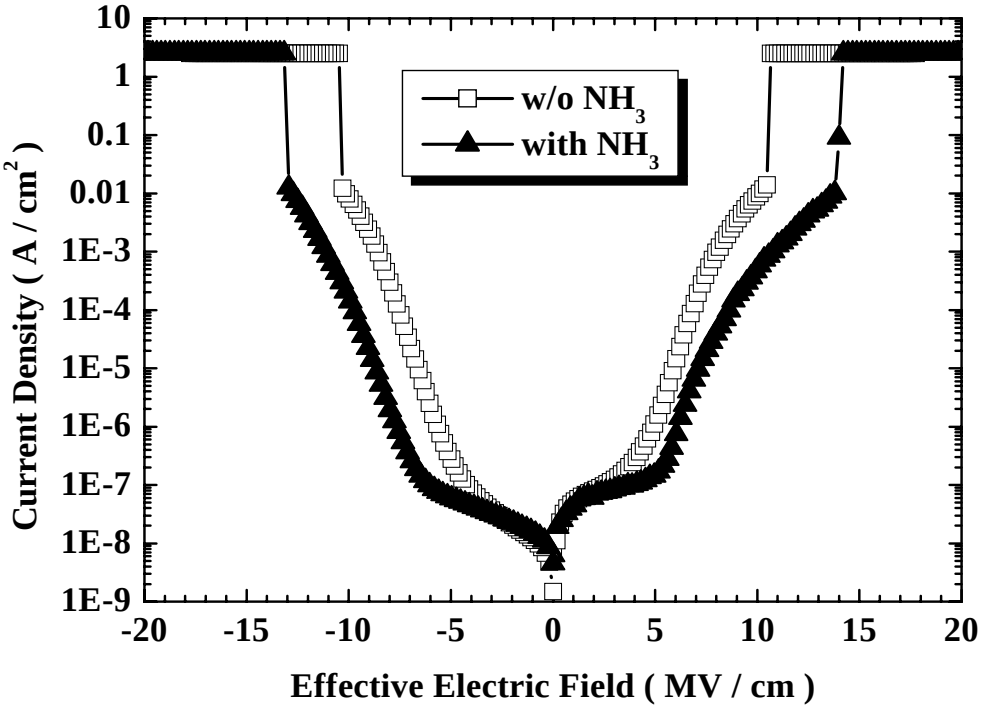
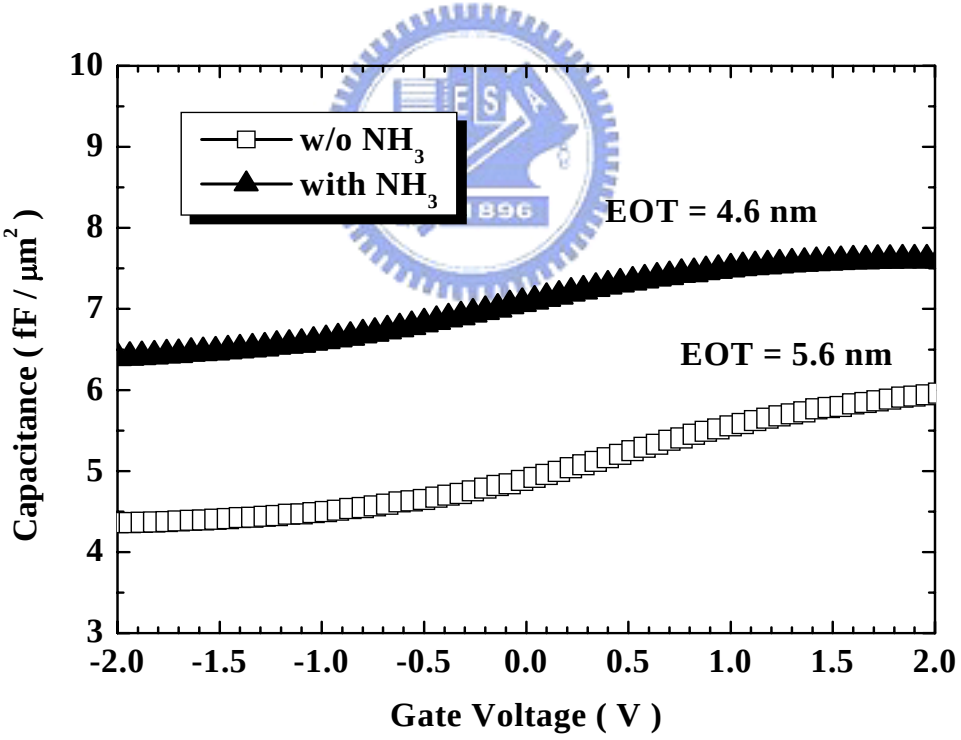


Fig. 6.2 Key process steps of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition oxygen annealing.

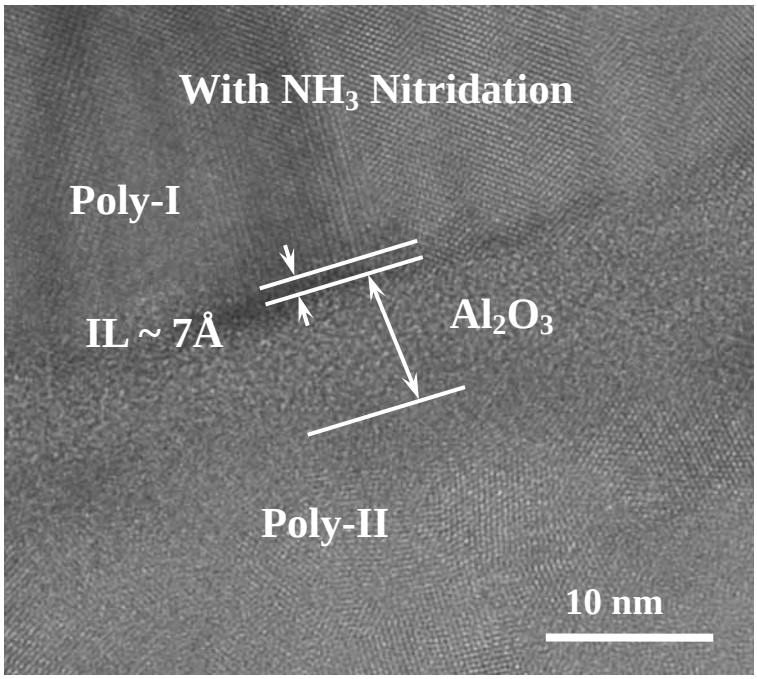


(a)

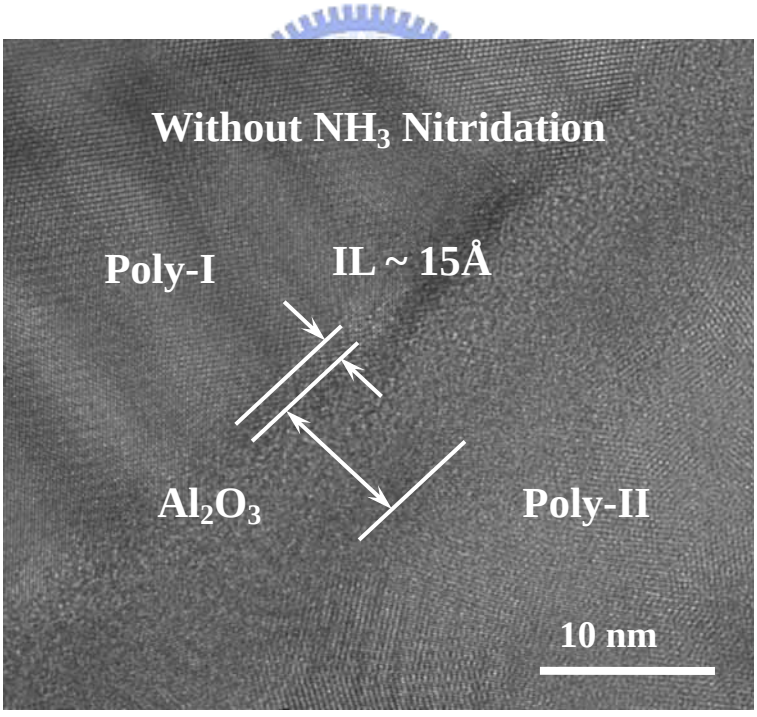


(b)

Fig. 6.3 (a) *J-E* characteristics (b) *C-V* curves of 800°C-annealed Al_2O_3 inter-poly capacitors with and without surface NH_3 nitridation under both polarities. Surface nitridation is beneficial in thinning EOT and lowering leakage current density compared to samples without nitridation.

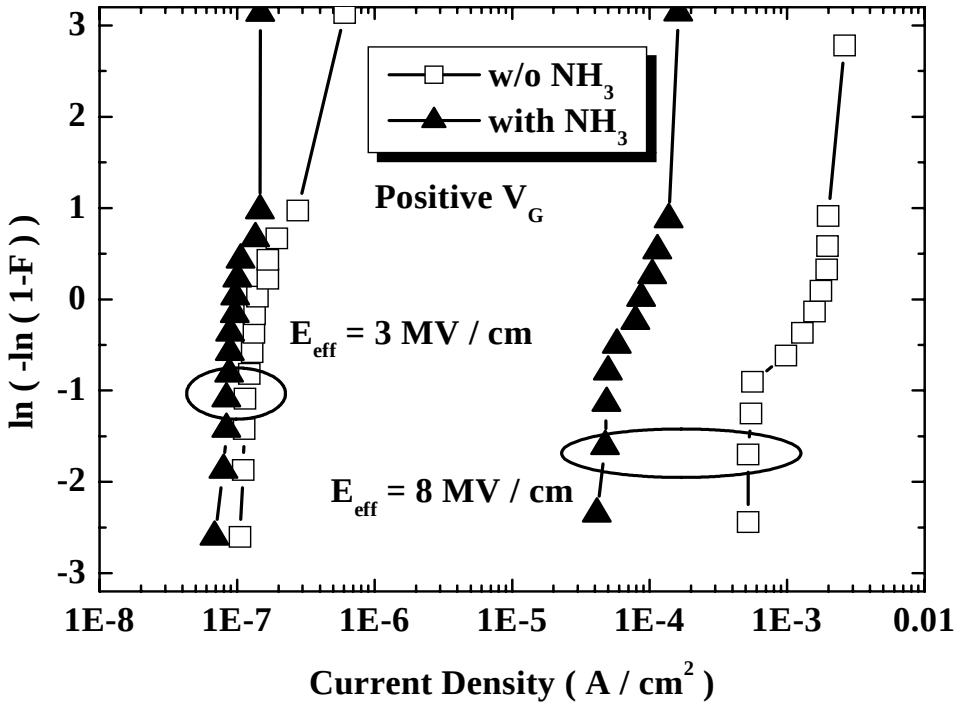


(a)

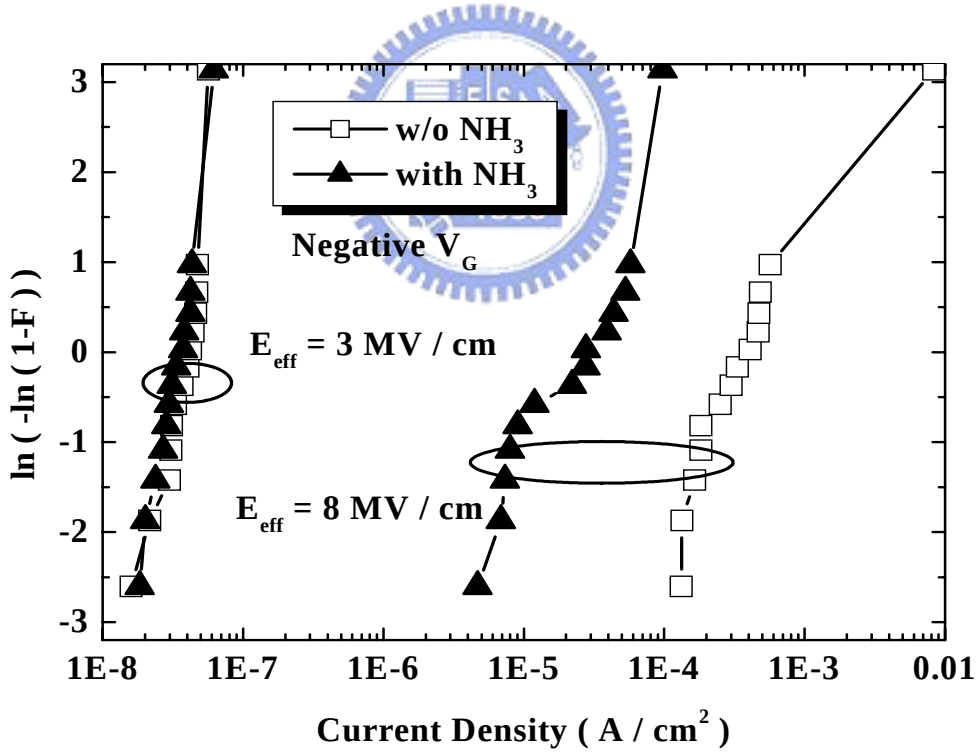


(b)

Fig. 6.4 High resolution TEM images of Al_2O_3 inter-poly capacitors after 800°C annealing (a) with (b) without surface NH_3 nitridation. Physical thickness of Al_2O_3 IPD is estimated to be 8.5 nm. Samples with NH_3 nitridation can effectively reduce interfacial layer growth and smooth interface roughness.



(a)



(b)

Fig. 6.5 Leakage current density Weibull distributions at 3 MV/cm and 8 MV/cm of 800°C-annealed Al_2O_3 inter-poly capacitors with and without NH_3 nitridation under (a) positive V_G (b) negative V_G. Surface NH_3 nitridation can effectively reduce low and high field leakage current under both polarities.

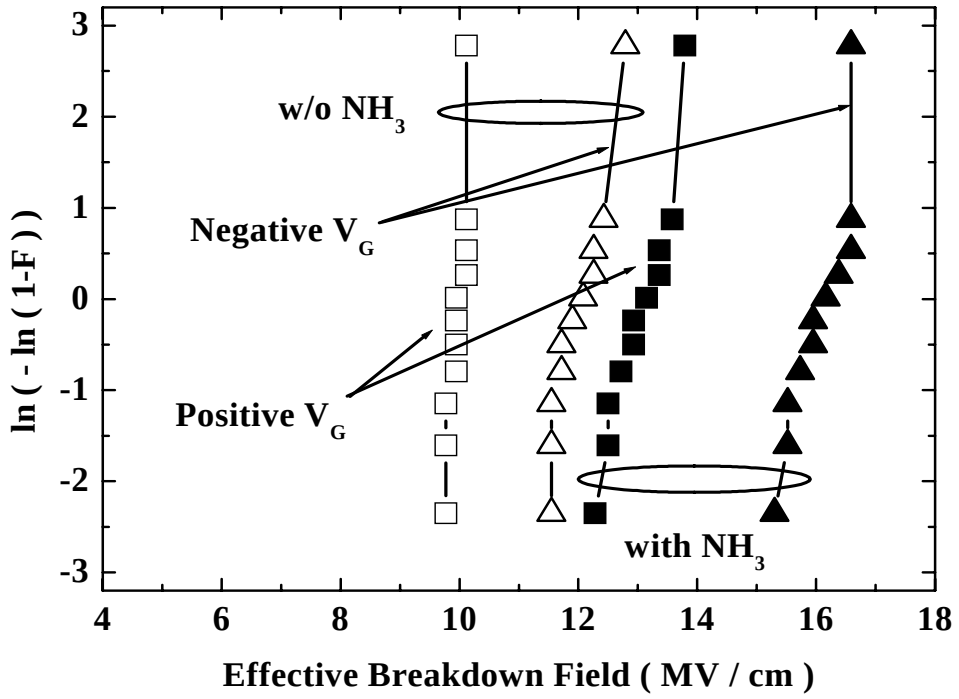


Fig. 6.6 Effective breakdown field Weibull distributions of 800°C-annealed Al_2O_3 inter-poly capacitors with and without NH_3 nitridation in both polarities.

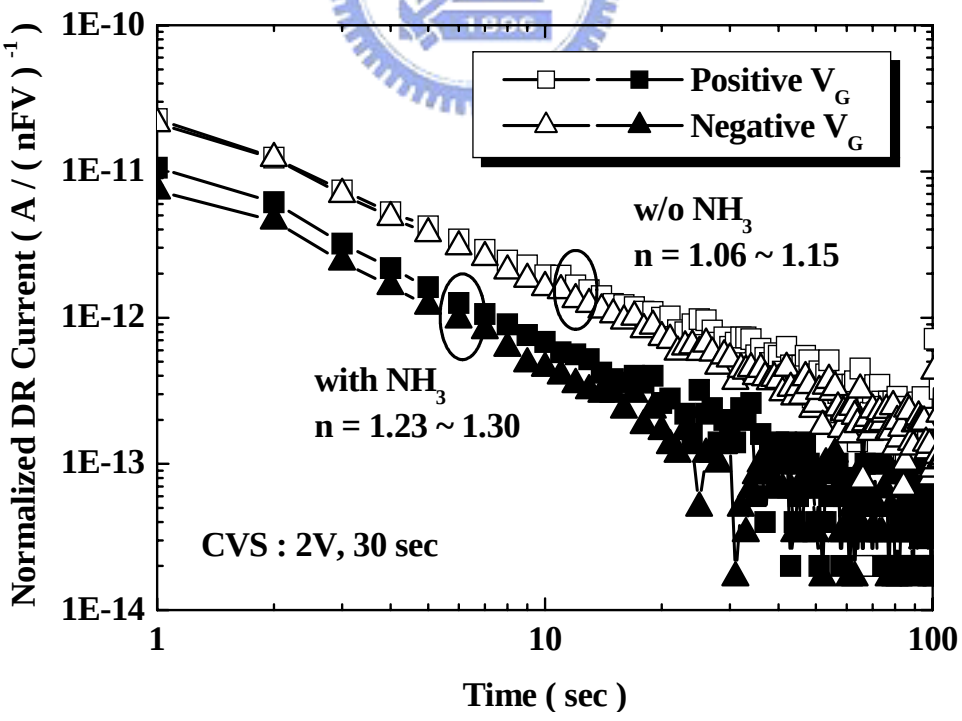
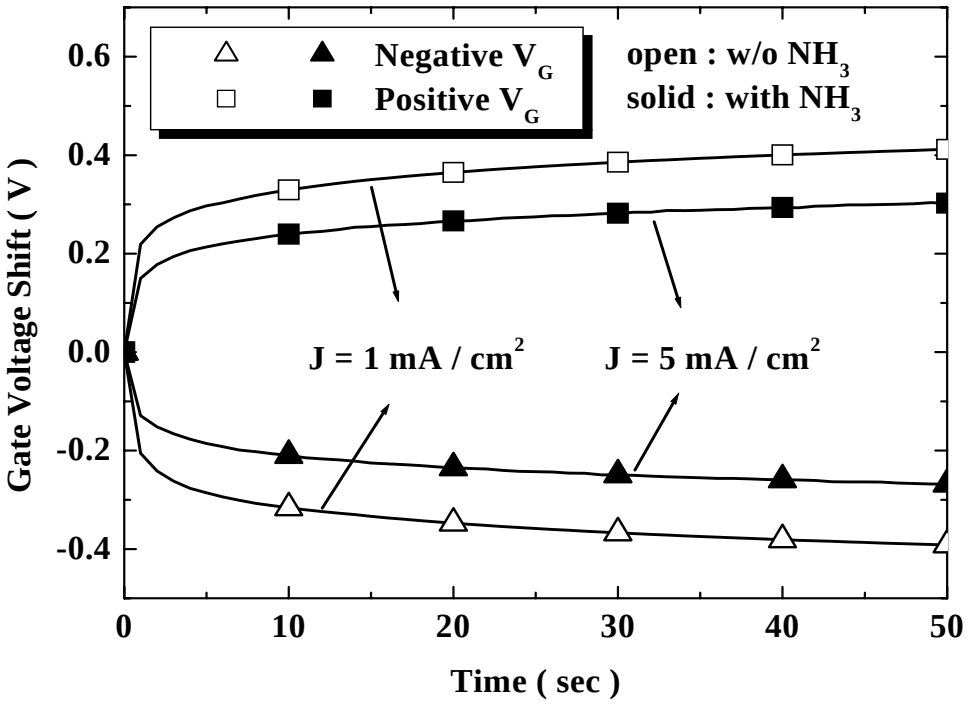
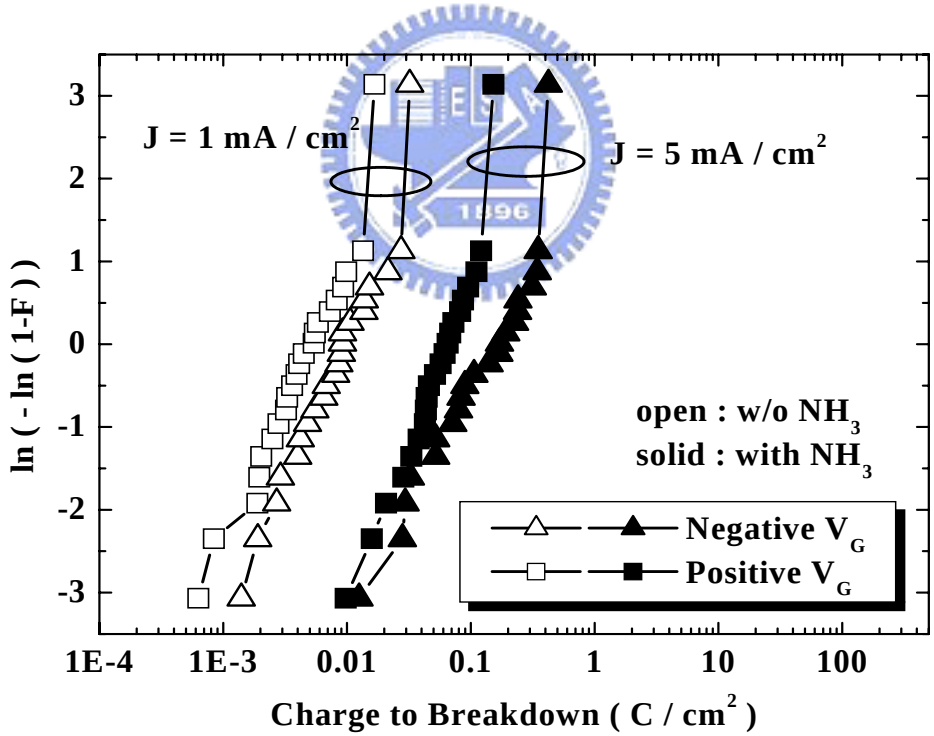


Fig. 6.7 Dielectric relaxation current of 800°C-annealed Al_2O_3 inter-poly capacitors with and without NH_3 nitridation in both polarities.

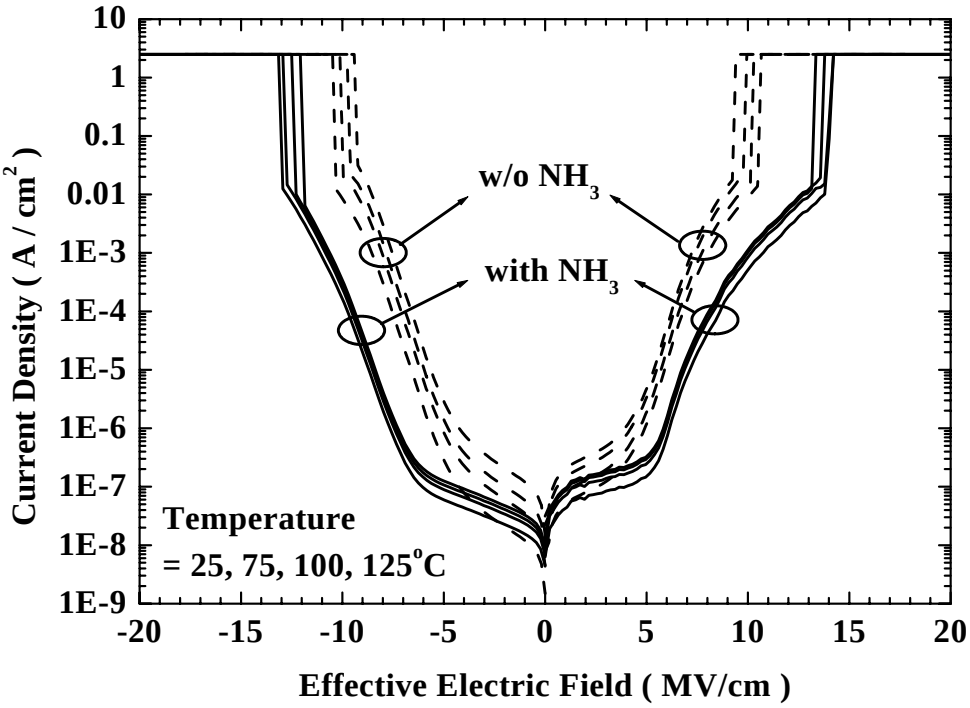


(a)

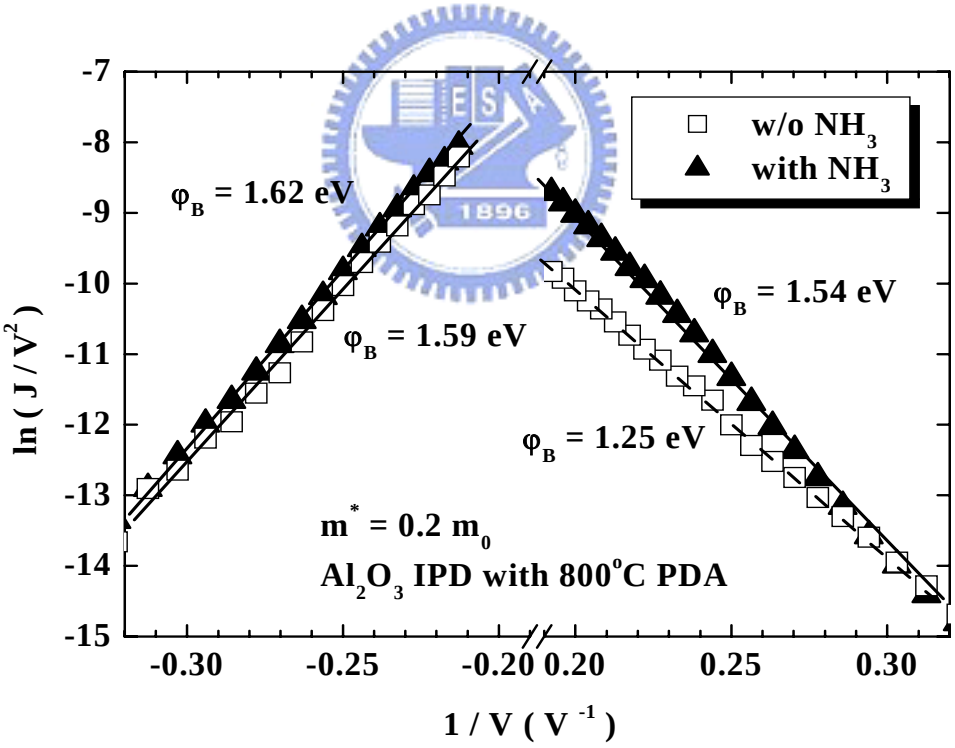


(b)

Fig. 6.8 (a) Curves of gate voltage shift (b) Q_{BD} Weibull plots of Al_2O_3 inter-poly capacitors after 800°C annealing with and without surface NH_3 nitridation under constant current stress. Samples with NH_3 nitridation can suppress electron-trapping generation and increase Q_{BD}.



(a)



(b)

Fig. 6.9 (a) Measuring temperature dependence of leakage current density (b) Fowler-Nordheim tunneling fitting of Al_2O_3 inter-poly capacitors after 800°C annealing with and without surface NH_3 nitridation.

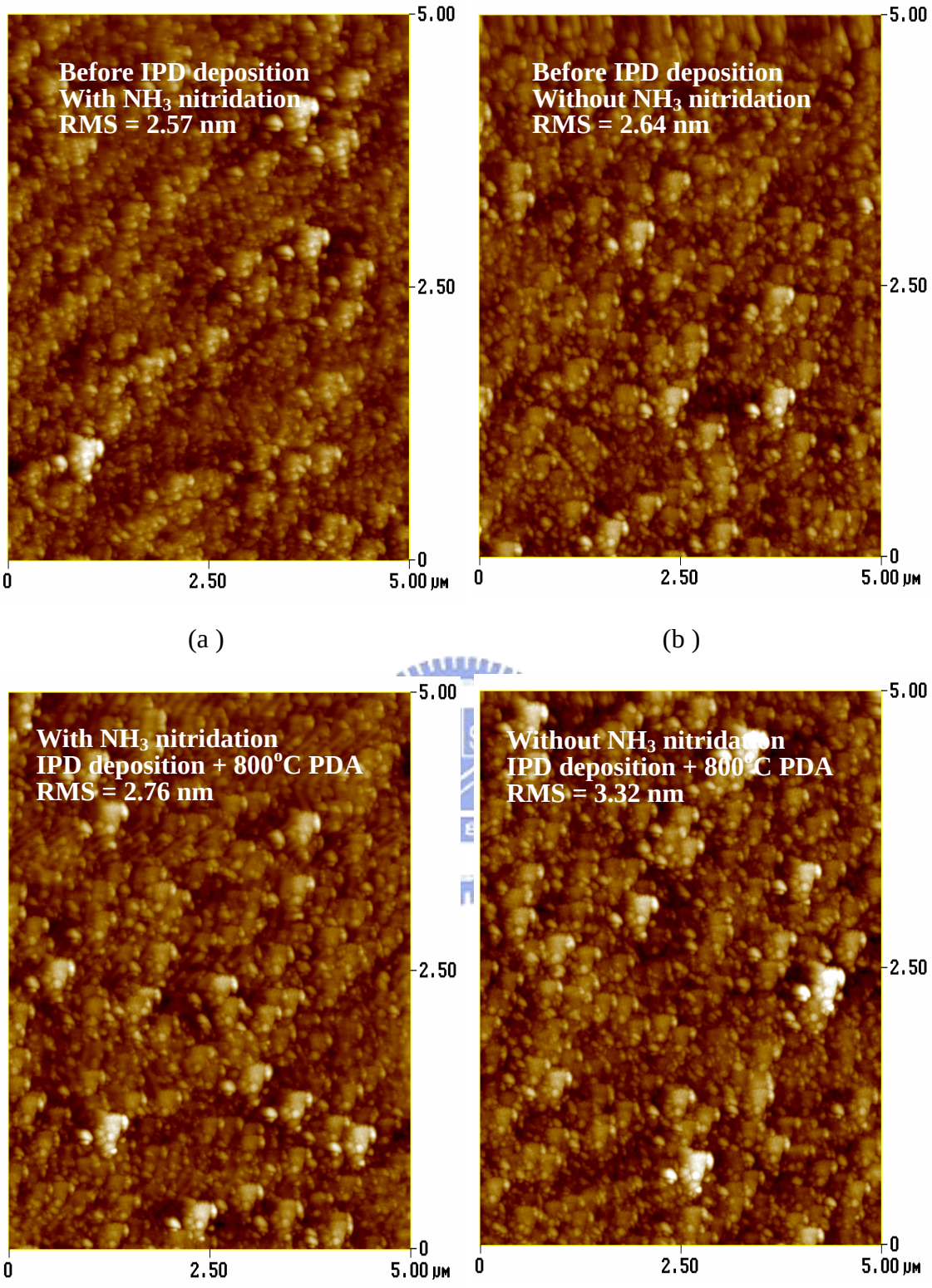


Fig. 6.10 AFM images (5μm×5μm) of the poly-I surface before Al_2O_3 IPD deposition (a) with (b) without surface NH_3 nitridation, and after 800°C O_2 annealing (c) with (d) without surface NH_3 nitridation. Surface nitridation can eliminate surface roughness apparently.

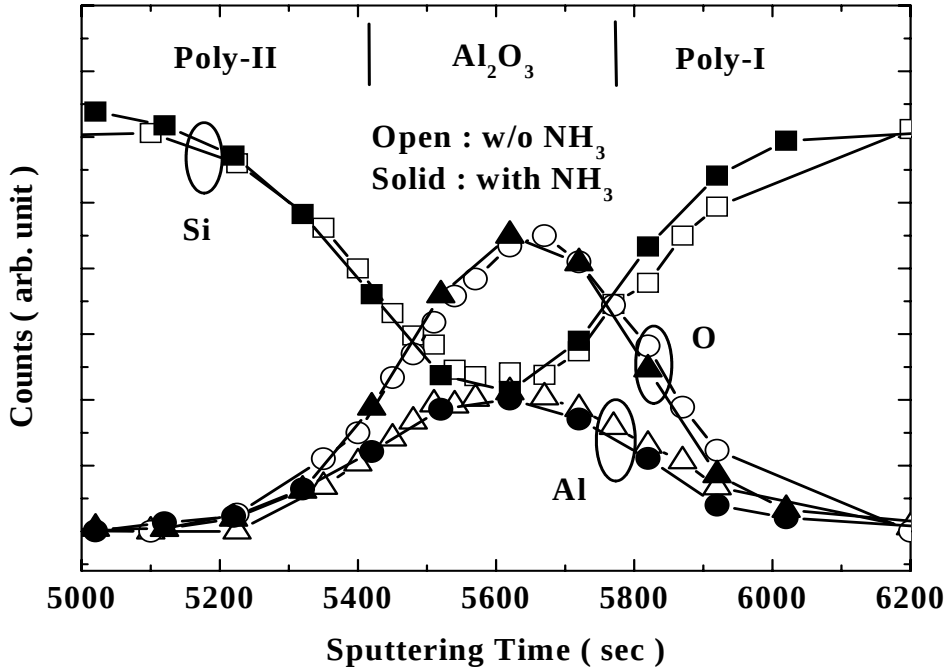


Fig. 6.11 AES depth profiles of Al_2O_3 inter-poly capacitors after 800^{o}C annealing with and without surface NH_3 nitridation. Surface nitridation clearly suppresses interfacial Al, O and Si inter-diffusion.

CHAPTER 7

Effects of PDA Temperature on the Electrical Properties of Al_2O_3 IPD with NH_3 Nitridation

7.1 Introduction

With the scaling down of thickness of the inter-poly dielectrics (IPD), the quality of dielectric becomes very critical for the application of the EEPROM and flash nonvolatile memories. Lower leakage of the dielectric means longer data retention time. In previous chapter, Al_2O_3 IPD with surface NH_3 nitridation has been shown improved electrical properties. It is found that the incorporation of nitrogen on the bottom poly-Si surface can not only reduce leakage current by one order of magnitude, but also enhance the breakdown field and the charge-to-breakdown (Q_{BD}) as well. This is ascribed to the resultant smoother interface between the dielectric and the floating gate by surface nitridation and less electron traps in the bulk. However, the Q_{BD} is quite low. Moreover, the effect of post-deposition annealing (PDA) temperature on the electrical properties and reliability characteristics of dc reactive-sputtered Al_2O_3 inter-poly capacitors with surface NH_3 nitridation are studied in this chapter. The electrical properties of the Al_2O_3 IPD are strongly influenced by the PDA temperature. The optimum is 900°C in terms of leakage current, electron trapping rate and Q_{BD}. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) depth profile showed that the excess oxygen plays an important

role in determining the resultant IPD electrical properties.

7.2 Experimental Details

The n^+-polysilicon/Al_2O_3/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 950^{o}C to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620^{o}C and subsequently implanted with phosphorous at 5×15cm^{-2}, 20keV, then activated with RTA at 950°C for 30s. Prior to the growth of Al_2O_3 IPDs, the native oxide covered Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, all samples were subjected to ammonia (NH_3) nitridation in the LPCVD furnace at 800°C for 1hour. Then, 10nm Al_2O_3 IPD was deposited by reactive sputtering (RS) in an Ar/O_2 ambient. Annealing of Al_2O_3 IPDs was carried out by rapid thermal annealing at temperatures ranging from 800^{o}C to 1000^{o}C in an O_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD and implanted with phosphorous at 5×15cm^{-2}, 20keV. Dopants were then activated with RTA at 950°C for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional view and key process steps of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition oxygen annealing are the same as Fig. 6.1 and 6.2, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (100kHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284 LCR meter. Moreover, the physical thickness was estimated by high resolution transmission electron microscopy (HRTEM). The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer. The atomic concentrations and depth profiles of the Al_2O_3 IPD were extracted by XPS and AES respectively. The blanket wafers with Al_2O_3 dielectric deposition on top of the Poly-I annealed at various PDA temperatures were also prepared for surface roughness measurement by atomic force microscopy (AFM). Phase change after high temperature annealing was analyzed by X-ray diffractometer (XRD).

7.3 Results and Discussions

In this chapter, the effect of PDA temperature on the RS Al_2O_3 IPD with surface NH_3 nitridation are investigated in terms of leakage current, surface roughness and dielectric reliabilities.

7.3.1 The Effects of Post-Deposition Temperature Annealing on the RS Al_2O_3 IPD

Figure 7.1(a) indicates *C-V* curves of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800^{o}C to 1000^{o}C. The EOT is increased as raising annealing temperature, which can be ascribed to the thick interfacial layer (IL) growth. Figure 7.1(b) compares the *J-E* characteristics of the Al_2O_3 inter-poly capacitors with

NH_3 nitridation at various PDA temperatures under both polarities. It is found that the sample with 900°C annealing can effectively reduce the low-field leakage current than 800°C- and 1000°C-annealed samples, which is helpful to suppress charge loss from the floating gate.

Figure 7.2(a) presents the transient currents for the annealed Al_2O_3 IPDs under a low field of 2 MV/cm in order to suppress the creation of stress-induced traps. Filling of the pre-existing electron traps in the dielectric leads to the decrease of the current leakage magnitude over time for all samples [115], [125]. Moreover, the rate of leakage current reduction in either polarity is nearly identical, suggesting that the traps are distributed uniformly across the films. Therefore, we believe that the dependence of the IPD characteristic on annealing temperature is closely related to the bulk defects in the dielectric, i.e., point defects. Dielectric relaxation current (transient gate current) for the annealed Al_2O_3 IPDs was measured instantly after a gate voltage step, which is shown in Fig. 7.2(b). When gate voltage pulses are applied to inter-poly capacitors, the gate current amplitude reaches a high level instantly after the switch and then decays to a low constant level. The *J-t* curves are nearly a straight line in log-log scale with slope ~ -1 [126], [127]. Due to the asymmetry of the energy band structure, electron transport is easier in positive polarity than negative polarity. As a result, positive polarity shows larger relaxation current. Moreover, dielectric relaxation current is also depended on the PDA temperature. 900°C-annealing apparent reduce the relaxation current due to smaller trapping density and trapping rate, which is evidenced below.

Figure 7.3(a) depicts the curves gate voltage shifts of the Al_2O_3 inter-poly capacitors with surface nitridation annealed at 800°C to 1000°C under a constant current stress (CCS) of 5 mA/cm^2 in both polarities. The increase in the absolute gate

voltage indicates that the primary mechanism responsible for the long-term wear-out in Al_2O_3 is the creation of electron traps. Moreover, Al_2O_3 inter-poly capacitors annealed at 900^{o}C exhibits small electron trapping rate than annealed at 800^{o}C or 1000^{o}C. The Weibull distributions of Q_{BD} for samples with various PDA temperatures are shown in Fig. 7.3(b). The dependence of Q_{BD} on polarity due to NH_3 nitridation has been discussed in previous chapter. For positive gate bias, IPD with NH_3 surface nitridation can significantly suppress the formation of an additional layer with lower dielectric constant during post-annealing process and obtain smoother interface, compared to that without nitridation treatment. Furthermore, the presence of a thin Si-N layer can make PDA more effective in eliminating traps existing in the as-deposited films and improve dielectric characteristics under negative polarity. The results clearly reveal Al_2O_3 IPD with optimized 900^{o}C PDA and surface NH_3 nitridation can effectively reduce electron trapping rate as well as obtain high Q_{BD}, which can be ascribed to the less bulk defect density after high-temperature annealing.

The extracted dielectric constant (κ) and IL thickness of Al_2O_3 inter-poly capacitors with surface nitridation annealed at 800^{o}C to 1000^{o}C is seen in Fig. 7.4. The result is consistent with EOT extracted from *C-V* curves and clearly reveals Al_2O_3 IPD with 900^{o}C PDA exhibits better dielectric properties, i.e. higher κ-value and thinner IL, than 800^{o}C and 1000^{o}C annealing.

7.3.2 Conduction Mechanism of the RS Al_2O_3 IPD

Figure 7.5 illustrates the temperature dependence of gate current density at 6 MV/cm of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800^{o}C to 1000^{o}C in O_2 ambient. In general, all samples exhibited considerably weak

measuring temperature dependence on the leakage current density in either polarity, implying that the tunneling mechanism for the Al_2O_3 IPD is Fowler Nordheim-like, rather than Frankel Poole-like. On the other hand, the magnitude of the leakage current was found to be strongly depended on the annealing temperature. The leakage current density of IPD subjected to 900°C annealing is less than 30 nA/cm^2 at 6 MV/cm, which is one order of magnitude lower as compared to 800°C annealing. Moreover, further increasing the annealing temperature up to 1000°C did not help improve the characteristic of the dielectric. The reason for this may be many-fold, and a more detailed description will be given later. According to the results shown in Fig. 7.1 and Fig. 7.5, we believes Al_2O_3 IPD with 900^{o}C PDA can significantly reduce the charge loss from floating gate due to less than 30 nA/cm^2 leakage current at 6 MV/cm even measured at 150^{o}C. The extracted positive-biased and negative-biased effective barrier height (φ_B) of the 900^{o}C-annealed Al_2O_3 IPD is 2.18eV and 2.24eV, respectively, by assuming the effective electron mass in Al_2O_3 to be $0.2m_0$ [119]. Al_2O_3 IPD with 900^{o}C PDA exhibits the largest φ_B than 800^{o}C- and 1000^{o}C-annealed sample, which can reduce electron tunneling probability and lead to better charge retention characteristics.

The trapped charge centroid (X_t) and density (Q_t) in the Al_2O_3 IPDs can be estimated according to the bi-directional *I-V* method [128], [129].

$$X_t = EOT \times \left(\frac{\Delta V_{G+}}{\Delta V_{G+} + \Delta V_{G-}} \right) \tag{7-1}$$

$$Q_t = \frac{\varepsilon_{ox}}{EOT} \left(\Delta V_{G+} + \Delta V_{G-} \right) \tag{7-2}$$

where ε_{ox} is the permittivity of SiO_2, ΔV_{G+} and ΔV_{G-} are the gate voltage shifts when

Poly-II is positively and negatively stressed by a constant current respectively. Gate voltage shifts are extracted from the linear portion of the *J-V* curves at a current level 100 times smaller (1 μA/cm^2) than that of the injection current (100 μA/cm^2) in order to reduce possible re-emission of the trapped electrons [128]. Figure 7.6(a) compares the calculated X_t of Al_2O_3 inter-poly capacitors annealed at various PDA temperatures under positive and negative CCS. Polarity dependent dielectric characteristics can be partially explained by variation of charge centroids. It is shown that the trapped charge centroid for negative CCS is relatively far away from the electron injection electrode, i.e. cathode, results in smaller charge trapping rate and higher Q_{BD} than positive CCS, which is consistent with previous results. Traps near electron injection cathode in positive polarity also enhance dielectric relaxation current. Furthermore, as PDA temperature increases, both centroids of positive and negative CCS move from Al_2O_3/Poly-I interface toward Poly-II/Al_2O_3 interface.

The trapped charge densities of Al_2O_3 inter-poly capacitors at various PDA temperatures under positive and negative CCS are shown in Fig. 7.6(b). Pronouncedly, negative CCS results in smaller trapped electron density than positive CCS, consistent with the lower trapping rate observed in Fig. 7.5(a). Moreover, IPD with 900°C annealing shows a nearly one order of magnitude reduction in the trapped charge density as compared to the 800°C-annealed sample. Al_2O_3 inter-poly capacitors with optimized 900^{o}C PDA and surface NH_3 nitridation can suppress electron trapping rate less than 1×10^{-4}, which is relatively small as comparing to the 800°C- and 1000^{o}C-annealed samples. The corresponding band diagrams including charge centroids and trapped charge densities of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under both polarities are drawn in Fig. 7.7. As charge centroid moving toward electron injection cathode, large voltage shift during CCS is induced

and enhances electron trapping. As a result, polarity dependent dielectric reliabilities are observed in the Al_2O_3 IPDs regardless of annealing temperatures.

7.3.3 Physical Evidences of the Optimized 900°C PDA

In order to study the XPS spectra of Al_2O_3 dielectrics, the blanket wafers with Al_2O_3 deposition on top of the Poly-I annealed at different PDA temperatures are prepared. The detected binding energy of the Al 2p and O 1s signals are calibrated by C 1s signal (284.5eV) [130]. As shown in Fig. 7.8(a), the binding energy of the Al 2p signal is found to gradually increase, while the binding energy of the O 1s signal decreases as the PDA temperature increases to 900°C. This consequence suggests that the dielectric becomes more completely oxidized during high temperature O_2 annealing (the electronegativity of Si, O and Al is 1.9, 3.44 and 1.61, respectively). However, as annealed temperature reaches up to 1000°C, the O binding energy increases but the Al binding energy remains unchanged as compared to the 900°C-annealed IPD. After arranging the background signal to equivalent level, as seen in Fig. 7.8(b), O intensity gradually increases but Al intensity saturates when annealing temperature is higher than 900°C. With annealing temperature larger than 900°C, the oxidation of Al metallic atoms is nearly completed, excess O from annealing ambient turns to oxidize underneath Si substrate and form additional SiO_2 interfacial layer, which is also proven by large EOT shown in Fig. 7.1(a). Both the turnovers of O binding energy and saturated Al intensity are strong evidence that large amounts of Si-O bonds are formed during 1000°C PDA.

Figure 7.9 presents the Al and O atomic concentrations extracted from XPS for various PDA temperatures. The O/Al ratio of as-deposited Al_2O_3 IPD is found to be

higher than 1.5 due to oxygen-rich dielectric deposition [131]. Initially, this non-stoichiometric value decreases as the PDA temperature increases [132]. The O/Al atomic ratio reduces to a nearly stoichiometric value of 1.52 at 900°C, but increases again at 1000°C due to Al loss [133]. Moreover, increased O/Al atomic ratio at 1000°C is partially ascribed to the interfacial SiO_2 growth. According to the previous studies, the electrical properties of Al_2O_3 were reported to be intimately correlated to the film composition. To explain the variation of electrical properties when the annealing temperature increases from 800 to 900°C, including breakdown field and Q_{BD}, we resort to the changes in composition and surface roughness.

The Weibull distributions of breakdown fields for the samples are shown in Fig. 7.10. Sample with 800°C PDA has the largest effective breakdown field than 900°C- and 1000°C-annealed. Since the presence of excess free oxygen can suppress the aluminum rich defects and results in a larger breakdown field [134], the large breakdown field of 800°C-annealed Al_2O_3 IPD can be partially explained by high O/Al ratio. Furthermore, surface roughness also play a key role in determine breakdown field. Taking into account the increased surface roughness of Poly-I upon increasing annealing temperature, as indicated in Fig. 7.11, our result shows that the 800°C-annealed sample did have a higher breakdown field than the 900°C-annealed quite straightforwardly.

In contrast, the dependence of Q_{BD} on the annealing temperature shown in Fig. 7.5 is not consistent with the trend in breakdown field. This occurrence owes to the fact that breakdown is triggered once a critical electron trap density is reached based on the so-called percolation model [71]. The critical electron trap density is strongly dependent on the thickness and inherent physical properties of the dielectric. Therefore, thicker IPDs coming from increasing the annealing temperature exhibit

higher Weibull slopes and Q_{BD} mean value. Moreover, an insufficient thermal annealing budget will result in excess oxygen presented in the bulk, which can act as efficient electron trap centers, making the dielectric more vulnerable to charge wear-out. As a result, the dielectric annealed at 900°C exhibits a better stoichiometric characteristic, smaller trapping rate, and lower trapped electron density, even though the effective breakdown is relatively small.

On the other hand, the situation with 1000°C annealing is more complex. There are several possible mechanisms responsible for the degradation. First, the amount of excess oxygen increases, acting as electron trap centers and degrades Q_{BD}. Second, the formation of extra grain boundaries from the dielectric crystallization during such high temperature annealing serves as additional electron trapping sites [135]. Based on X-ray diffraction (XRD) spectra shown in Fig. 7.12, we observe that after 900°C annealing, the Al_2O_3 film has crystallized. A diffraction peak associated with crystalline Al_2O_3 appears at about 32.9° after 900°C PDA, which corresponds to the $(20\bar{2})$ plane for monoclinic Al_2O_3 [136]. Third, in Fig. 7.11, the measured surface roughness of Poly-I after selectively Al_2O_3 IPD etching was found to increase from 2.89nm for the 900°C annealed IPD to 3.26nm for the 1000°C annealed Al_2O_3 IPD. A rougher interface is more harmful due to the enhanced localized field which leads to higher leakage current, lower Q_{BD} and effective breakdown field [121]. Fourth, the Al_2O_3/Si system is not stable at an ambient of 1000°C, and severe intermixing has been observed in previous research [137]. Figure 7.13 demonstrates the AES depth profiles for Al, O, N and Si elements. Clearly, the inter-diffusion between the Al_2O_3 IPD and underlying Poly-I becomes more notable when annealed at 1000°C. The existence of these Al-Si-O mixtures may act as positive fixed charge centers [138] and facilitate the trapping of electrons. Fifth, phosphorous diffusing from poly-Si may act

as a network modifier and produce non-bridging oxygen, resulting in increased atomic ratio as the PDA becomes higher than 900°C [139]. Consequently, the IPD annealed at 1000°C not only exhibits a slightly larger leakage current, but also a higher electron trapping rate and a smaller Q_{BD} than when annealed at 900°C.

7.4 Summary

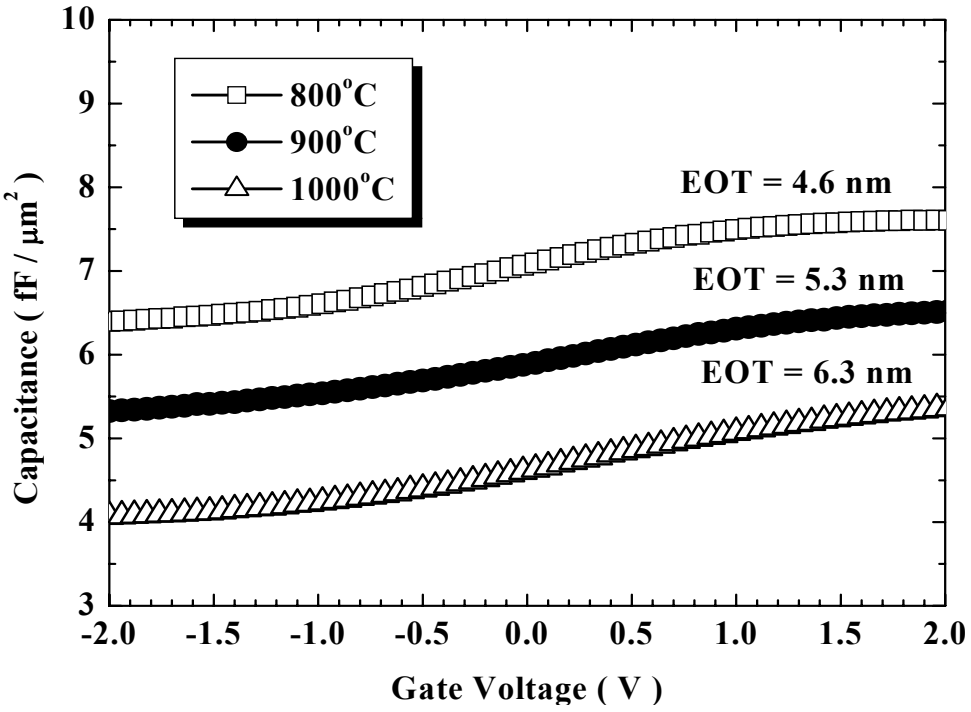
The effects of PDA temperature on the electrical properties and reliability characteristics of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation are evaluated in this chapter. It was found that the electrical properties of Al_2O_3 IPD strongly depend upon the PDA temperature. 900°C annealing is the best condition for the Al_2O_3 IPD electrical characteristic in terms of leakage current, electron trapping rate and Q_{BD}. The XPS and AES analyses indicate that this consequence is closely related to the compositional changes and excess oxygen concentration when changing annealing temperature. The results apparently demonstrate Al_2O_3 IPD with surface nitridation and optimized PDA temperature can effectively reduce charge transfer between control gate and floating gate, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD. The Al_2O_3 dielectric with surface NH_3 nitridation and 900°C annealing thus appears to be very promising for future flash memory devices. Table 7.1 lists several physical and electrical parameters, including EOT, Poly-I surface roughness and the 63%-failure Q_{BD} values of the Al_2O_3 IPDs with surface NH_3 nitridation annealed at various temperatures. κ-value, interfacial layer thickness and extracted φ_B of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures in O_2 ambient are summarized in Table 7.2.

Table 7.1 EOT, Poly-I surface roughness and 63%-failure Q_{BD} values of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under positive and negative CCS at various PDA temperatures in O_2 ambient. Due to the extremely large leakage current, the corresponding EOT and 63%-failure Q_{BD} values of the as-deposited Al_2O_3 inter-poly capacitors can not be determinable.

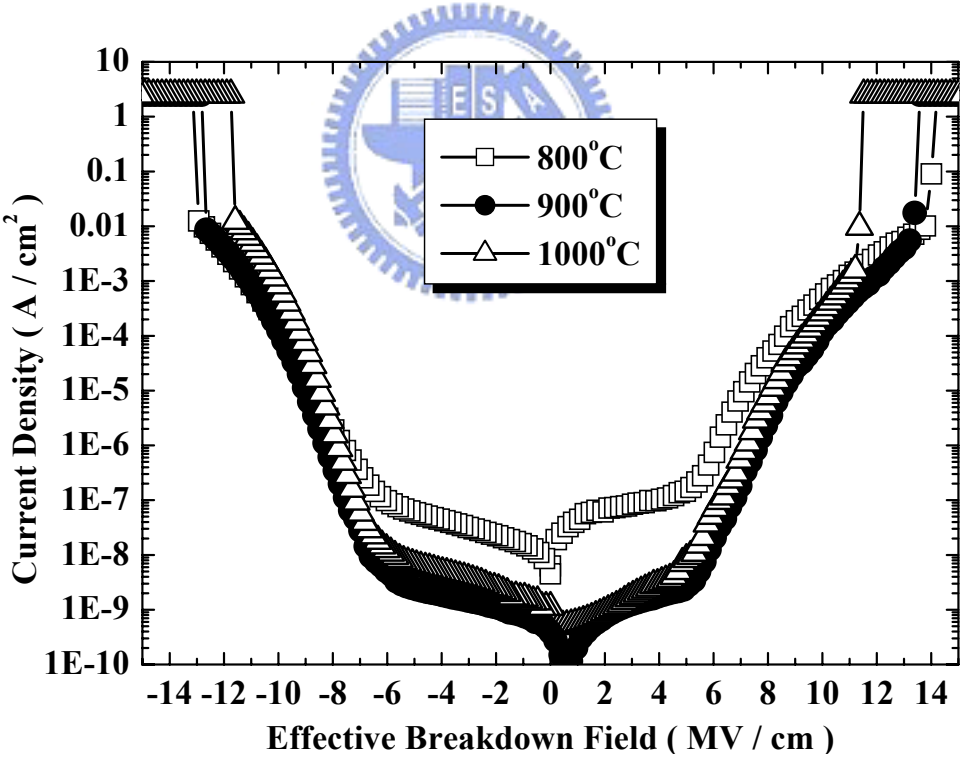
PDA (°C)	EOT (Å)	Poly-I surface roughness (nm)	63% Q_{BD} (C/cm^2)	
			positive	negative
as-deposit	N/A	2.66	N/A	N/A
800	46	2.76	0.065	0.171
900	53	2.89	0.288	0.861
1000	63	3.26	0.257	0.728

Table 7.2 κ-value, interfacial layer thickness and extracted barrier heights of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures in O_2 ambient.

PDA (°C)	κ	IL Thickness (Å)	φ_B (eV)	
			positive	negative
800	8.2	8	1.54	1.62
900	9.3	11	2.18	2.24
1000	9.4	20	2.10	2.15

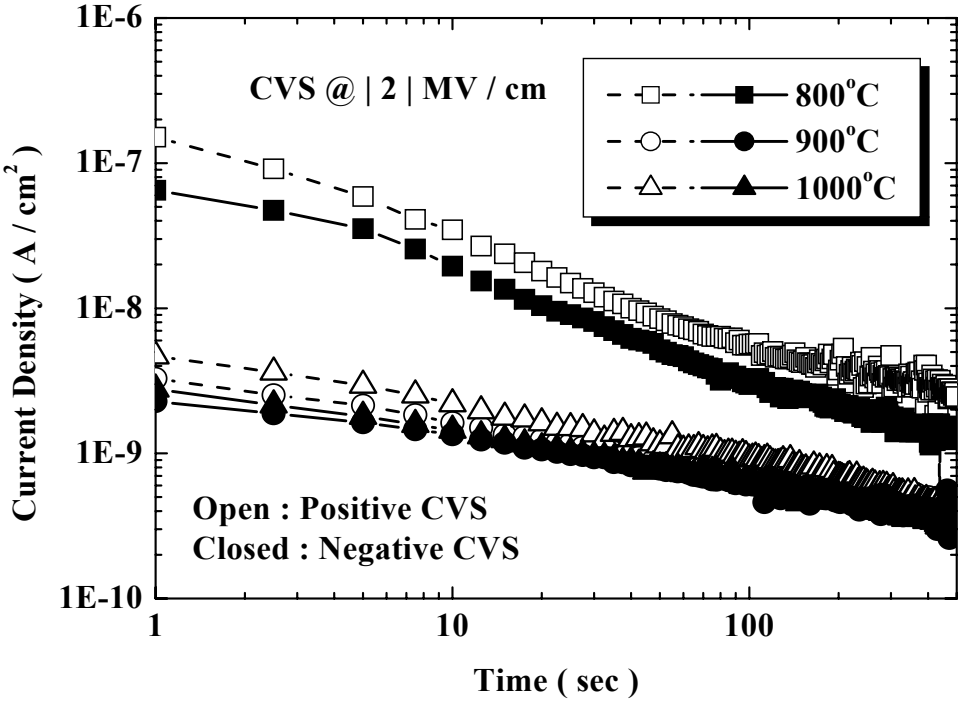


(a)

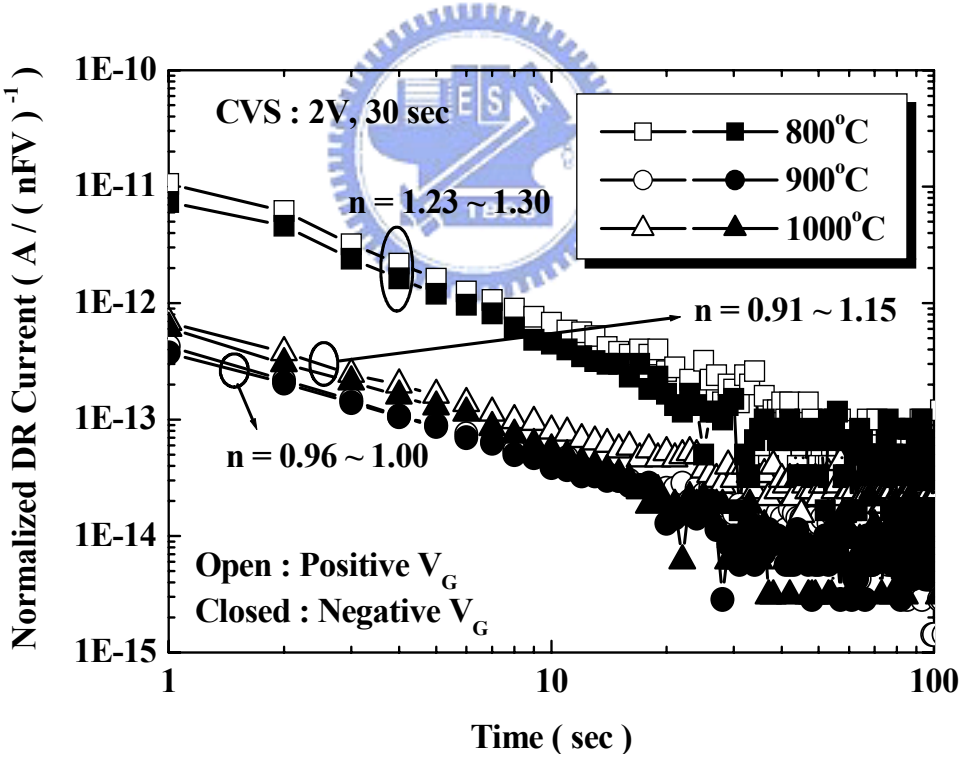


(b)

Fig. 7.1 (a) *C-V* curves (b) *J-E* characteristics of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient. Al_2O_3 inter-poly capacitor with 900°C PDA in O_2 ambient is beneficial in scaling EOT and suppressing low-field leakage current density.

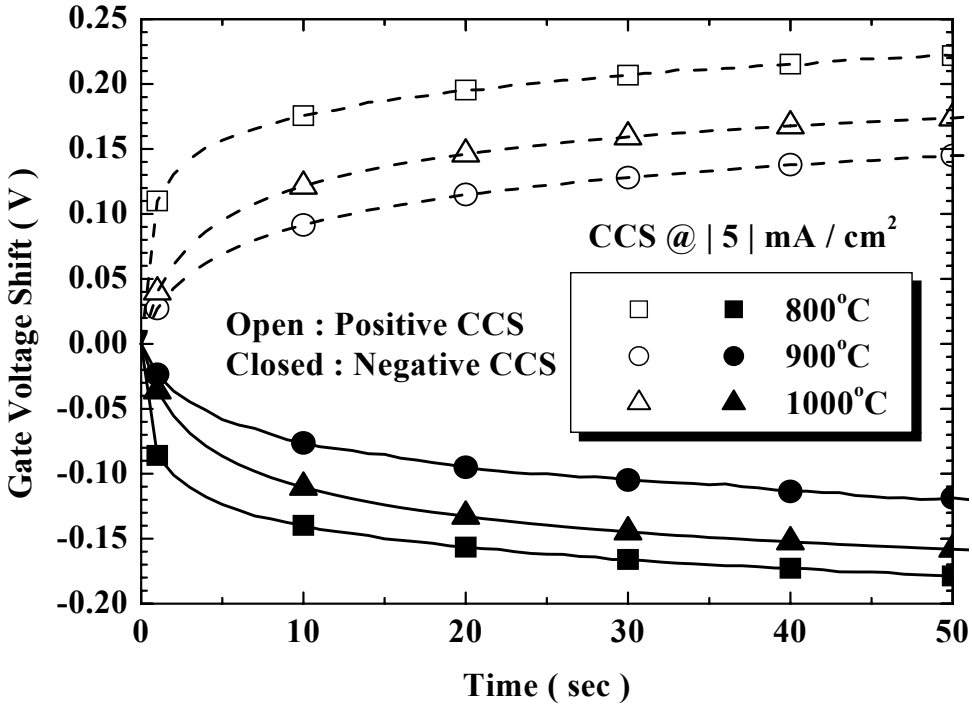


(a)

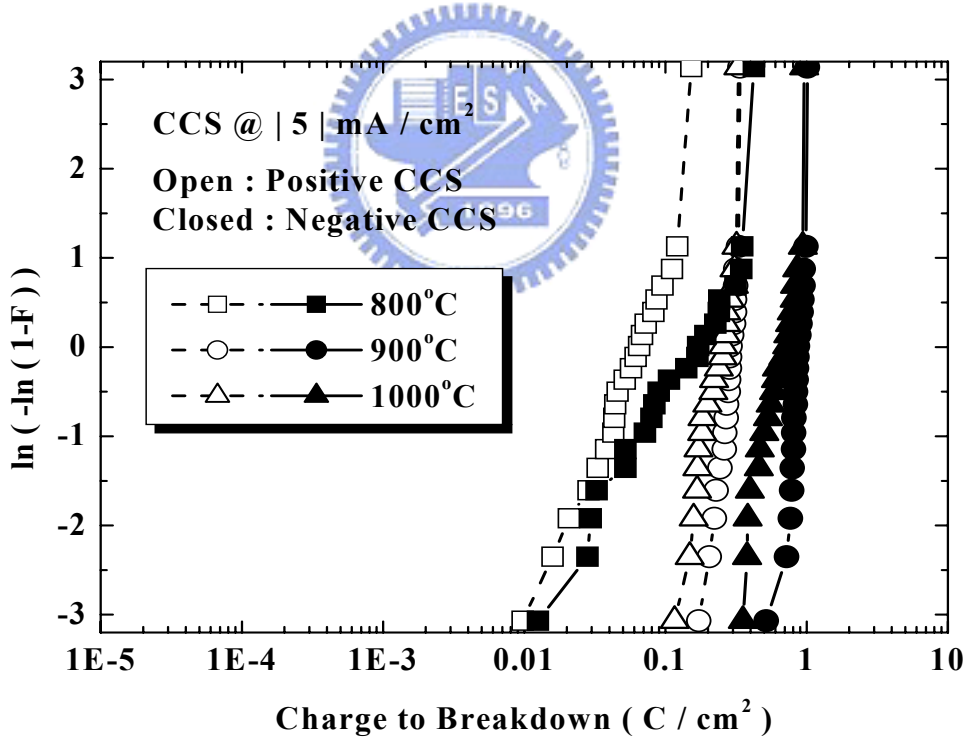


(b)

Fig. 7.2 (a) As-fabrication trap densities evaluation at 2 MV/cm constant voltage stress (CVS) (b) dielectric relaxation current of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient. Al_2O_3 inter-poly capacitor with 900°C PDA in O_2 ambient can reduce as-fabricated trap densities.



(a)



(b)

Fig. 7.3 (a) Curves of gate voltage shift (b) Q_{BD} Weibull plots of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient under constant current stress. Al_2O_3 inter-poly capacitors with optimized 900°C PDA can suppress electron-trapping and increase Q_{BD}.

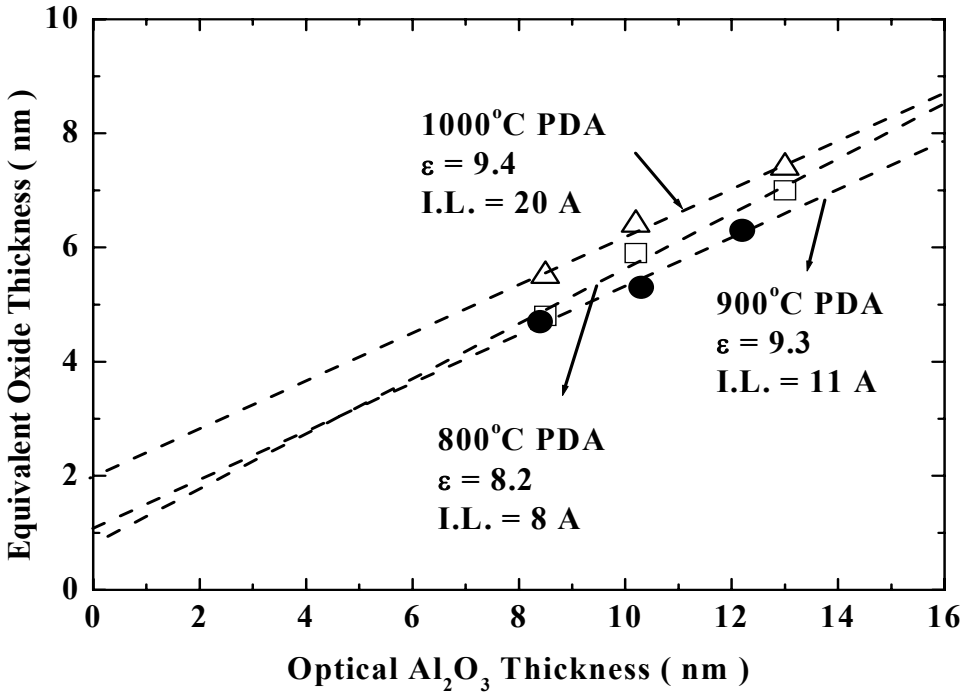


Fig. 7.4 κ-value and IL thickness extraction of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient.

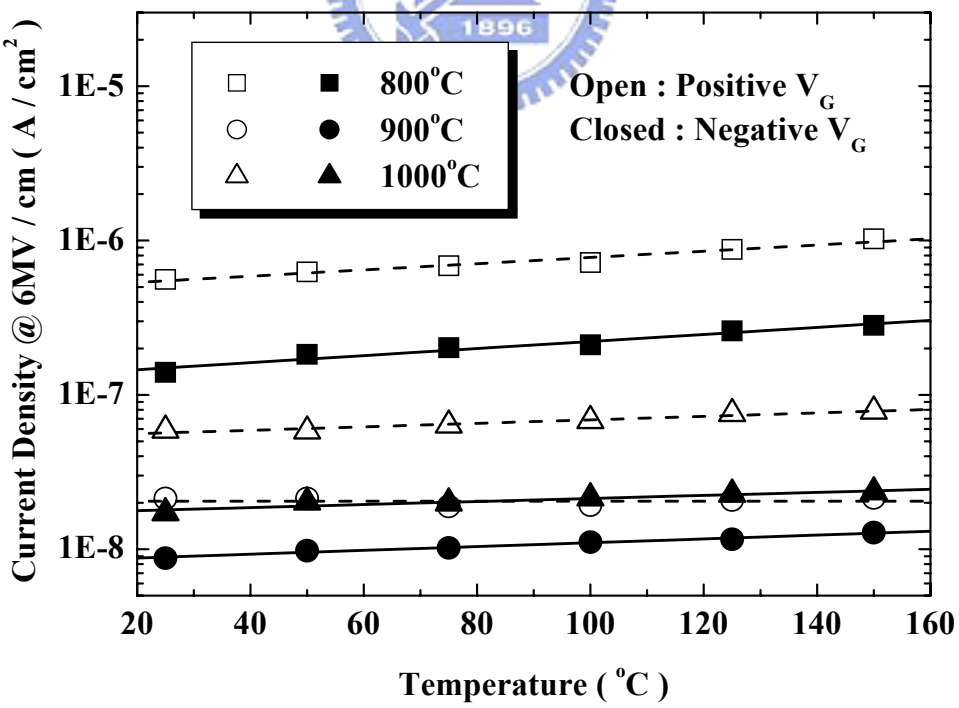
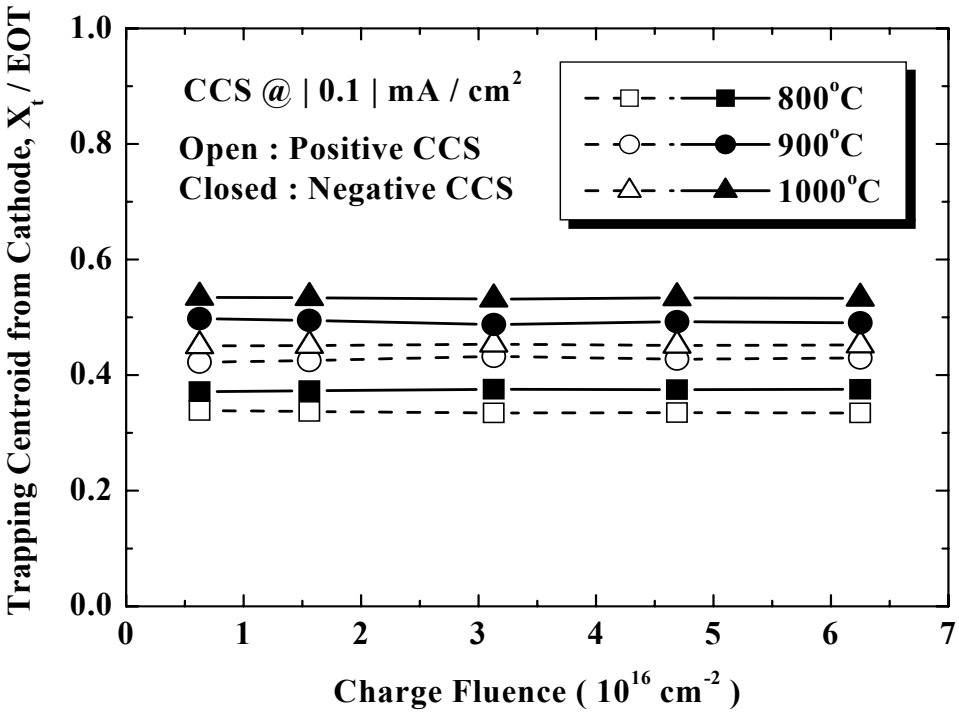
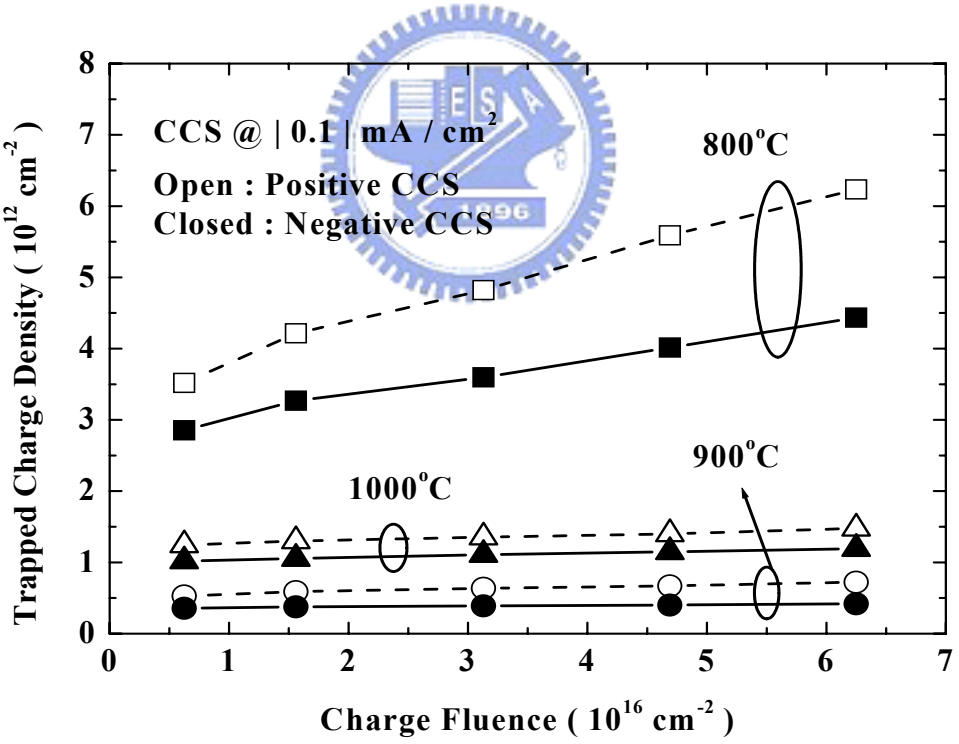


Fig. 7.5 Temperature dependence of gate current density at 6 MV/cm of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C.

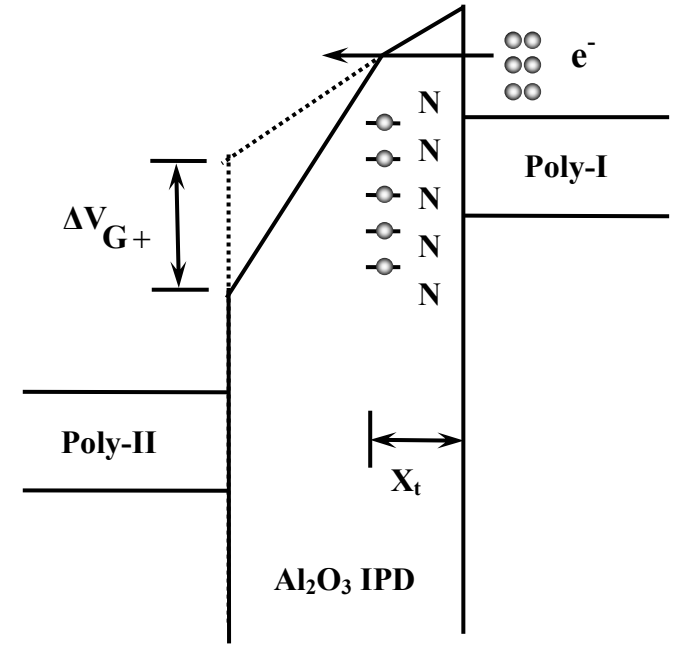


(a)

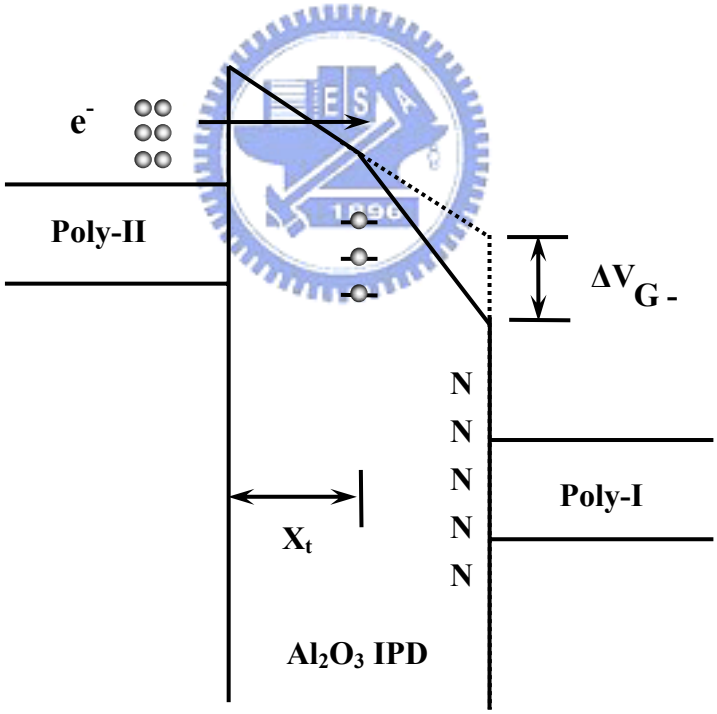


(b)

Fig. 7.6 (a) Centroid of trapped charges (b) trapped charge density of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient under constant current stress. Al_2O_3 inter-poly capacitors with optimized 900°C PDA can suppress electron trapping rate below 10^{-4}.

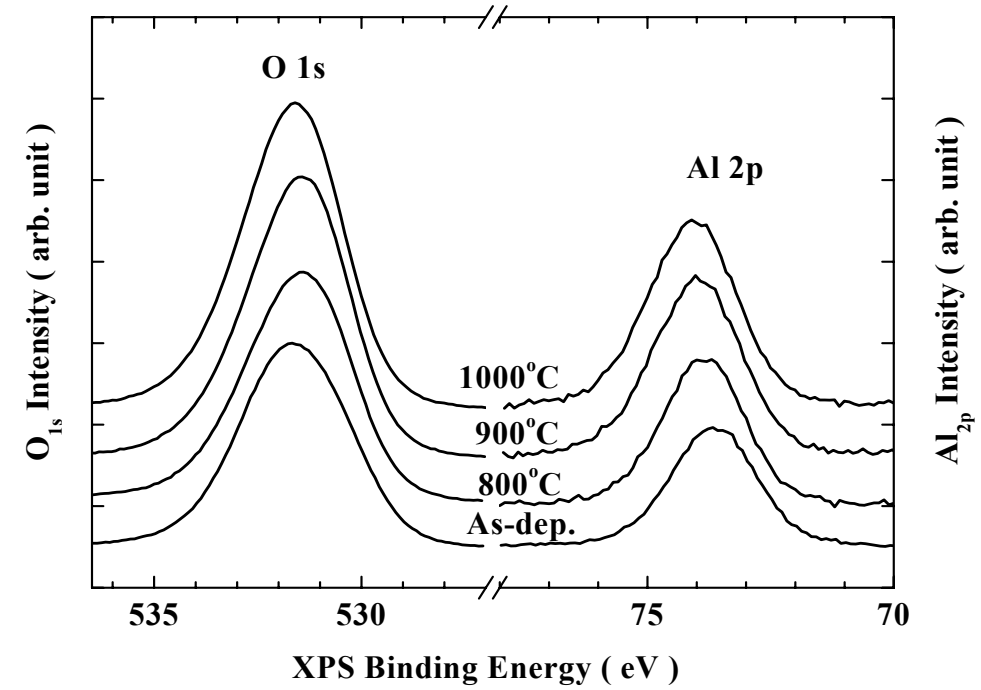


(a)

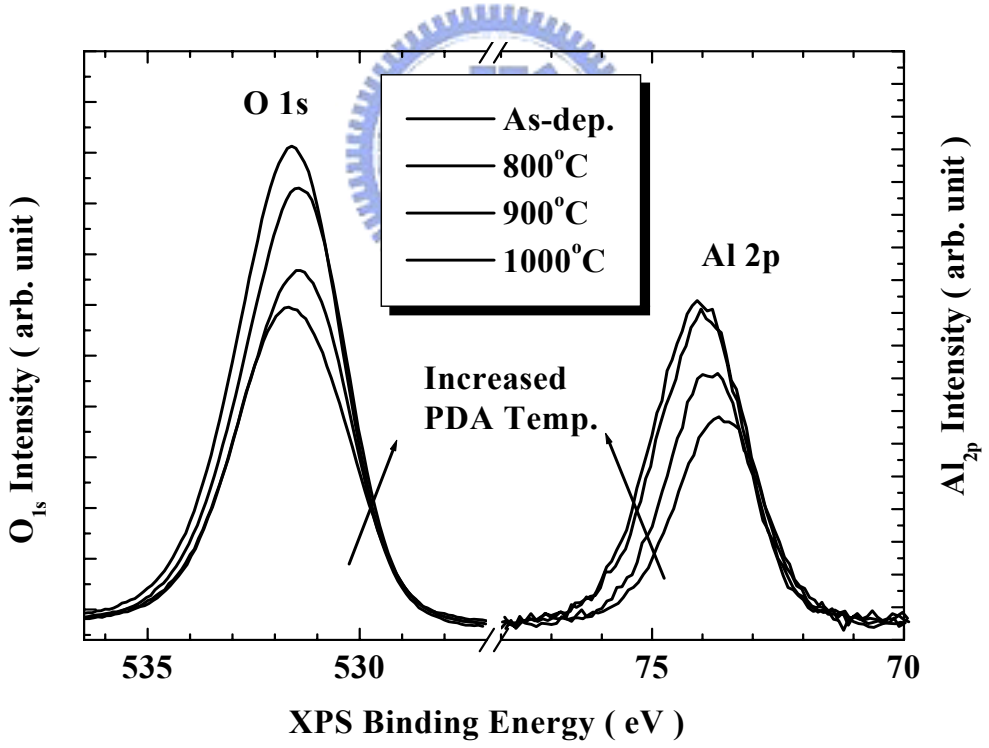


(b)

Fig. 7.7 Band diagrams of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under (a) positive (b) negative gate voltage biased to the Poly-II. Al_2O_3 inter-poly capacitors at negative polarity show less electron trapping and gate voltage shift.



(a)



(b)

Fig. 7.8 (a) XPS binding energy spectrum (b) corresponding XPS binding energy spectrum after arranging to the equivalent background signal for the O 1s and Al 2p signals as a function of PDA temperatures with C 1s calibration at 284.5 eV. The binding energy of O and Al signals is strongly dependent on PDA temperature.

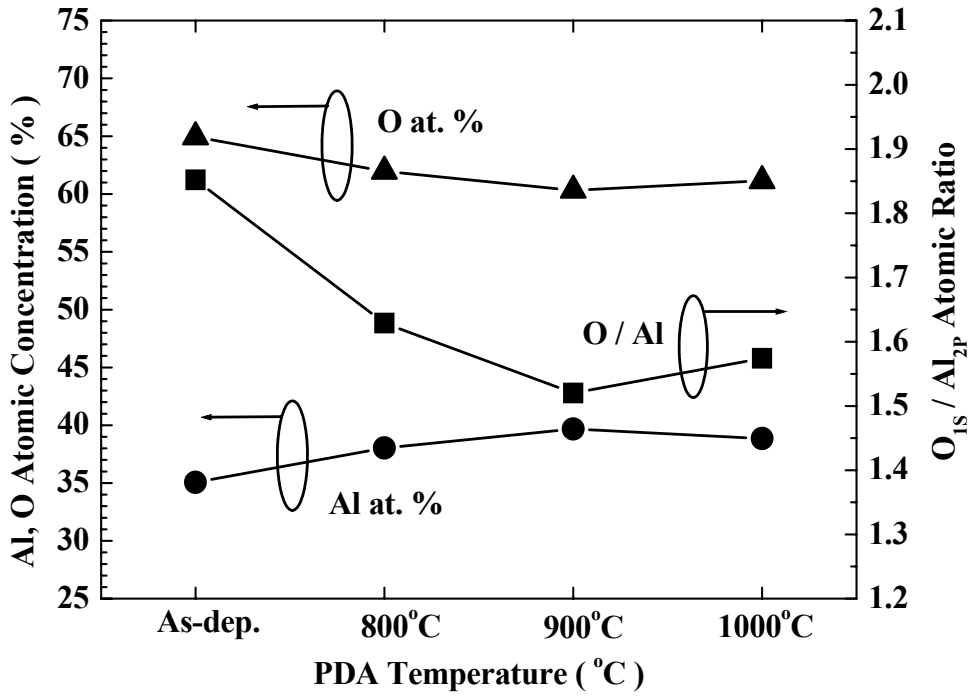


Fig. 7.9 Al and O atomic concentrations extracted from XPS as a function of PDA temperatures with C 1s calibration at 284.5 eV.

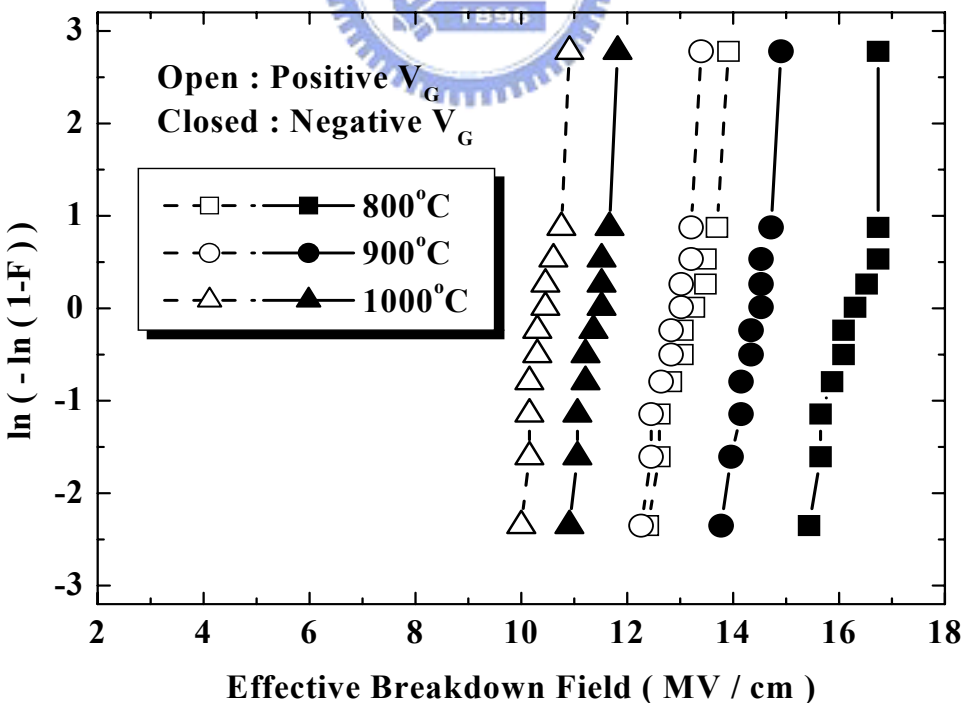
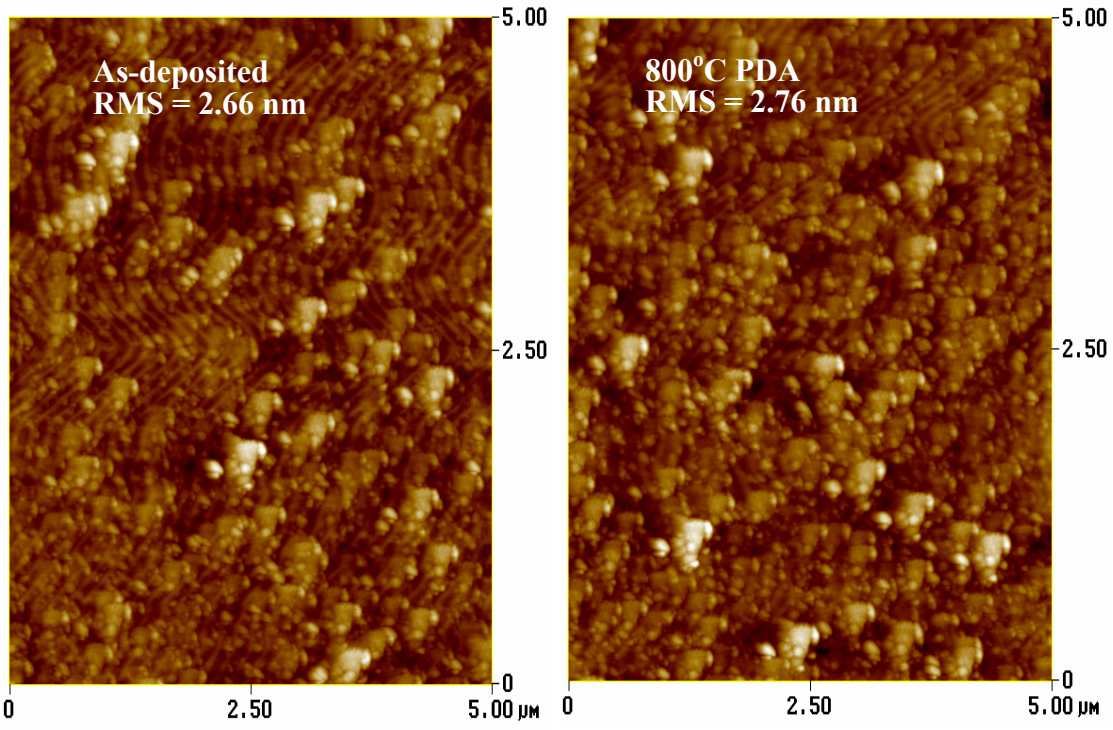


Fig. 7.10 Weibull plots of effective breakdown field of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient.



(a)

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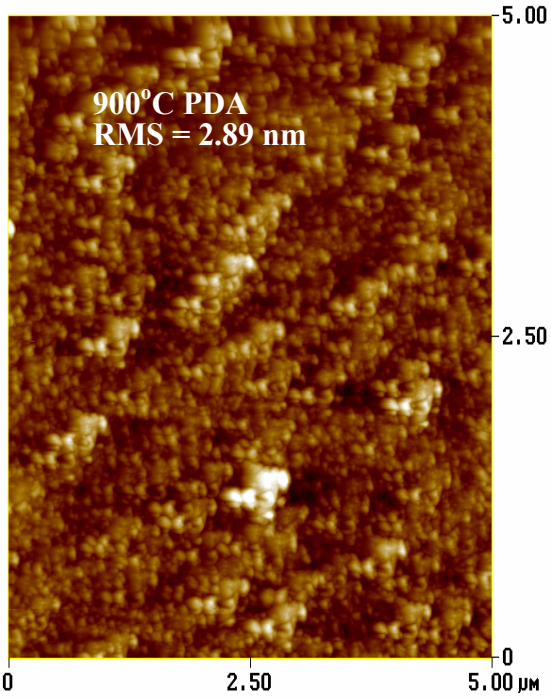

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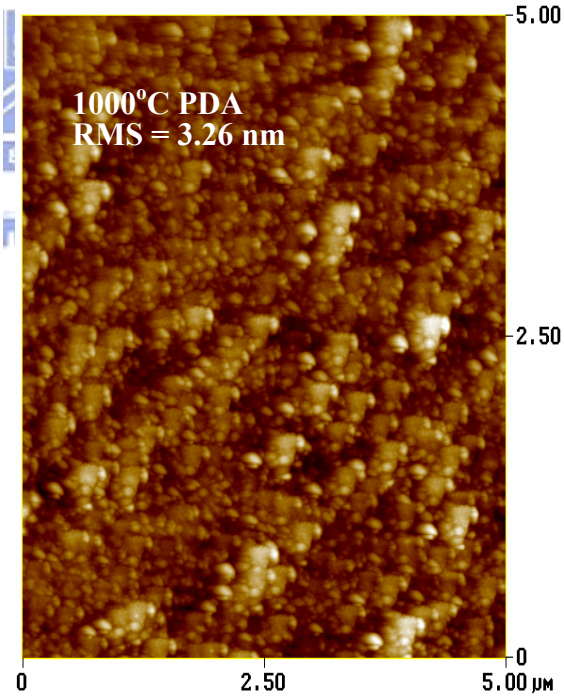

(d)

Fig. 7.11 AFM images (5μm×5μm) of the poly-I surface of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation for (a) as-deposited (b) 800°C (c) 900°C (d) 1000°C PDA in O_2 ambient. Surface roughness becomes more severe as PDA temperature increasing.

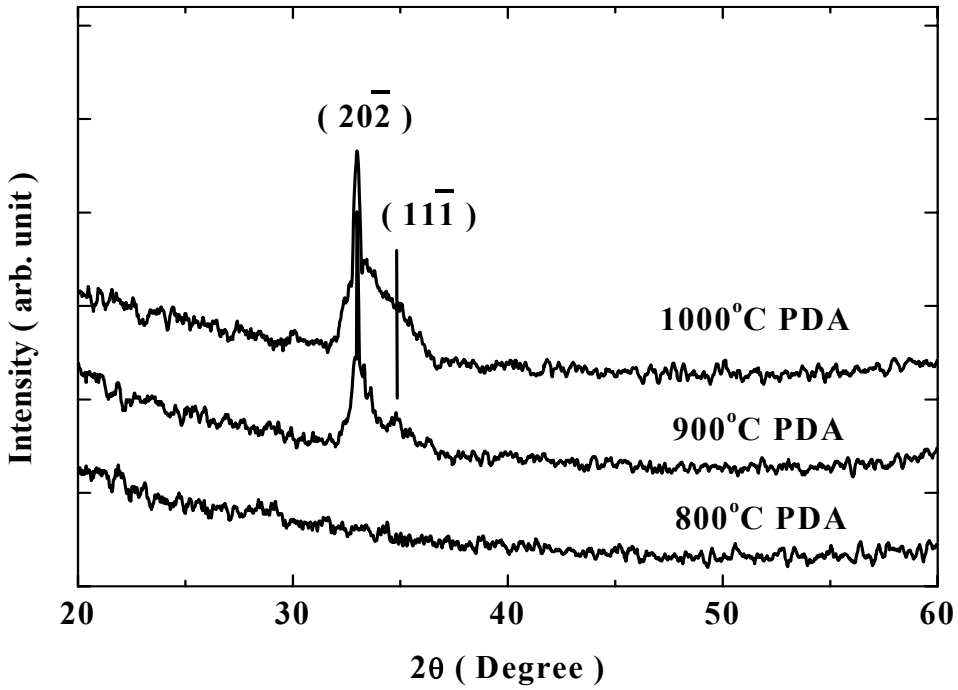

Fig. 7.12 XRD spectra for aluminum oxide on Si(100). Al_2O_3 IPD is crystallized while PDA temperature larger than 900°C.

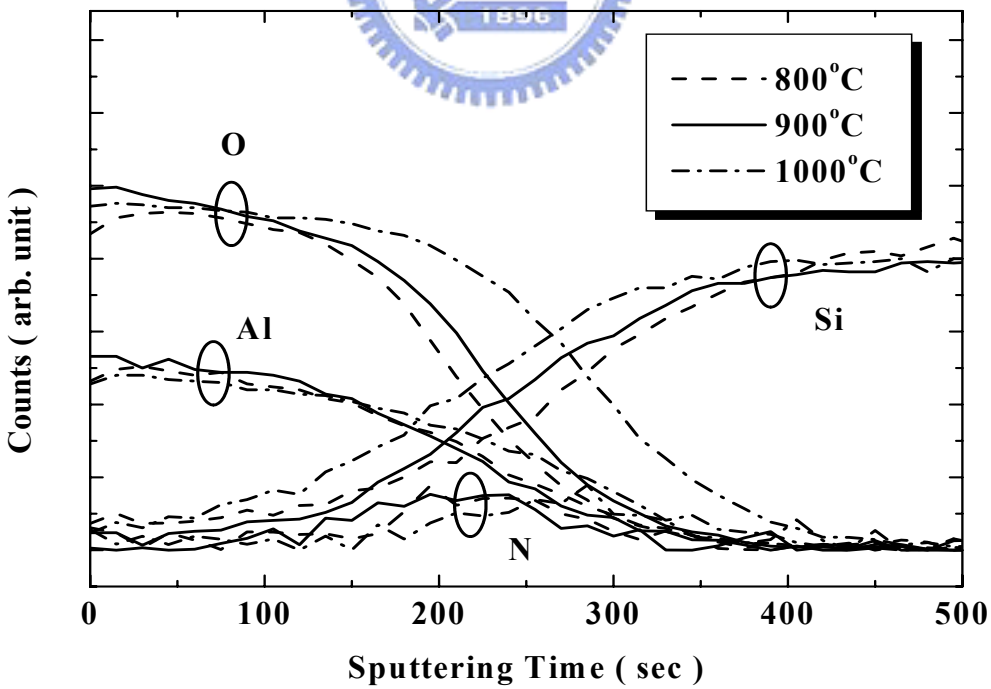

Fig. 7.13 AES depth profiles of Al_2O_3 IPD with surface NH_3 nitridation annealed at 800°C to 1000°C in O_2 ambient. The signal of N is magnified by 5 times.

CHAPTER 8

Thickness Scaling and Reliability Improvement of High-κ IPD for Next Decade Stacked-Gate Flash Memories

8.1 Introduction

Recently flash market increases exponentially and especially mass storage applications have took-off in addition to code storage area. In the coming decade, we will be required to provide flash technologies that are compatible with embedded DRAM read/write speed with high retention. In order to meet the requirement, not only to reduce leakage current through inter-poly dielectric (IPD) and tunnel oxide, but also to improve electric field and charge-to breakdown of the dielectrics. Previous, we had presented the effects of surface NH_3 nitridation and post-deposition annealing temperature on reactive-sputtered Al_2O_3 IPD characteristics in Chapter 6 and 7, respectively. However, even after process optimization, the breakdown charges of Al_2O_3 IPD deposited by reactive sputtering are relatively low [22], [23]. In this chapter, inter-poly dielectric thickness scaling and reliability characteristics are studied on the Al_2O_3 and HfO_2 IPDs, and compared with TEOS IPD. Drastically leakage current reduction and reliability improvement has demonstrated by replacing TEOS IPD by high-κ IPDs, which are suitable to apply for mass production in the future.

8.2 Experimental Details

The n^+-polysilicon/High-κ IPD/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 950^{o}C to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620^{o}C and subsequently implanted with phosphorous at 5×15cm^{-2}, 20keV, then activated with RTA at 950°C for 30s. Prior to the deposition of high-κ IPDs, Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides, then subjected to ammonia (NH_3) nitridation in the LPCVD furnace at 800°C for 1hour. Sub-10nm Al_2O_3 and HfO_2 IPDs was deposited either by reactive sputtering (RS) in an Ar/O_2 ambient at room temperature or by metal organic chemical vapor deposition (MOCVD) with O_2 gas at 400^{o}C. Post-deposition annealing of Al_2O_3 and HfO_2 IPDs was carried out by rapid thermal annealing at 900^{o}C and 800^{o}C, respectively, for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD and implanted with phosphorous at 5×15cm^{-2}, 20keV. Dopants were then activated with RTA at 950°C for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional view and key process steps of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition oxygen annealing are shown in Fig. 4.1 and 5.2, respectively. Tera-ethyl-ortho-silicate (TEOS) IPD deposited at 700^{o}C LPCVD followed by 900^{o}C annealing was used for references.

The equivalent oxide thickness (EOT) was obtained from the high frequency (100kHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284 LCR meter. Moreover, the physical thickness was estimated by high resolution

transmission electron microscopy (HRTEM). The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer. Table 8.1 summarized the deposition conditions and EOT of the various IPDs deposited either by LPCVD, RS or MOCVD.

8.3 Results and Discussions

Figure 8.1 plots leakage current density at V_G = 5V for various IPD candidates. Leakage current density is increasing as EOT of IPD scaling down. Comparing to TEOS IPD, RS Al_2O_3 IPD can reduce leakage current density larger than 1 order of magnitude in both polarities. Further leakage current reduction can be achieved by changing RS Al_2O_3 IPD to MOCVD Al_2O_3 and HfO_2 IPD. Larger than 2 and 3 order of magnitude leakage current reduction comparing to TEOS IPD is expected by alternative deposition instrument.

Breakdown voltage (BV) comparison between high-κ IPDs and TEOS IPD is shown in Fig. 8.2. As EOT scaling down, BV decreases. RS Al_2O_3 IPD can provide larger than 1V BV increment than TEOS IPD in both polarities, although the improvement seems to vanish for EOT less than 5nm. Comfortingly, MOCVD Al_2O_3 IPD exhibits larger than 10V BV, which is nearly twice of TEOS IPD. While adopting to HfO_2, BV can maintain larger than 6V as the EOT = 3.3nm regime. After eliminating thickness effect, effective breakdown electric field (BE_{eff}) is still higher than TEOS IPD, presented in Fig. 8.3. BE_{eff} is extended to larger than 2 MV/cm and 8 MV/cm for RS and MOCVD Al_2O_3 IPD, respectively. Both MOCVD Al_2O_3 and HfO2 IPD can stand for as high as 19 MV/cm breakdown field, which are enough to be

applied for next decade flash memory.

In the dielectric reliability point of view, high-κ IPDs also examine superior charge-to-breakdown (Q_{BD}), as drawn in Fig. 8.4. Our results indicate Q_{BD}-value of IPDs is strongly dependent on dielectric thickness. From percolation model [71], the critical electron trap density is strongly dependent on the thickness and inherent physical properties of the dielectric. Therefore, thicker IPDs exhibit higher breakdown voltage and Q_{BD} mean value, contribute to bulk-dominant dielectric breakdown in both polarities. RS Al_2O_3 IPD reveals near 1-order of magnitude Q_{BD} improvement than TEOS IPD in both polarities. On the other hand, albeit that RS Al_2O_3 IPD can tolerate higher Q_{BD} than TEOS IPD, the maximum Q_{BD} observed is only ~ 1 C/cm^2, which may be a another major challenge for RS Al_2O_3 IPD to be used to replace conventional IPD. Insufficient Q_{BD} becomes more severe as EOT scaling down due to bulk-dominant dielectric breakdown, predicted by percolation model. Fortunately, Q_{BD} can be drastically improved by MOCVD tool. The 63% failure Q_{BD} of MOCVD Al_2O_3 IPD is about 5.5 C/cm^2 in positive polarity, which is near 1 order of magnitude improvement comparing to RS Al_2O_3 IPD. Nevertheless, negligible Q_{BD} improvement is observed for negative polarity. Mechanism of significantly polarity-dependent Q_{BD} of MOCVD Al_2O_3 IPD is unknown yet and need further inspection. For MOCVD HfO_2 IPD, the calculated Q_{BD} is relatively poor partially from thinner EOT than Al_2O_3 IPD. Breakdown voltage, effective breakdown field and Q_{BD} values of the various IPDs deposited either by LPCVD, RS or MOCVD are listed in Table 8.2.

Although the real mechanism for dielectric characteristics promotion of MOCVD IPDs is not clear yet, one possible explanation is speculated from less defect density and uniform thickness of MOCVD deposited dielectrics. Consequently, EOT of IPD can be further scaled down to 3nm by HfO_2 IPD without degradation dielectric

characteristics significantly, which is the thinnest EOT of IPD for stacked-gate flash memory in our knowledge.

8.4 Summary

Previous, we had presented the effects of surface NH_3 nitridation and post-deposition annealing temperature on reactive-sputtered Al_2O_3 IPD characteristics in Chapter 6 and 7, respectively, and found an optimized 900^oC PDA with surface nitridation could significantly improve IPD reliability. However, even after process optimization, the quality of Al_2O_3 IPD deposited by RS still can not meet the stringent requirement due to relative low Q_{BD}. In this chapter, dielectric characteristics including, leakage current density, effective breakdown field and Q_{BD} of Al_2O_3 IPD are compared with LPCVD TEOS IPD and MOCVD Al_2O_3 and HfO_2 IPD. The results clearly indicate high-κ IPDs, regardless of deposition tools, exhibits high potential to replace TEOS IPD. Moreover, MOCVD deposition demonstrates significant reliability improvement compared to RS deposition. The Q_{BD} can be significantly improved as well as reduced leakage current density, enhanced breakdown voltage and effective breakdown field by using MOCVD replacing RS. According to the 2003 ITRS roadmap, the required low-field leakage current should be less than 1 mA/cm^2 @ 5V [28]. Our results clearly demonstrate that as thin as 5nm and 3nm EOT of MOCVD-deposited Al_2O_3 and HfO_2 IPD is suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories, respectively.

Table 8.1 Deposition conditions and EOT of the various IPDs deposited either by LPCVD, RS or MOCVD.

IPD Material	Surface Nitridation	PDA (°C)	EOT (Å)
TEOS	**without**	**900**	**65**
RS Al_2O_3	**with**	**900**	**47**
RS Al_2O_3	**with**	**900**	**53**
RS Al_2O_3	**with**	**900**	**63**
MOCVD Al_2O_3	**with**	**900**	**55**
MOCVD HfO_2	**with**	**800**	**32**

Table 8.2 Breakdown voltage, effective breakdown field and 63%-failure Q_{BD} values of the various IPDs deposited either by LPCVD, RS or MOCVD.

IPD Material	BV (V)		BE_{eff} (MV/cm)		63% Q_{BD} (C/cm^2)	
	positive	negative	positive	negative	positive	negative
TEOS	**8.5**	**7.5**	**13.08**	**11.54**	**0.103**	**0.067**
RS Al_2O_3 47Å	**5.6**	**5.9**	**11.9**	**12.55**	**0.159**	**0.619**
RS Al_2O_3 53Å	**6.9**	**7.6**	**13.0**	**14.3**	**0.287**	**0.861**
RS Al_2O_3 63Å	**8.2**	**8.9**	**13.0**	**14.1**	**0.554**	**1.151**
MOCVD Al_2O_3	**10.4**	**10.6**	**18.9**	**19.3**	**5.491**	**0.891**
MOCVD HfO_2	**6.2**	**6.2**	**19.4**	**19.4**	**0.191**	**0.023**

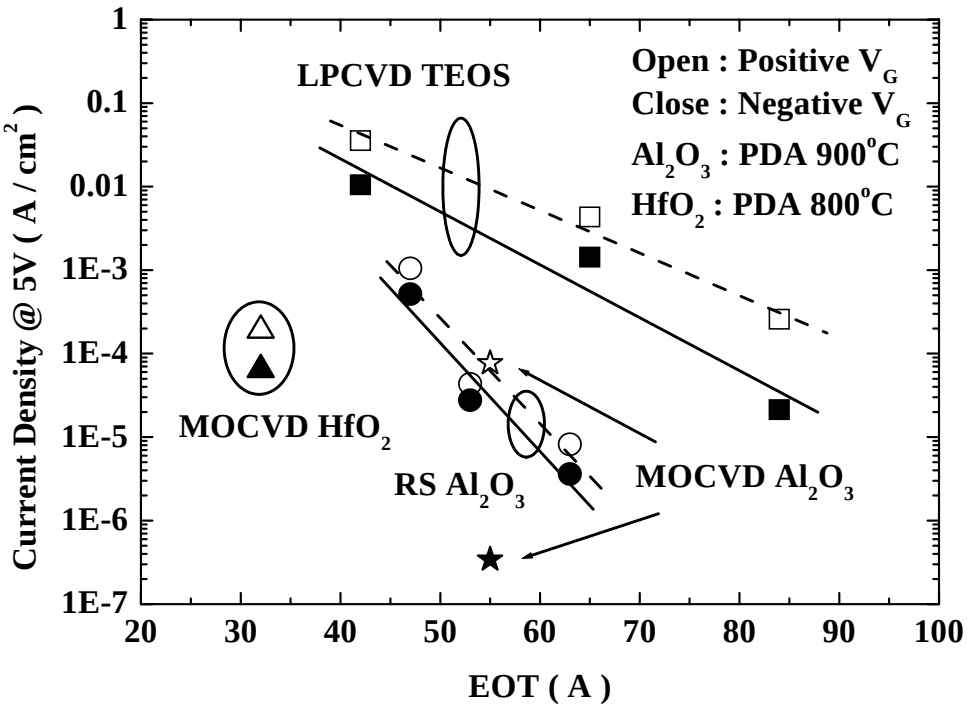

Fig. 8.1 Current density at 5V as a function of EOT for various IPDs. High-κ IPDs can reduce leakage current larger than 1-order of magnitude.

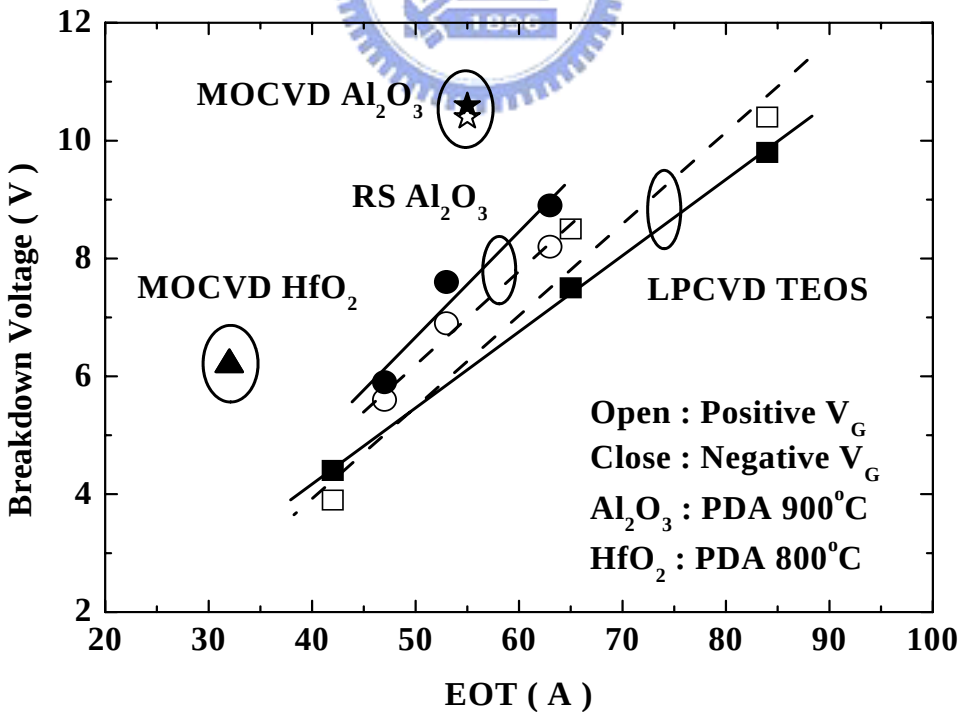

Fig. 8.2 Breakdown voltage as a function of EOT for various IPDs. High-κ IPDs exhibits higher breakdown voltage than TEOS IPD.

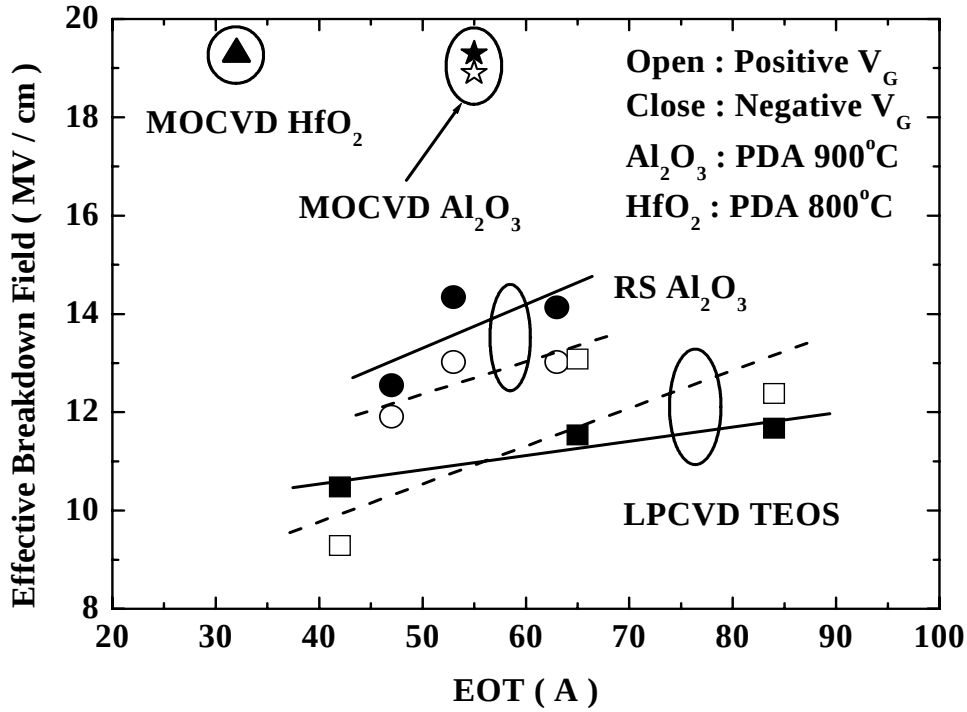

Fig. 8.3 Effective breakdown field as a function of EOT for various IPDs. High-κ IPDs exhibits higher breakdown field than TEOS IPD.

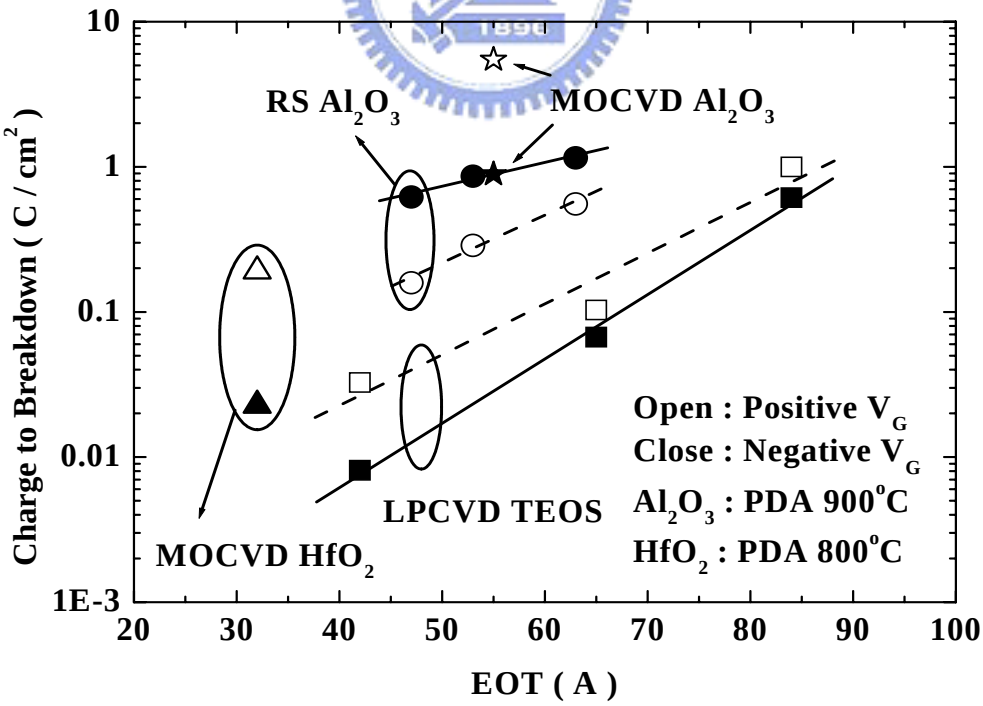

Fig. 8.4 Charge-to-breakdown as a function of EOT for various IPDs. High-κ IPDs exhibits higher Q_{BD} than TEOS IPD.

CHAPTER 9

Conclusions and Recommendations for Future Works

9.1 Conclusions

According to SIA roadmap, oxide thickness small than 20Å is necessary for deep sub-quarter micron devices. However, pure SiO_2 can't meet the requirement due to the large tunneling current. In our study, N atomic concentration is shown to depend on the initial oxide thickness, i.e., with decreasing oxide thickness from 63Å to 22Å, the N concentration increases from 2.12 to 4.45 at.% in the interface, which was desired for the improvement of dielectric reliability in the ultrathin region. NO-annealing can achieve better SILC immunity for both constant voltage and constant current stress. Moreover, NO-annealing also improves interface smoothness and results in tighter TDDB distribution. Even after process optimization in the future, NO-annealing can be used to improve device performance more apparent, as predicting in mind. As a result, NO-annealed nitrided oxides can improve dielectric reliability and are suitable to replace traditional SiO_2 at 0.13μm and beyond.

The dielectric properties and reliability characteristics of NIS nitrided oxides are also investigated. An obvious oxidation rate retardation effect is observed for nitrided oxides with nitrogen-implanted substrate. Dielectric property is strongly depended on NIS dosage and post-oxidation annealing temperature. NIS dosage less than 1×10^{14} cm^{-2} is helpless to oxidation rate suppression and degrades dielectric reliability as well.

On the contrary, samples with 1×10^{15} cm^{-2} NIS not only can use to grow multiple oxide thickness to meet SOC requirement, but also improve stress immunity apparently. Nitrogen implantation also generates a uniform distribution nitrogen profile in the dielectric bulk, which can be used as an effective diffusion barrier to resist boron penetration. NIS nitrided oxides could effectively suppress trap generation and improve time-to-breakdown and charge-to-breakdown, also suitable to reduce process steps of the SOC technology.

In order to realize high speed and low power operation of flash memory technologies, devices with high coupling ratio are necessary. From MEDICI simulation, Al_2O_3 IPD and HfO_2 IPD can increase gate-coupling ratio by 45% and 92%, respectively. By 2-D MEDICI simulation, flash memories with high-κ IPDs clearly exhibit significant improvement in programming/erasing speed over those with conventional ONO IPD. Moreover, it is found that high-κ IPDs is more effective for the memories programmed/erased with FN tunneling rather than channel hot carrier injection. Choosing HfO_2 as the IPD and using FN programming/erasing scheme, the operating voltage can be reduced 48% at a typical program time of 10 μs and 0.1 ms erasing time. Therefore, Al_2O_3 and HfO_2 with medium high κ value and sufficient barrier height show the great potential for the application of high seed and low voltage flash memories. Our results also show that dielectrics with very high permittivity (κ > 25) may not be necessary for the IPD in stacked-gate flash memories.

On the other hand, the effect of high-κ TDs is quite different with high-κ IPDs. Due to the reduced gate coupling ratio, the programming/erasing speed of stacked-gate flash memories with high-κ TDs by using FN tunneling is helpless in reduction operation voltage. On the other hand, the increased electric field on HfO_2 IPD would produce excess charge loss and narrow the operation window between

programmed and erased state. Although the electric field on high-κ tunnel dielectrics is lower than SiO_2 tunnel oxide, enhanced impact ionization rate and lower φ_B contribute to higher CHE injection current and efficiency. Consequently, high-κ TDs are only effective for the memories programmed/erased with hot electron injection rather than FN tunneling. Due to the contrary improvement in programming/erasing schemes, high-κ IPDs and TDs are suitable for next-generation NAND- and NOR-type stacked-gate flash memories, respectively.

Finally, the effect of NH_3 nitridation of Poly-I and PDA temperature on the electrical properties and reliability characteristics of the Al_2O_3 inter-poly capacitors are evaluated. With surface NH_3 nitridation, the formation of an additional layer with lower dielectric constant during post-annealing process can be significantly suppressed and reduced the EOT to 4.6nm, compared to that without nitridation treatment. Furthermore, the presence of a thin Si-N layer can make post-deposition annealing more effective in eliminating traps existing in the as-deposited films. As a result, a smoother interface and smaller electron trapping rate can contribute to the drastically reduced leakage current, enhanced breakdown field and Q_{BD} of Al_2O_3 interpoly capacitors with surface NH_3 nitridation for both polarities. Moreover, it was found that the electrical properties of Al_2O_3 IPD strongly depend upon the PDA temperature. 900°C annealing is the best condition for the Al_2O_3 IPD electrical characteristic in terms of leakage current, electron trapping rate and charge-to-breakdown. The XPS and AES analyses indicate that this consequence is closely related to the compositional changes and excess oxygen concentration when changing annealing temperature. The results apparently demonstrate Al_2O_3 IPD with surface nitridation and optimized PDA temperature can effectively reduce charge transfer between CG and FG, better retention and disturb characteristics are expected

by replacing ONO IPD to Al_2O_3 IPD. MOCVD Al_2O_3 and HfO_2 IPD are investigated in order to further promote Q_{BD} of RS Al_2O_3 IPD. The Q_{BD} can be significantly improved as well as reduced leakage current density, enhanced breakdown voltage and effective breakdown field by using MOCVD replacing RS. As thin as 5nm and 3nm EOT of Al_2O_3 and HfO_2 IPD is suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories, respectively.

9.2 Recommendations for Future Works

1. More HRTEM images to evidence thickness variation and interfacial layer reaction.
2. Further reduced surface roughness to promote charge-to-breakdown value larger than 10 C/cm^2.
3. Alternative high dielectric constant candidates, including AlON, HfSiO and HfSiON, etc.
4. Fully fabricated stacked-gate flash memories with high-κ inter-poly dielectrics and tunnel dielectrics to study the device characteristics, including program/erase speed, retention time and charge loss mechanism.

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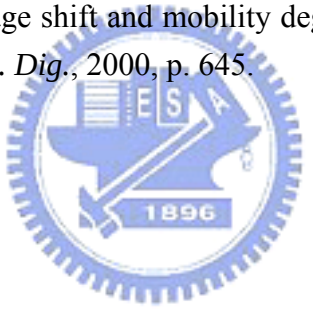

VITA

YEONG-YUH CHEN was born on February 7, 1975, Changhua, Taiwan, Republic of China. He finished his elementary and junior education in Changhua, Taiwan. In 1989, he attended the National Taipei Institute of Technology in the Department of Electronics Engineering. In 1995, he attended the National Taiwan Institute of Technology in the Department of Electronics Engineering. He graduated and received his Bachelor degree in 1997. He started his graduate study in the Institute of Electronics, National Chiao-Tung University in 1997, under the guidance of Professor Jen-Chung Lou and Dr. Chao-Hsin Chien. Since 1998 he has been studying for his Ph. D. degree. His doctoral research involved the thickness scaling and reliability investigation of gate dielectrics and inter-poly dielectrics using nitrided oxides and high-dielectric constant materials.

During the academic year 2000-2001, he worked at the Diffusion Division, Macronix International Corporation on advanced nitrided oxides development. During June 2001 to so far, he joined the high-κ dielectric investigation group under the direction of Dr. Chao-Hsin Chien, and focus on the impact of high-κ materials on stacked-gate flash memories through 2D Medici simulation and experimental characteristics of the inter-poly high-κ dielectrics. During Jan. 2003 to so far, he joined the Diffusion Department, Process Section II, Powerchip Semiconductor Corporation on advanced Ta_2O_5 high-κ dielectrics development cooperated with ERL, ITRI for next generation DRAM. During March 2004 to so far, he joined the Advanced Technology Development Division, Nanya Technology Corporation on alternative Al_2O_3 high-κ dielectrics development for next generation DRAM.

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