CHAPTER 3

Growth of the device-quality GaAs epitaxial layers on Si substrates

A SiGe buffer structure for growing of the high-quality GaAs layers on Si (100) substrate is proposed in this chapter. For the growth of this SiGe buffer structure, a 0.8μm $Si_{0.1}Ge_{0.9}$ layer was first grown. Due to the large mismatch between this layer and the Si substrate, many dislocations formed near the interface and in the low part of the $Si_{0.1}Ge_{0.9}$ layer. A 0.8μm $Si_{0.05}Ge_{0.95}$ layer and a 1.0μm top Ge layer were subsequently grown. The strained $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ and Ge/ $Si_{0.05}Ge_{0.95}$ interfaces formed can bend and terminate the upward-propagated dislocations very effectively. The *in situ* annealing process is also performed for each individual layer. Finally a 1-3 μm GaAs film was grown by MOCVD at 600℃. The experimental results show that the dislocation density in the top Ge and GaAs layers can be greatly reduced, and the surface was kept very smooth after growth, while the total thickness of the structure was only 5.1μm (2.6μm SiGe buffer structure + 2.5μm GaAs layer). Besides, the growth of the device quality GaAs epitaxial layers utilizing a novel $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layer on the off-cut Si substrates is reported. It was found that the crystallinity of the GaAs epitaxial layers can be improved using 6^o off-cut Si substrate and the sample grown exhibited ultra-low threading dislocation density. The out-diffusion of Ge into the GaAs epilayer was also successfully suppressed using the 6^o off-cut substrate. The results indicate that device quality GaAs epitaxial layers can be grown on silicon using the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers with 6^o off-cut Si substrates.

3-1 Introduction

The growth of GaAs epitaxial layer on Si substrate has attracted considerable interests due to the potential benefits of integrating GaAs devices with Si circuits on a single chip. Such systems have great potential for future applications such as optoelectronic integrated circuits (OEICs) and eventually system on a chip (SoCs) because GaAs and Si materials complement each other. Solar cell for space application is one example that involves the integration of GaAs semiconductor with Si substrate [1-3]. This technology will also provide low-cost, light-weight, and large-area III-V compound substrates with high mechanical strength and excellent thermal conductivity. However, there are two major problems in obtaining high-quality III-V films on Si. One is high density dislocation generation due to large difference of their lattice constants, and another is residual stress due to the large difference in their thermal expansion coefficients. In order to grow high-quality GaAs films on Si, the Ge layer can be used as a buffer, because Ge and GaAs have the similar lattice constants and thermal expansion coefficients.

However, the remaining problem is how to grow high-quality Ge layer on Si, because Ge has a 4.2% lattice mismatch with Si. Various growth techniques and treatments have been developed to solve this problem. It has been reported that the compositionally graded buffer (CGB) layers [4], low-temperature Si buffer layers [5], compliant silicon-on-insulator (SOI) substrate [6], two-step procedure [7], and selective area growth combined with thermal cycle annealing can be used to grow high-quality strain-relaxed SiGe and Ge layers [8]. Among them, the CGB layers are the most practically and widely used ones today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer from a thickness of approximately 10 μm with a Ge composition ranging from zero to 1.0, which makes the integration of devices on the Si-based circuits difficult. Second, the CGB layers often exhibit a cross-hatch pattern, which makes the surfaces very rough [9], and the chemical mechanical polishing (CMP) technique has to be employed to solve this problem.

The formation of antiphase domains (APD) also makes the growth of GaAs on Si difficult. Various methods are tried with most of the work were done with Si wafers which have misoriented from the (100) orientation by a few degrees [10,11]. Yuan Li et al. presented a model which based on a concept that the sublattice location for polar material grown on nonpolar material is defined by the relative intensity of nucleation at the steps and on the terraces between the steps is proposed to explain the APD formation [10]. The possible final growth of the GaAs epilayer on Ge (100) off towards (111) is shown schematically in Fig. 3.5. Therefore, the off-cut angle substrate is adapted to reduced APD formation in this work. Additionally, the inter-diffusion across the GaAs/Ge interface that occurs during epitaxial growth is important because it affects the control of the doping profile in GaAs. Several approaches have been proposed to suppress the Ge inter-diffusion, as reported in Refs [11,12].

In this chapter, we report a new approach to obtaining a high-quality Ge layer, and then report growth of high-quality GaAs on this Ge buffer. The procedure for the growth of Ge mainly involves growing three epitaxial layers (see Fig.2.6). The first layer is the $Si_{0.1}Ge_{0.9}$ layer, the second is the $Si_{0.05}Ge_{0.95}$ layer, and the third is the Ge layer. After the growth of each individual layer, *in situ* 750^{o}C annealing for 15 min was performed. Due to the large lattice mismatch at the interface between $Si_{0.1}Ge_{0.9}$ and Si layers, many close small islands are formed during growth at low temperatures. As growth proceeded, these islands quickly coalesced into a continuous film. At the same time, many dislocations generated and interacted with each other to form closed nonpropagating loops and networks near the interface. A small portion of the dislocations that did not have the chance to pair up continued to propagate upward. A similar technique has been widely used in growing highly mismatched heterostructures, for example, GaN on Sapphire [13]. Due to the proper lattice mismatch strains at the upper interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$, the upward-propagated dislocations can be bent sideward and terminated effectively. Details of the behavior of dislocations at the mismatched interfaces can be seen in references 14 and 15.

Additionally, the thermal annealing process, which was performed after growing each individual layer, can further reduce dislocation density in the epitaxial layers. The mechanism of the threading dislocation reduction employed in this work is shown schematically in Fig. 2.6. The improvements of the GaAs crystallinity on off-cuts Si substrates were investigated. The inter-diffusion and optical characteristics of the GaAs samples grown on different off-cut Si substrates were studied. Secondary ion mass spectroscopy (SIMS), X-ray diffraction (XRD), transmission electron microscopy (TEM) analysis, and PL measurements were performed to elucidate the structural and optical characteristics of the off-cut GaAs/Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si samples.

3-2 GaAs epitaxial layer growth procedures

The growth of the SiGe and Ge layers was carried out using an ultra-high vacuum chemical vapor deposition (UHV/CVD) system with a base pressure of less than 2×10^{-8} Torr [16]. First, a 4-inch Si(100) substrate wafer with a 6^{o} off-cut toward the [110] direction was cleaned by 10% HF dipping and high-temperature baking at 800^{o}C in the growth chamber for 5 min. Then, a 0.8 μm $Si_{0.1}Ge_{0.9}$, a 0.8 μm $Si_{0.05}Ge_{0.95}$, and a 1.0 μm Ge layer were grown at 400^{o}C in sequence. The growth rate of Ge layer was 0.8 μm/hour. Between successive layers, growth was interrupted for an *in situ* 15 min 750^{o}C annealing. GaAs layers were grown by a commercial metal organic chemical vapor deposition (MOCVD) system on the grown Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ buffer structure at a temperature of 600^{o}C by one step. The growth conditions of GaAs are as follows: growth pressure was 40 torr, Ⅴ/Ⅲ ratio was 100 and growth rate was 1.7 μm/hour. Transmission electron microscopy (TEM) was used to observe the thickness of the epitaxial layers and the dislocation distribution, and to estimate the threading dislocation density. The Ge surface morphology was analyzed by Nanoscope III atomic force microscopy (AFM) in the contact mode. The x-ray diffraction and photoluminescence (PL) were additionally used to evaluate the crystalline quality of the

sample. SIMS analysis was used to investigate the Ge cross-diffusion in this study.

3-3 Material characteristics of the GaAs epilayer on the off-cut Ge/GeSi/Si

In our previously investigation, the quality of the Ge/GeSi buffer structure was excellent and can be used as high quality virtual substrate to growth high-quality GaAs epilayer on Si substrate. Figure 2.7 shows the cross-sectional TEM image of the Ge/GeSi buffer structure. There are a large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. The upward propagated dislocations were bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ and Ge/ $Si_{0.05}Ge_{0.95}$ interfaces. Almost no threading dislocation can propagate into the top Ge layer. The image shows that the total thickness of these three epitaxial layers is only approximately 2.6 μm, which is much smaller than that of CGB layers reported earlier. By analyzing several plan-view TEM images, the threading dislocation density is estimated to be about $3\times10^{6}cm^{-2}$. In this study, the Ge composition variation at the two strained interfaces is set at 0.05. We found that if the Ge composition variation is too large, new dislocations will generate from the interfaces due to the relatively large lattice mismatch [17]. On the contrary, if the Ge composition variation is too small, the mismatch stress formed at the interfaces is not strong enough to terminate the dislocations effectively.

The surface roughness was measured by AFM. Figure 3.1 presents the AFM images of the surfaces of the (a) Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ sample and (b) GaAs/ Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ sample, respectively. No cross-hatching pattern on both Ge and GaAs surfaces were observed. The root mean square (RMS) of the Ge surface is only 32 Å, which is much smaller than that of the CGB layers (about 180 Å) reported by reference 18. The RMS of surface for GaAs/ Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ sample is 61.2 Å, in comparison with RMS of 11.3 Å for the surface of GaAs/ GaAs sample.

Figure 3.2 shows the cross-sectional TEM (XTEM) image of the GaAs layer grown on the Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ buffer structure by MOCVD at 600°C. The thickness of the GaAs layer was about 2.5μm. It can be seen that the dislocation density in the GaAs layer appears to be greatly reduced in comparison with the sample of GaAs grown directly on Si as reported in earlier, where the dislocation density is high [19]. Additionally, due to the 0.01% lattice mismatch still existed between GaAs and Ge, a weak strain field at the GaAs/ Ge interface is induced. The XTEM image also clearly shows this strain field at the GaAs/ Ge interface.

The crystallinity of the GaAs epitaxial layers on Si strongly affects the performance of the GaAs devices. In this study, 0^o, 4^o and 6^o off-cut Si substrates were used in order to examine whether the off-cut buffer layers can effectively improves the GaAs crystallinity on Si. XRD analysis was used to determine the crystallinity of the GaAs epilayers. Figure 3.3 (a) presents the XRD spectra of 2.1 μ m-thick GaAs epilayer grown on the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$buffer with an 6^o off-cut Si substrate. The XRD spectrum includes nine main peaks as follows; (400) Si, θ =34.7°, (400) GaAs, θ =33.15°, (400) $Ge_{0.95}Si_{0.05}$+(400) $Ge_{0.90}Si_{0.10}$, θ =33.09°, Ge, θ =33.0° ,(400) Si, θ =30.8°, Ge, θ =29.9°, (501) Ge, θ =22.5°, (200) GaAs, θ =15.8° and (220) Ge, θ =10.27°. These diffraction angles completely match the values calculated from the equation by Bragg's law. The intensity of the (400) GaAs diffraction peak is 5.7×10^5 cps which exceeds that of the (400) Si diffraction peak. The width at half maximum (FWHM) of the (400) GaAs peak is only 0.172 degree. While, the intensity of the (400) GaAs peak obtained from the 4^o and 0^o off-cut samples was 3.7×10^4 and 2.1×10^4 cps, respectively. The FWHM of the (400) GaAs peaks calculated from the 4^o and 0^o off-cut samples were 0.212 and 0.301 degree, respectively, as shown in Fig. 3.3 (b). These results clearly reveal that the crystal quality of the GaAs epitaxial layer grown on Si, using the novel Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ buffer layer with an 6^o off-cut Si substrate, is superior to those grown with 4^o and 0^o off-cut Si.

The low-temperature PL measurements were performed to further characterize the crystallinity of the GaAs epilayer grown on the off-cut Si substrates using the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers. Figure 3.4 plots the results obtained from the 13K PL spectra of the various off-cut samples. The GaAs epilayer grown on GaAs substrate is also shown for comparison. The GaAs/GaAs sample is designated as A, and samples with 6^o, 4^o, and 0^o off-cut are denoted as B, C and D in Fig. 3.4(a), respectively. In the PL spectra, peak A at 1.504 eV is associated with the separation of light holes, the peaks at 1.488eV and 1.486 indicated as B and C, respectively, are related to the separation of heavy holes in the valence band caused by the deformation of the band [20]. Peak D at 1.472 eV is considered to be corresponding to a neutral-carbon-related free-to-bound (FB) recombination, attributable to the dominant residual impurities acting as acceptors in GaAs [21]. It can be seen that, the FWHMs of peaks B and C are 32 and 33meV and are near to that of the GaAs/GaAs reference sample (28meV), while that of peak D is 47meV, as shown in Fig. 3.4(b). The PL intensity of the 6^o off-cut sample exceeds that of the 4^o and 0^o off-cut samples, as also shown in Fig. 3.4(b). These results imply that the GaAs epilayer on Si with the 6^o off-cut Si substrate has better crystalline quality and optical characteristics than the other samples.

TEM was used to elucidate the distribution of the dislocations, and to determine the threading dislocation density (TDD) in the epitaxial layers grown. Figures 3.6(a) and 3.6(b) show the cross-sectional TEM (XTEM) images of 0^o and 4^o off-cut samples, respectively. From the TEM observations, the 0^o and 4^o off-cut samples exhibited more TDDs in the GaAs epitaxial layers than the 6^o off-cut samples, although several threading dislocations were blocked at the GaAs/Ge interface. For the sample with 6^o off-cut $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrate, the surface morphology was very smooth and mirror-like, indicating that the magnitude of the off-cut angle can solve the problem of polar semiconductors grown on non-polar substrate in this work [10]. Figure 3.6 (c) presents the XTEM image of the 6^o off-cut sample. Many dislocations located near the $Ge_{0.9}Si_{0.1}/Si$ interface and at the lower part

of the $Ge_{0.9}Si_{0.1}$layer. The upwardly propagating dislocations were bent sideward and were terminated very effectively by the Ge/$Ge_{0.95}Si_{0.05}$ and $Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ interfaces. The TDD in the Ge layer was greatly reduced. Almost no new dislocations were observed at the GaAs/Ge interface, indicating that the TDD in GaAs epitaxial layer should be in the order of 10^6 cm^{-2}, the value of the TDD in the Ge layers grown on Si with $Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ buffer layer was reported in our earlier paper. The atomic force microscopy (AFM) measurements also showed that the 4^o and 0^o off-cut samples have poorer surface morphologies than the 6^o off-cut sample.

3-4 Analysis of Ge inter-diffusion in GaAs/Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si

The suppression of atomic inter-diffusion across the heterostructure is a key challenge in increasing yield, performance and reliability of the device processed based on the heterostructure. This is a major issue that influences the GaAs buffer layer in devices such as solar cells [22] and is important in applications such as forming junctions, and controlling doping profiles. SIMS analysis was used to detect possible Ge, Ga, and As inter-diffusion in the GaAs/Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si system in this study. Figures 3.7(a), 3.7(b) and 3.7(c) show the SIMS depth profiles obtained for Ge in GaAs, As and Ga in Ge for the various off-cut samples. Ge atom inter-diffused markedly for the 0^o and the 4^o off-cut samples as shown in Figs. 3.7(a) and 3.7(b). During 600℃ epitaxial growth, Ge out-diffusion depths in the 4^o and the 0^o off-cut samples were 0.55 and 0.83 μm, respectively. Figure 3.7(c) shows the depth profiles for the 6^o off-cut sample. The suppression of the out-diffusion of Ge atom was remarkable for sample with the 6^o off-cut Si substrate and the GaAs/Ge interface was quite abrupt. However, the diffusion of Ga and As atoms into the Ge layer is not evident for all the samples under study. Two reasons may explain why the 6^o off-cut sample showed suppressed Ge out-diffusion. First, the surface morphology of 6^o off-cut Ge buffer layer is smoother than those of the 4^o and the 0^o off-cut samples. Second, the TDD of the 6^o off-cut

GaAs sample is less than those of the 4^o and the 0^o off-cut samples, which resulted in less diffusion paths for the Ge atoms.

3-5 Conclusions

We have designed a novel SiGe buffer structure for growth of high-quality GaAs on Si substrates. The method mainly involves: (1) growth of three layers consisting of a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer, a 0.8 μm $Si_{0.05}Ge_{0.95}$ layer, and a 1.0 μm top Ge layer, and (2) *in situ* 750^oC annealing for 15 min performed on each individual layer. By this procedure, many dislocations were formed at the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. Moreover, the upwardly propagated dislocations can be bent and terminated effectively by the interfaces of $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ and Ge/ $Si_{0.05}Ge_{0.95}$. The top Ge layer exhibits a low threading dislocation density and a smooth surface. Finally, using this Ge layer as a buffer, we have grown a high-quality GaAs layer on the Si(100) substrate with a 6^o off-cut toward the [110] direction.

The improvement of the crystallinity of the GaAs was demonstrated by using the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layer grown on 6^o off-cut Si substrate. It is shown that the GaAs epitaxial layers grown by this approach is exhibit ultra-low threading dislocation densities. The suppression of Ge inter-diffusion into GaAs epilayers was also succeeded using the 6^o off-cut Si substrate. The use of the proposed $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layer grown on the 6^o off-cut substrates is demonstrated to be very practical for growing device-quality GaAs epilayers on Si substrates and the technology is very promising for the manufacturing of the OEICs in the future.

3-6 References

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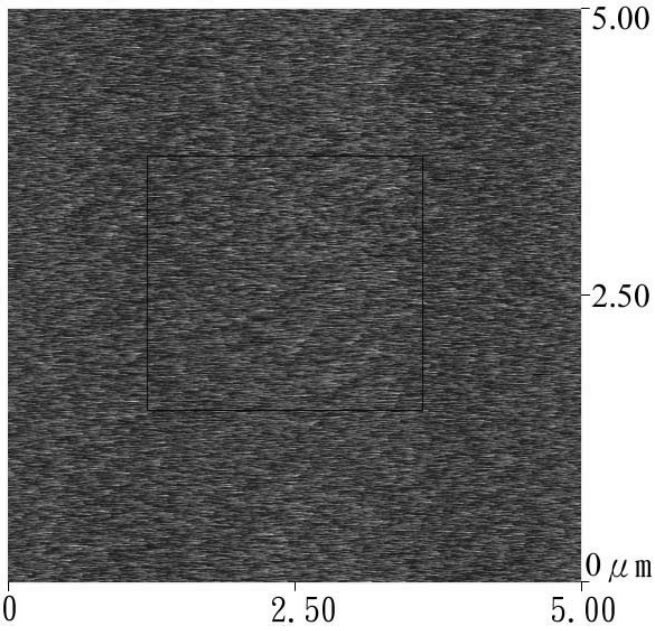
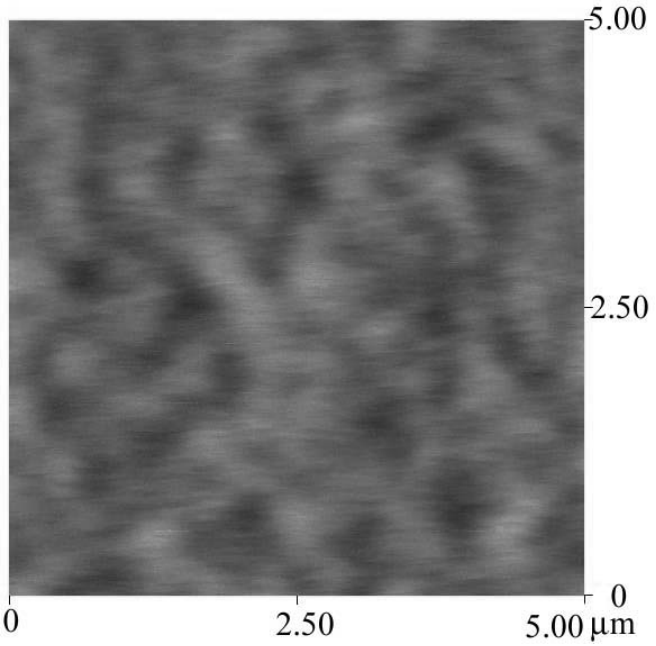


(a)



(b)

Fig. 3.1 The AFM images of the surfaces of the (a) Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ sample and (b) GaAs/ Ge/ $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ sample, respectively.

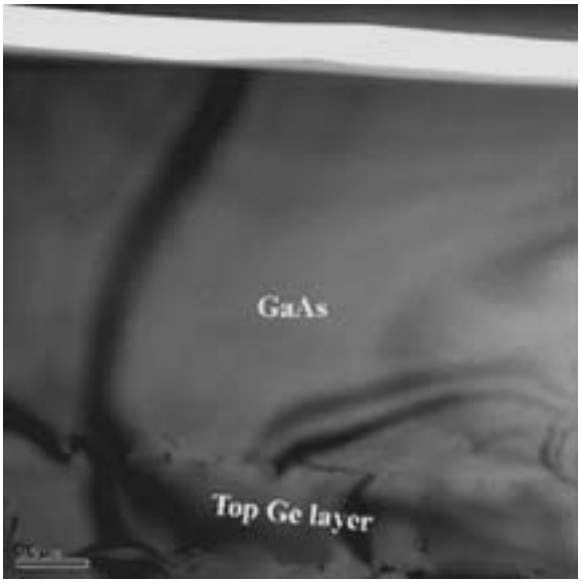


Fig. 3.2 The 2.5 μ m GaAs layer grown by MOCVD on the SiGe buffer structure.

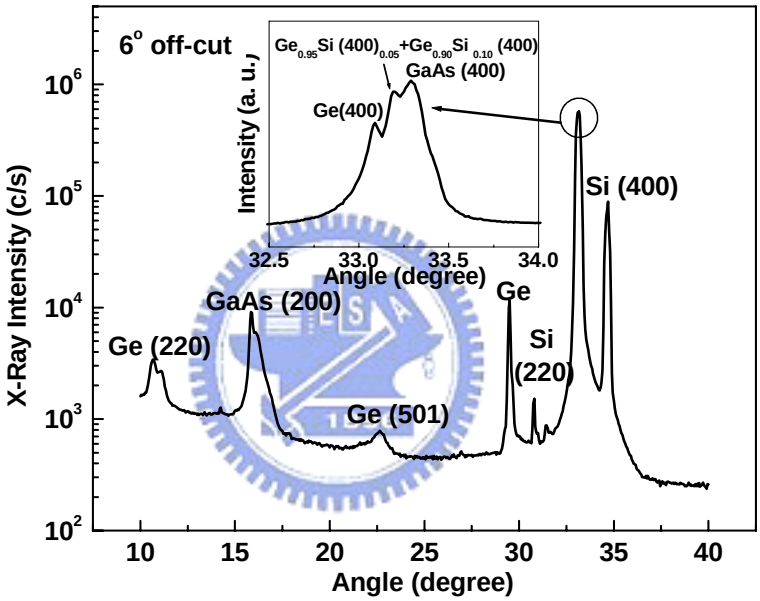


Fig.3.3 (a) XRD spectram of GaAs grown on 6^{o} off-cut Si substrate utilizing the novel $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers

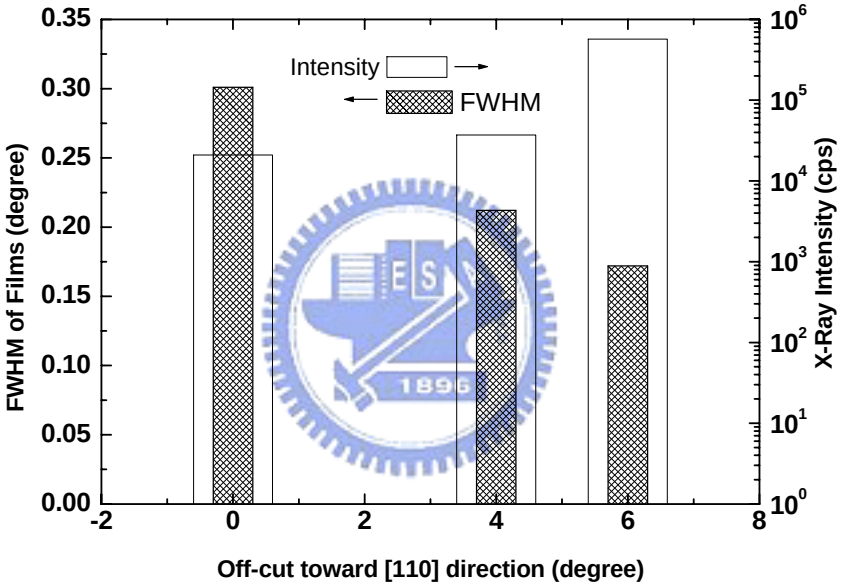


Fig. 3.3 (b) Intensity and FWHM column graph of 6^{o}, 4^{o} and 0^{o} off-cut samples.

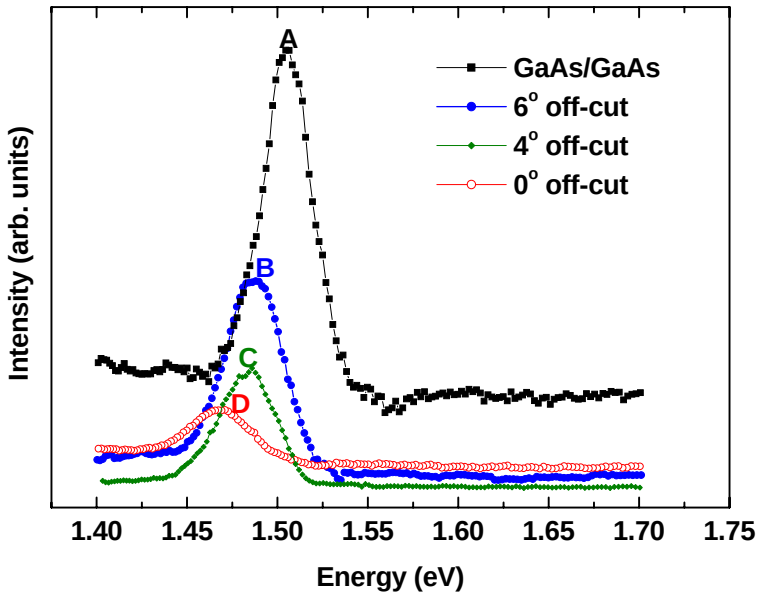


Fig. 3.4 (a) The photoluminescence spectra of GaAs/GaAs, 6^{o}, 4^{o} and 0^{o} offcut samples.

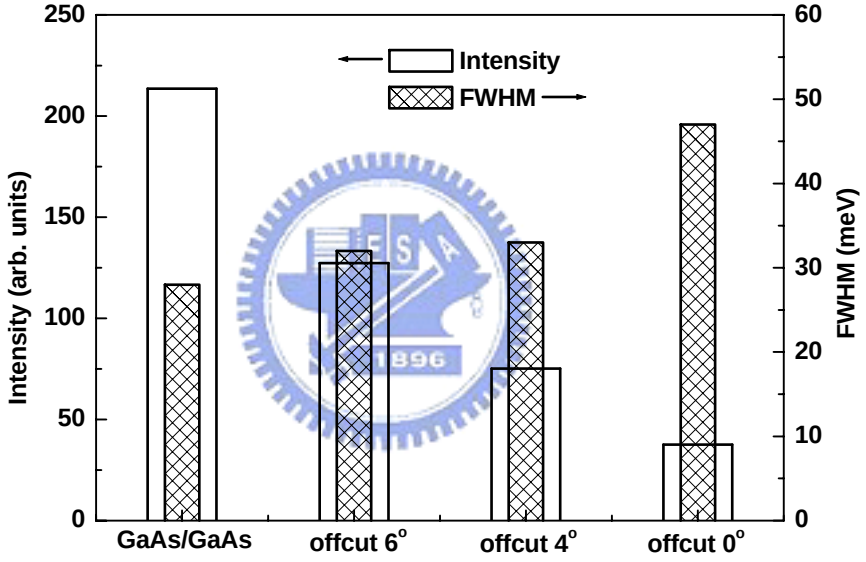


Fig. 3.4 (b) Intensity and FWHM column graph of GaAs/GaAs, 6^{o}, 4^{o} and 0^{o} offcut samples.

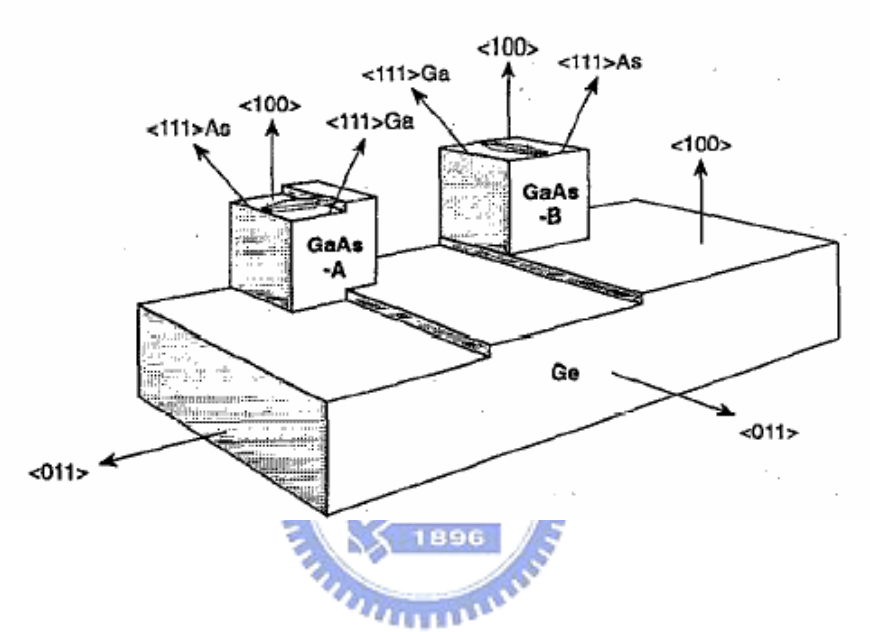


Fig. 3.5 The two possible sublattice locations of Ga and As atoms in GaAs grown on a Ge (100) substrate. Here domain GaAs-A, with its [011¯] orientation perpendicular to the surface steps, corresponds to the case that the first atomic layer on the Ge surface is as, while GaAs-B, with its [011¯] orientation parallel with the surface steps, represents the situation that the first atomic layer on the Ge surface is Ga, based on the double step model of the Ge (100) surface and the simple layer-by-layer growth mechanism.

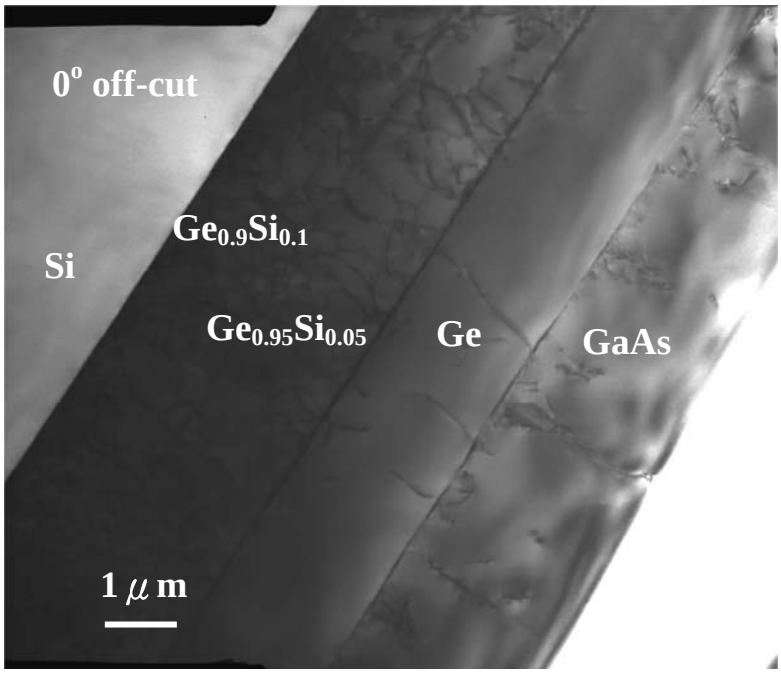


Fig. 3.6 (a) The XTEM image of the GaAs epilayers grown on 0^o Si substrates utilizing the novel $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers.

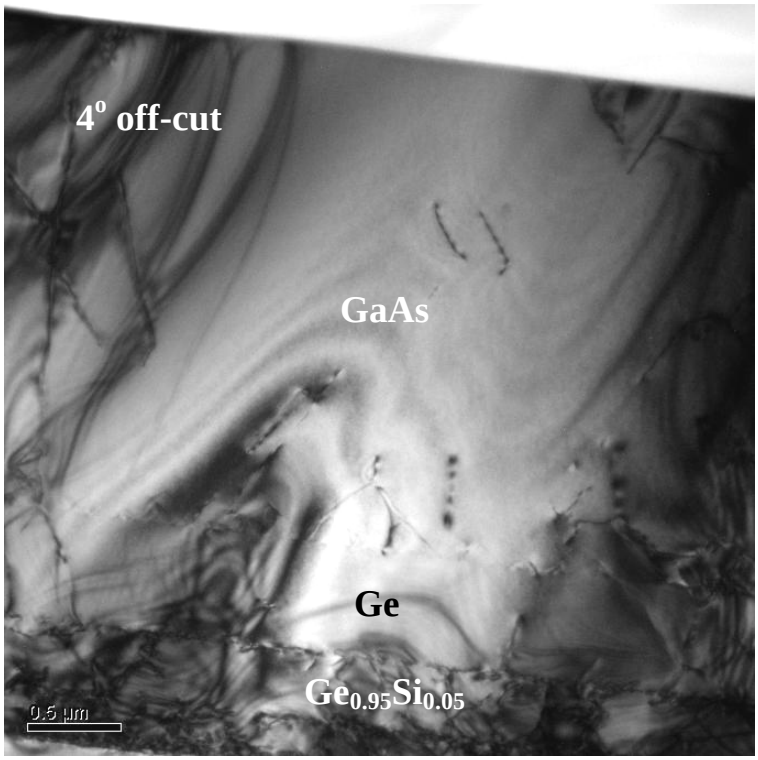


Fig. 3.6 (b) The XTEM image of the GaAs epilayers grown on 4^{o} Si substrates utilizing the novel $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers.

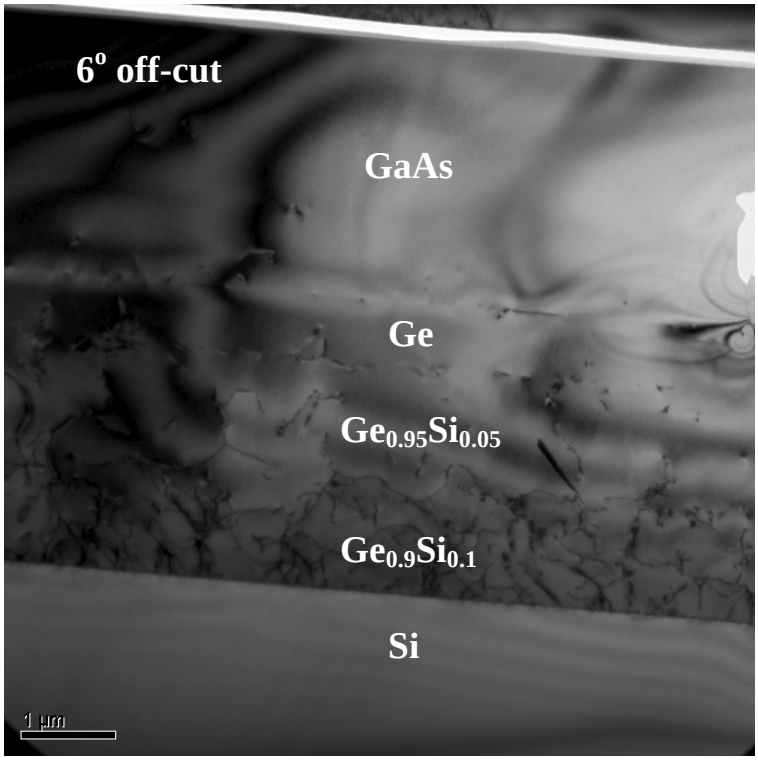


Fig. 3.6 (c) The XTEM image of the GaAs epilayers grown on 6^{o} Si substrates utilizing the novel $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers.

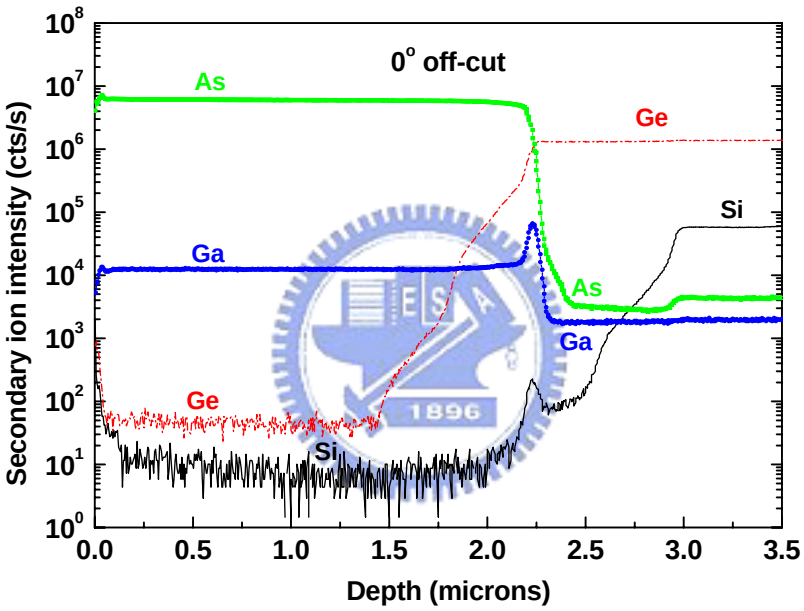


Fig. 3.7 (a) The SIMS profile of Ge, As and Ga in GaAs layer grown on 0^{o} $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrates.

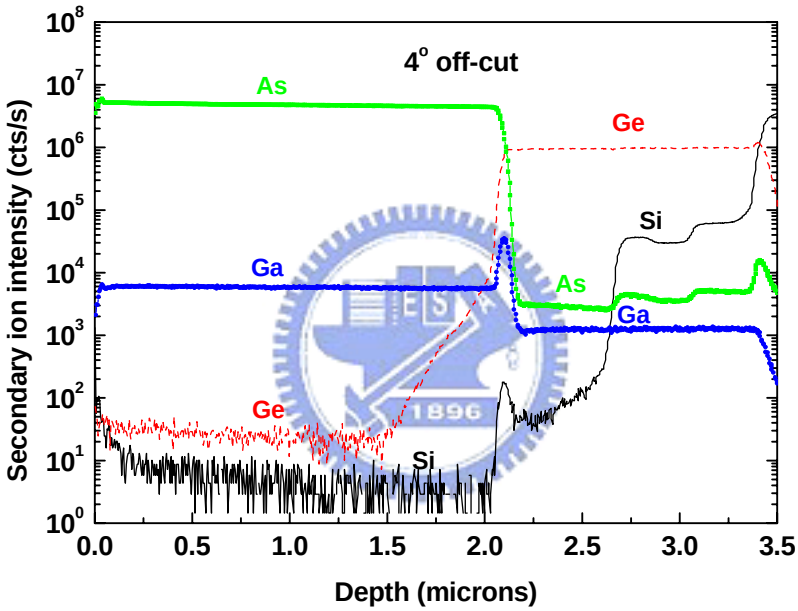


Fig. 3.7 (b) The SIMS profile of Ge, As and Ga in GaAs layer grown on 4° Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si substrates.

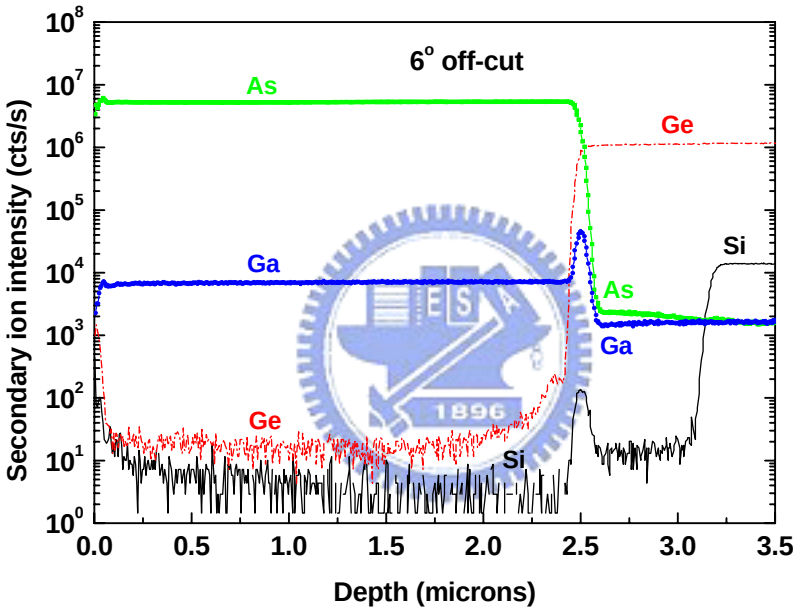


Fig. 3.7 (c) The SIMS profile of Ge, As and Ga in GaAs layer grown on 6° Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si substrates.