CHAPTER 4

Growth of ZnSe epilayer on Si substrate using Ge/Ge_xSi_{1-x} buffer structure

In this chapter the epitaxial growth of ZnSe layers on Si substrates utilizing a Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ buffer structure is presented. In this study, we examine the structure, optical characteristics and atomic interdiffusion of the ZnSe epilayer grown on Si. In a sample with large off-cut angle Si substrate, the outdiffusion of Ge into the ZnSe epilayer is suppressed. The low-temperature PL measurements indicate that the sample with large off-cut angle Si substrate has improveed its optical characteristics. The X-ray diffraction analysis and transmission electron microscopy (TEM) results also indicate that the use of a large off-cut angle Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si substrate markedly improves the crystallinity of ZnSe epilayer and reduced the number of threading dislocations in ZnSe grown on Si. The method of low substrate temperature MEE and buffer layer growth with *in-situ* annealing has demonstrated to suppress the formation of the deep-level emission (DLE) in the ZnSe/Ge/Ge_xSi_{1-x} structure effectively.

4-1 Introduction

In recent years, ZnSe epilayers have been used extensively in optoelectronics [1] and light-emitting diode (LED) [2] applications. Presently, ZnSe is grown on GaAs and Ge substrates because it is almost lattice-matched to these materials [3]. However these substrates are very expensive and highly brittle. If high-quality ZnSe epilayers can be grown on Si substrates, these drawbacks can be overcome and the integration of ZnSe devices with Si circuits on a single chip can be realized. However, the mismatch between the lattice constants of ZnSe and Si is 4.3%, which generates high densities of dislocations on heteroepitaxial ZnSe/Si directly. The large difference in thermal expansion coefficient between these two materials also makes the growth of ZnSe on Si difficult. The formation of antiphase boundary

(APB) in GaAs/Si system, which is expected to provide deep levels inside the forbidden band and to act as strong scattering centers [16,17], this effect also in ZnSe/Si system. The phenomenon of APD is due to the growth of polar materials on nonpolar materials, two equivalent orientations corresponding to a difference in the location of cation atoms and anion atoms in the two sublattices can be expected in the epilayer. Domains of different sublattice location are separated by an antiphase boundary (APB). Various methods have been proposed to improve the crystallinity of ZnSe grown directly on Si substrates [4-6]. A high growth temperature improves the quality of epilayers since it increases step-flow growth through an increase in surface migration length [7]. However, a high growth temperature also inherently enhances atomic interdiffusion in heteroepitaxy [8]. Therefore, a low growth temperature is usually preferred in order to prevent atomic interdiffusion. In the ZnSe/GaAs heteroepitaxy, the Ga-Se or Zn-As bonds formed at the interface due to the atomic interdiffusion may induce an excess or a deficiency of electrons. Several approaches have been used to suppress the atomic interdiffusion as reported in refs.9 and 10. Similarly, interdiffusion across the ZnSe/Ge interface that occurs during epitaxial growth is also important because it affects impurity level in the epilayers. In this investigation, the growth of high-quality ZnSe epilayers on Si substrates using the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layer developed by the authors is realized [11]. The improvement in crystallinity and the effects of the interdiffusion and optical characteristics of the ZnSe epilayers on off-cut Si substrates were investigated in this study. The method of low substrate temperature MEE and buffer layer growth with *in-situ* annealing can suppress the formation of the deep-level emission (DLE) in the off-cut angle $ZnSe/Ge/Ge_xSi_{1-x}$ structure effectively is also demonstrated. Secondary ion mass spectroscopy (SIMS), X-ray diffraction (XRD) analysis, transmission electron microscopy (TEM) and PL measurements were performed to elucidate the morphological, structural and optical characteristics of the $ZnSe/Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ samples.

4-2 ZnSe epitaxial layer growth procedures

The growth of the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$ buffer layers was carried out using an ultrahigh vacuum chemical vapor deposition (UHV/CVD) system at a base pressure of less than 2×10^{-8} Torr [11]. In this study, a 4" *p*-Si (100) substrate and a *p*-Si substrate (100)-oriented with a off-cut toward the in-plane [110] direction were used. First, the Si substrates were cleaned by 10% HF dipping. After that, high-temperature baking at 800℃ in the growth chamber was performed for 10 min. Then, a 0.8 μm $Ge_{0.9}Si_{0.1}$, a 0.8 μm $Ge_{0.95}Si_{0.05}$ and a 1.0 μm Ge layer were grown at 400℃ on the substrate in sequence. Between successive layers, growth was interrupted by an *in-situ* 750℃ 15 min annealing. ZnSe epilayers were grown on the Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si substrates using the Veeco-Applied-EPI 620 molecular beam epitaxy (MBE) system. The solid sources of Zn (6N) and Se (6N) were used for the growth. The cell temperatures of Zn and Se were 300 and 175 ℃, respectively. The substrate surface temperature was controlled at 250-350℃ throughout the growth process. The low substrate temperature MEE and buffer layer growth with *in-situ* annealing method includes: Zn prelayer to initiate migration enhance epitaxy (MEE) and buffer layer were grown at 250℃ in sequence then *in-situ* annealing at 400℃ for 10mins in the high vacuum. The mechanism of the low substrate temperature MEE and buffer layer growth with *in-situ* annealing method employed in this work is shown schematically in Fig. 4.1.6. SIMS analysis was used to investigate atomic interdiffusion. Epilayer quality was verified using XRD analysis. TEM was used to observe the dislocation distribution and estimate threading dislocation density. Low-temperature PL measurements were performed at 13 K using a closed-cycle refrigerator to determine crystal quality.

4-3 Analysis of Ge inter-diffusion in ZnSe/Ge/$Ge_{0.95}Si_{0.05}$/$Ge_{0.9}Si_{0.1}$/Si

The suppression of atomic interdiffusion across the ZnSe/Ge heterostructure is a key challenge in increasing the yield, and improving the performance and reliability of this

structure for future device applications. The SIMS depth profiles of the heteroepitaxial $ZnSe/Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ heterostructure were taken to examine whether the use of an off-cut Si substrate can effectively suppress the diffusion of Ge, Zn and Se into the heterostructure. Figure 4.1 shows the SIMS depth profiles of Ge, Zn and Se in the $ZnSe/Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ heterostructure with (a) 0° and (b) 2° off-cut Si substrates. Ge atoms diffused markedly into the heterointerface for the 0° off-cut sample as shown in Fig. 4.1(a). For the 0° off-cut sample, the Ge outdiffusion depth was 0.22 μm and the Ge concentration was approximately 1×10^{20} atoms/cm^{-3}. For the 2° off-cut sample, Ge concentration decreases abruptly at the heterointerface, clearly indicateing that the interdiffusion of Ge into the ZnSe epilayer is suppressed using the 2° off-cut Si substrate. The diffusion of Zn and Se into the Ge buffer layer is not evident in all the samples.

4-4 Optical characteristics of the ZnSe epilayers grown on Ge/GeSi/Si system

The crystal quality and optical characteristics of the ZnSe epilayers grown on Si can be examined by low-temperature PL measurements. Figure 4.2 (a) shows the PL spectra measured at 13 K for the (a) 2° and (b) 0° off-cut Si substrates. These samples with Zn atoms to initiate the MEE growth at 350℃. The narrowest and most intense PL peak at approximately 2.800 eV is compared with that observed for the high-quality ZnSe epilayers grown on GaAs substrates in our previous investigation [12]. This peak includes an impurity-bound exciton (X/I) and free-exciton (FX) emission [12,13]. At 2.770 eV, a weak peak was found to indicate the donor to valence band recombination [12,14]. Another peak at approximately 2.600 eV, called the Y_0 line, is associated with misfit dislocations [10,12]. Finally, the peak in the range from 2.500 to 2.000 eV corresponds to deep-level emission (DLE) [15], which is weak in the 2° off-cut sample, while it is appreciable in the 0° off-cut sample. In ref. 15, the authors suggested that the origin of DLE is defects such as Zn

vacancies. According to SIMS and PL results, Ge-interdiffusion-induced Zn vacancies may be suppressed by the use of 2° off-cut Si substrates. Comparing spectrum (a) with spectrum (b), it was found that FX vanished in spectrum (b), while X/I dominated the spectrum, which supports the notion, that the use of a 2° off-cut Si substrate can improve crystal quality effectively.

4-5 Material characteristics of the ZnSe epilayers grown on Ge/GeSi/Si system

The crystallinity of the ZnSe epilayers on the $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrates was examined by X-ray diffraction analysis. Figure 4.3 shows the x-ray diffraction pattern of the ZnSe sample on the 2° off-cut substrate. The diffraction pattern has nine major peaks as follows (400) Si, θ=34.7^o, (400) Ge, θ=33.1^o (400) ZnSe, θ=32.9^o, (220) Si, θ=30.5^o, Ge, θ=29.9^o, (501) Ge, θ=22.5^o, (200) ZnSe, θ=15.7^o, (112) Ge, θ=16.64^o and (220) Ge, θ =10.27^o. These diffraction angles almost coincide with those calculated using the equation of Bragg reflection condition. The intensity and full width at half maximum (FWHM) of the (400) ZnSe diffraction peak are 1.1×10^5 cps and 0.187 degree, respectively. Meanwhile, the intensity of the (400) ZnSe peak obtained from the 0° off-cut sample is 7.2×10^4 cps and the FWHM is 0.320 deg.. This, again, indicates that the crystal quality of the 2° off-cut sample is better than that of the 0° off-cut sample.

TEM was used to determine the distribution of dislocations and estimate threading dislocation density (TDD). The 0° off-cut sample exhibited a higher TDD (1×10^7 cm^{-2}) than the 2° off-cut sample from the TEM observations. The surface of the sample was smooth when a 2° off-cut $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrate was used. A high-resolution TEM lattice image of the top ZnSe epilayer and the bottom Ge buffer layer for the 2° off-cut sample is shown in Fig. 4.4(a). The high-resolution TEM image shows that the ZnSe lattice matches well with the Ge lattice at the heteroepitaxy interface. Additionally, there is no dislocation in

this image. A plan-view TEM image of the 2° off-cut sample is shown in Fig. 4.4 (b). There is no dislocation in this image. By analyzing several plan-view TEM images, the TDD is estimated to be about 3×10^6 cm^{-2}, which is close to the TDD of buffer $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ layers, as reported in Ref. 11.

4-6 Suppression of DLE formation using the method of low temperature MEE and buffer layer growth with *in-situ* annealing

Figure 4.5 shows the PL spectrum of (a) 0°, (b) 4° and (c) 6° off-cut sample with 300℃ initial MEE layers. The formation of DLE in the $ZnSe/Ge/Ge_xSi_{1-x}$ structure reduces with the increase of the off-cut angle of the virtual substrates. This indicates the virtual substrate with higher off-cut angle can suppress the defects, Zn vacancies and atomic interdiffusion effectively. Comparing Fig. 4.2 and Fig. 4.5, it was found that the low substrate temperature MEE growth can suppress the formation of DLE in the $ZnSe/Ge/Ge_xSi_{1-x}$ structure. Hence, the higher off-cut angle virtual substrate and lower MEE growth temperature is needed for suppressing the formation of DLE in the $ZnSe/Ge/Ge_xSi_{1-x}$ structure.

For further suppressing the formation of DLE in the $ZnSe/Ge/Ge_xSi_{1-x}$ structure, the method of low substrate temperature MEE and buffer layer growth with *in-situ* annealing was adopted. The use of Zn prelayer to initiate the MEE can suppress defect, Zn vacancies and interdiffusion in the epilayer was demonstrated as shown in previously discussions. Figure 4.6 (a) shows Zn prelayer to initiate the MEE on the off-cut substrate. Generally at low growth temperature, two-dimensional nucleation is prevailing [18,19]. This means that at low growth temperature nucleation may occur not only at step sides, but also on the terraces between the steps as shown in Fig. 4.6 (b). The nuclei at the steps will thus be surrounded by the nuclei on the terrace so that they are not able to connect with each other. We assume that (i) the initially nucleated ZnSe crystallographic orientation is perpendicular to the step at surface the (ZnSe-A); (ii) the nuclei formed on the terraces have the reversed sublattice location, ZnSe-B.

Low temperature buffer growth on such a surface will have the result that the initially nucleated ZnSe at the surface steps will become less dominant during further growth and at last will completely annihilate, as shown in Fig. 4.6 (c). After that, a *in-situ* annealing at 400 ℃ for 10min was performed for removing of defects that possibly generate in the ZnSe layer grown at low temperature. Finally, growth of ZnSe on such a surface at 300℃, as shown in Fig. 4.6 (d).

Figure 4.1.7 shows the PL spectrum of the 6°off-cut ZnSe samples grown by using (a) high temperature directly growth (b) only initial MEE growth and (c) initial MEE with low temperature buffer growth process. Comparing spectrum (a), (b) and (c), it was apparently found that the method of low substrate temperature MEE and buffer layer growth with *in-situ* annealing can suppress the formation of DLE in the 6° off-cut $ZnSe/Ge/Ge_xSi_{1-x}$ structure.

Figure 4.1.8 shows the PL spectrum of (a) 6°off-cut ZnSe sample grown by using initial MEE with low temperature buffer layer and (b) directly grown ZnSe on GaAs sample. The formation of DLE in the 6° off-cut $ZnSe/Ge/Ge_xSi_{1-x}$ structure is still conspicuous but closing to the peak of ZnSe/GaAs structure, this maybe attribute to the surface morphology of Ge and the dislocation density of the Ge virtual substrate.

4-7 Conclusions

The growth of high-quality ZnSe epilayers on Si substrates using a $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layer was demonstrated. The use of the large off-cut Si substrate improved the crystallinity of the ZnSe epilayer grown and successfully suppressed Ge diffusion into the ZnSe layers. The ZnSe epilayers grown on the large off-cut $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}$ buffer layers also exhibited a low threading dislocation density. The PL spectrum of the large off-cut ZnSe sample shows intense FX with a narrow peak width. These results indicate that the use of the large off-cut Si substrate suppresses interdiffusion through the heterointerface and helps the growth of high-quality layers by reducing

dislocation generation. The method of low substrate temperature MEE and buffer layer growth with *in-situ* annealing to suppress the formation of the deep-level emission in the ZnSe/Ge/Ge_xSi_{1-x} structure was also demonstrated. This technique is very promising for the development of integrating optical and electronic devices in the same chip in the future.

4-8 References

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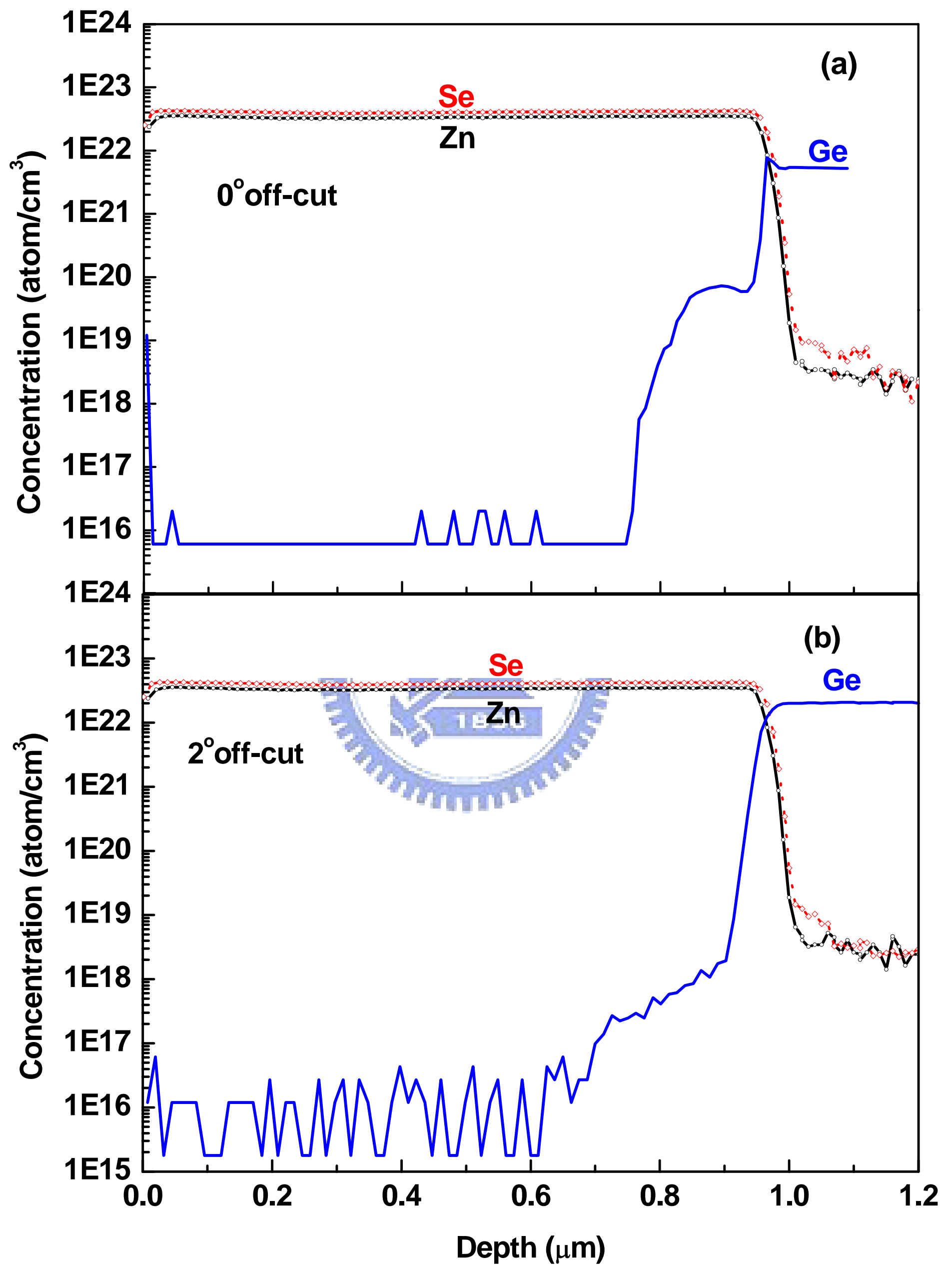


Fig. 4.1 SIMS profiles of Ge, Zn and Se in heteroepitaxial layers grown on (a) 0° and (b) 2° $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrates.

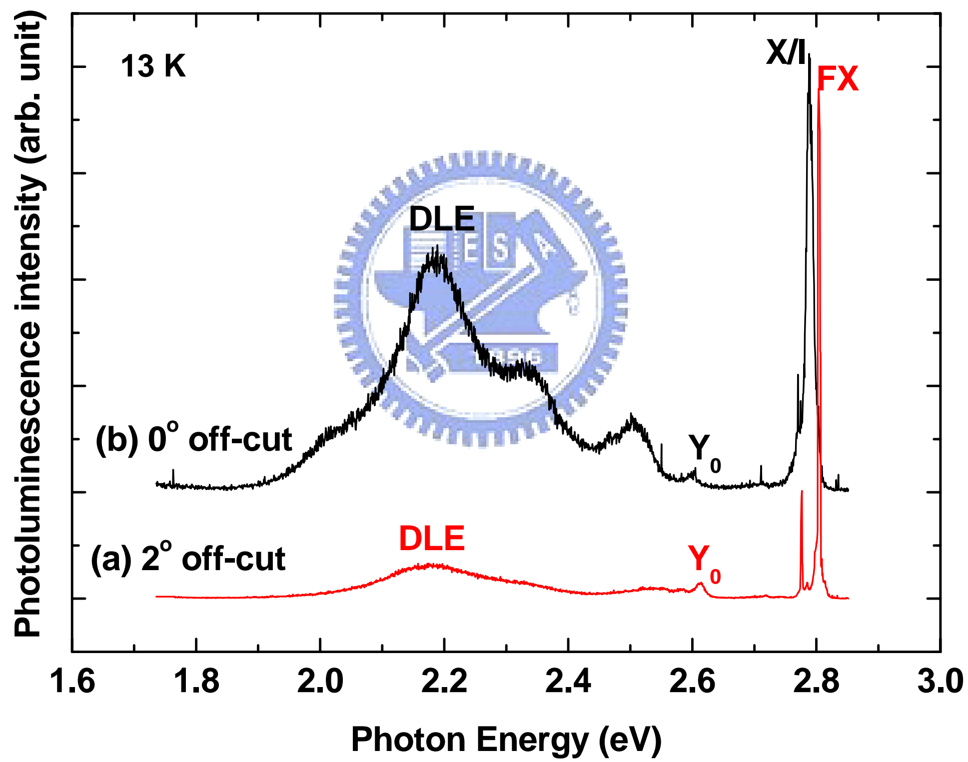


Fig. 4.2 PL spectra of the 1.0-μm-thick ZnSe layer on (a) 2° and (b) 0° off-cut $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrates.

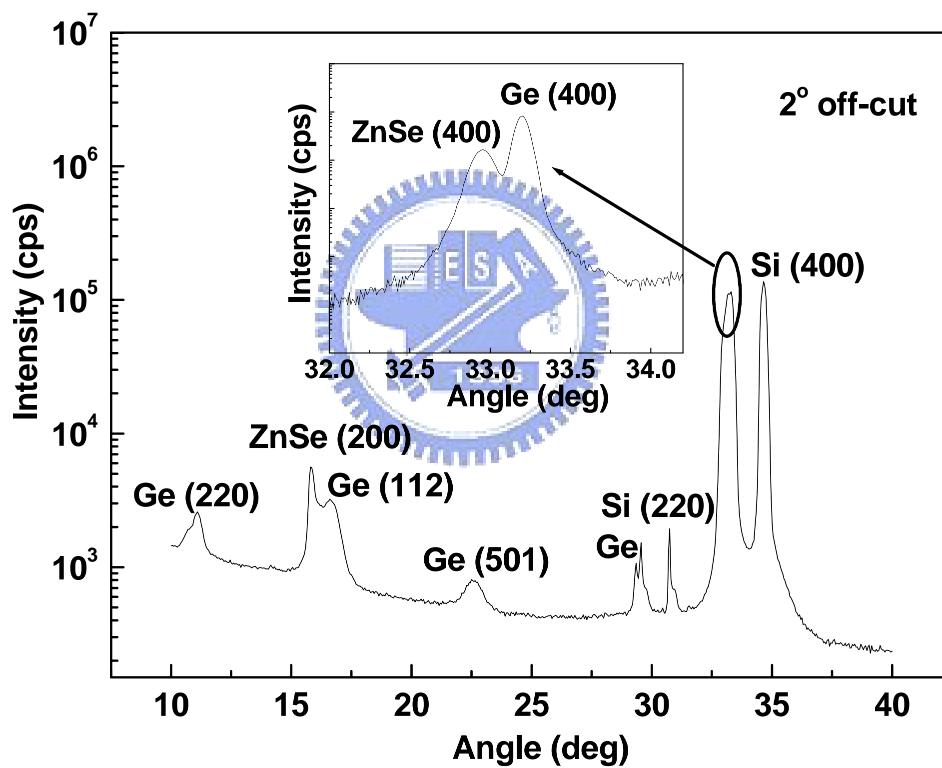
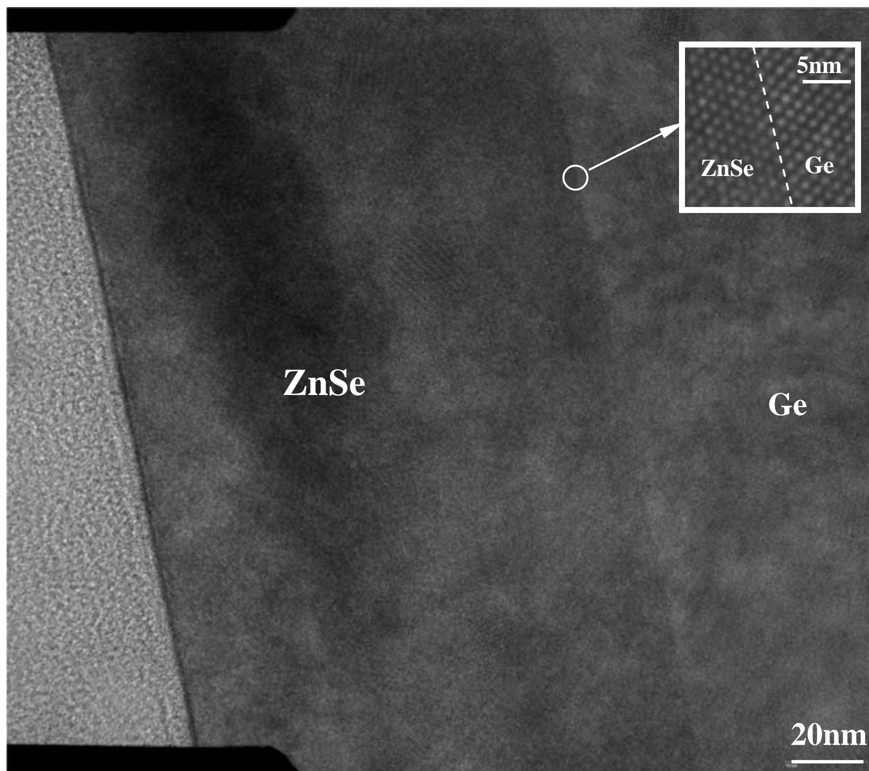


Fig. 4.3 X-ray diffraction pattern of ZnSe on $Ge/Ge_{0.95}Si_{0.05}/Ge_{0.9}Si_{0.1}/Si$ substrate.



(a)

Fig. 4.4 (a) Cross-sectional high-resolution TEM image of ZnSe grown on Si.

(b)

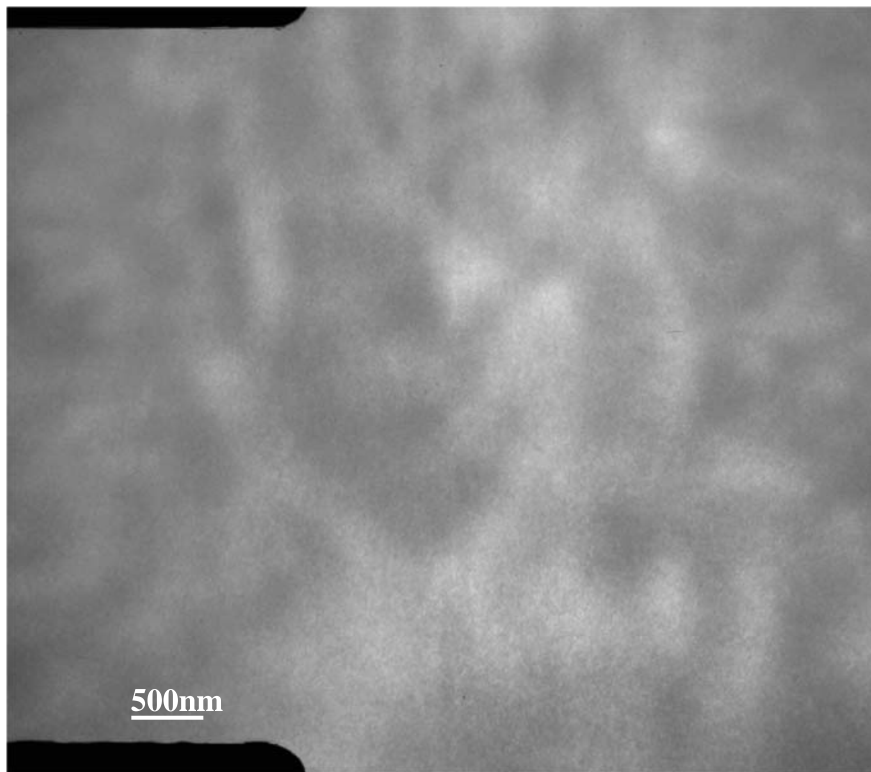


Fig. 4.4 (b) plan-view TEM image of ZnSe grown on Si.

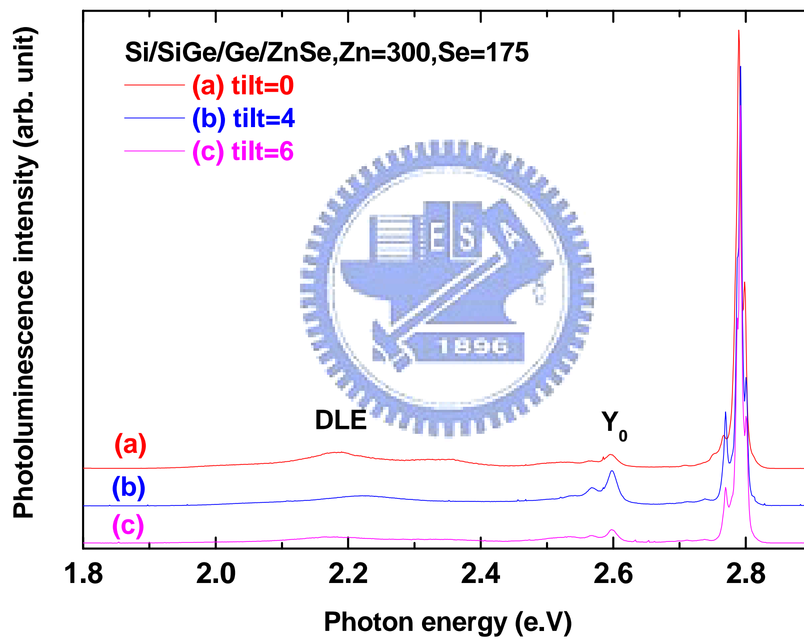


Fig. 4.5 PL spectra of (a) 0°, (b) 4° and (c) 6° off-cut sample with 300℃ initial MEE layers.

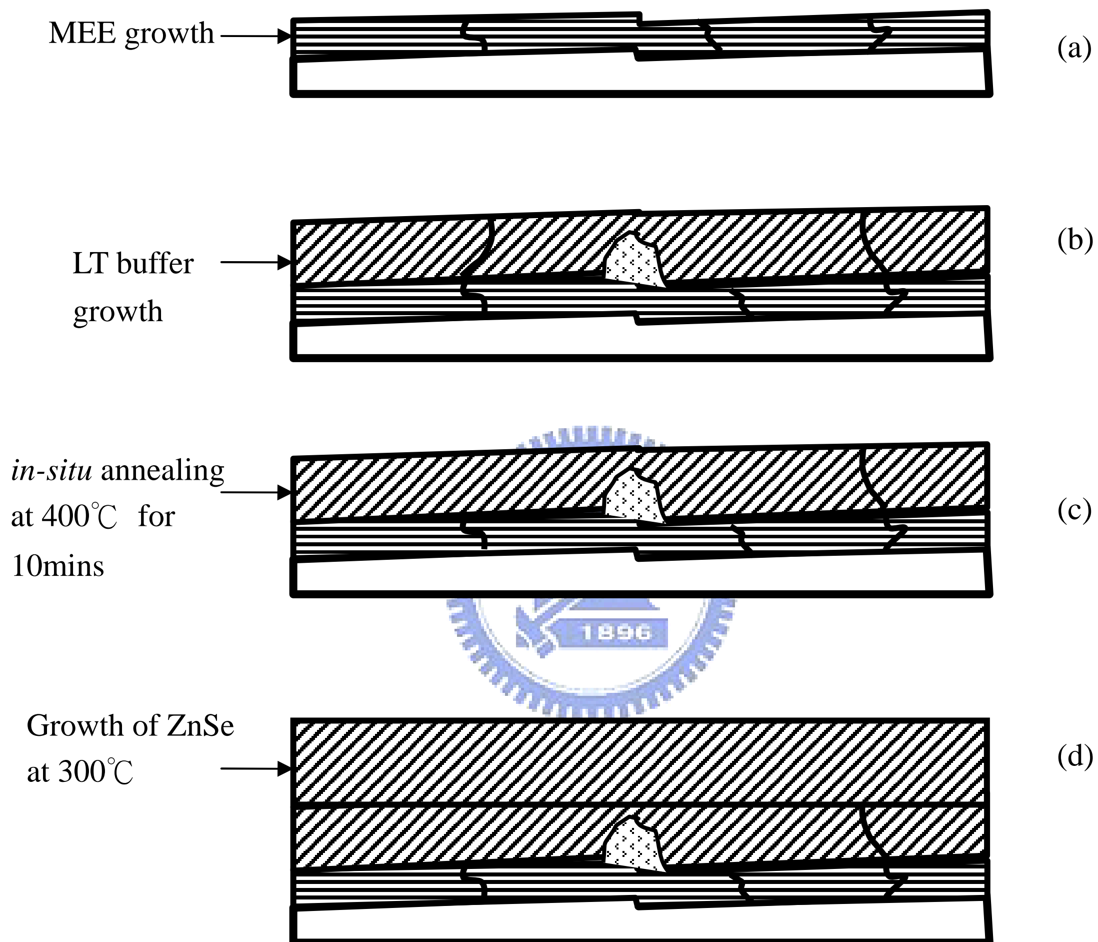


Fig. 4.6 Schematic of the mechanism of the low temperature MEE and buffer layer growth with *in-situ* annealing method.

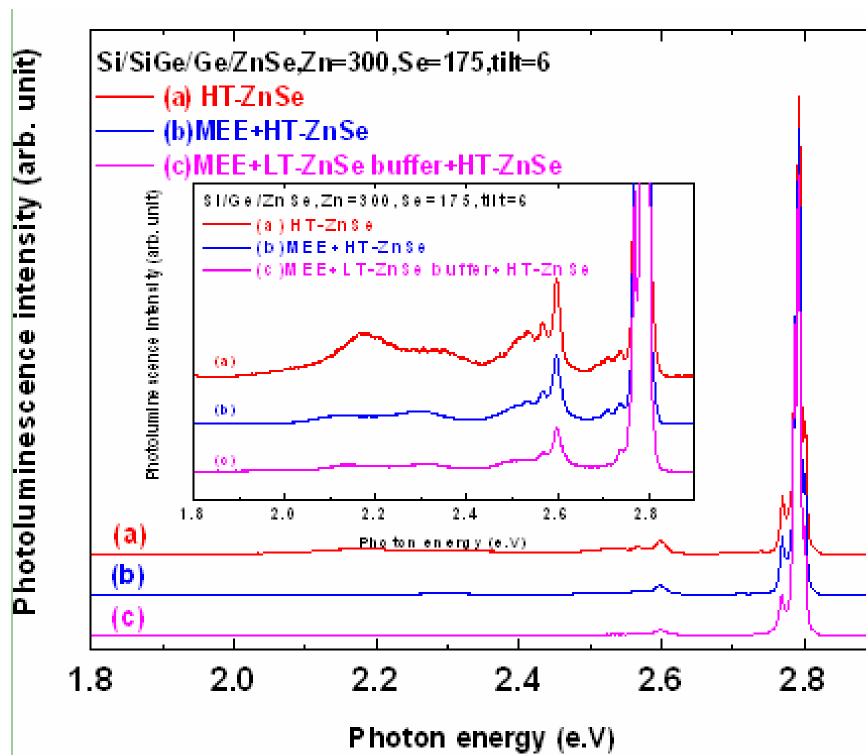


Fig. 4.7 PL spectra of the 6°off-cut ZnSe samples grown by using (a) high temperature directly growth (b) only initial MEE growth and (c) initial MEE with low temperature buffer growth process.

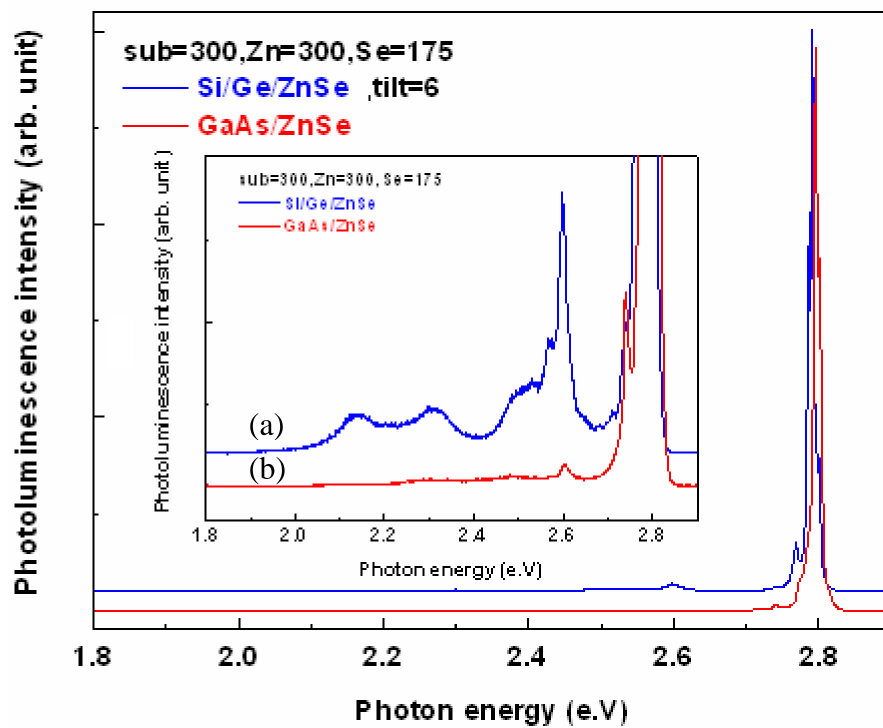


Fig. 4.8 PL spectra of (a) 6°off-cut ZnSe sample grown by using initial MEE with low temperature buffer and (b) directly grown ZnSe on GaAs sample.