

CHAPTER 1

Introduction

1 General background and motivations

The mismatched heterostructures are important for the microelectronic and optoelectronic devices. The examples include SiGe heterojunction bipolar transistors (HBTs) [1], Ge photo-detector integrated on Si substrate [2,3], III-V high electron mobility transistors (HEMTs) [4], and II-VI semiconductors blue-green lasers [5]. In these examples, the lattice mismatched layers are pseudomorphic to the underlying semiconductor substrates. The lattice mismatched heterostructures can have high defect density in the epilayers. The induced defect is a crucial issue for utilizing these heterostructures for electronic and optoelectronic device applications. Therefore, it is important to restrain the defect densities in the heterostructures. In this investigation, novel techniques for controlling dislocation densities in the $\text{Si}_{1-x}\text{Ge}_x$, GaAs, ZnSe epilayers on Si substrates are demonstrated. Nickel germanosilicide Ohmic contacts are also studied in this dissertation since they are very important constituents for the $\text{Si}_{1-x}\text{Ge}_x$ -based devices. Nevertheless, it was found that the thermal effect of germanosilicide was very different from that of the silicides in the Si technique. Therefore, the technology of the nickel germanosilicide contacts formed on $\text{Si}_{1-x}\text{Ge}_x$ layer needs further study. In the first part of this chapter, the growth of the strained and relaxed $\text{Ge}_x\text{Si}_{1-x}$ epilayers was introduced. Methods of growing relaxed Ge and $\text{Ge}_x\text{Si}_{1-x}$ layers on the Si substrates were introduced and the mechanisms for the reduction of reduce threading dislocations in the lattice mismatched heterostructures were illustrated. Additionally, a novel technique for the growth of high-quality Ge epilayer on the Si substrate is introduced. This novel structure provides the possibility of growing III-V and II-VI epilayers on Si substrates due to the reduction of dislocation density in these films. In the second part, techniques for growing GaAs on Si in the past few years are reviewed. A method for growing high-quality GaAs layer on Si

substrate is also presented in this dissertation. In the third part, approaches for growing ZnSe layer on Si in previously years are reviewed. A technique for growing high-quality ZnSe layer on Si substrate is also discussed in this investigation. In the fourth part, metal germanosilicide contacts formation study in the past few years is reviewed. In order to improve the properties of the nickel silicide on $\text{Si}_{1-x}\text{Ge}_x$, a Si capping layer grown on top of $\text{Si}_{1-x}\text{Ge}_x$ epilayers was introduced for the contact formation in this study. The last part of this chapter is the outline for this dissertation.

1-1 Growth of the $\text{Si}_{1-x}\text{Ge}_x$ and Ge epitaxial layers on Si substrate

Strained $\text{Si}_{1-x}\text{Ge}_x$ alloys have attracted considerable attention over the past few years. Early work by B. S. Meyerson in 1986 [6] demonstrated epitaxial growth of $\text{Si}_{1-x}\text{Ge}_x$ by using ultrahigh vacuum/chemical vapor deposition (UHV/CVD). The technique of growing $\text{Si}_{1-x}\text{Ge}_x$ films on Si substrate was first introduced in this time span, and the first case was applied to the epitaxial $\text{Si}_{1-x}\text{Ge}_x$ -base heterojunction bipolar transistors (HBT's). In recent years, $\text{Si}_{1-x}\text{Ge}_x$ layers were also applied to the well established (CMOS dominated) Si-based semiconductor industry. The strained-Si MOSFET is a promising device for the sub-100nm CMOS technology because of its high electron and hole mobilities. Developing this device currently requires a high-quality $\text{Si}_{1-x}\text{Ge}_x$ virtual substrate. Relaxation of the lattice strain during epitaxial growth of the $\text{Si}_{1-x}\text{Ge}_x$ layers always generates dislocation, surface roughness and cross-hatching. Nevertheless, the quality of the epilayer and the surface of the virtual substrate were quite unsatisfactory up to date. Several techniques for growing high Ge content in $\text{Ge}_x\text{Si}_{1-x}$ epilayer have been reported but still need further improvement. As the scaling of Si or $\text{Si}_{1-x}\text{Ge}_x$ MOSFET approaches its fundamental physics limit, the devices need new materials with high carrier mobility to improve the device performance. One of the promising materials is Ge due to its higher carrier mobility which results in larger drive current and the smaller bandgap for supply voltage scaling [16]. Inspired by the recent progress of high-k

dielectric gate in Si MOSFET applications, the Ge MOSFETs have attracted more and more attention and extensively investigated again [47,48].

Furthermore, a large lattice constant Ge semiconductor epitaxially grown on Si has been extensively studied in recent years. There are several applications such as solar cell [15] and Ge photo-detectors [2,3]. Especially application is provide a beneficial preliminary structure for III-V and II-VI devices integration on Si circuits in the future. $\text{Si}_{1-x}\text{Ge}_x$ is a candidate as a buffer structure for growing Ge epitaxial layer on Si substrate. However, the major problems of growing Ge on Si are the high density of threading dislocations and the high surface roughness arising from the 4.2% lattice mismatch between Ge and Si. This is due to the epitaxial growth of lattice mismatched $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures when the thickness of epilayer beyond the critical thickness [17] which generally results in the formation of threading dislocation. Due to this reason various of techniques have been attempted to circumvent the problem of threading dislocation. There are the compositionally graded buffer (CGB) layer [18], low-temperature Si buffer layer [19], compliant silicon-on-insulator (SOI) substrate [20], two-step procedure [21], and selective area growth combined with thermal cycle annealing [22]. Among them, the CGB layers are the most practically and widely used ones today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer from a thickness of approximately $10\mu\text{m}$ with a Ge composition ranging from zero to 1.0, which makes the integration of devices on the Si-base circuits difficult. Second, the CGB layers often exhibit a cross-hatch pattern, which makes the surfaces very rough [23]. In this study, we report a novel approach to obtaining a high-quality Ge layer. The total thickness of all epitaxial layers is only $2.6\mu\text{m}$. The threading dislocation density in the top Ge layer can be reduced to approximately $3\times 10^6\text{ cm}^{-2}$. The Ge surface roughness is only 32 \AA .

1-2 Growth of the GaAs epilayer on Si substrate

Single crystalline silicon (Si) is the most probable material for high-speed devices because of superior native oxide, low cost, large-area availability, high quality, and high thermal conductivity of the substrates. GaAs has advantages over Si for some applications due to its higher electron mobility, direct bandgap and wider bandgap. One way to take benefit of many of the best characteristics of both materials is to grow GaAs epitaxially on Si substrates. There are several potential advantages of this structure such as system on chip (SOC), lower costs, thermal and manufacturing improvement. However, the GaAs on Si system has many problems. They are: high lattice mismatch between Si and GaAs (4%); a large thermal expansion coefficient (~63%) between GaAs and Si; highly stressed GaAs films on Si; the growth of polar materials on non-polar substrates; poor surface morphologies and auto doping of Si from substrate into the GaAs film [24]. Figure 1.1 shows lattice constants and linear thermal expansion coefficients of IV, III-V and II-VI [24]. For GaAs grown directly on Si substrate that negates the advantages of GaAs on Si system by generating large densities of dislocations in the GaAs epitaxial layers due to high lattice mismatch. While many methods for controlling and reducing the threading dislocation density (TDD) have been explored, including III-V buffers and/or thermal cycling [25-32], compositionally graded $\text{Ge}_x\text{Si}_{1-x}$ buffer layer (CGB) is the most practical and is extensively used currently [25]. However, CGB layer approach faces two major challenges, which make the integration of the GaAs devices on the Si-based circuits difficult. First, the crosshatch pattern of the CGB layer makes its surface very rough [33]. Second, the CGB layer is very thick. Additionally, the inter-diffusion across the GaAs/Ge interface that occurs during epitaxial growth is important because it affects the control of the doping profile in GaAs. Several approaches have been proposed to suppress the Ge inter-diffusion, as reported in Refs [34,35]. In this thesis, the techniques of growing high-quality GaAs on Si with suppressed interdiffusion by using novel Ge/GeSi/Si, improved crystalline and optoelectronic property of GaAs on Si are investigated.

1-3 Growth of the ZnSe epilayer on Si substrate

ZnSe is a very interesting material for optoelectronics applications [36]. In recent years the mature molecular beam epitaxy (MBE) and other growth techniques [37] have been made in order to obtain high quality ZnSe layers. However, improvements of ZnSe epilayer crystal quality are necessary for commercial device production. The lack of suitable substrates to grow ZnSe is one of the problems impede the development of high performance optoelectronic devices. ZnSe substrates are now available but they are sparse and very expensive. Therefore, GaAs that has a small lattice mismatch to ZnSe (0.27%) has been the substrate of choice for the growth of the ZnSe epitaxial layers [38]. However, the heteroepitaxial growth of ZnSe on GaAs presents some intrinsic problems like the generation of dislocations when the epilayer thickness exceeds a critical thickness, the difference in the thermal expansion coefficients, surface segregation of Ga, etc. [39-41]. These problems are due to the crystal defects generated at the ZnSe/GaAs interface. Besides, Ge also has a small lattice mismatch to ZnSe, which is another suitable substrate for growing ZnSe/Ge heteroepitaxial [42]. A different approach for growing ZnSe layer is use the Si substrates [43]. Si substrates are cheaper and have better thermal and mechanical properties than GaAs substrates. Moreover, the possibility of integrating the optoelectronics based on ZnSe with Si circuit is one of the most important motivations to study the growth of ZnSe on Si. However, the large lattice mismatch (4.3%) between ZnSe and Si and the chemical reactions at the interface between these two materials make the growth of ZnSe on Si difficult [44-46].

In this thesis, the techniques for growing high-quality ZnSe on Si with suppressed interdiffusion by using novel Ge/GeSi/Si buffer structure is investigated, and improved the crystal properties of ZnSe on Si is achieved.

1-4 Nickel germanosilicide contact formation

For the high speed device applications the metal silicide based Ohmic contacts are very important constituents for the $\text{Si}_{1-x}\text{Ge}_x$ based devices. Silicide was first introduced to LSI devices, as a MoSi_2 polycide word line in 256K DRAM in early 1980s, which was one of the first applications of polycide to LSI production. Then, WSi_2 polycide was popularly used for the gate electrode of logic LSIs from the middle of the 1980s because the sheet resistance of WSi_2 is smaller than that of the MoSi_2 . When the self-aligned silicidation (salicide) became popular in recent years, TiSi_2 was used in 1990s. TiSi_2 was selected as the material for salicide, because the sheet resistance is much smaller than WSi_2 . However, TiSi_2 was eventually found to be relatively difficult material to treat due to the controllability in thermal process, because high temperature process caused severe agglomeration. Thus, CoSi_2 replaced TiSi_2 from the late 1990s and have made the metallization process more suitable toward deep-sub micron CMOS. However, for the sub-100 nm technology node, the widely used CoSi_2 contact is expected to be replaced by NiSi contact, this is especially true for the $\text{Si}_{1-x}\text{Ge}_x$ device applications in the future.

For the sub-100 nm $\text{Si}_{1-x}\text{Ge}_x$ -based devices the metal germanosilicide Ohmic contacts are very important constituents. Germanosilicided $\text{Si}_{1-x}\text{Ge}_x$ junction has attracted lots of attention due to its potential applications as the contacts for the SiGe based electronic devices such as the base metal for HBTs [7] and advanced SiGe source/drain for deep submicron CMOS [8]. The performances of the $\text{Si}_{1-x}\text{Ge}_x$ -based devices, such as switching speed and high-power characteristics depend critically on the properties of these Ohmic contacts. Interfacial reactions of metals such as Co and Ni with $\text{Si}_{1-x}\text{Ge}_x$ films to form metal silicide Ohmic contacts have been investigated [9-12]. Nickel silicide has attracted much attention as a potential alternative to cobalt silicide since it requires lower thermal budget. Additionally, the low-resistivity, one-step silicidation process with no adverse narrow line effect on sheet resistance makes Ni silicide an attractive candidate for use in self-alignment technology

[13,14]. Unfortunately, the morphological stability of the nickel germanosilicide film formed by direct annealing of nickel on $\text{Si}_{1-x}\text{Ge}_x$ layer $\text{Ni-Si}_{1-x}\text{Ge}_x$ is notably bad and the Ge segregation appeared during the long time thermal (400°C) stress. For $\text{Si}_{1-x}\text{Ge}_x$ based device applications, these problems shall be solved immediately. In this study, a suitable thickness of Si capping layer was deposited on the top of SiGe layer to improve the material and electrical properties of the Ohmic contacts is presented and excellent results were obtained.

1-5 Outline of this dissertation

This dissertation presents the growth of heterostructure semiconductors ($\text{Ge}_x\text{Si}_{1-x}$, GaAs, ZnSe) on Si and nickel germanosilicide contacts on $\text{Si}_{1-x}\text{Ge}_x$ layers and is divided into 6 chapters, including:

In Chapter 2, we present a mechanism of interface-blocking to reduce the threading dislocations in the $\text{Si}_{1-x}\text{Ge}_x$ and Ge layers on Si (100) substrates. Additionally, growth of high-quality epitaxial Ge layers on a Si (100) substrate by using this mechanism is presented. Experimental results show that the dislocation density in the top Ge layer can be greatly reduced, and the surface is very smooth, while the total thickness of the structure is only $2.6\mu\text{m}$. This buffer structure also provides a virtual substrate to grow III-V and II-VI heterostructure on Si in this study.

In Chapter 3, the growth of high-quality GaAs layers on Si (100) substrate by using Ge/ $\text{Si}_{1-x}\text{Ge}_x$ buffer structure is proposed. The experimental results show that the dislocation density in the top GaAs layers can be greatly reduced, and the surface is kept very smooth after the growth, while the total thickness of the structure is only $5.1\mu\text{m}$. Moreover, out-diffusion of Ge into the GaAs epilayer is also successfully suppressed using the 6° off-cut Ge/ $\text{Ge}_{0.95}\text{Si}_{0.05}$ / $\text{Ge}_{0.9}\text{Si}_{0.1}$ /Si virtual substrate.

In Chapter 4, the epitaxial growth of ZnSe layers on Si substrates utilizing a Ge/ $\text{Ge}_{0.95}\text{Si}_{0.05}$ / $\text{Ge}_{0.9}\text{Si}_{0.1}$ buffer structure is presented. In this study, we examine the material

and optical characteristics of ZnSe epilayer grown on Si. Additionally, atomic interdiffusion in the ZnSe epilayer is also investigated. In a sample with a large off-cut Si virtual substrate, the outdiffusion of Ge into the ZnSe epilayer is suppressed. The low-temperature PL measurements indicate that the sample with a large off-cut Si substrate improves its optical characteristic effectively. The X-ray diffraction analysis and transmission electron microscopy (TEM) results indicate that the crystallinity of the ZnSe epilayer on Si is markedly improved. The method of low temperature MEE and buffer layer growth with *in-situ* annealing can suppress the formation of the deep-level emission in the ZnSe/Ge/Ge_xSi_{1-x} structure effectively is also demonstrated.

In Chapter 5, we present the material and electrical properties of the nickel germanosilicide formed on various Si_{1-x}Ge_x (x=0, 0.2 and 0.3) layers, such as formed phase, agglomerates, sheet resistance and specific contact resistivity. Besides, thermal stability of the nickel germanosilicide on high-dose B⁺, BF₂⁺, P⁺ and As⁺-implanted Si_{0.8}Ge_{0.2} epilayers are also investigated. The Si capping grown on the top of the Si_{1-x}Ge_x layers are adopted to improve the property of the nickel silicide Ohmic contacts. By using this method, the agglomeration occurred in the silicidation film is suppressed and the electrical characteristics are improved. Additionally, the morphological stability of the nickel germanosilicide after aging at temperature of 400°C is also discussed.

In Chapter 6, important conclusions are drawn. They are (1) the growth and characterization of the Si_{1-x}Ge_x, GaAs and ZnSe epilayers on Si (100) substrates are systematically studied. (2) The mechanism of interface-blocking is proposed to reduce the threading dislocations in the Si_{1-x}Ge_x and Ge epilayers on Si substrates and experimentally are demonstrated. (3) The high-quality epitaxial Ge layers on a Si substrate are achieved. (4) High-quality of GaAs and ZnSe epilayers grown on Si using Ge/Ge_xSi_{1-x}/Si buffer structure are successfully substantiated. (5) The properties of nickel germanosilicide contact on Si_{1-x}Ge_x are also investigated and improved.

1.6 References

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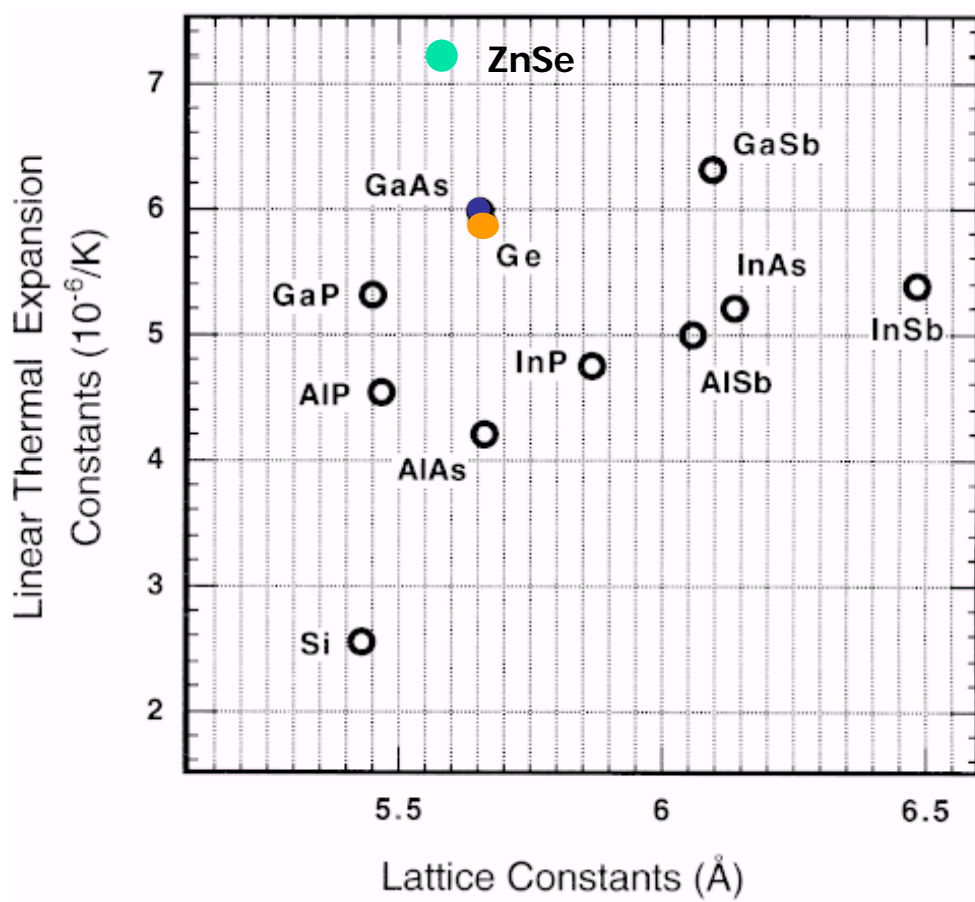


Fig. 1.1 Lattice constants vs linear thermal expansion coefficients of IV, III-V and II-VI.