CHAPTER2

Growth of the SiGe and Ge epitaxial layers on Si substrate

In this chapter a mechanism of interface-blocking is proposed and implemented to reduce the threading dislocations in the $Si_{1-x}Ge_x$ and Ge layers on the Si(100) substrates. In this work, epitaxial $Si_{1-x}Ge_x$/ $Si_{1-(x-y)}Ge_{x-y}$ and Ge/ Si_yGe_{1-y} layers were grown by UHV/CVD. It is surprisingly found that if the variation of the Ge composition, y, across the interface of $Si_{1-x}Ge_x$/ $Si_{1-(x-y)}Ge_{x-y}$ or Ge/ Si_yGe_{1-y} was higher than a certain value, most of the threading dislocations appeared to be blocked and confined in the underlying $Si_{1-(x-y)}Ge_{x-y}$ or Si_yGe_{1-y} layer by the interface. This finding provides a simple way to grow high-quality strain relaxed $Si_{1-x}Ge_x$ and Ge layers on the Si substrates. Additionally, a method of growing high-quality epitaxial Ge layers on a Si (100) substrate is reported. In this method, a 0.8μm $Si_{0.1}Ge_{0.9}$ layer is first grown. Due to the large lattice mismatch between this layer and the Si substrate, many dislocations formed near the interface and in the lower part of the $Si_{0.1}Ge_{0.9}$ layer. A 0.8μm $Si_{0.05}Ge_{0.95}$ layer and a 1.0μm top Ge layer were subsequently grown on the $Si_{0.1}Ge_{0.9}$ layer. The formed $Si_{0.05}Ge_{0.95}$/ $Si_{0.1}Ge_{0.9}$ and Ge/ $Si_{0.05}Ge_{0.95}$ interfaces can bend and terminate the upward-propagated dislocations in the lower layers very effectively. The *in situ* annealing process is also performed for each individual layer. Experimental results showed that the dislocation density in the top Ge layer was greatly reduced, and the surface was very smooth, while the total thickness of the structure was only 2.6μm.

2-1 Introduction

Heterostructures of the SiGe and Ge epitaxial layers on the Si substrates have attracted considerable attentions due to their potential device applications and compatibility with Si-based technology [1]. In particular, strain-relaxed SiGe and Ge layers provide a virtual substrate for the growth of high-electron-mobility structures and for the integration of the III-V devices on Si substrate [10]. In addition, the integration of Ge with Si is of much importance for the application of Ge photodetectors. The major problems of these relaxed layers are the high density of threading dislocations and the high surface roughness arising from the 4.2% lattice mismatch between Ge and Si. Various growth techniques and treatments have been developed to solve these problems. It has been reported that the compositionally graded buffer (CGB) layers [2], low-temperature Si buffer layers [3], compliant silicon-on-insulator (SOI) substrate [4], two-step procedure [5], and selective area growth combined with thermal cycle annealing [6] can be used to grow high-quality strain-relaxed SiGe and Ge layers. Among them, the CGB layers method is the most practically and widely used one today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer the fact it requires a thickness of approximately 10 μm for the Ge composition to range from zero to 1.0, which increases crucially the price of the SiGe devices processed on this substrate and hinders their integration with conventional Si-based circuits. Second, the CGB layers often exhibit a cross-hatch pattern, which makes the surfaces very rough [7].

It has been reported earlier that the strained isoelectronically In-doped GaAs layer grown on the GaAs wafers allow one to reduce the dislocations density drastically, where the authors found that the interface formed between the In-doped GaAs layer and GaAs substrate can bend the dislocations effectuality [8]. We believe that a similar mechanism can be easily used to grow SiGe and Ge layers with reduced dislocation densities on the Si(100) substrates.

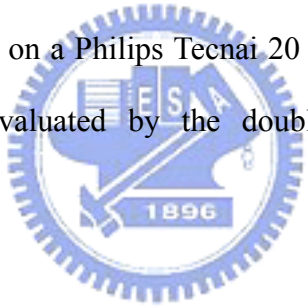
In addition, we also report an alternative approach to obtaining a high-quality Ge layer.

The total thickness of all epitaxial layers is only 2.6μm. The threading dislocation density in the top Ge layer can be reduced to approximately 3×10^6 cm^{-2}. The Ge surface roughness is only 32 Å. The procedure mainly involves growing three epitaxial layers (see Fig. 2.6). The first layer is the $Si_{0.1}Ge_{0.9}$ layer, the second is the $Si_{0.05}Ge_{0.95}$ layer, and the third is the Ge layer. After the growth of each individual layer, *in situ* 750℃ annealing for 15 min was performed. Due to the large lattice mismatch at the interface between $Si_{0.1}Ge_{0.9}$ and Si layer, many close small islands were formed during the growth at low temperatures. As growth proceeded, these islands quickly coalesced into a continuous film [11]. At the same time, many dislocations generated and interacted with each other to form closed non-propagating loops and networks near the interface. A small portion of the dislocations that did not have the chance to pair up continued to propagate upward. A similar technique has been widely used in growing highly mismatched heterostructures, for example, GaN on Sapphire [12]. Due to the proper lattice mismatch strains at the upper interfaces of $Si_{0.05}Ge_{0..95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$, the upward-propagated dislocations can be bent sideward and terminated effectively. Details of the behavior of dislocations at the mismatched interfaces can be seen in refs. 8 and 13. Additionally, the thermal annealing process, which was performed after growing each individual layer, can further reduce dislocation density in the epitaxial layers. The mechanism of threading dislocation reduction employed in this work is shown schematically in Fig. 2.6

2-2 Ge/SiGe epitaxial layer growth procedure

In our laboratory, the epitaxial SiGe and Ge layers were grown by UHV/CVD equipment using silane and germane as the Si and Ge sources [14]. Usually, growth temperature of 550°C was used to grow $Si_{1-x}Ge_x$ layers with $x<0.3$, and 420°C was used to grow Ge layer and $Si_{1-x}Ge_x$ layer with $x>0.8$. The samples in this work were grown based on two structures (see fig. 2.1). For the structure (a), a $Si_{1-(x-y)}Ge_{x-y}$ was first grown, after in-situ annealing it at

950°C for 5min for strain-relaxation, a second layer $Si_{1-x}Ge_x$ was then grown. For the structure (b), a Si_yGe_{1-y} was first grown, after in-situ annealing at 750°C for 15min for strain relaxation, a Ge layer was subsequently grown. Finally, an annealing of 750°C for 15min was performed again for removing the defects that may generate in the Ge layer grown at low temperature. The improvement method of growing high-quality Ge epitaxial layers on a Si substrate was involved: First, a 4-inch Si (100) substrate wafer was cleaned by 10% HF dipping and high-temperature baking at 800℃ in the growth chamber for 5 min. Then, a 0.8μm $Si_{0.1}Ge_{0.9}$, a 0.8μm $Si_{0.05}Ge_{0.95}$, and a 1.0μm Ge layer were grown at 400℃ in sequence. Between successive layer, growth was interrupted for an *in suit* 15 min 750℃ annealing. Transmission electron microscopy (TEM) was used to observe the dislocation distribution and the interaction of the dislocations with the interfaces. These TEM measurements were carried out on a Philips Tecnai 20 microscope. The crystalline quality of Ge layer was additionally evaluated by the double-crystal x-ray diffraction (DCXD) measurement.



2-3 Characteristics of the SiGe and Ge epitaxial layers

Figure 2.2 is a cross-sectional TEM (XTEM) image of a sample with a 7500Å $Si_{0.8}Ge_{0.2}$ layer on Si. No measure was taken to control the dislocations. This sample was also annealed at 950°C for 5 min for its full relaxation. From the image, a large number of threading dislocations were observed to generate from the $Si_{0.8}Ge_{0.2}$/Si interface and continue to propagate through the entire epitaxial layer to the surface.

Figure 2.3 is an XTEM image of a sample on which an epitaxial structure of $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}$ was grown the first $Si_{0.8}Ge_{0.2}$ layer which was about 1.2μm thick, and the second $Si_{0.76}Ge_{0.24}$ layer was grown about 0.5μm thick. It is seen that some threading dislocations that generate within the first $Si_{0.8}Ge_{0.2}$ layer were blocked by the $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}$ interface, but others still penetrate through the interface to the top layer.

However, for the $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ sample the first $Si_{0.8}Ge_{0.2}$ layer was about 1.2μm thick, and the second $Si_{0.7}Ge_{0.3}$ layer was about 0.6μm thick. It is seen that the dislocations that generate within the first $Si_{0.8}Ge_{0.2}$ layer were remarkably blocked by the $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ interface. The threading dislocations that penetrated through the interface were greatly reduced (see Fig. 2.4).

Figure 2.5 (a) is an XTEM of a sample on which the first layer is a 1.5μm thick $Si_{0.08}Ge_{0.92}$ layer, and the second layer is a 1.0μm thick Ge layer. It is surprisingly found that the high-density dislocations that generate within the $Si_{0.08}Ge_{0.92}$ layer were also blocked drastically by the interface of Ge/ $Si_{0.08}Ge_{0.92}$. The top Ge layer exhibits a good crystalline quality with a low threading dislocation density. Under the optical microscope, it is estimated that the dislocation density in this top Ge layer is about $6\times10^6/cm^2$, by counting the etch-pits that were selectively etched by solution of $CH_3COOH:HNO_3:HF:I_2$=67ml:20ml:10ml:30mg for 10s. Figure 2.5 (b) is the DCXD result for this sample. The peak of Ge is sharp, which also implies that the crystalline quality of the top Ge layer is superior. Moreover, the total thickness of these two layers is only about 2.5μm, which is much less than that of traditional CGB structure.

The mechanism of interface-blocking of dislocations is considered to be due to the dislocation bending behavior under the stress field. When the stress field around the interface is strong enough, the dislocation can be bent and traverse along the interface. From the XTEM images, it can be found that the interfaces of the $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ and the $Ge/Si_{0.08}Ge_{0.92}$ (see Fig. 2.4 and Fig. 2.5) are rough. It implies that a strong non-uniform stress field exists at these interfaces. When the dislocations in these two samples meet the interfaces, they can be blocked very effectively. The phenomenon of the dislocation bending under the stress can also be found in other material structures such as the GaN lateral overgrowth on the sapphire substrate as reported recently, where the authors observed many dislocations bend at the edges of the GaN ridges due to the stress distributed there [9].

Figure 2.7 shows the cross-sectional TEM image of the sample. There are a large number of dislocations located near the $Si_{0.1}Ge_{0.9}$/Si interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. The upward propagated dislocations are bent sideward and terminated very effectively by the $Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$ and Ge/$Si_{0.05}Ge_{0.95}$ interface. Almost no threading dislocation can propagate into the top Ge layer. The image shows that the total thickness of the three epitaxial layers is only approximately 2.6μm, which is much smaller than that of CGB layers reported earlier. In this study, the Ge composition variation at the two strained interfaces is set at 0.05. We found that if the Ge composition variation is larger than 0.05, new dislocations will generate from the interfaces due to the relatively large lattice mismatch. On the contrary, if the Ge composition variation is less than 0.05, the mismatch strain formed at the interfaces is too small to terminate the dislocation effectively. The thickness of each SiGe layer in the sample may not be optimum. Further experiments are required to investigate the effects of changing the thickness.

A plan-view TEM image of the sample surface is shown in Fig. 2.8 There is no dislocation in this image. By analyzing several plan-view TEM images, the threading dislocation density is estimated to be about 3×10^{6} cm^{-2}.

The surface roughness was measured by AFM (see Fig. 2.9). No cross-hatch pattern was observed. The root mean square (RMS) of the surface is only 32 Å, which is also much smaller than that of the CGB layers reported earlier. This smooth surface is useful for fabrication of devices and growth of III-V materials.

2-4 Conclusions

In conclusion, a mechanism of interface-blocking was proposed to reduce the threading dislocations in the SiGe and Ge layers on the Si(100) substrates. When the variation of the Ge composition, y, across the interface of the $Si_{1-x}Ge_x$/ $Si_{1-(x-y)}Ge_{x-y}$ or Ge/ Si_yGe_{1-y} is higher than a certain value, most of the threading dislocations appear to be blocked and confined in the

underlying $Si_{1-(x-y)}Ge_{x-y}$ or Si_yGe_{1-y} by the interface. For $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}/Si$ (y=0.1) and Ge/ $Si_{0.08}Ge_{0.92}/Si$ (y=0.08) samples, both top layers show low dislocation densities on the sample. It implies that the mechanism of interface-blocking can be easily used to control the dislocations for growth of the relaxed SiGe and Ge layers on the Si substrates.

Additionally, we have designed a method of growing high-quality Ge epitaxial layers on the Si substrates. The method mainly involves: (1) growth of three layers consisting of 0.8μm $Si_{0.1}Ge_{0.9}$, a 0.8μm $Si_{0.05}Ge_{0.95}$, and a 1.0μm top Ge layer, and (2) *in situ* 750℃ annealing for 15 min performed on each individual layer. By this procedure, many dislocations were formed at the $Si_{0.1}Ge_{0.9}/Si$ interface and at the lower part of the $Si_{0.1}Ge_{0.9}$ layer. Moreover, the upward propagated dislocation can be bent and terminated effectively by the interfaces of $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and Ge/ $Si_{0.05}Ge_{0.95}$. The top Ge layer exhibits a low threading dislocation density and a smooth surface, while the total thickness of the epitaxial structure is relatively small. It is show that this method is very practical for growing of high-quality Ge epitaxial layers on Si substrates.

2-5 References

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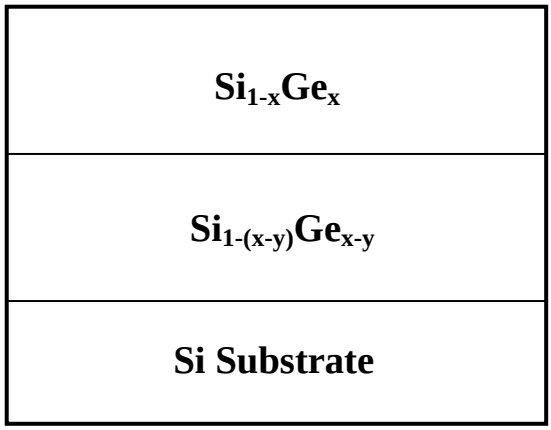
(a)



(b)

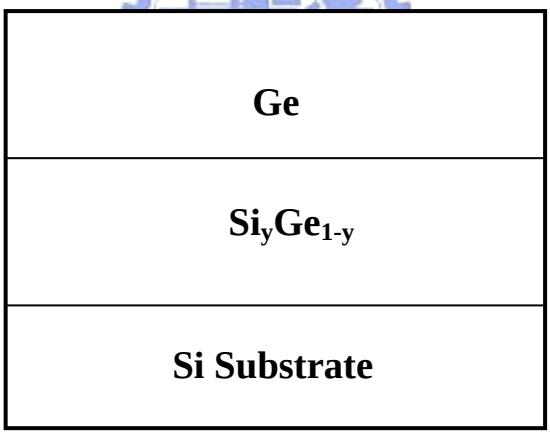


Fig.2.1 Samples structures (a) and sample structure (b). Their detailed growth conditions are described in context.

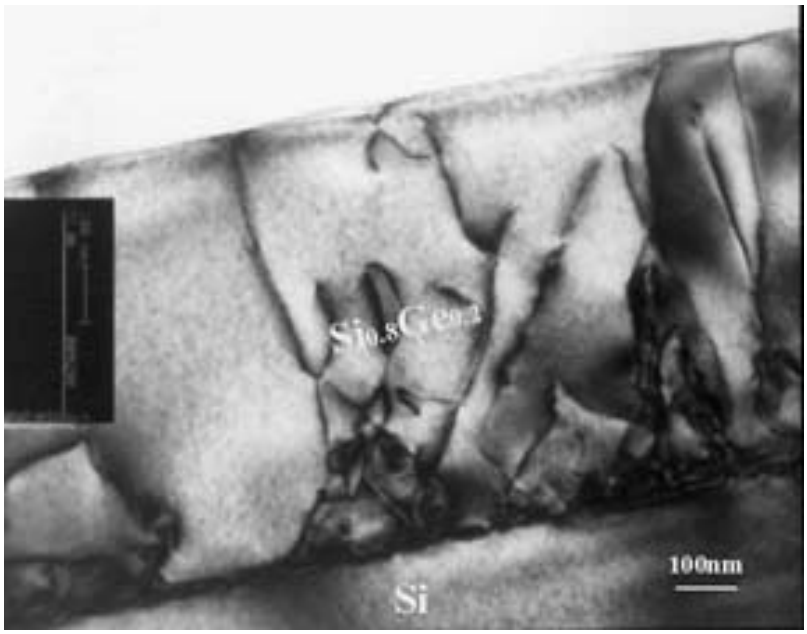


Fig.2.2 XTEM image of the $Si_{0.8}Ge_{0.2}$/Si epilayers. Dislocations distribute in the entire epitaxial layer.

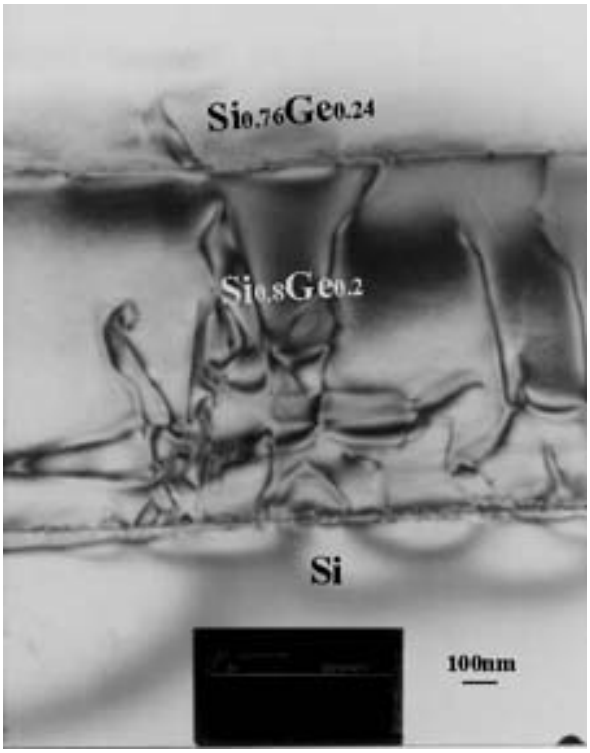


Fig.2.3 XTEM image of the $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}/Si$ epilayers. Some dislocations were blocked by the interface, but some penetrated the interface.

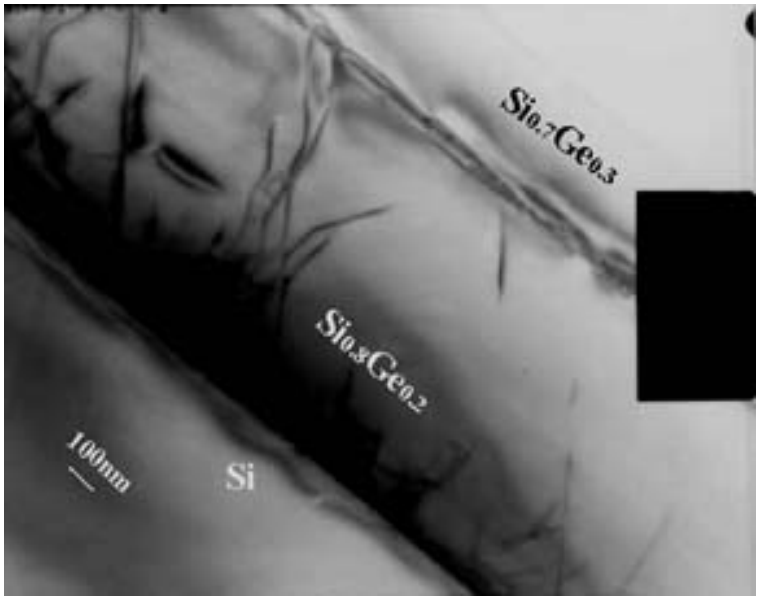


Fig.2.4 XTEM image of the $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}/Si$ epilayers. Almost all the dislocations were blocked by the $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ interface.

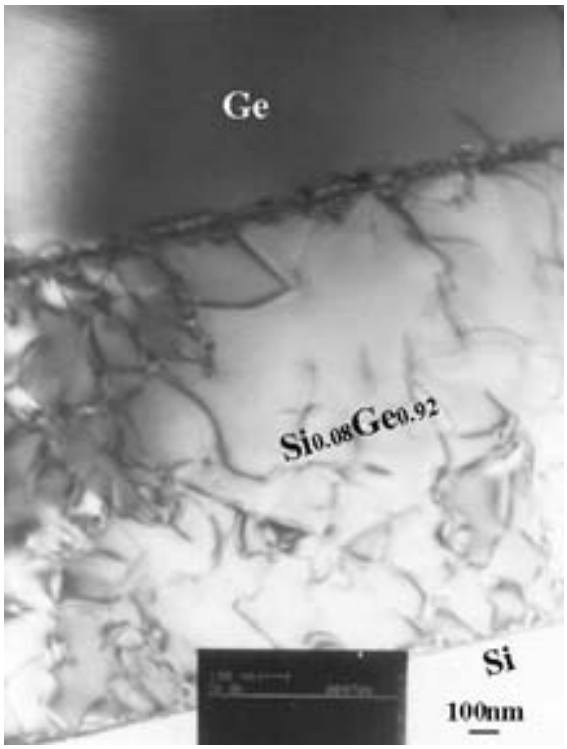


Fig.2.5 (a) XTEM image of the Ge/$Si_{0.08}Ge_{0.92}$/Si epilayers. Dislocations are blocked effectively by the Ge/$Si_{0.08}Ge_{0.92}$ interface.

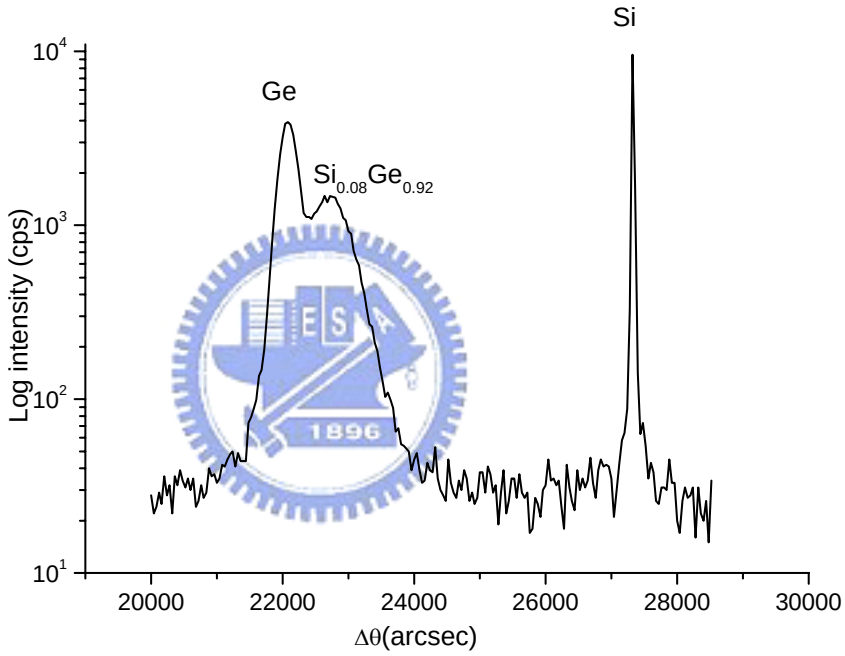


Fig. 2.5 (b) Double-crystal x-ray diffraction result for the $Ge/Si_{0.08}Ge_{0.92}/Si$ sample.

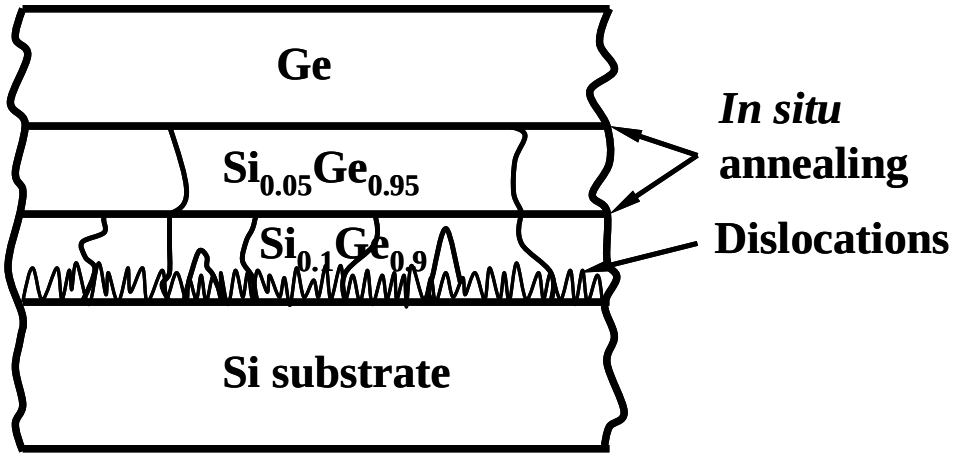


Fig. 2.6 Schematic of the mechanism of the reducing threading dislocations.

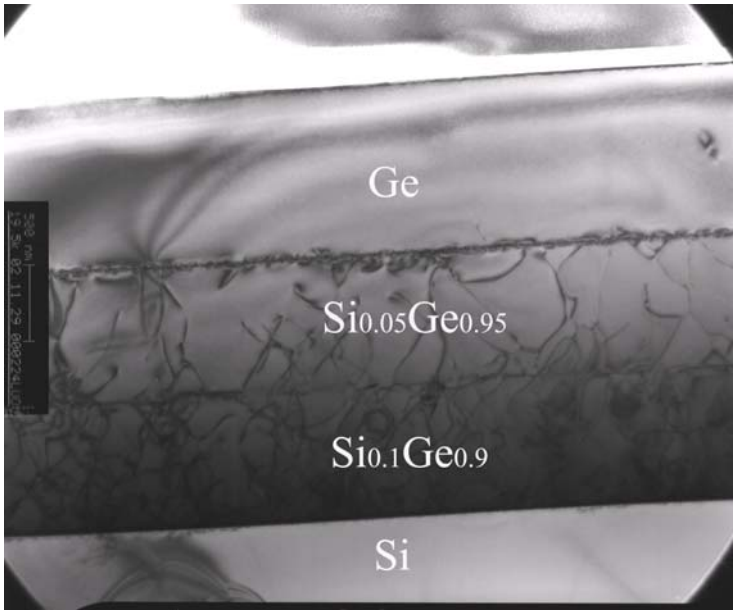


Fig. 2.7 Cross-sectional TEM image of the epitaxial structure.

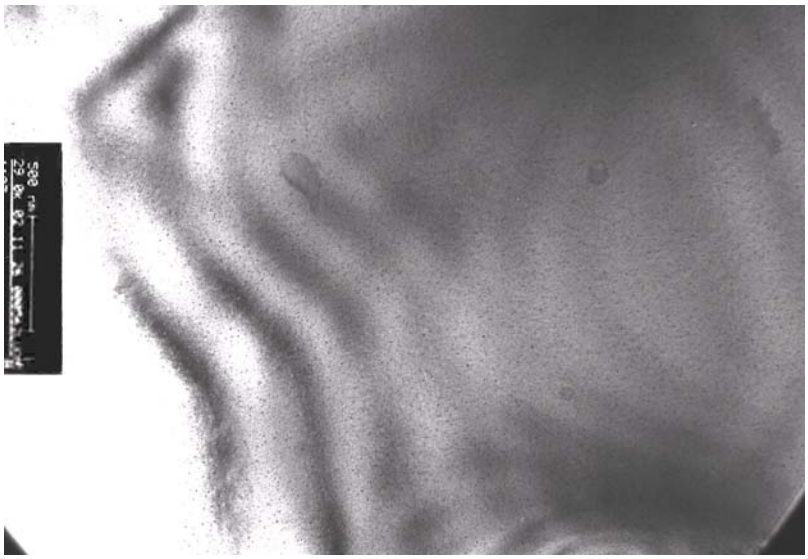


Fig. 2.8 Plan-view TEM image of the top Ge layer.

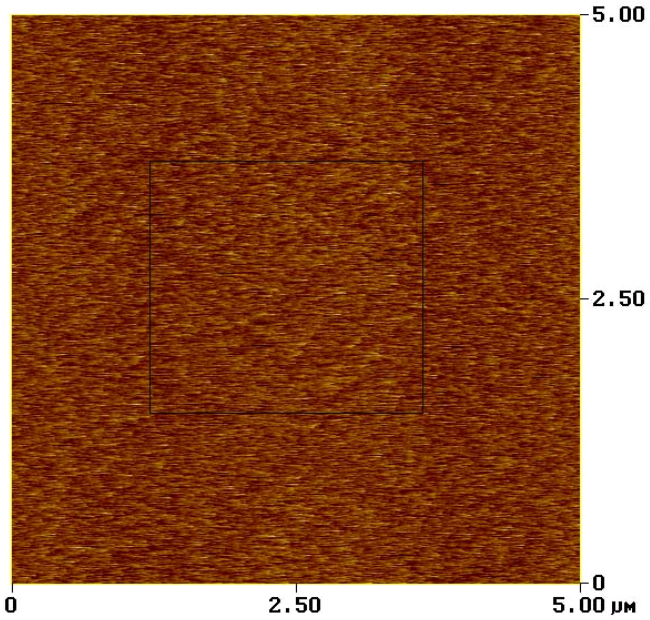


Fig. 2.9 AFM image of the surface of the top Ge layer.