A Decorrelating Design-for-Digital-Testability Scheme for $\Sigma-\Delta$ Modulators

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***Abstract*—This paper presents a novel decorrelating design-for-digital-testability ($\mathbf{D^3T}$) scheme for $\Sigma-\Delta$ modulators to enhance the test accuracy of using digital stimuli. The input switched-capacitor network of the modulator under test is reconfigured as two or more subdigital-to-charge converters in the test mode. By properly designing the digital stimuli, the shaped noise power of the digital stimulus can be effectively attenuated. As a result, the shaped noise correlation as well as the modulator overload issues are alleviated, thus improving the test accuracy. A second-order $\Sigma-\Delta$ modulator design is used as an example to demonstrate the effectiveness of the proposed scheme. The behavioral simulation results showed that, when the signal level of the stimulus tone is less than −5 dBFS, the signal-to-noise ratios obtained by the digital stimuli are inferior to those obtained by their analog counterparts of no more than 1.8 dB. Circuit-simulation results also demonstrated that the $\mathbf{D^3T}$ scheme has the potential to test moderate nonlinearity. The proposed $\mathbf{D^3T}$ scheme has the advantages of achieving high test accuracy, low circuit overhead, high fault observability, and the capability of conducting at-speed tests.**

***Index Terms*—Analog digital conversion, built-in self-test (BIST), CMOS mixed-mode circuits, design-for-testability (DFT), integrated-circuit testing, sigma–delta modulation.**

I. Introduction

AMONG VARIOUS analog-to-digital converter (ADC) architectures, $\Sigma-\Delta$ modulator is a popular one for implementing high-resolution ADCs because of its robustness against circuit imperfections [1]. They are widely used in low- and medium-speed applications such as instrumentation, audio, and xDSL. Traditionally, testing such high-resolution ADCs is expensive and troublesome because of the requirements of the high-end mixed-signal automatic test equipment (ATE), a long test time induced by the sequential mixed-signal test flow, and an ultralow-noise testing environment [2].

Functional-test-based built-in self-test (BIST) schemes are appealing approaches to reduce the testing cost [3]–[6]. The idea is to simply implement the necessary high-performance analog-stimulus generator (ASG) on-chip in order to digitalize all the input/output (I/O) interfaces during testing. The functional-test-based feature of such BIST systems ensures that the test results are both detailed and flexible. In addition, unifying the testing interfaces into purely digital ones saves the testing cost. The costly mixed-signal ATE, now, can be replaced with a cheaper digital one. The test time may also be reduced because a concurrent mixed-signal test flow is possible. Moreover, the off-chip environmental interferences are alleviated which makes the loadboard design easier.

The key requirements of a successful functional-test-based BIST implementation include the following conditions.

1) High test accuracy: The test stimuli generated by the embedded ASG must have a higher signal-to-noise-and-distortion ratio (SNDR) than the circuit under test (CUT) can achieve. Otherwise, the ASG will dominate the test results rather than the CUT itself.
2) Low cost: The additional circuits for testing purpose should be robust enough so as not to reduce the production yield, and their hardware overhead should be small in order to save the fabrication cost.
3) High fault observability: All components active in normal operation should be excited during testing as well as for propagating the possible faulty effects to certain observable outputs.
4) At-speed test capability: The test scheme should not impose any extra load on the timing-critical components, e.g., operational amplifiers (OPAMPs), in order to test the CUT at the rated speed.

Many researches focused on implementing the embedded ASG cost effectively [4], [7]–[15]. They can be classified into the following categories: employing the available on-chip multibit digital-to-analog converter (DAC) [4], [7], [8], using a ramp waveform generator [9], [10], and exerting an exponential waveform generator [11]. Applying a single-bit DAC followed by an analog antialiasing filter is another attractive approach [3], [12]–[14], [16].

In [17], a $\Sigma-\Delta$-modulation-based design-for-digital-testability (DfDT) scheme for $\Sigma-\Delta$ modulators that meets most of the key requirements aforementioned has been proposed. At an oversampling ratio (OSR) of 128, the digital stimulus is able to measure a signal-to-noise ratio (SNR) of the second-order modulator under test (MUT) higher than 76 dB. Yet, the measured SNRs by the digital stimuli are still inferior to those using their analog counterparts by 0.7–7.6 dB, depending on the signal level of the stimulus tone. The peak SNDR of the digital tests was obtained by the −6-dBFS stimulus. Rolindez *et al.* [15] proposed an alternative implementation that can accept pure digital stimuli. Their measurement results also showed that the signal levels of the digital stimuli had better not to exceed −12 dBFS; otherwise, the tested SNDRs of the digital tests will significantly degrade [18].

In this paper, we propose a decorrelating DfDT ($\mathrm{D^3T}$) scheme for general switched-capacitor (SC) $\Sigma-\Delta$ modulators

Manuscript received January 9, 2007; revised January 30, 2008. First published June 6, 2008; current version published February 4, 2009. This work was supported by the National Science Council, Taiwan, under Grant NSC93-2215-E009-050 and Grant NSC94-2215-E009-081. This paper was recommended by Associate Editor I. Bell.

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Digital Object Identifier 10.1109/TCSI.2008.926986

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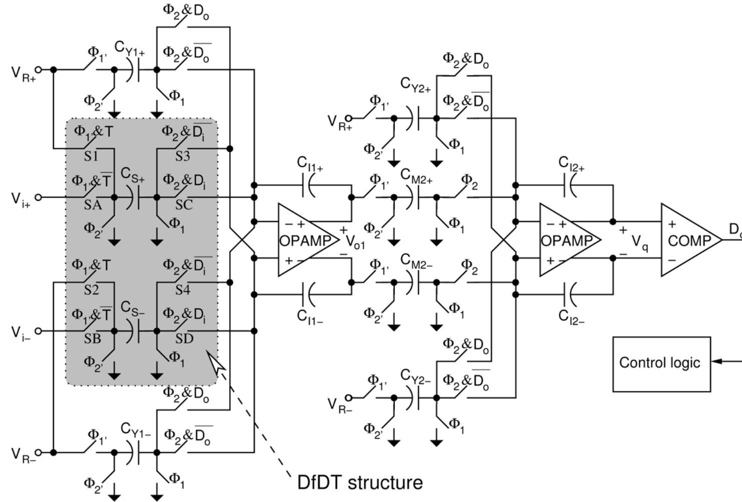

Fig. 1. Schematic of the original DfDT second-order $\Sigma-\Delta$ modulator proposed in [17].

that improves the test accuracy of using digital stimuli, while it preserves the advantages of the original DfDT scheme such as having a small hardware overhead, high fault observability, and the capability to perform at-speed tests. Section II reviews the original DfDT scheme and explains the root causes of the test accuracy degradation when applying the digital stimuli. Based on the results, Section III introduces the proposed $\mathrm{D^3T}$ scheme and its operation principles. Section IV discusses how to design the circuits as well as the tests of the $\mathrm{D^3T}$ $\Sigma-\Delta$ modulators. A $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator design modified from [17] was used as an example. Behavioral and circuit simulations were conducted to demonstrate the $\mathrm{D^3T}$'s superiority in Section V. Finally, Section VI draws our conclusions.

II. Reviews of the DfDT $\Sigma-\Delta$ Modulator

Fig. 1 shows the schematic of the DfDT second-order $\Sigma-\Delta$ modulator proposed in [17]. This schematic is identical to that of a normal $\Sigma-\Delta$ modulator except for the DfDT structure indicated by the shaded region. The DfDT circuit is modified from the original one in the normal $\Sigma-\Delta$ modulator by adding the four additional switches, including $S1$ to $S4$. The control signals of the switches in the DfDT structure are also modified.

The DfDT scheme operates as follows. The test-mode control signal T sets the operation mode. When T is set to zero and the digital stimulus D_i is fixed on one, the switches $S1$ to $S4$ are off, and the modulator operates in the normal mode. Fig. 2(a) and (b) shows the DfDT circuit states in the two nonoverlapped phases. During Φ_1, the sampling capacitors C_{S+} and C_{S-} sample the analog inputs V_{i+} and V_{i-}, respectively. During Φ_2, the sampled charge will be integrated by the first integrator. In other words, the analog stimulus source sends a total charge of

$$C_S V_i(n) \tag{1}$$

to the first integrator in the nth cycle, where $V_i \equiv V_{i+} - V_{i-}$ and $C_S \equiv C_{S+} = C_{S-}$.

Setting $T = 1$ will turn off the switches SA and SB and makes the modulator operate in the test mode. Now, the sampling capacitors C_{S+} and C_{S-} samples the reference voltages V_{R+} and V_{R-}, respectively. The sampled charge will be integrated by the first integrator during Φ_2 according to the value of D_i, where $D_i \in \{1, 0\}$.

Fig. 2(c) and (d) shows the DfDT circuit states in both phases. Let $V_R \equiv V_{R+} - V_{R-}$, the first integrator in the test mode accepts total charge of

$$C_S V_R \left(2D_i(n) - 1\right) \tag{2}$$

in the nth cycle.

Comparing (1) with (2), it is clear that the required high-performance embedded ASG for testing purpose can be realized by reconfiguring the DfDT structure as a one-bit digital-to-charge converter (DCC) in the test mode. The reconfigured SC DCC is then controlled by a repetitively applied digital stimulus D_i and generates the required high-quality analog test stimuli. The digital stimulus is synthesized by a digital bit-stream generator (BSG) which is a single-bit $\Sigma-\Delta$ modulator made of either software or hardware [16]. The single-bit characteristic of the DCC ensures that the generated stimuli have no nonlinearity issue. Since both normal and test modes have the same signal paths, the inherent nonlinearity of the circuits has similar impacts on the modulator's outputs. The digital stimuli, thereby, are potentially able to provide compatible measurement results with those of conventional analog tests.

A. Analysis of the DfDT MUT

To analyze the DfDT MUT, the signal-flow-graph-analysis method [19] was adopted. Each of the switched capacitor shown in Fig. 1 can be modeled as if it has a transfer function of $C_k z^{-1}$, where C_k represents the capacitance value it consists of. If the input of the switched capacitor is a dc voltage, the transfer function reduces to C_k. To simplify the expressions, let us define $C_{I1} = C_{I1+} = C_{I1-}$, $C_{I2} = C_{I2+} = C_{I2-}$, $C_{Y1} = C_{Y1+} = C_{Y1-}$, $C_{Y2} = C_{Y2+} = C_{Y2-}$, and $C_{M2} = C_{M2+} = C_{M2-}$. We also define the normalized binary digital signals Y_i and Y_o as

$$\begin{aligned} Y_i &= 2D_i - 1 \\ Y_o &= 2D_o - 1 \end{aligned} \tag{3}$$

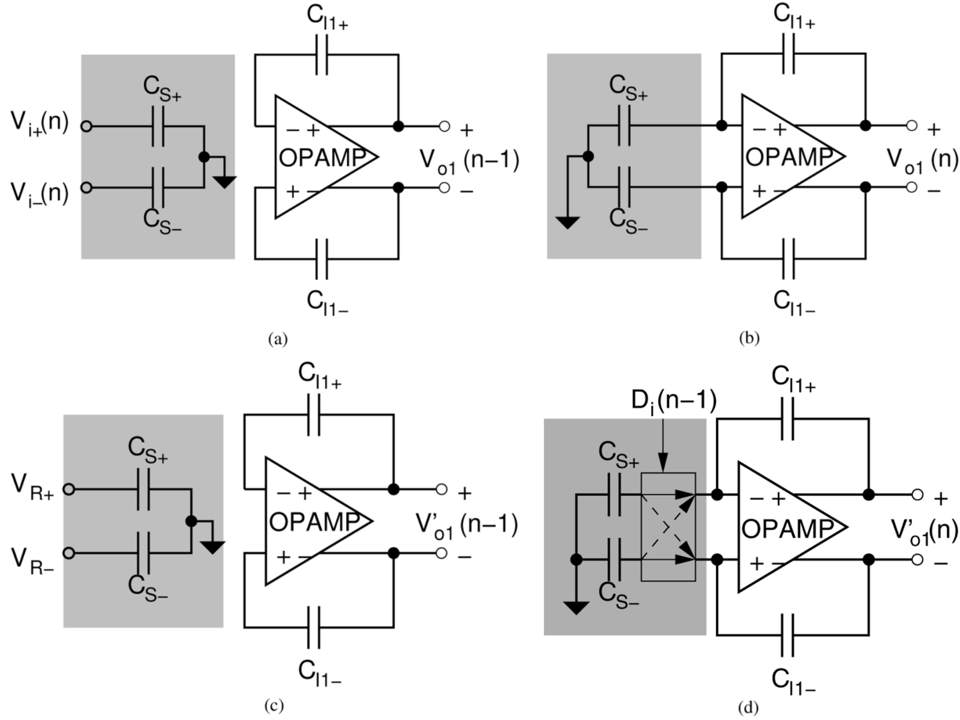

Fig. 2. Circuit operation of the DfDT circuits and the first summing integrator in both modes. The DfDT circuits are highlighted in the shaded area. (a) During active Φ_1 in the normal mode. (b) During active Φ_2 in the normal mode. (c) During active Φ_1 in the test mode. (d) During active Φ_2 in the test mode.

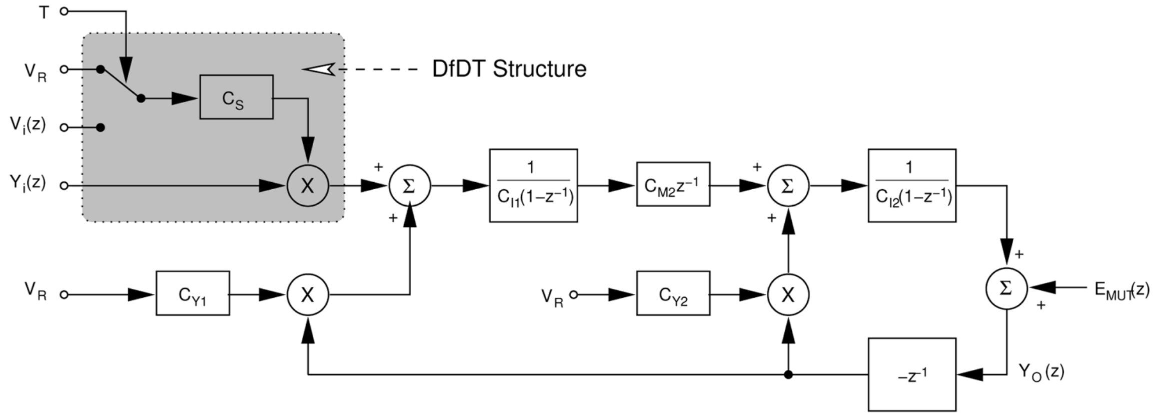

Fig. 3. Signal flow graph of the DfDT second-order $\Sigma-\Delta$ modulator.

whose values are either 1 or -1 instead of 1 or 0. By assuming that the quantization noise is white and additive, the comparator can be modeled as a quantization noise source $E_{\rm MUT}(z)$. The complete signal flow graph of the DfDT second-order $\Sigma-\Delta$ modulator is shown in Fig. 3.

The I/O relationship of the test-mode-enabled MUT can be easily derived according to Fig. 3. The result is

$$Y_o(z)=\frac{\frac{C_S C_{M2}}{C_{I1}C_{I2}}}{\mathrm{DEN}(z)}z^{-1}Y_i(z)+\frac{(1-z^{-1})^2}{\mathrm{DEN}(z)}\frac{E_{\rm MUT}(z)}{V_R} \quad (4)$$

where

$$\mathrm{DEN}(z)=1-\left(2-\frac{C_{Y2}}{C_{I2}}\right)z^{-1}+\left(1-\frac{C_{Y2}}{C_{I2}}-\frac{C_{Y1}C_{Y2}}{C_{I1}C_{I2}}\right)z^{-2}. \quad (5)$$

For convenience, (4) is usually normalized with respect to V_R and can be rewritten as

$$Y_o(z)=\mathrm{STF}_{\rm MUT}(z)Y_i(z)+\mathrm{NTF}_{\rm MUT}(z)E_{\rm MUT}(z). \quad (6)$$

Since $Y_i(z)$ is the output of a digital $\Sigma-\Delta$ modulator, it has a similar I/O relationship to (6) which is expressed as

$$Y_i(z)=\mathrm{STF}_{\rm BSG}(z)X_{\rm BSG}(z)+\mathrm{NTF}_{\rm BSG}(z)E_{\rm BSG}(z). \quad (7)$$

In (6) and (7), $\mathrm{STF}_{\rm BSG}(z)$ and $\mathrm{STF}_{\rm MUT}(z)$ stand for the signal transfer functions (STFs), $\mathrm{NTF}_{\rm BSG}(z)$ and $\mathrm{NTF}_{\rm MUT}(z)$ are the noise transfer functions (NTFs), and $E_{\rm BSG}(z)$ and $E_{\rm MUT}(z)$ symbolize the quantization noises of the BSG and

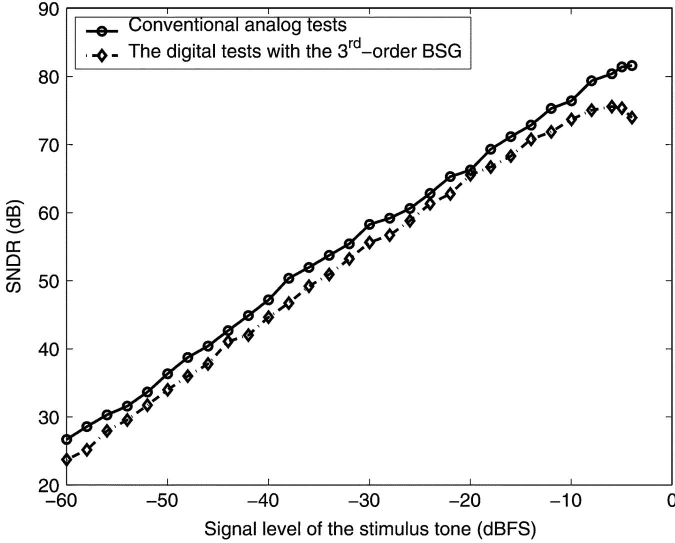

Fig. 4. Measured SNR of the DfDT $\Sigma-\Delta$ modulator shown in Fig. 1, [17].

MUT, respectively. Substituting the $Y_i(z)$ in (6) with (7), the I/O relationship of the test-mode-enabled MUT is derived to be

$$\begin{aligned} Y_o(z) = &\mathrm{STF_{MUT}}(z)\mathrm{STF_{BSG}}(z)X_{\mathrm{BSG}}(z) \\ &+ \mathrm{STF_{MUT}}(z)\mathrm{NTF_{BSG}}(z)E_{\mathrm{BSG}}(z) \\ &+ \mathrm{NTF_{MUT}}(z)E_{\mathrm{MUT}}(z). \end{aligned} \tag{8}$$

Note that both quantization noise sources are respectively shaped by their NTFs. These noise-shaping terms attenuate most of the quantization noise power out of the passband. Intuitively, if the two shaped noise were uncorrelated and we make

$$|\mathrm{STF_{MUT}}(z)\mathrm{NTF_{BSG}}(z)E_{\mathrm{BSG}}(z)| \ll |\mathrm{NTF_{MUT}}(z)E_{\mathrm{MUT}}(z)| \tag{9}$$

in the passband, then the passband response of the test-mode-enabled MUT could be approximated by

$$Y_o(z) \simeq \mathrm{STF_{MUT}}(z)\mathrm{STF_{BSG}}(z)X_{\mathrm{BSG}}(z) + \mathrm{NTF_{MUT}}(z)E_{\mathrm{MUT}}(z). \tag{10}$$

Equation (10) is similar to that of the MUT operating in the normal mode. It implies that the digital stimuli may have similar responses to their analog counterparts in the passband. As a result, the DfDT MUT may be accurately tested by the digital stimuli. The requirement of (9) can be met by selecting a suitable BSG structure such as a higher order $\Sigma-\Delta$ modulator.

B. Root Causes of the SNR Degradation in Digital Tests

However, the measurement data shown in Fig. 4 indicate that the DfDT MUT reported somewhat lower SNRs with the digital stimuli than with their analog counterparts [17]. The differences are more significant when the signal level of the stimulus tone becomes higher. Since the only difference between the analog stimulus and the digital one is the shaped noise generated by the BSG, it concludes that the additional shaped noise in the digital stimulus leads to the MUT's SNR degradation in the test mode. In fact, two mechanisms including the shaped-noise correlation between the BSG and MUT and the modulator overload degrade the test accuracy using the digital stimuli. We will explain about them in the following.

1) Shaped-Noise Correlation: An essential assumption in deriving (10) is that the shaped noises $\mathrm{NTF_{MUT}}(z)E_{\mathrm{MUT}}(z)$ and $\mathrm{STF_{MUT}}(z)\mathrm{NTF_{BSG}}(z)E_{\mathrm{BSG}}(z)$ were uncorrelated. If the correlation exists, the total in-band shaped noise power will be higher than the sum of those calculated from each term [20]. Unfortunately, the shaped-noise correlation does exist. The reason is that both the quantization noise sources are high-pass filtered by their noise-shaping terms; consequently, the two shaped noises have similar spectra. Since the correlation between two random processes indicates how similar they are, the two shaped noises are correlated to some degree. Its significance depends upon the circuit design of the MUT and the tests.

No analytical method can well predict the shaped-noise correlation due to the nonlinear nature of practical $\Sigma-\Delta$ modulation loops. Only behavioral simulations with a suitable behavioral model give us reliable predictions. The fully settled linear behavioral plus noise (FSLB+N) model is such a model [21]. It has been shown to be able to precisely predict the SNR performance of the DfDT MUT in the range of 0.05−−2.2 dB, no matter what mode the MUT operates in [21]. In the rest of this paper, all behavioral simulations are conducted with the FSLB+N model.

2) Modulator Overload: Another mechanism which degrades the tested SNRs of the MUT by the digital stimuli is that the MUT may be overloaded when the input power is high. Recall that $\Sigma-\Delta$ modulators produce pulse-density-modulated bit-stream outputs; in other words, the signal level of the input sample is represented by the output's pulse density. Since the maximum pulse density is one, there is a signal-level limit of the input that the MUT can accept without performance degradation. A more general view of this criterion is from a power perspective. Because the output power of the MUT is limited, the sum of the input power and the shaped quantization noise power has an upper bond. That is

$$P_{qn} + P_{\mathrm{inmax}} \leq P_{\mathrm{bond}} \tag{11}$$

where P_{bond} represents the upper bond, P_{inmax} stands for the maximum input power allowed, and P_{qn} symbolizes the total shaped quantization noise power of the MUT accumulated from dc to half the sampling rate. Let Δ be the quantization step and assume that the quantization noise $E_{\mathrm{MUT}}(z)$ were uniformly distributed and uncorrelated to the input, it can be shown that

$$P_{qn} = \frac{\Delta^2}{12}\mathrm{NPG}. \tag{12}$$

The NPG above is named as the noise power gain of the MUT which is defined as

$$\mathrm{NPG} = \frac{1}{\pi}\int_0^{\pi} |\mathrm{NTF_{MUT}}(j\omega)|^2 \, d\omega. \tag{13}$$

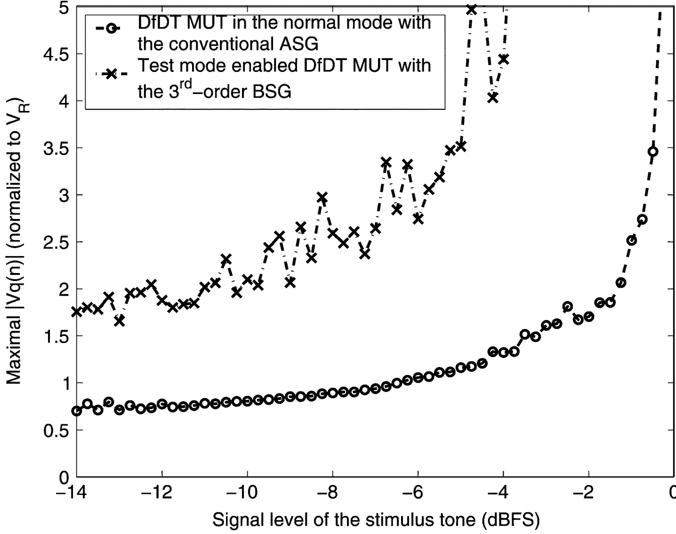

Fig. 5. Maximum $|V_q(n)|$ of the DfDT MUT versus the signal level of the stimulus tone.

By (12) and normalizing P_{bond} and P_{inmax} to the full-scale input power $\Delta^2/8$, (11) can be rewritten to be

$$\text{NPG} \leq 1.5P_{\text{bond}}^N - 1.5P_{\text{inmax}}^N. \tag{14}$$

The notations P_{bond}^N and P_{inmax}^N denote that these values are normalized. Similar criteria can be found in designing general Σ–Δ modulators. For instance,[22] uses the following normalized equation as a criterion to design the NPG:

$$\text{NPG} \leq C_{\text{SDM}} - 3P_{\text{inmax}}^N. \tag{15}$$

Here, C_{SDM} is a constant depending on the structure of the target modulator design.

Although (15) is not an analytical result but an empirical conclusion based on observing the results of many simulations, it is quite similar to (14). The difference between (14) and (15) comes from the discrepancy between theory and practice. When deriving (14), the quantization noise was assumed to be uncorrelated to the input. In practice, they do have some correlation. Therefore, some modifications are necessary to compromise with the correlation.

For the DfDT MUT operating in the test mode, its input contains the test stimulus as well as the additional shaped noise generated by the BSG. As a result, the digital stimulus has higher power than its analog counterpart. According to (11), the higher stimulus power is more likely to overload the MUT.

To find out when the DfDT MUT will be overloaded, Fig. 5 shows the simulation results of the maximal $|V_q(n)|$ versus the signal level of the stimulus tone, where $|V_q(n)|$ denotes the absolute value of the input voltage of the MUT's quantizer. The pure analog sinusoidal stimuli and the third-order digital stimuli are examined.

A $\Sigma-\Delta$ modulator is said to be overloaded if it produces a quantization noise out of $\pm\Delta/2$. For the design example, the MUT is overloaded if any one of its $|V_q(n)|$ is larger than $2V_R$. According to Fig. 5, the MUT operating in the normal mode is overloaded when the signal level of the analog stimulus is larger than -1.5 dBFS. Once the MUT is overloaded, the approximation that the quantization noise has a uniform distribution is getting worse. The total harmonic distortion plus noise (THD+N) power in the passband thus increases. Consequently, the peak SNR of the MUT does not appear at 0-dBFS input but somewhere between 0 and -1.5 dBFS. On the other hand, the DfDT MUT operating in the test mode is overloaded at a stimulus level as low as -10 dBFS. It explains why the measured SNR curve with the digital stimuli in Fig. 4 bends down at the high stimulus levels.

III. Decorrelating DfDT $\Sigma-\Delta$ Modulator

In order to alleviate the impairment effects of the shaped-noise correlation and modulator overload, an intuitive way is to reduce the shaped noise $\text{NTF}_{\text{BSG}}(z)E_{\text{BSG}}(z)$ of the digital stimulus. Since the BSG's quantization noise is high-pass shaped, adding a low-pass filter (LPF) to the MUT by some means to filter the digital stimuli would enhance the test accuracy using the digital stimuli.

A. Schematic of the Decorrelating DfDT Second-Order $\Sigma-\Delta$ Modulator

Fig. 6 shows the schematic of the proposed D^{3}T second-order $\Sigma-\Delta$ modulator which can provide the required LPF feature for the digital stimuli. It is modified from Fig. 1 by splitting the DfDT circuits into two identical ones. Each of them can be considered as a sub-DCC in the test mode.

There are also two operation modes. In the normal mode, the test-mode control pin T is set to zero and the stimulus input pins $D_{ij}(z), j \in \{0,1\}$ are fixed on one. The switches $S1_j$ to $S4_j$, $j \in \{0,1\}$, are turned off as a consequence. The whole D^{3}T MUT behaves as a normal second-order $\Sigma-\Delta$ modulator.

When operating in the test mode, the test-mode control pin T is set to one, thus turning off the switches SA_j and SB_j where $j \in \{0,1\}$. The sampling capacitors $C_{S0+}, C_{S0-}, C_{S1+}$, and C_{S1-} now sample the reference voltages V_{R+} and V_{R-}, respectively. The stored charge is then transferred to the integration capacitors C_{I1+} and C_{I1-} through either the switches $S3_j$ and $S4_j$ or SC_j and SD_j, depending on the digital stimuli $D_{ij}(z)$. The rest of the MUT circuits keep the same operation as if they were in the normal mode. The proposed scheme reuses and excites all the components of the $\Sigma-\Delta$ modulator in the test mode, except for the four switches SA_0, SA_1, SB_0, and SB_1. Since there is no noise margin for analog signals, every faulty effect of the parametric and catastrophic faults of the stimulated components will propagate to the primary output. As a result, it achieves high fault observability.

In addition, the test configuration does not change the loading conditions of the OPAMPs, thus providing the MUT with the capability of conducting at-speed tests.

The hardware overhead only consists of 16 switches and some digital circuits to generate the control signals, showing that the D^{3}T scheme is a low-cost approach. Besides, the function of a switch (turning on and off) is quite insensitive to the process variation, hence the extra circuits for testing purpose have negligible impact on the functional yield. Process variation may alter the turn-on resistances of the switches and result in a different

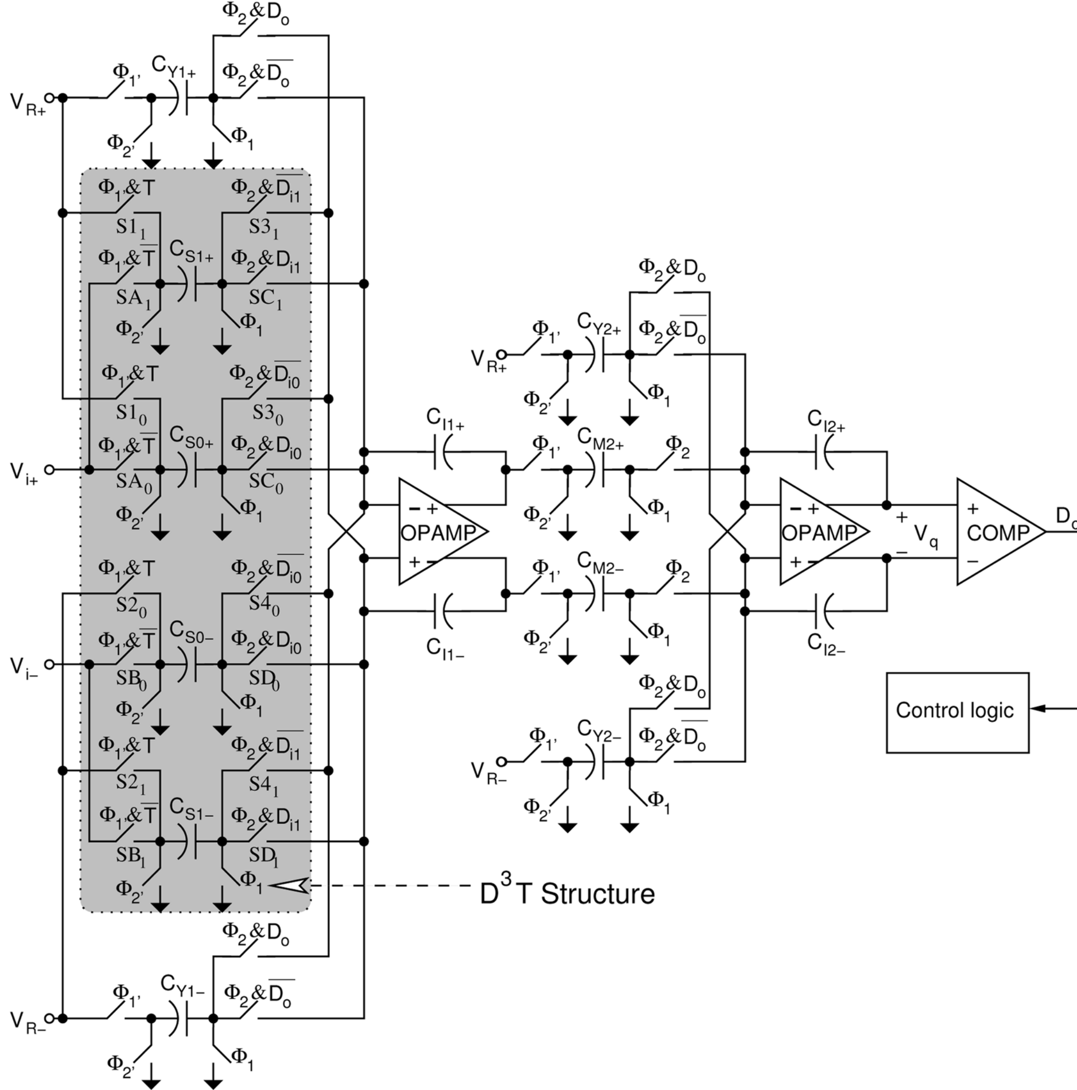

Fig. 6. Schematic of the proposed $\mathrm{D}^3\mathrm{T}$ second-order $\Sigma-\Delta$ modulator.

maximum operating speed. This issue can be addressed by designing the switches with suitable design margins or identified by the permissible at-speed tests.

B. Analysis of the MUT

Fig. 7 shows the signal flow graph of the $\mathrm{D}^3\mathrm{T}$ second-order $\Sigma-\Delta$ modulator in the test mode. The shaded area points out the signal flow graph of the $\mathrm{D}^3\mathrm{T}$ circuits. In fact, it is a combination of two copies of the shaded area as shown in Fig. 3. According to this figure, the normalized I/O relationship of test-mode-enabled $\mathrm{D}^3\mathrm{T}$ MUT can be derived to be

$$\begin{aligned} Y_o(z) = {} & \mathrm{STF}_{\mathrm{MUT0}}(z)Y_{i0}(z) \\ & + \mathrm{STF}_{\mathrm{MUT1}}(z)Y_{i1}(z) + \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z) \end{aligned} \quad (16)$$

where

$$\begin{aligned} Y_{ij}(z) = {} & \mathrm{STF}_{\mathrm{BSG}}(z)X_{\mathrm{BSG}j}(z) \\ & + \mathrm{NTF}_{\mathrm{BSG}}(z)E_{\mathrm{BSG}j}(z), \qquad j \in \{0,1\}. \end{aligned} \quad (17)$$

Let $Y_{i1}(z) = z^{-n}Y_{i0}(z)$ and $\mathrm{STF}_{\mathrm{MUT0}}(z) = \mathrm{STF}_{\mathrm{MUT1}}(z) = \mathrm{STF}_{\mathrm{MUT}}(z)/2$, then (16) can be rewritten to be

$$Y_o(z) = \mathrm{STF}_{\mathrm{MUT}}(z)\frac{1+z^{-n}}{2}Y_{i0}(z) + \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z) \quad (18)$$

where n is the relative input delay between the two digital stimuli. Choosing $Y_{i0}(z) = Y_i(z)$, we have

$$\begin{aligned} Y_o(z) = {} & \frac{(1+z^{-n})}{2}\mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{STF}_{\mathrm{BSG}}(z)X_{\mathrm{BSG}}(z) \\ & + \frac{(1+z^{-n})}{2}\mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{NTF}_{\mathrm{BSG}}(z)E_{\mathrm{BSG}}(z) \\ & + \mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z). \end{aligned} \quad (19)$$

Comparing (19) with (8), an additional finite-impulse-response (FIR) LPF term $(1+z^{-n})/2$ is formed to filter out some shaped noise of the digital stimulus. In the meantime, the stimulus tone is not affected since the term $(1+z^{-n})/2$ has a low-pass response and a dc gain of one. The requirement of $\mathrm{STF}_{\mathrm{MUT1}}(z) = \mathrm{STF}_{\mathrm{MUT0}}(z) = \mathrm{STF}_{\mathrm{MUT}}(z)/2$ can be

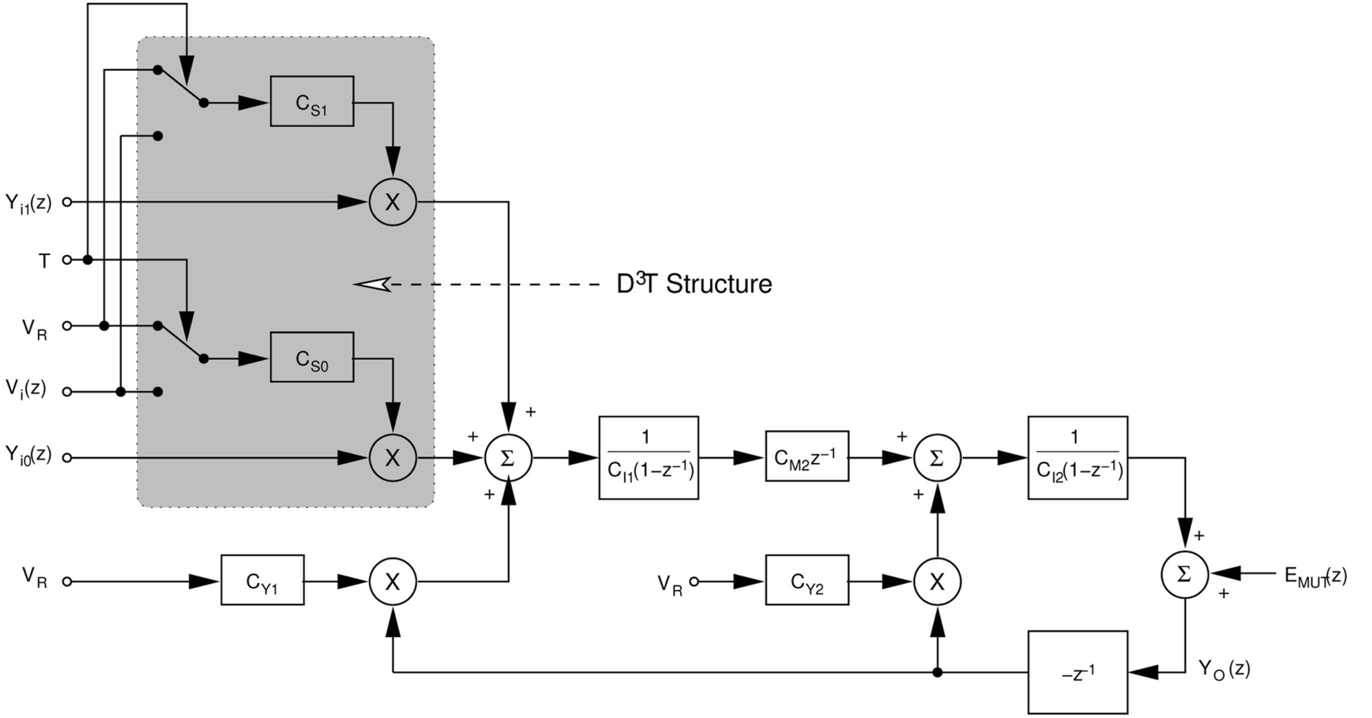

Fig. 7. Signal flow graph of the proposed $\mathrm{D}^3\mathrm{T}$ second-order $\Sigma-\Delta$ modulator.

easily fitted in by choosing $C_{S0+} = C_{S1+} = C_{S0-} = C_{S1-} = C_S/2$.

IV. Design of the Decorrelating DfDT Scheme

The proposed $\mathrm{D}^3\mathrm{T}$ scheme can be extended to a more general structure. Several design parameters such as the decomposition number, the decomposition factor, the relative input delay, and the BSG structure can be designed in order to acquire the most accurate result of a test. In the following, we use the second-order $\Sigma-\Delta$ modulator example to discuss the design of the $\mathrm{D}^3\mathrm{T}$ MUT.

A. Decomposition Number

By applying a FIR LPF term with more taps, more shaped-noise power of the digital stimulus can be attenuated [23]. Hence, the digital stimulus becomes more similar to its analog counterpart. The required decorrelating LPF term can be realized by decomposing the input SC network into more sub-DCC networks. However, increasing the decomposition number of the sub-DCC networks runs the risk of inducing more in-band thermal noise power. Let N and C_S be the decomposition number and the input sampling capacitance in the normal mode, respectively, and let C_S be evenly decomposed into N sub-DCC networks. The total in-band thermal noise power induced by the input sampling capacitor is $(KT)/(C_S \cdot \mathrm{OSR})$ in the normal mode, but each sub-DCC network causes $(NKT)/(C_S \cdot \mathrm{OSR})$ total in-band thermal noise power in the test mode. If these sub-DCC networks operated independently, the total in-band thermal noise power in the test mode induced by the $\mathrm{D}^3\mathrm{T}$ structure would be as high as $(N^2KT)/(C_S \cdot \mathrm{OSR})$. The increased thermal noise power might significantly diminish the test accuracy. For example, if $N = 4$, then the measured SNR of the MUT in the test mode may be 12 dB worse, even if there were neither shaped-noise correlation nor modulator-overload impairment in the test. As a result, it is suggested that the decomposition number should be kept as small as possible.

The appropriate decomposition number can be designated through extensive behavioral simulations. We take two as the decomposition number in our design example because of its simpler circuit implementation and satisfying accuracy.

B. Decomposition Factor

Generally speaking, it is not necessary to decompose the input sampling capacitor into two identical ones. Structurally, the general relationship between $\mathrm{STF}_{\mathrm{MUT0}}(z)$, $\mathrm{STF}_{\mathrm{MUT1}}(z)$, and $\mathrm{STF}_{\mathrm{MUT}}(z)$ can be expressed as

$$\mathrm{STF}_{\mathrm{MUT0}}(z) + \mathrm{STF}_{\mathrm{MUT1}}(z) = \mathrm{STF}_{\mathrm{MUT}}(z). \tag{20}$$

Defining the decomposition factor γ as

$$\gamma = \frac{C_{S0}}{(C_{S0} + C_{S1})} \tag{21}$$

will return $\mathrm{STF}_{\mathrm{MUT0}}(z) = \gamma \mathrm{STF}_{\mathrm{MUT}}(z)$ and $\mathrm{STF}_{\mathrm{MUT1}}(z) = (1-\gamma)\mathrm{STF}_{\mathrm{MUT}}(z)$. The I/O relationship of the $\mathrm{D}^3\mathrm{T}$ MUT in the test mode thereby becomes

$$\begin{aligned} Y_o(z) = &(\gamma + (1-\gamma)z^{-n})\mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{STF}_{\mathrm{BSG}}(z)X_{\mathrm{BSG}}(z) \\ &+(\gamma + (1-\gamma)z^{-n})\mathrm{STF}_{\mathrm{MUT}}(z)\mathrm{NTF}_{\mathrm{BSG}}(z)E_{\mathrm{BSG}}(z) \\ &+\mathrm{NTF}_{\mathrm{MUT}}(z)E_{\mathrm{MUT}}(z). \end{aligned} \tag{22}$$

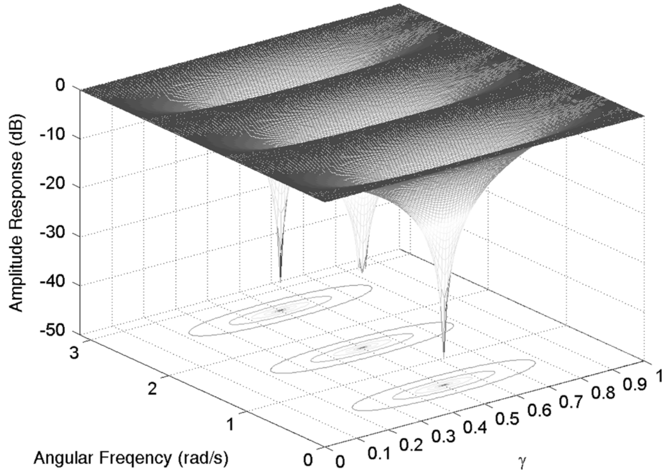

Fig. 8. Shaped-noise attenuation versus decomposition factor γ.

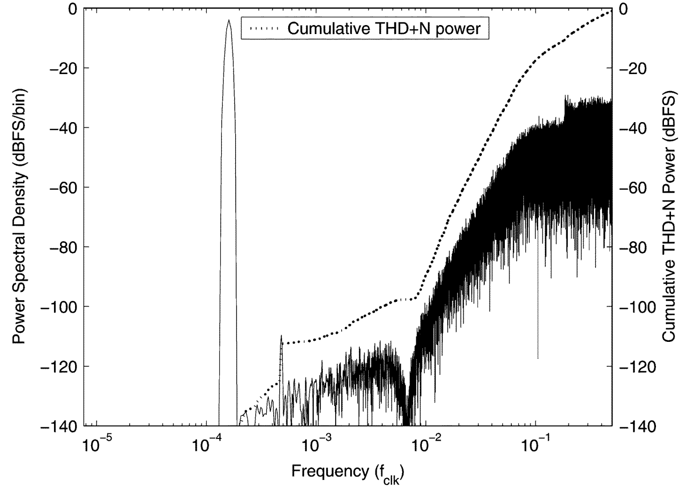

Fig. 9. Spectrum of the −4-dBFS digital stimulus generated by the third-order BSG.

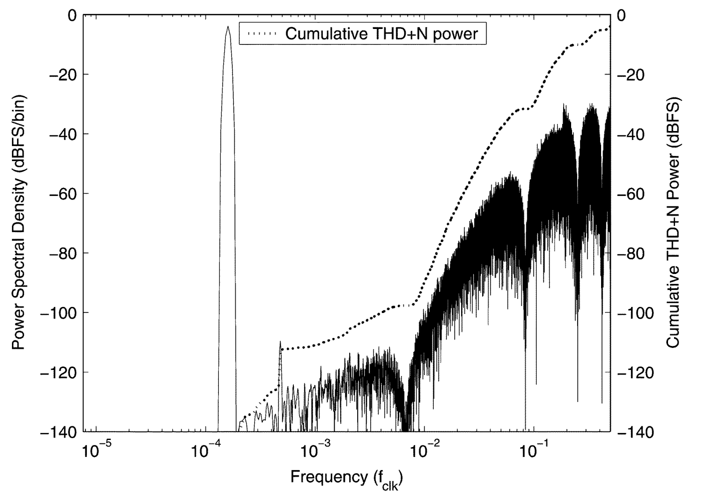

Fig. 10. Spectrum of the equivalent stimulus of the $\mathrm{D}^3\mathrm{T}$ MUT operating in the test mode where $n = 6$.

According to the equation given above, the general decorrelating LPF term associated with the digital stimulus is

$$\gamma + (1 - \gamma)z^{-n}. \tag{23}$$

Equation (23) has a flat unit-gain frequency response at low frequencies (close to $z^{-n} = 1$). Consequently, the in-band frequency response of the test stimulus $X_{\mathrm{BSG}}(z)$ is very similar to that in the normal mode.

To find out the suitable decomposition factor γ, recall that our original objective of adding the decorrelating LPF term is to filter out as much shaped-noise power of the digital stimulus as possible. It is instructive to check the relationship between γ and the attenuation capability of (23). Fig. 8 shows the results. The relative input delay n is set to six here. Obviously, $\gamma = 0.5$ achieves the maximum attenuation for this design. The result can be interpreted as that, to maximize the noise attenuation in certain frequency range, the most effective way is to put some real zeros in it because an FIR filter cannot provide any pole [23]. Equation (23) provides zeros on the unit circle of z-domain if and only if $\gamma = 0.5$. Fig. 8 also shows that the $\mathrm{D}^3\mathrm{T}$ scheme tolerates moderate capacitor mismatch. Capacitor mismatch between the spilt-sampling capacitors C_{S0} and C_{S1} may cause γ somewhat deviating from 0.5. Even though, the shaped noise of the digital stimulus can still be effectively attenuated.

C. Relative Input Delay

The last design parameter needed to be determined is the relative input delay n between the two digital stimuli. The design scenario here is trying to put real zeros on certain frequencies to remove as much shaped-noise power of the digital stimulus as possible. A larger n puts more zeros on different frequencies, but the effective attenuation band of each zero becomes narrower.

In practice, the selection of a suitable n is quite complicated because of the nonlinear nature of $\Sigma{-}\Delta$ modulation loops. Fig. 9 shows the spectrum of the −4-dBFS digital stimulus generated by the third-order BSG used in [17]. There are lots of significant spurs at the frequencies higher than one-fifth the sampling rate that are not revealed by (7). Putting a zero nearby these dominant spurs would be a more effective way to cut down the shaped-noise power. However, the spectral distribution of the spurs depends on the structure of the BSG as well as the signal level and frequency of the stimulus tone. Hence, we conducted extensive behavioral simulations to demonstrate that there is an appropriate n with which the digital test can reveal the highest SNR of the MUT. The results will be presented in Section V.

Fig. 10 shows the spectrum of the equivalent stimulus of the $\mathrm{D}^3\mathrm{T}$ MUT in the test mode. The two digital stimuli, D_{i0} and D_{i1}, are the same as that shown in Fig. 9 except for a relative input delay of six. High-frequency noise and spurs are effectively attenuated. Its shaped noise therefore bears less resemblance to that of the MUT. As a consequence, the shaped-noise correlation becomes less.

Comparing both cumulative THD+N power plots as shown in Figs. 9 and 10 with each other, the total shaped-noise power of the digital stimulus is reduced by 3 dB using the $\mathrm{D}^3\mathrm{T}$ scheme. Consequently, the maximal level of the stimulus tone without overloading of the $\mathrm{D}^3\mathrm{T}$ MUT extends to be higher than

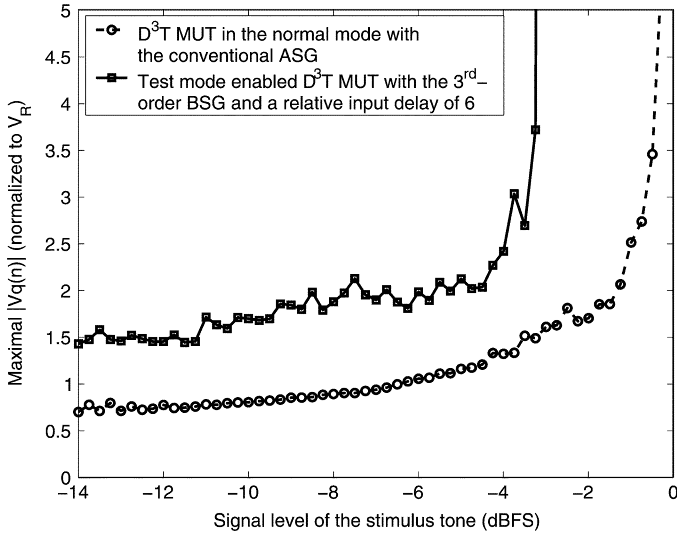

Fig. 11. Maximum $|V_q(n)|$ of the $\mathrm{D^3T}$ MUT versus the signal level of the stimulus tone.

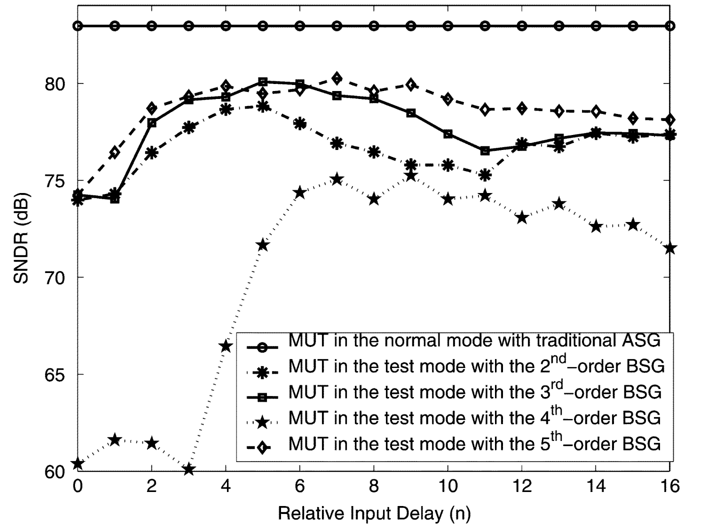

Fig. 12. Simulated SNR results of the $\mathrm{D^3T}$ MUT with various stimulus generators and relative input delays.

-5 dBFS, as shown in Fig. 11. The test-mode-enabled $\mathrm{D^3T}$ MUT thus achieves high test accuracy even at high stimulus levels.

V. Simulation Results

To verify the $\mathrm{D^3T}$ scheme, behavioral simulations with the FSLB +N model of the design example were conducted first. All necessary circuit parameters were according to the design of [17]. The OPAMPs were assumed having an offset voltage of 0.41 mV, an open-loop gain of 75 dB, and an output swing of ± 2.8 V. All transient responses were assumed to be fully settled. The thermal noise induced by the switched capacitors was also included. The frequency of the test stimulus was set to 21/128 K times the sampling rate. Since the test accuracy of the digital stimulus is getting worse at a higher stimulus level, the signal level of the stimulus tone was set to -4 dBFS unless otherwise noted.

In addition to the second-order BSG candidate whose structure is the same as that of the MUT, three high-order BSG candidates were adopted from [22] to justify the importance of selecting a suitable BSG. They are the third- and fifth-order feedforward single-bit $\Sigma-\Delta$ modulators and the fourth-order multiple-feedback one.

A. Selection of the Relative Input Delay, BSG, and Decomposition Number

According to (19), the maximum allowable n is limited by the decorrelating LPF term, $(1+z^{-n})/2$, in the STF of the test stimulus $X_{\mathrm{BSG}}(z)$. A too large n will significantly distort the stimulus tone's response. Therefore, we only examine the n less than 17. Fig. 12 shows the simulation results.

The $\mathrm{D^3T}$ $\Sigma-\Delta$ modulator $(n \neq 0)$ achieves better results than the original DfDT design $(n = 0)$. Depending on the selected BSG structure, the optimal relative input delay is in the range of four to nine. Further increasing the relative-input-delay value does not improve the test accuracy. As has been discussed, a high relative-input-delay value narrows the attenuation band of each zero, thus some significant spurs may not be effectively attenuated. Behavioral simulations are thereby substantial to determine an adequate design using the $\mathrm{D^3T}$ scheme.

The combination of the fifth-order BSG with a relative input delay $n = 7$ achieves the best test result, which is 80.2 dB. It is 6.3 dB better than that of the original DfDT scheme. The best test setup may be different when a different test stimulus or a different MUT is applied.

The second-order BSG performs worse than the third- and fifth-order BSGs, owing to its insufficient in-band attenuation capability, as we would expect according to (4). Surprisingly, the fourth-order BSG provides the worst result in this case, even worse than the second-order one. It is because the selected fourth-order BSG leaves the $\mathrm{D^3T}$ MUT too much shaped-noise power in the test, even with the help of the decorrelating LPF term. As a consequence, the MUT is severely overloaded. Although the fourth-order BSG is superior to the second-order one at low stimulus levels as shown in Table I, it is not suitable for the test which requires the -4-dBFS stimulus tone. It indicates that selecting a suitable BSG structure for a specified test is necessary.

Finally, since the test accuracy of using the digital stimulus is already within 3.1 dB for the design example, the improvement headroom by increasing the decomposition number N of the $\mathrm{D^3T}$ scheme is limited, while it costs more hardware overhead. Hence, we only discuss the cases in which the decomposition number is two.

B. Test Accuracy

Table I lists the simulated SNR results of the $\mathrm{D^3T}$ MUT with various stimulus generators. The digital stimuli are applied to the MUT with the same relative input delay which is six. The results show that the digital stimuli are as linear as their analog counterparts.

The overall test errors, defined as the differences between the SNRs obtained by the digital stimuli and those of their analog

TABLE I
SIMULATED SNR RESULTS (in decibels) OF THE D^3T MUT WITH VARIOUS STIMULUS SOURCES

Stimulus Level (dBFS)	Conventional ASG	The 2nd-order BSG	The 3rd-order BSG	The 4th-order BSG	The 5th-order BSG
-60.0	28.1	25.1	26.9	27.0	27.3
-58.0	30.0	26.5	28.9	28.8	29.3
-56.0	31.3	28.9	30.7	31.0	30.5
-54.0	33.1	31.9	32.3	33.2	33.2
-52.0	35.4	33.5	34.0	34.3	34.9
-50.0	36.3	34.5	36.7	37.6	36.8
-48.0	38.3	37.1	38.3	40.1	38.9
-46.0	40.2	39.1	40.5	41.0	41.2
-44.0	42.8	41.2	42.6	43.5	42.8
-42.0	46.1	44.1	44.8	45.1	46.0
-40.0	48.3	45.8	46.9	47.2	47.7
-38.0	50.0	47.8	48.4	48.4	48.5
-36.0	51.4	49.4	51.1	51.5	51.5
-34.0	54.6	51.4	52.7	53.1	53.1
-32.0	56.0	54.1	54.8	55.5	55.5
-30.0	57.8	56.1	57.3	57.7	56.9
-28.0	60.9	59.0	59.4	59.3	59.5
-26.0	62.1	60.2	61.0	61.0	60.9
-24.0	64.5	62.1	62.7	62.6	63.5
-22.0	66.7	64.6	65.6	64.1	65.8
-20.0	67.8	66.4	67.5	67.1	67.1
-18.0	70.0	68.0	68.9	69.2	69.5
-16.0	72.3	69.8	71.9	70.1	71.6
-14.0	74.7	71.9	73.3	72.9	73.5
-12.0	76.3	73.5	74.7	74.7	74.7
-10.0	77.8	75.5	76.7	77.0	76.8
-8.0	79.9	77.0	78.6	78.1	78.4
-6.0	81.1	78.4	79.7	79.2	80.0
-5.0	82.1	77.9	80.3	80.1	80.6
-4.0	83.0	78.5	79.8	75.1	79.9

counterparts, of the design examples with the third- and fifth-order BSGs are shown in Fig. 13.

For the low-stimulus-level tests (< -10 dBFS) where the shaped-noise correlation effect dominates, the original DfDT MUT with the third-order BSG has the worst test error of -3.4 dB. By applying the D^3T scheme, the modified MUT successfully decorrelates the shaped noises of the BSG and the MUT. The D^3T MUT achieves test errors no worse than -1.8 dB with the same stimuli applied to the original DfDT MUT.

The D^3T scheme improves the test accuracy of the digital stimuli not only at low stimulus levels but also at high stimulus levels where the overloading effect becomes significant. Take the same third-order BSG cases as examples, Fig. 13 shows that the original DfDT scheme has the worst test error of -5.7 dB for the test stimulus whose level is not higher than -5 dBFS. On

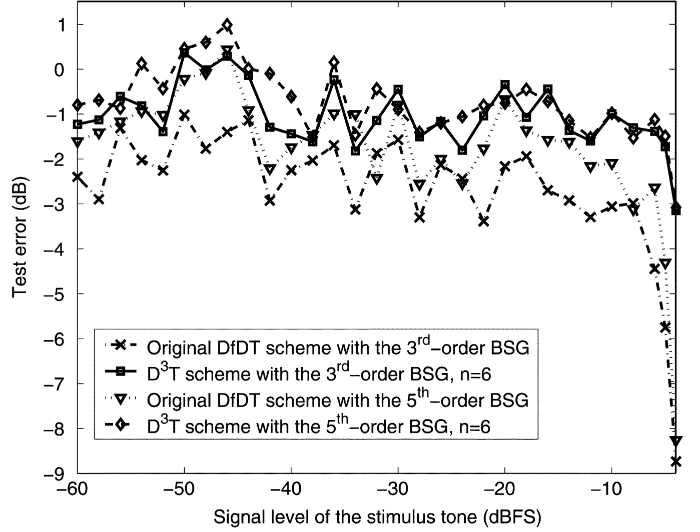

Fig. 13. Test errors of various test schemes.

the other hand, the test errors of the D^3T MUT are not worse than -1.8 dB within the same range. About 4-dB improvement is achieved, owing to that the D^3T MUT in the test mode has a higher overload limit of its stimulus level.

Even at -4 dBFS where the overload effect is the most significant, the test error of the test-mode-enabled D^3T MUT is still better than -3.1 dB. More than 5.5-dB improvement over the original DfDT scheme is achieved. Obviously, the D^3T scheme is superior to the original DfDT scheme for all kinds of tests.

C. Shaped-Noise Correlation and Modulator Overload

It is interesting to examine what happened to the MUT when the -4-dBFS test stimuli were applied. Figs. 14 and 15 show the output spectra of the MUT in both modes. The corresponding cumulative THD+N power plots are also shown.

Fig. 14 shows the output spectrum of the test with the conventional analog stimulus. In addition to the stimulus tone, the spectrum is composed of two types of noise. The thermal noise which has the property of a uniform distribution dominates at frequencies less than $f_{\mathrm{clk}}/256$ as shown by the flat noise floor. On the other hand, the shaped quantization noise dominates at higher frequencies due to the MUT's noise-shaping characteristic.

Each output spectrum of the digital tests shown in Fig. 15 can be divided into a thermal noise floor and also a shaped-noise part. However, the shaped-noise power of the DfDT scheme is higher than the proposed D^3T scheme. In fact, all simulations of Fig. 13 show that the shaped-noise power of the DfDT scheme is higher. Recall that higher shaped-noise correlation will lead to higher shaped-noise power. We conclude that the D^3T scheme does decorrelate the shaped noise of the digital stimulus and that of the MUT.

Comparing Figs. 14 with 15, the in-band noise of the D^3T test shows a great resemblance to that of the analog test. On the other hand, their shaped noises are still somewhat different. Fig. 16 shows the cumulative THD+N power plots of the three tests to gain more insights into the effects of the shaped-noise correlation. Every THD+N plot can be divided into a high-slope

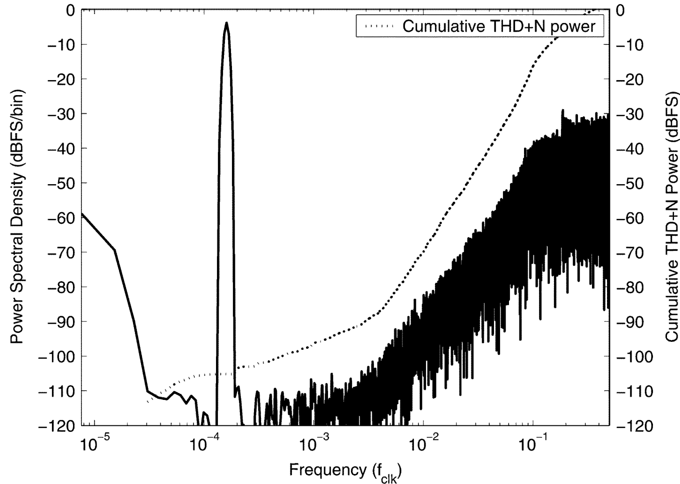

Fig. 14. Output spectrum of the $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator operating in the normal mode with the pure analog stimulus.

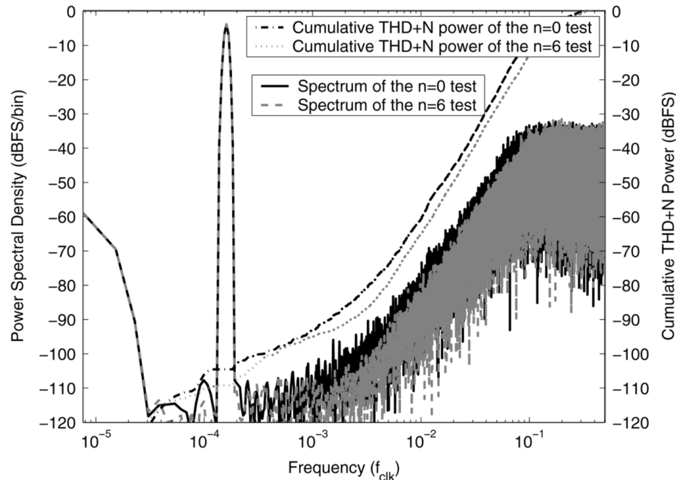

Fig. 15. Output spectra of the digital tests including the DfDT test $(n = 0)$ and the $\mathrm{D^3T}$ test with $n = 6$.

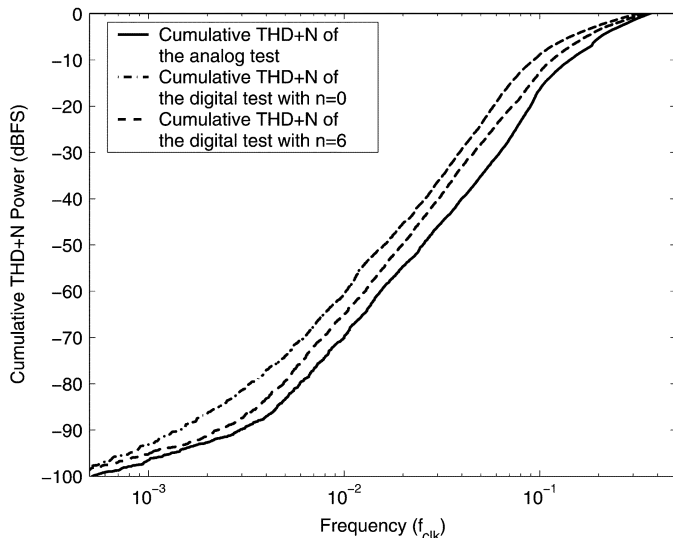

Fig. 16. Cumulative THD+N power plots of different tests.

TABLE II
CIRCUIT-SIMULATION RESULTS OF THE $\mathrm{D^3T}$ MUT

Test setup	SNR (dB)	SNDR (dB)	3rd Harmonic (dBFS)	5th Harmonic (dBFS)
Normal mode	75.4	65.8	-71.7	-83.5
Test mode				
n=0	72.3	71.6	-89.3	-91.1
n=1	72.1	67.7	-75.0	-90.3
n=2	72.3	70.9	-81.9	-99.5
n=3	72.4	70.6	-80.1	-98.9
n=4	73.1	69.4	-77.8	-86.2
n=5	73.2	70.4	-78.9	-95.0
n=6	71.9	69.9	-79.8	-91.7

segment and a low-slope segment. The shaped-noise dominates the high-slope segments while the thermal noise rules the low slope ones. The figure implies that the test errors are relative to the rated OSR of the MUT. For instance, the test error of the $\mathrm{D^3T}$ one in Fig. 15 is reduced from -3.1 to -1.1 dB if the OSR is increased from 128 to 256. It is because, at such an OSR, the SNR is mainly determined by the thermal noise. As a result, the shaped-noise correlation has no significant impact on the final SNR. Yet, the application determines the rated OSR and thus the test error.

D. *Circuit-Simulation Results*

In addition to the behavioral simulations, we also conducted circuit simulations in order to demonstrate the feasibility of the proposed $\mathrm{D^3T}$ scheme. The circuits shown in Fig. 6 has been simulated using HSPICE. The design adopted the same circuits used in [17] except for the $\mathrm{D^3T}$ structure. The OPAMPs were intentionally made somewhat asymmetric to induce them an offset of 4.7 mV. Due to the very long simulation time, we could only take 32 K output samples for each analysis. The same -5-dBFS sinusoidal stimulus tone with a frequency of 23/32K times the clock frequency was applied to all simulations. The master clock frequency, f_{clk}, was set to 25 MHz. Table II summarizes the circuit-simulation results.

Note that there are three major differences between the circuit simulations and the behavioral simulations. First, it is hard to include the thermal noise and flicker noise into the circuit simulations. These noise sources will dither the internal signals of the MUT and may impact on the results [21]. Second, our behavioral simulations assumed that the OPAMPs have linear gains, and their outputs will be hard clamped once they exceed the defined saturation voltages. Therefore, the behavioral simulation results contain less nonlinear information of the MUT. Lastly, the circuit simulations induce numerical errors while the behavioral simulations do not.

1) Testing SNR: The tested SNRs listed in Tables I and II are somewhat different. As explained earlier, the noise sources and test setups of the behavioral and circuit simulations are different. Consequently, the best relative input delay may be different. For our example, setting $n = 5$ results in the highest SNR which is

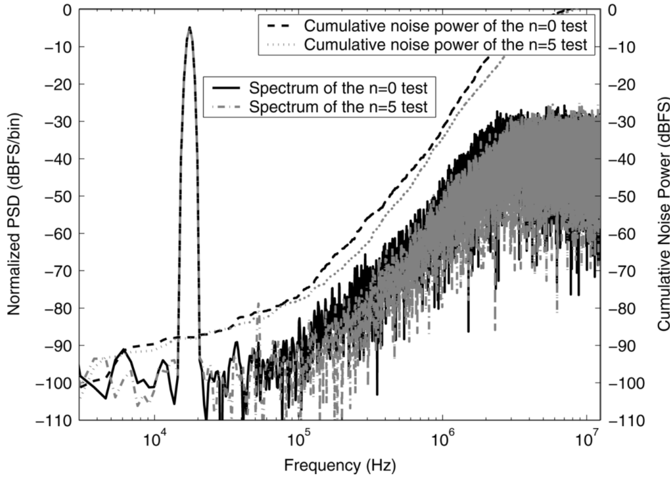

Fig. 17. Output spectra of the $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator operating in the test mode with the third-order digital stimulus and relative input delays of zero and five.

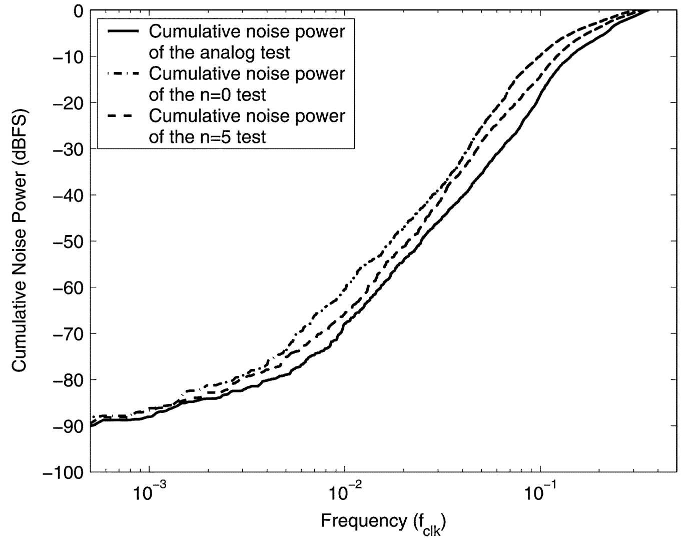

Fig. 18. Cumulative THD+N power plots of the $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator.

73.2 dB. This value is only 2.2 dB lower than that of the analog test.

It is worthy to note that the circuit-simulation results of the analog test are very similar to the normal-mode results of the original DfDT design in [17]. However, the circuit simulations underestimated the performance of the DfDT MUT. The measurement results showed that the DfDT MUT in the normal mode achieved an SNR of 82 dB and a third harmonic below -104 dBFS [17], whereas the corresponding SPICE simulation gave an SNR of about 75 dB and a third harmonic around -72 dBFS. Nevertheless, the circuit-simulation results can be considered as those of a practical design whose in-band white noise is high and linearity is poor.

Fig. 17 shows the output spectra of the digital tests with $n = 0$ and $n = 5$. Consistent with Fig. 16, the shaped-noise power of the proposed $\mathrm{D^3T}$ scheme is also lower than the original DfDT scheme. Once again, it proves that the $\mathrm{D^3T}$ scheme indeed helps in alleviating the shaped-noise correlation, yet their tested SNRs at an OSR of 128 are not much different.

We show the cumulative noise power plots of various tests in Fig. 18 to gain more insights into the test results. Comparing Fig. 18 with 16, the circuit simulations presented 6-dB higher in-band white noise power. The corner frequencies of the spectra at which the shaped noise becomes dominant thereby shift to the higher frequencies. At an OSR of 128, the rated passband is below the corner frequencies. Consequently, the tested SNRs are mainly determined by the in-band white noise rather than the shaped noise. That is the reason why the SNR improvement of the $\mathrm{D^3T}$ schemes $(n \neq 0)$ is not so significant even though they suffer less from the shaped-noise correlation.

2) Testing Nonlinearity: Fig. 19 shows the output spectra of the $\mathrm{D^3T}$ MUT operating in the normal mode. The circuit simulation reported that the MUT in the normal mode has the third and the fifth harmonics of -71.7 and -83.5 dBFS, respectively. However, the test-mode-enabled MUT with a relative input delay of zero, i.e., the original DfDT MUT, failed to reveal the harmonic distortions. The reason of the test's impotence in detecting the harmonic distortion is that the digital stimulus contains significant high-frequency noise which will dither the MUT. As a consequence, the tested harmonic distortion is greatly reduced. Similar dithering techniques are commonly used for $\Sigma-\Delta$ modulators to enhance their linearity [24]–[26].

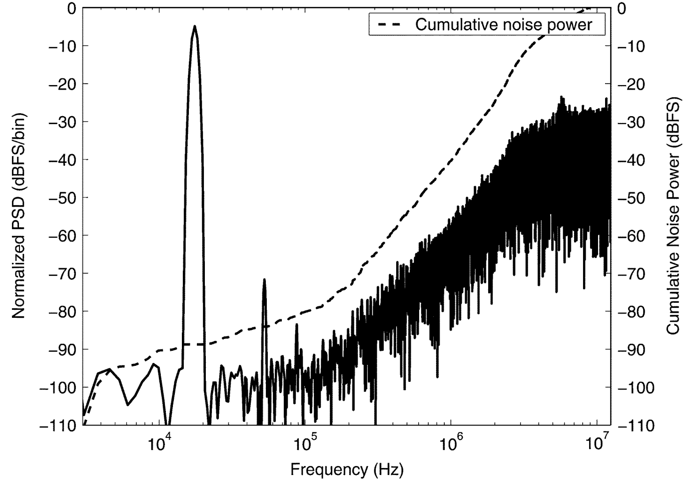

Fig. 19. Output spectrum of the $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator operating in the normal mode with the conventional analog stimulus.

Yet, testing moderate nonlinearity is also a desired goal for us. Refer to Table II, the test setup using $n = 1$ did a good job for testing the nonlinearity although it is not the most suitable one for testing the SNR. Fig. 20 shows the output spectrum. The tested third-harmonic distortion is -75.0 dBFS which differs from the normal-mode result by only 3.3 dBFS. Setting n to other nonzero values also helps. For example, the output spectrum of the digital test with $n = 4$ is shown in Fig. 21. The tested third and fifth harmonics are -77.8 and -86.2 dBFS, respectively. Both are more accurate than the results using the DfDT scheme.

Similar to the discussion of the shaped-noise correlation, it is very difficult to analyze what test setup is the most suitable for testing the nonlinearity. We conducted several simulations with different test setups and found $n = 1$ is a good initial

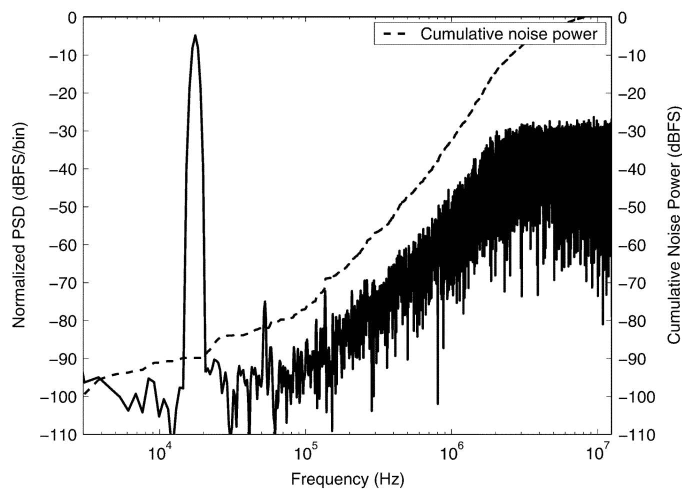

Fig. 20. Output spectrum of the $\mathrm{D}^3\mathrm{T}$ second-order $\Sigma-\Delta$ modulator operating in the test mode with the third-order digital stimulus and a relative input delay of one.

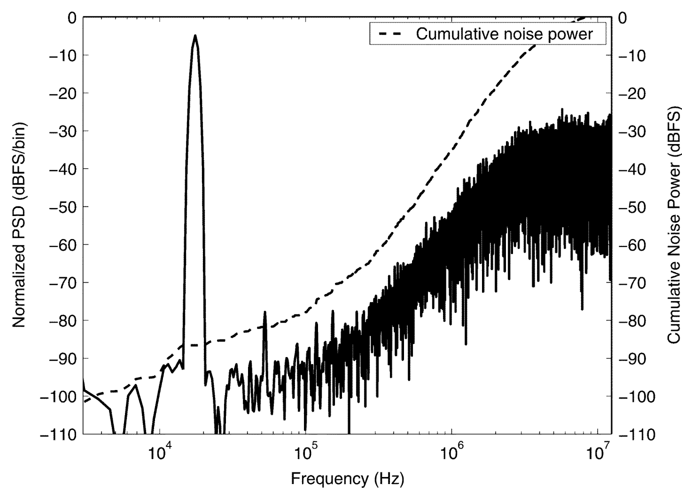

Fig. 21. Output spectrum of the $\mathrm{D}^3\mathrm{T}$ second-order $\Sigma-\Delta$ modulator operating in the test mode with the third-order digital stimulus and a relative input delay of four.

guess. In practical applications, some tests can be conducted in advance to determine the best test setup. Then, we can find out the correlation between the test results of the $\mathrm{D}^3\mathrm{T}$ scheme and those of their analog counterparts for making the final pass/fail decisions.

VI. Conclusion

In this paper, a novel $\mathrm{D}^3\mathrm{T}$ scheme for $\Sigma-\Delta$ modulators to improve their test accuracy with digital stimuli is presented. The input SC network of the MUT in the test mode is decomposed into two or more sub-DCCs that accept the $\Sigma-\Delta$-modulated bit-streams as their stimuli. With appropriate design, the digital stimuli are low-pass filtered by a decorrelating LPF term to alleviate the shaped-noise correlation and MUT overload issues. The behavioral simulations of the second-order $\Sigma-\Delta$ modulator example showed that the test errors of the digital stimuli are no worse than -1.8 dB when the MUT is not overloaded. Even with the -4-dBFS stimulus which severely overloads the MUT, the test error is still no worse than -3.1 dB. Circuit simulations also demonstrated that the $\mathrm{D}^3\mathrm{T}$ scheme has the potential to test moderate nonlinearity. In addition to the high test accuracy, the proposed $\mathrm{D}^3\mathrm{T}$ scheme also achieves the advantages of low hardware overhead, high fault observability, and the capability of conducting at-speed tests in the test mode. The $\mathrm{D}^3\mathrm{T}$ scheme can be easily applied to other kinds of $\Sigma-\Delta$ modulators as well and makes them also digitally testable. Based on the proposed idea, the digitally testable designs in [18] and [27] can be modified to enhance their testing accuracy.

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