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INTERCONNECTION LOSS FROM SUBSTRATE EFFECTS ON LNA PERFORMANCE AND DESIGN ACCURACY

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ABSTRACT: *A 5.2 GHz 0.18-μm SiGe BiCMOS low noise amplifier is implemented with guided-wave interconnections in this letter. These interconnections reduce the substrate skin and proximity effects and hence are suitable for high frequency circuits. The guided interconnections bring 1.7-dB gain and 0.55-dB noise figure enhancement for the low noise amplifier. In addition, accurate and simple design methodology relies on the complete models of components and interconnections when the postsimulation from the rc extraction is not enough for the high frequency circuit design. The measurement results give excellent agreements with the schematic simulation.* © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 144–146, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23968

Key words: *CPWG, interconnection, low noise amplifier, SiGe BiCMOS.*

1. INTRODUCTION

System-on-chip is a dream. All system blocks including baseband circuitry, analog circuitry, and radio frequency circuitry are implemented together on the same wafer. There are many challenges to design radio frequency circuits quickly and accurately. Device modeling is also much tough at higher frequencies and layout parasitics influence circuit performance seriously [1]. Especially, the substrate effect is uncertain and annoying. It results in loss, noise, and coupling [2]. Most dedicated device models are characterized in device level. This is not enough for accurate circuit simulation because of the neglect of the interconnection and substrate effects [3–5]. In the conventional design procedure, it takes much time for iterations between schematic and postlayout simulations. In the postlayout rc extractions, only the metal resistance is involved and, however, the ac resistance from the substrate proximity effect becomes more and more vital at high frequencies. The metal inductance can not be ignorable as well. Therefore, the cell-based modeling and design are proposed in order to reduce design iterations [6]. However, there are many efforts to implement subcircuit cells and to characterize their models.

Coplanar waveguide grounded (CPWG) transmission lines are utilized as guided interconnections to avoid cross coupling between adjacent signal paths and to weaken the substrate effect. Electromagnetic (EM) simulations of the CPWG interconnections are included instead of the rc extraction but the EM simulations demand much computing power as well as consuming much time, especially for more complicated circuits. In fact, the CPWG transmission line model is well established in simulators. The schematic-level circuit can be codesigned with the CPWG library in order to increase simulation accuracy and to speed up the entire design process. In this letter, a 5.2-GHz low noise amplifier is designed with guided interconnections and fabricated using the 0.18-μm SiGe BiCMOS technology. Compared with the unguided low noise amplifier, there are 1.7-dB and 0.55-dB enhancements in gain and noise figure for the guided amplifier, respectively.

2. CIRCUIT DESIGN

For conventional low noise amplifiers displayed in Figure 1, inductors are so large that long interconnections are needed to surround them [7]. However, the conventional layout parasitic extraction only focuses on parasitic capacitance (metal-to-substrate and metal-to-metal capacitance) and resistance (interconnection resistance). The lossy substrate effect like the proximity effect is not included and the metal inductance is not extracted as well, which causes inaccuracy in the postlayout simulation. Namely, L_S,

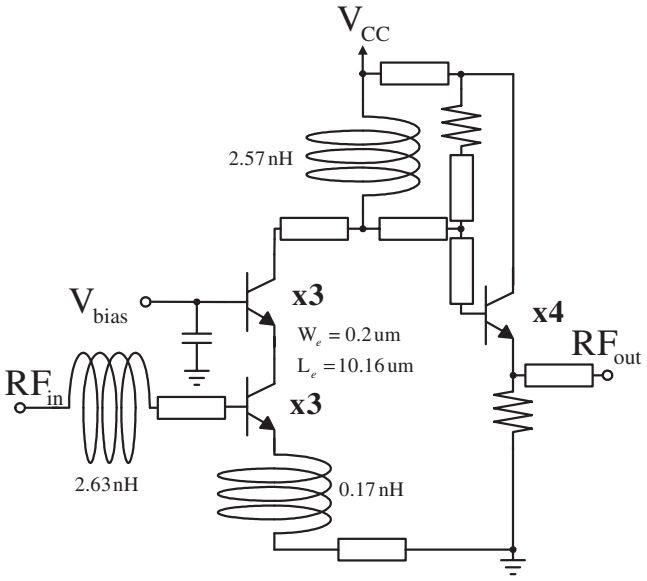

Figure 1 Schematic of a 5.2 GHz low noise amplifier

R_{sub}, and C_{sub} are not taken into considerations, as shown in Figure 2(a). Therefore, the LNA postsimulation is overoptimistic. Here, the grounded shielding shown in Figure 2(b) is added in the design to eliminate the substrate effect. The interconnections are formed by upper metals as the ground planes embrace them as if interconnections form a CPWG transmission line. In the grounded metal layer 1, metal slots are used to avoid metal migration and metal splints are perpendicular to the signal paths for reducing eddy currents. The metal inductance is usually calculated by the EM simulation. Nevertheless, the iterations between schematic and postlayout/EM simulations are a time-consuming job. On the other hand, the schematic simulation is performed with a CPWG interconnection model to design the low noise amplifier. The database of the CPWG had been well established in the simulator so that the presimulation based on the device and interconnection models can foresee the circuit performance accurately. Consequently, the design procedure will speed up without much iteration between layout and postsimulations.

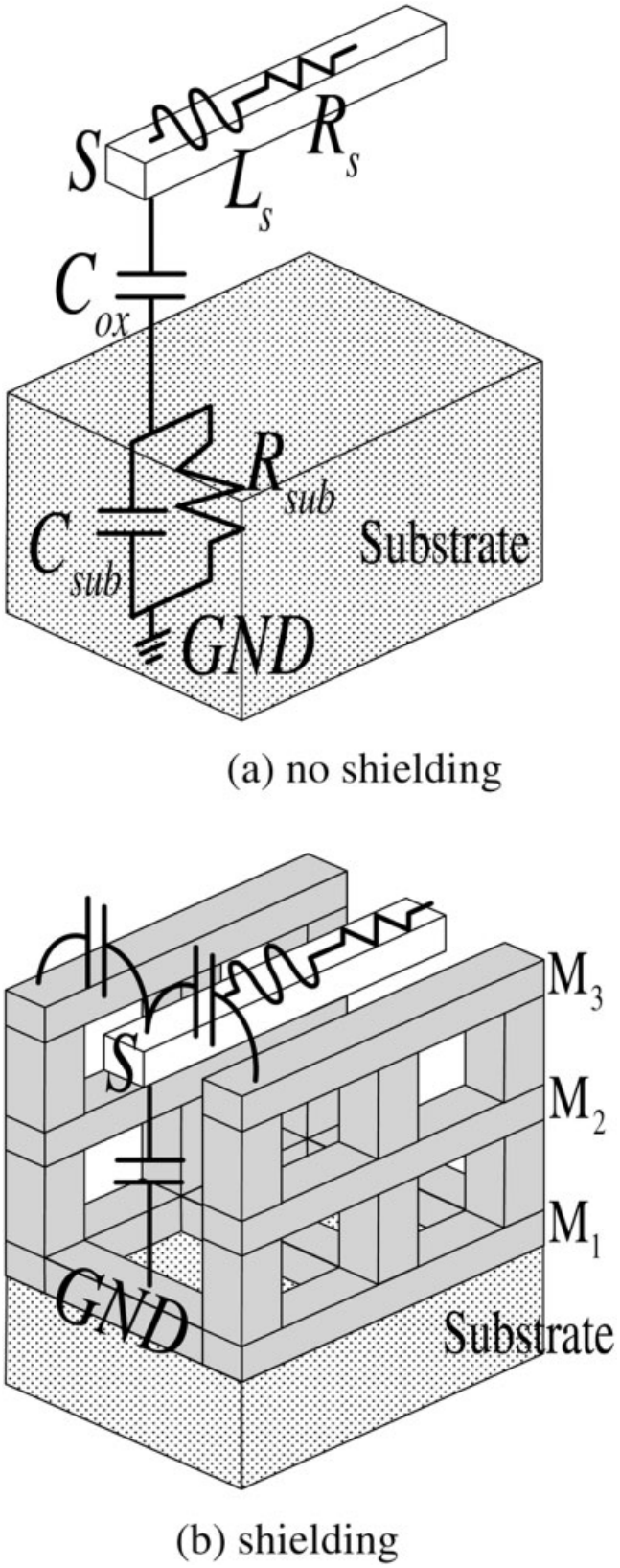

Figure 2 Parasitics of an interconnection

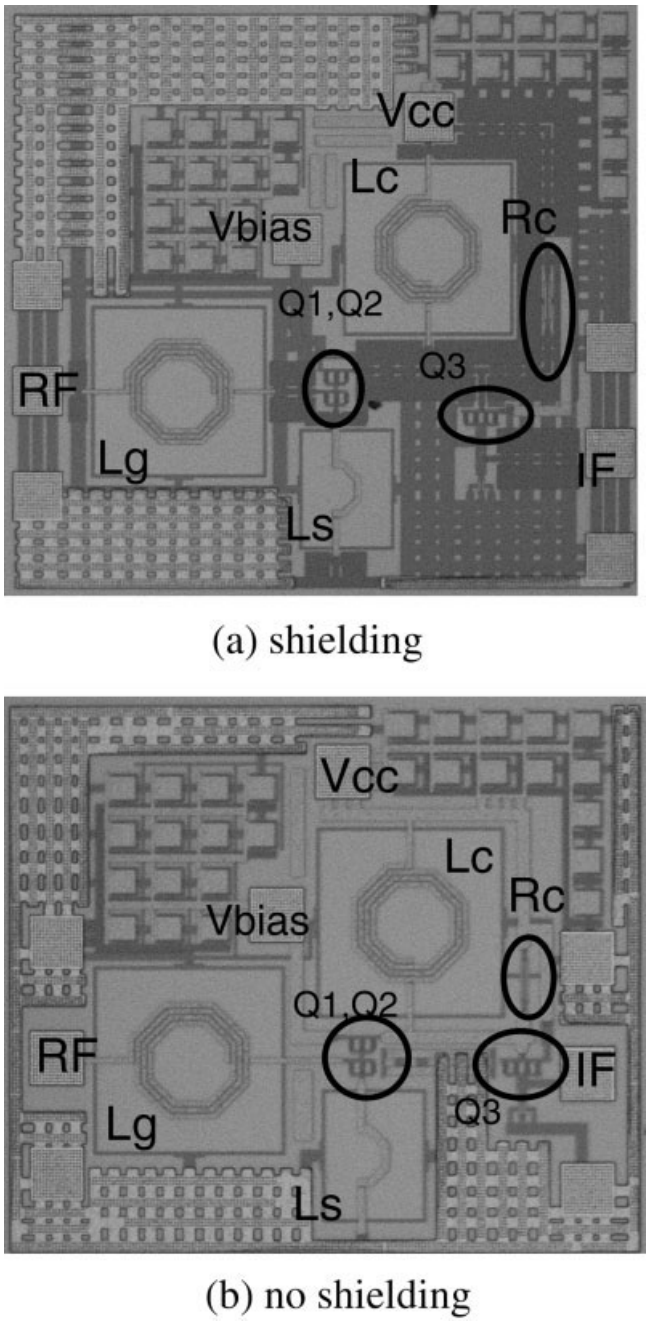

Figure 3 Die photos of the 5.2 GHz low noise amplifiers

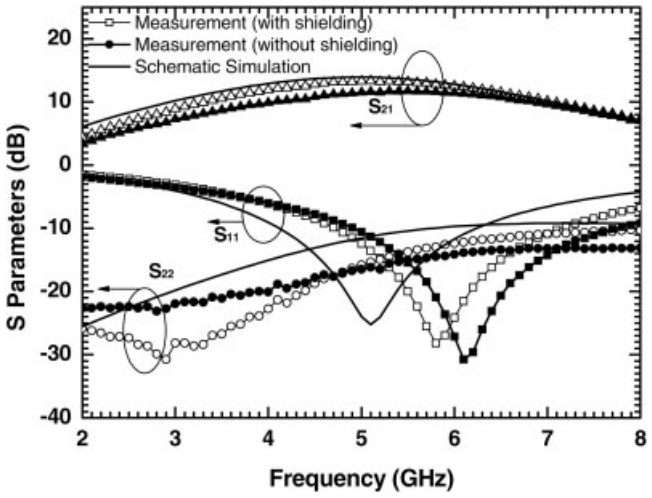

Figure 4 Measured S parameters of the 5.2 GHz low noise amplifiers

3. MEASUREMENT RESULTS

Two low noise amplifiers are fabricated using the 0.18-μm SiGe BiCMOS technology. One has the guided interconnections and the other does not. As shown in Figure 3, the chip size of the guided amplifier is 0.9×0.82 mm^2 and the other has the estate of 0.82×0.71 mm^2. All components (transistors, inductors, resistors, and capacitors) used in both amplifiers are identical. All npn transistors have the emitter width of 0.2 μm and the emitter length of 10.16 μm. The maximum cut-off frequency of those high voltage transistors is about 45 GHz. At 1.8 supply voltage, total current consumption is 4.6 mA. As shown in Figure 4, the gain of the amplifiers with and without shielding is about 13.2 and 11.6 dB, respectively. Figure 5 displays that the guided low noise amplifier has 3.2-dB noise figure and this performance is 0.55 dB better than that of the unguided amplifier. Because the signal is deteriorated by the lossy substrate, the gain and noise figure of the unguided amplifier are downgraded.

The schematic simulation is executed with foundry-provided device models and well-established interconnection libraries, whereas the postlayout simulation is performed from the layout rc extractions. As shown in Figure 5, the deviation between the measured and simulated data due to the skip of the substrate effects in the simulation. For the guided amplifier, the schematic simulation is very accurate thanks due to the substrate shielding even if the substrate effect is not calculated. In this letter, only using device and CPWG interconnection models can simulate the circuit performance accurately. The circuit performance is optimized according to the schematic simulation and this reduces the iterations between layout and postlayout simulations.

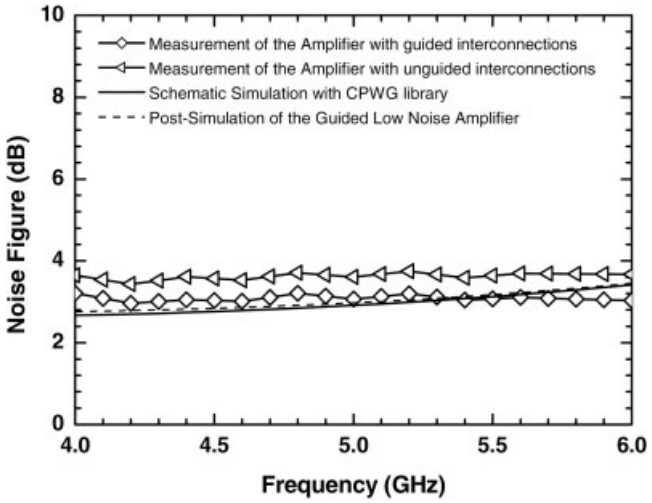

Figure 5 Measured noise figure of the 5.2 GHz low noise amplifiers with and without guided interconnections

4. CONCLUSIONS

This letter designs a 5.2 GHz 0.18-μm SiGe BiCMOS low noise amplifier with guided-wave interconnections according to the schematic-level simulation. Generally, the parasitics are not negligible at high frequencies and the schematic-level simulation hence does not forecast the circuit performances well. However, the interconnections with shielding not only eliminate the substrate skin and proximity effects but also can be easily modeled as a CPWG transmission line. They hence are suitable for high frequency circuit design. In addition, the simple schematic simulation can give excellent agreements with the measurement results accurately, which speed up the design flow. The guided interconnections bring 1.7-dB gain and 0.55-dB noise figure enhancement to the low noise amplifier.

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